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Solution processable multi-channel ZnO nanowire field-effect transistors with organic gate dielectric

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ABSTRACT

The present work focuses on nanowire (NW) applications as semiconducting elements in solution processable field-effect transistors (FETs) targeting large-area low-cost electronics. We address one of the main challenges related to NW deposition and alignment by using dielectrophoresis (DEP) to select multiple ZnO nanowires with the correct length, attract, orientate and position them in predefined substrate locations. High performance top-gate ZnO NW FETs are demonstrated on glass substrates with organic gate dielectric layers and surround source-drain contacts. Such devices are hybrids, in which inorganic multiple single crystal ZnO NWs and organic gate dielectric are synergic in a single system. Current-voltage (I-V) measurements of a representative hybrid device demonstrate excellent device performance with high on/off ratio of $\sim 10^7$, steep subthreshold swing (s-s) of ~ 400 mV/dec and high electron mobility of ~ 35 cm²/Vs in N₂ ambient. Stable device operation is demonstrated after 3 months of air exposure, where similar device parameters are extracted including on/off ratio of $\sim 4 \times 10^6$, s-s ~ 500 mV/dec and field-effect mobility of ~ 28 cm²/Vs. These results demonstrate that DEP can be used to assemble multiples NWs from solvent formulations to enable low temperature hybrid transistor fabrication for large area inexpensive electronics.

1. INTRODUCTION

Solution-based fabrication of field-effect transistors (FETs) using semiconducting ‘inks’ at low temperatures and on large area substrates is an attractive technology for the development of low-cost, lightweight and flexible electronics, including sensors[1], RFID[2], memory elements[3] and displays[4].

Semiconducting single-crystalline nanowires (NWs) are excellent candidates for high performance, low cost electronics due to their high charge carrier mobility, comparable to their bulk single crystalline forms[5, 6]. The NWs small size permits solvent dispersions and subsequent solvent processing on various substrates at room temperature. However, to realistically fulfil the potential of semiconducting NWs as the active channel material in high performance FETs, several key issues still need to be addressed, such as: (i) development of solution-based deposition techniques, offering scalability and integration into industrial fabrication processes; (ii) formation of ohmic contacts on top of NWs to define device channels; (iii) deposition of device quality gate dielectric layers, which must

be fully compatible with low temperature large-area device assembly strategies; (iv) printing of metallic electrodes. In this work we focus on challenges (i), (ii) and (iii). Challenge (iv) related to ink-jet printing of metal nanoparticle inks for source-drain electrodes and significantly reducing the number of photolithographic steps we address in a different part of our investigation[7, 8]. Several NW assembly strategies, including shear force[9], microfluidic flow[6], Langmuir Blodgett[10] and blown - bubble technique[11] offer dense NW-arrays coating on various substrates, including plastics. However, the majority of them do not offer precise NW positioning. Among the various NW assembly strategies developed, dielectrophoresis (DEP) is currently one of the few deposition techniques, offering precise positioning of various nanostructures, including semiconducting/metallic NWs and carbon nanotubes (CNTs), whilst providing high degree of material orientation[12, 13] in respect to charge flow direction. Recently, truly large-area device integration has been demonstrated with DEP positioning of single silicon nanowires over 16,000 electrode sites, although no electrical data has been presented[14].

The performance of nanowire transistors is strongly affected by the gate dielectric. High dielectric constant materials such as Al_2O_3 and HfO_2 which can be processed at low temperatures via atomic-layer-deposition techniques (ALD) are offering low NW transistor gate driving voltages [15, 16]. However, high quality gate dielectric layers, offering reduced source-gated leakage currents still require high temperature annealing ($>500^\circ\text{C}$) thus making these dielectric materials incompatible with plastic substrates [15, 17]. Polymers such as poly(methyl methacrylate) (PMMA) [18], polyimide [19], and self assembly nanodielectrics (SAND) [20] can also be used as gate dielectrics in NW-based solution processed FETs. Although, the multiple process steps needed for SAND[20] formation will be challenging to reproduce over large-area substrates including plastics.

There are very few reports of hybrid NW FETs employing vapour-phase deposited organic gate dielectrics such as poly-para-xylylene (parylene N). This is surprising since parylenes are optically transparent materials with excellent dielectric and barrier properties, including low- k (~ 2.6), high dielectric strength, and good moisture barrier characteristics. The latter can help to mitigate moisture-related device instability issues, including turn-on voltage drift phenomena and hysteresis routinely encountered in NW FETs.

This present work demonstrates DEP NW deposition of solution-suspended ZnO nanowires, where dielectrophoretic process serves three purposes: extraction of nanowires with lengths comparable to transistor channel length from poor quality nanowire powders, alignment of multiple NWs along FET channel and charge transport direction and finally, positioning of these nanowires exclusively on predefined electrode locations to bridge FETs' source and drain. Transistor devices utilize transparent indium-tin-oxide (ITO) source and drain (s/d) electrodes for good near-ohmic contacts to the ZnO NWs. Using the hybrid approach we demonstrate high performance top-gate ZnO NW FETs with polymeric parylene N gate insulator and Au gate electrodes.

2. EXPERIMENTAL

The ZnO NWs used in this work were synthesized via a vapour transport technique[21]. The growth was carried out at $\sim 700^{\circ}\text{C}$ in a quartz tube positioned in a tube furnace. Zn powder (99.999%, Sigma Aldrich) was loaded into alumina boat positioned close to the centre of the growth chamber. Prior to turning the furnace on, the quartz tube was sealed and purged with N_2 ($\sim 1000\text{sccm}$) for $\sim 1\text{hr}$. At a furnace temperature of $\sim 450^{\circ}\text{C}$, the N_2 gas flow was reduced ($\sim 500\text{sccm}$) and O_2 gas ($\sim 4\text{-}12\text{sccm}$) was introduced into the growth chamber. After $\sim 1\text{hr}$ at $\sim 700^{\circ}\text{C}$, the furnace was switched off and allowed to cool naturally. The resulting ZnO NWs appeared as white/grey deposits, which were collected on aluminium foils in the low temperature downstream region of the chamber.

To obtain NW solvent suspensions, aluminium foils were removed from the growth chamber, immersed in methanol and agitated in a sonic bath. During sonication nanowires were released from the growth foils, collected in methanol and formed nanowire dispersions.

The as-prepared ZnO NWs formulations were then drop cast on Si/SiO₂ wafers and carbon grids and were characterized using a combination of scanning electron microscopy (SEM) and transmission electron microscopy (TEM), as shown in Fig. 1 and Supporting information.

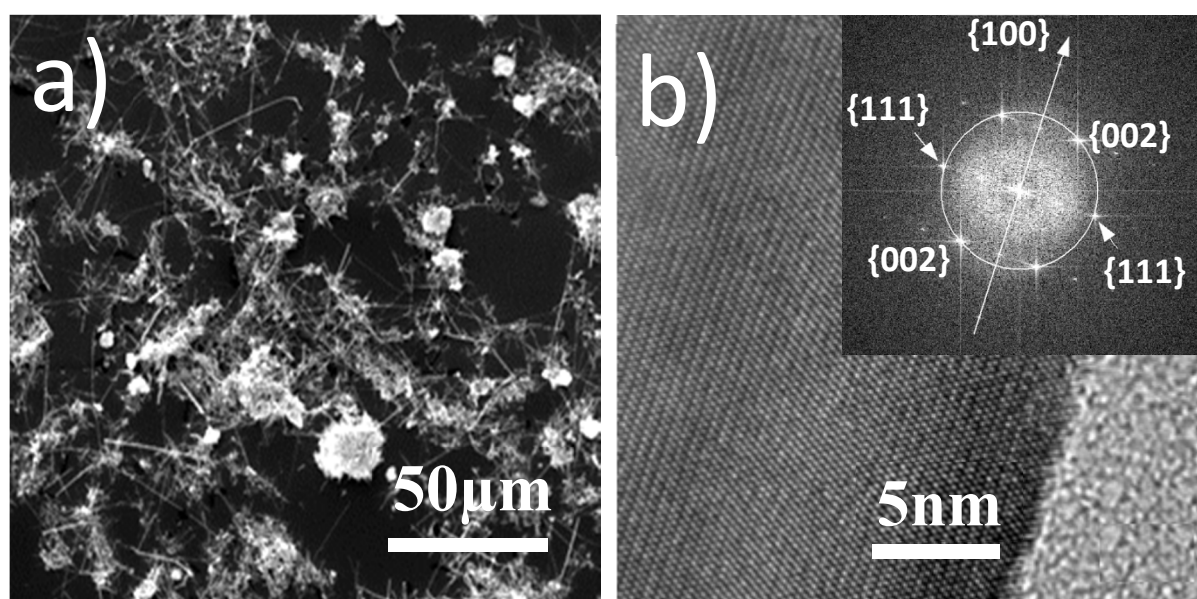


Figure 1 SEM image of a random mesh of ZnO NWs on a SiO₂/Si (n^{++}) substrate, prepared by drop-casting nanowire dispersions. Significant amount of impurities is present in the nanowire powder. b) High resolution TEM image of the ZnO NW supported on amorphous carbon, with the inset diffractogram showing a typical zincite structure. Growth direction is $\{100\}$.

From analysis of several SEM images, as-synthesized typical NW length was determined to range from $\sim 1\mu\text{m}$ to tens of μm long. A significant amount of impurities, mostly ZnO nanocrystal material has been observed. The high resolution TEM (HRTEM) image of a representative ZnO NW in Fig. 1b revealed the typical structure of a highly crystalline material. The diffractogram of the image was used to assign crystallographic direction families and to identify the growth direction $\{100\}$.

Low resolution TEM images (Supporting information) were used to determine the mean ZnO NW diameter to be ~120nm.

ZnO NW FETs in this work were assembled on low-sodium glass substrates as top-gate devices with a 300nm thick vapour-phase deposited parylene N as the gate dielectric, as shown in Fig. 2. ITO electrode structures were first patterned on the glass substrates via photolithography (lift-off) and these served as DEP alignment electrodes. The dielectrophoretic nanowire deposition process began with the application of an AC field across two parallel electrodes. To ensure that ZnO NW droplet solutions were confined to a small area, substrates were pre-treated with octyltrichlorosilane (OTS, ~1mMol in toluene) self-assembled monolayer, which rendered substrate surfaces hydrophobic. ZnO NWs dispersions in methanol (~10 μ L droplets) were placed over electrode gap area, where external alternating voltage potential of 10V_{peak-to-peak} and sinusoidal frequency of 16 KHz was applied by PSM1735 Numetriq impedance analyser. After the DEP process, excess solution was absorbed by a tissue. Typically, several ZnO NWs (~5-20NWs) were observed bridging the gap between the electrodes (Fig. 2a). Notably, nanowires were deposited preferentially in the electrodes gap perpendicular to the device electrode edges, with minimal amount of non-nanowire impurities.

To improve the s/d contact properties to ZnO NWs, a second photolithographic (lift-off) step was performed to pattern additional ITO contacts on top of aligned nanowires. At this stage all-round contacts were formed on the ends of the NWs and this ensured that carrier injection can occur over the entire NW regions sandwiched between the top and bottom ITO contacts. However, whilst this step was essential to improve contact properties to the ZnO NWs, it also resulted in the removal of several ZnO NWs from the channel due to poor nanowire-electrode adhesion during the lift-off process. Nonetheless, several ZnO NW FETs with multiple nanowires in the channel area were fabricated and characterized. Device fabrication yield was noted in more detail for Si nanowires FETs (not shown in this paper) produced with the same deposition process. Typically ~85% fabrication yield was obtained. With ZnO NW devices produced in this work we observed similar fabrication yield.

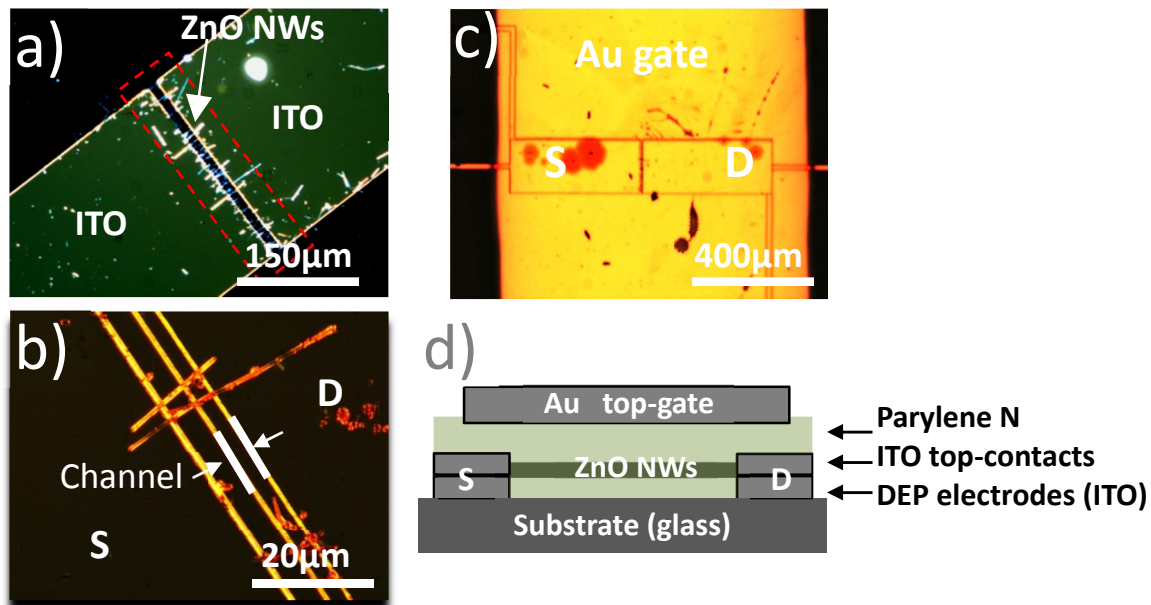


Figure 2 Polarized optical microscope images of: a) DEP assembled ZnO NWs on top of ITO alignment electrodes, positioned perpendicular to the edges; b) device channel at high magnification with visible edges of DEP electrodes and ITO top contacts. Due to a misalignment of photolithographic mask process, edges of top and bottom electrodes are shifted by few microns. c) Optical image of a completed device. d) Schematic cross-section of the device.

To complete the hybrid devices, substrates were transferred to a custom built parylene N deposition chamber consisting of a horizontal tube furnace with two separate heaters, and $\sim 300\text{nm}$ thick layers were deposited. The vapour deposition began with the sublimation of the raw material (diparaxylylene) at $\sim 150^\circ\text{C}$ in low vacuum ($\sim 0.1\text{torr}$). In the gaseous state, at 650°C the dimer decomposed to form gaseous monomers (para-xylylene). The monomers condensed and polymerised in the sample part of the deposition chamber maintained at room temperature, and transparent polymer films (poly-p-xylylene) were formed. Unlike solution based polymer dielectrics [18, 19], parylene N films were conformal, filling all topological voids around NWs. Following deposition of dielectric layers, a $\sim 60\text{nm}$ thick Au gate strips were thermally evaporated (Kurt J. Lesker) via shadow mask to overlap the device channels. Current-voltage (I-V) measurements of the devices were first performed in dry N_2 glovebox immediately after fabrications and later in ambient air, following 12 weeks ambient air exposure of the fabricated devices. Electrical measurements were performed on a home built probe stage using a semiconductor characterisation system (Keithley 4200).

3. RESULTS AND DISCUSSION

3.1 Dielectrophoretic nanowire alignment

The DEP is a process that can be understood as the motion of uncharged, polarizable particles in non-uniform electric fields.[14, 22, 23] The DEP force arise from the interaction between an electric field (generated by electrically driven parallel electrodes) and the dipole induced in particles[14]. Whilst the magnitude and direction of the DEP force exerted on a nanowire (\mathbf{F}_{DEP}) is difficult to determine

precisely for an arbitrary shape such as a nanowire, previous work have shown that such particles can be approximated to a prolate ellipsoid with long radius a and short radius b . The expression for \mathbf{F}_{DEP} experiencing a gradient in electric field strength ∇E^2 in a medium with permittivity ε_m , is given by[23]:

$$\mathbf{F}_{\text{DEP}} = \frac{2\pi ab^2}{3} \varepsilon_m \text{Re}[K(\omega)] \nabla E^2 \quad (1)$$

The term $\text{Re}[K(\omega)]$ refers to the real part of the Clausius Mossotti factor, a measure of the relative polarisability of particle and medium. For an ellipsoid,

$$K(\omega) = \left[\frac{\varepsilon_p^* - \varepsilon_m^*}{\varepsilon_m^* + A(\varepsilon_p^* - \varepsilon_m^*)} \right] \quad (2)$$

where $\varepsilon^* = \varepsilon - j\sigma/\omega$, ε is permittivity, σ is conductivity, $j = \sqrt{-1}$ and ω angular frequency, the subscripts m and p refer to the particle and medium respectively, and A is a shape factor that tends to zero for high aspect ratios. $\text{Re}[K(\omega)]$ is frequency-dependent and can take positive and negative values, corresponding to movement up and down the field gradient respectively.

DEP has several advantages for the selective manipulation of nanowires. On one hand, long nanowires are preferentially attracted over small debris because of their greater volume, and even if debris attracted it rarely bridges the inter-electrode gap. Since a stronger dipole can form along the longest axis of the particle it will also align itself with the electric field lines and thereby preferentially bridge the inter electrode gap. Secondly, since single crystalline particles have a higher specific conductivity than the polycrystalline debris, a pure single crystalline particle will be the more polarizable and thereby experience maximum force over a greater frequency range; since the significance of the conductivity in the term decreases with frequency, it is clear from Equation (2) that a particle with a higher conductivity will experience positive (attractive) DEP at higher frequencies than a less conductive particle. This allows the assembly process to be optimized by selecting a frequency that attracts only the most conductive particles while repelling the less conductive particles. Crystal defects in a particle decrease the specific conductivity of the particle. So the purest nanowires should have the highest specific conductivity while amorphous or polycrystalline particles have a lower specific conductivity. This allows selecting a frequency where pure nanowires are attracted preferentially, allowing the assembly of high quality devices.

3.2 Nanowire transistors

Fig. 3 shows measured electrical transport data (in N_2 ambient) for a representative hybrid ZnO NW FET containing ~ 7 nanowires in the channel area. From the experimental data, it can be seen that the device demonstrates n-channel enhancement mode characteristics corresponding to the positive range of bias voltages. The family of transfer scans (Fig. 3a) also reveals an incremental increase in I_D with increasing V_D (from 2V to 10V), suggesting that the device demonstrated good gate-to-channel coupling, not significantly influenced by s/d contact related issues such as Schottky barriers. The output scans (Fig. 3b) further reveal good gate-channel modulation with near-ohmic behaviour at low V_D . This is not surprising since the ITO work function of ~ 4.4 - 4.5 eV is closely matched to ZnO conduction band edge (~ 4.5 eV) to enable near-ohmic contact.[24, 25]

From the family of transfer scans, device parameters, including threshold voltage (V_T), on/off current ratio, sub-threshold swing $s - s = \log_{10} [I_{on}/I_{off}]$, transconductance $g_m = \partial I_D / \partial V_G$ and field-effect mobility (μ) were extracted. From transfer characteristics linear regime, the device V_T was evaluated to be $\sim -4.8 \pm 0.6$ V. The devices also exhibited low off-currents (~ 3 pA) and high peak currents ($\sim 43 \mu$ A at $V_G = 30$ V), corresponding to on/off ratio close to 10^7 . The extracted off-currents, on-currents and on/off current ratio attained by the device were found to be better than majority of reported data for single ZnO NW FET structures employing various organic dielectric, including 15nm organic nanodielectric layers [18, 20]. Moreover, these parameters are also significantly better than reported data for DEP assembled multiple ZnO nanowire channel FET structures with SiO_2 gate dielectric layers [12, 26]. Another critical device performance parameter is the s-s value, described by $\frac{kT}{q} \times \ln 10 \times \left[\frac{C_T + C_i}{C_T} \right]$, where C_T is the gate coupling capacitance and C_i represents the components of capacitances due to interfacial states and parasitic effects.[25]

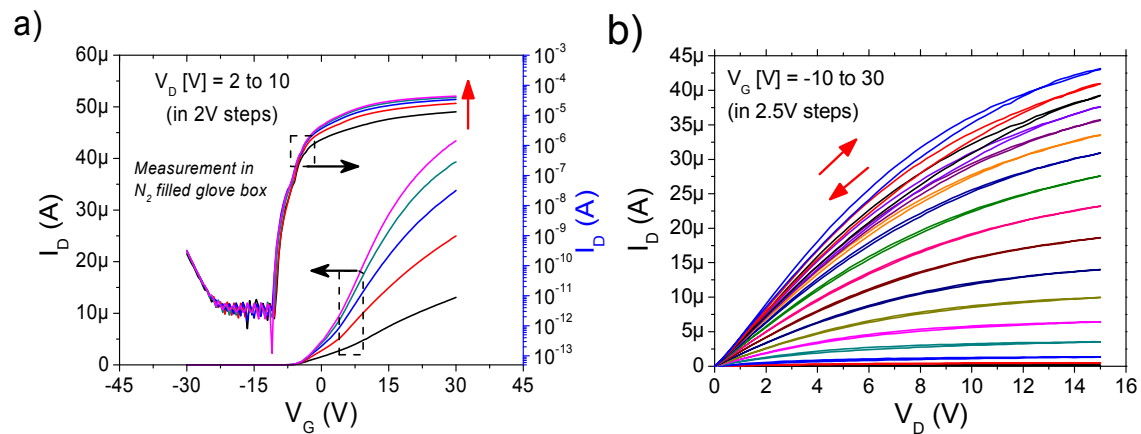


Figure 3 N_2 ambient I-V data for a hybrid ZnO NW FET with channel length $L = 5 \mu$ m and NW density = 7NWs. a) Family of transfer scans at $V_D = 2$ V to 10V, in 2V steps. b) Family of output scans for V_G stepped from -10V to 30V in 2.5V steps. Both forward and reverse scans are plotted. Arrows indicate the direction of voltage scan. g_m for this device was evaluated to be $\sim 2 \mu$ S at $V_D = 10$ V.

For low power applications, low $s-s$ is essential (~ 60 mV/dec, theoretical limit) and this can only be achieved for small C_i . From Fig. 3a, $s-s$ in the present device was calculated to be ~ 400 mV/dec, which is comparable to those of state of the art poly-Si FETs (~ 200 mV/dec) [6] and is significantly better than organic and α -Si FETs, which typically show $s-s$ from 1 V/dec to several volts per decade.[4] Such low $s-s$ value attained by the present hybrid device points to the excellent ZnO NWs-parylene N interface characteristics, with low density of interface states and/or effective encapsulation of the ZnO NW channel from ambient species, including moisture and oxygen. These species were collectively linked to device instability issues, including poor carrier mobility, degradation in output currents and hysteresis behaviour in NW FETs and CNT FETs [27-29]. Ambient instability of ZnO has been ascribed in the literature to the adsorption of oxygen on ZnO surface which depletes the surface of electrons, leading to positive V_T shifts in ZnO NW based FETs. [30] Song et al [31] presented some evidence of single ZnO NW FET sensitivity to ambient air, in which positive V_T shifts and degradation in I-V curves were observed after devices were exposed to ambient air. The authors demonstrated that passivation of the ZnO NW surface with PMMA can offer a more stable device operation.

To assess the stability of our devices to atmospheric conditions, we measured the same hybrid multi-channel ZnO NW transistors in normal lab conditions following 12 weeks exposure to air environment.

Fig. 4 shows the experimental transfer and output scans in air for the hybrid top gate device. From the data in Fig. 4a obvious features to note are as follows: (i) the clear increase in I_D at positive V_G suggests that the device is still operating as an n-channel enhancement mode; (ii) the device exhibits high gate-to-channel modulation with incremental increase of V_D . The family of output scans at the different V_G biases (Fig. 4b) demonstrates near-linear I_D - V_D relationship at low V_D , weakly saturating at high V_D .

From the transfer scans in Fig. 4a, we extracted the off-current, peak-current and on/off current ratio to be 5pA, $\sim 22\mu\text{A}$ and $\sim 4 \times 10^6$, respectively. These parameters agree well with those attained by the device in N_2 ambient thus demonstrating good stability of the device under atmospheric air conditions. We do however acknowledge that the progression of the output scans (Fig. 4a) at the different V_G in ambient air does reveal small degradation (approximately a factor of 2 lower) in I_D compared to that in N_2 ambient conditions (Fig. 3b) at $V_D = 10\text{V}$. This decrease in I_D may be explained by (i) an increase in the ITO resistivity (due to reduction in oxygen vacancies) at the exposed contact pads used for electrical probing of the hybrid device. (ii) Adsorption of small amount of electronegative ambient species which can deplete the ZnO surface of residual charge. The latter situation can lead to upward band bending of the of the ZnO NW conduction and valence band edges, resulting in a positive V_T shifts since additional gate voltage will be required to re-establish flat-band conditions at the ZnO-parylene N interface. Notably, the consecutive transfer scans at the different drain voltage potentials initially showed positive threshold voltage shift of $\sim 2.5\text{V}$ (V_T from -2.6V at

$V_D = 2V$ to $-0.1V$ at $V_D = 4V$) followed by a gradual negative voltage shift, finally stabilising at $V_T = -0.6V$ at $V_D = 10V$. However, additional scans showed no significant changes to the transfer curves. These results are demonstrating that top-gate deposition effectively provides FET channel passivation and reduction of ambient induced instabilities which can result in excessive V_T shifts and significant degradation in key transistor performance metrics.[31]

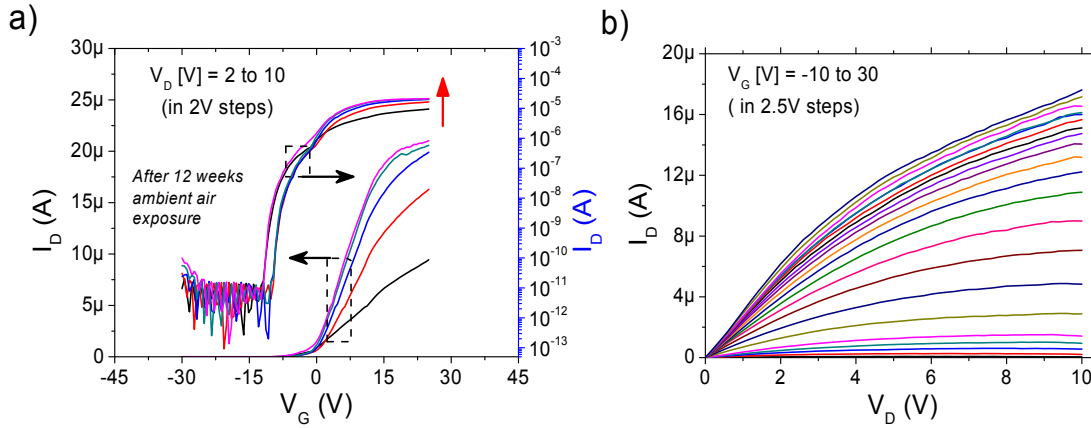


Figure 4 I-V characteristics for the hybrid top-gate device following 12 weeks ambient air exposure. a) Family of transfer scans in linear-linear and log-linear scale at $V_D = 2V$ to $10V$, in $2V$ steps. b) Output scans for the device at $V_G = -10V$ to $30V$ (in $2.5V$ steps).

Unlike conventional thin-film transistors, composed of thin semiconductor films, the lack of extended device geometry in NW FETs leads to large parasitic capacitance resulting from electrostatic fringing of the gate field acting on the cylindrical-like nanowires. As a result, carrier mobility (μ_{eff}) in NW FETs is typically calculated using the cylinder-on plate model (Eq. 3) and the MOSFET model in the linear regime (Eq. 4).[6, 20, 29]

$$C_T = N \times \frac{2\pi\epsilon_0\epsilon_r L}{\cosh^{-1}\left(\frac{r+d}{r}\right)} \quad (3)$$

$$\mu_{eff} = g_m \times \frac{L^2}{V_D \times C_T} \quad (4)$$

where C_T is the coupling capacitance, N is NW density (7 ZnO NWs), ϵ_0 is absolute permittivity ($\sim 8.85 \times 10^{-12}$ F/m), ϵ_r is parylene N dielectric constant (~ 2.6), L is channel length (taken as the separation between the source-drain, $\sim 5\mu m$ in the present device), r is average NW radius ($\sim 60nm$) and d is dielectric thickness (300nm). For the present device, we estimated C_T to be $\sim 2fF$; assuming channel geometry is seven 120nm diameter ZnO NWs connected in parallel. With the estimated C_T and the calculated g_m values in both N_2 and under atmospheric conditions ($\sim 0.5\mu S$ and ~ 0.4 at $V_D=2V$, respectively), effective carrier mobility (μ_{eff}) was deduced to be ~ 35 cm^2/Vs (N_2) and $28cm^2/V-s$ (air) at $V_D = 2V$. Note that the calculated μ_{eff} values represent the lowest estimate of the actual mobility because the cylinder-on-plate model (Eq.3) only describes an ideal capacitor composed of two perfect conductors (a cylinder and infinite plate conductors) imbedded in a perfect

dielectric medium. So, the model does not describe fully the complex relationship between charge carrier density vs. V_G and the model does not account for bulk/interfacial charges on both side of the channel (glass-ZnO NW and insulator-ZnO NW interfaces). Nonetheless, the μ_{eff} values are significantly better than reported data elsewhere for hybrid ZnO NW FETs employing various organic gate dielectrics with mobility 1.6-4 cm^2/Vs [18, 32] and significantly higher than those of typical organic and α -Si FETs ($\sim 1 \text{ cm}^2/\text{Vs}$). We do however acknowledge that key device parameters, including μ_{eff} , V_T and $s-s$ are largely independent of NW density except device output currents, which was shown to increase linearly with ZnO NW density in device channel.[33] Therefore we expect that device reproducibility and predictability of our hybrid NW FETs, targeting complex circuitry in future applications can be significantly enhanced by increasing NW concentration in solution suspension. This will enable higher density of NWs to be assembled using DEP alignment process, enabling consistent device output currents. Our preliminary results show that it is possible to trap a larger number of nanowires, close to 50 in the $200\mu\text{m}$ wide FET channel, thus improving reproducibility of nanowire transistors and minimising the influence of small statistical variations of number of nanowires during DEP process.

4. CONCLUSIONS

Single crystalline ZnO NWs were synthesized using a vapour transport method, then transferred in methanol and were preferentially deposited between indium-tin-oxide alignment electrodes on substrates using dielectrophoresis. Well aligned ZnO NWs were then used as charge transport channels in hybrid top-gate ZnO NW FETs with near ohmic ITO top source-drain contacts and polymer gate dielectric layers. Room temperature current-voltage measurements performed on devices in both N_2 and also in ambient air after 12 weeks air exposure showed n-channel enhancement mode type FET characteristics with excellent performance metrics, including high on/off current ratios of 10^7 and 4×10^6 , steep subthreshold swing of 400 mV/dec and 500 mV/dec, and field-effect mobility of $\sim 35 \text{ cm}^2/\text{Vs}$ and $28 \text{ cm}^2/\text{Vs}$, in N_2 and air conditions respectively. This work has demonstrated that high performance ZnO NWs can be assembled using low-cost solution assembly based nanowire positioning strategies in predefined locations and that high on/off ratio and mobility can be achieved in devices using plastic components, including polymeric gate dielectric layers for future electronic systems on plastic substrates suitable for printed electronics applications.

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