High-κ dielectrics on germanium for future high performance CMOS technology

by

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A thesis submitted to

Department of Electrical Engineering and Electronics

In The University of Liverpool

In partial fulfillment of the requirements

For the degree of

Doctor of Philosophy

September 2015

Abstract

Traditional silicon CMOS scaling has approached its limits due to the high leakage current induced by the reduction of the silicon-dioxide gate oxide thickness. Thus, high permittivity dielectric is suggested to replace SiO_2 to achieve low gate leakage current while maintaining the same capacitance. Moreover, high mobility materials are being considered to replace Si as channel materials motivated by the requirement for higher drive current and faster switching speed of MOSFETs. Germanium (Ge) has attracted much attention as a channel material, attributed to its high hole and electron mobility. Overall, it could be concluded that a high-κ dielectric for the Ge gate stack could be an effective solution for future CMOS technology which could resolve these two concerns. However, surface passivation between the material high-κ and the Ge channel is a major challenge for this solution. Direct deposition of a high-κ dielectric on Ge suffers from a low-quality interface. The native oxide, GeO_2 has been found to form a good interfacial layer on Ge before the deposition of a high-κ dielectric. Two methods are introduced in this work, to passivate the interface. Electrical and XPS characterization is employed to investigate the property of the interface.

Several admittance behavior issues related to Ge-based MOS capacitor could lead to errors in the extraction of the interface state density using the conventional *C-V* or *G-V* based methods. The availability and scope of these methods are studied in details when applied on the Ge-based MOS capacitor. Three issues related to the conductance method as a preferable method are explored.

A conduction band notch which represents a potential charge trapping site may exist at the interface between the interfacial native GeO_2 and high-κ dielectric layer in a Ge MOSFET gate stack. It could induce threshold voltage instability. The number of electrons and its induced threshold voltage is calculated and the main conclusion is that charge storage in this notch is insignificant at the relevant technology node.

The low frequency response of the capacitance voltage characteristic is observed for the Ge-based MOS capacitor in the inversion region, even at high frequency. It is considered to be the result of the fast minority carrier generation response. The extraction of activation energies through temperature measurement indicates that the thermal generation process is responsible for the generation of minority carriers at room temperature. The minority carrier generation life time is measured to model the thermal generation in the depletion region for Ge-based MOS. The frequency dispersion apparent in the accumulation regime of *C-V* plots for Ge-based MOS is considered to be caused by oxide traps within the oxide layer. A model is employed to estimate the oxide trap concentration. It is demonstrated that the oxide traps are distributed non-uniformly over both oxide depth and energy level.

Acknowledgements

The accomplishment of this study is not possible without the support from many individuals. Firstly, I would like to take this precious opportunity to express my sincerest gratitude to my primary supervisor, Professor Steve Hall, for all his guidance and support during my last 4 years study. I am particularly impressed by his deep insights and his vision on numerous potential research areas. His continuous encouragement and useful suggestions play an important role on my research.

In addition, I would like to thank Dr Naser Sedghi. I have learned a lot from his extensive knowledge and experience. He is always patient and friendly to provide a lot useful advices and help for my study.

During my Ph.D., I felt quite fortunate to interact and collaborate with some great individuals I also acknowledge Sean Mather for his sample fabrication for my research and Althobaiti, Mohammed for his XPS measurements. I am also grateful to Dr Jidong Jin, Don Weerakkody, Andrew Shaw and Ibrahim Nemr Noureddine in our office. Working with them was very fruitful and enjoyable.

I would like to thank all my friends during my life in Liverpool including Chen Lu, Teng Ma, Long Yan, Lin Liu, Chenhao Wei, Fei Yang, Chaowei Liu, Jie Zhu, Zhe Yang, Yue Li, Shaonan Zhang, Kevin, Anna, Yang Li, Ziwei Zhang, and Chen Li.

Finally, I would like to give my special thanks to my families and wife for their continuous support and love.

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Chapter 1 Introduction and literature review

This chapter firstly illustrates the main ideas behind the introduction of high-κ gate dielectric oxide on the high mobility Ge (germanium) channel for the future development of complementary metal oxide semiconductor (CMOS) technology. An outline of the thesis is presented here together with a literature review into surface preparation procedures suitable for the semiconductor substrates investigated in this thesis.

The Metal-Oxide-Semiconductor Field-Effect Transistor (MOSFET) is the vital component in complementary MOSFET technology and the driving force in the field of the semiconductor industry over the past decades. The continuous down-scaling of MOSFETs following Moore's law which describes the number of transistor on an integrated circuit increases exponentially by doubling every 2–3 years, has contributed to an unprecedented revolution in semiconductor devices over the past several decades [1]. Nowadays, the number of transistors in one microprocessor can be over 1 billion, with faster operation speed, lower power consumption and, most importantly, less cost than early stages [2].

1.1 Scaling rules

The ideal scaling guideline was proposed by Dennard *et al* and is referred to as constant-field scaling [3]. Constant-field scaling allows scaling of the device voltage, the device dimensions (gate length L, channel width W, junction depth x_j, thickness of oxide t_{ox} and doping concentration N_d or N_a) by the same factor k, so that the electric field E remains unchanged as shown in Fig. 1.1. Based on this guideline, the performance of the device indicated by reduced delay time τ, increased number of transistor n and decreased power dissipation per transistor can improve without increasing power density (nP/A) by dimensionally scaling the device as indicated in Table 1.1.

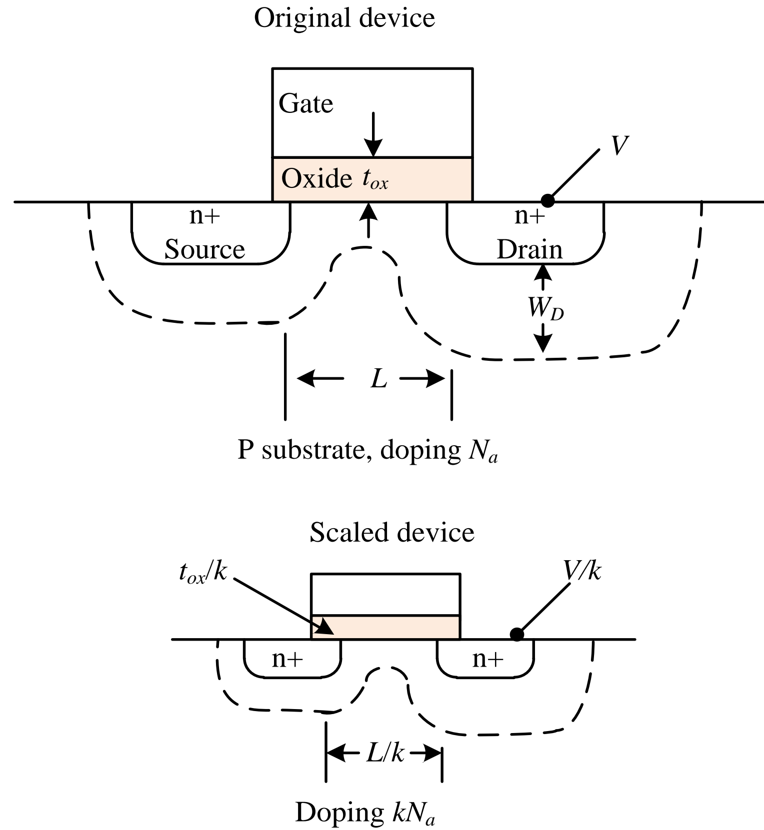

Fig. 1.1. Principle of nMOSFET constant-electric field scaling (After Dennard, 1986 [3]).

Table 1.1. Scaling of the MOSFET device and circuit parameters [4].

	MOSFET Device and Circuit Parameters	**Multiplicative Factor (k > 1)**
Scaling assumption	Device dimension (t_{ox}, L, W, x_j)	$1/k$
	Doping concentration (N_a, N_d)	k
	Voltage (V)	$1/k$
Derived scaling behavior of Circuit parameters	Electrical field (E)	1
	Circuit delay time ($\tau \sim CV/I$)	$1 / k$
	Oxide capacitance (C_{ox})	$1 / k$
	Power dissipation per transistor ($P \sim VI$)	$1 / k^2$
	Number of transistor per area (n/A)	k^2
	Power density (nP/A)	1
	Current, drift (I)	$1 / k$

1.2 High-κ oxide materials

However, in recent years further scaling down of MOSFETs has become problematic due to the limitation of silicon dioxide (SiO_2) gate oxide thickness t_{ox}. The native oxide, SiO_2 plays a key role in the successful CMOS development, due to several superior properties namely high electrical quality of the Si/SiO_2 interface, thermal and chemical stability, insulating properties and large band gap [5]. The reduction of SiO_2 oxide thickness following aggressive dimensional scaling eventually leads to increasing leakage current which is induced by a quantum mechanical tunneling process [6]. The thickness of SiO_2 gate oxide has reached around 1.1 nm which leads to an exponential increase of gate leakage current exceeding 1 A/cm^2 at 1 V, as shown in Fig. 1.2 with associated degradation of the electrical performance of the device due to the unacceptable static power dissipation. Moreover, such thin films can result in problems for the reliability of the device [7-9].

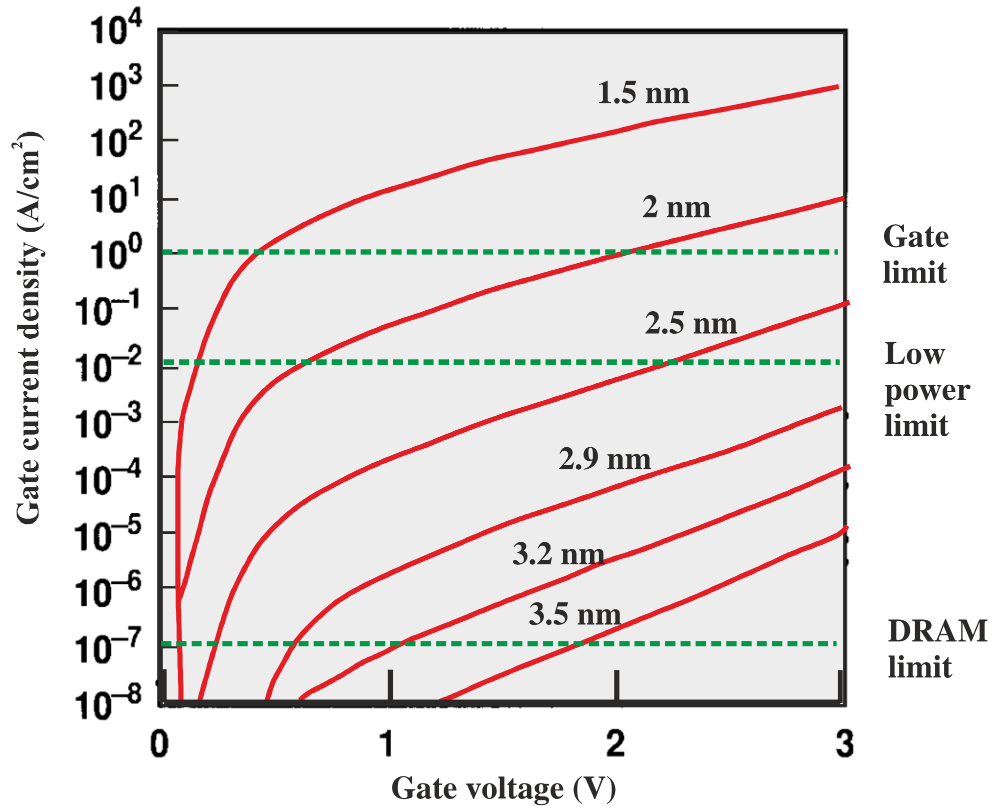

Fig. 1.2. Leakage current vs voltage for various thicknesses of SiO_2 layers after Robertson *et al.* [10].

Scaling is still the mainstream road to improve the performance of the device in the future, thus this concern was suggested to be resolved by replacement of SiO_2 with a dielectric material with higher permittivity ε_κ (high-κ).

The capacitance per unit area for high-κ gate oxide is given by:

$$C_{high-\kappa} = \frac{\varepsilon_{\kappa}\varepsilon_0}{t_{\kappa}} \tag{1.1}$$

where ε_0 is the vacuum permittivity, t_κ is the thickness of high-κ gate oxide.
The equivalent capacitance for SiO_2 gate oxide is given by:

$$C_{SiO_2} = \frac{\varepsilon_{SiO_2}\varepsilon_0}{t_{EOT}} \tag{1.2}$$

where ε_{SiO2} is the relative permittivity of SiO_2. The equivalent oxide thickness, t_{EOT} is defined as the thickness of SiO_2 oxide which is needed to obtain the same capacitance density as the high-κ oxide used.
Then, if the same capacitance is needed:

$$C_{SiO_2} = C_{high-\kappa} \tag{1.3}$$

The equivalent oxide thickness (EOT) can be given by:

$$t_{EOT} = \frac{\varepsilon_{SiO_2}}{\varepsilon_{\kappa}} t_{\kappa} \tag{1.4}$$

Because the permittivity of high-κ oxide is higher than that of SiO_2, the use of high-κ as the gate oxide allows an increase in thickness of the oxide, thus greatly reducing the leakage current while maintaining the oxide capacitance C_{ox}. For instance, the 1.2 nm SiO_2 oxide can be replaced by a thicker, high-κ (3.0 nm) to achieve the same capacitance as shown in Fig. 1.3. Therefore, there is a tremendous research effort concentrated on high-κ dielectric as a replacement of silicon dioxide for future CMOS technology [10].

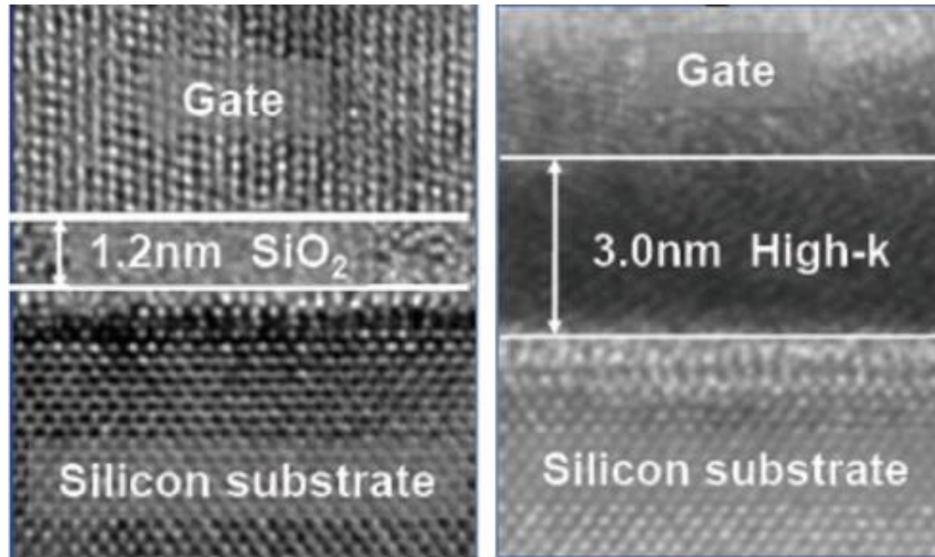

Fig. 1.3. The high-κ oxide replaces silicon oxide [10].

In terms of choosing the correct high-κ material, there are several criteria [10]. Firstly, the value of κ should be higher than 12, the preferable value is between 25 and 35. Larger κ is more beneficial to achieve a thicker high-κ oxide while maintaining the same capacitance as

discussed. Secondly, HfO_2 based materials have been regarded as the most promising high-κ material due to its high permittivity value and thermal stability [10]. In addition, the energy band offsets between high-κ and semiconductor have undergone considerable scrutiny, because a high potential barrier at each band is imperative to prevent conduction by the emission of electrons and holes into the oxide bands. Materials such as Al_2O_3, ZrO_2, HfO_2, Y_2O_3, La_2O_3 could satisfy such requirement [10]. HfO_2 was envisioned as a promising high-κ material in both academic and industry. Intel introduced HfO_2 as the gate oxide in the 45 nm technology node.

1.3 High-mobility channel material Ge

Germanium recently has been considered as a promising alternative channel material, primarily due to its higher hole (3900 $cm^2 V^{-1} s^{-1}$) and electron mobility 1900 $cm^2 V^{-1} s^{-1}$ than Si, as shown in Table 1.2. It is being considered to replace Si in the channel of a MOSFET to achieve higher drive currents and switching speeds [12]. Ideally, Ge exhibits the highest hole mobility when compared to other possible channel materials, whereas III–V compounds have received considerable attention as promising materials, attributed to their higher electron mobility. Therefore, co-integrating III–V compounds (n-channel) and Ge (p-channel) on the Si platform provides for an ideal CMOS technology in the future, as shown in Fig 1.4. However, an "all Ge" solution would be preferable for ease of processing. In addition, Ge belongs to the Group IV materials, similar to Si and so is more promising from a process integration perspective, removing the additional growth in manufacturing costs associated with introducing non-Group IV substrates [2].

Table 1.2. The mobility of electrons and holes for Ge and Si [11].

Material	Mobility ($cm^2 V^{-1} s^{-1}$)	
	Electron	Hole
Si	1400	470
Ge	3900	1900
GaAs	8500	400
InAs	33000	460
InSb	80,000	1250
InP	4,600	150

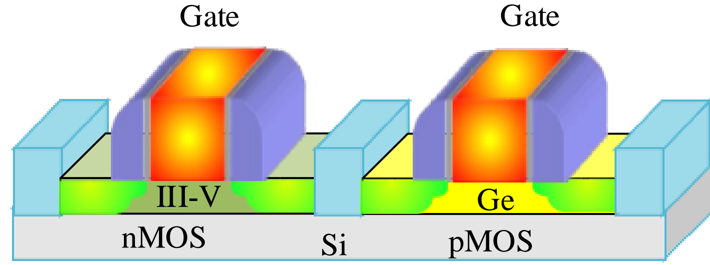

Fig 1.4. High-mobility MOSFETs built by co-integrating III–V compounds (n-channel) and Ge (p-channel) on Si platform

The deployment of metal electrodes is used to replace poly-silicon which is widely employed in Si CMOS technology based on following reasons: firstly, Fermi-level pinning at the poly-silicon/high-κ interface can cause high threshold voltage and instability [13]. Secondly, the poly-silicon/high-κ gate stack exhibits strong remote phonon scattering and degrades the channel mobility [14]. In addition, the employment of metal gate eliminates the depletion capacitance in the poly-silicon electrode [10].

1.4 Industrial Application

With the purpose to obtain a more comprehensive picture concerning the significant role of high-κ on Ge on the trend of semiconductor development nowadays, it is a good idea to look at the technology roadmap of Intel as a leading semiconductor company [12]. As shown in Fig. 1.5, for 90 nm technology, Intel used a strained silicon transistor architecture for the first time. The most significant novelty of the 90 nm technology is strained silicon which gives higher mobility. At the next stage, similar technology is used but Intel 65-nm technology has already approached the limit of SiO_2 with thickness reduced to 1.2 nm which can cause an unacceptable increase of gate leakage. Therefore Intel introduced a novel high scaling factor (high-κ) with metal gate stack into the 45-nm node technology which is called "The Biggest Change in Transistor Technology in 40 Years" by Gordon Moore [1]. The EOT of high-κ is 1 nm at this stage. Following the 45-nm node, the 32 nm technology further reduces oxide EOT to 0.9 nm. Beyond the 22 nm technology node, some fundamental constraints limit the maximum of achievable performance by CMOS. Therefore, in 22 nm and 14 nm node, Intel used new fin-FET as transistor to keep the Moore's law alive. From the perspective of technology development at Intel, it can be summarized that once the traditional performance increase of device slows down, novel materials (oxide, semiconductor) and device architectures are vitally necessary and introduced to continue to boost the performance of device. Referring to the current research, the high-κ on Ge is an attractive approach to scale the device and improve the performance for future application of CMOS technology.

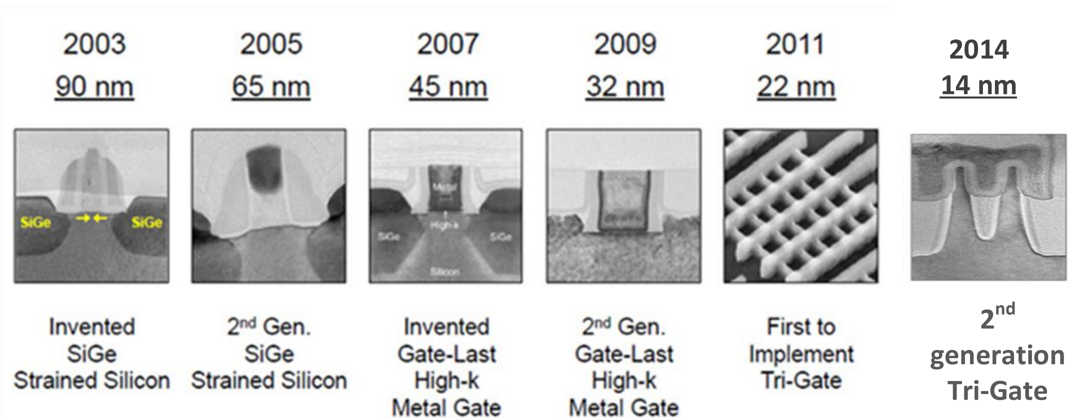

Fig. 1.5. The technology node of Intel SOURCE: Intel [15].

1.5 The Outline of Thesis

In chapter 1, the introduction of high-*κ* gate dielectric oxide on high mobility Ge channel materials for the future development of semiconductor device and its advantages over the conventional Si MOS field-effect transistor will be discussed.

In chapter 2, a literature review of commonly used techniques for the formation of GeO_2 as interfacial layer between high-κ oxide and Ge substrate is described. Lastly, the organization of this thesis is presented.

In chapter 3, the fabrication methods used in this research will be explained. XPS，TEM characterization methods will be employed to study samples.

In chapter 4, the admittance of high-*k*/Ge MOS is elaborated. Correct interpretation of the routinely used admittance characteristics is of high importance for high-*k*/Ge MOS technology since frequently used interface states density extraction methods are dependent on the admittance behavior. Capacitance-voltage (*C*-*V*) and conductance-voltage (*G*-*V*) based methods are discussed and compared in details. Their applicable scopes and problems for electrical characterization of interface states are discussed. Several issues related to the extraction of interface states density based on conductance method are demonstrated in details.

In chapter 5, The *C*-*V* characteristic for different samples are presented. The interface state density is measured to evaluate the quality of interface between Ge and the stack. The method is conductance method as discussed in chapter 4. In addition, the current over voltage (*I*-*V*) characteristics will be presented. The dielectric constant of HfO_2 will extracted at last.

In Chapter 6, a model is presented to allow calculation of the bound states in the conduction band notch at the interface between the interfacial native GeO_2 and high-*k* dielectric layer in a Ge MOSFET gate stack. The notch represents a potential charge trapping site, which can induce threshold voltage instability. The model is applied to a three-dimensional structure, and the number of electrons or average occupancy of confined electrons in the notch is

calculated. The effect of device physical and electrical parameters on the number of bound states and average occupancy of states in the notch is discussed. The significance of the confined charge in the notch and its effect on the threshold voltage shift in an 8-nm node Ge MOSFET is investigated.

In chapter 7, the minority carrier generation in inversion region for samples will be discussed. Low frequency behaviour apparent in the *C-V* plots of high-*k*/Ge MOS will be explained by two mechanisms. One mechanism is thermal generation another is a diffusion process. The temperature measurement associated with Arrhenius plot is used to identify the dominant mechanism. The measured minority generation lifetime is used subsequently, to fit the experimental data.

In chapter 8, oxide traps in high-*k*/Ge MOS are studied by analyzing the admittance characteristics. In this chapter, Yuan’s model is presented to explain the frequency dispersion observed in the CV plot accumulation region.

Chapter 9: the experimental results and achievements of the thesis are summarized. Suggestions for work worthy for further investigation are made.

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Chapter 2 Literature review of high-κ on Ge

Direct deposition of high-κ on Ge exhibits a low-quality interface associated with a high density of interface states D_{it} between high-κ gate oxide and Ge substrate, which severely restrains the application of high performance Ge MOSFETs [1]. Thus, the introduction of an effective interfacial layer between high-κ oxide and Ge substrate is proposed to obtain a high-quality interface [1]. Various methods for forming Ge compounds such as GeO_2 [2], Ge_3N_4 [3], and GeO_xN_y [4, 5] as an interfacial layer have been investigated. Among them, GeO_2 is generally considered as one of the most promising interfacial layers similar to SiO_2 in Si CMOS [2]. One reason why Si has been the dominant semiconductor material in the modern electronic industry since 1960s primarily can be attributed to its high quality native oxide SiO_2 which forms an excellent interface with Si. However, GeO_2 exhibits two problems: firstly, GeO_2 is hygroscopic and water soluble; secondly, GeO_2 is thermally unstable and can be converted into volatile GeO [6]. Intermediate forms of GeO_x result in dangling bonds and interface states together with slow traps in the oxide. Therefore, recently extensive studies are focused on obtaining a high-quality GeO_2 interfacial layer. The different techniques proposed to fabricate a high-quality GeO_2 interfacial layer are described in this chapter. In addition, sulphur-treatment of the Ge surface is shown to be an effective way to improve the quality of the interface between high-κ and Ge [7]. Al_2O_3 also is considered as an effective barrier layer to protect the interfacial layer from loss of oxygen and consequent degradation of GeO_2.

2.1 Formation of the GeO_2

Methods to form GeO2 have been investigated extensively. The current section provides an overview for the different techniques.

2.1.1 Thermal oxidation

Thermally grown GeO_2 has been extensively examined in terms of different process conditions such as temperature and time. In-situ low temperature vacuum annealing after dry oxidation 500 ℃ and prior to gate electrode could improve the GeO_2 interfacial layer [8]. Minimum D_{it} smaller than 10^{11} eV^{-1} cm^{-2} has been achieved with an oxidation temperature of 575 ℃ over range of 450, 500, 550, 575 and 600 ℃ [2]. Lee *et al.* demonstrated high-pressure thermal oxidation is helpful to obtain an improvement of GeO_2 [9, 10]. Lee *et al.* further employed a high-pressure oxidation method followed by a low temperature oxygen annealing. This significantly enhances the GeO_2 quality and 1.2 nm thick equivalent oxide thickness (EOT) GeO_2/Ge gate stack with low D_{it} 10^{11} eV^{-1} cm^{-2} has been achieved [11]. Their group recently introduced an yttrium oxide Y_2O_3/Ge stack which achieved improved quality GeO_2 which may be attributed to a capping effect by the Y_2O_3 to protect the thermally grown GeO_2

[12]. The orientation dependence of the Ge substrate with GeO_2 formed by thermal oxidation was investigated to determine which orientation could achieve the lowest interface states [13]. For different orientations, it is reported that D_{it} in the upper part of the band gap shows no significant difference, while D_{it} in the lower band gap exhibits the lowest D_{it} for (111) orientation of Ge substrate. This conclusion is consistent with the result that p-channel MOSFETs with orientation (111) Ge substrate exhibit higher mobility and lower interface state compared to other orientation [14, 15].

2.1.2 Ozone oxidization

Ozone has higher reactivity than oxygen and consequently can enhance the thermal oxidation of Ge at lower temperature. Kuzum *et al.* have demonstrated minimum D_{it} of 3×10^{11} cm^{-2} eV^{-1} for Al_2O_3/GeO_2 Ge-based MOSFETs [16]. More recently, cycling ozone method associated with the atomic layer deposition (ALD) process was proposed to obtain high quality GeO_2 which achieved a minimum D_{it} of 1.9×10^{11} cm^{-2} eV^{-1} [17-19]. Molle *et al.* found that 300 ℃ is the optimal temperature to maximize the production of GeO_2; higher temperature can transform GeO_2 into the suboxide state [20]. The oxidation mechanism of ozone has been studied by Baldovino *et al.* [21]. Two groups have demonstrated 1.5 times higher electron mobility exceeding the universal Si mobility for Ge n-MOSFETs associated with ozone oxidation for the GeO_2 interfacial layer [16, 18].

2.1.3 Plasma-assisted method

Plasma treatment using O_2 is considered as a promising method to grow a high quality GeO_2 interfacial layer at low temperature [22, 23]. Xie *et al.* suggest GeO_2 formed by O_2 plasma combined with a plasma-enhanced ALD for high-κ could offer an effective route to achieve a high quality interfacial layer [24]. Zhang *et al.* proposed a method which employs electron cyclotron resonance (ECR) plasma post oxidation through a thin ALD deposited Al_2O_3 capping layer on a Ge substrate, which serves to prevent the degradation of the GeO_2 in post-processing [25]. The relationship between the thickness of GeO_2 and D_{it} has been investigated and 0.5 nm GeO_2 is considered as the minimum thickness to maintain acceptable MOS interface properties [26]. The main mechanisms of the mobility degradation of Ge p- and n-MOSFETs by using post plasma oxidation have been systematically studied [27]. The following table shows a summary of Ge-based MOSFET with GeO_2 as an interfacial layer.

Table 2.1 The Ge-based MOSFETs with GeO_2 as the interfacial layer, studied in literature review.

Device	Peak mobility of inversion carriers (cm^2/V-s)	EOT (nm)	GeO_2	D_{it} Mid-gap energy level (eV^{-1} cm^{-2})	Doping concentration (cm^{-3})
Al_2O3/GeO_2 p-MOSFETs [28]	575 (hole)	--	Thermal grown from 0 to 20 nm	2.1×10^{11}	2.1×10^{15}
$LaLuO_3/GeO_2$ p-MOSFETs [29]	260 (hole)	1.14	Thermal grown 1.5 nm	--	--
HfO_2/GeO_2 p-MOSFETs [30]	400 (hole)	1	Thermal grown 2 nm	2.0×10^{11}	--
Al/GeO_2 n-MOSFETs [31]	1100 (electron)	5	Thermal grown 8.5 nm	3.5×10^{11}	--
Y_2O_3/GeO_2 n-MOSFETs [32]	1500 (electron)	22, 12	Thermal grown 3 nm	1.0×10^{11}	--
Al_2O3/GeO_2 n-MOSFETs [33]	1200 (electron)	5	Ozone oxidation 2 nm	3.6×10^{11}	2.1×10^{15}
Al_2O3/GeO_2 p-MOSFETs [25]	515, 466, and 401 (hole)	1.18, 1.06, 0.98	Post plasma oxidation from 1.2 to 0.23 nm	2.0×10^{11}	--

2.1.4 Sulphur treatment

Sulphur passivation has been suggested as an attractive solution to passivate Ge surface attributed to its well-known application on III–V compound material channels [23]. S-passivation is realized by immersing into aqueous ammonium sulphide $(NH_4)_2S$ solution [34] or reacting in the H_2S gas phase [35]. Both methods could induce the adsorption of S on the Ge surface. Additionally, the amount of adsorbed S and the surface ordering can be different

[36]. The accurate cover of S on the Ge after the (NH4)2S treatment are different over various papers [36]. During deposition of the high-κ material g, S is presented at the interface, and thus the interface is free of Ge-oxides. Therefore, this S-treatment is considered as a promising method to achieve high-quality interface [36].

2.1.5 Role of the Al_2O_3 capping layer

Al_2O_3 is considered as preferable high-κ material attributed to its diffusion barrier properties allowing to protect GeO_2 and achieve enhancing interface compared to other high-κ materials such as HfO_2 [37-39]. However, the permittivity of Al_2O_3 is relatively low among all high-κ materials, thus a gate stack high-κ/Al_2O_3/GeO_2 has been studied to achieve a high-quality GeO_2 interfacial layer while maintaining the low EOT [37, 39].

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Chapter 3 Fabrication and characterization

3.1 Introduction

Alumina (Al_2O_3) is considered as a preferable high-κ material due to its diffusion barrier properties which could protect the native oxide, GeO_2 which provides for a good interface compared to other high-κ materials such as HfO_2 [1, 2]. However, the permittivity of Al_2O_3 is relatively low compared to other high-κ materials, thus a gate stack high-κ/Al_2O_3/GeO_2 has been studied to achieve a high-quality GeO_2 interfacial layer while maintaining a lower EOT [3, 4]. In addition, sulphur (S) has been introduced into GeO_2 to achieve a superior Ge gate stack [5, 6]. In this chapter, two groups of fabrication processing are described. For the first group, Al_2O_3, formed in a molecular beam epitaxy (MBE) system, acts as a protecting layer to achieve a high quality interface. The second group includes S-passivation as a method to achieve a good interface. The current chapter will present the details of the fabrication of MOS samples through this research. All the samples used in this thesis were fabricated by collaborators in the Materials Science department. X-ray Photoelectron spectroscopy (XPS) measurements were undertaken by collaborators to investigate the physical properties of the interface for these samples. The electrical quality of the interface is evaluated using the conductance method to measure the density of interface states.

3.2 Al_2O_3 protecting layer

N-type Ge (100) wafers were cleaned in ultra-high vacuum (<10−6 mbar) at 500 ℃ for 10 min to evaporate any native oxide and thus obtain an oxide free surface. Subsequently, the wafers were placed in an MBE chamber and exposed to an Al flux for a range of times to deposit ultrathin Al layers. The samples were allowed to oxidise at ambient temperatures in the MBE load lock to produce Al_2O_3 layers. The samples were transferred within 1 min to an Oxford Instruments OpAL reactor and thin films of HfO_2 were deposited on the Al_2O_3 using atomic layer deposition (ALD). The HfO_2 depositions used a [$(CpMe)_2HfOMeMe$] precursor coupled with an O_2 plasma as the oxidising species. Different numbers of cycles were used to grow HfO_2 thicknesses of 3.5 (sample Ge12S1), 7 (sample Ge12S2) and 14 (sample Ge12S3) nm at 250 ℃ as shown in **Error! Reference source not found.**. A fabrication process diagram is given in Fig. 3.1. For electrical measurements, circular gold contacts with a range of diameters were deposited onto the films to form MOS gate electrodes and Al was deposited onto the back of the Ge wafers to provide an ohmic contact.

Table 3.1 The summarization for the thickness of different samples with Al_2O_3 as protecting layer.

Sample	Thickness of HfO_2
Ge12S1	3.5 nm
Ge12S2	7 nm
Ge12S3	14 nm

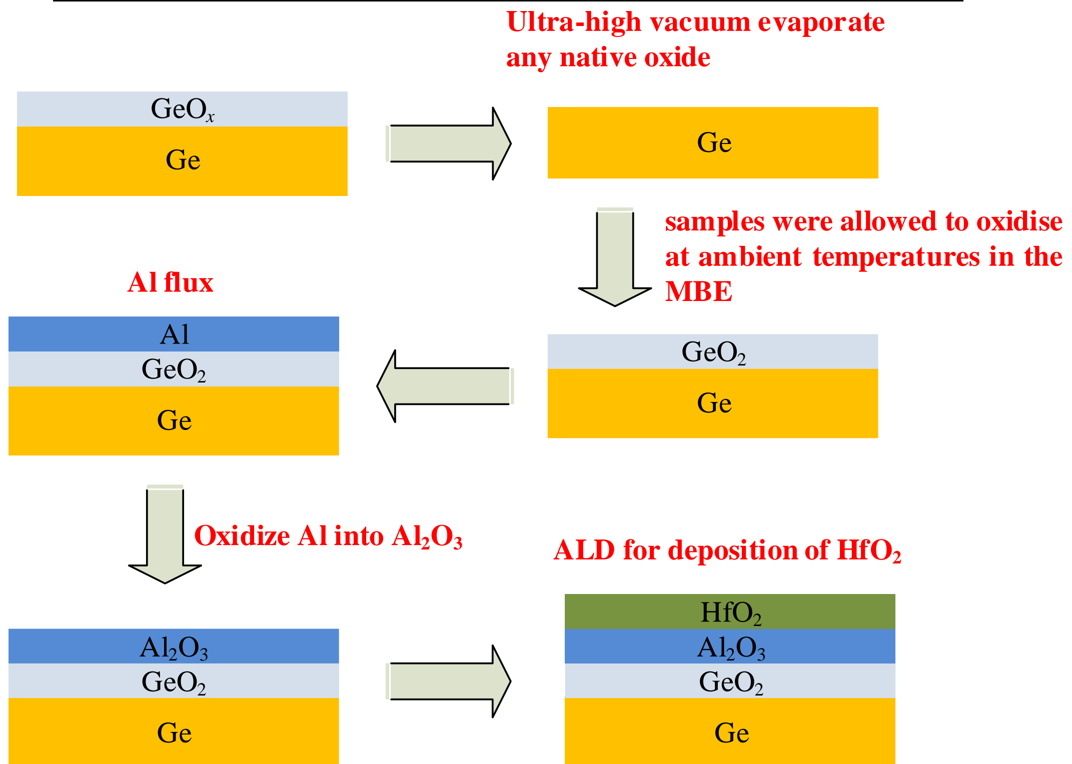

Fig. 3.1. Method to deposit a high-κ stack on Ge with Al_2O_3 as protection layer.

The main advantages of this fabrication process have been summarized as following: firstly, Al_2O_3 layer can act as an oxygen barrier, which suppresses the growth of an unnecessarily-thick Ge oxide layer, owing to its intrinsic oxygen permeability [2, 7]. The Al_2O_3 layer also prevents GeO_2 from deterioration caused by subsequent ALD processing when depositing HfO_2. In addition, the Al is oxidized at ambient temperatures in the MBE (molecular beam epitaxy) load lock to form Al_2O_3, which significantly reduces the oxygen desorption of GeO_2 with thermal instability induced by high temperature.

3.3 Second fabrication process

N-type (100) Ge of resistivity 0.3–3 Ω cm were degreased using acetone in an ultrasonic bath and then given a cyclic HF/water rinse in order to remove the native oxide layer. This was

followed by sulphur deposition by dipping the samples in a 20% ammonium sulphide, $(NH_4)_2S$, solution in water for 10 min and then dried under an argon gas flow. The samples were then immediately transferred into an Oxford Instruments OpAL ALD reactor and different number of cycles were used to deposit different thickness of HfO_2 layers using [(CpMe)2HfOMeMe] precursor coupled with remote oxygen plasma (Fig. 3.2 (a)). As shown in **Error! Reference source not found.**, three samples with different thickness of HfO_2 are given: 3.5 (sample Ge39S1), 7 (sample Ge39S2) and 14 (sample Ge39S3) nm. In addition, as discussed before, Al_2O_3 still can be used as a protecting layer. One extra S-treated sample was exposed to an Al flux for a range of times to deposit ultra-thin Al layers to compare with those without the Al_2O_3 protecting layer. This sample was oxidized at ambient temperatures in the Molecular Beam Epitaxy (MBE) load lock to produce sub-nm Al_2O_3 layers as for the first group. Then, this sample was transferred to the ALD reactor, as shown in **Error! Reference source not ound.**, 3.5 nm (sample Ge39S4) thickness of HfO_2 films was deposited using ALD cycles with the same HfO_2 precursor and O-plasma as oxidant.

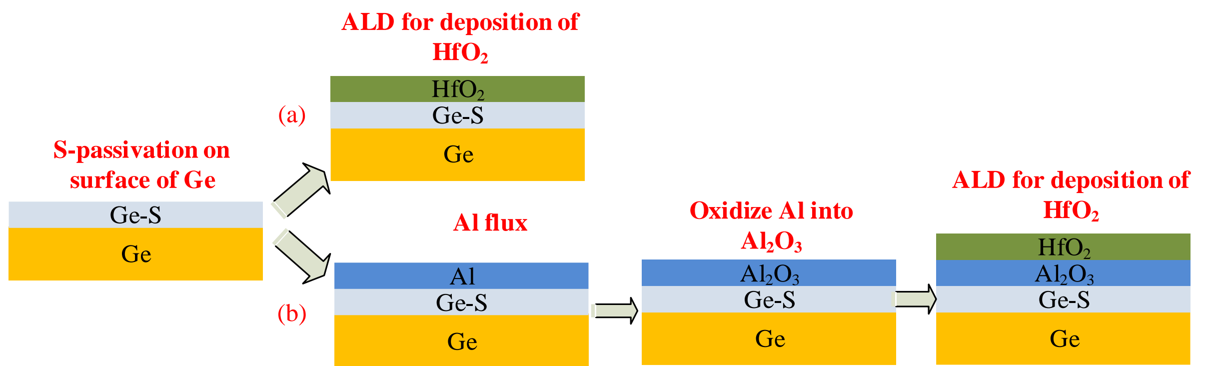

Fig. 3.2. Proposed processing steps: (a) S-passivation without Al_2O_3; (b) S-passivation with Al_2O_3.

Table 3.2. Summary of high- κ layer thickness of different samples with S-passivation.

Sample	Thickness of HfO_2
Ge39S1	3.5 nm
Ge39S2	7 nm
Ge39S3	14 nm
Ge39S4 (S-passivation with Al_2O_3)	3.5 nm

3.4 TEM and XPS characterization

Fig. 3.3 shows an HRTEM (High-resolution Transmission electron microscopy) image of sample Ge12S2 with 10 s exposure to the MBE Al source and with number of ALD cycles to deposit 7 nm HfO_2. The image was obtained with a JEOL 2100F TEM operating in STEM mode with an operating voltage of 200 kV. The TEM image shows a 2 nm thickness layer of GeO_2/Al_2O_3 with a 7 nm HfO_2 layer on top.

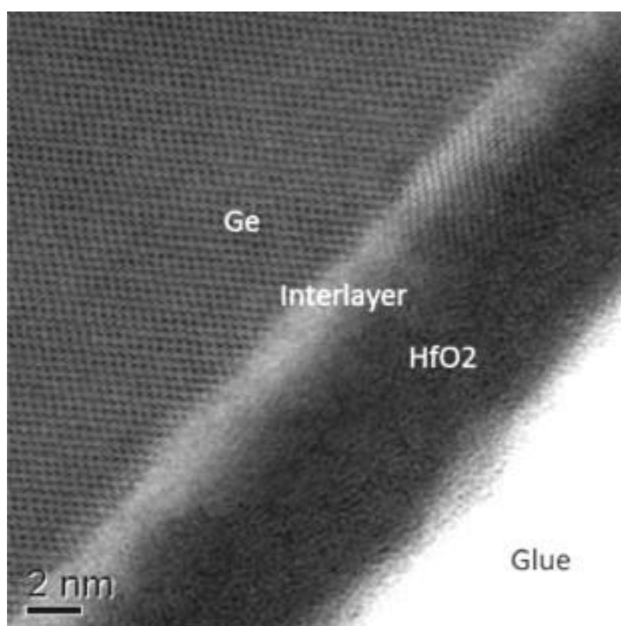

Fig. 3.3. TEM image of a about 2 nm thick GeO_2/Al_2O_3 layer with HfO_2 on top.

XPS was carried out to investigate the chemical bonding presented in the films. Fig. 3.4 shows XPS Al (2p) spectra from sample Ge12S1 confirming that Al_2O_3 is formed when compared to a reference Al foil. The small peak at 73 eV is attributed to differential charging across the thin alumina layer. The XPS Ge (3d) data of Fig. 3.5 for sample Ge12S1, shows that a layer of GeO_2 is present at the Ge surface.

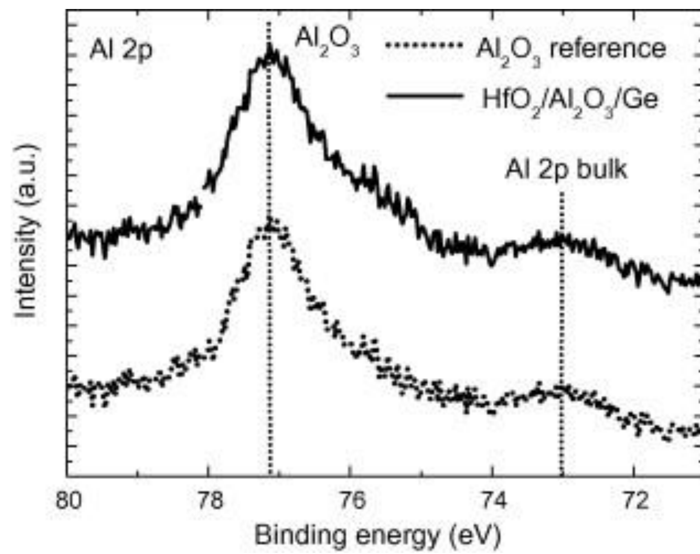

Fig. 3.4. XPS spectra from sample Ge12S1 for Al 2p from 10 s Al MBE exposure with number of ALD cycles of HfO_2.

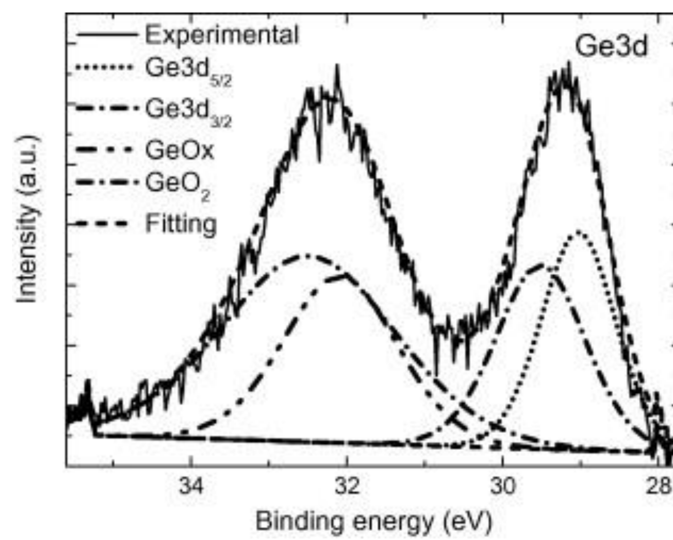

Fig. 3.5. XPS spectra from sample Ge12S1 for Ge 3d from 10 s Al MBE exposure and number of ALD cycles of HfO_2.

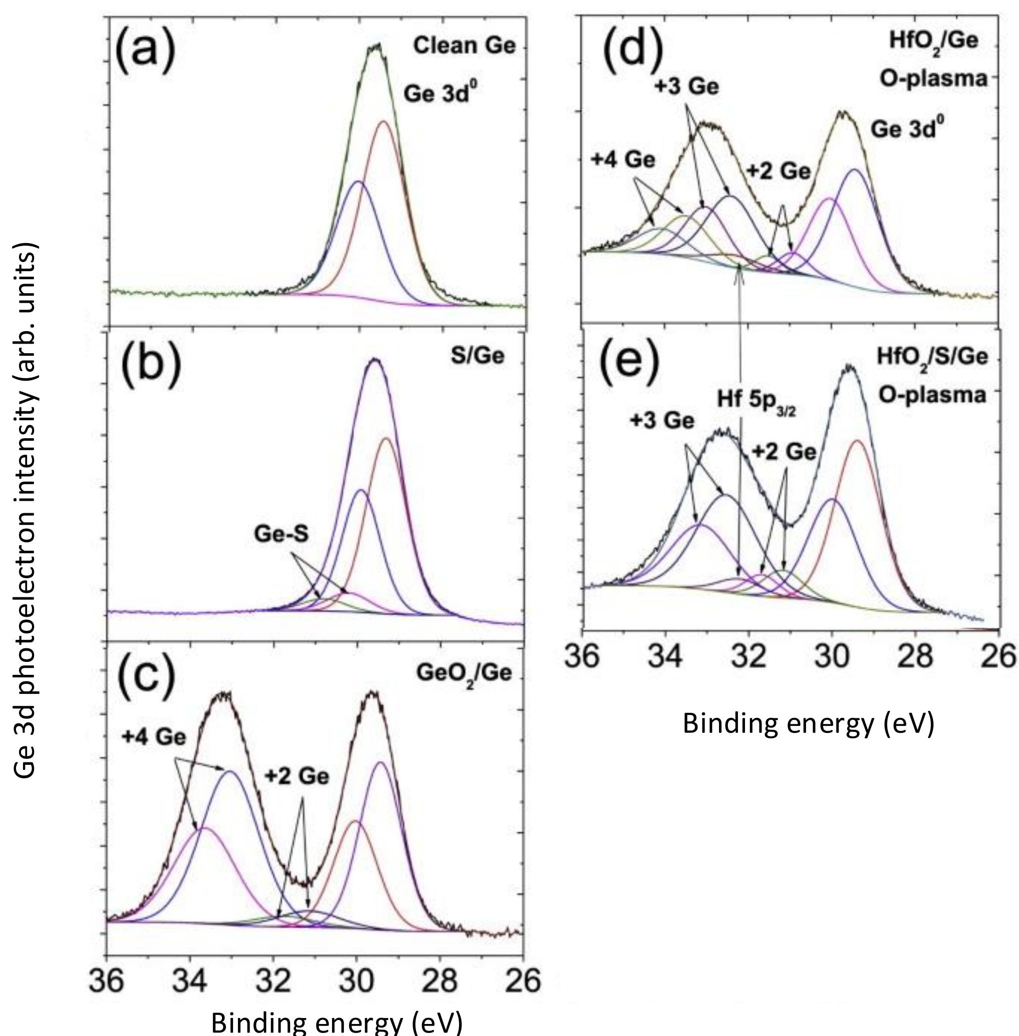

Fig. 3.6. Ge 3d XPS core level line-shape for: (a) clean Ge, (b) S-passivated Ge, (c) native GeO_2/Ge, (d) HfO_2/Ge, (e) HfO_2/S/Ge using oxygen plasma as oxidant during ALD deposition.

Fig. 3.6 shows a comparison of the Ge 3d line shape measured from several samples. The XPS Ge 3d CL spectrum for a sample of clean Ge is shown in Fig. 3.6 (a). The experimental curve is fitted with two sub-peaks corresponding to Ge $3d_{5/2}$ at 29.42 eV and Ge $3d_{3/2}$ at 30.37 eV, corresponding to the spin–orbit doublet. Compared to the spectrum of clean Ge sample, the S-treated Ge sample in Fig. 3.6 (b) shows an additional feature, which is also fitted with a doublet. Fig. 3.6 (c) shows the spectrum of native GeO_2/Ge. The peak fitted at 33.03 eV is attributed to the +4 Ge oxidation state (i.e. GeO_2), while a small peak centred around 1.7 eV above the Ge 3 d °(indicated on the figure with arrows) is related to +2 Ge oxidation state. Compared to the S-passivated sample, it is clear that the introduction of sulphur is promising in passivating the sample, as proven by the disappearance of the GeO_2 peak in Fig. 3.6 (b). Fig. 3.6 (d) and (e) is the Ge 3d line-shape from HfO_2 deposition by using oxygen plasma without and with S-passivation. The growing appearance of GeO_x can be attributed to the introduction of O-plasma. Especially, the +2 Ge is observed by the growing intensity during the area between

the two main peaks, at around 31 eV. This can be further proven by comparing to Fig. 3.6 (c) where the sample exhibits the predominant GeO_2 layer on Ge. From the whole line-shape, it is observed the GeO_2 peak (see Fig. 3.6 (d)-(e) in comparison to Fig. 3.6 (c)) to be broadened, along with the appearance of Hf $5p_{3/2}$ peak from HfO_2 at around 32 eV as shown by the arrows.

3.5 Conclusion

In summary, two kinds of surface passivation method for Ge-based MOS with HfO_2 have been discussed in detail. The Al_2O_3 layer is formed by deposition of Al using MBE followed by its oxidation at room temperature. The S-passivation is also a possible method to passivate the surface between Ge and HfO_2. Detailed X-ray photoelectron spectroscopy and electrical characterization results show that sulphur passivation and Al_2O_3 can prevent the formation of GeO_x at the interface.

3.6 References

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Chapter 4 Interface Characterization Techniques for Ge MOS

4.1 Introduction

As discussed before, interface passivation is a major challenge for Ge-based MOSFET technology. High interface state density is a probable cause of the mobility degradation and threshold voltage instability of Ge-based MOSFETs [1]. Therefore, it is critical to correctly evaluate the quality of the interface which is mainly quantified by the density of interface states. Some inherent properties of Ge could affect the correct estimation of interface states extracted from conventional *C-V* and *G-V* based measurements which can be correctly used on Si-based device. More specifically, the characteristic time constant of interface states and the thermal generation or diffusion of minority carrier charge from the bulk Ge substrate could cause misinterpretation of the evaluation for interface states density. In this chapter, firstly the physical mechanism of interface states and the associated equivalent circuit based on Nicollian and Goetzberger's theory will be investigated [1]. Then, several conventional methods for profiling the interface states are discussed. The weakness, advantages and limitations of these methods applied on Ge-based MOS are presented. The three issues related to the conductance method on Ge-based MOS will be investigated.

4.2 The physical mechanism and equivalent circuit of interface states

Interface states refer to charge traps located at the oxide-semiconductor interface and are distributed across the band gap of the semiconductor. The interface states exchange carriers with the conduction band by capturing or emitting electrons and with the valence band by capturing or emitting holes as depicted in Fig. 4.1 (a). Nicollian and Goetzberger treat a single interface state as a Shockley-Read-Hall recombination centre [1]. Thus, the admittance impact of interface states caused by the discharging or charging of a single interface state following application of a small ac signal can be modelled by a Y equivalent circuit as shown in Fig. 4.1 (b).

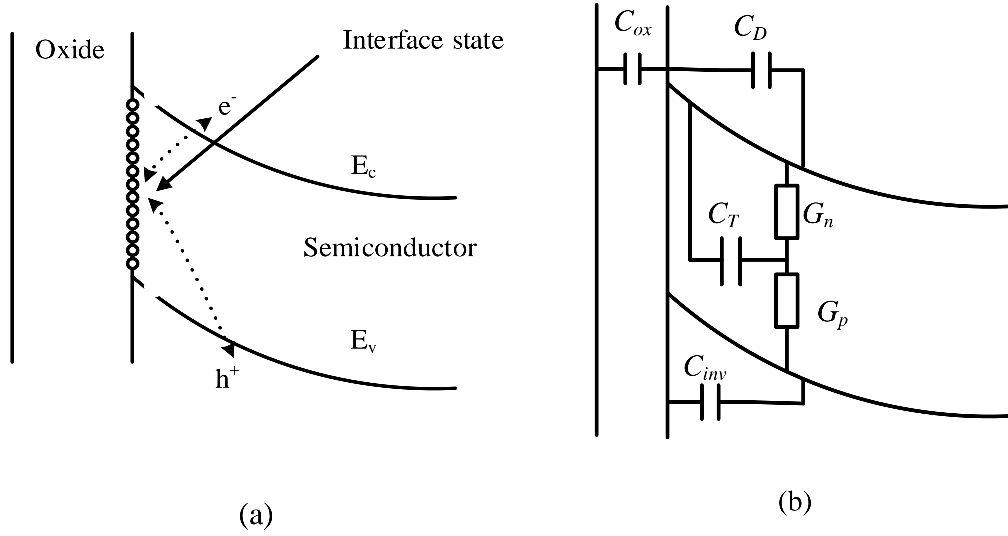

Fig. 4.1. (a) Interface states exchange carriers with conduction band and valence band; (b) Equivalent circuit of a single interface state (n-type semiconductor substrate).

Referring to Fig. 4.1 (b), G_p and G_n represent the communication of a single interface state with both the conductance band and the valence band respectively. C_{ox} is the oxide capacitance, C_D is the depletion capacitance and C_{inv} is the inversion capacitance. The expressions for C_T, G_n, and G_p are:

$$C_T = \frac{q^2}{kT} N_T f(1-f) \tag{4.1}$$

$$G_n = \frac{q^2}{kT} N_T f(1-f)\tau_n^{-1} \tag{4.2}$$

$$G_p = \frac{q^2}{kT} N_T f(1-f)\tau_p^{-1} \tag{4.3}$$

where f is the Fermi–Dirac distribution function, τ_n and τ_p are the characteristic time constants of electrons and holes for interface states, which are used to measure the exchange time between interface and conduction or valence band, N_T is the density of interface states, T is absolute temperature and k is Boltzmann's constant. Furthermore,

$$\tau_n = \left(\sigma_n v_{th}^n n_s\right)^{-1} \tag{4.4}$$

$$\tau_p = \left(\sigma_p v_{th}^p p_s\right)^{-1} \tag{4.5}$$

σ_p and σ_n are the hole and electron capture cross sections of the interface state, υ^n_{th} and υ^p_{th} are electron and hole thermal velocity, n_s and p_s are the electron and hole concentration at the interface between oxide and semiconductor which can be further expressed as:

$$n_s = N_c \exp\left(-\frac{E_C - E_T}{kT}\right) \tag{4.6}$$

$$p_s = N_V \exp\left(-\frac{E_T - E_V}{kT}\right) \quad (4.7)$$

E_T is the energy level of interface state.

Then substitution of these two equations into the previous Eqs (4.4) and (4.5), gives the characteristic time constants can be expressed as:

$$\tau_n = \frac{\exp\left(\frac{E_C - E_T}{kT}\right)}{\sigma_n v_{th}^n N_C} \quad (4.8)$$

$$\tau_p = \frac{\exp\left(\frac{E_T - E_V}{kT}\right)}{\sigma_p v_{th}^p N_V} \quad (4.9)$$

The interface states are continuously distributed across the band-gap; the equivalent circuit including a distribution of the interface states is shown in Fig. 4.2.

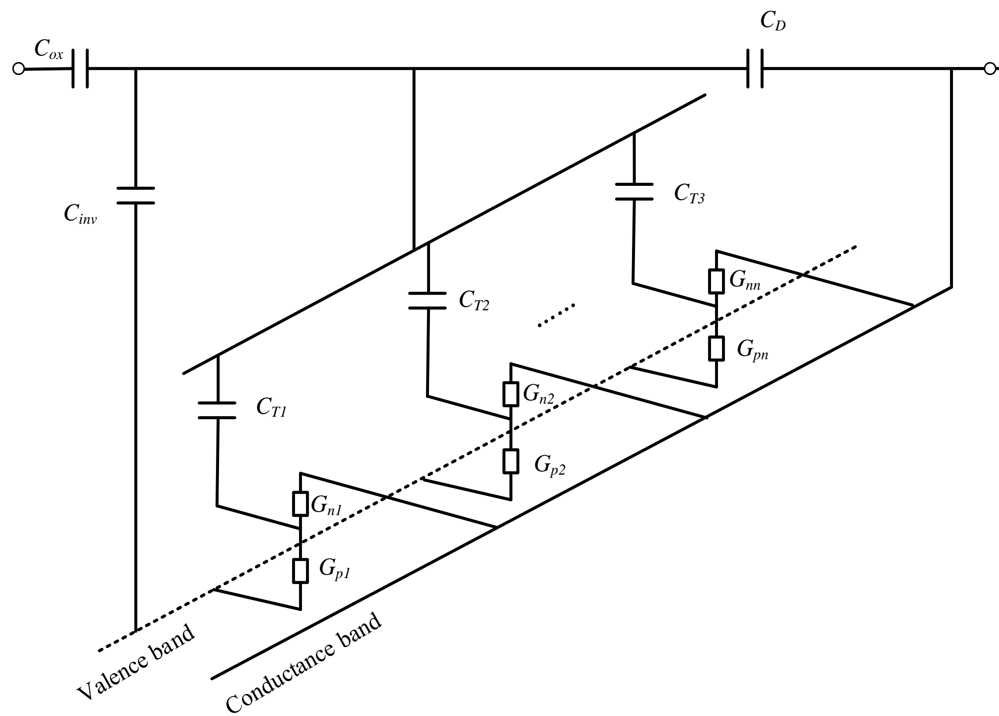

Fig. 4.2. The equivalent circuit including a distribution the interface states.

To integrate the total admittance of this equivalent circuit, every single Y-circuit needs to be converted to a Δ-circuit, then:

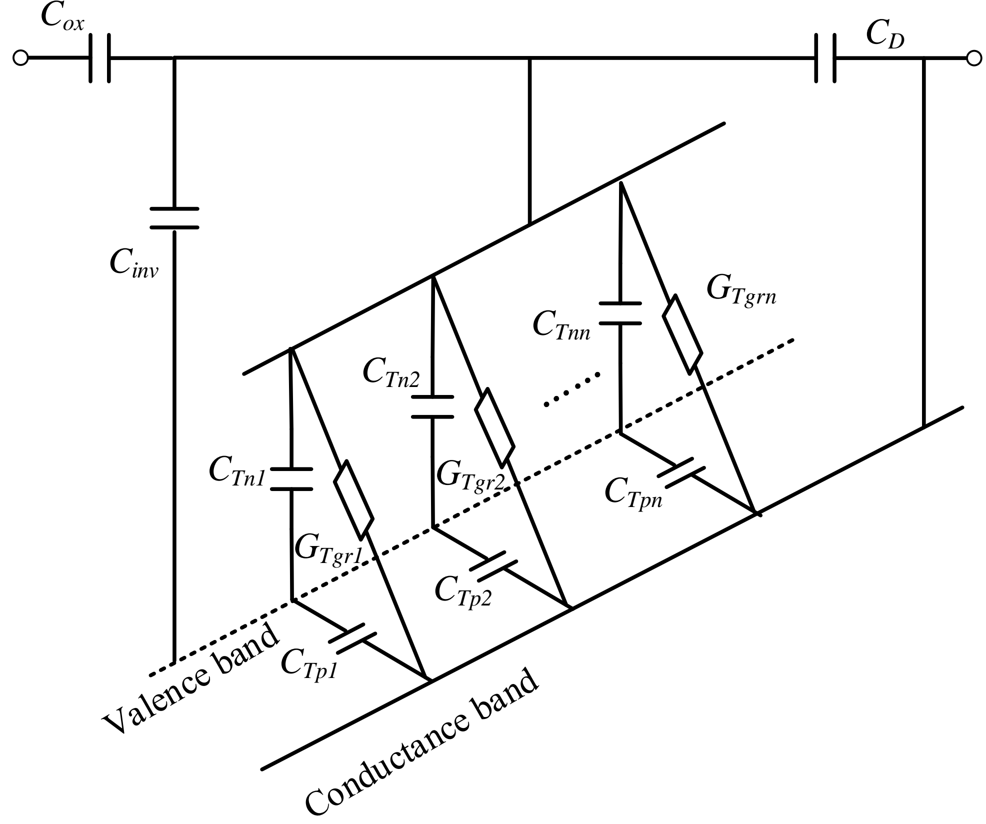

Fig. 4.3. The converted Δ-circuit based on Fig. 4.2.

For a single interface state, the G_{Tgr}, C_{Tn} and C_{Tp} are given by:

$$G_{Tgr} = \frac{G_n G_p}{D} \tag{4.10}$$

$$C_{Tn} = \frac{G_T G_p}{D} \tag{4.11}$$

$$C_{Tp} = \frac{G_T G_n}{D} \tag{4.12}$$

Where $D = j\omega G_T + C_n + C_p$.

Then integrate all interface states based on the above circuit as shown in following equations,

$$C_{Tn,sum} = qD_{it}\tau_n^{-1}\int_0^1 df(1-f)\times\left[j\omega f(1-f)+f\tau_p^{-1}+(1-f)\tau_n^{-1}\right]^{-1} \tag{4.13}$$

$$C_{Tp,sum} = qD_{it}\tau_p^{-1}\int_0^1 df\times f\times\left[j\omega f(1-f)+f\tau_p^{-1}+(1-f)\tau_n^{-1}\right]^{-1} \tag{4.14}$$

$$G_{gr,sum} = qD_{it}\tau_p^{-1}\tau_n^{-1}\int_0^1 df\left[j\omega f(1-f)+f\tau_p^{-1}+(1-f)\tau_n^{-1}\right]^{-1} \tag{4.15}$$

where D_{it} is the density state of interface states.

Finally, the equivalent circuit for all interface states is simplified as:

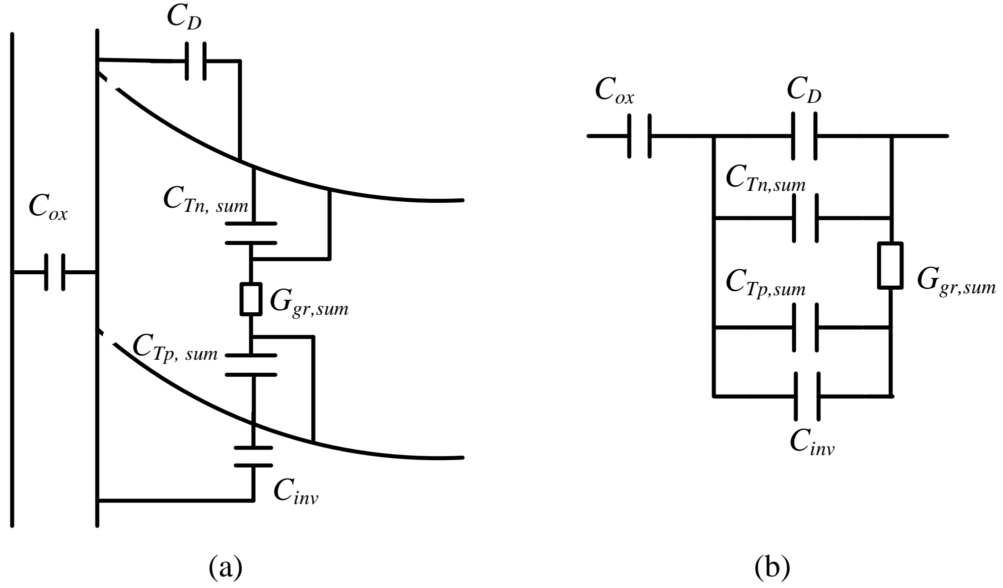

Fig. 4.4. (a) Final equivalent circuit after integrated all the interface states; (b) further simplified circuit from (a).

The physical mechanism for charging and discharging process of interface states and their equivalent circuit based on Nicollian and Goetzberger's theory has been described. The following part will examine several methods conventionally used to estimate the density of interface states based on the equivalent circuit described above.

4.3 Low-high frequency method [1]

The MOS capacitor is measured at sufficiently low frequency which allows all the interface state to follow the small ac signal. At quite low frequency, the conductance $G_{gr,sum}$ is negligible, the Fig. 4.4 (b) can be transferred to the circuit as shown below:

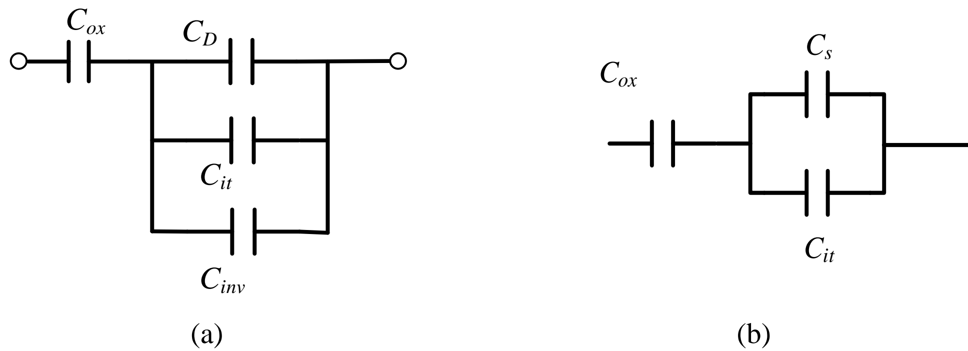

Fig. 4.5. (a) Low frequency equivalent circuit; (b) further simplified circuit from (a).

where $C_s = C_D + C_{inv}$ is the surface capacitance, C_{it} is interface state capacitance, and for low frequencies, C_{it} is:

$$C_{it} = C_{Tn,sum} + C_{Tp,sum} \approx qD_{it} \tag{4.16}$$

The measured capacitance at low frequencies C_{lf} shown in Fig. 4.5 (b) can be expressed as

$$\frac{1}{C_{lf}} = \frac{1}{C_{ox}} + \frac{1}{C_{it} + C_s} \tag{4.17}$$

Then D_{it} can be extracted using:

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{lf}}{C_{ox} - C_{lf}} - C_s\right) \tag{4.18}$$

C_s can be theoretically calculated based on the doping concentration.

The theoretical calculation of C_s, may require much work with potential error arising from inaccurate knowledge of the doping concentration profile and oxide capacitance in determination of D_{it}. Castagene and Vapaille suggest that C_s is better extracted at high frequency [2]. When the frequency is high enough, it is safe that assume all the interface states cannot follow the small ac signal and the equivalent circuit is shown in Fig. 4.6. Thus Castagne and Vapille's method does not need a theoretical calculation of C_s, which can be given by Eq (4.19).

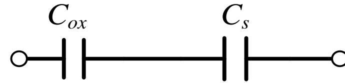

Fig. 4.6. High frequency equivalent circuit.

$$C_S = \frac{C_{ox}C_{hf}}{C_{ox} - C_{hf}} - \frac{1}{C_{ox}} \tag{4.19}$$

where C_{hf} is the measured capacitance in high frequency.

Substitute Eq (4.19) into (4.18), then D_{it} can be obtained:

$$D_{it} = \frac{1}{q}\left(\frac{C_{ox}C_{lf}}{C_{ox} - C_{lf}} - \frac{C_{ox}C_{hf}}{C_{ox} - C_{hf}}\right) \tag{4.20}$$

Thus by combining the low and high frequency methods, the density of interface states can be extracted.

4.4 Terman's method

Terman developed and employed a high frequency capacitance method to estimate interface state density [3]. In this method, *C-V* is measured at sufficiently high frequency, so that all the interface states cannot respond. Therefore, the measured capacitance should be equal to the ideal MOS capacitance without any ac contribution from interface states. However, the interface states still lead to the "stretch-out" of *C-V* curve compared to the ideal *C-V* curve because these interface states can change their occupation following Fermi level change determined by the *DC* gate voltage bias as shown in Fig. 4.7. The ideal capacitance without a contribution from interface states theoretically can be obtained based on the doping

concentration and oxide capacitance. The interface state density based on Terman's method is determined from equation [3]:

$$D_{it} = \frac{C_{ox}}{q} \frac{d(\Delta V_g)}{d\psi_s} \tag{4.21}$$

where ΔV_g is the voltage shift of the experimental compared to the ideal curve.

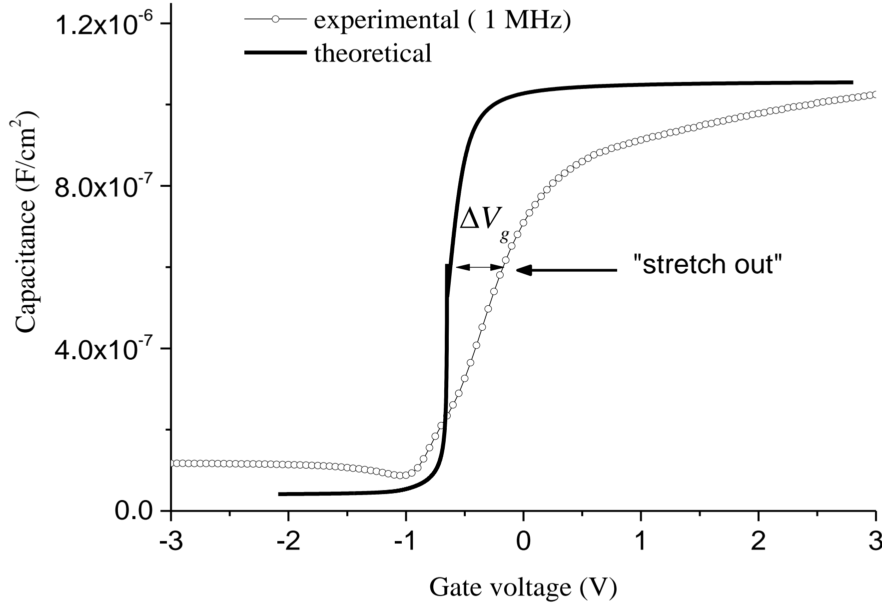

Fig. 4.7. The solid line is the theoretical Ge-based MOS *C–V* without D_{it}. The parameters for calculation of the theoretical *C-V* (1 MHz): doping concentration $N_{sub} = 5.2 \times 10^{16}$ cm^{-3}; oxide capacitance. $C_{ox} = 1.1 \times 10^{-6}$ F/cm^2. The circles represent experimental data measured from sample Ge39S1 at 1 MHz.

4.5 Gray-Brown method

Gray-Brown [4] uses a similar method to that of Terman. However, the Fermi-level occupation change in interface states is determined by the temperature. There is no need to calculate a theoretical *C-V* which is an advantage compared to the Terman's method, as this is avoided by measuring the capacitance at flat-band condition at different temperature. When the temperature is changed, the Fermi-level position will shift, thus the occupation of interface state is altered. Thus, the gate voltage for flat-band condition will change. Terman method measure both interface states and oxide traps. Because Terman method measure density state through voltage shift, both interface states and oxide traps lead to voltage shift. Thus it measures two type of traps.

For different temperatures, the flat-band condition gate voltage is expressed as V_g, the difference of flat-band condition gate voltage at different temperatures is given by:

$$V_{diff} = V_{g1} - V_{g2} = \frac{q \int_{E_f(Vg2)}^{E_f(Vg1)} dE \cdot D_{it}(E)}{C_{ox}} \quad (4.22)$$

V_{g1} and V_{g2} are flat-band voltages at different temperatures, E_f (V_{g1}) and E_f (V_{g2}) are Fermi level positions at different temperature.

Thus by measuring the shift of voltage V_{diff} at the flat-band condition at different temperatures, the interface state density can be obtained [1]:

$$D_{it} = \frac{C_{ox}}{q}\frac{dV_{diff}}{dE_f} \quad (4.23)$$

Sun *et al.,* [5] modified the Gray-Brown method to measure the interface states of Ge MOS capacitors. As discussed before, the Terman method basically measures two type of traps namely interface states and oxide bulk traps. Sun *et al.,* modified the Gray-Brown method by excluding the effects of interface states measured from the conductance method, thus the oxide-trap can been obtained without interface states.

4.6 Conductance method

The conductance method proposed by Nicollian and Goetzberger is extensively employed to measure the interface state density and is considered to have the highest sensitivity [1]. Interface state density down to 10^9 cm^{-2} eV^{-1} can be measured by using the conductance method. Referring to (b), Nicollian and Goetzberger assume for n-type semiconductor, in the depletion region, the time constant of majority carriers is much smaller than that of minority carriers ($\tau_n << \tau_p$). In this case, the charge exchange between interface states and valence band can be ignored and this figure can be converted to Fig. 4.8 (a).

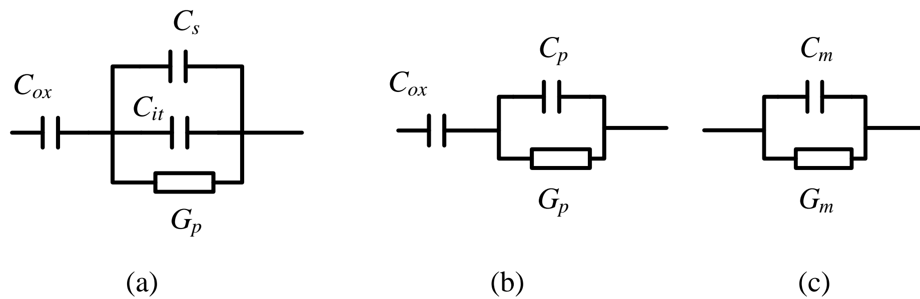

Fig. 4.8. (a) The converted circuit of Fig. 4.5 (b); (b) simplified circuit of (a); (c) measured circuit of (b) in parallel mode.

C_{it} is expressed as Eq (4.16), $G_p = G_{gr,sum}$ as shown in Eq (4.15), $C_p = C_s + C_{it}$.

From Fig. 4.8, it can be seen that there is one advantage; the conductance method extracts the interface state density based on conductance without C_S. This is an important advantage over the other three capacitance-based methods, because it avoids any errors involved in obtaining C_s. The conductance method eliminates this uncertainty by excluding C_s and only needing

conductance. For n-type semiconductor, interface states in the upper half of the band gap can be extracted; and for p-type, the lower half can be extracted. For n-type semiconductor, in the depletion regime, C_p and G_p can be expressed as:

$$C_p = C_s + qD_{it}(\omega\tau_n)^{-1}\tan^{-1}(\omega\tau_n) \qquad (4.24)$$

$$G_p/\omega = qD_{it}(2\omega\tau_n)^{-1}\ln\left[1+(\omega\tau_n)^2\right] \qquad (4.25)$$

When G_p / ω is plotted as a function of ω, it shows a maximum at $\omega = 1.98 / \tau_n$ and at the maximum:

$$D_{it} = 2.5G_p/\omega$$

Thus, D_{it} and τ_n can be determined from maximum G_p / ω.
Generally experimental G_p / ω versus ω curves are broader than theoretically predicted due to surface potential fluctuations arising from such as non-uniformities in doping, fixed charge. When surface potential fluctuations are taken into account:

$$G_p/\omega = q\int_{-\infty}^{\infty} D_{it}(2\omega\tau_n)^{-1}\ln\left[1+(\omega\tau_n)^2\right]P(U_S)dU_S \qquad (4.26)$$

where

$$P(U_S) = \frac{1}{\sqrt{2\pi\sigma^2}}\exp\left(-\frac{\left(U_S-\overline{U_S}\right)^2}{2\sigma^2}\right) \qquad (4.27)$$

$P(U_s)$ is the probability distribution of surface potential fluctuation, $\overline{U_S}$ is the mean surface potential and σ is the standard deviation.

4.7 Characteristic time constants of interface state

The characteristic time constant of interface states is an important parameter for interface density states. This section shows calculations of the characteristic time constant of interface states across the band gap in Ge. Based on this result, the conventional interface state measurement method discussed in prior sections including capacitance-based or conductance-based methods are investigated when they are applied to Ge-based MOS.
Recalling equation (4.8) and (4.9), then the characteristic time of the interface states can be calculated over the full band gap using the parameter values of
Table 4.1. The characteristic time constant τ, and its corresponding characteristic frequency f are given by the following equation:

$$2\pi f\tau = 1 \qquad (4.28)$$

The characteristic frequency of interface states for electrons and holes in Si and Ge as a function of the energy within the bandgap using the parameters given in Table 4.1, are shown in Fig. 4.9.

Table 4.1. Parameters used for calculation of Fig. 4.9.

Parameters	**Units**	**Material**
		Ge
Band gap	eV	0.66
Effective density states for conduction band N_C	cm^{-3}	1.0×10^{19}
Effective density states for valence band N_V	cm^{-3}	5.0×10^{18}
Electron thermal velocity v_{th}^{n}	cm/s	3.1×10^{7}
Hole thermal velocity v_{th}^{p}	cm/s	1.9×10^{7}
Capture cross section of interface state for electron σ_n	cm^{-2}	0.7×10^{-14}
Capture cross section of interface state for hole σ_p	cm^{-2}	10^{-15}

In Table 4.1, effective density states and thermal velocity are properties of Ge, their value can be found in the literature [6]. The capture cross section is a property of the interface state. For electrons, the capture cross section can be extracted from experimental data. For holes, the capture cross section is used as for silicon; 10^{-15} cm^{-2} which is a typical value of capture cross section of interface states [7].

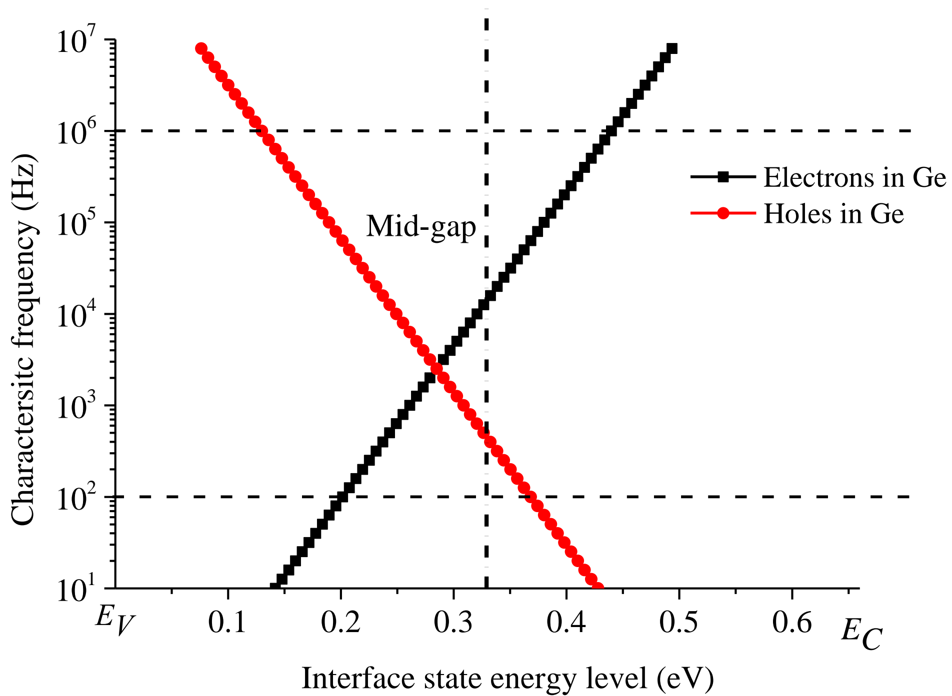

Fig. 4.9. Characteristic frequencies of interface states for electrons and holes in Ge.

As shown in Fig. 4.9, the dashed horizontal lines indicate the frequency range available for measurement, taken as 100 Hz–1 MHz. Although the interface states with a characteristic frequency beyond this range could still contribute to the frequency dispersion in *C-V* or *G-V* characteristic. However, only interface states with a characteristic frequency located within this range can be measured accurately by the capacitance-based or conductance-based methods as discussed in previous sections.

4.8 Low-high frequency method

Firstly recall the low-high frequency method whereby a high frequency small signal is applied to extract C_s, by assuming that all the interface states across the band gap cannot follow the signal. However, referring to the characteristic frequencies of interface states in Ge as shown in Fig. 4.9 (a), for the upper half of the band gap, the interfaces states with characteristic frequency higher than 1 MHz are distributed within the range from 0.43 eV (=E - E_V) to the conduction band edge. There is a significant fraction of interface states with high characteristic frequency that can still follow a 1 MHz ac signal. To quantitatively explain this, recall Eqs (4.24) and (4.25) in the depletion region, these two equations are still correct to express the electrical characteristics of interface states. Equation (4.25) can be written as:

$$G_P = qD_{it}(2\tau_n)^{-1}\ln\left[1+(\omega\tau_n)^2\right] \tag{4.29}$$

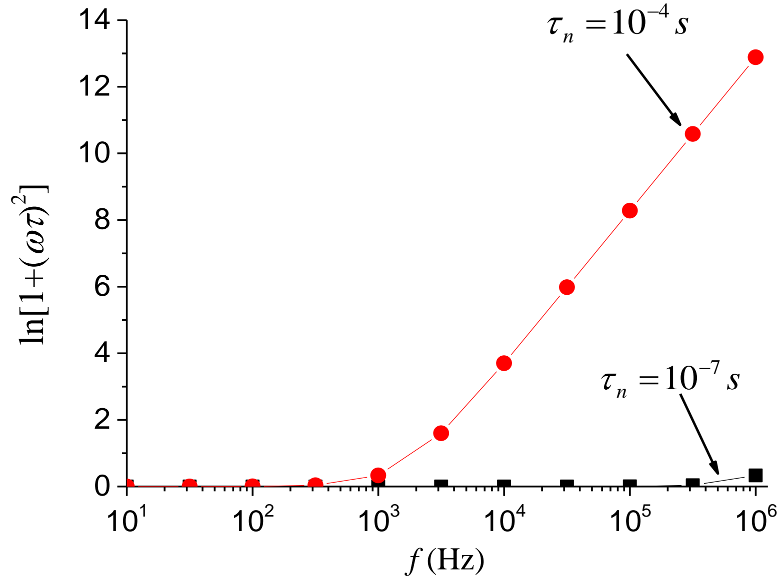

Fig. 4.10. Plot of Eq (4.29).

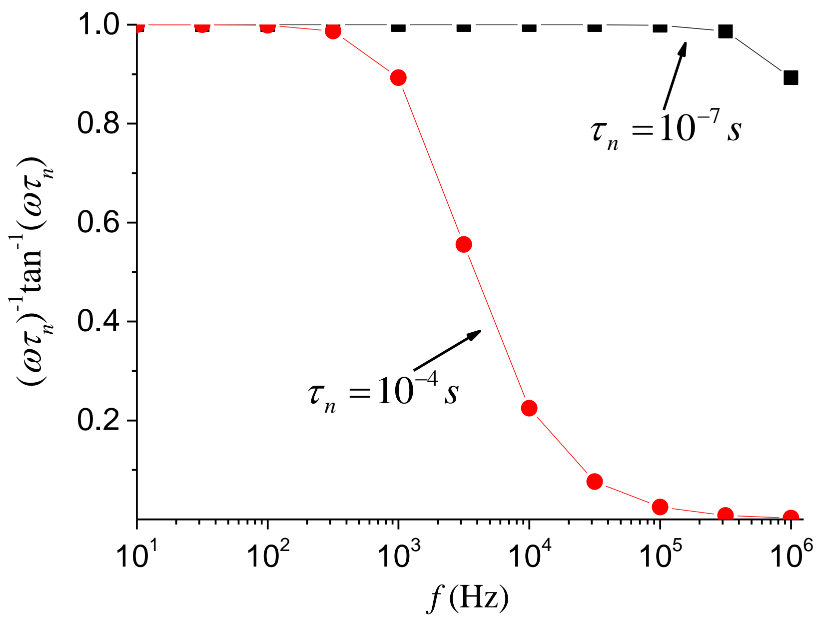

Fig. 4.11. Plot for equation Eq (4.24).

When the frequency approaches a high value (1 MHz), the interface state has a characteristic time constant of $\tau_n = 10^{-4}$ s, and C_{it} approaches 0 and G_P approaches a relatively high value as shown in Fig. 4.10 and Fig. 4.11. This is equivalent to saying that the interface states cannot respond at such a high frequency; that is, such interface states do not affect *C-V* or *G-V* which is also the reason why the equivalent circuit of Fig. 4.6 can be obtained at high frequency.

However, when the characteristic time constant of interface states is small (τ_n = 10^{-7} s), the 1 MHz frequency is not high enough to satisfy the condition to obtain such an equivalent circuit. Therefore, the C_{it} and G_P can still affect *C-V* or *G-V*, which means even at very high frequency (1 MHz), the interface states with high characteristic frequency higher than 1MHz can follow the signal which could lead to errors in the extraction of C_S. Thus the extracted C_S from 1 MHz *C-V* is no longer accurate due to the introduction of the significant part of interface states with high characteristic frequency. Similar for the lower half of the band gap in Ge, there is a significant fraction of interface states with high characteristic frequency existing in the range from 0.13 eV (= E - E_V) to the valence band edge. Overall, due to the presence of a significant fraction of interface states with quite high characteristic frequency, the low-high frequency method cannot be applied to measure interface states in Ge.

4.9 Conductance method

For the conductance method, G_p / ω is plotted as a function of ω to extract the density of interface states by reading the maximum of G_p / ω at ω = 1.98 / τ_n. However, for interface states with the characteristic frequency higher than 1 MHz, the maximum of G_p/ω cannot be read. This is illustrated in Fig. 4.12, where the maximum of G_p / ω cannot be observed as the frequency limit of the characteristic frequency near around band edge, because it is out of range of the available frequency range (100 Hz -1 MHz). Thus, the conductance method cannot measure the interface states round the band edge at room temperature.

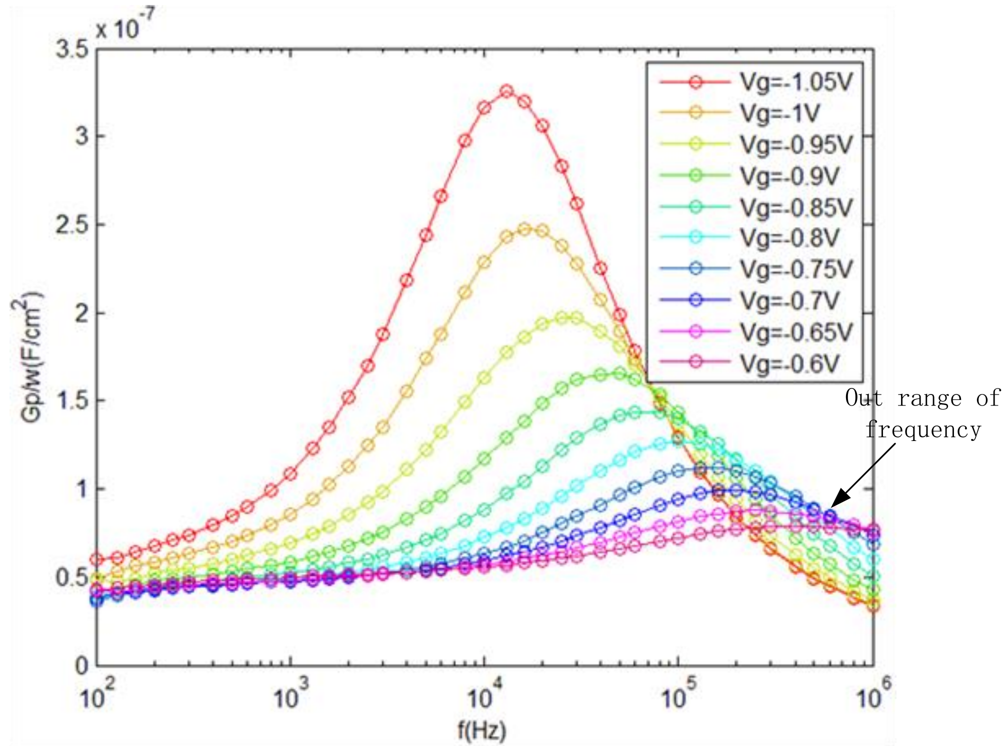

Fig. 4.12. G_p / ω plot for experimental data measured from sample Ge39S1. The corresponding position of interface states over the band gap is at E_C - E = 0.13 eV when V_g = -0.65 V.

Thus, due to the band gap properties of Ge, the available range of bandgap for Ge-based MOS which can be measured by the conductance method is different from conventional Si-based MOS. For p-type Ge, interface states lying 0.14 eV above the valence band edge to mid-gap can be measured. For MOS structures on n-type Ge, the states located from 0.13 eV (= E_C - E) to mid-gap can be measured. The interface states lying closer to the valence and conduction band edge are not accessible using the conductance method in Ge MOS. In total, there is a significant part of the band gap close to the conduction or valence band edge that cannot be sensed.

4.10 Terman's method

For the Terman's method, both fast and slow states are measured. The measured interface state density would be higher than that measured using the low-high frequency and conductance methods [8]. The density of interface states extracted using Terman's method usually is over-estimated due to the presence of slow traps, because the stretch-out of the *C–V* plot can be caused by both slow traps and interface states. Even when the stretch-out is only caused by interface states, the Terman's method based on the 1 MHz *C–V* is unlikely to yield correct answers, because there is a fraction of interface states near the band edge with small time constant.

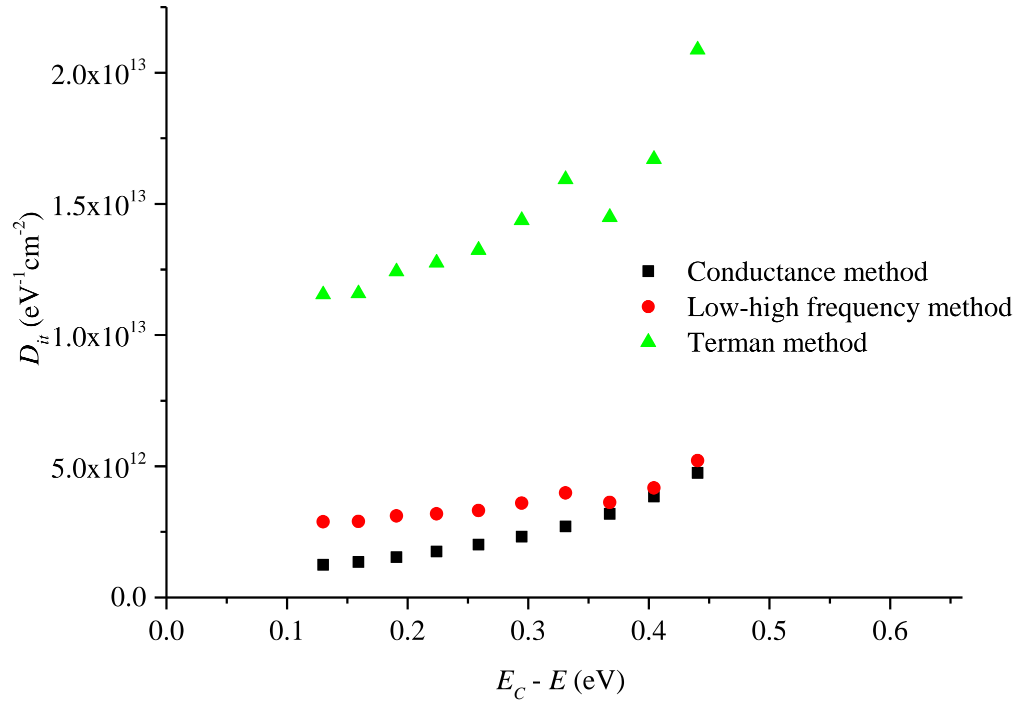

Fig. 4.13. The density of interface states obtained using different methods experimentally measured from sample Ge39S1.

In Fig. 4.13, the D_{it} measured by the Terman's method is much higher than those obtained by the conductance and low-frequency method.

To conclude, both low-high and Terman's based methods fail when applied on Ge-based MOS. In addition, Terman's method could overestimate the D_{it} due to the presence of slow traps as shown in Fig. 4.13. Comparing between the conductance and low-high frequency methods, it shows that the interface states measured by the low-high frequency method is higher than measured by the conductance method as shown in Fig. 4.13. This is because for low-high frequency method, it lacks a sufficiently high frequency *C-V* which can exclude the effect of interface states. The conductance method is still available to measure the density of interface states when it is applied on Ge MOS, however, this method is not effective to measure the interface states near the valence or conduction band edge in Ge at room

temperature. Overall, the conductance method can measure the interface states in Ge-based MOS, and a solution should be proposed to measure all the interface density states.

4.11 Three issues for the conductance method

As discussed before, the conductance method is preferred compared to the low-high frequency and Terman's methods. However, three issues for the application of the conductance method should be taken into account when applied to Ge-based MOS.

4.11.1 First issue: Low-T measurement

A possible solution to measure interface states near to the band edges is to decrease the temperature, so that the characteristic frequencies of these interface states can be located within the available frequency range of 100 Hz – 1 MHz. Calculation of the corresponding characteristic frequencies of interface states in Ge at different temperature are shown in Fig. 4.14. It can be seen that by decreasing temperature, the interface states near the band edges exhibit lower characteristic frequency which is approaching the available frequency range of 100 Hz – 1 MHz.

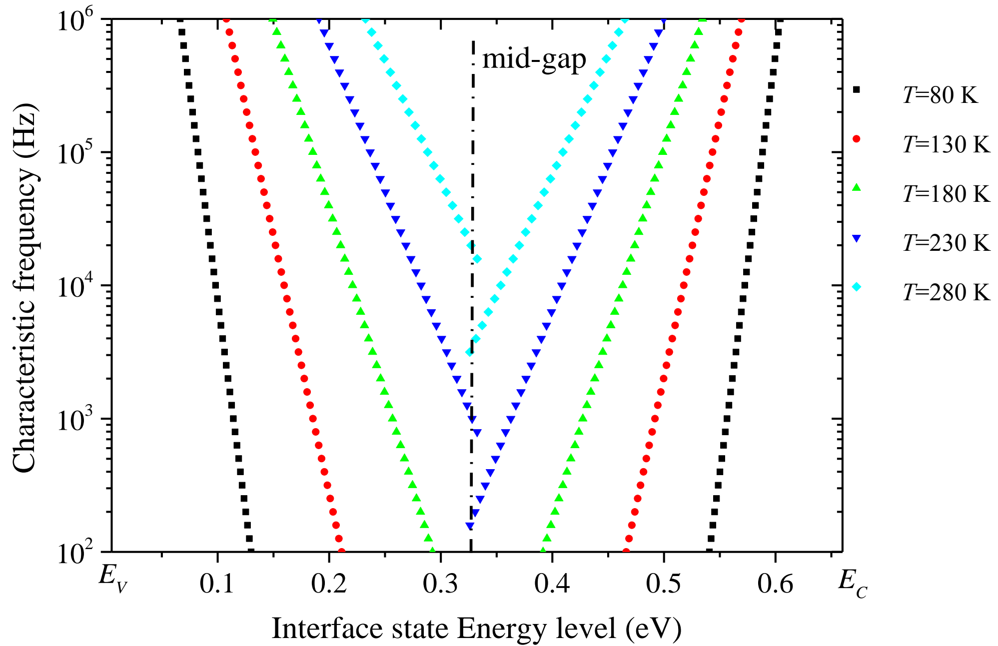

Fig. 4.14. The characteristic frequencies of interface states for holes (from E_V to mid-gap) and electrons (from E_C to mid-gap)

4.11.2 Second issue: the condition for characteristic constants of interface state for majority carriers is much smaller than that for minority carriers in depletion

The use of the conductance method has been questioned [9]. The concern relates to whether the condition that characteristic time constant of interface states for minority carriers is much

smaller than that for majority carriers in depletion is still satisfied as it is for conventional Si-based MOS. By looking at Fig. 4.9, it can be seen that for n-type Ge, this condition is still satisfied from the conduction band to mid-gap. The characteristic time constant of majority carriers (electrons) is smaller than that for minority carriers, as discussed before, Thus for the conductance method in n-type Ge, the measured range of the band gap is from conduction band to mid-gap. However, for p-type Ge-MOS, from valence band to mid-gap, the condition is not satisfied when the interface state location crosses mid-gap. This means that the conduction method cannot be used to measure accurately the interface states near mid-gap for p-type Ge-based MOS.

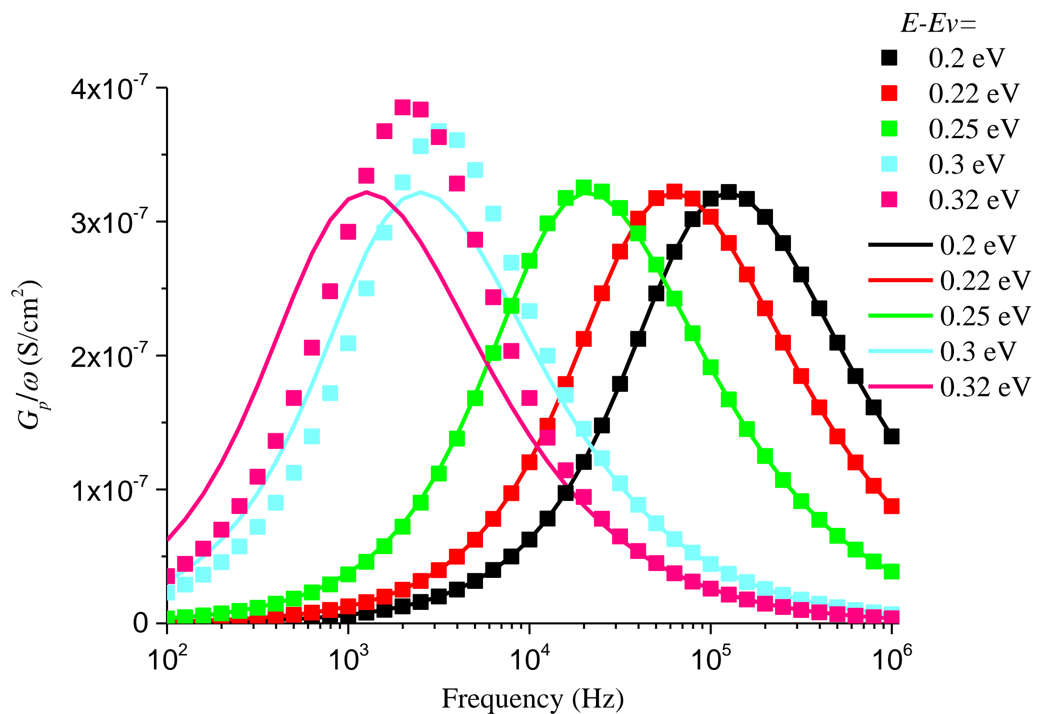

Fig. 4.15. The solid line is the calculation of G_P / ω plot for the conductance method for p-type Ge MOS based on the circuit of Fig. 4.4 (b) which considers both majority and minority carrier exchange with conduction and valence bands. The rectangular denote the G_P / ω plot only considering the majority charge exchange with the conduction band for n-type Ge MOS.

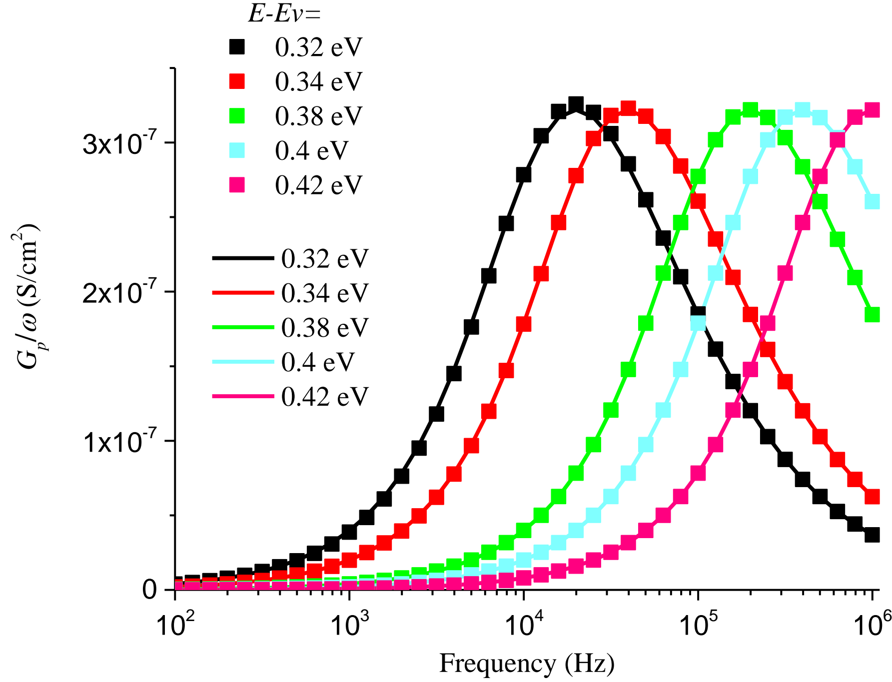

Fig. 4.16. The solid line shows the calculation of G_P / ω plot in the conductance method for n-type Ge MOS which considers both majority and minority carrier exchange with condition and valence bands. The rectangular plots denote the G_P / ω plot only considering the majority change exchange with conduction band for p-type Ge MOS.

Fig. 4.15 shows calculations around mid-gap, for p-type Ge, The peak value of G_P / ω based on the conductance method circuit is lower than the model considering both majority and minority carrier exchange. Thus the conductance method will lead to over-estimation around mid-gap for p-type MOS. However, for n-type, when the Fermi level approaches mid-gap, the condition for the conductance method is satisfied as shown in Fig. 4.16, the conductance method is still correct to use.

To summarize, for Ge-based MOS around mid-gap, for n-type (upper half of the band gap) the conductance method can be employed. However, for p-type (lower half band gap), around the mid-gap, the conductance method should be used carefully, because the lifetime of majority carriers (holes) can be larger than that of the minority carriers. The condition for use of the conductance method is not satisfied and will lead to over-estimation of the density of the interface states.

4.11.3 Third issue: generation of minority carriers after the Fermi level crosses mid-gap

When the Fermi level moves from the conduction band to mid-gap (n-type), the thermal generation of minority carriers will affect the measurement. For n-type Ge, the condition (τ_n << τ_p) of the conductance method is still true after mid-gap as shown in Fig. 4.9. This implies that the range which can be measured is more than half the upper band gap for n-type Ge-

based MOS. However, after mid-gap, the generation of minority carriers in Ge is significant and must be taken into account. The generation of minority carriers is mainly from two sources, namely diffusion from the bulk substrate and thermal generation within the depletion region [10]. The generation of minority carriers leads to a sharp increase of the peak in the G_P / ω plot and thereby could lead to the erroneous measurement of interface states beyond mid-gap. The diffusion-induced minority carrier response is modelled by inserting a conductance G_d and the thermal generation conductance can be expressed as G_{gr} in Fig. 4.17.

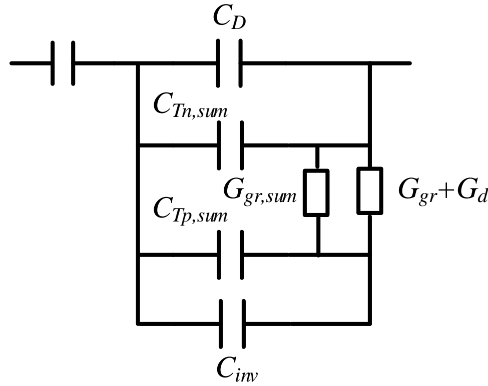

Fig. 4.17. The equivalent circuit considering the diffusion and thermal generation components of minority carriers beyond mid-gap.

In Fig. 4.17, the equivalent circuit is modified from circuit Fig. 4.5 (b), to take account of both interface states and the minority carrier generation for n-type Ge.

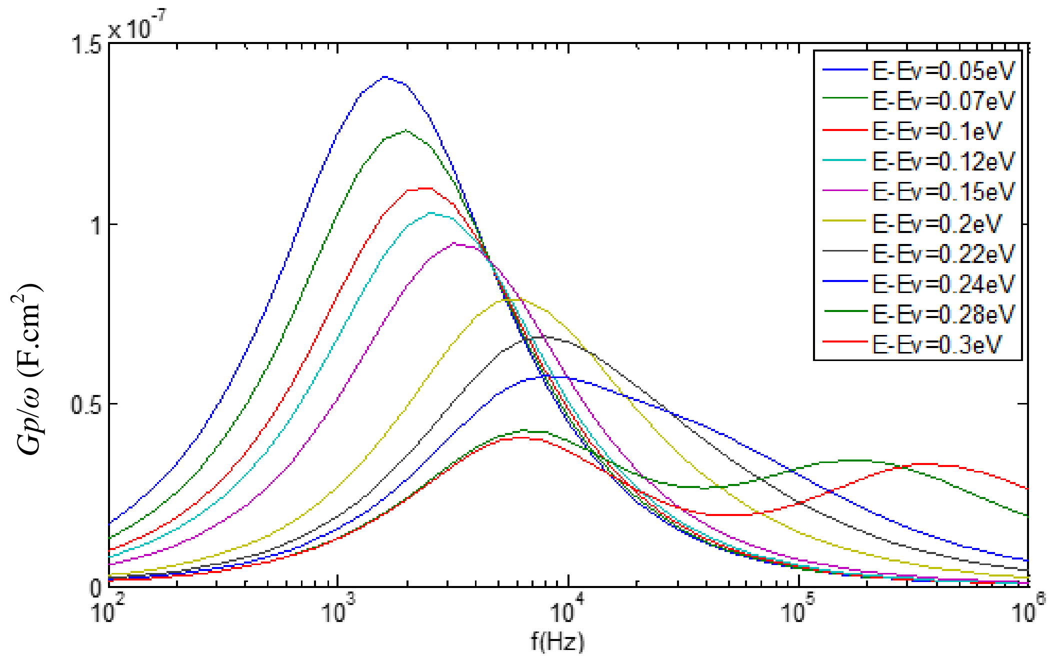

Fig. 4.18. Calculation of G_P / ω plots considering the G_d and G_{gr} based on the equivalent circuit of Fig. 4.17.

In Fig. 4.18, after the Fermi-level goes beyond the mid-gap (from $E - E_V = 0.33$ eV to $E - E_V = 0.05$ eV), there is a sharp increase in the peak value of G_p / ω. This will lead to an over-estimation of the density of interface states. This figure can explain the experimental data in Fig. 4.12, as the mid-gap position is achieved when gate voltage $V_g = -0.9$ V; when $V_g < -0.9$ V, the minority carrier generation is responsible for the sharp increase in the peak value of G_p / ω. Thus, the generation of minority carriers in Ge after mid-gap leads to a sharp increase of the peak value.

4.12 Conclusions

To conclude, methods to measure the interface state density in Ge-based MOS with CV measurements have been presented and discussed. The low-high frequency method fails in measurement of interface state density in Ge-based MOS, because the extraction of C_S from *C-V* at the 1 MHz. has been affected by interface states with high characteristic frequency. Terman's method suffers from the same problem. In addition, Terman's method measures both slow traps and interface states, the presence of slow traps will over-estimate the extracted interface state density. The conductance method is preferable but low temperature is required to sense interface states near band edges in both n- and p-type Ge-based MOS. Besides, for the conductance method, two other issue have been investigated: firstly, the measurement near mid-gap is correct for n-type Ge-based MOS, because the condition $\tau_n << \tau_p$ is still satisfied. Secondly, the effects of minority carrier generation around mid-gap is calculated which shows the sharp increase of peak value of G_P / ω after mid-gap.

4.13 References

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Chapter 5 Electrical characterization of samples

In this chapter, The *C-V* characteristic for different samples are presented. The interface state density is measured to evaluate the quality of interface between Ge and the stack. The method is conductance method as discussed in chapter 4. In addition, the current over voltage (*I-V*) characteristics will be presented. The dielectric constant of HfO_2 will extracted at last.

5.1 Samples with different thickness HfO_2 deposited by ALD using O-plasma as oxidant with Al_2O_3 as protection layer:

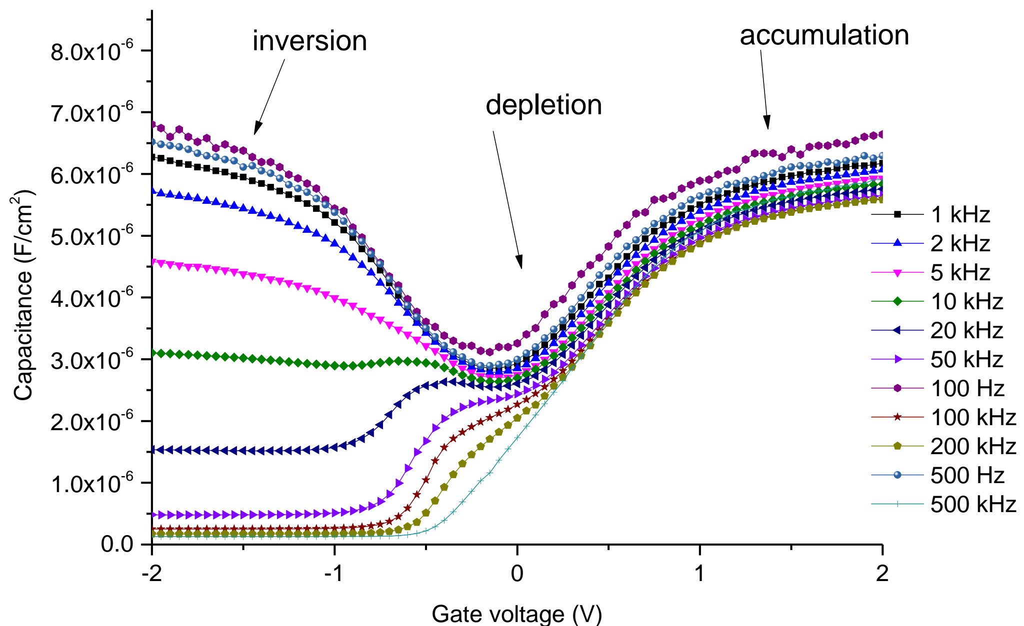


Fig. 5.1 *C-V* characteristic from sample Ge12S1 with 3.5 nm HfO2 deposited by ALD using O-plasma as oxidant with Al2O3 as protection layer in parallel measurement mode.

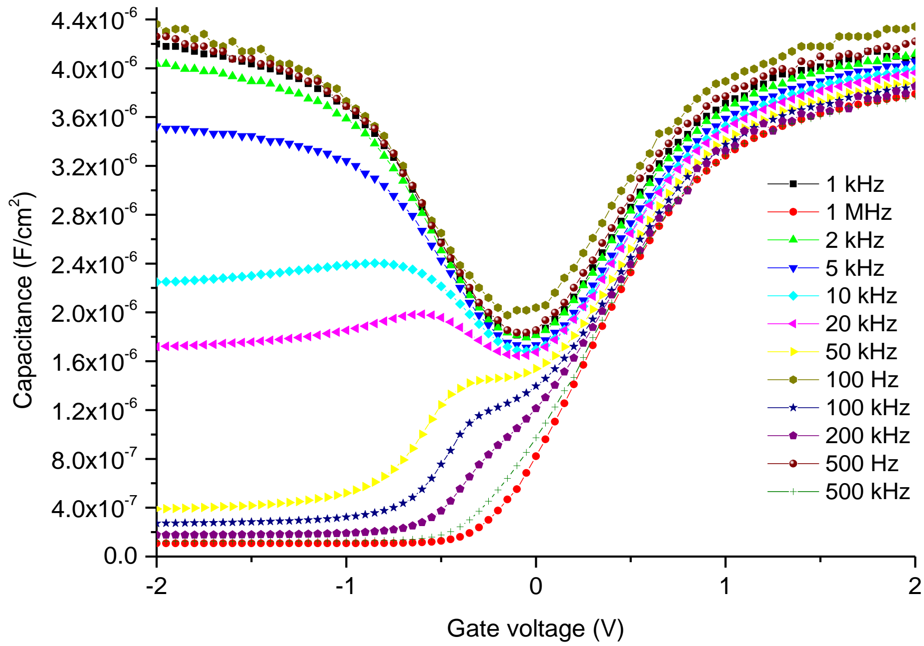


Fig. 5.2 C-*V* characteristic sample Ge12S2 with 7 nm HfO2 deposited by ALD using O-plasma as oxidant with Al_2O_3 as protection layer in parallel measurement mode.

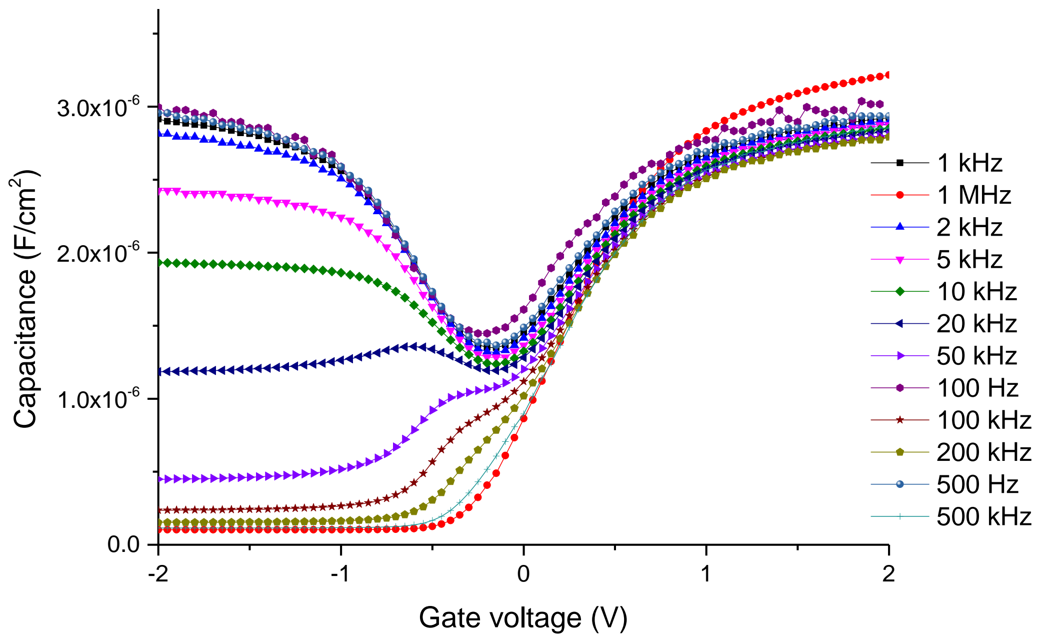


Fig. 5.3 *C-V* characteristic from sample Ge12S3 with 14 nm HfO2 deposited by ALD using O-plasma as oxidant with Al2O3 as protection layer in parallel measurement mode.

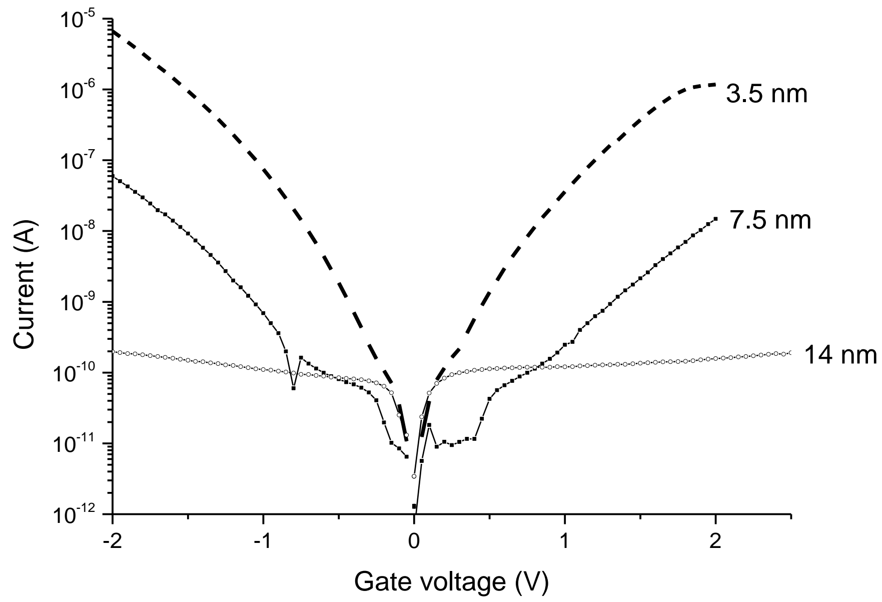


Fig. 5.4 *I-V* characteristics of sample Ge12S1 with 3.5 nm HfO_2, Ge12S2 with 7 nm HfO_2 and Ge12S3 with 14 nm HfO_2.

As shown in Fig. **5.4** the HfO_2 increase, the leakage current decreases. When the HfO_2 approaches to 14 nm, the leakage current becomes extremely low.

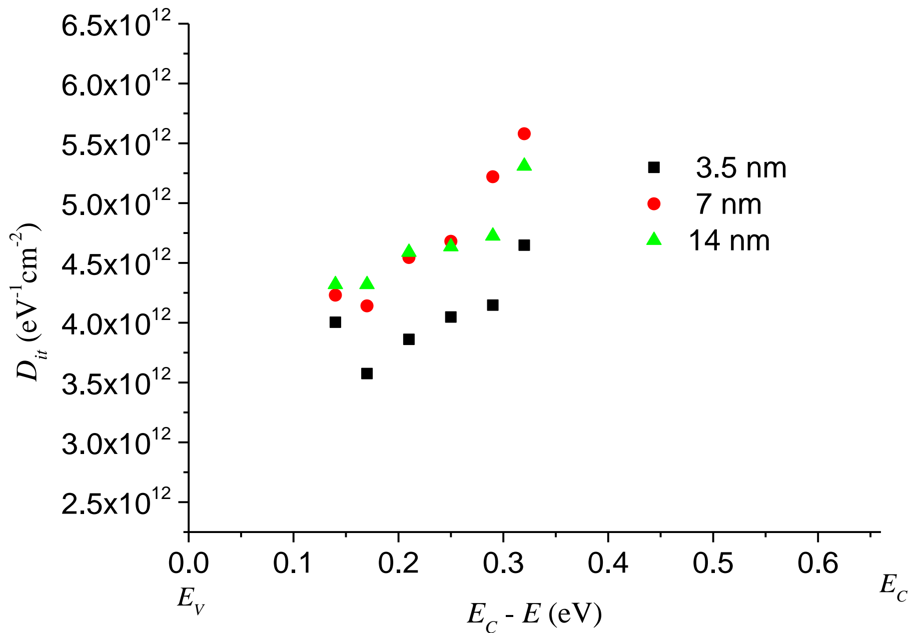


Fig. 5.5 The D_{it} distribution for the three sample with different thickness of HfO_2 with Al_2O_3 as protection layer.

In addition, the above three samples use the same thickness of GeO_2 interfacial layer, thus the dielectric constant of HfO_2 can be determined. The accumulation capacitance C_{acc} can be treated as the high-k oxide capacitance C_{hk} in series with an interfacial layer capacitance C_{IL}. In accumulation, the capacitance can therefore be given by:

$$\frac{1}{C_{acc}} = \frac{1}{C_{hk}} + \frac{1}{C_{IL}} \tag{5.1}$$

In the above three samples, the thickness of the interfacial layer is unchanged and thus C_{IL} is constant.

$$\frac{1}{C_{acc}} = \frac{1}{C_{hk}} + \frac{1}{C_{IL}} \tag{5.2}$$

Because

$$C_{hk} = \varepsilon_{hk} / t_{hk} \tag{5.3}$$

Substitute Eq (5.3) into Eq (5.2), then

$$1/C_{acc} = t_{hk}\frac{1}{\varepsilon_{hk}} + \frac{1}{C_{IL}} \tag{5.4}$$

Plotting $1/C_{acc}$ versus t_{hk} gives slope of $1/\varepsilon_{hk}$. A value of $\varepsilon_{hk} = 22$ is extracted from the graph shown in Fig. 5.6.

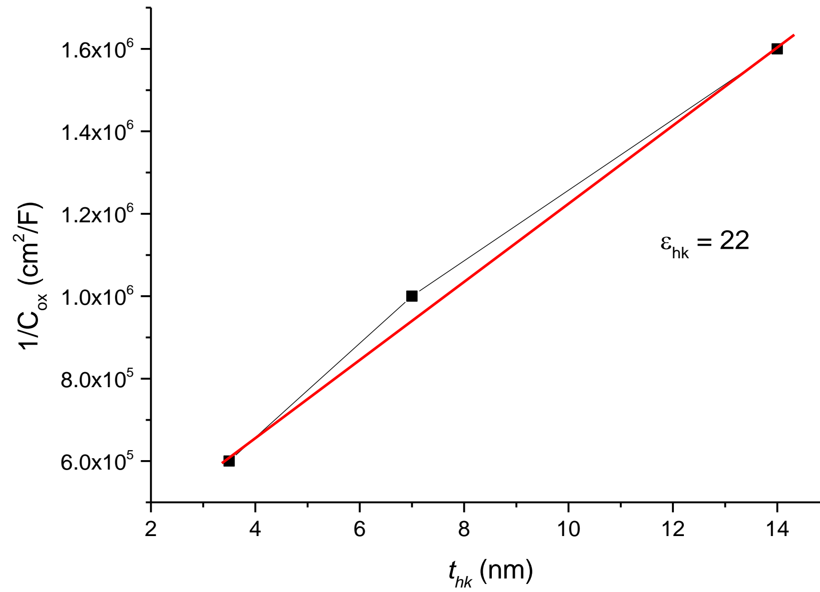


Fig. 5.6 The extraction of high-κ dielectric constant through $1/C_{ox}$ as a function of thickness for HfO_2.

The extracted ε_{hk} is 22 which is close to dielectric constant 25 of HfO_2 [1].

As shown in Fig. 5.1-Fig. 5.3, frequency dispersion is observed in depletion and accumulation and attributed to fast minority carrier response, interface states D_{it} and oxide traps respectively, as will be discussed in detail in later chapters. The interface state density was extracted by employing the conductance method. The Berglund integral method [8] was used to obtain the relationship between surface potential and gate voltage. Shows the D_{it} for the three different thickness of HfO_2. The figure shows that the interface state density is the order of 10^{12} eV^{-1} cm^2 for all thicknesses of high-*κ* oxide for the first group of samples with Al_2O_3 as the protecting layer.

5.2 Samples comprising gate stacks with different thickness HfO_2 deposited by ALD using O-plasma as oxidant:

Similarly, the *C-V* characteristics for S-treated samples and ALD using O-plasma are shown in Fig. 5.7-Fig. 5.9.

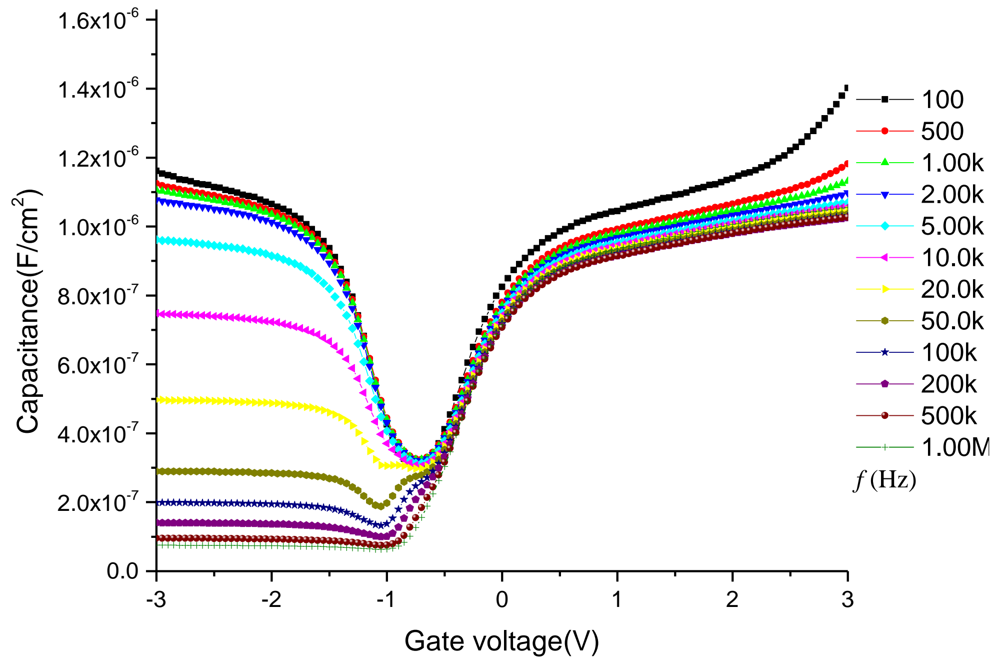


Fig. 5.7. *C-V* characteristics from sample Ge39S1 comprising HfO_2/S/Ge gate stacks with 3.5 nm HfO2 deposited by ALD using O-plasma as oxidant in parallel measurement mode.

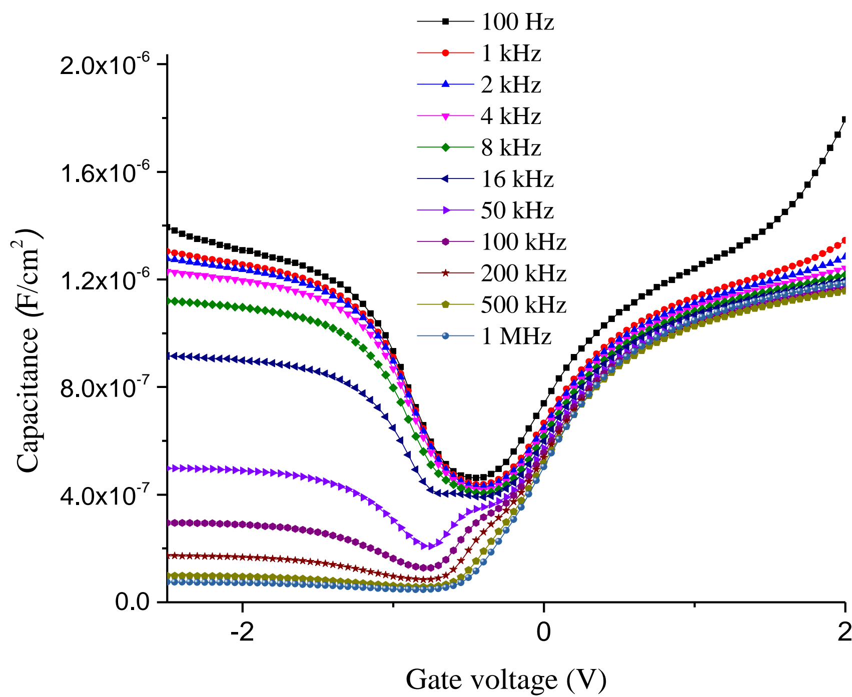


Fig. 5.8. *C-V* characteristics from sample Ge39S2 comprising HfO_2/S/Ge gate stack 7 nm HfO2 deposited by ALD using O-plasma as oxidant in parallel measurement mode.

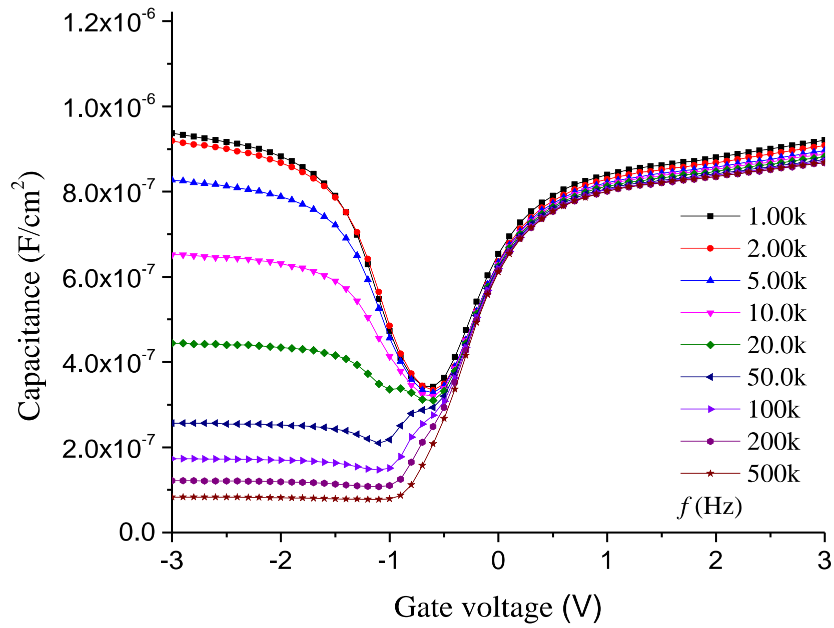


Fig. 5.9. *C-V* characteristics from sample Ge39S3 comprising HfO_2/S/Ge gate stack 15 nm HfO2 deposited by ALD using O-plasma as oxidant in parallel measurement mode.

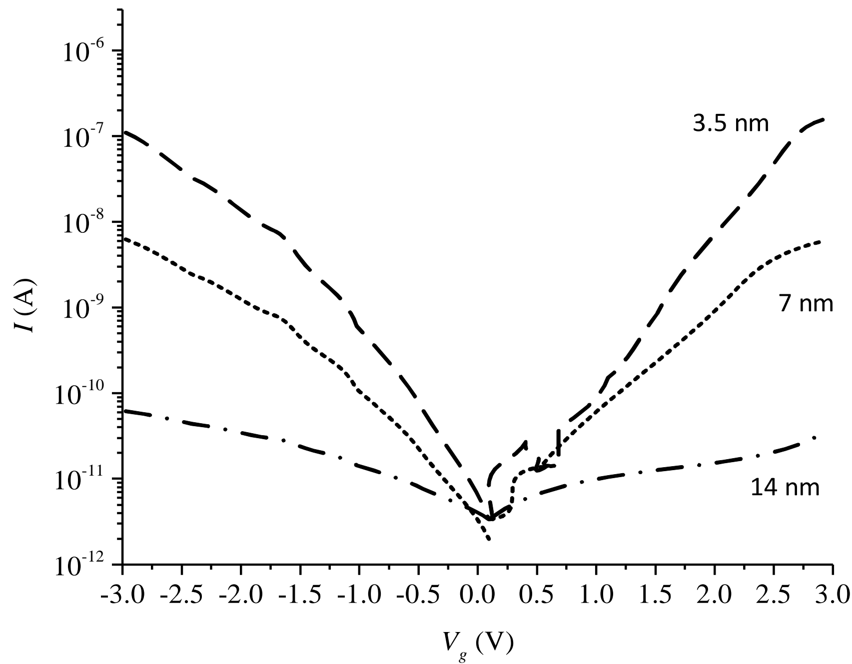


Fig. 5.10. The *I-V* characteristics of sample Ge39S1 with 3.5 nm HfO_2, Ge39S2 with 7 nm HfO_2 and Ge39S3 with 14 nm HfO_2.

Fig. 5.11-Fig. 5.13 show plots of G_P / ω, from which the interface state densities can be obtained:

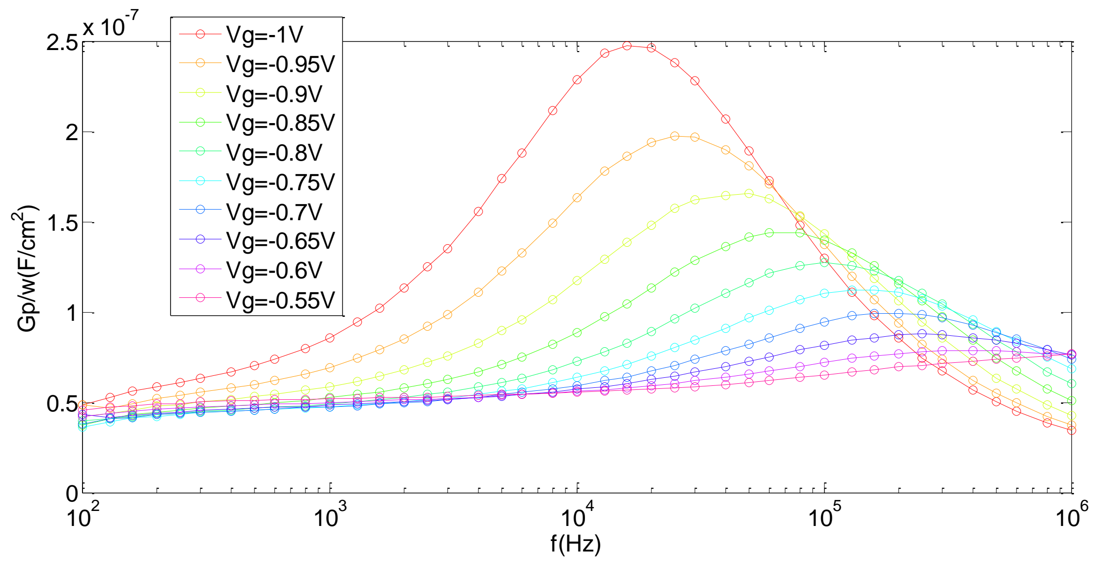


Fig. 5.11. Plot of G_P / ω corresponding to Fig. 5.7.

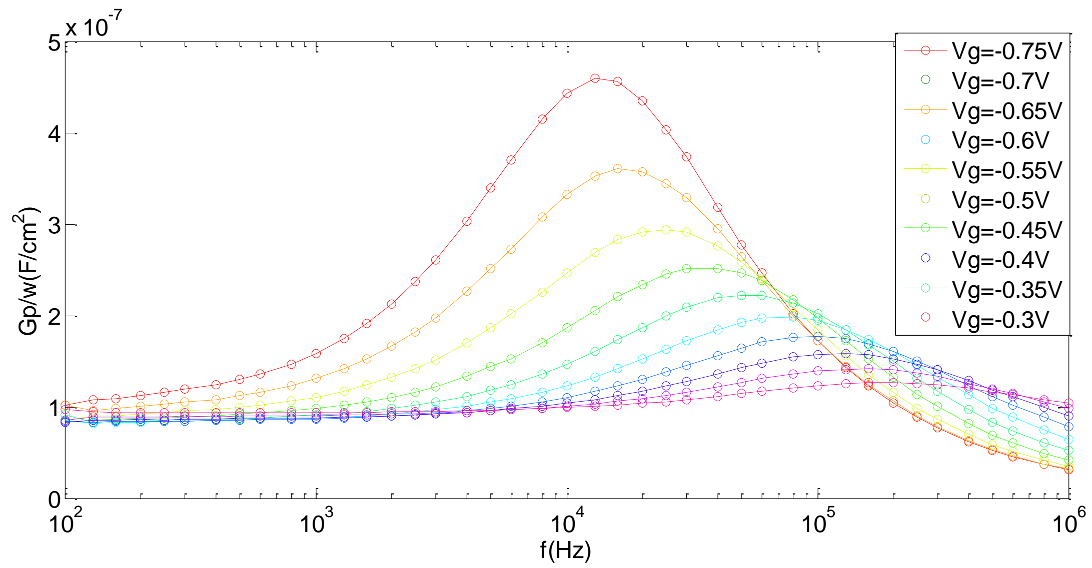


Fig. 5.12. Plot of G_P / ω corresponding to Fig. 5.8.

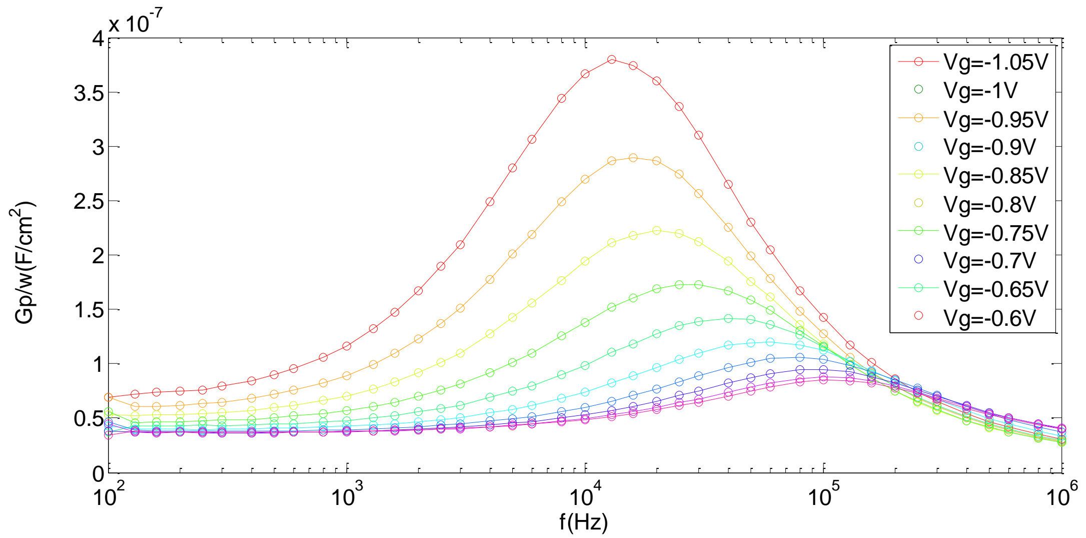


Fig. 5.13. Plot of G_P / ω corresponding to Fig. 5.9.

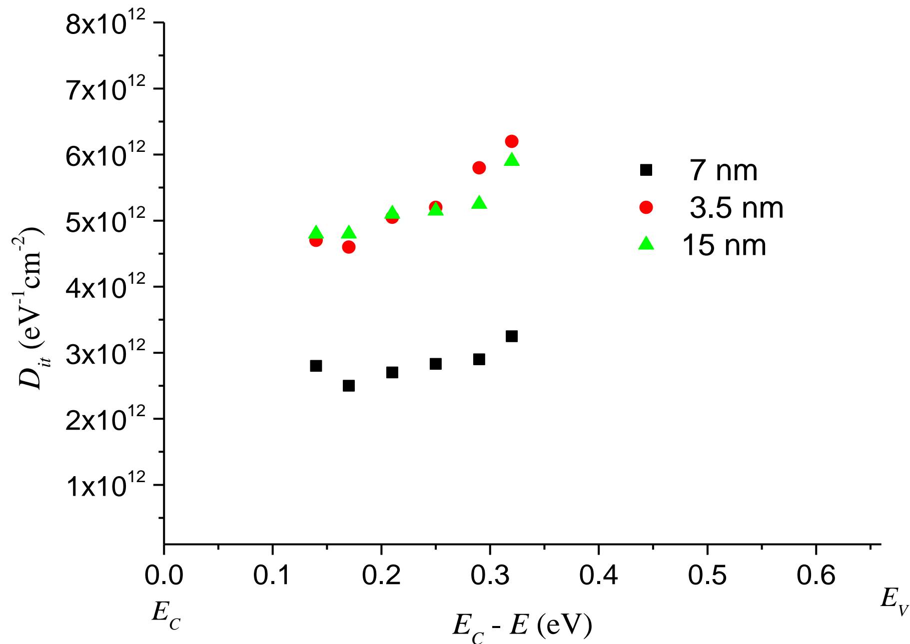


Figure 5.14. The D_{it} distribution for the three sample with different thicknesses of HfO_2.

From, it can be observed that the minimum D_{it} is 2.5×10^{12} eV^{-1}cm^{-2}. Compared to the first group of samples which employs Al_2O_3, the S-treated samples exhibit the same order of magnitude of interface state density; about 10^{12}. This figure shows that the interface state density is the order of 10^{12} eV^{-1}cm^{2} for different thicknesses of high-κ/Ge stack for S-passivated samples. In addition, as discussed before, S-treated with another sub-nm Al_2O_3 (sample (Ge39S4)) is measured to compare with sample Ge39S1 without the Al_2O_3 layer. The *C-V* characteristic is shown in Fig. 5.15.

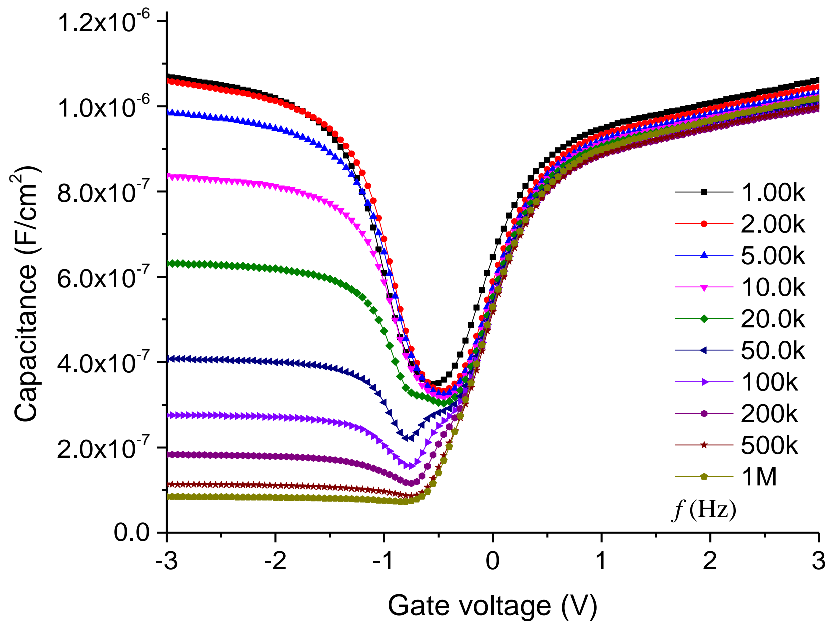


Fig. 5.15. *C-V* characteristics from sample Ge39S4 comprising $HfO_2/Al_3O_2/S/Ge$ gate stack in parallel measurement mode.

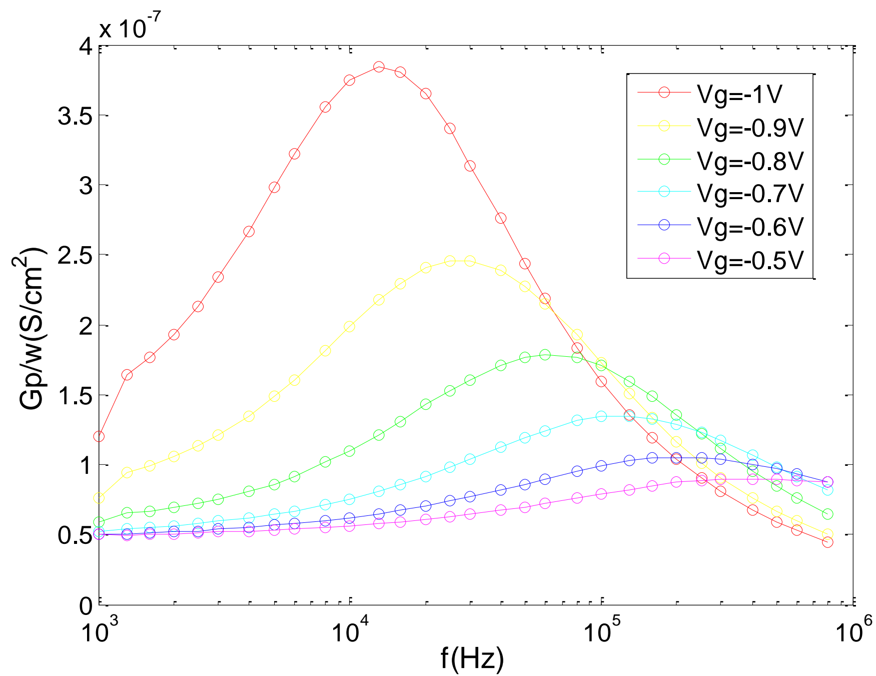


Figure 5.16 Plot of G_P / ω corresponding to Fig. 5.15.

Compared to the S-treated samples with and without Al_2O_3, there is no significant improvement of the interface as shown in Fig. 5.17**Error! Reference source not found.**. The introduction of Al_2O_3 does not further enhance the interface quality.

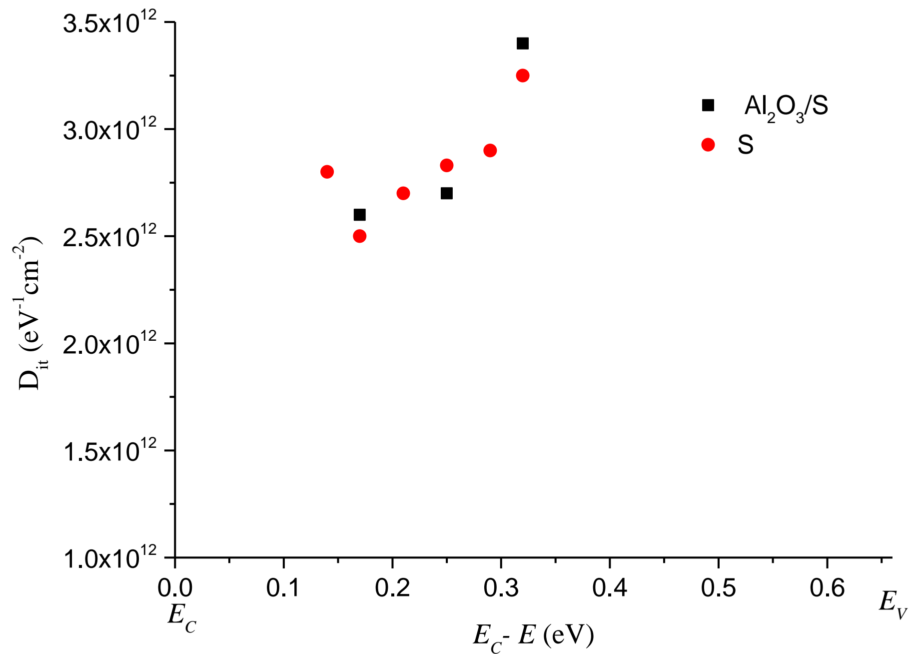


Fig. 5.17 Comparison of interface state density for of S-treated sample Ge39S1 and S/sub-nm Al_2O_3 sample Ge39S4.

5.3 Reference

[1] J. Robertson and R. M. Wallace, “High-K materials and metal gates for CMOS applications,” Materials Science and Engineering: R: Reports, vol. 88, pp. 1-41, 2015.

Chapter 6 Bound states within the notch of the HfO_2/GeO_2/Ge stack

A model is presented to allow calculation of the bound states in the conduction band notch at the interface between the interfacial native GeO_2 and high-κ dielectric layer in a Ge MOSFET gate stack. The notch represents a potential charge trapping site, which can induce threshold voltage instability. The model is applied to a three-dimensional structure, and the number of electrons or average occupancy of confined electrons in the notch is calculated. The effect of device physical and electrical parameters on the number of bound states and average occupancy of states in the notch is discussed. The significance of the confined charge in the notch and its effect on the threshold voltage shift in an 8-nm node Ge MOSFET is investigated. The main conclusion is that charge storage in this notch is insignificant at the relevant technology node.

Fundamental aspects of quantum and statistic mechanics is described first, in order to explain the physical principles behind the model. Then the details of the model are presented.

6.1 Quantum and statistics mechanics

6.1.1 Time-independent Schrödinger equation [1]

Quantum mechanics describes a particle based on the time-independent Schrödinger equation,

$$-\frac{\hbar^2}{2m}\frac{\partial^2\psi}{\partial x^2}+V\psi=E\psi \tag{6.1}$$

where m is the effective mass, ψ is wave function, E is energy level, and V is potential energy, $\hbar$ is reduced Planck constant. This equation can be written as:

$$\hat{H}\psi=E\psi \tag{6.2}$$

where $\hat{H}$ is the Hamiltonian operator, and

$$\hat{H}=-\frac{\hbar^2}{2m}\frac{\partial^2}{\partial x^2}+V \tag{6.3}$$

6.1.2 The electron-in-box approach [1]

Assume an electron is confined inside an infinite potential well

$$V(x)=\begin{cases}0,(0\le x\le a)\\ \infty, otherwise\end{cases} \tag{6.4}$$

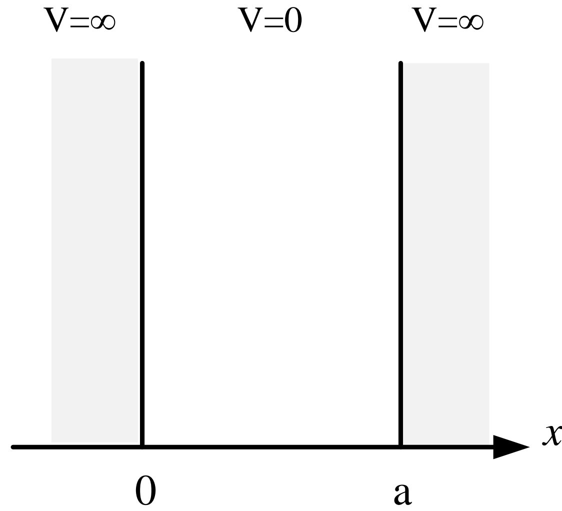


Fig. 6.1. The infinite potential well.

Inside the well, V=0, thus Eq. (6.1) can be written as:

$$-\frac{\hbar^2}{2m}\frac{\partial^2\psi}{\partial x^2} = E\psi \tag{6.5}$$

The general solution for this equation is:

$$\psi(x) = A\sin(kx) + B\cos(kx) \tag{6.6}$$

where A and B are arbitrary constants and are fixed by the boundary conditions. Referring to the potential well used, B should be 0 to satisfy the boundary conditions. Hence, solutions can be expressed as

$$\psi(x) = A\sin(k_n x) \tag{6.7}$$

where

$$k_n = \frac{n\pi}{a}, \text{ with } n = 1, 2, 3, \ldots \tag{6.8}$$

Hence the possible values of E are given as

$$E_n = \frac{\hbar^2 n^2 \pi^2}{2ma^2} \tag{6.9}$$

In such a potential well, electrons can only exist at certain discrete energy states as shown in Fig. 6.2. To find A, ψ can be normalized as:

$$\int_0^a \psi(x)^2\,dx = \int_0^a |A|^2 \sin^2(k_n x)dx = |A|^2 \frac{a}{2} = 1 \tag{6.10}$$

thus A can be derived:

$$|A| = \sqrt{\frac{2}{a}} \tag{6.11}$$

Pick the positive real root, $A = \sqrt{2/a}$; finally the wave function solutions are derived as:

$$\psi_n(x) = \sqrt{\frac{2}{a}} \sin\left(\frac{n\pi}{a} x\right) \tag{6.12}$$

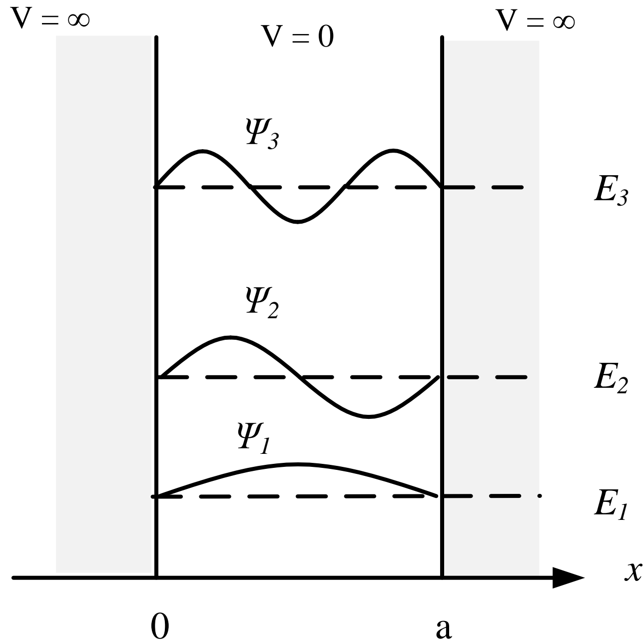


Fig. 6.2. The first three stationary states of the infinite potential well.

These functions have two important properties which will be employed to solve problems in this chapter later.

Firstly, they are mutually orthogonal.

$$\int \psi_m(x)^* \psi_n(x) dx = 0 \tag{6.13}$$

Whenever $m \neq n$

This statement can be further expressed by the Kronecker delta function:

$$\int \psi_m(x)^* \psi_n(x) dx = \delta_{mn} \tag{6.14}$$

Where δ_{mn} is defined as:

$$\delta_{mn} = \begin{cases} 0, (m \neq n) \\ 1, (m = n) \end{cases} \tag{6.15}$$

Secondly, these equations are complete, which means any other function $f(x)$ can be expressed as a linear combination of them.

$$f(x) = \sum_{n=1}^{\infty} c_n \psi_n(x) = \sqrt{\frac{2}{a}} \sum_{n=1}^{\infty} c_n \sin\left(\frac{n\pi}{a} x\right) \tag{6.16}$$

The coefficients c_n can be evaluated for a given $f(x)$, by multiplying both sides of Eq. (6.16) with $\psi_m(x)^*$ and the integration:

$$\int \psi_m(x)^* f(x)dx = \sum_{n=1}^{\infty} c_n \int \psi_m(x)^* \psi_n(x)dx = \sum_{n=1}^{\infty} c_n \delta_{mn} = c_m \tag{6.17}$$

thus the n'th coefficient in the expansion of $f(x)$ is

$$c_n = \int \psi_n(x)^* f(x)dx \tag{6.18}$$

These two properties are very useful, and they are not specific to the infinite square potential well.

6.1.3 Three dimensional box [2]

Above, the one dimensional potential well is discussed. This part will extend to 3-Dimension (3-D) potential well. Assume an electron is confined inside of a 3-D potential box and each axis can be treated independently, the time-independent Schrödinger equation of 3-D is expressed as:

$$-\frac{\hbar^2}{2m}\nabla^2\psi(x,y,z) + V(x,y,z)\psi(x,y,z) = E\psi(x,y,z) \tag{6.19}$$

Finally the permitted energy levels in 3 dimensional can be given by:

$$E_n = \frac{\hbar^2}{2m}\left[\left(\frac{n_x\pi}{L_x}\right)^2 + \left(\frac{n_y\pi}{L_y}\right)^2 + \left(\frac{n_z\pi}{L_z}\right)^2\right] \tag{6.20}$$

6.1.4 The Grand Canonical Ensemble [3]

In statistical mechanics, a grand canonical ensemble is the statistical ensemble that is used to represent the possible states of a mechanical system of particles that is being maintained in thermodynamic equilibrium (thermal and chemical) with a reservoir. The average value for an occupancy number P based on Fermi–Dirac statistics in a canonical ensemble can be given by the equation:

$$P = \frac{1}{\exp\left(\frac{E_i - E_f}{kT}\right) + 1} \tag{6.21}$$

where E_i is the energy level and E_f is the Fermi level.

6.2 Introduction of the "Notch"

As discussed before, Ge native dielectrics such as GeO_2, GeON, and Ge_3N_4 are employed as the interfacial layer between the Ge substrate and high-κ dielectric with the native oxide being currently the most promising solution [4]. Furthermore, the use of HfO_2 technology as the high-κ material is attractive due its acceptance in standard Si processing [5].

The use of a stack comprising of GeO_2 and HfO_2 brings a particular problem for the n-channel device [6] as depicted in Fig. 6.3 and now described below. The conduction band offset between Ge and the native GeO_2 dielectric ($E_{C,\ IL}$ = 0.8-1.5 eV [7]) is smaller than the corresponding conduction band offset for a high-κ dielectric ($E_{C,\ HK} \approx 2$ eV [8]). Therefore, in the inversion condition, the band alignment between interfacial layer (IL) and high-κ can cause a potential well or "notch". In addition, for p-channel MOSFETs, the valence band off-set between Ge and GeO_2 is higher than the corresponding valence band off-set for HfO_2 [5], thus there is such notch no potential well could exist in inversion mode in this case. There is controversy on the values of conduction band offset between Ge and GeO_2 reported in the literature. Lucovsky *et al.,* found band offsets of 1.35–1.55 eV using ultraviolet photoemission spectroscopy measurements [5]. Values of 0.9–1.5 eV and 1.04 eV have been reported by Kobayashi *et al.,* [8] and [9] Ohta *et al.,* respectively, from x-ray photoemission spectroscopy measurements. Afanas'v *et al.,* have reported a band offset of 1.44–1.84 eV from internal photoemission measurements; however, the GeO_2 band gap they found is around 4.3 eV, more than 1 eV lower than 5.5–5.7 eV reported by the others [10]. Lin *et al.,* have calculated the conduction band offset of 0.8 eV with GeO_2 band gap of 6.1 eV [7]. Sasada *et al.,* extracted values in the range of 1.2–1.4 eV from Fowler–Nordheim plots in GeO_2 [11]. In this work, the worst case is considered, that is, the lowest reported value of 0.8 eV for the conduction band offset, which gives the highest notch depth. All other values will produce lower threshold voltage shifts.

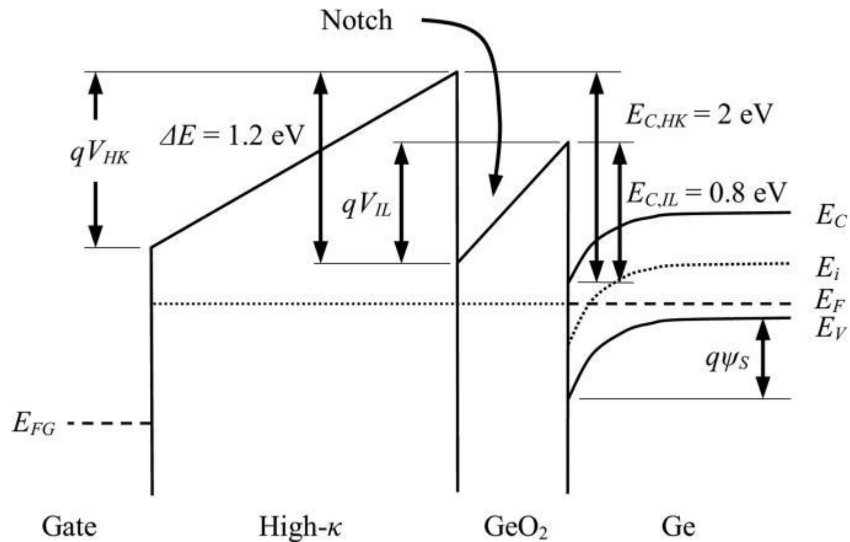


Fig. 6.3. Notch at the interface of IL and high- dielectric (after Lucovsky *et al.* [6])

The height of the barrier on the right of Fig. 6.3 is equal to the fraction of the gate voltage that falls across the interfacial layer, V_{IL}, and the height of the left barrier is dictated by the difference between conduction band offsets of Ge to high-κ dielectric and to GeO_2 as $\Delta E_{C,\ HK} = E_{C,\ HK} - E_{C,\ IL}$. Consequently, there is the possibility for bound states to exist within this

potential well, dependent upon the electric field in the stack. Electrons from the inversion layer could tunnel into this potential well and occupy the bound states, thus these electron hold within the notch could induce a threshold voltage shift. Theoretical simulations are used to model the electrical behavior of the "notch" and hence estimate the threshold voltage shift induced by the charge stored there.

6.3 Modelling

The model is based on the numerical solution of the Schrödinger equation coupled with the calculation of induced threshold voltage by those electrons confined within notch of the simulated structure.

6.3.1 Bound states in the notch

A Hamiltonian matrix is constructed using a set of localized basis states in the gate stack. The energy levels and the associated eigenstates are then found by diagonalization of the Hamiltonian matrix. Only those energy eigenstates that are localized within the notch need to be identified. The position of states within the gate stack is shown in Fig. 6.4. Only the states with their energy levels lower than E_{lmax} and E_{rmax} are localized in the notch and are considered as bound states. The states with energy level above these parameters are not stable and can leak to the conduction band of Ge or high-κ dielectric stack to the gate. Furthermore, those states with energy levels close to these boundaries are not thermally stable and can leak by thermal activation.

The energy eigenstates are calculated by taking a general superposition state, formed from sinusoidal basis states, as discussed in the introduction, Eq. (6.16).

$$\varphi_n(x) = \sum_{k=1}^{M} A_{nk}\psi_k(x) = \sqrt{\frac{2}{t_{HK} + t_{IL}}} \sum_{k=1}^{M} A_{nk} \sin\left(\frac{\pi k x}{t_{HK} + t_{IL}}\right) \qquad (6.22)$$

where t_{HK} is the high- κ dielectric thickness, t_{IL} is the GeO_2 thickness, M is the number of basis states used in the numerical expansion, and A_{nk} is the coefficient of the n'th eigenstate associated with the k'th basis state, normalized such that for all n

$$\varphi_n(x) = \sum_{k=1}^{M} |A_{nk}|^2 = 1 \qquad (6.23)$$

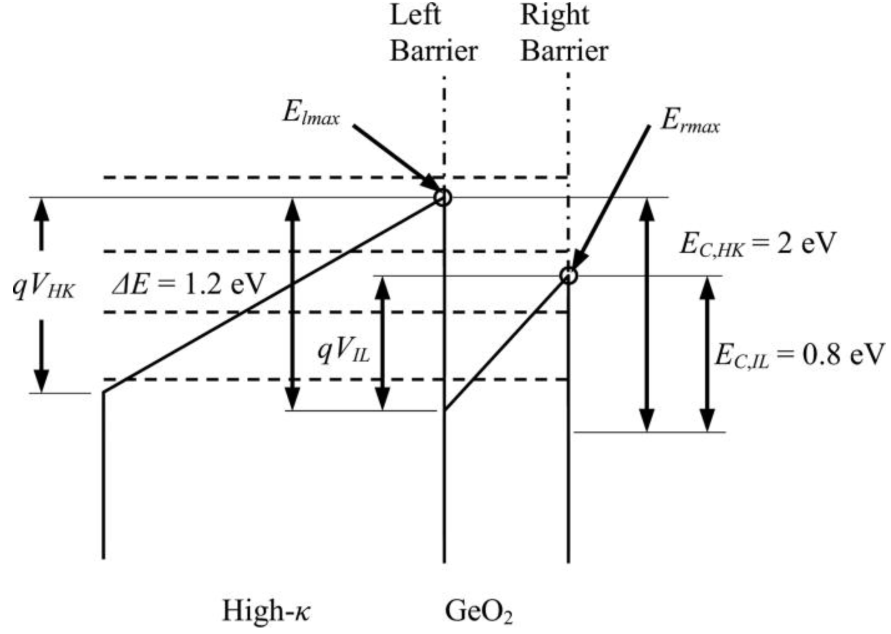


Fig. 6.4. Energy band diagram of HfO_2/GeO_2 gate stack showing typical eigenstates. The bound states are only those localized in the IL region.

The coefficients are found by forming the matrix Eqs. (6.14-6.18)

$$H_{jk} = \int_0^{t_{HK}+t_{IL}} \psi_j^*(x) H(x) \psi_k(x) dx$$
$$= \left[\frac{h^2 k^2}{8m_e(t_{HK}+t_{IL})}\right]\delta_{jk} + \frac{2}{t_{HK}+t_{IL}} \times \int_0^{t_{HK}+t_{IL}} \sin\left(\frac{\pi j x}{t_{HK}+t_{IL}}\right) V(x) \sin\left(\frac{\pi k x}{t_{HK}+t_{IL}}\right) \quad (6.24)$$

where δ_{jk} is the Kronecker delta, $V(x)$ is the potential as a function of the position in the stack, m_e is the effective electron mass, and h is Planck's constant. The matrix H_{jk} is then diagonalized numerically, with the eigenvalues of the diagonal matrix being the energy levels, $E_n(x)$, and the eigenvectors being the coefficients of the energy eigenstates, φ_n. This diagonalization is equivalent to solving the time-independent Schrödinger equation for the stack potential as shown in Fig. 6.5.

$$H(x)\varphi_n(x) = E_n^{(x)}\varphi_n(x) \quad (6.25)$$

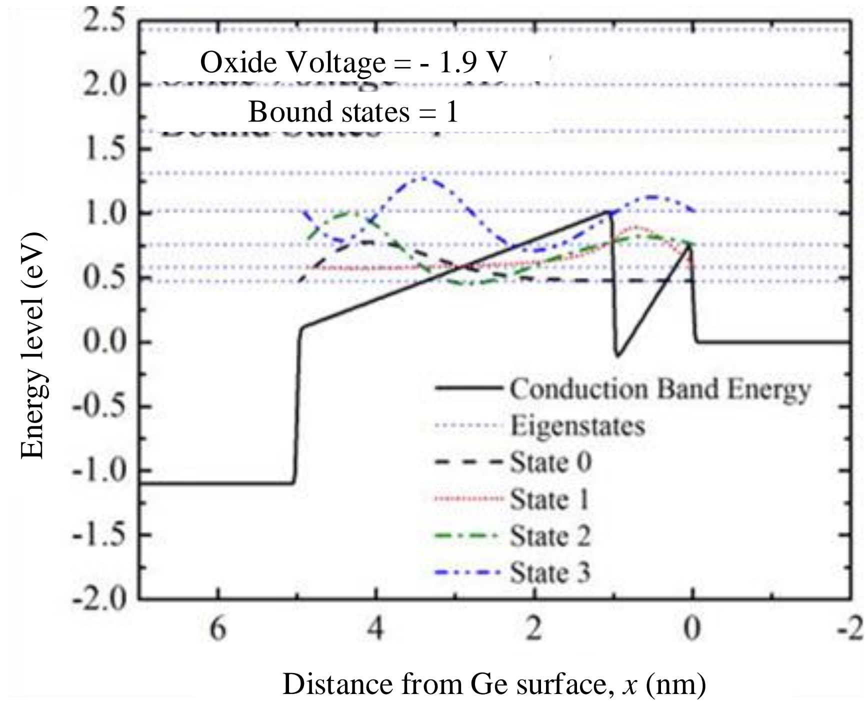


Fig. 6.5. Energy states calculated at oxide voltage of 1.9 V illustrating the bound and unstable states.

6.3.2 Three-dimensional notch

For each bound state in the one-dimensional (1-D) potential well, there is also a set of transverse excitations, corresponding to the same 1-D excitation but in two transverse directions. The lateral or transverse dimension of the device is significantly larger than the IL thickness; therefore, each 1-D state forms a "band" of closely spaced three-dimensional (3-D) energy states. The number of states should take account of the spin properties of the electrons, two states for each single particle spin state. The transverse dimensions can be modelled as a rectangular box, where excitations are independent of the longitudinal dimension. Rectangular box states have energy levels given by [2]

$$E_n = \frac{h}{2m_e}\left[\frac{n_y^2\pi}{L_y^2} + \frac{n_z^2\pi}{L_z^2}\right] \tag{6.26}$$

where h is Planck constant, m_e is effective electron mass, n_y and n_z are transverse excitations, and L_y and L_z are the transverse dimensions of the device.

6.3.3 3-D thermal occupation of notch

The notch can be treated as a small system in thermal contact with a reservoir (the substrate), for bound states. The system allows the transfer of heat/energy, and consequently, particles can fluctuate across the barrier either via thermal activation or resonant tunneling. A small system in thermal contact with a reservoir, which also allows particle fluctuation, is statically described by the "Grand Canonical Ensemble," in which the energies of the states and the chemical potential, or the Fermi level, affect the occupation of the small system. This

approximation is valid as long as the resonant tunneling or thermal activation of electrons into and from the notch occurs on timescales much shorter than those considered here. Using the Fermi-Dirac occupation probability and the density of states, the average occupation of the notch as a function of gate voltage and IL thickness can be found. Under the Grand Canonical Ensemble, the steady-state average number of electrons *N*, in the notch is given by [12]

$$N(T) = \sum_{i=1}^{N_{bt}} \frac{1}{\exp\left(\frac{E_i^{(x,z,y)} - E_f}{k_B T}\right) + 1} \tag{6.27}$$

where E_f is the Fermi level or chemical potential, T is temperature. i is a label for the bound states (i=1, 2, 3…N_{bt}), N_{bs} is the total number of bound states, and k_B is the Boltzmann constant. $E_i^{(x,z,y)}$ is the energy of the 3-D bound states [including the energies for the 1-D states, $E^{(x)}$, and the transverse excitations, $E^{(y,z)}$.]

6.4 Simulation strategy

The energy eigenstates and energy levels for the stack are calculated by solving the time-independent Schrödinger equation using numerical diagonalization of the Hamiltonian matrix, calculated using a set of approximately 100–200 sinusoidal basis states and the longitudinal stack potential given by the device parameter values given in Table 6.1. A set of typical quantum states in the notch is shown in Fig. 6.5, with the energy levels and the spatial probability distributions for the corresponding eigenstates. There is only one localized notch state, marked by "State 1". This state has an energy that is lower than the right hand side barrier and far away from the top of the left hand side barrier, and the integrated probability to the left of the left hand barrier is minimal. Therefore, it is unlikely to be thermally unstable or generate significant leakage into the high-κ dielectric region through quantum tunnelling.
The ground state for this model labelled as "State 0," is localized largely in the high-κ dielectric region and is therefore unbound, leaking to the left. The "State 3" is above the right barrier and leaks to the right. The "State 2" is very close to the top of the right barrier and is deemed to be thermally unstable.

Table 6.1: Values of parameters used in simulation.

N_{sub}	substrate doping	1.0×10^{23} m^{-3}
n_i	Intrinsic carrier concentration (Ge)	2.0×10^{19} m^{-3}
ε_s	Ge permittivity	16 ε_0
ε_{IL}	GeO_2 permittivity	6 ε_0
ε_{hk}	high-k permittivity	25 ε_0
t_{IL}	interfacial layer thickness	0.1 – 2.0 nm
t_{hk}	high-k layer thickness	2 – 4 nm
ε_0	Free space permittivity	8.85×10^{-12} Fm^{-1}
q	electronic charge	1.6×10^{-19} C

The number of bound states as a function of oxide voltage and IL thickness for two values of high-κ dielectric thickness in a 1-D device is shown in Fig. 6.6. There is no bound state if the IL thickness is larger than about 0.7 nm. There are two bound states only if the IL thickness is larger than 1.8 nm and the oxide voltage is around 1.5 V. If there are no bound states in 1-D device, then no bound states can exist in a 3-D structure. The similar graphs for a 3-D structure with lateral dimensions of 8 nm are shown in Fig. 6.7. The logarithm of the total number of electrons in the notch or the notch states occupancy as a function of oxide voltage and IL thickness is shown in Fig. 6.8 for two values of high-κ dielectric thickness. It can be seen that for IL thickness less than 1 nm the average occupancy is always less than 1×10^{-9}. Also for voltages less than 1.3 V, the average occupancy is always less than 1×10^{-9}. For a realistically scaled device, with IL thickness of 0.5 nm and high-κ dielectric oxide equivalent thickness (EOT) of 0.5 nm (total EOT of 0.83 nm), the average occupancy is zero for all values of applied voltage.

Now the technologically relevant case of an 8-nm node Ge-based MOSFET with lateral channel dimension of 8 nm, IL thickness of 0.5 nm, high-κ dielectric thickness of 3 nm with dielectric constant of 30, giving total EOT of 1 nm is considered. It is assumed that all electrons confined in the notch are forced by the electric field into a sheet charge located at the interface between IL and high-κ dielectrics. The confined charge induces an image charge Q_S at the substrate. Using Gauss's law,

$$Q_S = -\frac{1}{1+\frac{\varepsilon_{HK} t_{IL}}{\varepsilon_{IL} t_{HK}}} Q_{\text{Notch}} \tag{6.28}$$

where Q_s and Q_{Notch} are charge per unit area in the substrate and in the notch, ε_{IL} and ε_{HK} are relative permittivity, and t_{IL} and t_{HK} are thicknesses of interfacial layer and high-κ dielectric, respectively. The shift in threshold voltage by the image charge can be written as

$$\Delta V_T = -\frac{Q_S}{C_{\text{Stack}}} \tag{6.29}$$

C_{stack} is the capacitance of gate stack per unit area, the series equivalent of IL and high-κ dielectric capacitances, C_{IL} and C_{HK}.

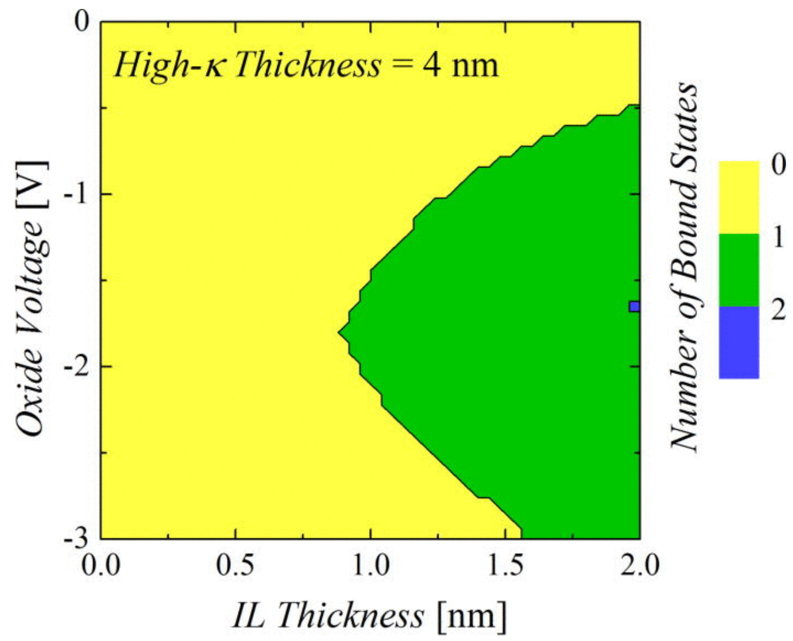
$$C_{\text{Stack}} = -\frac{1}{1/C_{IL} + 1/C_{HK}} = \frac{\varepsilon_{HK}}{t_{HK}} \frac{1}{1 + \frac{\varepsilon_{HK} t_{IL}}{\varepsilon_{IL} t_{HK}}} \tag{6.30}$$

Using the above equations, the threshold voltage shift can be found as:

$$\Delta V_T = -\frac{t_{HK}}{\varepsilon_{HK}} Q_{\text{Notch}} = -\frac{t_{HK}}{\varepsilon_{HK}} qN_{\text{Notch}} = -\frac{t_{HK}}{\varepsilon_{HK}} \frac{qN_0}{WL} \tag{6.31}$$

where N_{Notch} is the number of electrons in the notch per unit area and N_0 is the total number of electrons in the notch for a device with lateral dimension of $W = 8$ nm and $L = 8$ nm.

If only one electron is confined in the notch, using a simple electrostatic model, the threshold voltage shift induced by the electron charge is estimated as 28 mV. The average number of electrons in the notch for this device is actually less than 1×10^{-10}. The estimated threshold voltage shift induced by this charge is in the range of 1×10^{-27} V and therefore vanishingly small. It can be concluded that the notch states and their corresponding confined charge are not a problem for scaled Ge devices. However, for devices with IL thickness larger than 1.2 nm and operating voltage more than 2 V, the charge and induced threshold voltage shift can be significant.



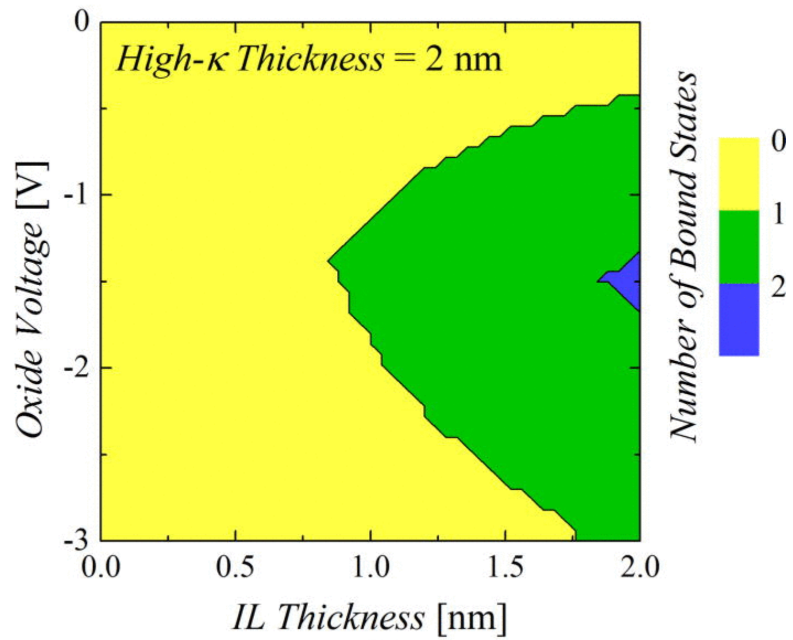
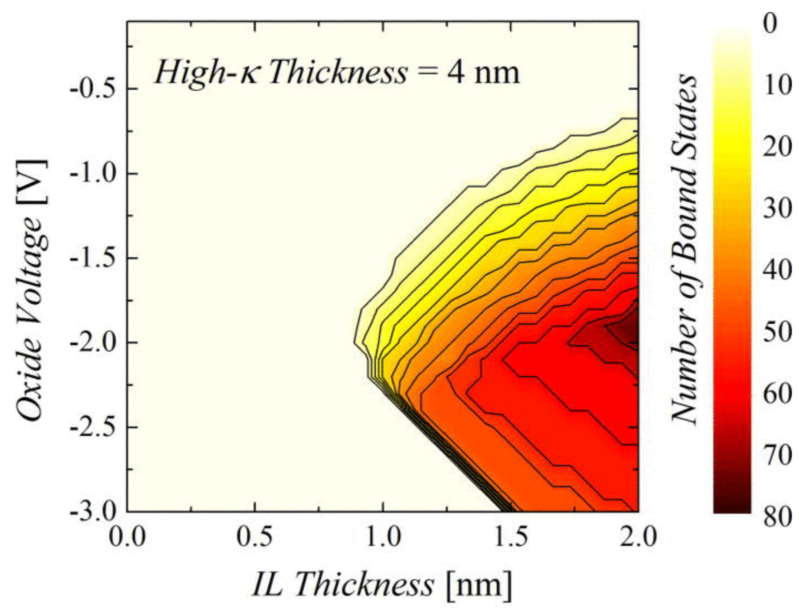
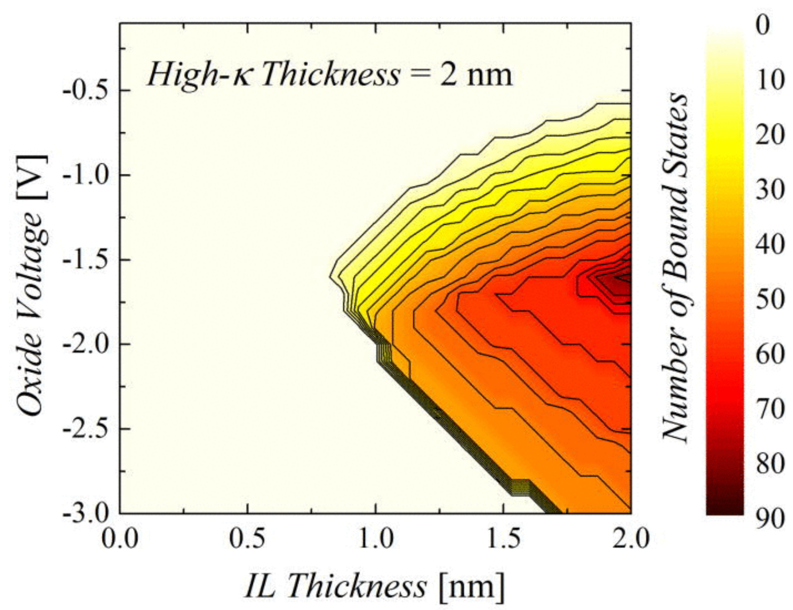


Fig. 6.6. Number of bound states in the 1-D notch as a function of IL thickness and oxide voltage for high-κ dielectric thickness of (a) 4 nm and (b) 2 nm.

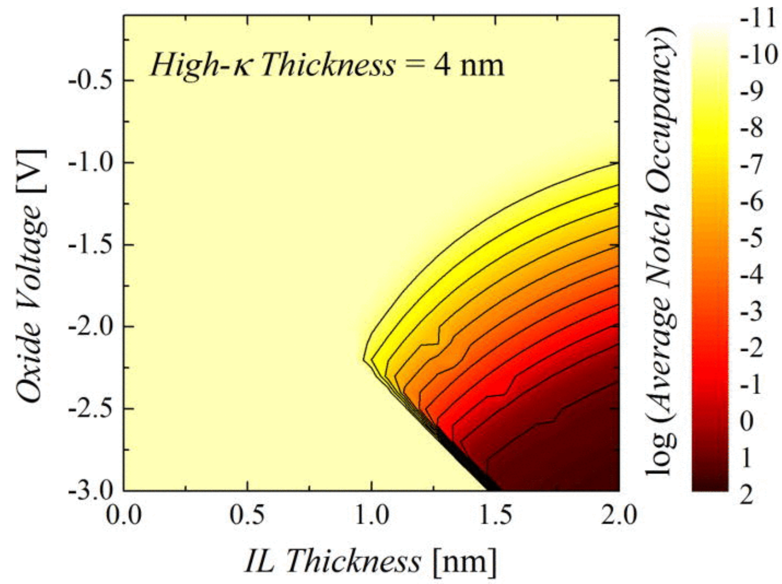


(a)

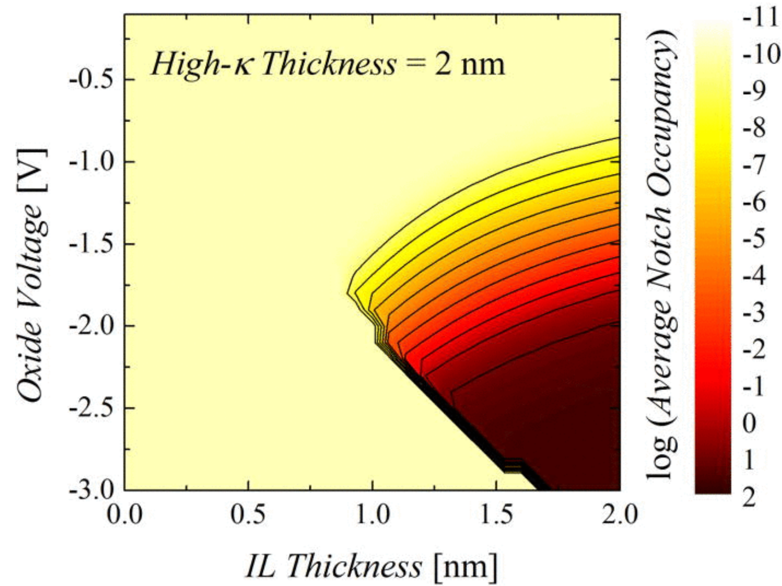


(b)

Fig. 6.7. Number of bound states in the 3-D structure as a function of IL thickness and oxide voltage for high-κ dielectric thickness of (a) 4 nm and (b) 2 nm.



(a)



(b)

Fig. 6.8. Average occupancy in the 3-D structure as a function of IL thickness and oxide voltage for high-κ dielectric thickness of (a) 4 nm and (b) 2 nm.

6.5 Conclusions

The presence of a potential well or notch at the interface of native GeO_2 and high-κ dielectric and its role as a possible charge trapping site was addressed in this chapter. The number of quantum bound states was calculated by solving the Schrödinger equation. The model then was extended to a three-dimensional structure and the average electron occupancy of notch for various device parameters was calculated. The simulation results reveal that there are no stable states in the notch for IL thickness less than 1 nm. The threshold voltage shift induced by the electrons confined in the notch was calculated from simple electrostatics with the

conclusion that the threshold voltage shift for an 8-nm node Ge MOSFET is vanishingly small. However, the shift would be significant for larger devices and when the IL thickness is more than 1.2 nm. In terms of the samples fabricated in this thesis, the IL thickness is between 1 and 2 nm, thus charge storage in the notch may lead to a threshold voltage shift of the order 6-11 mV.

6.6 References

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Chapter 7 Low-frequency behaviour of Ge-based MOS C-V plots

7.1 Introduction

Capacitance-voltage *C-V* measurements have been widely employed to characterize Ge gate stacks. As shown in Fig. 7.1, a low frequency response of the *C-V* characteristic is apparent even at high frequency for sample Ge39S1. The capacitance in the strong inversion regime approaches the oxide capacitance, C_{ox}. In Si-based MOS, this phenomenon only happens at very low frequency [1-3]. This phenomenon is also seen in the *C-V* characteristics for all samples considered in chapter 2. This behaviour in Ge-based MOS indicates minority carriers can be easily generated in the inversion regime. Two mechanisms have been suggested to describe this high rate of minority carrier generation in Ge-based MOS [1, 3, 4]: (a) the minority carriers are generated in the bulk through thermal generation and then diffuse into interface by the diffusion process; (b) the minority carriers are directly produced in the depletion region through thermal generation via mid-gap traps and then drift to the interface between oxide and semiconductor as shown in Fig. 7.2. Additionally, minority carriers may be supplied from an external source beyond the gate, e.g., peripheral charge induced by device processing steps. However, the minority carrier response observed does not vary with area, therefore excluding any contribution of peripheral or external charge effects [5]. The mechanism responsible for the low-frequency response behaviour in the samples is now investigated. Then the measurement of generation lifetime of minority carriers is carried out to further study this phenomenon.

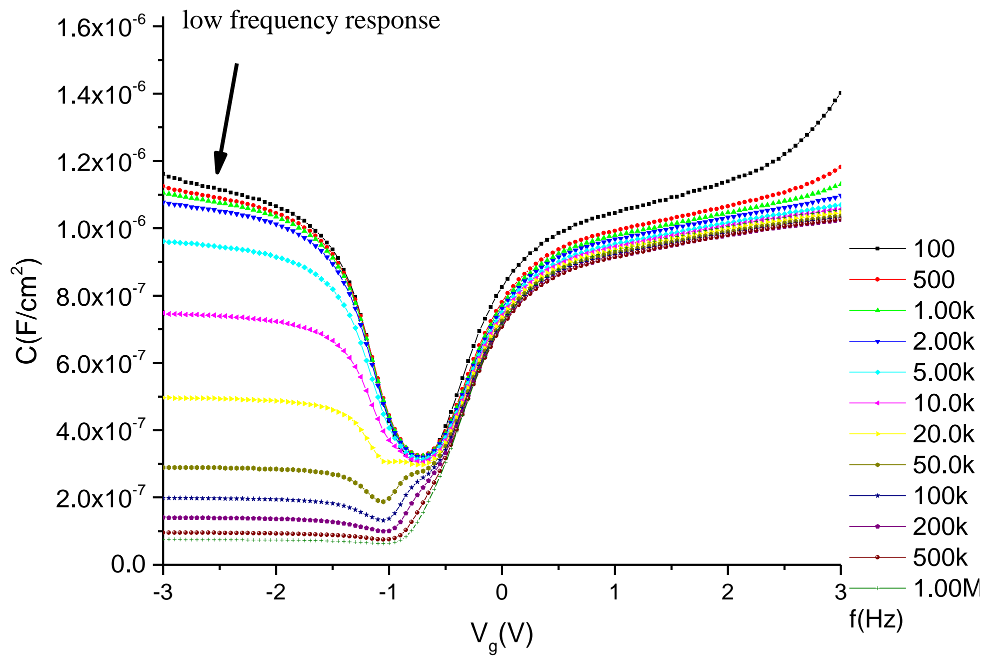

Fig. 7.1. The *C-V* characteristics for sample Ge39S1 shows low frequency response in the inversion region.

In Fig. 7.1, the minimum of capacitance in inversion could be obtained through:

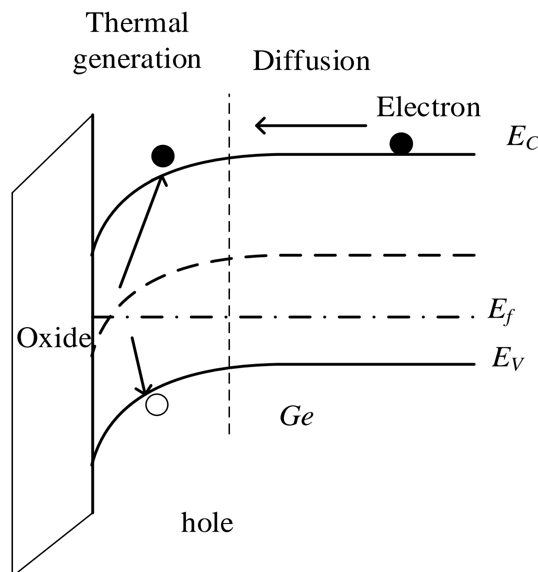

Fig. 7.2. A schematic showing the depletion and neutral regions of a p-type Ge-based MOS and the two mechanisms for generation of minority carriers.

To study which mechanism is responsible for the low frequency behaviour of *C-V* characteristics in the inversion regime for Ge-based MOS, firstly, mathematical expressions

for the two mechanisms are derived. Calculations are performed to illustrate that the temperature dependence of the two mechanism is mainly dependent on the intrinsic concentration n_i. Then temperature dependent measurements are employed to obtain Arrhenius plots with the purpose to identify which mechanism is actually responsible for the low frequency behaviour. The generation lifetime of minority carriers in Ge is an important parameter for mechanism (a), thus, it is estimated using the pulsed MOS capacitance technique. Based on this measurement, the generation lifetime of minority carriers in Ge is used to fit calculations based on mechanism (a) with experimental data.

7.2 Theory for the two mechanisms

Mathematical expressions for the two mechanisms are derived in this section.

7.2.1 Thermal generation of minority carriers through mid-gap defects in the depletion region

Using the continuity equations, for an applied small ac signal on MOS, the variation of the current density J_n is given by the number of electrons generated minus the number of electrons recombining with holes; this variation U_n is provided by generation and recombination of electrons in the depletion region [6], thus:

$$\frac{1}{q}\frac{\partial J_n}{\partial x} = U_n \qquad (7.1)$$

Then:

$$\partial J_n = qU_n \partial x \qquad (7.2)$$

A detailed band diagram at the surface of a p-type Ge is shown in Fig. 7.3. The potential $\phi(x) = \phi(x=0) - \phi(x=\infty)$ is defined as the amount of band bending at position x, where x=0 is at the Ge surface and ($x=\infty$) is the intrinsic potential in the bulk of Ge. The boundary conditions are $\phi(x=\infty)$ =0 in the bulk of Ge and $\phi(0)= \phi_S$ at the surface.

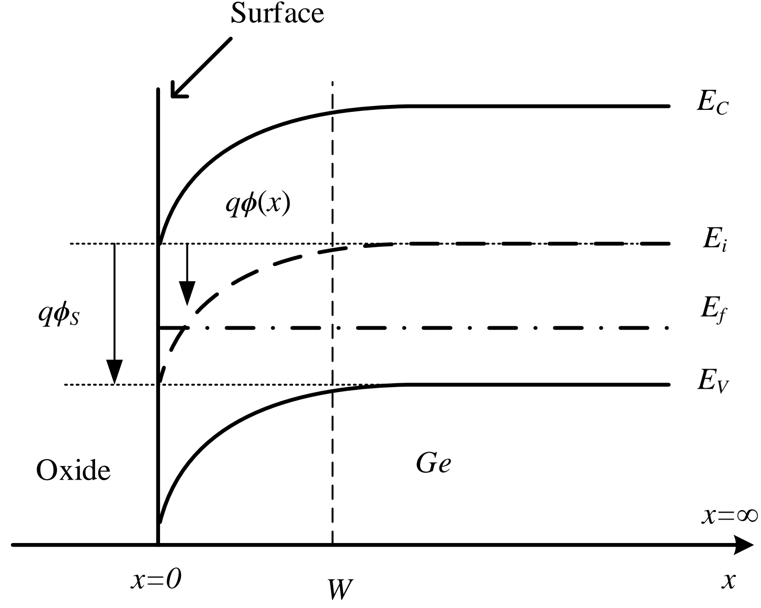

Fig. 7.3. The band diagram of n-type MOS in the inversion regime.

For a MOS structure in inversion, the potential is given by [6]:

$$\phi(x) = \phi_S \left(1 - \frac{x}{W}\right)^2 \tag{7.3}$$

where

$$\phi_S = \frac{qN_{sub}W^2}{2\varepsilon_{GE}} \tag{7.4}$$

where N_{sub} is the acceptor concentration, ε_{GE} is the permittivity of Ge.
Differentiate Eq. (7.3) and then:

$$\frac{\partial\phi(x)}{\partial x} = 2\phi_S \left(1 - \frac{x}{W}\right)\frac{1}{W} \tag{7.5}$$

Then:

$$\partial\phi(x) = 2\phi_S \left(1 - \frac{x}{W}\right)\frac{1}{W}\partial x \tag{7.6}$$

The ac current at x = 0 entering the surface by drift, when x= 0 following equation can be obtained:

$$\partial\phi(0) = \partial\phi_S = \frac{qN_{sub}W}{\varepsilon_{Ge}}\partial x \tag{7.7}$$

N_{sub} is the doping concentration, W is depletion width and ε_{Ge} is the permittivity of Ge.
The conductance per unit area can be obtained:

$$G_g = \frac{\partial J}{\partial\phi_S} \tag{7.8}$$

Recall the SRH generation and recombination rate [7]:

$$U_n = \frac{pn - n_i^2}{\tau_p(n+n_i) + \tau_n(p+n_i)} \tag{7.9}$$

τ_p, τ_n are lifetimes for electrons and holes in the steady-state regime, respectively; n is electron concentration, p is the hole concentration, n_i is intrinsic concentration of Ge

where

$$\tau_\mathrm{n} = \frac{1}{\mathrm{N}_t v_{th} \sigma_n} \tag{7.10}$$

$$\tau_p = \frac{1}{\mathrm{N}_t v_{th} \sigma_p} \tag{7.11}$$

And the average thermal velocity of carrier is given by $v_{th} = \sqrt{3kT/m^*}$, N_t is the density of traps, and σ_n and σ_p are electrons and holes capture cross sections respectively, m^* is an average effective mass of carriers, k is Boltzmann's constant and T is absolute temperature.

In the depletion area, $p << n_i$ and $n << n_i$ and assume $\tau_g = \tau_p = \tau_n$

So that Eq. (7.9) can be written as:

$$U = \frac{-n_i}{\tau_p + \tau_n} = \frac{-n_i}{2\tau_g} \tag{7.12}$$

Combine these Eqs. (7.2), (7.7), (7.8) and (7.11), then

$$G_g = \frac{qn_i K}{2\tau_g \sqrt{\phi_S}} \tag{7.13}$$

where $K = \sqrt{2\varepsilon_{Ge}/qN_{sub}}$

7.3 The diffusion of minority carriers from the semiconductor bulk

In this section, the conductance per unit area for diffusion minority carrier response is derived. The conductance per unit area for the diffusion of electrons from the germanium substrate is given by Eq. (7.8).

Using the continuity equation for minority carriers (electrons) [2]:

$$\frac{\partial n}{\partial t} = D_n \frac{\partial^2 n}{\partial x^2} - \frac{(n - n_B)}{\tau_n} \tag{7.14}$$

n_B is the equilibrium electron concentration, D_n is the electron diffusion coefficient, t is time and n is electron concentration. The first term on the right is the diffusion of electrons across the quasi-neutral region and the second term indicates generation and recombination of electrons in the quasi-neutral region.

Assume the time dependence of n is given by:

$$n(x,t) = n_B + \delta n(x)\exp(j\omega t) \tag{7.15}$$

ω is the angular frequency.

Substitute this equation into Eq. (7.14), then

$$j\omega\delta n = -\frac{\delta n}{\tau_n} + D_n \frac{\partial^2 \delta n}{\partial x^2} \tag{7.16}$$

Based on the boundary condition $\delta n = \delta n_w$ at $x=W$, and $\delta n = 0$ when x is infinite large, W is the depletion width, then solution can be obtained:

$$\delta n = \delta n_w \exp\left[(x - W)\left(\frac{1 + j\omega\tau_n}{D_n \tau_n}\right)^{1/2}\right] \tag{7.17}$$

Consider the case where $\omega\tau_n << 1$, with this approximation then:

$$\delta n = \delta n_w \exp\left[-\frac{W - x}{(D_n \tau_n)^{1/2}}\right] \tag{7.18}$$

With Eq. (7.18), the ac current at $x = W$, entering the depletion layer by diffusion is given by:

$$J_n = qD_n \left.\frac{\partial \delta n}{\partial x}\right|_{x=w} = \left(\frac{qD_n}{L_p}\right)\delta n_w \tag{7.19}$$

where L_n is the diffusion length of electrons

$$L_n = (D_n \tau_n)^{1/2} \tag{7.20}$$

The Einstein relation gives:

$$D_n = \mu_n \frac{kT}{q} \tag{7.21}$$

Substitute this equation into (7.19), thus:

$$J_n = \left(\frac{kT}{q}\right)\frac{q\mu_n \delta n_w}{L_n} \tag{7.22}$$

For this quasi-equilibrium, small-signal case,

$$\delta n_w = n_B \beta \delta\phi(x) \tag{7.23}$$

where $\beta = (kT / q)^{-1}$

The variation in n is determined by the quasi-fermi level variation. Then:

$$n_B = n_i^2 / N_{sub} \tag{7.24}$$

Recall Eq. (7.15) with Eqs. (7.22, 7.23, 7.24), finally the diffusion conductance is:

$$G_d = \frac{q\mu_n n_i^2}{L_n N_{sub}} \tag{7.25}$$

These previous two sections have provided the equations for the two mechanisms as discussed above.

7.4 Temperature dependence of the two mechanisms

For mechanism (a), the thermal generation conductance G_g which is given by Eq (7.13) has an exponential dependence on temperature mainly because of its dependence on n_i. The lifetime τ_g is weakly dependent on temperature. For mechanism (b), the diffusion conductance G_d (Eq (7.13)) also has an exponential dependence on temperature due to n_i. The other parameters L_n, τ_n, and D_n are weakly dependent on temperature.

Recall the equation for the two mechanism Eqs. (7.13) and (7.25), where the intrinsic concentration n_i is given by [6]:

$$n_i = \sqrt{N_v N_c}\exp\left(-\frac{E_g}{2kT}\right) \tag{7.26}$$

and N_v and N_c are:

$$N_v = 2\left(\frac{2\pi m_h^* kT}{h^2}\right)^{3/2} \tag{7.27}$$

$$N_c = 2\left(\frac{2\pi m_e^* kT}{h^2}\right)^{3/2} \tag{7.28}$$

Thus:

$$n_i^2 = N_v N_c \exp\left(-\frac{E_g}{kT}\right) \tag{7.29}$$

The temperature dependence of mobility limited by acoustic phonon interaction can be represented as $\mu_n \infty T^{-3/2}$ [8].

When T=300 K, the bulk mobility of electrons in germanium is approximately 3900 (cm^2 V^{-1} s^{-1}) [8],

$$\mu_n(T) = C_1 T^{-3/2} \tag{7.30}$$

where C_1 is a constant. For T = 300K, taking the electron as 3900 (cm^2 V^{-1} s^{-1}), gives C_1 = 5196.2.

The lifetime dependence on temperature based on equation (7.10) is: $\tau_g \infty T^{1/2}$ [9]

$$\tau_g(T) = C_2 T^{1/2} \tag{7.31}$$

where C_2 is constant. For T = 300 K, the lifetime is assumed to be 10 ns, thus C_2 is 5.7 $\times 10^{-8}$.

The temperature dependence of L_n and D_n can be obtained from Eqs (7.20) and (7.21). Fig. 7.4 shows a theoretical Arrhenius plot for G_d and G_g.

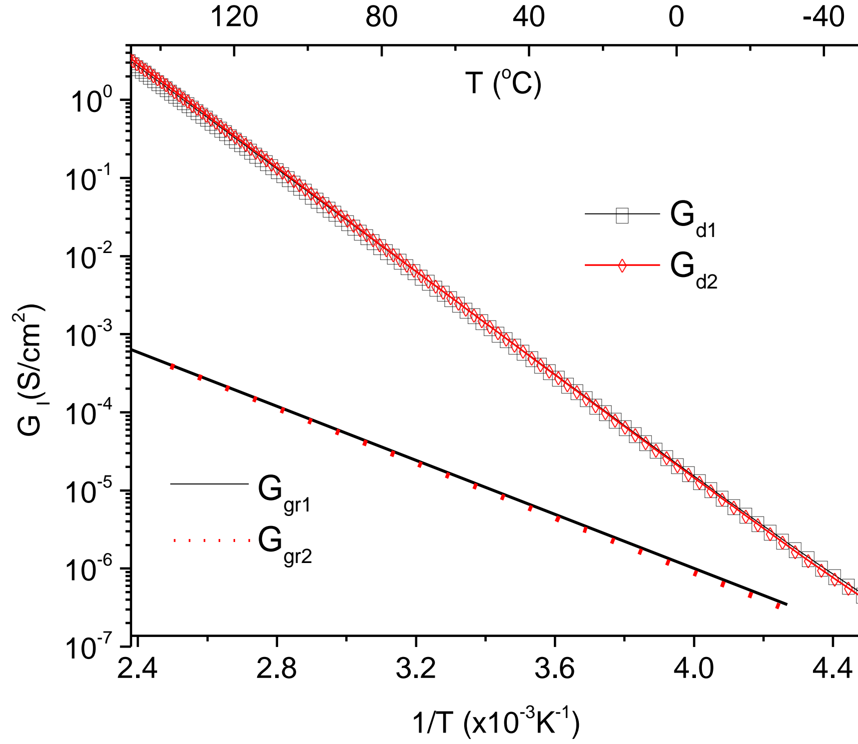

Fig. 7.4. The diffusion conductance G_{d1} takes all parameter temperature dependencies into account and G_{d2} denotes the conductance using only the temperature dependence exponential term of n_i. The thermal generation conductance G_{gr1} takes all temperature dependencies into account and G_{gr2} denotes the conductance using only the temperature dependence exponential term of n_i.

From Fig. 7.4, it can be summarized that both the diffusion conductance G_d and generation-recombination conductance G_{gr} can be treated as only dependent on temperature through n_i, because other temperature-dependent parameters are very weak compared to it.

An Arrhenius plot displays the logarithm of kinetic constants (log(K_{arr}), ordinate axis) plotted against inverse temperature ($1/T$), the Arrhenius equation is given by [10]:

$$K_{arr} = A\exp\left(-\frac{E_A}{k_B T}\right) \tag{7.32}$$

Take the natural logarithm of equation (7.32), then:

$$\log(K_{arr}) = \ln(A) - \frac{E_A}{k_B T} \tag{7.33}$$

Where E_A is activation energy, A is pre-exponential factor, and T is absolute temperature.

When plotted in the manner described above, the slope of the line will be equal to $-E_A / k_B$. Referring to Eqs (7.13) and (7.25), taking the natural logarithm, the only temperature dependence is from the exponential part of n_i then:

For the diffusion conductance G_d:

$$\ln(G_d) = \ln\left(\frac{q\mu_n n_i^2}{L_n N_{sub}}\right) = A - \frac{E_g}{k_B T} \tag{7.34}$$

where A is a constant.

For the thermal generation process conductance G_{gr}:

$$\ln(G_g) = \ln\left(\frac{q n_i K}{2\tau_g \sqrt{\phi_S}}\right) = B - \frac{E_g/2}{k_B T} \tag{7.35}$$

where B is a constant

These two equations have the same format with the Arrhenius equation, thus the activation energy E_A for diffusion conductance G_d is the full band gap E_g, and for the thermal generation process, half the band gap, E_g / 2. The activation energy E_A can be extracted from the slope of the logarithm of kinetic constants (K_{arr}, ordinate axis) plotted against inverse temperature (1 / T). By obtaining the slope from the plot, active energy E_A can be derived which can be used to identify which mechanism is responsible for the generation of minority carriers in inversion.

7.5 Experimental measurement and discussion

The equivalent circuit when the MOS capacitor is in inversion is given [2] by Fig. 7.5.

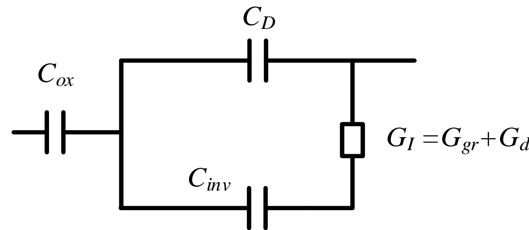

Fig. 7.5. The equivalent circuit in strong inversion.

In strong inversion, the inversion capacitance C_{inv} is much larger than C_D, thus this equivalent circuit can be converted into [2]:

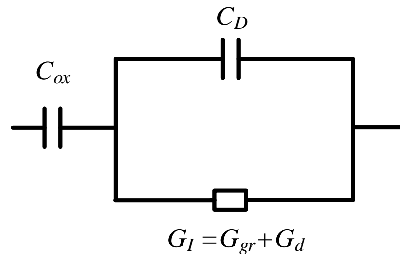

Fig. 7.6. Simplified circuit of Fig. 7.5.

The inversion conductance G_I, can be obtained from the measured conductance (G_m) and capacitance (C_m) by Eq. (7.36) when the MOSC is measured in the parallel mode.

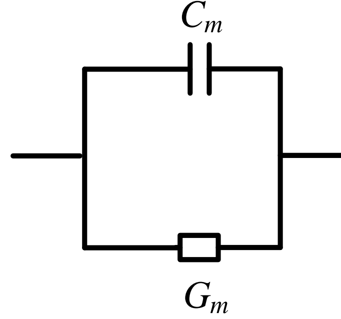

Fig. 7.7. Measured circuit in parallel mode

The extracted G_I based on equivalent circuit (Fig. 7.6) and equivalent circuit employed in the measurement (Fig. 7.7) is obtained by [2]:

$$G_I = \frac{\omega C_{ox} \tau_o (1 + \omega^2 \tau_m^2)}{\omega^2 \tau_o^2 + [\omega^2 \tau_m (\tau_o - \tau_m) - 1]^2} \qquad (7.36)$$

where $\tau_m = C_m / G_m$ and $\tau_o = C_{ox} / G_m$

The Arrhenius plots for the three samples examined in this work are shown in Fig. 7.8, Fig. 7.9 and Fig. 7.10.

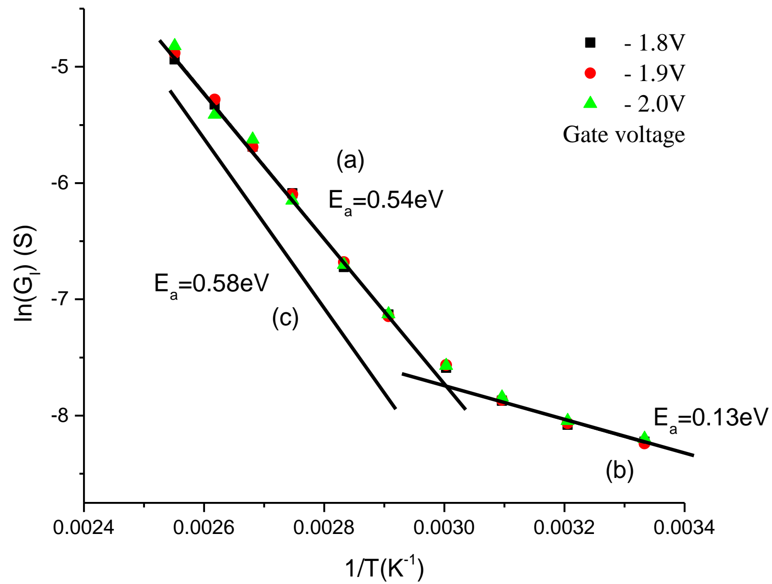

Fig. 7.8. Arrhenius plots of the inversion parallel conductance log (G_I) plotted versus 1 / T for sample Ge12S1 measured at different gate voltages. Curve c is obtained based on the subtraction (b) from (a).

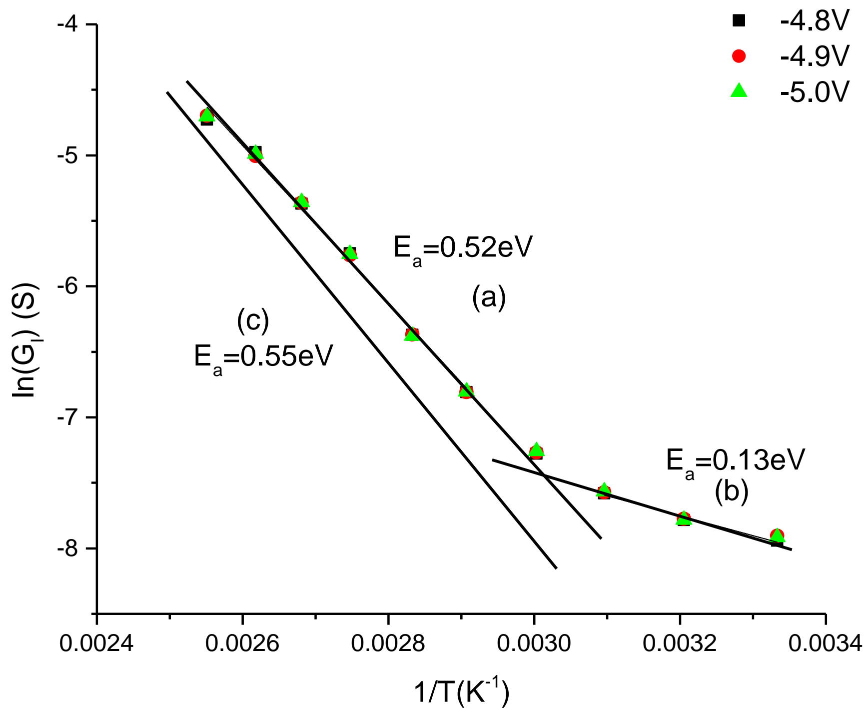

Fig. 7.9. Arrhenius plots of the inversion parallel conductance log (G_I) plotted versus 1 / T for sample Ge12S2 measured at different gate voltages. Curve c is obtained based on the subtraction (b) from (a).

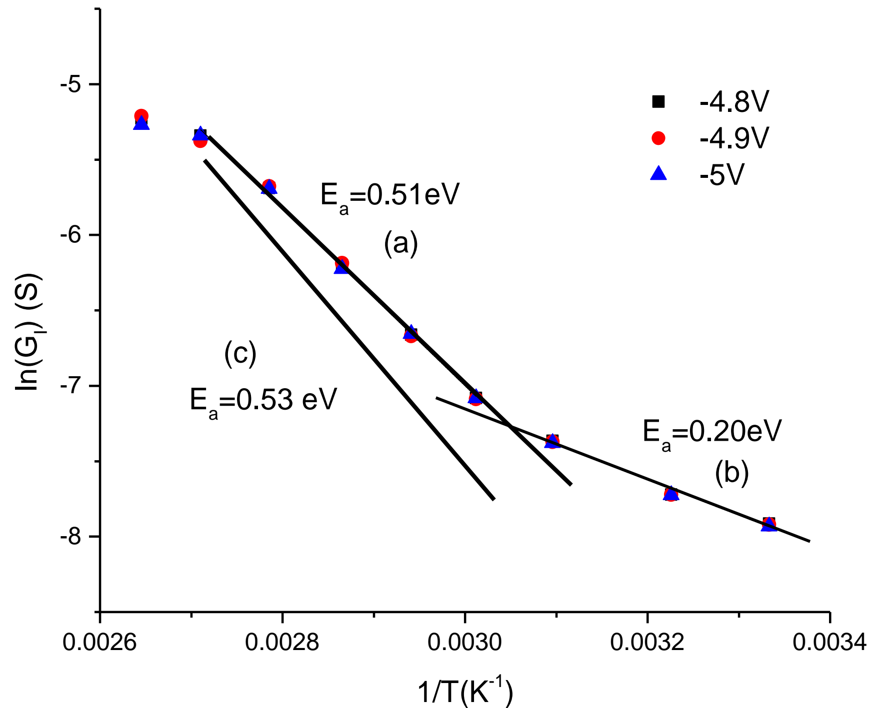

Fig. 7.10. Arrhenius plots of the inversion parallel conductance log (G_I) plotted versus 1 / T for sample Ge12S3 measured at different gate voltages. Curve c is obtained based on the subtraction (b) from (a).

From the above three figures, it can observed that the extracted activation energy E_a is about 0.2 eV for curve (a) and 0.13 eV for curve (b) for different samples and is considered reasonably close to half the band gap of Ge over the low temperature range (20 to 45 °C). The activation energy is around 0.51 eV which is close to the full band gap of Ge over the higher temperature range. Although in the low temperature range, the extracted active energy is smaller than half the band gap (0.33 eV), it is likely that the minority carrier generation mechanism is due to thermal generation. The small extracted activation energy in low temperature range is indecipherable. Similarly, over the high temperature range, the mechanism of minority carrier generation is likely to be the diffusion process as the extracted activation energy is about, 0.5 eV which is close to the full band gap of Ge. To obtain more accurate activation energy for the diffusion, following procedure could been utilized. This subtracts the contribution of depletion layer generation and recombination at higher temperature and is performed by subtracting the extrapolated values of curve (b) in low temperature from curve (a) in high temperature, yielding curve (c) without the effect of thermal generation. As shown in above figures, curve (c) give closer activation to full energy band gap.

Thereby, it can be concluded that at room temperature, thermal generation in the depletion region is responsible for the low frequency response observed in *C-V* characteristics. As minority carrier generation lifetime is an important parameter for the thermal generation process, it will be measured experimentally in the next section.

7.6 Measurement of the generation lifetime

Minority carrier lifetime is an important semiconductor material property. The lifetime of the average time that excess free electrons (or holes) will "survive" before recombining, or the average time that electrons will be "missing" before being "re-generated". The first case is called the minority carrier recombination lifetime, the latter is called the minority carrier generation lifetime. In this section, the minority generation lifetime is measured using the deep deletion method on a Ge MOS capacitor. When an MOS capacitor is pulsed into the deep depletion state, it returns to the quasi-equilibrium inversion condition as a result of thermal carrier generation in the bulk and or diffusion from the surface of the device. When an MOS capacitor is pulsed from accumulation into deep depletion, five generation components contribute to its return to equilibrium. They are [11-13]:

1) bulk generation in the space charge region (scr) characterized by the generation lifetime, τ_g;

2) lateral scr generation characterized by the surface generation velocity, S_0;

3) scr generation under the gate characterized by the surface generation velocity, S;

4) quasi-neutral bulk generation characterized by the minority carrier diffusion length, L_n;

5) back surface generation characterized by the generation velocity, S_c.

The components 4 and 5 can be ignored by assuming minority carrier diffusion length is smaller than the thickness of the wafer [12].

The rate of change of the surface layer carrier density, n_s is related to the carrier generation in the scr by

$$\frac{dn_s}{dt} = \frac{n_i}{\tau_g} W_g + n_i S_0 \frac{A}{A_g} + n_i S \qquad (7.37)$$

Where n_i is the intrinsic carrier concentration, $A_g=\pi r^2$ is the gate area, r is the radius and d is the diameter of the gate electrode, $A=2\pi r W_g$ is the area of the lateral portion of the scr, $W_g=W-W_f$ is the generation region width, W and W_f are the width of the scr and its final value, respectively. The major approximation for Eq.(7.37) is that the lateral dimension of scr is the same as its longitudinal width W.

Eq.(7.37) can be further expressed as:

$$\frac{dn_s}{dt} = \frac{n_i}{\tau'_g} W_g + n_i S \tag{7.38}$$

τ_g is called the effective lifetime.

$$\tau'_g = \tau_g \left(1 + \frac{4S_0 \tau_g}{d}\right)^{-1} \tag{7.39}$$

where d is the diameter of the gate of the MOS capacitor.

Recalling the MOS structure, oxide field is proportional to the net charge per unit area in the semiconductor [6]; that is

$$C_{ox}[V_G - \psi_s] = q\left[n_s(t) + \int_0^{W(t)} dx N_{sub}\right] \tag{7.40}$$

where ψ_s is the instantaneous band bending, and N_{sub} is the dopant density. x is the distance from interface between oxide and semiconductor. C_{ox} is the capacitance per unit area of oxide and V_G is the gate voltage. $W(t)$ is the instantaneous value of depletion layer width. When the gate bias voltage is unchanged, differentiate with respect to time and then:

$$\frac{dn_s}{dt} = -\frac{C_{ox}}{q}\left(\frac{d\psi_s}{dt}\right) - n_s W(t) \frac{dW}{dt} \tag{7.41}$$

Ignoring the potential across inversion layer then the band bending can be obtained:

$$\psi_s(t) = \frac{q}{\varepsilon_0 \varepsilon_s} \int_0^{W(t)} x N_{sub} dx \tag{7.42}$$

Neglecting the voltage drop across in the inversion layer and substituting Eq (7.42) into (7.41), then

$$\frac{dn_s}{dt} = -N_{sub}\left(1 + \frac{C_{ox}}{\varepsilon_0 \varepsilon_s} W\right)\frac{dW}{dt} \tag{7.43}$$

Recall the familiar relationship between depletion width and capacitance of MOS:

$$W = \varepsilon_0 \varepsilon_s \left(\frac{1}{C} - \frac{1}{C_{ox}}\right) \tag{7.44}$$

Substitute Eq (7.44) into (7.43), then:

$$\frac{dn_s}{dt} = -\frac{C_{ox}}{C} N_{sub} \varepsilon_0 \varepsilon_s \frac{d}{dt}\left(\frac{1}{C} - \frac{1}{C_{ox}}\right) = -\frac{N_{sub} \varepsilon_0 \varepsilon_s}{2C_{ox}} \frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 \tag{7.45}$$

Combine Eqs (7.38) and (7.45), then:

$$-\frac{d}{dt}\left(\frac{C_{ox}}{C}\right)^2 = \frac{2n_i}{N_{sub}} \times \left[\frac{C_{ox}}{\tau'_g C_f}\left(\frac{C_f}{C} - 1\right) + \frac{C_{ox} S}{\varepsilon_0 \varepsilon_s}\right] \tag{7.46}$$

Eq (7.46) is used for the so-called Zerbst plot [13].

7.6.1 Modified method for measuring the generation lifetime of minority carriers

Recall the Eq (7.37), assume the generation rate outside the depletion region is negligible, so the second and third terms can be eliminated, which means the depletion region charge is reduced by carrier generated in the depletion region in terms of physical mechanism.

Then Eq (7.37) can be simplified as:

$$\frac{dn_s}{dt} = \frac{n_i}{2\tau} W_g \tag{7.47}$$

Where τ_g=2τ, τ is the lifetime of hole and electron (assume their lifetime are same)

The final scr width W_f can be expressed based on Eq. (7.47):

$$W_f = \varepsilon_0 \varepsilon_s \left(\frac{1}{C_f} - \frac{1}{C_{ox}} \right) \tag{7.48}$$

Substitute Eqs. (7.44) and (7.48) into Eq (7.47), then:

$$\frac{dn_s}{dt} = \frac{qn_i}{2\tau_g}\left(W - W_f\right) = \frac{\varepsilon_0 \varepsilon_s q n_i}{2\tau_g}\left(\frac{1}{C} - \frac{1}{C_f} \right) \tag{7.49}$$

Combine the Eqs (7.47) and (7.49), then

$$-\frac{N_{sub}(W)\varepsilon_0 \varepsilon_s}{2C_{ox}} \frac{d}{dt}\left(\frac{C_{ox}}{C} \right)^2 = \frac{\varepsilon_0 \varepsilon_s q n_i}{2\tau_g}\left(\frac{1}{C} - \frac{1}{C_f} \right) \tag{7.50}$$

Eq (7.50) is a differential equation for the time dependence of C, separation of variables for with C=C_0 at t=0 yields the solution

$$\left(1 + \frac{C_{ox}}{C_f} \right) \times \ell n \left[\frac{\frac{C_f}{C} - 1}{\frac{C_f}{C_o} - 1} \right] + C_{ox}\left(\frac{1}{C} - \frac{1}{C_f} \right) = -\frac{t}{T} \tag{7.51}$$

where T=2τ(N_B/n_i)

This model is based on the assumption of ignoring the scr generation under the gate characterized by the surface generation velocity S, as well the lateral scr generation characterized by the surface generation velocity S_0. The lateral scr generation characterized by the surface generation velocity S_0 can be neglected for well-passivated interfaces [12]. For scr generation under the gate characterized by the surface generation velocity S, This component can also be neglected if the MOS capacitor is initially biased into strong inversion and then pulsed into deep depletion rather than pulsing from accumulation into deep depletion [15]. The reason is if MOS capacitor is initially biased into accumulation, then go to deep depletion and surface generation proceeds at a maximum rate during the early portion of capacitance transient response. Alternatively, initially biased into inversion, results in

shielding from the bulk and the scr generation under the gate characterized by the surface generation velocity S can be small.

7.6.2 Experimental measurement and discussion

7.6.2.1 First group of measurements

The first group of measurement is applied to n-type MOS capacitors of 0.5mm diameter dot size on sample Ge12S3 (n-type). The sample was initially biased into inversion with different positive biased voltages of – 2 V and then pulsed into deep depletion with – 3 V, – 4 V and – 5 V pulses. The transient MOS capacitance versus time is recorded using 0.002 s sampling rate as the capacitor returns from non-equilibrium deep depletion into equilibrium inversion.

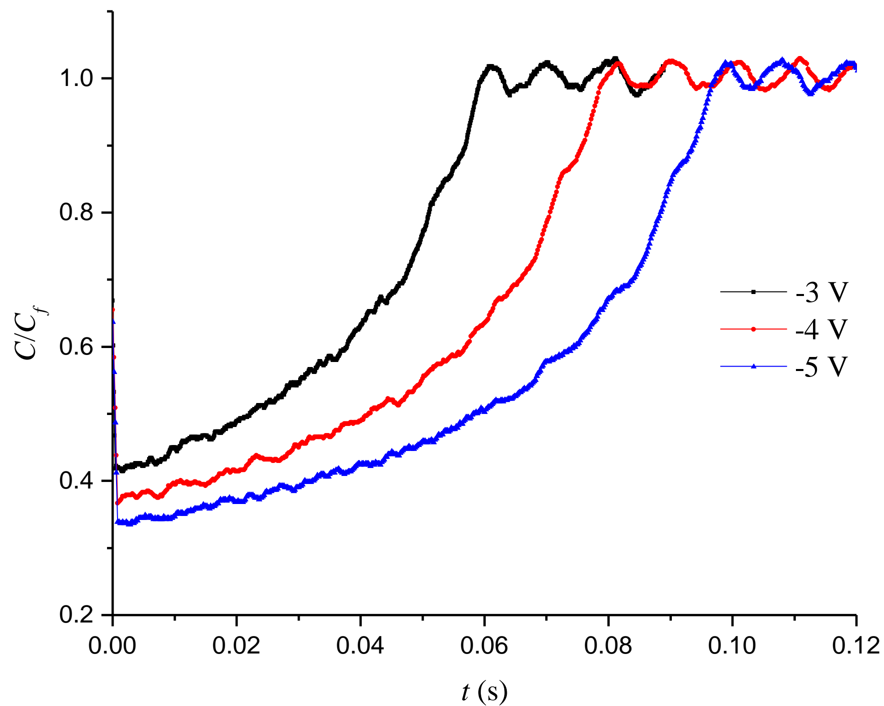

Fig. 7.11. For 0.5 mm diameter gate MOS capacitor sample Ge12S3, *C-t* transient response from deep depletion into inversion when a pulse with different voltage amplitude is applied to the gate. The capacitor was initially biased into inversion and then pulsed using – 3 V, – 4 V and – 5 V voltage steps, into deep depletion respectively.

The differences for time for the MOS capacitor return from deep depletion into inversion is due to the different gate step voltage applied. Consequently, it takes more time to return into inversion from deep depletion. Eq. (7.51) is now used to fit the experiment data.

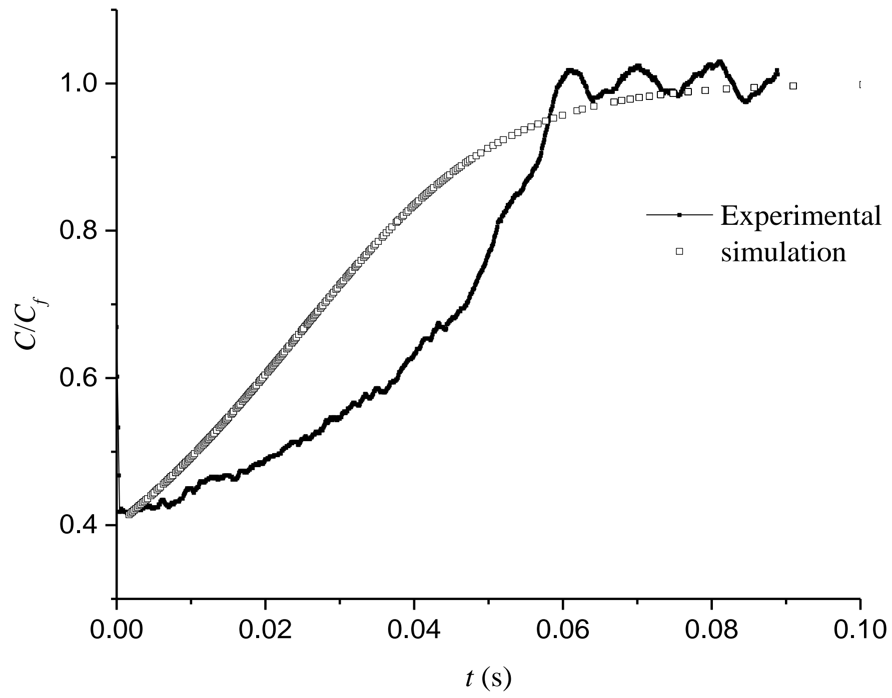

Fig. 7.12. Lifetime τ = 21 ns for – 3 V pulsed into deep depletion for sample Ge12S3 with 0.5 mm dot.

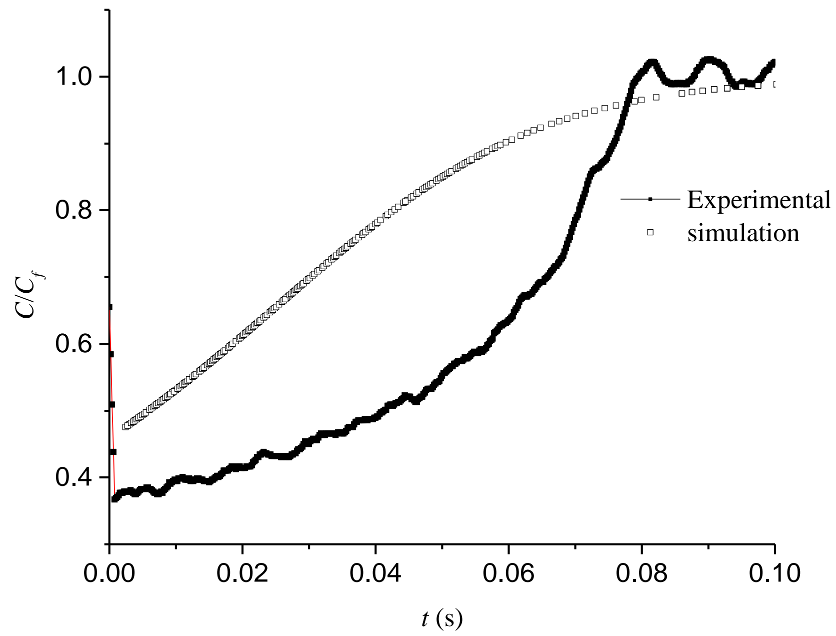

Fig. 7.13. Lifetime $\tau = 30$ ns for – 4 V pulsed into deep depletion for sample Ge12S3 with 0.5 mm dot.

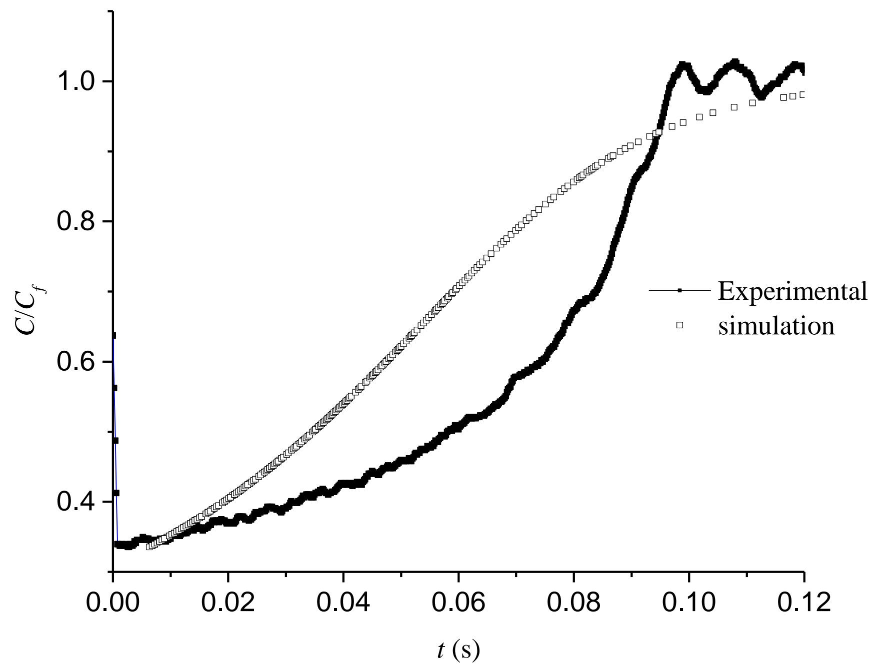

Fig. 7.14. Lifetime $\tau = 30$ ns for - 5 V pulsed into deep depletion for sample Ge12S3 with 0.5 mm dot.

These three results all use the same lifetime of $\tau = 30$ ns in the theoretical equation. So lifetime estimated is 30 ns. In addition, the three figures show that the simulation line does not fit well with the experimental data. However, the total relaxation time from deep depletion to inversion matches with experimental data. The reason can be explained: if the lifetime of carrier is not a constant but changes with time possible due to a non-uniform distribution of defects in the depletion region. However, in the calculation, the parameter of lifetime is taken as a constant.

By rewriting Eq. (7.50) in term of C and C_f, then:

$$\frac{dC}{dt} = \frac{C^2}{TC_{ox}}\left[1 - \frac{C}{C_f}\right] \tag{7.52}$$

According to this equation, the measurement of slope at any value of C will obtain the time constant T which is a function of lifetime. Based on this equation, the instantaneous lifetime versus time can be plotted.

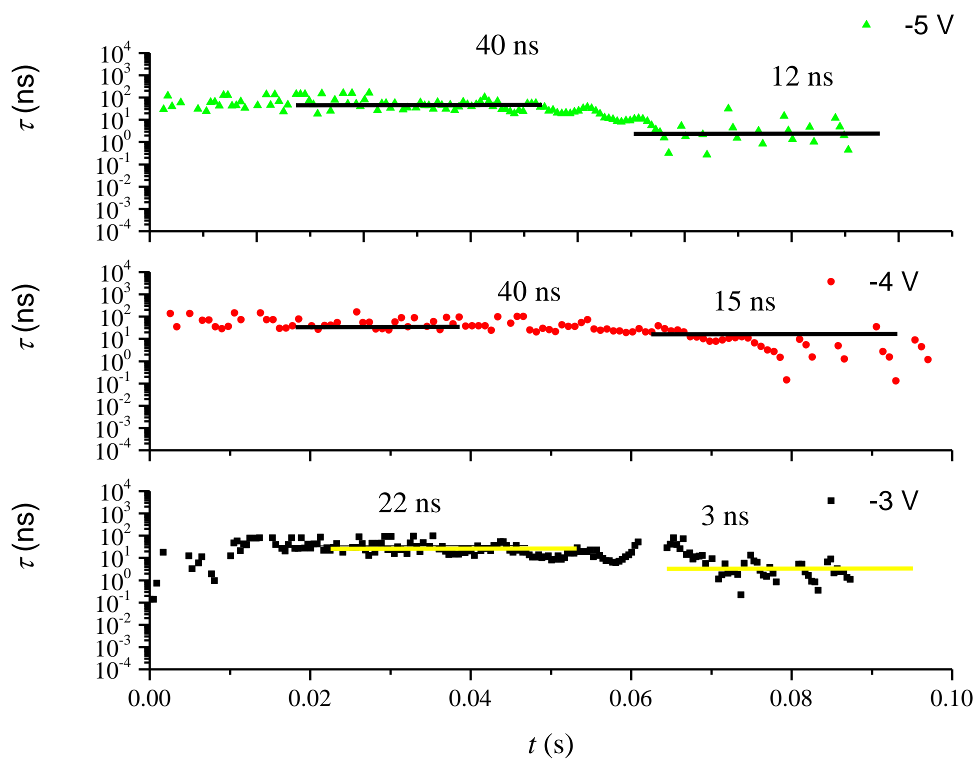

Fig. 7.15. Corresponding to Fig. 7.12, Fig. 7.13 and Fig. 7.14, the instantaneous lifetime versus time (sample Ge12S3 with 0.05 mm).

From Fig. 7.15, it can be observed that the measured lifetime is between 100 ns and 10 ns. So the measured lifetime is not constant. At the beginning, usually the lifetime is larger than later values in Fig. 7.15. This may be due to a surface generation contribution at the beginning.

This may explain why the experiment data does not fit well with the theory data in Fig. 7.12, Fig. 7.13 and Fig. 7.14. The average generation lifetime time is about 15 ns.

7.6.2.2 Second group of measurements

The 1 mm diameter dot MOS capacitor for sample Ge12S3 was used. The sample was again initially biased into inversion and then pulsed into deep depletion with different step voltages of – 3 V and – 4 V.

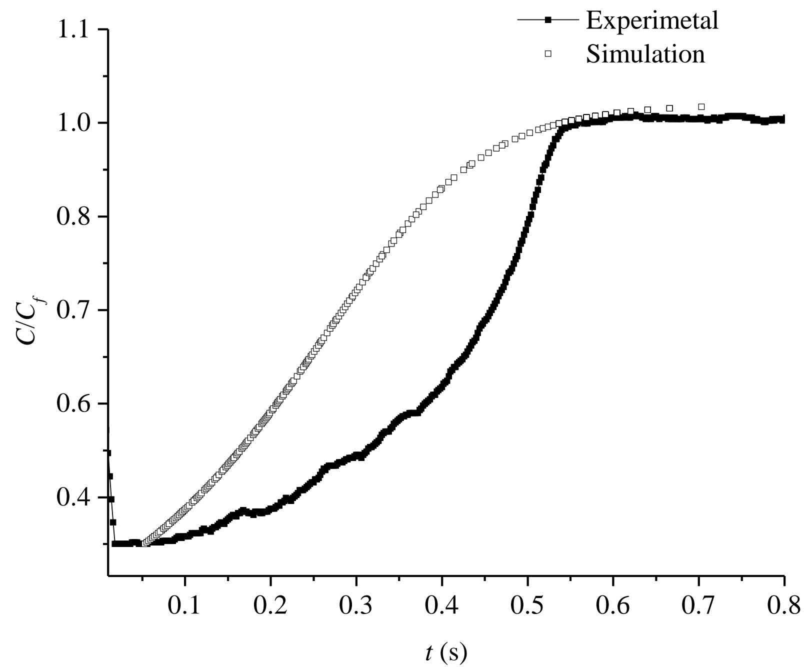

Fig. 7.16. Lifetime τ = 150 ns with when – 3 V pulse voltage applied for sample Ge12S3 with 1mm dot.

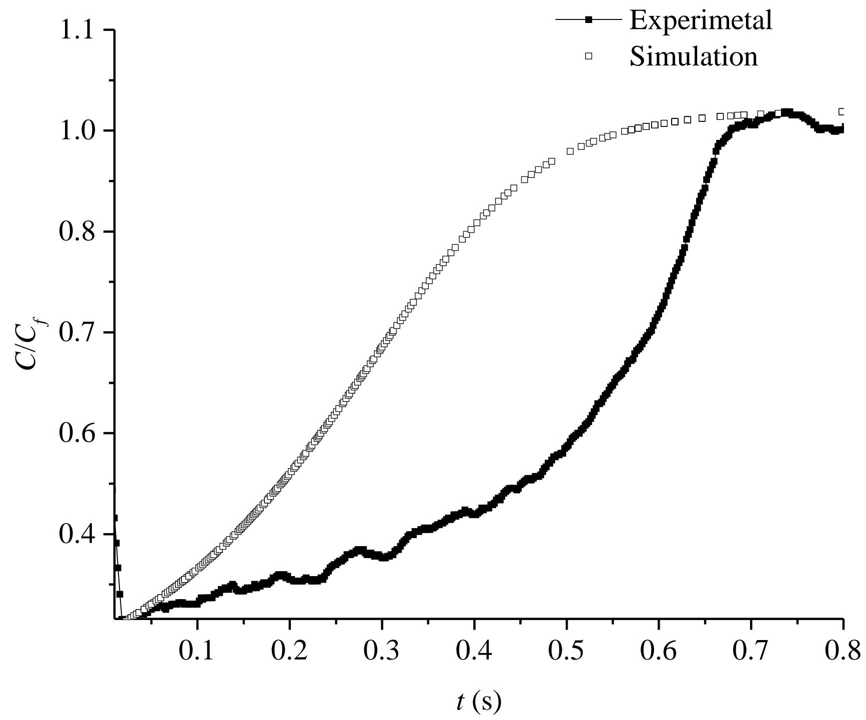

Fig. 7.17. Lifetime τ = 150 ns for – 4 V pulse voltage applied for sample Ge12S3 with 1mm dot.

These two results use the same lifetime τ = 150 ns in the theoretical equation. Compared to the first group measurement with 0.5 mm diameter gate used, the lifetime is larger by about one order of magnitude. The following figure also confirms this result.

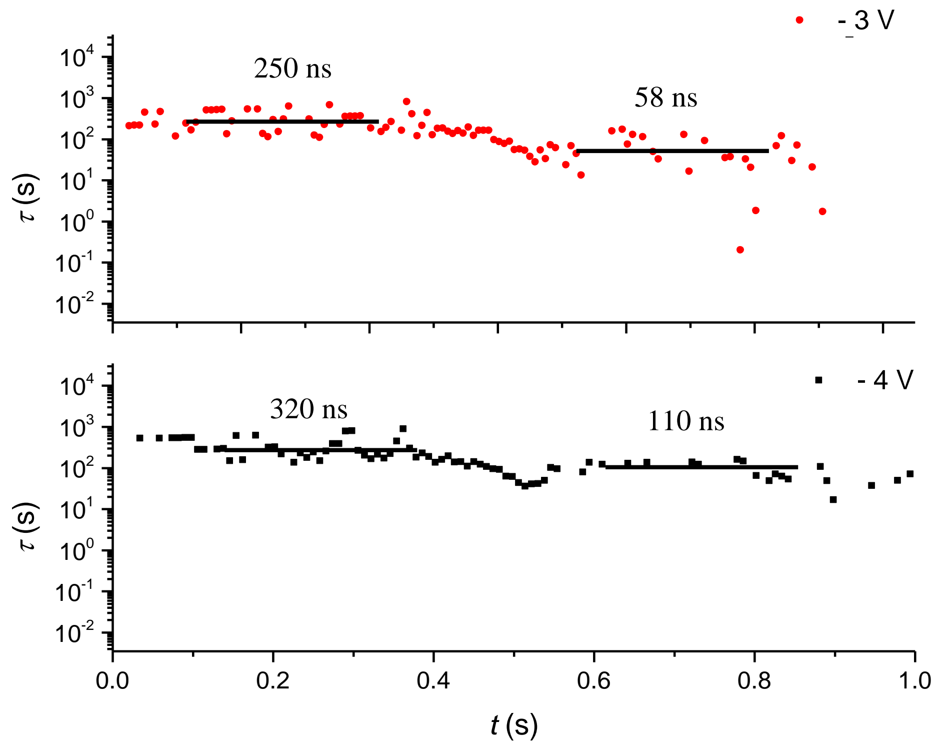

Fig. 7.18. Corresponding to Fig. 7.16 and Fig. 7.17, the instantaneous lifetime versus time.

Based on Fig. 7.15 and Fig. 7.18, the generation lifetime of minority carriers is 150 ns for a 1 mm diameter gate MOS capacitor and 30 ns for a 0.5 mm diameter gate MOS capacitor. The difference in lifetime for the two kinds of different diameter gate could be due to the differing contributions of scr generation under the gate characterized by the surface generation velocity *S*. Although the initially biased from inversion, it still cannot eliminate the surface generation velocity *S*. So the instantaneous lifetime versus time plot shows a higher lifetime at the early stage, afterwards it will become smaller due to the disappearance of surface generation. Measured after this early stage, the lifetime is of the order 10 ns.

The generation lifetime of minority carriers can be used to fit mechanism (a) with the experimental data. Fig. 7.19 shows the fits between calculations of capacitance in inversion with experimental data taken from sample Ge12S3. The calculation of capacitance is based on the equivalent circuit of Fig. 7.5, at room temperature; G_l is just the conductance of thermal generation process as discussed before. Fig. 7.19 shows the thermal generation of minority carriers could indeed lead to the low frequency response for the CV plots, at room temperature.

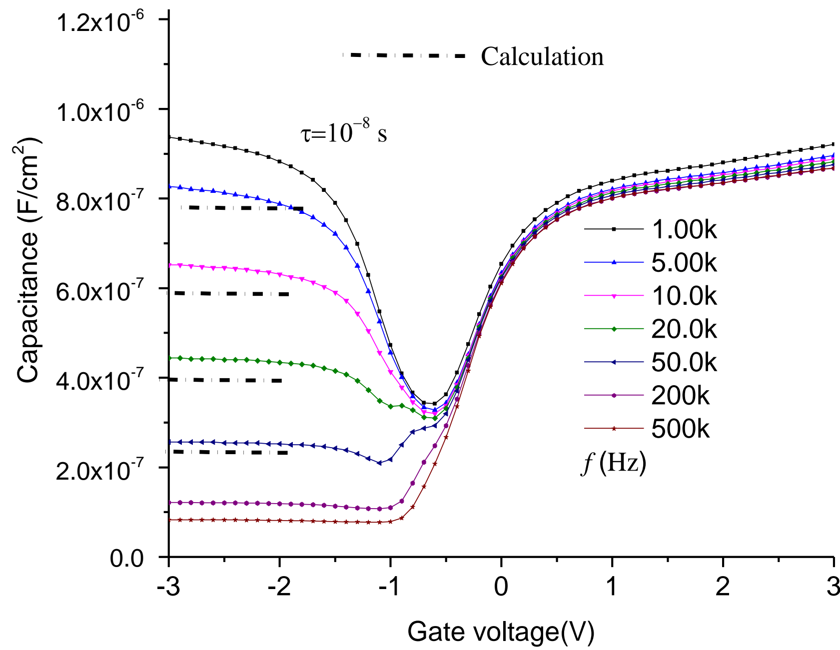

Fig. 7.19. The calculation of capacitance in the inversion region fits with experimental data of sample Ge12S3. Extracted doping concentration N_{sub} = 10^{16} cm^{-3}, and $C_D = 0.8 \times 10^{-7}$ F / cm^2, C_{inv} = 4.5 F / cm^2, mobility of hole is taken as 1200 cm^2 s^{-1} V^{-1}.

7.7 Conclusion

In conclusion, by measuring the ac conductance in strong inversion as a function of temperature, the extraction of activation energies indicates the thermal generation process represented by the parameter, G_{gr} is responsible for the low-frequency behaviour apparent in MOS capacitors measured at room temperature. The minority carrier generation life time is an important parameter used to model the thermal generation in depletion region for Ge-base MOS.

7.8 References

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Chapter 8 Models for frequency dispersion in accumulation

8.1 Introduction

This chapter will investigate another critical issue related to Ge-based device. That is, it has been widely observed there is frequency dispersion in the accumulation regime of *C-V* plots for Ge-based and III-V MOS device [1-4]. Such frequency dispersion can be attributed to exchanging carriers between conduction band states and oxide traps through the tunnelling process [1], as shown in Fig. 8.1. Oxide traps refer to the traps located within the oxide layer. When the MOS capacitor is in accumulation, the Fermi level locates near or above the conduction band of the semiconductor; such traps are also called 'bulk-oxide border traps' [1]. Moreover, these traps are usually associated with long characteristic time constants, thus also are treated as 'slow traps' based on this electrical property. In this chapter, the term 'oxide traps' is used throughout the chapter. These oxide traps could degrade the mobility of carriers and lead to threshold voltage instability [5, 6]. Therefore, it is vital to characterize oxide traps in Ge-based MOS devices.

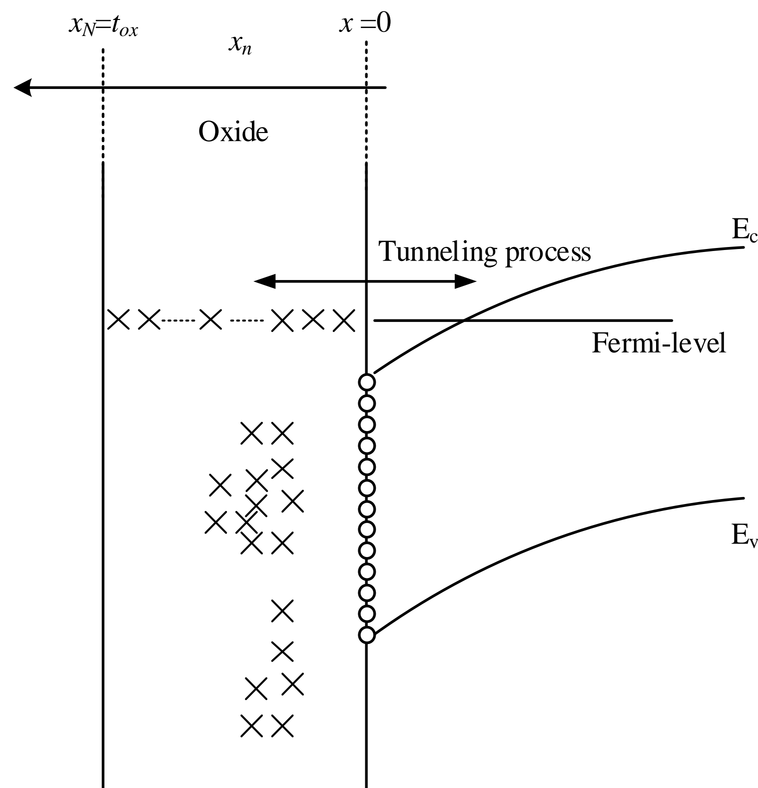

Fig. 8.1. Band diagram of an n-type Ge-based MOS when it is biased in accumulation. The Fermi-level is above the conduction band, and electrons are exchanged between oxide traps and conduction band states though the tunnelling process.

In this chapter, a distributed oxide traps model proposed by Yuan *et al* [1] is employed to study the frequency dispersion of *C-V* characteristics in accumulation regime for Ge-based MOS capacitors. Firstly, Yuan oxide trap model for Ge-based MOS will be described briefly. Then the oxide traps are evaluated based on Yuan's model. In addition, another phenomenon related to such frequency dispersion will be investigated, that is, the observation that frequency dispersion becomes pronounced as the gate voltage increases further into accumulation.

8.2 Model description

The frequency dispersion in the accumulation regime for Ge-based MOS has been attributed to the exchange of mobile carriers between oxide traps and conduction band states through the tunnelling process [1]. A sophisticated model has been proposed to explain this frequency dispersion in accumulation by Yuan *et al* [1]. The oxide traps are continuously distributed over the oxide depth with the equivalent circuit for this distribution of oxide as shown in Fig. 8.2. In this equivalent circuit, the oxide capacitance with thickness t_{ox} is divided into an number N of segments with branches of $\Delta Y_{ox}(x_n)$ connected at different depths.

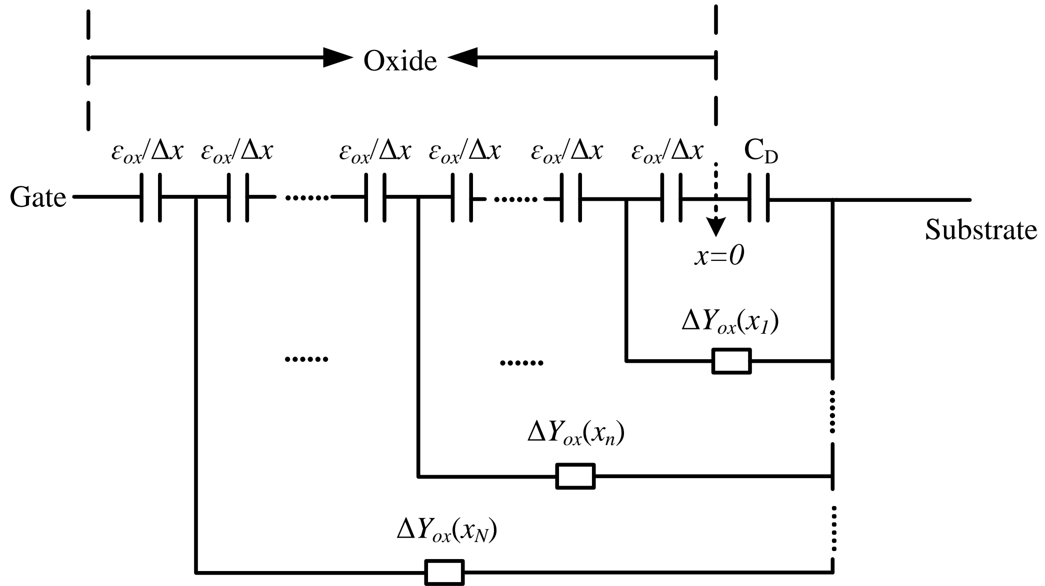

Fig. 8.2. Equivalent circuit for bulk-oxide traps distributed over the depth of the oxide layer for an n-type MOS capacitor in accumulation.

Following Yuan's model [1], the time constant for charge exchange between oxide traps and the conduction band based on the tunnelling process to the depth x_n can be expressed as:

$$\tau(x_n) = f_0 \tau_0 e^{2\kappa x_n} \tag{8.1}$$

where τ_0 is the time constant of the oxide traps over the interface between oxide and Ge

$$\tau_0 = (n_s \sigma v_{th})^{-1} \tag{8.2}$$

Here, n_s is the carrier density at the semiconductor surface, σ is the trap cross-section, and v_{th} is the carrier thermal velocity.

The total incremental admittance at x_n is given by:

$$\Delta Y_{bt}(\mathrm{x_n}) = \frac{q^2 N_{bt} \ln\left(1 + j\omega\tau_0 e^{2\kappa x_n}\right)}{\tau_0 \mathrm{e}^{2\kappa \mathrm{x_n}}} \Delta x \tag{8.3}$$

where q is electron charge N_{bt} is the oxide trap density per volume per energy (cm^3J^{-1}) at x_n and at the Fermi energy E_f, κ is the attenuation coefficient of tunnelling in cm^{-1},

This can be expressed as:

$$\kappa(E) = \sqrt{2m^*\left(E_C^{ox} - E\right)}\Big/\hbar \tag{8.4}$$

m^* is the effective electron mass in the oxide, the tunnelling barrier decided by the conduction band edges of the oxide (E_C^{ox}), the trap energy (E), and the reduced plank constant $\hbar$.

The equivalent admittance at position x_n by looking into the semiconductor in Fig. 8.2, the recursive nature of the distributed circuit gives the admittance of the next position x_{n+1}

$$Y_{n+1} = \Delta Y_{bt}(x_n) + \frac{1}{\dfrac{\Delta x}{j\omega\varepsilon_{ox}} + \dfrac{1}{Y_n}} \tag{8.5}$$

where ε_{ox} is the oxide permittivity; initial condition $Y_1(x=0) = j\omega C_D$; where C_D is the accumulation capacitance when the capacitor is in accumulation.

8.2.1 Dependence of depth probing with frequency

The relationship between the depth probed within the oxide layer and the time constant of oxide traps can be found from Eq (8.1). The depth probed is proportional to the time constant of a trap. The oxide traps located deeper within the layer have long time constants and can only follow lower frequency small ac signals. In this study, the maximum depth can be probed when the frequency is down to 100 Hz. The depth can be obtained through Eq (8.6) converted from Eq (8.1). Only oxide traps residing between the interface and maximum depth probed contribute to the frequency dispersion in accumulation.

$$x_{\max} = \frac{1}{2\kappa} \ln\left(\frac{1}{\omega\tau_0}\right) \tag{8.6}$$

8.3 Results and discussion

Fig. 8.3, Fig. 8.4 and Fig. 8.5 show the C-V characteristics of sample Ge39S1, Ge39S2 and Ge39S3 at room temperature when they are measured in the parallel measurement mode, respectively. It can be observed that there is frequency dispersion in accumulation for all three samples. In addition, another phenomenon associated with this frequency dispersion can be observed in Fig. 8.3, Fig. 8.4 and Fig. 8.5, that is, the frequency dispersion becomes stronger

when gate voltage increases; especially when as the MOS approaches strong accumulation, the frequency dispersion become extreme high as shown in Fig. 8.3 and Fig. 8.4. A similar phenomenon has been reported [7] when capacitors with significant leakage current is measured in the series measurement mode. The sample Ge39S1 measured in series measurement mode is shown in Fig. 8.6.

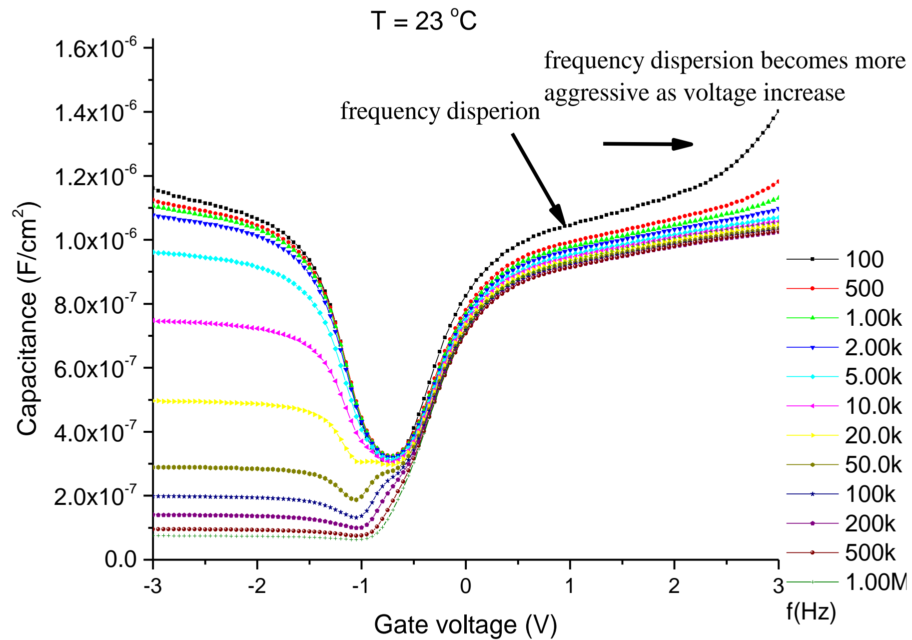

Fig. 8.3. The *C-V* characteristics of MOS sample Ge39S1 at room temperature (parallel measurement mode).

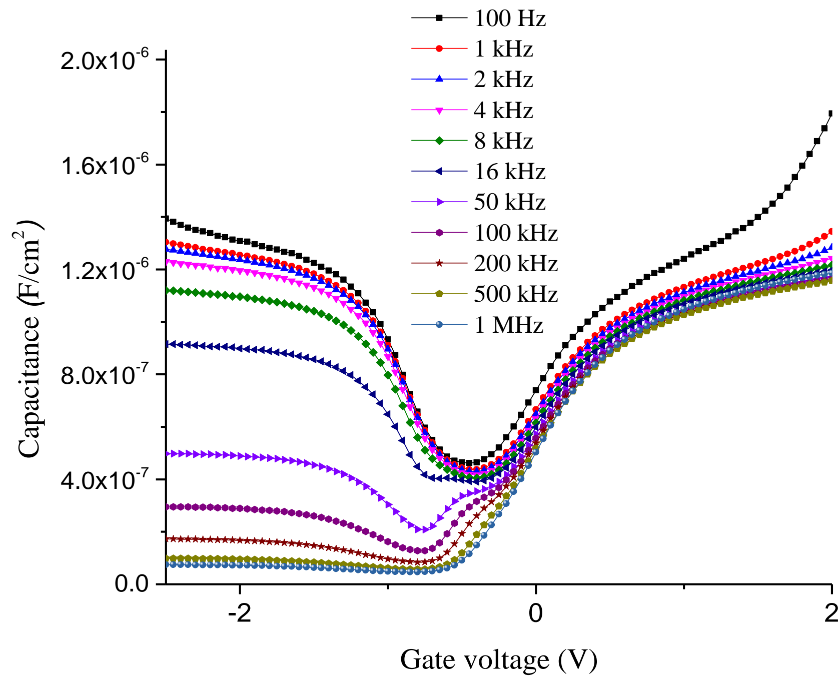

Fig. 8.4. The *C-V* characteristics of MOS sample Ge39S2 at room temperature (parallel measurement mode).

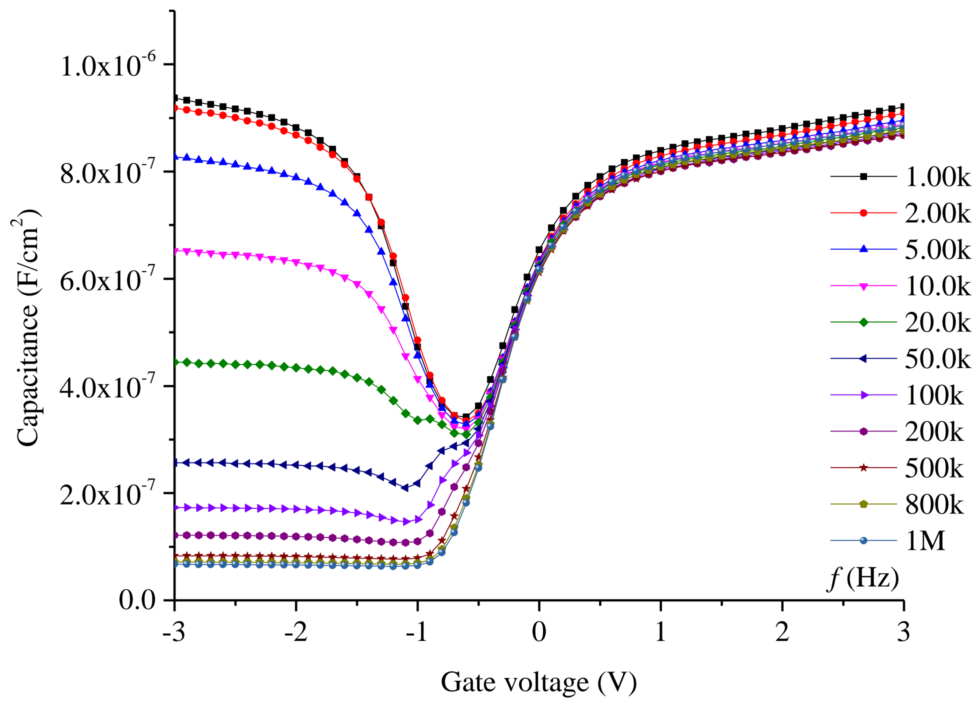

Fig. 8.5. The *C-V* characteristics of MOS sample Ge39S3 at room temperature (parallel measurement mode).

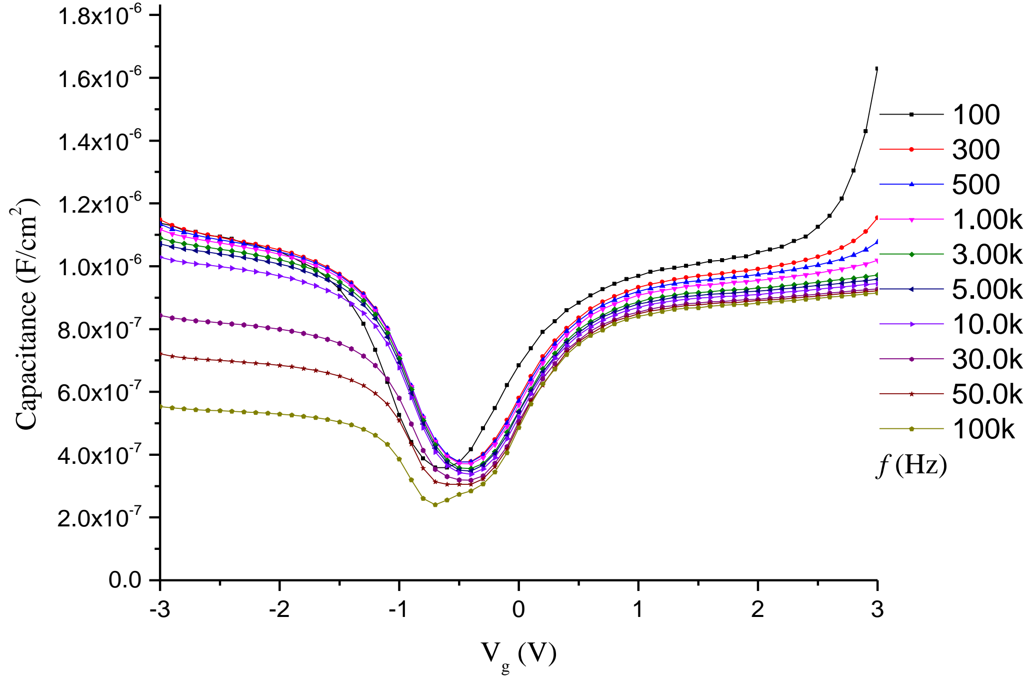

Fig. 8.6. The *C*-*V* characteristics of MOS sample Ge39S1 at room temperature (series measurement mode).

As shown in Fig. 8.6, when the capacitor is measured in series mode, the frequency dispersion also remains strong when gate voltage increases. As discussed before, leakage current may be responsible for this phenomenon when measured in series measurement mode as shown in Fig. 8.6. In addition, the leakage current may also be responsible for this phenomenon when MOS is measured in parallel measurement mode as shown in Fig. 8.3, Fig. 8.4 and Fig. 8.5. To identify if this dispersion is caused by leakage current, a three-element circuit model of a MOS capacitor in accumulation with series resistance and leakage current [8] is explored, as illustrated in Fig. 8.7 (a); C_{ox} is oxide capacitance, G_{ln} represents the conductance which is associated with the leakage current through the oxide and R_s refers to the series resistance of the bulk semiconductor and contacts. Regarding the measurement mode: parallel measurement mode means the MOS capacitor is represented by a capacitance C_{mp} and conductance G_{mp} in parallel connection as shown in Fig. 8.7 (b); series parallel measurement mode means the MOS capacitor is represented by a capacitance C_{ms} and resistance R_{ms} in series connection, as shown in Fig. 8.7 (c).

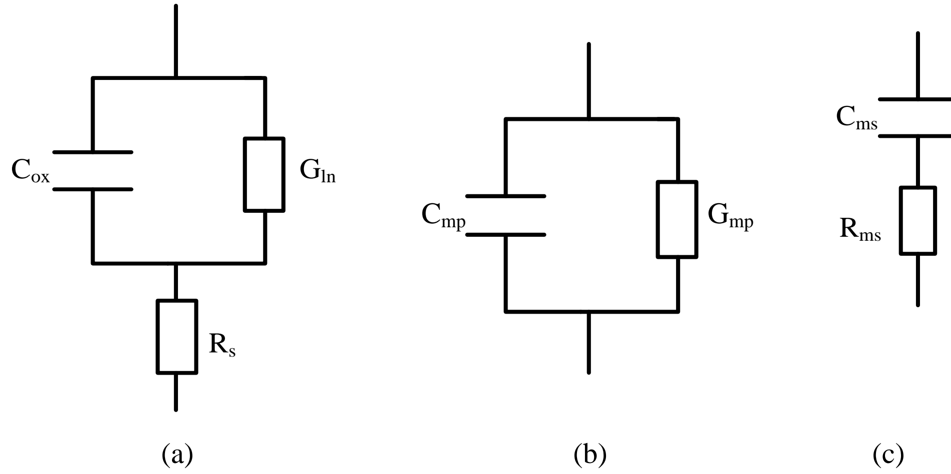

Fig. 8.7. (a) Equivalent circuit for MOS capacitor in accumulation; (b) parallel measurement mode; (c) series measurement mode.

For the three circuits shown in Fig. 8.7, the impedance can be obtained respectively based on Eqs (8.7), (8.8) and (8.9) where Z_a is the impedance of circuit as shown in Fig. 8.7 (a), and the measured impedance Z_{mp} in parallel mode (Fig. 8.7 (b)) and Z_{ms} in series mode (Fig. 8.7 (c)):

$$Z_a = \frac{1}{C_{ox} j\omega + G_{\ln}} + R_s \qquad (8.7)$$

$$Z_{mp} = \frac{1}{C_{mp} j\omega + G_{mp}} \qquad (8.8)$$

$$Z_{ms} = \frac{1}{C_{ms} j\omega} + R_{ms} \qquad (8.9)$$

Next, based on these circuits, the effects of the series resistance and leakage current on *C-V* characteristics are explored respectively.

When the MOS is measured in parallel mode, the following equation is satisfied:

$$Z_a = Z_{mp} \qquad (8.10)$$

Comparing the real and imaginary parts of Z_a and Z_{mp}, measured capacitance in parallel mode can be obtained:

$$C_{mp} = C_{ox}\left(1 - \frac{2R_s G_{\ln} + R_s^2 G_{\ln}^2 + \omega^2 C_{ox}^2 R_s^2}{(1 + R_s G_{\ln})^2 + \omega^2 C_{ox}^2 R_s^2}\right) \qquad (8.11)$$

Similarly, for series measurement mode, comparing the real and imaginary parts of Z_a and Z_{ms}, and the measured capacitance in series mode can be obtained:

$$C_{ms} = C_{ox}\left(1+\frac{G_{\ln}^2}{C_{ox}^2\omega^2}\right) \tag{8.12}$$

The theoretical capacitance for both parallel and series measurement mode have now been obtained. Nest the influence of leakage current on the capacitance will be explored. Both equations (8.11) and (8.12) contain the leakage current conductance G_{ln}. The current-voltage (I-V) measurement is shown in Fig. 8.8 for sample GeW39S1. Two dots of MOS sample are measured, and the area of the capacitor is 4.9×10^{-4} cm^2 (0.25 mm diameter dot).

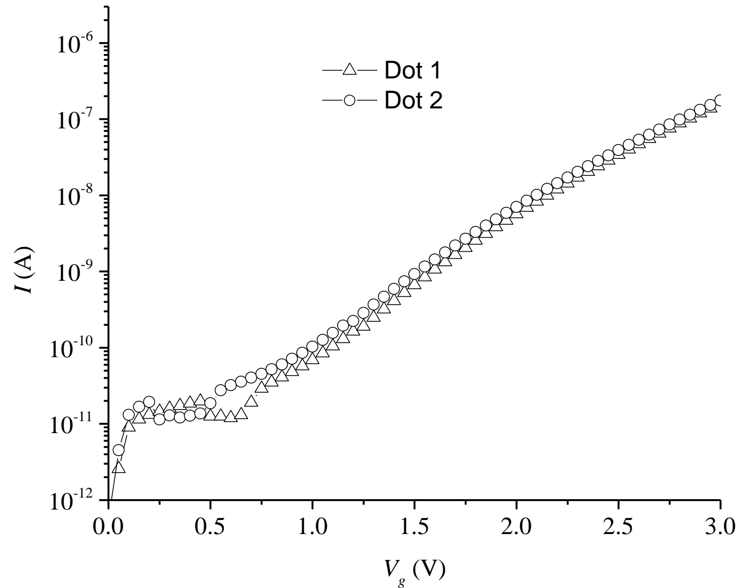

Fig. 8.8. I-V plot for MOS capacitor from sample Ge39S1 for 0.25mm diameter dot.

From Fig. 8.7 (a), it can be observed that the leakage current flows through G_{ln} and R_s. Moreover, this circuit can be converted to the equivalent circuit as shown in Fig. 8.9 of where $R_{ln} = 1/G_{ln}$.

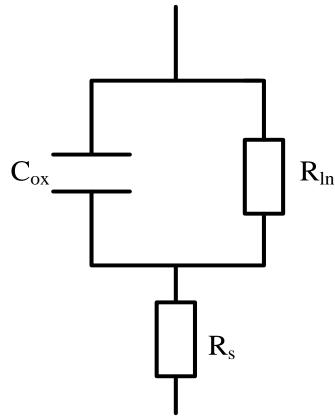

Fig. 8.9. The equivalent circuit derived from that of Fig. 8.7 (a).

The small signal leakage current is represented by gate voltage across resistance R_{ln}+R_s. The value of R_{ln}+ R_s can be extracted from the ΔV_{dc} / ΔI_{dc} based on the (*I-V*) characteristic, as shown in Fig. 8.10.

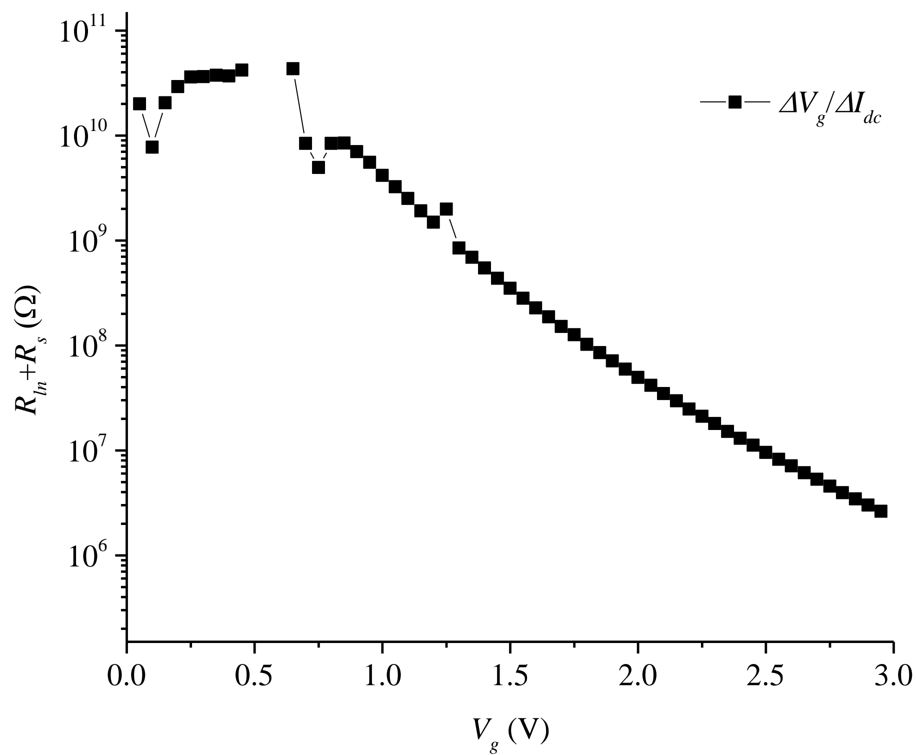

Fig. 8.10. Extracted R_{ln}+ R_s based on *I-V* characterization for MOS capacitor of sample Ge39S1.

R_s is expected to be constant as gate voltage changes. From Fig. 8.10, it can be observed, $R_{ln}+R_s$ decreases as gate voltage increases. Therefore, it can be assumed that the decrease of $R_{ln}+R_s$ is attributed to decrease of R_{ln}. Thus, it is reasonable to assume $R_{ln} >> R_s$, because the main change in $R_{ln}+R_s$ is associated with R_{ln}.

8.3.1 Theoretical capacitance for parallel measurement mode

Eq (8.11) for the theoretical measured capacitance in parallel mode can be transformed into the following form:

$$C_{mp} = C_{ox}\left(\frac{1}{(1+R_s G_{\ln})^2 + \omega^2 C_{ox}^2 R_s^2}\right) \tag{8.13}$$

The parameter G_{ln} is extracted from Fig. 8.10 for sample Ge39S1. The oxide capacitance C_{ox} obtained from Fig. 8.3 for sample Ge39S1 is 1.02×10^{-6} F/cm^2 at 2 kHz. Fig. 8.11 shows theoretical plots of the capacitance using Eq (8.13), with series resistance R_s 40.7 Ω to explore its effect [8]. However, because the series resistance R_s is a fixed value thus the induced frequency dispersion should not change with gate voltage. As shown in Fig. 8.11, the calculated frequency dispersion caused by series resistance indeed does not significantly change with gate voltage. Therefore, it can be concluded that the frequency dispersion in accumulation of Fig. 8.3, Fig. 8.4 and Fig. 8.5 is not mainly attributed to series resistance, because these frequency dispersion becomes stronger when gate voltage increases. In addition, although the leakage current is taken into account in this calculation, there is no effect from it as shown in Fig. 8.11. Thus, the phenomenon that frequency dispersion in accumulation becomes stronger when gate voltage increases is not caused by leakage current when the MOS is measured in parallel measurement mode.

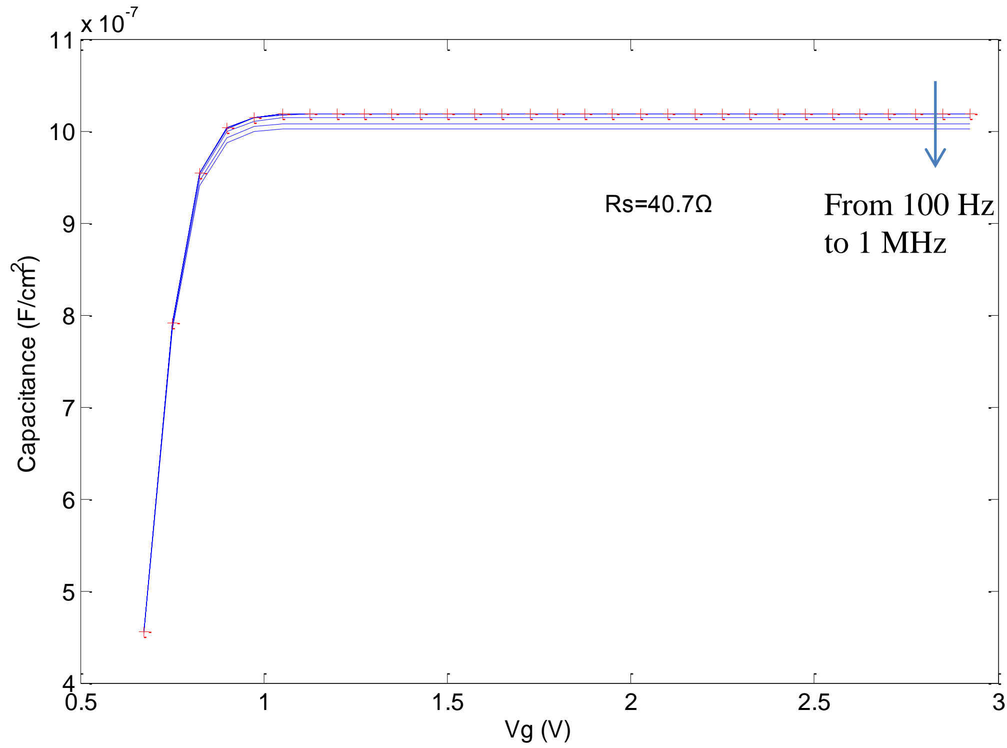

Fig. 8.11. Calculated capacitance using equation (8.13), in parallel mode with different series resistance 40.7 Ω when MOS is measured in parallel measurement mode.

8.3.2 Theoretical capacitance for series measurement mode

The capacitance measured in series measurement mode can however be influenced by the leakage current, which is denoted by G_{ln}. At a given frequency, when the gate voltage increases, the oxide leakage current also increases, therefore in Eq (8.12), the leakage current conductance G_{ln} is dependent on gate voltage. Fig. 8.12 shows the calculation based on Eq (8.12) for the capacitance in accumulation when measured in series measurement mode. The oxide capacitance is 1.02×10^{-6} F/cm^2 for sample Ge39S1. The G_{ln} as a function of gate voltage is also extracted from Fig. 8.10.

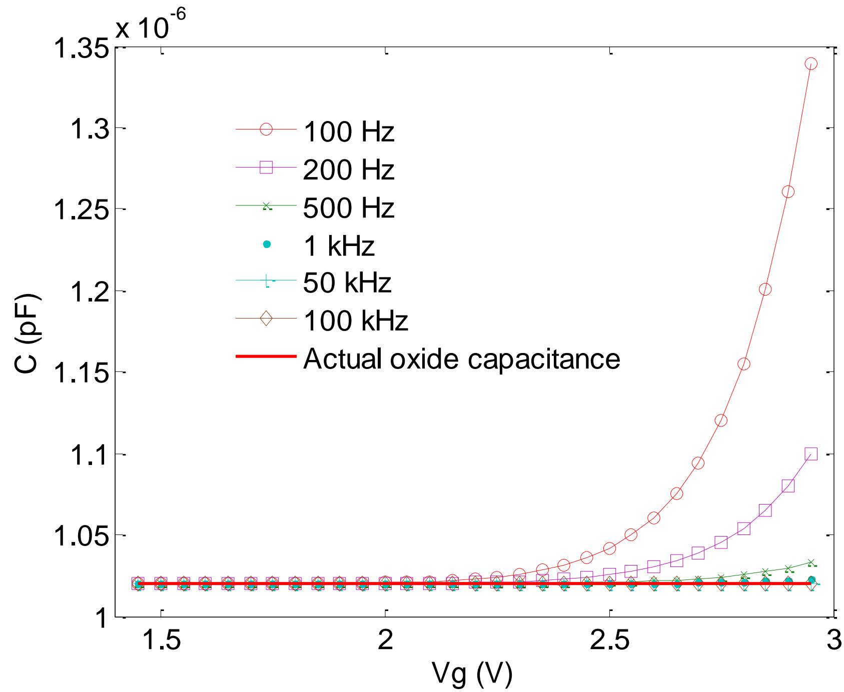

Fig. 8.12. Calculated capacitance when MOS is measured in series measurement mode

From Fig. 8.12, it can be observed that the effect of the leakage current is to cause the apparent measured capacitance to increase as the gate voltage increases over the low frequency range from 100 to 500 Hz. However, when the frequency is higher than 1 kHz, the apparent increase of capacitance with gate voltage is not observed. This is because at sufficiently high frequency, the denominator of the second term, namely $1+G_{in}/(C_{ox}\omega)^2$, in equation (8.12) becomes very large compared to the numerator as the square of G_{In}, the second term is quite small, and then measured capacitance approaches oxide capacitance at high frequency. However, this phenomenon only happens for series rather than the parallel measurement mode.

To conclude, the leakage current may explain the phenomenon in the series measurement mode. However, the series resistance is not the reason for frequency dispersion in accumulation when MOS is measured in the parallel mode, because frequency dispersion induced by series resistance does not change as gate voltage increases. The possible reason for such phenomenon when MOS is measured in parallel measurement is investigated in the next section.

8.3.3 Distribution of oxide traps

The most likely reason for the dispersion phenomenon is related to the distribution of oxide trap concentration. The distribution of oxide trap concentration could vary over both oxide depth and energy level. At different gate voltages, the Fermi level changes and hence the trap occupation could vary. If there is a higher concentration as the Fermi level is shifted by increasing gate voltage, the frequency dispersion becomes stronger. A distribution of oxide

trap concentration with Fermi-energy level is shown in Fig. 8.13. In this model, the oxide trap concentration with depth is assumed to be constant. The oxide trap concentration changes with the energy level which is determined by the gate voltage. The calculation of frequency dispersion based on a non-uniform distribution of oxide traps has been obtained and shown in Fig. 8.14. It should be noted that in this calculation, the oxide trap concentration over the oxide depth is assumed to be constant at a certain energy level. The oxide trap concentration only changes with the energy level. The change of oxide trap concentration over oxide depth will be discussed later. In this section the relationship between frequency dispersion and the distribution of oxide trap concentration alone is considered. The profile of oxide trap concentration with the gate voltage can be given by simply assuming the increase of oxide trap concentration is proportional to gate voltage as shown Fig. 8.13. Because this calculation is used to shows relationship between frequency dispersion and oxide traps concentration, a simple linear profile of oxide traps concentration is considered.

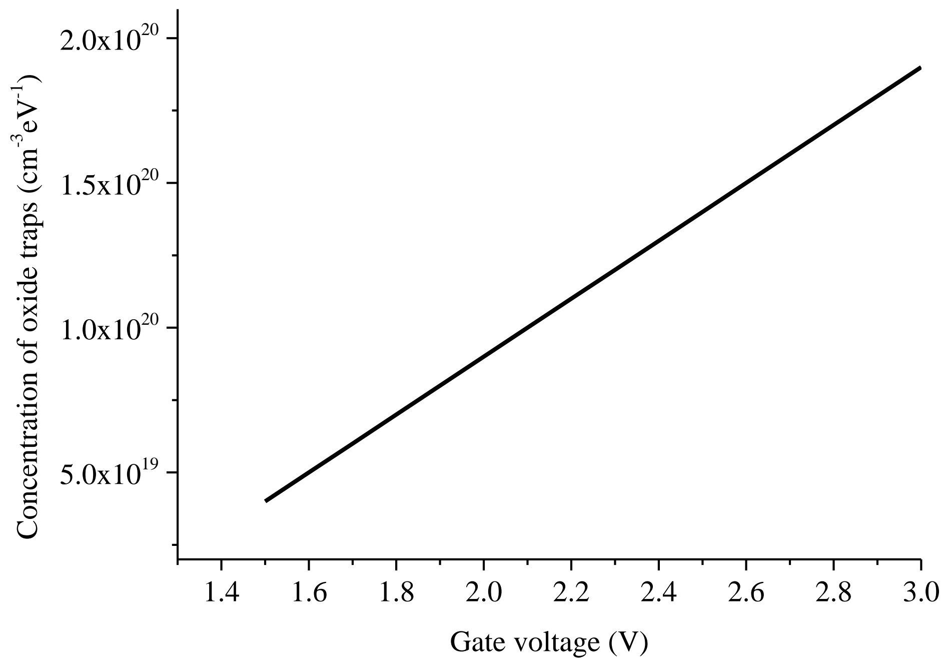

Fig. 8.13. The profile of concentration of oxide traps over the gate voltage.

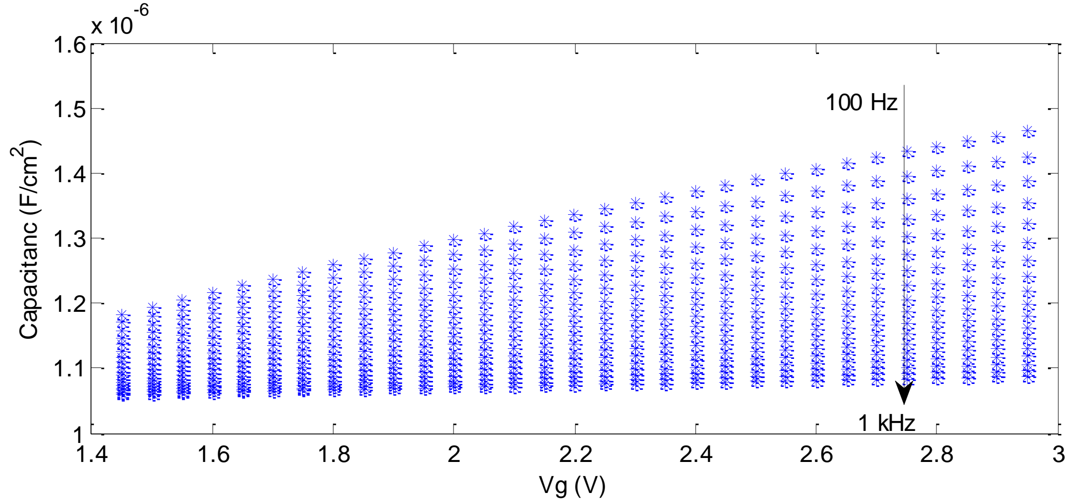

Fig. 8.14. The *C-V* characteristic which uses the non-uniform distribution of oxide traps with gate voltage.

Model parameters used are: C_{ox}=1.05×10^{-6}F /cm^2, $t_{il,GeO2}$=4.7 nm, $\varepsilon_{il,GeO2}$= 6×8.85×10^{-14} F/cm^2, C_s=4.2×10^{-5}F/cm, τ_0=10^{-10} s, κ is calculated based on a band-offset between Ge and GeO_2 of 0.80 eV.

It can be observed that as the Fermi level approaches higher energy levels with higher oxide traps concentration following increasing gate voltage, the frequency dispersion becomes stronger as shown in Fig. 8.14. The distribution of oxide trap concentration with gate voltage has an impact on the frequency dispersion. This could explain why the frequency dispersion becomes stronger as gate voltage increases. Thus, the non-uniform distribution of oxide trap concentration over energy level can be responsible for the reason why frequency dispersion becomes stronger when gate voltage increases.

8.3.4 Model fit with experimental data

The distributed bulk-oxide trap model is employed to fit *C-V* plots in accumulation for samples Ge39S1, Ge39S2 and Ge39S3. The model parameters is given in Table 8.1.

Table 8.1. Parameters used in calculation [1, 9].

	C_{ox}	τ_0	κ	C_s	$\varepsilon_{hk,HfO2}$
Ge39S1	1.02×10^{-6}F /cm^2	10^{-10} s	3.47×10^{7}cm^{-1} (based on a band-offset between Ge and GeO_2 of 0.80 eV and electron effective mass m^*=0.56m_0)	4.2×10^{-5}F/cm	6×8.85×10^{-14} F/cm^2
Ge39S2	1.2×10^{-6}F /cm^2				
Ge39S3	0.9×10^{-6}F /cm^2				

The capacitance is measured at two different gate voltages, and the oxide trap concentration N_{bt} is used to fit with experiment data.

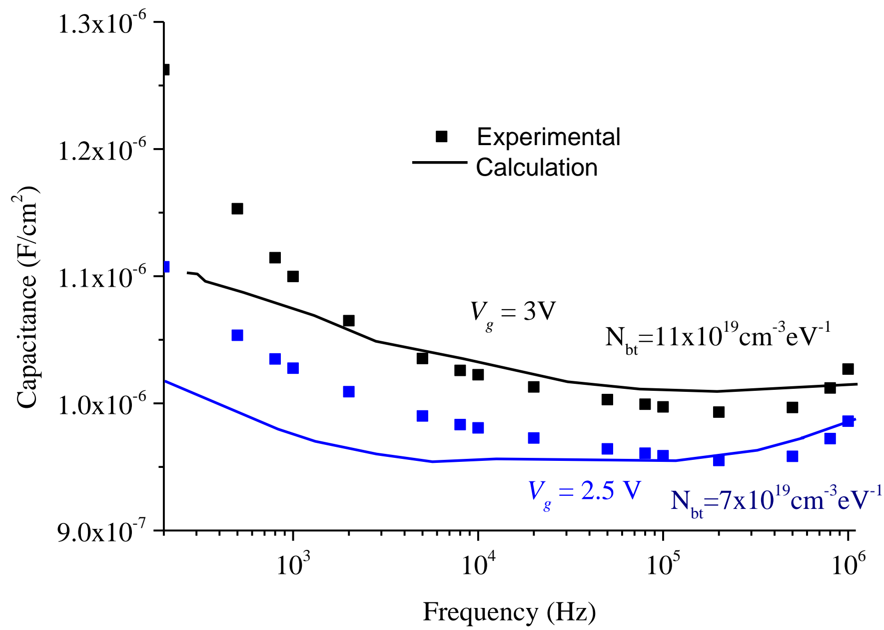

Fig. 8.15. The model and experimental data fit when gate voltage is 2.5 V and 3 V for sample Ge39S1.

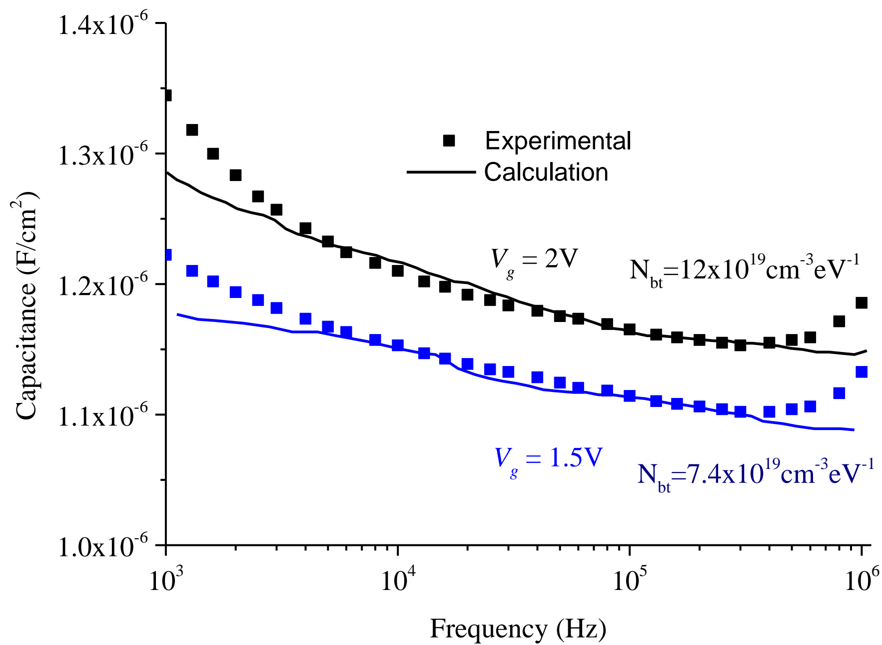

Fig. 8.16. The model and experimental data fit when gate voltage is 2 V and 1.5 V for sample Ge39S2.

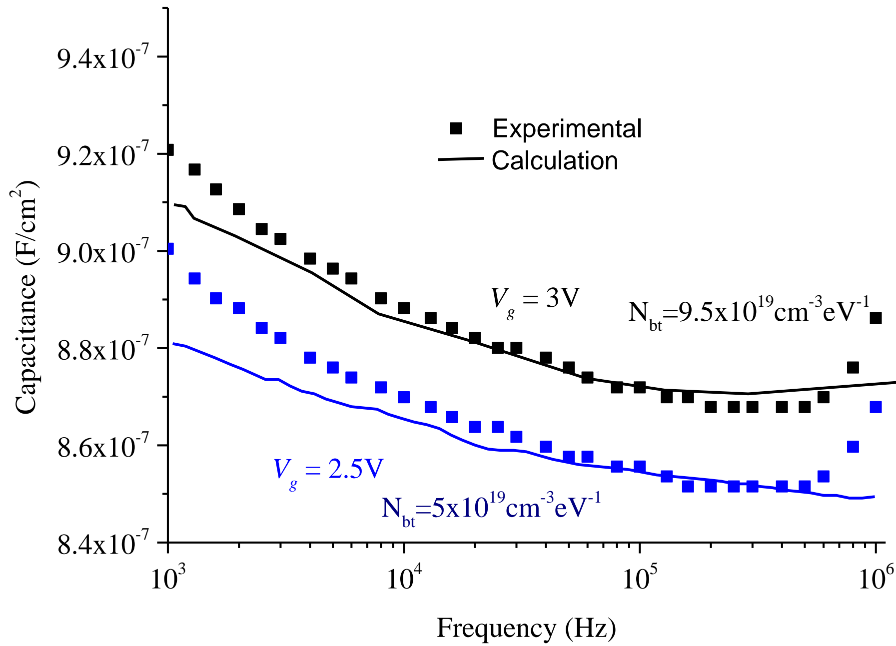

Fig. 8.17. The model and experimental data fit when gate voltage is 3 V and 2.5 V for sample Ge39S3.

The results show a good match is over some range of the frequency, the oxide traps can successfully explain the frequency dispersion in strong accumulation. At low frequency and high frequency there is a difference between theoretical and experimental data. As discussed, the oxide traps could vary over both oxide depth and energy level. At a given gate voltage, a constant oxide concentration is given to fit model and experimental. However, the oxide concentration could vary over depth. Thus there is some disagreement between model and experimental data.

8.3.5 Instrument errors

A further possibility for frequency dispersion in accumulation lies in the ability of the LCR meter to accurately measure the capacitance. If the oxide leakage becomes too large, the dissipation factor can be used to check the accuracy of the measurement, using measured capacitance G_m and conductance G_m. An approximation for the instrumentation error in the presence of high leakage is given by the formula $0.1\times\left(1+\sqrt{1+D^2}\right)$ where $D=\frac{real(Z_m)}{imag(Z_m)}$ [10].

The maximum of D is 1.4 over the frequency and gate voltage range in parallel measurement mode (Fig. 8.18). The error is found to be no more than 0.3%. Therefore, the frequency dispersion in accumulation is not caused by instrument error.

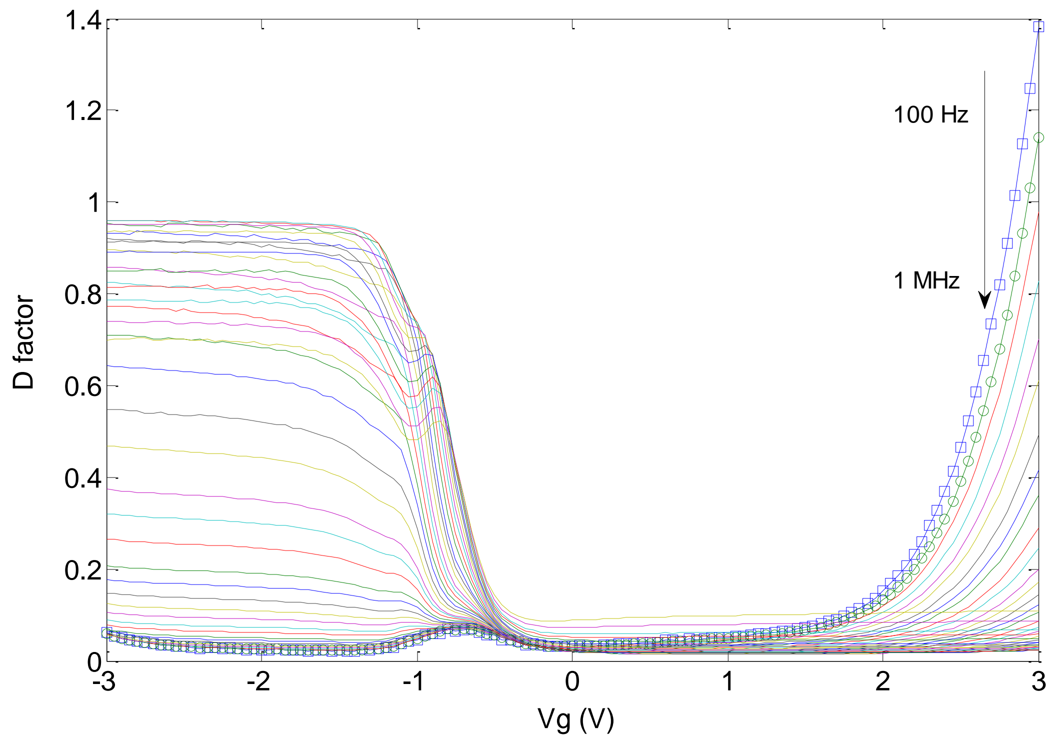

Fig. 8.18. Estimated *D* factor over the gate voltage and frequency range in parallel measurement mode.

8.4 Conclusion

Yuan's model has been employed to study the frequency dispersion in accumulation for samples Ge39S1, Ge39S2 and Ge39S3. The stronger frequency dispersion with increasing gate voltage has been analyzed and discussed. Possible reasons have been considered and discussed. Model results indicate that a non-uniform distribution of oxide traps rather than leakage current is the most likely explanation for the stronger frequency dispersion. The result also suggests the necessity for further developing high-quality gate dielectrics with low border trap concentration for improving the stability of Ge-based MOSFETs.

8.5 References

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Chapter 9 Conclusions and future work

9.1 Experimental conclusion

In this thesis, electrical characterization has been used to obtain key MOS parameters from Ge-MOS gate stacks, namely interface state densities and oxide traps. This section will present the conclusion of these results.

Table 9.1 Summary of first sample group Ge12S with different thickness HfO2 deposited by ALD using O-plasma as oxidant with Al_2O_3 as protection layer:

Samples	HfO_2 oxide thickness	Interface states density (mid-gap)	Oxide traps (V_g = 3 V)
Ge12S1	3.5 nm	4.1×10^{12} eV^{-1} cm^2	9.2×10^{19} cm^3eV^{-1}
Ge12S2	7 nm	3.9×10^{12} eV^{-1} cm^2	8×10^{19} cm^3eV^{-1}
Ge12S3	14 nm	2.6×10^{12} eV^{-1} cm^2	7.8×10^{19} cm^3eV^{-1}

Table 9.2 Summary of second sample group Ge39 comprising gate stacks with different thickness HfO2 deposited by ALD using O-plasma as oxidant:

Samples	HfO_2 oxide thickness	Interface density states	Oxide traps
Ge39S1	3.5 nm	4.9×10^{12} eV^{-1} cm^2	11×10^{19} cm^3eV^{-1}
Ge39S2	7 nm	4.7×10^{12} eV^{-1} cm^2	12×10^{19} cm^3eV^{-1}
Ge39S3	14 nm	2.9×10^{12} eV^{-1} cm^2	9.5×10^{19} cm^3eV^{-1}
Ge39S4 (S-passivation with Al2O3)	3.5 nm	2.7×10^{12} eV^{-1} cm^2	11.6×10^{19} cm^3eV^{-1}

Both tables show that the interface state density is slightly different and of the order 10^{12} $eV^{-1}cm^2$ for all thicknesses of high-κ oxide for the first group of samples with Al_2O_3 as the protecting layer. The results demonstrate that the thickness of high-κ oxide has no significant effect on the interface states density. Therefore the interface quality is mainly decided by the interfacial layer rather than hafnia thickness. It also shows that the oxide trap concentrations are of the order 10^{19} eV^{-1} cm^3 for all thicknesses of high-κ oxide for the first group of samples. This indicates that the thickness of high-κ oxide has a significant effect on the interface state density.

Comparison of samples Ge12S and Ge39S, shows that the interface states density is of the same order of magnitude which indicates that both methods have same level of ability to

passivate the interfacial layer. In addition, the oxide trap densities are slightly different and of the order of 10^{19} cm^3eV^{-1}. Both methods yield similar values of oxide traps.

9.2 Summary

Continuously scaling of Si MOSFETs has been limited due to high leakage current through the MOS gate which is caused by the need for an ever thinner oxide layer. To overcome this scaling problem, high-κ dielectric is introduced to replace the SiO_2 oxide and allow further scaling of MOSFETs. With the purpose to increase the speed of circuit and drive current, an alternative MOSFET channel material with high carrier mobility should be incorporated. Ge, as a material candidate in same group with Si exhibits higher electron and hole mobility has been proposed. High-κ on Ge can be a competitive solution to achieve two goals. However, the unstable Ge native oxide GeO_2 between high-κ and Ge has been one of major problem for Ge channel MOSFETs.

Two methods in this work are used to fabricate high-κ on Ge MOS. Al_2O_3 formed in MBE is employed as a layer to protect the GeO_2. Sulphur-passivation is a possible solution to passivate the interface. This work explores several issues related to high-κ on Ge gate.

Firstly, several conventional interface states measurement method are investigated in terms of Ge-based MOS. The low-high frequency method fails in measurement of interface state density in Ge-based MOS, because the extraction of C_S from the C-V plot at 1 MHz. has been affected by interface states with high characteristic frequency. Terman's method suffers from the same problem. In addition, Terman's method measures both slow traps and interface states. The presence of slow traps will over-estimate the extracted interface state density. The conductance method is preferable but low temperature is required to sense interface states near band edges in both n- and p-type Ge-based MOS.

Secondly, the presence of a potential well or notch at the interface of native GeO_2 and high-κ dielectric and its role as a possible charge trapping site was addressed in this work. The number of quantum bound states was calculated by solving the Schrödinger equation. The model was then extended to three-dimensions and the average electron occupancy of notch for various device parameters was calculated. The simulation results reveal that there are no stable states in the notch for IL thickness less than 1 nm. The threshold voltage shift induced by the electrons confined in the notch was calculated from simple electrostatics with the conclusion that the threshold voltage shift for an 8-nm node Ge MOSFET is vanishingly small. However, the shift would be significant for larger devices and when the IL thickness is more than 1.2 nm.

Thirdly, the low-frequency behaviour of Ge-based MOS was investigated. By measuring ac conductance in strong inversion as a function of temperature, the extraction of activation energies indicates the thermal generation process represented by the parameter, G_{gr} is

responsible for the low-frequency behaviour apparent in MOS capacitors measured at room temperature. The minority carrier generation lifetime is an important parameter used to model the thermal generation in depletion region for Ge-base MOS.

Finally, the frequency dispersion in accumulation region for samples is studied based on Yuan's model. Model results indicate that a non-uniform distribution of oxide traps rather than leakage current is the most likely explanation for the stronger frequency dispersion. The result also suggests the necessity for further developing high-quality gate dielectrics with low oxide traps concentration for improving the stability of Ge-based MOSFETs.

9.3 Future work

This thesis investigates, demonstrates, and examines various issues related to Ge-based MOSFETs with high-κ dielectric for future CMOS development. In order to realize the full performance advantage in applying Ge into deeply scaled MOSFETs devices, further research is worthwhile studying in the following areas:

The high-quality interface between high-κ and Ge is still vital to achieve a high performance MOSFETs. In this work, two kinds of methods have been employed to achieve 10^{12} $cm^{-1}eV^{-1}$ interface state density and similar oxide traps. Lower interface density still should be obtained by employing different methods to further improve performance of the Ge-based MOSFETs.

Although the minority carrier generation rate has been studied here, through the use of temperature measurements, the extracted activation energy is not as expected, namely half of the band gap. A further explanation for this phenomenon should be explored to understand the minority carrier generation in these structures.

This work is based on MOS capacitors. Methods of interface passivation developed in this work should be employed in the fabrication of complete MOSFET to study the features of the device for future application.