Hafnium oxide-based dielectrics by atomic layer deposition

Thesis submitted in accordance with the requirements of
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Abstract

In 2007 there was an important change in the architecture of nanotransistors - the building blocks of modern logic and memory devices. This change was from utilising thermally grown silicon dioxide as a dielectric to so-called high-κ hafnium oxide dielectrics grown by atomic layer deposition. The first production logic devices of this era used a hafnium oxide dielectric layer deposited by thermal atomic layer deposition; using $HfCl_4$ and H_2O as the precursors. Present day fabrication makes use of hafnium oxide-based atomic-layer-deposited dielectric films. The latest nanotransistor devices utilise a third generation hafnium oxide-based dielectric material.

This thesis examines hafnium oxide-based thin film dielectric materials prepared by thermal atomic layer deposition on silicon substrates. Specifically the enhancement of the dielectric response of hafnium oxide by the addition of other elements is examined. Two ternary materials systems were deposited by thermal atomic layer deposition and analysed: titanium-hafnium oxide and cerium-hafnium oxide. Hafnium oxide films were deposited to be used as measurement benchmarks. Cerium oxide films were also deposited and analysed in their own right as potential dielectric layers.

The hafnium oxide and both ternary deposition experiments used $(MeCp)_2Hf(OMe)(Me)$ as the hafnium precursor. The titanium-hafnium oxide growth used $Ti(^iOPr)_4$ as a titanium source and the cerium oxide and cerium-hafnium oxide work utilised $Ce(mmp)_4$ as a cerium source. Post-deposition specimen sets consisted of an as-deposited sample, a sample spike-annealed in N_2 at 850 °C and a sample annealed for 30 minutes at 500 °C. These annealing regimes were performed to mimic typical gate-first and gate-last transistor processing steps. The compositions and thicknesses of the films were measured using medium energy ion scattering. The structure of the films was analysed by X-ray diffraction and Raman spectroscopy. Capacitance-voltage and current density-field measurements were taken from fabricated MOS capacitor specimens to assess the dielectric response of the films.

X-ray diffraction and Raman measurements showed that un-doped HfO_2 had monoclinic crystallinity as-deposited and after the two annealing regimes. The dielectric constant and leakage current density, 17 and 1.7×10^{-7} A/cm^2 at -1 MV/cm respectively, are

consistent with values reported in the literature for HfO_2 films.

The addition of titanium suppressed the crystallinity of the material resulting in amorphous films in compositions with $Ti_{0.3}Hf_{0.7}O_2$ titanium and above. The optimum electrical results were recorded for the titanium-hafnium oxide material in the composition $Ti_{0.5}Hf_{0.5}O_2$ which had a dielectric constant of 35 as-deposited and a leakage current density of 1.0×10^{-7} A/cm^2 at -1 MV/cm. This composition of film demonstrated similar values after the 500 °C/30 min anneal but both dielectric constant and leakage current density suffered after the 850 °C/spike anneal; 22 and 1.8 $\times10^{-6}$ A/cm^2 at -1 MV/cm respectively. Films with compositions of $Ti_{0.1}Hf_{0.9}O_2$ demonstrated much lower dielectric constant and higher leakage current density, especially after heat treatment.

The addition of cerium in a $Ce_{0.11}Hf_{0.89}O_2$ composition was found to suppress crystallinity as-deposited and then provoke a lattice-substitutional phase change to the metastable tetragonal/cubic phase after both types of heat treatment. This cerium-activated phase change resulted in a molar volume modulation compared to un-doped HfO_2. An increased dielectric constant compared to un-doped HfO_2 of 31 was recorded for the 500 °C/30 min anneal with the 850 °C/spike anneal resulting in a lower value of 21. Leakage current density was 1.3 $\times10^{-7}$ A/cm^2 and 3.2 $\times10^{-7}$ A/cm^2 at -1 MV/cm respectively for the same anneals.

Deposition with $Ce(mmp)_4$ and water was found to result in cubic crystalline films across a growth temperature range 150–350 °C. The frequency dependency of the dielectric properties was found to be influenced by the crystallite size which was governed by the deposition temperature. The highest dielectric constant, 42, was measured for the 150 °C growth temperature with C-V measurements performed at 1 MHz.

The two doped HfO_2-based materials systems studied have demonstrated potential as dielectric materials for use in future nanoelectronic devices.

Acknowledgements

Chapter 5 (data included in publication **i**):

- HfO_2 films deposited by M. Werner/S. Hindley
- Characterisation by P. J. King
- Heat treatments performed by M. Werner/P. J. King
- Electrical measurements performed by M. Werner/S. Mather

Chapter 6 (data included in publication **i**):

- Ti-HfO_2 films deposited by S. Hindley/P. J. King
- Characterisation by P. J. King
- TEM specimens prepared by P. J. King; measurements performed by S. Romani
- MEIS measurements performed by M. Werner/P. J. King
- Heat treatments performed by M. Werner/P. J. King
- Electrical measurements performed by M. Werner/P. J. King

Chapter 7 (data included in publications **ii**, **iii** and **iv**):

- CeO_2 films deposited by M. Werner/P. J. King;
- Ce-HfO_2 films deposited by P. J. King/S. Hindley
- Characterisation by P. J. King
- TEM specimens prepared by P. J. King; measurements performed by K. Dawson
- MEIS measurements performed by M. Werner/P. J. King
- Heat treatments performed by M. Werner/P. J. King
- Electrical measurements performed by M. Werner/P. J. King

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Peter J. King 2012

Contents

List of figures

List of tables

Acronyms and notation

ϵ_0	Permittivity of free space (8.854×10^{12} Fm^{-1})
κ; ϵ_r	Dielectric constant; relative permittivity (dimensionless)
^{i}OPr	Isopropanol or C_3H_8O ligand group
ALD	Atomic layer deposition
CMOS	Complementary metal oxide semiconductor
Cp	Cyclopentadienyl or C_5H_5 ligand group
E_C	Conduction band level (eV)
E_F	Fermi energy level (eV)
E_V	Valance band level (eV)
EOT	Equivalent oxide thickness (nm)
I_{off}	MOSFET off-state current (μA)
I_{on}	MOSFET on-state current (μA)
L_g	Gate length (nm)
Me	Methyl or CH_3 ligand group
MOCVD	Metallorganic chemical vapour deposition
MOSFET	Metal oxide semiconductor field-effect transistor
NMOS	'N-channel' MOS
PMOS	'P-channel' MOS
V_{DD}	MOSFET supply voltage (V)
V_{th}	MOSFET threshold voltage (V)

Publications

• Journal articles referred to in this thesis by bold roman numeral:

[**i**] M. Werner, **P. J. King**, S. Hindley, S. Romani, S. Mather, P. R. Chalker, P. A. Williams and J. A. van den Berg *Atomic layer deposition of Ti-HfO_2 dielectrics* J. Vac. Sci. Technol. A **31** 01A102 (2013)

[**ii**] H. C. Aspinall, J. Bacsa, A. C. Jones, J. S. Wrench, K. Black, P. R. Chalker, **P. J. King**, P. A. Marshall, M. Werner, H. O. Davies and R. Odedra *Ce(IV) Complexes with Donor-Functionalized Alkoxide Ligands: Improved Precursors for Chemical Vapor Deposition of CeO_2* Inorg. Chem. **50** 11644 (2011)

[**iii**] **P. J. King**, M Werner, P. R. Chalker, A. C. Jones, H. C. Aspinall, J. Basca, J. S. Wrench, K. Black, H. O. Davies and P. N. Heys *Effect of deposition temperature on the properties of CeO_2 films grown by atomic layer deposition* Thin Solid Films **519** 4192 (2011)

[**iv**] J. S. Wrench, K. Black, H. C. Aspinall, A. C. Jones, J. Bacsa, P. R. Chalker, **P. J. King**, M. Werner, H. O. Davies and P. N. Heys *MOCVD and ALD of CeO_2 Thin Films using a Novel Monomeric Ce(IV) Alkoxide Precursor* Chem. Vapor Depos. **15** 1 (2009)

• Material accepted for conference presentations (deposition and characterisation work from chapter 7):

[v] N. Sedghi, et al. *Cerium-Doped Hafnium Oxide on Silicon* accepted for poster presentation at IEEE Semiconductor Interface Specialists Conference, San Diego (December 2012).

- Other publications during Ph.D. time period:

[vi] P. R. Chalker, P. A. Marshall, **P. J. King**, K. Dawson, S. Romani, P. A. Williams, J. Ridealgh and M. J. Rosseinsky *Atomic layer deposition of germanium-doped zinc oxide films with tuneable ultraviolet emission* J. Mater. Chem. **22** 12824 (2012)

[vii] M. Ahmad, J. K. Luo, H. Purnawali, W. M. Huang, **P. J. King**, P. R. Chalker, M. Mireftab, J. J. Geng *Making shape memory polymers reprocessable and reusable by a simple chemical method* J. Mater. Chem. **22** 8192 (2012)

[viii] M. Ahmad, J. K. Luo, B. Xu, H. Purnawali, **P. J. King**, P. R. Chalker, Y. Q. Fu, W. M. Huang and M. Miraftab *Synthesis and Characterization of Polyurethane-Based Shape-Memory Polymers for Tailored T_g around Body Temperature for Medical Applications* Macromol. Chem. Phys. **212** 592 (2011)

[ix] K. Black, P. R. Chalker, A. C. Jones, **P. J. King**, J. L. Roberts and P. N. Heys *A New Method for the Growth of Zinc Oxide Nanowires by MOCVD using Oxygen-Donor Adducts of Dimethylzinc* Chem. Vapor Depos. **16** 106 (2009)

Chapter 1

Technological context

1.1 Introduction

The experimental work in this thesis focusses on potential improvements to hafnium-based dielectric materials; specifically in the context of dielectric layers in metal oxide semiconductor field-effect transistors (MOSFETs). The basic building block of modern logic circuits is the complementary MOSFET (CMOS) which utilises opposite pairs of MOSFETs. Central to the continued technological advancement of CMOS devices is the continued downscaling of MOSFETs and the issues associated with this downscaling when important materials property limits are reached. Figure 1.1 shows the reduction in CMOS technology node[1] in production transistors over the last ten years. With each technology step comes innovations in MOSFET design and materials which are briefly indicated in the figure. These innovations have often been vital in the continued miniaturisation of CMOS, frequently solving problems that seemed to signify the end of the technology. In 2007, when the MOSFET technology node had reached 45 nm, the CMOS fabrication industry moved to replace the incumbent dielectric layer, SiO_2, with a high-κ (higher permittivity in comparison to SiO_2) material: HfO_2 [1]. This step was taken as SiO_2, or SiON as was used in the late SiO-based transistors, could not be scaled any further without resulting in unacceptable levels of current leakage during device operation. Coupled with the necessary change in insulating material was a need to replace the previous gate electrode material, polycrystalline silicon, with a metal gate material.

[1] Technology node: minimum gate length utilised in transistor production; used as the main descriptor of each generation of MOSFET.

As well as changes made to device materials the dielectric layer substitution required a change in process technology and **atomic layer deposition** (ALD) was introduced as the deposition technique adopted by industry for dielectric layer growth [2]. Intel® have utilised ALD for dielectric film deposition from the 45 nm node in 2007 to the present day [3]. These materials and process changes represented a massive shift for the CMOS fabrication industry. Another gate length, 32 nm, was achieved with a second generation high-κ material in 2009 [4]. Recently Intel® reported a change in direction from planar MOSFET devices, to a new 'Trigate' geometry for the 22 nm gate length [5], which is now "in volume manufacturing". This represents a change from 'planar' MOSFET devices to ones that exploit three-dimensional transistor geometry as well as a third generation high-κ dielectric. Table 1.1 lists some technical data that accompany the MOSFET downscaling outlined in figure 1.1. As can be seen the technology node value is not necessarily the smallest dimension; the physical gate length (L_g) is usually

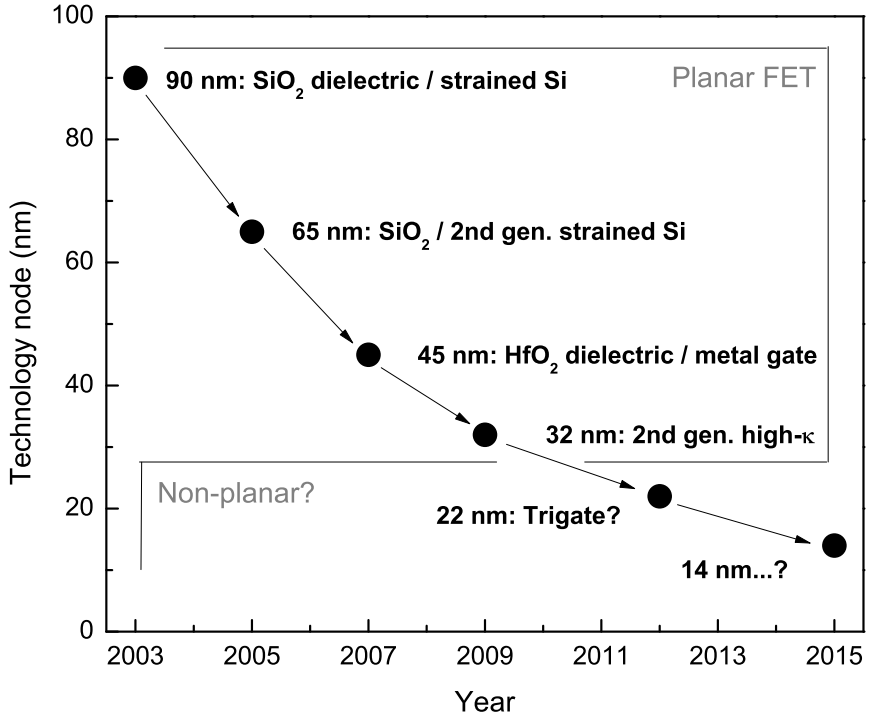

FIGURE 1.1: Progressive MOSFET technology nodes (minimum gate length) over the last ten years; specifically Intel®'s technology generations introduced bi-yearly.

smaller. Technology node values reflect the dimensions that can be produced by the current lithography technology, which is the method used to 'print' the nanocircuitry onto the substrate. Values in table 1.1 are split into relevance for high-performance (HP) and low standby power technology (LSPT). Effective oxide thickness (EOT) is the thickness of the gate dielectric material expressed as the equivalent thickness of SiO_2 that would exhibit the same permittivity as SiO_2. I_{on} and I_{off} are the on and off-state current of the device. V_{DD} is the supply voltage. What can be seen across the table is a trend in increasing I_{off} with each iteration of gate length. This has resulted in a serious power consumption issues - a high I_{off} means the circuit consumes a large amount of power in standby mode - and the reduction in the values for the 2012 technology node are a result of the introduction of the new device architecture at 22 nm. Other trends

TABLE 1.1: MOSFET technology nodes from 90 nm to 22 nm and related technical data. From [6], chapter 7.

Year of introduction	**2003**	**2005**	**2007**	**2009**	**2012**
Technology node (nm)	90	65	45	32	22
L_g (nm) (HP/LSTP)	37/65	26/45	22/37	16/25	13/20
EOT (nm) (HP/LSTP)	1.9/2.8	1.8/2.5	1.2/1.9	0.9/1.6	0.9/1.4
V_{DD} (V) (HP/LSTP)	1.2/1.2	1.1/1.1	1.0/1.1	1.0/1.0	0.9/0.9
I_{on} (μA/μm) (HP)	1100	1210	1500	1820	2200
I_{off} (μA/μm) (HP)	0.15	0.34	0.61	0.84	0.37
I_{on} (μA/μm) (LSTP)	440	465	540	540	540
I_{off} (μA/μm) (LSTP)	1E-5	1E-5	3E-5	3E-5	2E-5

in the data are the reduction of V_{DD} and the increase in I_{on} with each technology node. The reduction of V_{DD} is an ongoing way of decreasing the power consumption per chip while the increase in I_{on} is desirable to raise circuit speed.

This chapter introduces the device architectures discussed in this introduction, building up from the simpler metal-oxide-semiconductor (MOS) capacitor and p-n junction structures. After this the technical issues that relate to device scaling are discussed and an overview of the thesis is presented.

1.2 Device architecture and physics

1.2.1 Metal-oxide-semiconductor capacitor

A MOS capacitor is a two-terminal device which comprises a semiconductor substrate, an oxide insulating layer and a metal contact on top. The base of the substrate is coated in an Ohmic conducting layer such as aluminium (the dark strip at bottom of each MOS drawn in the schematics in figure 1.2). Here an 'Ohmic conductor' is one that has linear I-V characteristics under device measurement conditions. The substrate is commonly silicon, usually doped with either boron or phosphorous to produce p-type or n-type Si respectively. The purpose of the doping[2] is to introduce atoms that substitute for Si atoms in the crystal lattice that have one less or one more valance electron respectively than Si in the case of B or P. Si is a group IV element in the periodic table, B and P are examples of group III and group V elements respectively. These electrically-enhanced 'extrinsic' material states are opposed to intrinsic, or un-doped, semiconductors which have a carrier density based on intrinsic materials properties instead of being governed by the influence of dopants. An intrinsic semiconductor has an electrical conductivity derived from defects in the material or thermal excitations that promote carriers across the energy band gap between the valance and conduction bands. Intrinsic Si has an equal number of holes and electrons and the purpose of the dopant additions is to produce substrates which have a *majority* concentration of either holes (p-type) or electrons (n-type). In a lattice of covalently-bonded Si atoms one of the bonds around a substitutional B would have an electron missing whereas one of the bonds around a substitutional P would have an extra, loosely-bound electron. The missing electron site is an acceptor site or 'hole' which is considered a charge carrier in its own right with equal and opposite charge to an electron (the charge on an electron is -1.602×10^{-19} Coulombs). The oxide layer in a MOS capacitor is a dielectric oxide, described in more detail in chapter 2, which functions as an insulator. The interface between it and the substrate is essential to the functionality of the device. Figure 1.2 depicts the basic layout and shows MOS capacitors in four different operational states. The devices in the diagram comprise of

[2]The term 'doping' is used later on to describe the addition of substitutional atoms to a hafnium oxide matrix but the rationale for the two processes is very different. Doping in Si involves additions of $\sim10^{16}$ dopant atoms per cm^3. Si would generally have some 10^{22} atoms per cm^3 in its lattice meaning additions in the millionths of atomic percents.

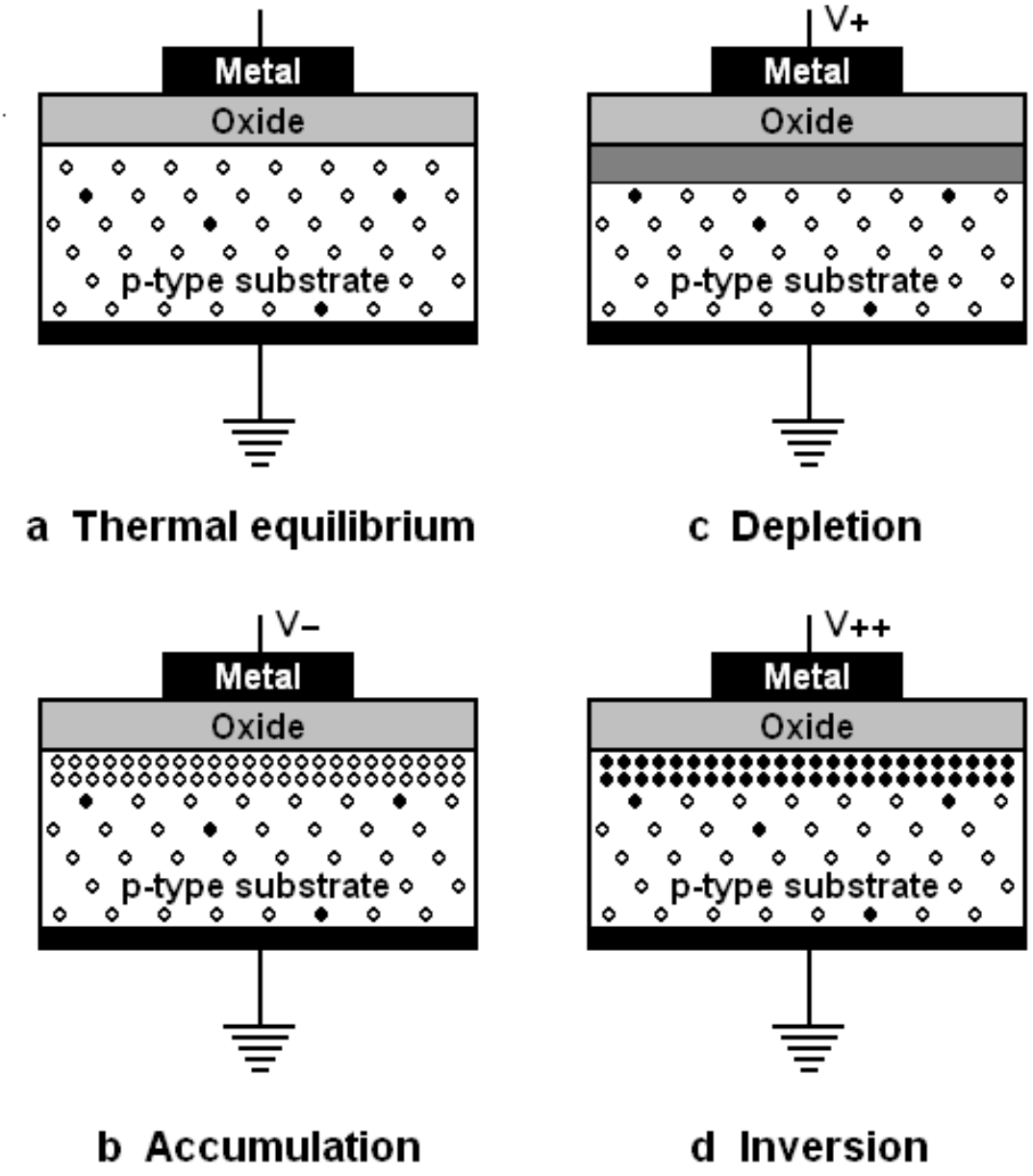

FIGURE 1.2: Schematic of p-type substrate MOS capacitor layout in various device modes depending on applied voltage. The open circles represent holes and the filled ones electrons (not to scale)

a p-type substrate (Si with B doping, majority of available carriers are holes), a SiO_2 dielectric oxide, a metal contact and metal Ohmic base contact. Without an applied voltage the device sits in **thermal equilibrium** (figure 1.2(a)). If a negative potential is applied to the metal contact and the majority carriers, holes in this case, accumulate at the Si/SiO_2 interface (figure 1.2**b**) the device is in a state of **accumulation**. If a small positive potential is applied to the metal contact the charge carriers in the section of substrate nearest the oxide/substrate interface are repelled, forming a region depleted of holes. This is called **depletion** (figure 1.2**c**), the grey band beneath the oxide represents the *depletion zone*. If the magnitude of the applied positive potential is increased the region depleted of carriers continues to grow beneath the oxide. Eventually it becomes energetically favourable for electrons present in the p-type substrate to congregate at the interface. This phenomenon of the minority carrier type amassing at the interface to that provided in excess by the type of doping is called **inversion** (figure 1.2**d**). The migration of electrons is not instantaneous and a quickly-pulsed applied potential can push the depletion level further than it should be allowed energetically. This state of extra depletion without inversion occurring is called deep depletion. In order to enhance this discussion of device modes of operation we now introduce the concept of the **Fermi energy level** and the electron band structure of a material. Figure 1.3**a**

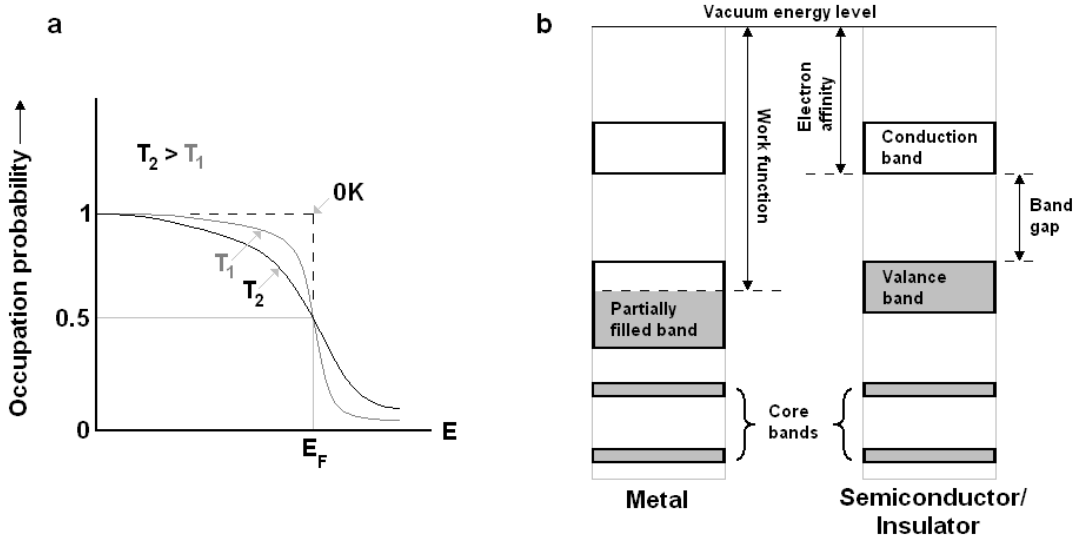

FIGURE 1.3: **a** Schematic curves for the Fermi function demonstrating the effects of temperature. **b** Electron occupation of the energy bands in a metal and semiconductor/insulator.

depicts a schematic of the Fermi function, f(E), for an electron. The function describes the Probability of an electron occupying a state at a given energy relative to the Fermi energy E_F. The function is temperature dependent as shown for two temperatures T_1 and T_2 where $T_2 > T_1$. At T=0 K the Fermi function becomes a step function with $f(E<E_F)=1$ and $f(E)>E_F=0$. At $E=E_F$, f(E)=0.5 independent of temperature. Figure 1.3**b** is a schematic drawing of the electron occupation of the energy bands in a metal and semiconductor or insulator. In a metal the highest occupied band is partially filled with electrons at 0 K. The fill level represents the Fermi level for a metal. Because of this the electrons can easily move into empty states and transport charge, making metals excellent conductors. The separation between the vacuum energy level[3] for electrons and the fill level of the partially filled band is called the *work function* of the metal. This is the minimum energy necessary to remove an electron from the metal surface. A semiconductor's valance band is completely filled and at 0 K its conduction band is completely empty. The band gap is the energy separation between valance and conduction band and the Fermi level is contained within the band gap. In a filled band, electrons cannot affect electrical conduction as they must move into an empty state to do so. This process involves promotion of electrons from valance to conduction band, and the width of the band gap has direct implications for the resistivity of the material. The separation between conduction band edge and vacuum energy level for electrons is the electron affinity.

Figure 1.4 demonstrates the effect on energy band structure for a MOS device in the four device states described in figure 1.2. With no applied voltage (figure 1.4**a**) the device is in thermal equilibrium with band-lines denoting the valance band energy for the substrate $\mathbf{E}_V$, the conduction band of the substrate $\mathbf{E}_C$, and the Fermi level $\mathbf{E}_F$ of the metal. The dashed E_F line shows the position of the equilibrium Fermi level in comparison to the changes in Fermi level brought about by applied voltage. In an un-doped, intrinsic Si substrate E_F would sit exactly between E_V and E_C defining the energy level at which the probability of occupation by an electron is 1/2. Dopant atoms in the lattice have the effect of creating energy levels within the band-gap. In p-type Si for example the effect is to shift the Fermi level closer to the valance band which

[3]Vacuum energy level: the energy of a free, stationary electron contained in a vacuum. Often used as an arbitrary reference point in energy band diagrams.

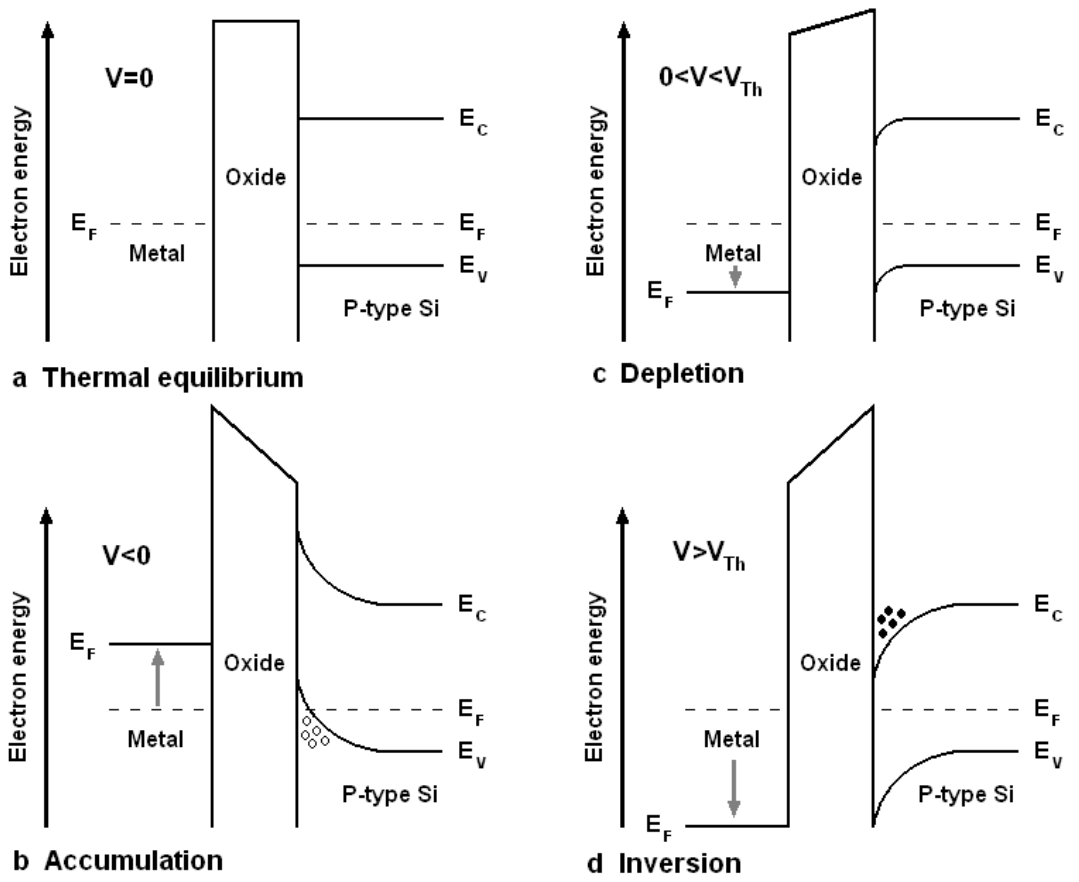

FIGURE 1.4: Schematic energy band structure for a MOS device in various device modes depending on applied voltage.

is why E_F is drawn closer to E_V in figure 1.4. This Fermi level position can change with applied potential in both the metal contact and substrate. Figure 1.4**a** depicts the band structure of a MOS device in thermal equilibrium with no applied voltage. In an ideal MOS device the work functions of the substrate and metal gate are equal with no applied voltage and the bands of the semiconductor substrate are flat. In a real device the charges trapped at the interface and in the oxide, as well as the difference between the gate/substrate work functions, shift the flatband voltage from this ideal. Sources of oxide charge are discussed in relation to electrical measurements in section 4.2.1. In **accumulation**, with an applied negative voltage (figure 1.4**b**) the majority charge carriers, holes, congregate at the oxide/substrate interface. The Fermi levels in the metal and substrate shift relative to each other causing band bending in the substrate E_V and E_C bands. At the substrate/oxide interface this results in the E_V band edge crossing

over the E_F level of the substrate leading to the hole population on the diagram. The state of **depletion** (figure 1.4**c**) comes from an applied voltage greater than zero but less than the *threshold voltage*, V_{th}, necessary for inversion. Band bending occurs due to the shift in relative Fermi levels but not to the extent necessary for minority charge carriers to group at the interface. In **inversion** (figure 1.4**d**) the applied voltage is of sufficient magnitude ($V>V_{th}$) for the substrate conduction band edge to bend to a level close to the energy of the Fermi level, resulting in the minority electron carrier population in the diagram and also in the MOS capacitors drawn in figure 1.2**d**.

1.2.2 P-n junction

Where materials doped p and n-type meet at an interface they form what is referred to as a *p-n junction*. At such a junction the interface divides a p-type region with a density of acceptor dopant atoms and an n-type region with a density of donor dopant atoms. The acceptor and dopant atoms are those resulting in the majority concentration of holes and electrons respectively. At the junction electrons and holes diffuse across the junction into the electron and hole-deficient regions respectively. Figure 1.5 depicts the band structure of **a** the p and n-type materials unconnected and **b** the p-n junction. These diffusing

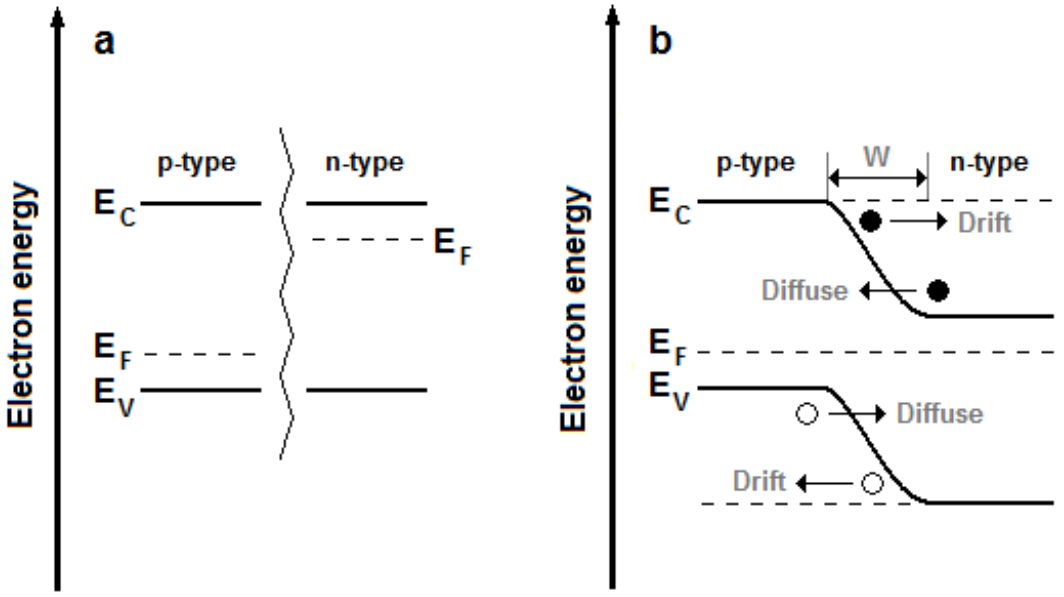

FIGURE 1.5: Schematic diagram of band structure of a p-n junction; 'w' denotes the width of the depletion region

charge carriers annihilate on contact with opposite charge carriers leaving the donor and acceptor ions near to the junction. This strip of opposing ions along each side of the junction forms the so-called depletion region at the junction. The areas of acceptor and donor ions create an electric field in the region which results in charge carrier drift in the opposite directions to the hole/electron diffusion. At thermal equilibrium a balance is reached between the diffusion and drift of both types of charge carrier and the Fermi level is constant across the interface (see figure 1.5**b**). P-n junctions are diodes in that they allow current flow in only one direction.

1.2.3 Metal oxide semiconductor field-effect transistor

The MOSFET is based on a doped Si substrate as before but has two regions of oppositely doped Si underneath the oxide that will define the channel that the charge carriers flow in in the device modes described in section 1.1.1. The metal contact described in the MOS diode is now termed the **gate** and is separated from the substrate by the oxide as before. The oppositely doped areas have contacts attached to them directly throughout the oxide which are called the **source** and **drain**. Figure 1.6 shows the basic layout of an n-channel (electrons as device-activating charge carriers) MOSFET (NMOS) in the four device modes described already for the MOS capacitor. If we consider that the substrate is p-type the device would utilise n-type source and drain regions. Figure 1.6**a** shows the MOSFET in accumulation. A negative voltage applied to the gate (V_{GS}-) draws the majority carriers, holes, from the p-type substrate to the channel below the dielectric oxide. As the source and drain are doped n-type they form p-n junctions at the source/channel and channel drain interfaces, meaning no current flows. Figure 1.6**b** shows the state of depletion for an NMOS with the holes being repelled from the channel area by the positive gate charge. A carrier-free depletion layer forms in the channel beneath the oxide layer and around the source and gate regions. If this positive voltage is high enough, above a threshold voltage V_{th}, an inversion layer forms in the channel below the dielectric layer; in our example this effectively joins up the source and drain with an n-type connecting channel (figure 1.6**c**). Although this connects the n-type source and drain with an n-type channel of carriers no current flow occurs until a drain bias is applied (V_{DS}). Figure 1.6**d** shows this bias applied and the direction of current

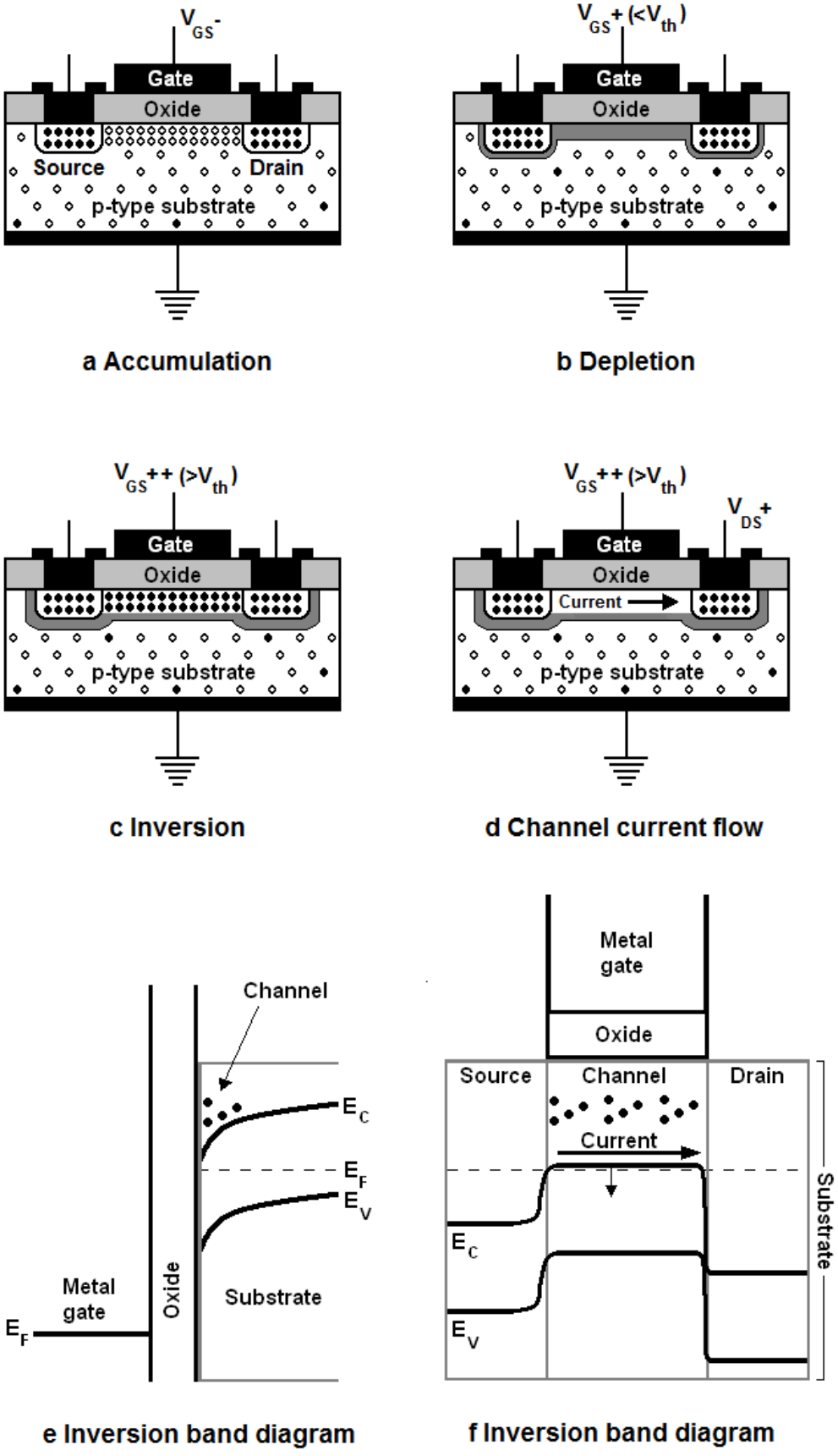

FIGURE 1.6: Schematic of n-channel MOSFET construction in **a** Accumulation, **b** Depletion, **c** Inversion and **d** Inversion with a drain bias applied. **e** and **f** show the band structure for the device in inversion from two different projections.

flow. This *enhancement-mode*[4] MOSFET can now function as a switch with a drain bias applied and V_{GS} alternated above and below V_{th}. Figure 1.6**e** show the energy band diagram for the device in inversion in the same projection used for band diagrams in the rest of this chapter; the source should be imagined towards the reader with the drain behind the page. With no applied gate voltage the source/channel and channel/drain interfaces form p-n junctions either side of the channel. Figure 1.6**f** depicts a rotated band diagram for the same projection as the device schematics on this page. An applied voltage brings the conduction band down close to the Fermi level, reducing the barrier formed by the p-n junctions and allowing current flow in the channel. Application of the drain bias distorts the band structure in the axis perpendicular to the page resulting in the lower energy band levels for the drain region. This is important because the application of V_{DS} injects current into both the doped regions, source and drain. As such a large enough V_{DS} must be applied to lower the bands of the drain region, reducing the number of carriers injected from the drain region to negligible and resulting in a net source-to-drain current.

A p-channel MOSFET (PMOS) is the same in construction and operation to the NMOS description but with a reversal of doping and hence activation voltage. In a PMOS device the substrate would be doped n-type with p-type source and drain regions. Application of a negative voltage over V_{th} for the device would produce an inversion layer of holes connecting the p-type source and drain. This description shows that the quality of interface between substrate and dielectric is important considering that it is this region in which charge flows in a MOSFET in inversion.

Figure 1.7 depicts a simplified series of schematic diagrams that describe the key process steps in MOSFET fabrication; specifically in a 'gate-first' type of fabrication process. Modern MOSFET fabrication is more complicated than this treatment but the objective is to contextualise the experimental work in this thesis using fabrication steps as examples. Step 1.7**1** is the starting substrate, p-type Si in this case. Step 1.7**2** is the deposition of the high-κ dielectric film via ALD. In steps 1.7**3** and 1.7**4** the oxide is selectively removed, in a process called lithography, to leave room for the source and

[4] A *depletion-mode* MOSFET has a channel doped the same way as the source and drain. Current flows with no applied voltage and the switching is done by 'pinching off' this current with the application of the relevant bias.

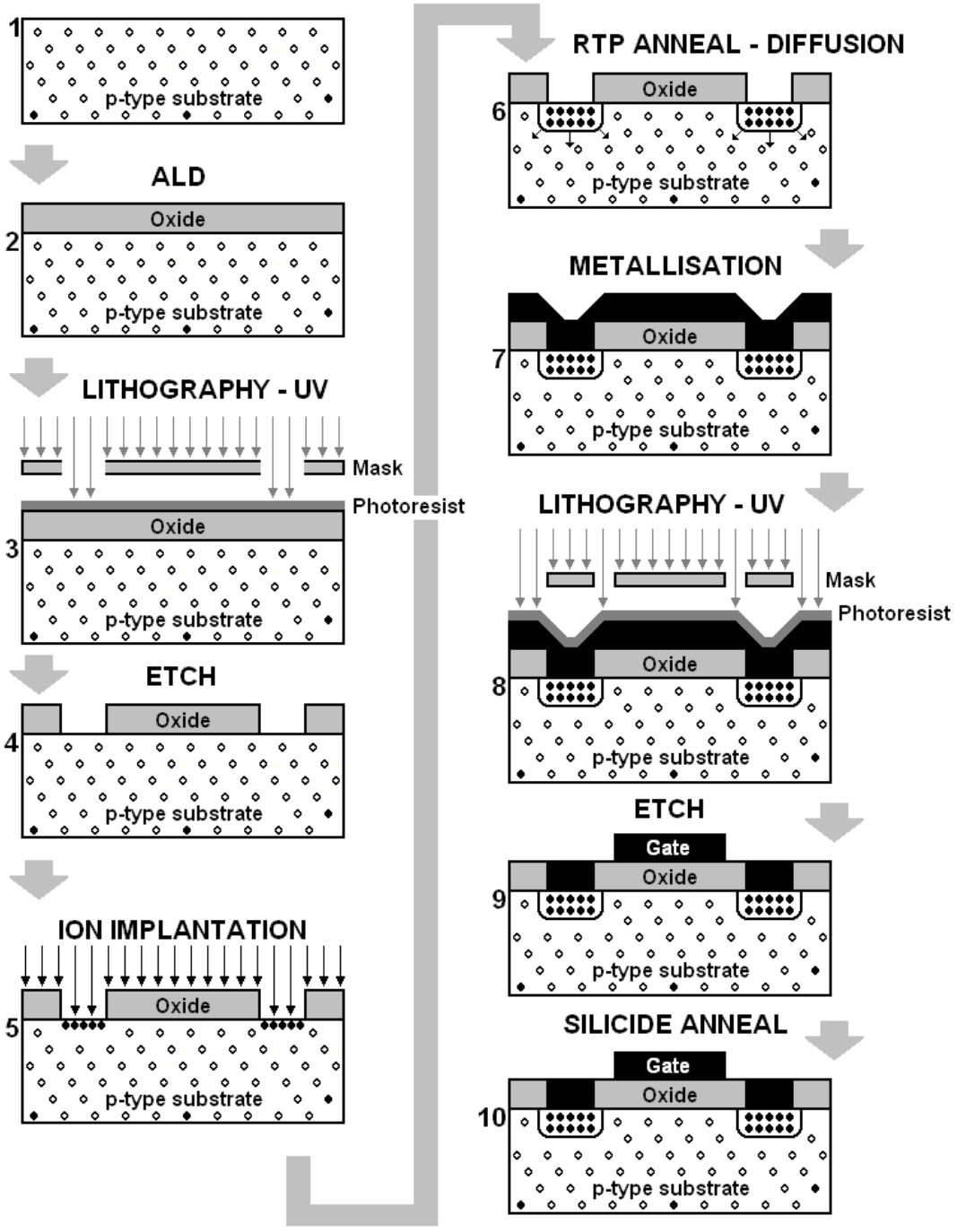

FIGURE 1.7: Simplified schematic diagrams of MOSFET fabrication steps in a 'gate-first' process.

drain areas. In order to do this the material is first coated in a 'photoresist' - a material sensitive to ultra-violet (UV) wavelength light. This is usually done by applying the photoresist as a liquid and spin-coating the substrate followed by a short low-temperature (∼90 °C) heat treatment to ensure a uniform, cured coating. The surface is then exposed selectively to UV light through a photomask (step 1.7**3**). The photomask is a quartz photoplate which contains the desired patterns of the bank of transistors to be formed. A 'positive' photoresist, like the one depicted here, contains a photo-sensitive stabilising agent that prevents its dissolution in an etchant. In the areas not shielded from the UV light by the mask this stabiliser breaks down. A subsequent application of an etchant solution, and removal of the photoresist material, leaves the desired patterns in the oxide (step 1.7**4**). Next, n-type 'wells' are formed by ion implantation which uses an electric field to accelerate ionised B, for example, into the substrate (step 1.7**5**). Ion implantation is used as it allows precision control over positioning and level of the doping. Following this is a high-temperature rapid thermal processing (RTP) step employed to diffuse the B atoms into the substrate in order to form the source and drain regions (step 1.7**6**). This RTP is typically ∼1000 °C and completed in ∼20 s. The RTP is said to 'activate' the doped regions while also restructuring the damaged material after ion bombardment. As a result of the diffusion extending in every direction from the implanted areas the source and drain overlap the gate edges slightly. As such an activation anneal is necessary for formation of the device regions it is an important parameter in device fabrication due to the effect it can have on materials already in place. In this work the key issue is whether the high-κ film will have to be subjected to this high-temperature RTP and what the ramifications are in terms of the engineered materials properties of the film. In the gate-first example of the diagram the next stage would be to apply a layer of conducting metal that will form the gate material and contacts to the doped source and drain regions (step 1.7**7**). This is then selectively removed in steps 1.7**8** and 1.7**9** in a similar lithography step to that described previously. Finally, step 1.7**10** is a 'silicide anneal' which is used to consolidate the interfaces between materials in the MOSFET structure formed. After this contacts can be made to the source, drain and gate regions and the basic MOSFET is complete. If a gate-last MOSFET fabrication strategy is employed the high-κ film is deposited after the RTP anneal and hence only has to be subjected to

the silicide anneal, which is lower temperature and lower temperature ramp-rate than the RTP. Chapter 3 contains a section on heat treatments employed in the experimental work and how the anneals performed are relevant to MOSFET fabrication steps. It is the annealing steps 1.7**6** and 1.7**10** that are emulated in the heat treatments performed before the electrical characterisation reported in the results chapters.

1.2.4 Complimentary metal-oxide-semiconductor

The complementary metal oxide semiconductor (**CMOS**) uses pairs of oppositely-doped MOSFETs - a PMOS device in conjunction with an NMOS device. Typically these devices are based on a p-type substrate with an n-type well in which the PMOS half of the device can be situated. The reason for basing such devices on p-type substrates is the higher mobility of electrons compared to holes. Not only is the functionality of n-channel devices superior as a result, devices built on n-type substrates produce more noise during measurements. An example of a combination device is the CMOS inverter which uses a tandem NMOS and PMOS as shown in figure 1.8**a**. When the input is negative the NMOS device shuts off and the PMOS device turns on, registering a positive output voltage. Application of a positive input voltage turns on the NMOS device and shuts off the PMOS resulting in a negative output voltage. In logic if a -V input is assigned to 0 and a +V input is assigned to 1 the device performs a logical inversion operation. Figures 1.8**b** and 1.8**c** show schematic circuit diagrams for a CMOS inverter with a positive and negative V_{in} respectively. With a positive applied voltage the NMOS device has current flow (1) where as the PMOS device is off (0). The current has a direct path to the ground and so the output is 0 (figure 1.8**b**). With a negative applied voltage the NMOS is off and the PMOS on. This means the V_{DD} contribution has a path to the V_{out} (figure 1.8**c**). CMOS circuits have the advantage of providing very low static power consumption as in each static device mode either the NMOS or PMOS are off and there is no current flow from V_{DD} directly to the ground. Due to this CMOS circuits consume much less power than other types of circuit.

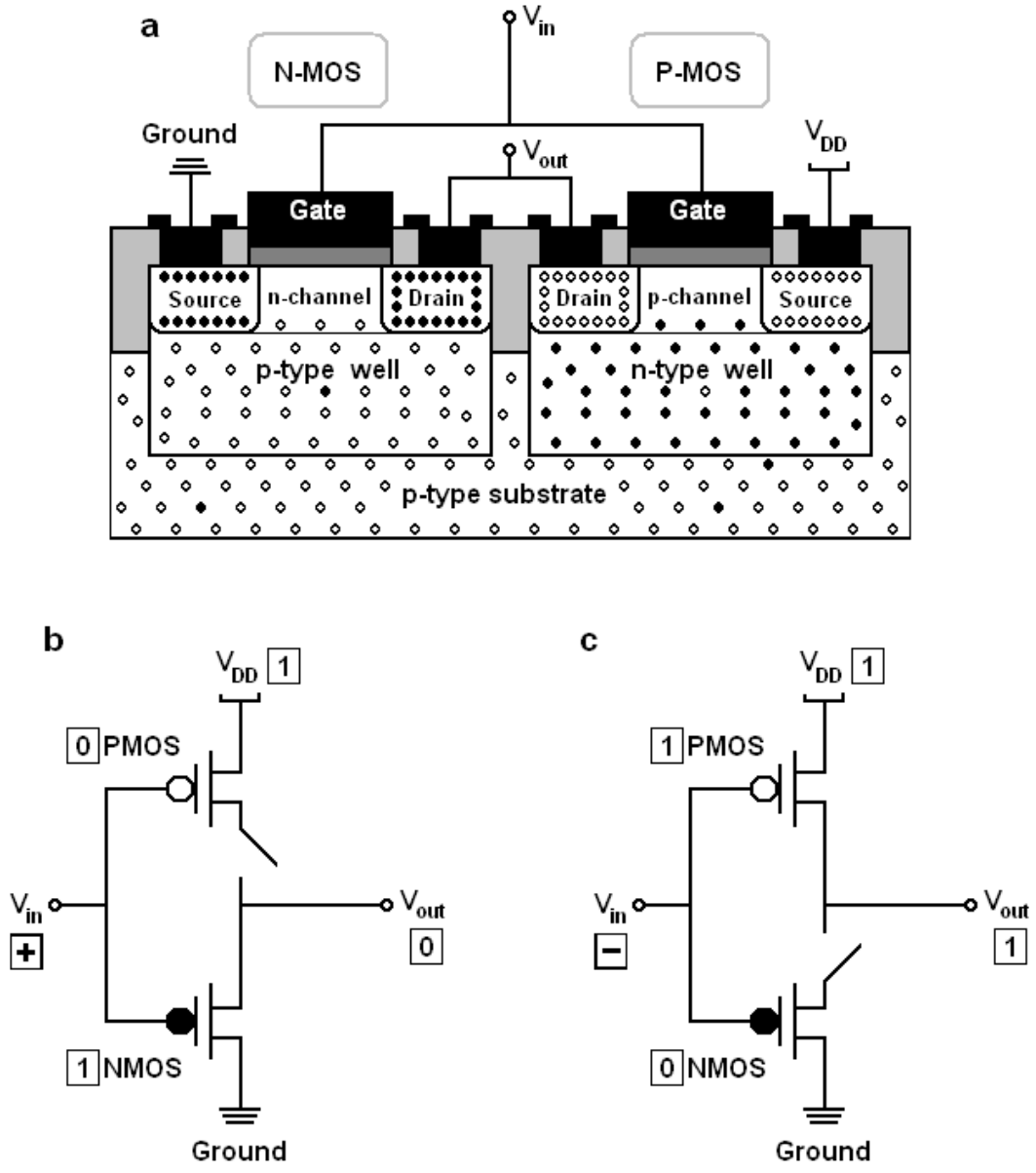

FIGURE 1.8: **a** Schematic of a CMOS transistor consisting of an NMOS and PMOS pair. **b** A CMOS inverter circuit with a positive V_{in}. **c** A CMOS inverter circuit with a negative V_{in}.

1.3 MOSFET evolution

1.3.1 Scaling

The technology nodes plotted in figure 1.1 refer to the minimum metal line widths involved in the fabrication of each successive technology generation in MOSFET miniaturisation. Each technology node results in the reduction in minimum metal line width to 70% of the previous line width; reducing the circuit area by half each time (i.e. $0.7\times0.7=0.49$: $\sim$50% reduction in area). Up to the 130 nm node this $0.7\times$ reduction was adhered to but from 90 nm onwards the scaling rate slowed as a consequence of trying to fully exploit Si-based technology down to its limits and of the materials switch in 2007 (see the shape of the plot in figure 1.1). This reduction in circuit area means nearly twice as many units can be manufactured per unit wafer area, which reduces the cost to produce MOSFET-based circuits significantly at each node (factoring in changes in tool technology etc.). As well as fitting more devices per unit area the MOSFET downscaling, and hence reduction in channel length, also has the effect of reducing the carrier transit time in the channel, increasing the speed at which the MOSFET switching can operate. Integrated circuit speed has increased by roughly 30% at each node [6]. Aggressive MOSFET scaling leads to a phenomenon known as the *short-channel effect*. A depletion layer forms around the oppositely doped sections of the substrate beneath the source and drain. A point in downscaling exists where the sum of the widths of these depletion layers equals the physical length of the channel. In this case the depletion layers merge and the functionality of the MOSFET ceases due to an applied voltage at the gate no longer controlling the current in the channel. Figure 1.9 demonstrates the short-channel effect using a schematic of a MOSFET being reduced in channel length. The grey transistor outline represents the initial long-channel MOSFET of channel length L_0. The grey arrows show the shrinking of the device into the MOSFET of channel length L drawn in black. Superimposed on the diagram are the conduction band curves for the long-channel and short-channel devices in grey and black respectively. If during MOSFET scaling only the channel length is changed with other dimensions constant a channel length is reached where the p-n junctions of the source/channel and the channel/drain overlap. This results in a conduction band profile like that drawn in black with

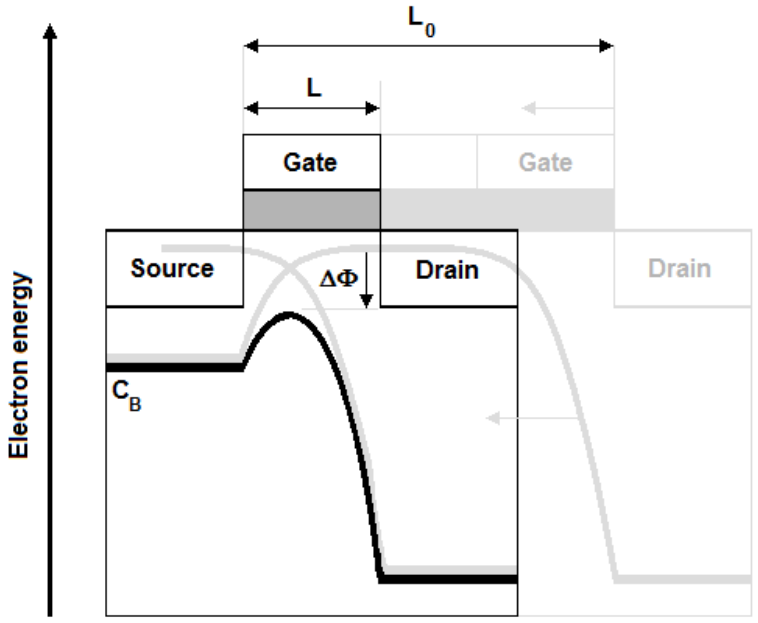

FIGURE 1.9: Schematic diagram showing the origin of short-channel effects in MOSFETs; the light grey capacitor structure and E_C curve represent a long-channel device of channel length L_0, with the black lines representing a short-channel device of channel length L. After [7].

a reduction in barrier height ($\Delta\Phi$). This conduction band reduction leads to a strong increase in current in the device. To combat this effect all transistor dimensions, and operating voltages, must be scaled together; the reductions plotted in figure 1.1 should be thought of as scaled dielectric oxide thickness and power supply voltage alongside the minimum metal line width.

The key issue with transistor miniaturisation, if the aspect ratios are kept constant to avoid short-channel effects, is that of **tunnelling**. There are a variety of tunnelling processes that result in electrons and holes negotiating the insulating layer in a MOS-type device but the most important one to highlight is quantum mechanical (QM) tunnelling (often referred to as 'direct tunnelling'). The wave function of a particle is a probability amplitude describing the particle's behaviour in space and time. **Direct tunnelling** involves charge carriers travelling through the insulating layer without residing in the insulator's conduction band. This occurs because the wave function of the charge carrier doesn't stop immediately at the insulator but decreases exponentially into the thickness of the layer at a rate dependent on the energy barrier height of the insulator. Even a

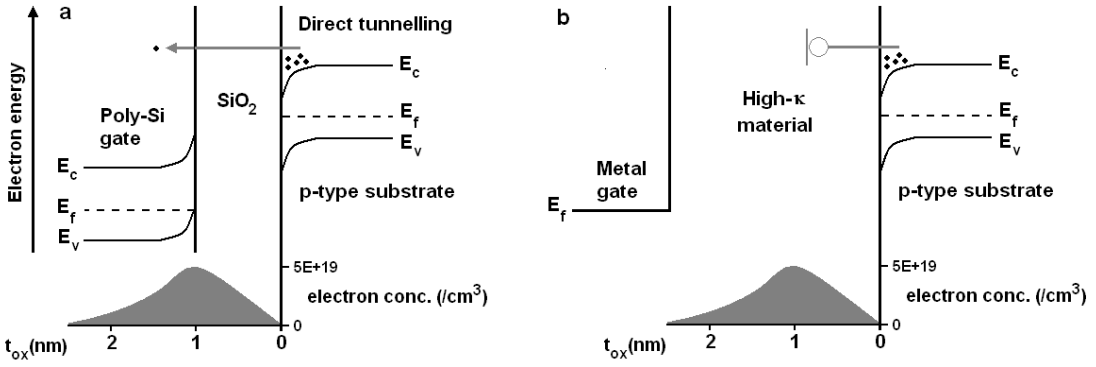

FIGURE 1.10: **a** Schematic diagram demonstrating direct tunnelling relative to a MOS band structure, **b** the effect of including a thicker high-κ material as a dielectric layer.

material like SiO_2, that has a wide band gap of $\sim$9 eV, can have a thickness at which statistically charge carriers would be expected to cross the gap. This phenomenon has been found to be independent of gate material, with a maximum in the electron concentration found to be at $\sim$1 nm into the dielectric layer [8]. Figure 1.10**a** depicts direct tunnelling through a 1 nm SiO_2 dielectric layer and figure 1.10**b** demonstrates preventing the effect by utilising a thicker high-κ layer. Figure 1.10 has a representation of the statistical electron concentration included at the bottom of each of the band diagrams from QM analysis [8]. The QM effects only matter when the oxide is downscaled to near the 1 nm thickness at which the maximum carrier concentration is found [9, 10]. One solution is to install a high-κ[5] layer in place of the SiO_2 which is thick enough to prevent unacceptable direct tunnelling levels while maintaining the same capacitance density. At a few nm of dielectric thickness the QM effects are minimised and the Fowler-Nordheim (F-N) tunnelling mechanism is prominent.

F-N tunnelling occurs due to the change in shape of the band profile of the dielectric layer in a MOS with applied voltage. In figure 1.4**d** for example the triangular shape at the top of the oxides energy profile is a result of the band bending caused by the applied voltages effect on the relative Fermi levels. F-N tunnelling is a special case of direct tunnelling as it still involves a statistical distribution of charge carriers across the oxide energy barrier that have not interacted with the conduction band of the oxide material. In the F-N tunnelling case the carriers are only travelling through part of the

[5]high-κ means high permittivity in a material and 'κ' or 'dielectric constant' values are quoted for permittivity measurements made on dielectric materials.

energy barrier and so this type of tunnelling mechanism can affect thicker films than direct tunnelling; below a certain thickness the direct tunnelling mechanism takes over.

The scaling of transistors using SiON as a gate dielectric was limited to transistor nodes above 65 nm. Below this node size the SiON gate oxide thickness was ∼1 nm and leakage current densities were becoming unacceptably large. Work ensued to try and find a balance between κ and thickness in new dielectric oxide layers with the aim of continuing the downscaling of the nanotransistor building blocks of MOSFET-based devices. The term 'equivalent oxide thickness' (EOT) is often used to describe how a particular material's permittivity compares to SiO_2 (κ∼3.9) which has filled the role of micro/nanotransistor dielectric for many years. EOT is defined:

$$EOT = (3.9/\kappa)t \tag{1.1}$$

where 3.9 is the permittivity of SiO_2 and κ and t are the permittivity and thickness respectively of the particular material system. For example a particular material that exhibits a permittivity of 39 could be 10 times as thick as its silicon oxide counterpart and provide the same capacitance density. An acceptable level of current leakage is one of several attributes that a would-be SiO_2 replacement must deliver; indeed the dominance of SiO_2 in this area is more to do with its excellence as an all-round functional material than just its dielectric properties - its thermal stability on, and adherence to, a silicon substrate as well as its equiaxial growth on silicon as a result of simple heat treatment are as important. Equally the leakage properties of the MOSFET stack rely on the bandgap of the dielectric layer and specifically the band off-set in comparison to the substrate. Some progress was achieved by using SiON as the gate dielectric and by utilising opposing strains on the p and n-type sectors of the transistors but to continue scaling a more radical switch was necessary. For metal gate/ high-κ high-performance chip technology, necessary EOTs were quoted as: 45 nm node=10 $\mathring{A}$ 32 nm node=8 $\mathring{A}$ 22 nm node=6 $\mathring{A}$ [11]. Although these are equivalent oxide thicknesses they require physical thickness values in the thickness regimes in which SiO_2 fails to deliver as an effective gate oxide.

With the replacement of SiO_2/SiON as a dielectric oxide material in technologies like CMOS the industry has switched from scaling SiO-dielectric-based devices to the

equivalent scaling of devices using a replacement material. HfO_2 became the next gate dielectric material due to its thermal stability on silicon and similar lattice parameter - the distance between neighbouring atoms in the repeating crystal lattice. This property is important as matching lattice parameters between interfaced materials results in a higher-quality interface; the interface being the region in which charge flows in a MOSFET device. HfO_2 also has a superior dielectric constant compared to SiO_2 making thicker films possible with the same capacitance density in the equivalence relation described in equation 1.1. While some improvements remain in the optimisation of HfO_2 films through tighter control over film stoichiometry, improving the quality of the film/-substrate interface and ironing out thickness variations [12] this thesis work involves permittivity enhancements to hafnia-based films via dopant additions.

1.3.2 Fabrication technologies

The last of the SiO-dielectric-based transistors utilised SiON as the dielectric material. In fabrication SiO_2 was grown thermally in dry O_2 followed by a plasma nitration and anneal. This processing produced SiON with 10–15% N and a dielectric constant of ∼4.8 [13]. Use of SiON helped to continue transistor scaling for another technology node but the gate oxide was ∼1.1 nm; beyond this direct tunnelling would halt further progress. The industry had no choice but to move away from thermal SiO-based dielectric layer production and towards utilising a deposition technology. ALD was utilised during this industry shift as the deposition technique due to its precise control of thickness and composition [2]. In ALD, precursors that provide each kind of atom are transported separately into the reaction chamber where they come into contact with the substrate. In a 'binary' metal oxide deposition process the precursor that provides the metal atom is fed into the chamber in a dose that is designed to saturate the acceptor sites on the substrate and leave a 'monolayer' of the desired atom on the surface. The chemistry of the precursor is designed to leave a surface that can then have an oxidant react with it before any excess precursor material is cleared from the chamber in an inert gas purge. The other half of the binary oxide growth would involve exposing the surface to an oxidant like H_2O or O_3. This reaction step is followed by another inert gas purge and then the steps are repeated to build up a film in alternate monolayers of metal and oxygen.

More components can be included in a film's growth by simply including extra steps that involve other precursors coming into contact with the substrate. A more detailed description of ALD is included in chapter 3.

Photolithography is the technique used to pattern banks of nanotransistors during fabrication. As introduced schematically in figure 1.7 the method involves selective removal of material leaving behind the desired circuit patterns. As MOSFETs have reduced in size another major obstacle was the minimum possible feature size that could be produced using photolithography. As the process uses light it is limited to the lowest functional wavelength of light that can be produced. Modern lithography uses low-ultra-violet-wavelength light in the order of 325 nm. The minimum feature size that could be defined was a function of the working distance between the mask (g) and the photoresist and this wavelength (λ) - feature size $\approx\sqrt{\lambda g}$. For a working distance of 500 nm and a wavelength of 325 nm this would still limit the minimum feature size to $\sim$403 nm. Wavelengths of lithography sources were improved into the deep ultra-violet wavelength range with the ArF excimer source that produces an incident line at 193 nm. From here the resolution of the technique was improved by introducing a system of optics between mask and resist that allowed much smaller features to be printed to the wafer: feature size$\approx\lambda$/NA, where NA is the numerical aperture of the optics. As well as switching to ALD high-κ/metal gate for the 45 nm node, lithography had to be adapted - the introduction of immersion lithography (IL). IL works by introducing a fluid into the gap between the optics' lens and photoresist. The fluid medium is chosen to have a refractive index which further improves the NA of the lithography set up compared to having an air-filled working distance between lens and photoresist. For the 22 nm technology node production extreme ultra-violet lithography has been developed which uses a wavelength of 13.5 nm from a laser produced plasma source.

1.4 Thesis overview

Chapter 2 will cover **Dielectric theory** and the literature on attempts to improve on hafnium oxide as a functional dielectric. Chapter 3, **Experimental: Growth and processing**, and Chapter 4, **Experimental: Analytical techniques**, will describe the experimental methods used in film deposition and film characterisation respectively. Chapter 5, **Results: HfO_2**, presents the deposition of and measurements made on HfO_2 thin films. Chapters 6 and 7, **Results: Ti-HfO_2** and **Results: Ce-HfO_2**, will introduce the cerium-doped and titanium-doped hafnium oxide systems. Chapter 8 will draw some **Conclusions** from the experimental work and subsequent analysis and discussion in the results chapters.

Chapter 2

Dielectric materials

2.1 Dielectric materials theory

2.1.1 General dielectric theory

A **dielectric** is an electrically insulating material that is permeable to, i.e. can be polarised by, an applied electric field and therefore has the ability to store charge when an external electric field is applied. Dielectrics don't conduct via the transport of charge carriers through the material but by the slight realignments of charges from their equilibrium positions to give the material a net charge. This makes them relatively poor conductors compared to materials with a dissociated sea of charge carriers like electrons in metals. A measure of the susceptibility, χ_e, of a material to polarisation in an electric field is given by

$$P = \epsilon_0 \chi_e E \tag{2.1}$$

where E is the applied electric field in V/m^2, ϵ_0 is the permittivity of free space (8.854×10^{12} Fm^{-1}) and P is the induced dielectric polarisation density. As F converts to C/V the units of P turn out to be C/m^2. In an isotropic material the polarisation is proportional to the applied field and aligned with the axis along which E is applied, although in an anisotropic material they need not necessarily be aligned along the same direction. The susceptibility is a dimensionless, material-dependent property that is related to relative permittivity, ϵ_r, by

$$\chi_e = \epsilon_r - 1 \tag{2.2}$$

ϵ_r is interchangeable with 'dielectric constant' and 'κ' and is also a dimensionless property. κ is independent of the strength of E for fields below a certain critical field at which carrier injection into the material becomes an important factor. Dielectric polarisation can be thought of as microscopic electrostatic strain stored in the material as a result of the applied electrostatic stress. As this physical response to the applied field involves masses in the material undergoing movement, acceleration and deceleration, then polarisation must have a time associated with it. Accordingly the frequency of an applied alternating field can have an effect on the polarisation which is treated as a complex function of the angular frequency of the applied field, ω, by

$$\hat{\epsilon}(\omega) = \dot{\epsilon}(\omega) + i\ddot{\epsilon}(\omega) \tag{2.3}$$

where i is $\sqrt{-1}$. Equation 2.3 separates the complex dielectric function into its real, $\dot{\epsilon}$, and imaginary, $\ddot{\epsilon}$, parts. $\dot{\epsilon}$ is related to the stored energy within the material and $\ddot{\epsilon}$ is related to the dissipation of energy within the material both relative to the applied electric field. A material may have several dielectric mechanisms that contribute to its overall κ value. Figure 2.1 shows the position on a frequency scale of dielectric mechanisms and their contributions to $\dot{\epsilon}$, and $\ddot{\epsilon}$. Highlighted on the figure are the frequencies at which space charge, dipolar, ionic and electronic mechanisms have an influence on dielectric response. Moving along the frequency axis of the figure from slower to faster frequency on the $\dot{\epsilon}$ trace it can be noted that each mechanism has a characteristic cutoff frequency at which it drops out in terms of the magnitude of stored energy. Correspondingly the cutoff frequencies also have a peak in the dielectric loss curve, the $\ddot{\epsilon}$ trace, which are shown as absorption bands in figure 2.1. The x-axis positions of each mechanism relate to the relaxation frequency, in the case of space charge and dipoles, or resonant frequency, in the case of ions and electrons, at which each type of dielectric response is at its maximum in $\dot{\epsilon}$ and the corresponding loss response shows a maximum in $\ddot{\epsilon}$. The magnitudes and frequencies of these effects are material specific. **Dielectric relaxation** refers to the time delay between application of an electric field and polarisation response in the material which affects the space charge and dipolar polarisation mechanisms. **Space charge** is a dielectric mechanism relating to spacial inhomogenities of carrier charge densities in a material. Such regions can result from a drift of mobile ions or electrons

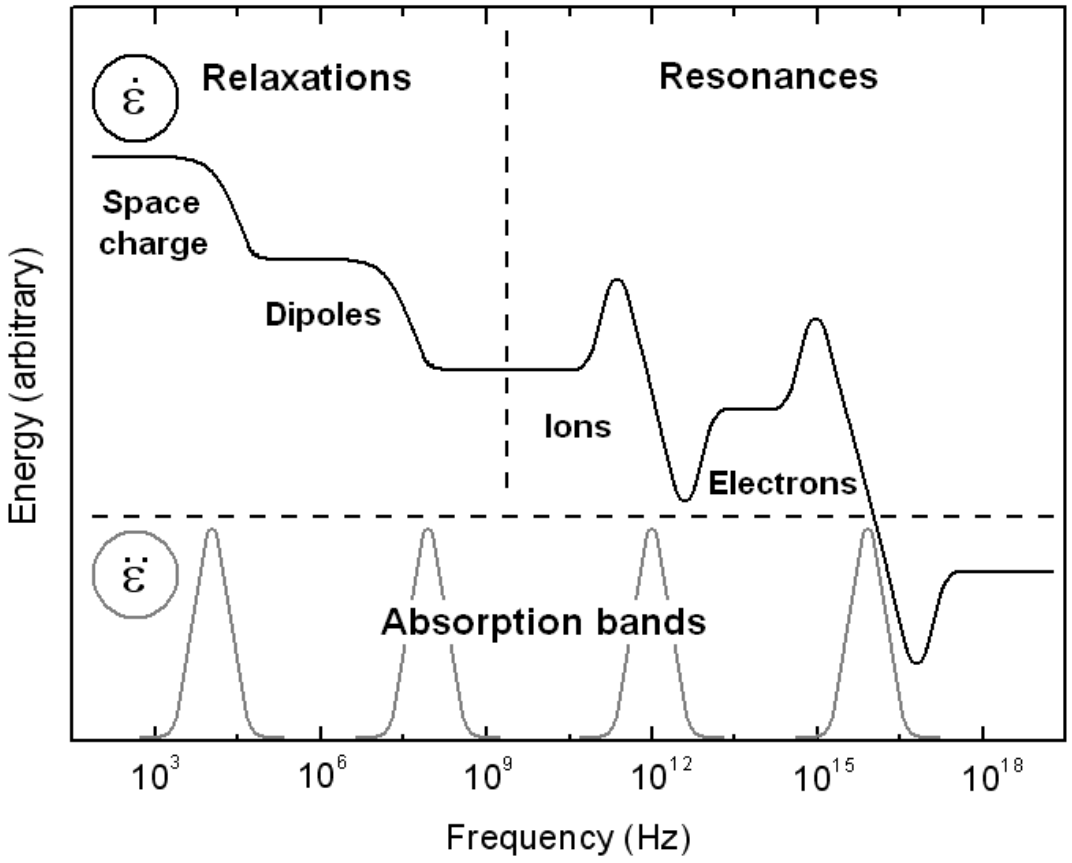

FIGURE 2.1: Complex dielectric response across the frequency range. The space charge, dipolar, ionic and electronic dielectric mechanism frequency positions are indicated. After [7].

which are confined to interfaces or discontinuities like grain boundaries in polycrystalline materials. **Dipole** contributions, or orientation polarisation, concern the alignment of permanent dipoles in a material. At ambient temperatures dipoles are usually randomly ordered in a material and orientation polarisation has strong temperature dependance - its dependance on temperature is often the only way to separate the two relaxation effects which can overlap in frequency response. These permanent dipole moments experience a torque in an applied field which orientates them with the field direction and produces a net polarisation. In the infrared frequency region ($\sim 10^{12}$–10^{13} Hz) is the **Ionic** resonance mechanism relating to the resonance of ionic lattices in the material. This can be thought of as an induced asymmetry in the electron field of bonded atoms in a lattice. Finally at $\sim 10^{15}$ Hz is the effect from the **electronic** polarisation resonance - the effect in an atom of the displacement of electrons with respect to the atomic nuclei.

The total dielectric polarisability of a material is a sum of these four contributions.

2.1.2 Dielectric enhancement of HfO_2 via doping

HfO_2 has appreciable dielectric properties itself with relative permittivity ∼20 for the monoclinic polymorph which is the crystal structure developed during common deposition/heat treatment regimes. As well as its κ value HfO_2 forms a thermally stable oxide layer on silicon, has a similar enough lattice parameter to silicon to provide a quality interface with the substrate and has an acceptable leakage current density [14]. A great deal of published work has looked at permittivity enhancements provoked by structural alterations in the material; what follows is a discussion on permittivity enhancements in thin film hafnia systems and the effects of dopant additions that introduce a change in dielectric response in the host material.

It might be expected that the dielectric behaviour of a ternary oxide might approximate to an average of the two constituent oxides. In many systems this approximation is close to the values seen for ternary dielectric materials but it depends on the specific mechanism(s) that the two constituents and the combination derive their dielectric response from. An addition of low levels of a dopant material can provoke phase changes in the host material and might help stabilise a phase with a higher dielectric constant than the equilibrium phase of the host. Excessive inclusion of an addition with a lower κ will eventually register as a reduction in the overall dielectric constant. There is frequently a dielectric peak recorded for an optimum addition level though the reasons for this behaviour can depend on the dielectric mechanisms in operation. A useful way of imagining the effects of morphological change on a system's dielectric response is to employ a simple version of the Clausius-Mossotti relation:

$$\frac{\kappa - 1}{\kappa + 2} = \frac{4\pi}{3}\frac{\alpha_m}{V_m} \tag{2.4}$$

Equation 2.4 demonstrates the reliance of the relative permittivity, κ, on both the molar polarisability (α_m) and the molar volume (V_m) of the system. In terms of polarisability materials can have permanent, electronic and ionic contributions, though dielectrics by definition are assumed not to have permanent polarisation. In simple ionic systems in an equilibrium state the ionic contribution to polarisation, α_{ion}, can be demonstrated

in the relation:

$$\alpha_{ion} = \frac{(Z^*e)^2}{M^*\omega_0^2} \tag{2.5}$$

where Z^*e is the effective charge and M^* is the reduced mass of a two-ion system. $M^*\omega_0^2$ is known as the force constant of the system and materials with unstable valence or a lighter atomic mass would derive their α_m value, and hence κ value, from this relationship. CeO_2 is an example of a system of relatively unstable valence and TiO_2 is an example of a system with both these attributes. A key consideration here is that alterations to the temperature that a material is processed at could have effects on both the molar volume and the polarisability. The molar volume[1] is related to the phases present and hence the thermally activated diffusion of atomic material during deposition/heat treatment. Intuitively it makes sense that if a material has ionic and electronic contributions to its dielectric response then increasing the density, or decreasing the molar volume, might maximise these contributions. The molecular polarisability is a function of the atoms' short range bonding structure and hence can also be strongly dependent on processing conditions [15]. Equation 2.4 and equation 2.5 help imagine a way to tailor the dielectric properties of a matrix material when considering the implication of each individual addition and their contribution to the system's overall dielectric response. Figure 2.2 demonstrates schematically the effects of a selection of dopant additions to hafnia and to which mechanism the change is attributed. For example, experimental [17] and 1st-principles computational [18] studies note the same increase in HfO_2 host κ value for small additions of Si. From the diagram SiO_2 acts as a crystalliser stabilising the non-equilibrium tetragonal phase and also as a molar volume modulator in its contribution to the higher-κ values measured. Silicon is an example of an atom that, included in the right proportions, can substitute for hafnium atoms in the lattice of the material. Above an optimum level the lower-κ silicon drags the overall dielectric constant down. Another plus to silicon is its +4 oxidation state; matching the host material's metal oxidation state goes some way to ensure electrical neutrality in the film and prevents the formation of oxygen vacancies to neutralise the overall film charge. In the results chapters of this thesis the two additions studied are two +4 atoms for this reason.

[1] A molar volume increase means a decrease in density of the material and vice versa.

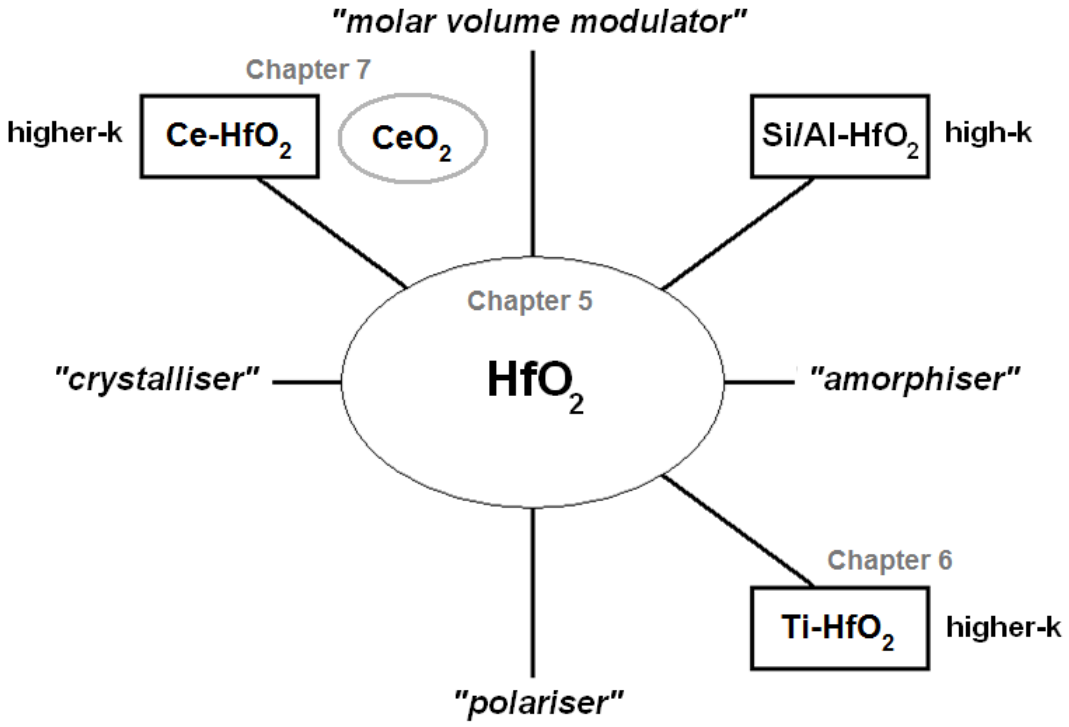

FIGURE 2.2: Effect of dopant additions to a hafnium oxide matrix by specific mechanism of dielectric alteration adapted from [16].

2.1.3 Metastable phase retention in HfO_2

As demonstrated later in this chapter a multitude of doping additions have been included in a HfO_2-based material and several have been found to stabilise metastable crystalline phases. There is some pattern to the successful stabilisers: Ce, Dy, Er and Gd are all lanthanides; Zr is a so-called chemical twin with Hf; finally Ba, Sr and Y surround Hf in the periodic table. This isn't a precise grouping of dopants, and other subtle factors have to be taken into consideration, but considering dopant additions in this way helps to explain the solid solution phase changes. First-principles computational results by Chen et al. [19] indicate that Y doping in a HfO_2 lattice provides better stability of the cubic phase by decreasing the energy difference between the material supporting the monoclinic and cubic phases. The addition was also found to reduce the transition pressure between phases compared to the undoped material. The computational work by Lee et al. [20] develops a discussion of 'type I' and 'type II' dopants in a HfO_2 matrix. The paper discusses addition elements in the context of their ionic radii compared to the ionic radius of hafnium. A general trend was noted in that the smaller ionic radius type

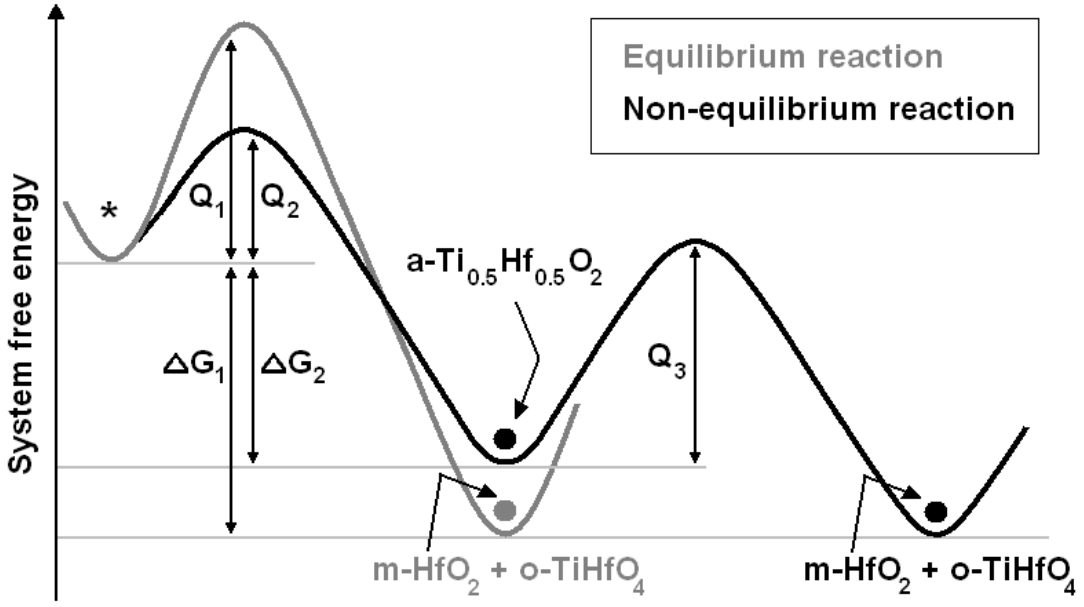

FIGURE 2.3: Schematic diagram of the energy paths for equilibrium and non-equilibrium phase changes in a $Ti_{0.5}Hf_{0.5}O_2$ thin film solid solution.

I additions (Si, Ge, Sn, P, Al and Ti in the paper) energetically favoured the tetragonal form of metastable HfO_2 while the relatively larger ionic radius type II additions (Y, Gd and Sc) favoured the cubic phase. The following discussion in the paper related these discoveries to the difference in bond lengths between an addition's oxide and the bonds it would have to form as part of a distorted HfO_2 lattice. From this treatment Ce, one of the dopants looked at in this thesis, would be expected to be a type II addition and so forming a metastable cubic phase would be expected.

Additionally the kinetics of nucleation have to be considered in a discussion on metastable phase change/retention, especially where an amorphous phase is retained making the reaction mechanism less transparent. Figure 2.3 shows a schematic diagram of the equilibrium and non-equilibrium reaction paths for a $TiHfO_4$ alloy - adapted from [21] to be relevant for a discussion of the materials systems examined in chapter 6. The diagram represents the post-deposition annealing of a $Ti_{0.5}Hf_{0.5}O_2$ ALD film. The Q maxima in the curves represent energy barriers to nucleation of a new phase while the ΔG values are free energy gains from each reaction. The asterisk is the reaction start-point while the dots represent potential phases formed in the reaction. For a 50:50 TiO_2:HfO_2 alloy the expected equilibrium phases are orthorhombic $TiHfO_4$ with HfO_2.

The non-equilibrium phase depicted is an amorphous $TiHfO_4$. The grey curve follows the equilibrium reaction with an energy barrier Q1 to overcome before forming the equilibrium products with a net energy gain ΔG1. The energy change ΔG2 is less than ΔG1 by definition as the latter is the favoured phase energetically. The energy barrier Q1 is greater than Q2 as a comparatively higher nucleation rate would be expected for the equilibrium phase formation. Following the black non-equilibrium reaction path the curve has a second energy barrier, Q3, preventing the reaction continuing on to form the equilibrium phases. This barrier would have to be as high or higher than Q2 to prevent the reaction continuing to form the equilibrium phases.

One of the conditions for amorphous phase nucleation in solid solutions is that one of the elements is a fast diffuser compared to the other and the negative heat of mixing of the amorphous alloy formed [22, 23]. A difference in relative diffusion speed between two atomic species is often correlated with a difference in atomic radius between the two; the smaller atom being the fast diffuser. Table 2.1 presents ionic radii for relevant

TABLE 2.1: Effective ionic radii for Hf, O and relevant addition species. Effective ionic radii are calculated from r^3 vs V plots. From [24].

Ion	**Electron config.**	**Coord.**	**Crystal radius**	**Effective ionic radius**
Hf^{4+}	$4f^{14}$	VIII	0.97	0.83
O^{2-}	$2p^6$	IV	1.24	1.38
Ce^{3+}	$6s^1$	VIII	1.283	1.143
Ce^{4+}	$5p^6$	VIII	1.11	0.97
Er^{3+}	$4f^{11}$	VIII	1.144	1.004
Gd^{3+}	$4f^7$	VIII	1.193	1.053
Ti^{4+}	$3p^6$	VIII	0.88	0.74

species taken from the 'revised effective ionic radii' work by Shannon [24]. Depending which values for atomic/ionic radii are used in a treatment on lattice substitutions the numbers can vary significantly, but the proportions between the species we consider here are always within a few percent between the quoted sets of values. In table 2.1 the first two rows are the data for the matrix material HfO_2, where Hf has VIII coordination and O has IV coordination. The four ions in the middle block are ones that have been shown to substitute for Hf in the lattice to cause the retention of cubic HfO_2 - we will assume cubic rather than tetragonal, despite the structural ambiguities, due to the average κ value quoted. What can be noted is that the Ce^{4+} ion offers a closer match to the Hf^{4+}

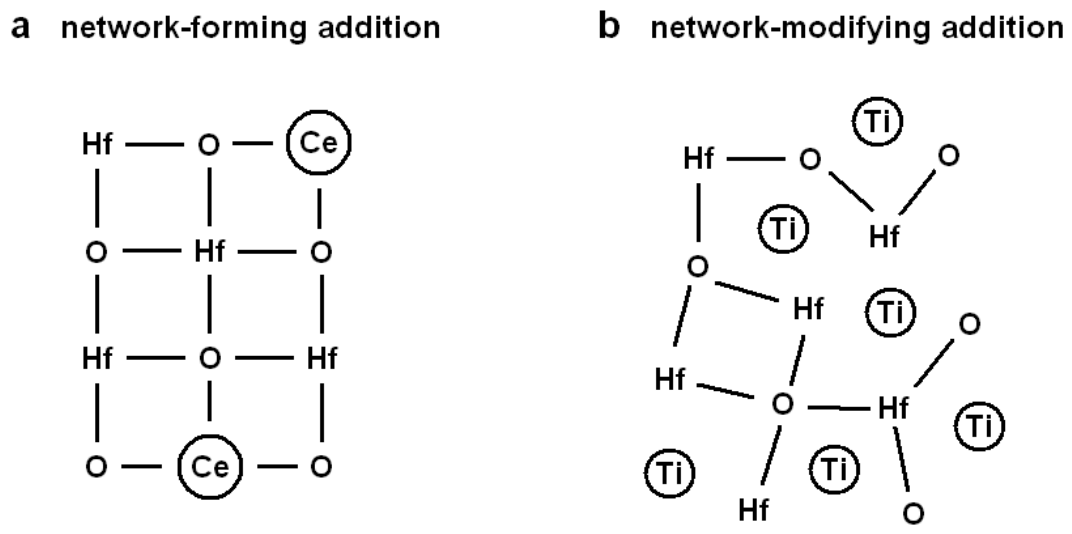

FIGURE 2.4: Schematic diagram of a network former (**a**) and a network modifier (**b**) in a HfO_2 matrix. Bond lengths/angles are not drawn to scale.

ion of ∼17% difference in ionic radius. The last ion in the table is Ti^{4+} which has a smaller effective ionic radius compared to Hf^{4+}. Although a smaller ion can potentially substitute in the lattice it might not promote the retention of a high-κ phase as a result. Also energetically such an inclusion is balanced against Ti's fast diffusive properties due to its size and hence network-modifying capabilities. Figure 2.4**a** shows schematically the substitution of Ce in a HfO_2 lattice. Figure 2.4**b** demonstrates the effect of adding a network-modifying addition in a high enough proportion to disturb the long range periodicity of the lattice. Additionally the thickness of the films is thought to be a factor when preserving an amorphous phase in a solid state reaction. At some critical film thickness the nucleation of the equilibrium phase is favoured [25]. The thin films described in the results chapters are in the thickness range to potentially promote the retention of such a non-equilibrium amorphous phase.

To summarise, in the addition of a species to produce a ternary oxide with HfO_2 as the starting material the film thickness, size and valance of addition ion and relative proportion are key parameters. Deposition temperature and post-deposition heat treatments are then of importance in influencing the type of material formed.

2.2 Reported HfO_2-based dielectric materials

This section presents a summary of the reported hafnium oxide-based dielectric films deposited by ALD and CVD. This is not an exhaustive list but is intended to draw together the literature concerning the implementation of HfO_2 dielectrics and the permittivity enhancements on basic HfO_2 discussed previously.

2.2.1 HfO_2 systems

A large volume of experimental work preceded ALD HfO_2's adoption as dielectric replacement for nitrided SiO_2 in transistor technology. Early device reports utilising ALD HfO_2 as a dielectric cited EOTs of $\sim$1.3 $\mathring{A}$ and leakage current density $\sim 10^{-7}$ A/cm^{-2} - figures of merit that demonstrated that the capacitance density of a HfO_2 thin film was enough to combat direct tunnelling while permitting further device miniaturisation [26, 27]. The $HfCl_4/H_2O$ ALD process was used by many investigators owing to it displaying robust ALD growth characteristics from a simple ligand exchange growth reaction (see chapter 3 for a description of the $HfCl_4/H_2O$ process). One issue with the process was the risk of Cl contamination; in the film itself affecting electrical performance but also in the substrate as a void former during fabrication anneals. O_3 was investigated as a more efficient oxidant resulting in lower Cl contamination but the $HfCl_4/H_2O$ ALD process results in higher oxygen concentration in the films - potentially resulting in a thicker interface layer. In the end an improved $HfCl_4/H_2O$ ALD process was preferred due to the extra manufacturing issues surrounding the use of O_3 generators.

Despite the positive aspects of these initial HfO_2 investigations poor channel mobility in HfO_2/poly-Si-gate-based devices remained a concern. Strained silicon had been implemented at previous technology nodes in order to up channel mobility but with the replacement dielectric material came a new issue. The contribution of soft phonon scattering to channel electron mobility degradation was seen experimentally in 2004 and a metal gate material suggested to screen the effect [28]. A HfO_2/metal-gate dielectric stack offered the improved capacitance density of the new dielectric material while utilising a metal gate proffered channel mobilities as good as the previous nitrided SiO_2/poly-Si-gate technology.

These encouraging experimental results resulted in a huge amount of interest in ALD HfO_2 in the research community. The studies that were published from 2001 onwards tended to focus both on new precursors to facilitate HfO_2 deposition and structural and electrical measurements to fully understand the dielectric films that were being produced. Specifically the dielectric constant and leakage current density values were of significance. ALD was used in 2005 to deposit HfO_2 films which were shown to be stoichiometric and amorphous as-deposited (albeit with signs of short-range monoclinic structure) [29]. Post-deposition annealing resulted in a polycrystalline monoclinic structure. Both of these studies commented on the growth of an interfacial layer between the substrate and film materials and the increase of this layer's thickness on subsequent heat treatment. The study by Loo et al. in 2005 [30] described HfO_2 films grown using metal oxide chemical vapour deposition (MOCVD) using alkoxide precursors - combining high volatility with low reactivity in air. The films were seen to be monoclinic as deposited and non-stochiometric with some carbon present in their Auger analysis. Additionally the plasma-enhanced ALD (PEALD) of HfO_2 was demonstrated [31]. This utilised metal t-butoxide precursors with oxygen plasma exposure during growth. A comparatively higher dielectric constant of $\sim$25 was reported as well as a smaller relative EOT as a consequence of the lower leakage current measured in the PEALD specimens. The 2005 paper by Potter [32] offered a direct comparison of HfO2 deposited by ALD and MOCVD using the same reactor. The report demonstrated that neither deposition method demonstrated truly self-limiting growth behaviour and an explanatory mechanism was proposed. Work by Niinistö et al. [33] introduced HfO2 films on silicon using $Cp_2Hf(CH_3)_2$ (Cp=cyclopentadienyl or C_5H_5) and water as the precursors. Their films demonstrated low impurity levels and promising dielectric response (this hafnium precursor was the one used in the deposition experiments described in the results chapters of this thesis). The 2008 McNeill et al. article covered the ALD of HfO_2 films at 250 °C using tetrakis-ethylmethylaminohafnium (TEMAH) and water vapour as precursors. Electrical measurements yielded a dielectric constant of 14-18. Metallocene-type precursors were utilised to grow ALD HfO_2 [34, 35]. The Black et al. article covers the use of two such precursors, $[(Cp_2CMe_2)HfMe_2]$[2] and $[(Cp_2CMe_2)HfMe(OMe)]$, with O_2 or ozone

[2]Me: methyl or CH_4 ligand.

used as the oxidant in MOCVD and ALD experiments respectively. Auger spectroscopy results showed a 1.8-2.8 at.% carbon incorporation in the ALD films while electrical characterisation yielded a low current leakage density of $\sim 6\times10^{-7}$ cm^{-2} at $\pm$2MV cm^{-1}. The Dezelah et al. work focussed on $(MeCp)_2HfMe_2$ and $(MeCp)_2Hf(OMe)(Me)$ as the hafnium source with water vapour as the oxidant in ALD growth experiments. Elastic recoil detection analysis performed showed the films generally had carbon inclusion below the detection of the apparatus ($\leq$0.5at.%) and current leakage density of 1×10^{-5} Acm^{-2} at -3-0.5 MVcm^{-1}. Kim et al. [36] utilised a hafnium tetrakis-iso-propoxide ($Hf(OCH(CH_3)_2)_4$) source with O_2 as an oxidant. Their study described an amorphous matrix with monoclinic HfO_2 crystallites distributed within the film and a leakage of 8.9×10^{-6} Acm^{-2} at -1 V. In 2010 Niinistö et al. reported the use of $CpHf(NMe_2)_3$ and $(CpMe)Hf(NMe_2)_3$ with ozone as the oxidant each time [37]. They produced high-purity films at 300 °C deposition temperature for both hafnium precursors which were found to be mixed monoclinic and cubic/tetragonal crystallinity as-deposited.

Many more HfO_2 thin film reports exist, continuing to the present day, but the key points are that low-impurity HfO_2 films could be deposited using a range of precursors utilising thermal ALD. The films were generally found to comprise of the monoclinic polymorph but several articles reported mixed phase hafnia or amorphous HfO_2. Reported dielectric constants were 12–25 depending on phase and process specifics, generally reported κ=$\sim$19. Leakage current density varied tremendously report-to-report but the best values were $\sim10^{-7}$ Acm^{-2}.

2.2.2 X:HfO_x systems

In these examples X denotes the dopant addition included in a HfO_2 material. Table 6.1 at the end of the chapter sums up the phases and figures of merit reported for the materials systems discussed.

Al:HfO_x systems

Due to the experimental reliability of the trimethylaluminum (TMA) precursor a large amount of ALD and CVD reports have featured the $HfAlO_x$ system. The bulk of the Al-HfO_2 articles found the ternary film to have a sliding permittivity and bandgap depending on the specific composition as well as an increasing crystallisation temperature with Al addition [38, 39]. Aluminium has been found to increase the crystallisation temperature of a hafnium oxide matrix coinciding with an increase in band gap and reduction in permittivity of the material. In most cases the addition of Al in a HfO_2-based dielectric is found to increase the crystallising temperature considerably. Films incorporating around half as much Al as Hf, $Hf_{0.66}Al_{0.33}O_2$, are found to be amorphous up to annealing at 900 °C [40–42]. Materials of this composition are reported to have a κ of 14-15.

Ba:HfO_x systems

Barium-doped HfO_2 has been grown by liquid injection MOCVD [43] using $Ba(thd)_2$ and $Hf(thd)_4$ as the precursors. The additional barium was found to stabilise a cubic phase in the hafnia matrix obtaining a κ measurement of 35 for the higher-permittivity polymorph from C-V analysis. Some studies have focused on Ba-HfO_2 and its dielectric improvement on HfO_2 using first-principles calculations [44, 45]. Incorporating Ba atoms into a hafnia matrix is thought to decrease the presence of positive charges associated with oxygen vacancies due to the coupling of the additional barium atoms with the vacancies, promoting charge neutrality in the film.

Ce:HfO_x systems

Cerium-doped hafnium oxide has been demonstrated with a composition of $Ce_{0.1}Hf_{0.9}O_2$ derived from MEIS measurements [46]. This work used a liquid injection ALD system

(see chapter 3), [Ce(thd)$_4$] and MeCp$_2$HfMeOMe (MeCp=$CH_3C_5H_4$) as the organometallic precursors and ozone as the oxidant at 300 °C substrate temperature. After a 900 °C anneal the films displayed XRD diffraction features consistent with either the cubic or tetragonal HfO_2 polymorphs. An improved permittivity of 32 was calculated from C-V measurements with thicknesses taken from TEM micrographs. The leakage current density after annealing was found to be $\sim 10^{-5}$ Acm^{-2} at ±1 MV

Dy:HfO$_x$ systems

Dysprosium has been incorporated into hafnium oxide dielectrics via ALD, using Dy(EDMDD)$_3$ and Hf(O^{t}Bu)$_2$(mmp)$_2$ [47], and co-sputtering [48]. The ALD study found a ∼10% level of Dy addition stabilised a cubic phase in the material.

Er:HfO$_x$ systems

$Er_yHf_{1-y}O_x$ films have been deposited by ALD in various compositions using Er(thd)$_4$, (MeCp)$_2$Hf(OMe)(Me) and ozone as the oxidiser.[49]. Films with composition $Er_{0.13}Hf_{0.87}O_x$ were found to have a cubic phase in place of the monoclinic phase for pure HfO_2 as-deposited. The 13 at.%Er is found to be the optimum level and a κ of ∼37 is quoted. In the paper they highlight the differences seen between their own results and those of Wu et al. [50] who reported an amorphous $ErHfO_x$ film as-deposited and after a 30 s RTA at 800 °C. After annealing at 1000 °C a monoclinic HfO_2 film was formed, despite very similar chemistry and deposition conditions. The explanation is the smaller percentage (7 at.% instead of 13 at.%) of Er added to the HfO_2 matrix. This highlights the importance of control over composition in deposition in order to introduce the optimum level of an addition element.

Gd:HfO$_x$ systems

Gadolinium-doped HfO_2 films have been demonstrated by ALD using [Gd(^{i}PrCp)$_3$], $HfCl_4$ and H_2O as sources [51]. The optimum doping level was found to be $Gd_{0.11}Hf_{0.89}O_2$ which crystallised in a cubic/tetragonal form after spike annealing at 1300 °C. This materials preparation led to a κ value of 36. PLD [52] and sputtered [53] Gd-HfO_2 articles have reported κ values in the 21–23 region.

Ge:HfO_x systems

Ge-HfO_2 has been produced by ALD from deposited layers of GeO_2 and HFO_2 that mix on annealing at 425 °C in N_2. The subsequent effective 'doping' is responsible for the improvement of the uniformity compared to HfO_2, which is attributed to the lowering of the oxygen-vacancy formation energy [54].

La:HfO_x systems

Co-sputtered $HfLaO_x$ films were investigated as a potential dielectric gate material [55]. The addition of lanthanum was found to increase the crystallising temperature of the hafnium oxide matrix it was added to. Due to this mechanism the 33%La-HfO_2 films were found to remain amorphous after post deposition heat treatment up to 1000 °C in an O_2/N_2 ambient. C-V measurements yielded a permittivity of 20 which is roughly equivalent to undoped HfO_2. Similar findings have been reported for MOCVD deposition of La-HfO_2 [56, 57] with κ values of 20 and 28 reported respectively albeit with larger leakage current density recorded in the Huang et al. work. ALD growth studies of La-doped HfO_2 have also been carried out [58–60] finding an improvement in the flatland voltage and leakage current density with a post-deposition anneal. Zhao et al. [61] deposited $La_2Hf_2O_7$ via ALD and recorded improved dielectric relaxation and reduced dielectric loss after a post-deposition anneal in N_2 at 900 °C.

Si:HfO_x systems

Si-doped hafnium oxide has been demonstrated by co-sputtering [17] and ALD [62] with stabilised tetragonal Si-HfO_2 resulting in permittivities of 27 and 35 respectively. Some reports found silicon to incorporate into an amorphous hafnium silicate [63, 64] with more modest permittivities of ∼10–12. An interesting computational paper from 2007 [18] looks at the balance between adding an optimum level of Si to promote the tetragonal Si-HfO_2 structure in the material. Above the optimum level further addition of Si results in a lower κ as the balance swings towards atoms of lower polarisability in the material. By the time the SiO_2:HfO_2 ratio is 50:50 an amorphous silicate structure is stable with the relatively poorer κ values of 10–12 mentioned above. This system, and the

computational and experimental measurements reported on it, is an excellent description of the balance between dielectric mechanisms in a material of variable composition.

Sr:HfO_x systems

Strontium-doped HfO_2 films in the ratio Sr:Hf 3:1 have been grown by plasma-assisted ALD recently [65] using $Sr(^iPr_3Cp)_2$ and $(MeCp)_2Hf(OMe)Me$ as precursor sources. XRD measurements demonstrated that the amorphous as grown films developed diffraction consistent with either the cubic or orthorhombic phase of $SrHfO_3$ after a 30 minute anneal in air. A κ value of 21 was derived from the accumulation capacitance of C-V measurements performed at 100 kHz.

Ta:HfO_x systems

As Tantalum oxide (Ta_2O_3) is considered a promising dielectric materials in its own right a large amount of studies have looked at Hf-Ta_2O_3; that is materials systems where Hf is the addition to a Ta_2O_3 matrix. Ta-doped HfO_2 has been grown by co-sputtering using targets of HfO_2 and Ta_2O_5 [66]. An incorporation of 18%Ta was found to preserve an amorphous film up to an annealing temperature of 500 °C

Ti:HfO_x systems

Titanium oxide is an interesting dielectric material in its own right, frequently yielding a very high κ measurement due to its polarisability and low vibrational force constant. Of the three TiO_2 polymorphs the two that are usually reported are anatase (cubic) and rutile (the higher-temperature tetragonal phase) with a range of transition temperatures recorded depending on the growth method and other parameters. κ values of ∼40 (anatase) and ∼50–70 (rutile, anisotropic) are commonly quoted measurements [67]. ALD and MOCVD experiments go back as far as 1995 and in $TiCl_4$ [68], TiI_4 [69] and $Ti(^iOPr)_4$ [70] there are excellent self-limiting ALD precursor options. Other reports have described TiO_2 films via sputtering and sol-gel processes that show the same anatase→rutile temperature-dependent phase transition and dielectric properties shift. Titanium-doped HfO_2 has been demonstrated by CVD [71], sputtering [72] and

ALD [73]. Generally a linear increase in permittivity was noted with increasing addition of titanium [74–76].

Y:HfO_x systems

Yttrium oxide thin films have been grown by ALD [77, 78] and form a cubic structure as-deposited. A permittivity of ∼12–16 and a leakage current density of $<10^{-7}$ A/cm^2 at 2 MV/cm are typical for yttria dielectric measurements [79, 80]. A number of authors have demonstrated forming a cubic Y-HfO_2 phase with yttrium incorporation of between 4% and 19% [81–83]. These structural enhancements result in an improvement in the dielectric constant to ∼30 with a leakage current density of $\sim10^{-5}$ A/cm^2, at 1 MV.

Zr:HfO_x systems

Many parallels exist between HfO_2 and ZrO_2 due to hafnium and zirconium being so-called 'chemical twins'. The contraction of atomic radii across the lanthanide series in the periodic table results in a smaller atomic radius for hafnium than might be expected (0.156 nm compared with zirconium's 0.159 nm). Zr and Hf therefore exhibit very similar chemical behaviour, due to their similar radii and electron configurations, despite the steep increase in atomic mass and density between the two. ZrO_2 has been deposited by ALD using $ZrCl_4$ [84], ZrI_4 [85], $Cp_2Zr(CH_3)_2$ [86], $Zr[OC(CH_3)_3]_4$ [87], cyclopentadienyl sources [88] and alkylamido-cyclopentadienyl compounds with ozone [89] among others. These report frequenty found that the higher permittivity cubic or tetragonal phases were attainable in as grown films via ALD. κ values commonly quoted are ∼17–23 with leakage current density $\sim10^{-7}$ A/cm^2. Zr-doped hafnium oxide has been deposited by sputtering [90], ALD using the two tetrachlorides [91] and tetrakis(ethylmethylamino) precursors [92] and MOCVD [93–95]. These Zr-HfO_2 reports generally found improved EOT/permittivity and improved thermal stability in comparison with undoped HfO_2 films. Higher Zr additions ∼50% were found to promote a higher-κ tetragonal phase of a $Hf_xZr_{1-x}O_2$ alloy also indicating reduced charge trapping with Zr addition.

TABLE 2.2: Summary of reported materials properties of hafnium oxide-based ALD dielectrics; the best values in the literature from relevant deposition/processing methods are used. C: cubic, T: tetragonal, O: Orthorhombic.

Addition	**Phase(s)**	κ	**Leakage density (Acm^{-2})**	**Refs.**
None	Monoclinic	15–22	$\sim 10^{-7}$	[29, 30, 32, 33, 96–100]
Al	Amorphous	(100%Hf)∼19–∼7(100%Al)	$\sim 10^{-8}$	[38, 39, 101]
Ba	C Ba-HfO_2	35	-	[43]
Ce	C/T Ce-HfO_2	32	$\sim 10^{-5}$	[46]
Dy	C Dy-HfO_2	-	-	[47]
La	Amorphous	20-30	Values reported from $1–10^{-8}$	[58–60]
Si	T Si-HfO_2;Hf silicate	35;10–12	1	[62];[63, 64]
Sr	C/O $SrHfO_3$	21	-	[65]
Ti	Amorphous	(100%Hf)∼19–∼50(100%Ti)	$\sim 10^{-8}$	[73–76]
Y	C Y-HfO_2	29	$\sim 10^{-5}$	[81, 102]
Zr	T $Hf_xZr_{1-x}O_2$	(100%Hf)∼19–∼35(100%Zr)	$\sim 10^{-5}$	[90–93]

Chapter 3

Experimental: growth and processing

3.1 Atomic layer deposition (ALD)

3.1.1 Deposition detail

ALD is a deposition method which introduces each component of a film separately, using separate precursors for each. Here 'precursor' means a solid or liquid material source which, when heated to a gas phase, is designed to deliver a specific element during deposition reactions. For example $HfCl_4$ is an example of a hafnium precursor; the desired element, Hf, surrounded by a ligand system, in this case four chlorine atoms. The ALD process involves employing self-limiting surface reactions for each precursor that is introduced. A successful ALD precursor is designed to be introduced to a substrate in the reaction chamber in a saturative dose. Ideally, precursor molecules react by surface reaction, or chemisorption, with every available reaction site on the substrate surface. Excess precursor molecules will not react with the surface once all available sites have been filled and this is what is meant by a saturative dose. The precursor chemistry is balanced so that once the target atom is absorbed the rest of the ligand structure surrounding the target atom forms a surface species that the next supply of precursor can react with; with some of the surrounding molecular material forming reaction products which are removed in an inert gas purge of the chamber. Different surface species may be produced depending on how many existing surface species the

precursor molecules reacts with or if the precursor molecule chemisorbs [103]. Once the first precursor pulse has reacted with the surface, and the excess ligand material has been removed in an inert gas purge, a co-precursor is introduced to the reaction chamber. In the case of an oxide the co-precursor would be an oxidant. Once the co-precursor has reacted with the available surface species any excess co-precursor material is removed in another inert gas purge of the reaction chamber. The co-precursor reaction leaves a surface structure that the next precursor dose can react with. ALD films are built up in repeats of this step-wise reaction routine until the desired thickness is reached. In oxides one precursor pulse deposits a monolayer of a particular element with the next pulse being an oxidant. Common oxidants used in ALD process steps include H_2O, O_3 and O_2 plasma. In these 'binary' ALD processes the recipe would involve alternate doses of the metallorganic precursor and the oxidant in a two-step, repeating process. Figure 3.1 demonstrates the ALD process for depositing a hafnium oxide using $HfCl_4$ and H_2O as the precursors. This choice of example comes from the $HfCl_4/H_2O$ ALD process being the first to be employed in HfO_2-based dielectrics by Intel® [2]. Figure 3.1**1** shows the first dose of $HfCl_4$ entering the chamber just before making contact with the substrate. The OH groups on the substrate represent surface sites that can react with incoming precursor molecules. In figure 3.1**2** three $HfCl_4$ molecules have reacted with surface sites on the substrate and left a monolayer of Hf atoms which still have part of the ligand structure connected to them. This example demonstrates an exchange type reaction where the incoming precursor molecule exchanges one, or more, of its ligand branches for species on the surface bonded to oxygen (hydrogen atoms in this example). The reaction evolves 4HCl which is removed from the chamber in an inert purge leaving surface species that the oxidant dose can react with. In figure 3.1**3** a dose of H_2O is introduced to the chamber and reacts with the surface species from the previous step. In figure 3.1**4** the chamber is purged removing more evolved HCl and leaving alternative surface species so that further reaction steps can take place. In a binary deposition process these four dose/purge steps are repeated to build a layer of alternating reaction products on the substrate. A typical growth rate for a two-step oxide recipe is in the order of an angstrom, $\mathring{A}$, (0.1 nm) per completed ALD cycle [104]. A low-volatility precursor might have a growth rate $\sim$0.3 $\mathring{A}$/cycle whereas a high-volatility precursor

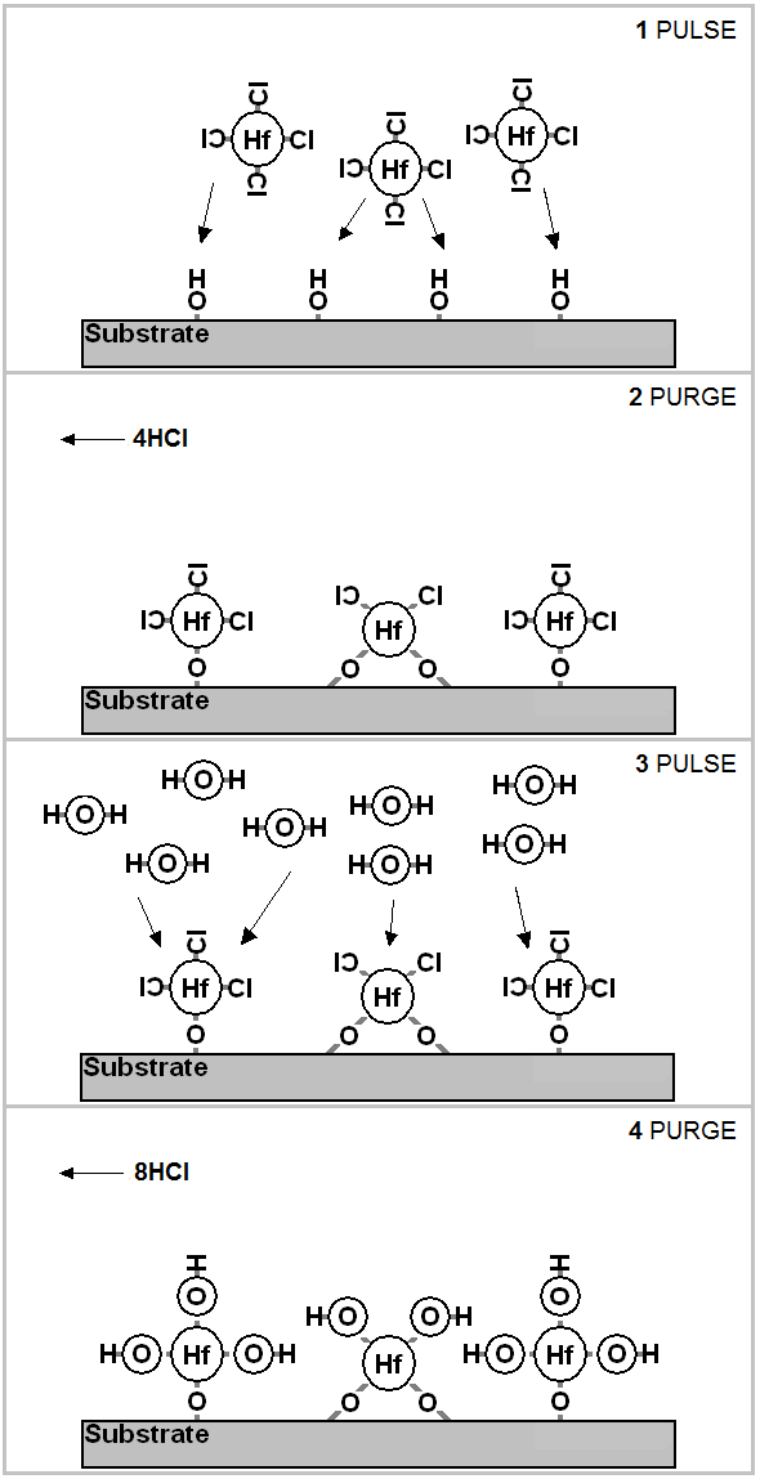

FIGURE 3.1: Schematic of the ALD layer-by-layer deposition process using the $HfCl_4$ ligand and water as an example system. Bond lengths/angles are not to scale and are drawn flat to the page.

might achieve ∼1 $\mathring{A}$/cycle. The $HfCl_4/H_2O$ process, with growth rate ∼0.6 $\mathring{A}$/cycle, can take 50 completed cycles to form a continuous film across the substrate surface [105]. This means a film thickness in the region of 3 nm before a continuous layer is present across the substrate surface. Slow growth rates are typical of polar precursor molecules in reaction with a hydrophobic substrate surface but this also demonstrates the island growth mechanism in the $HfCl_4/H_2O$ ALD process.

For a multi-component materials system the ALD recipe includes pulses of as many precursors as there are different components of the desired film composition, limited to how many sources can be connected to the reactor at any one time. The challenge with depositing multi-component oxides is to ensure that all precursor sources deposit in the same temperature window - potentially compromising on the ideal deposition parameters. Also each set of reactions, including alternate oxidant pulses, must leave a surface that the next precursor can react with in order to continue the step-wise reaction sequence.

3.1.2 Precursors

ALD precursors must satisfy several requirements to be successful practical candidates for deposition. The material must be volatile enough to promote vapour transfer from the bubbler to the reactor chamber; at least ∼0.1 Torr equilibrium vapour pressure at a temperature below that which would cause decomposition [106]. They should also vaporise rapidly and at a reproducible rate to replenish the headspace[1] of vapour inside the bubbler. They must not self-react but at the same time be highly reactive towards the surface states left on the substrate after the previous vapour pulse. The byproducts of the precursor/surface reaction must also be volatile enough to allow them to be easily removed in the gas purge. The reaction kinetics in ALD rely on the balance of bond strengths in the surface species and ligand structure. A well-designed ALD precursor will demonstrate an experimental 'ALD window' in which its deposition is truly self-limiting. Figure 3.2**a** demonstrates this in a schematic diagram. The window is a plateau of growth over a range of temperatures. Below the start of this range the process will demonstrate either low deposition rates from the reaction lacking the

[1] the headspace is the gaseous region of the bubbler contents, above the solid or liquid precursor.

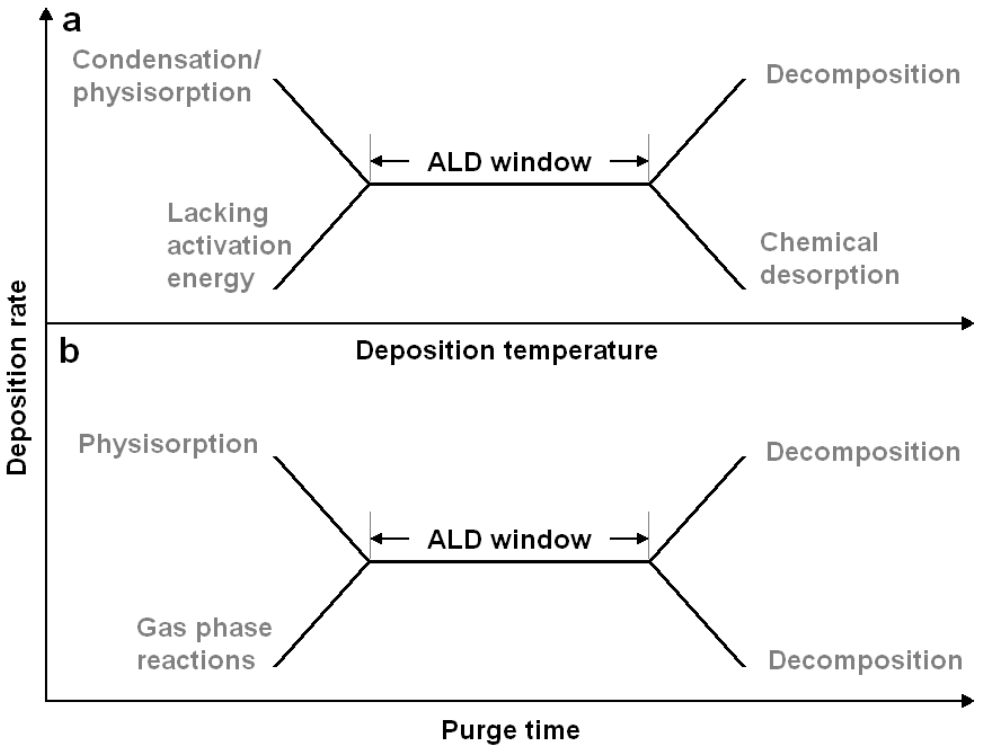

FIGURE 3.2: Schematic of the ALD process window depicting growth rate against **a** temperature and **b** purge time.

thermal energy necessary for chemisorption of the precursor on the substrate surface or too high a rate owing to condensation and physisorption of semi-reacted precursor material on the surface. Over the steady plateau the ALD process is demonstrating self-limiting deposition for the temperature range. Over a certain temperature there is the danger of precursor decomposition, the ligand structure protecting the target atom falling apart, or chemical desorption of the precursor before the second precursor has had chance to react with the resulting surface. Figure 3.2**b** demonstrates schematically that a similar window exists for growth rate vs purge time for a given precursor. Too little a purge time can result in two precursors being present in the reaction chamber at the same time, potentially leading to gas phase reactions between the two precursors. This can register as low growth rates or physisorption of reactants depending on where in the gas flow the gas phase reactions take place in relation to the reaction zone where the substrate is. With too long a purge time the adsorbed species from the precursor dose can be desorbed or thermally decomposed leading to lower or higher growth than expected depending on the reactions taking place. The dominant, and best understood,

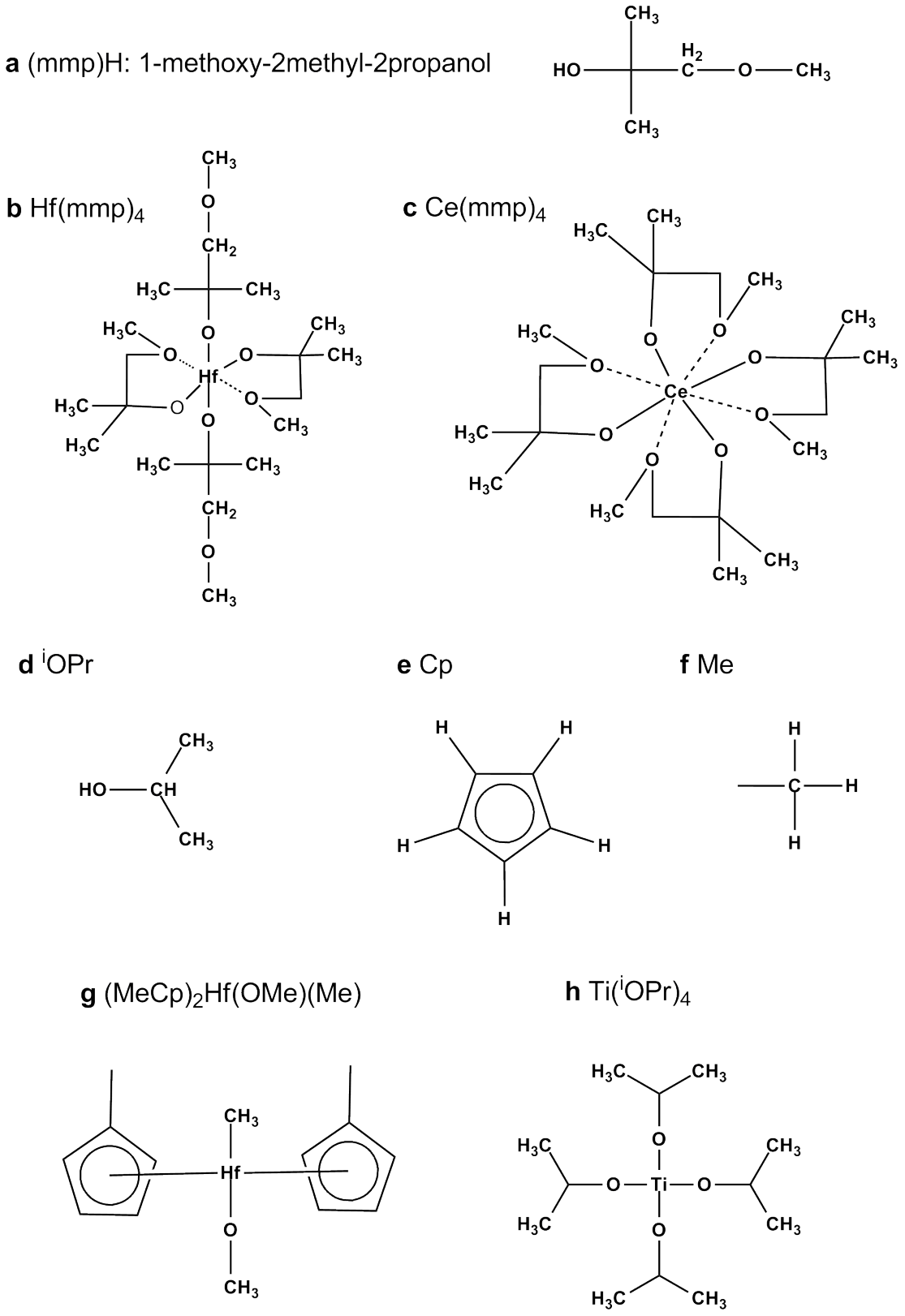

FIGURE 3.3: Schematic depictions of precursor ligand structures relevant to the deposition work. Bond lengths/angles are not to scale, the molecules are drawn flat to the page. **c**, **g** and **h** are the ligand structures of the precursors used in the experimental work.

ALD reaction is the 'ligand exchange' type of process which figure 3.1 typified where the incoming $HfCl_4$ breaks an O-H bond and joins the metal atom to the oxygen, releasing an HCl as a byproduct. Halide precursors like $HfCl_4$ have the advantage of being relatively inexpensive and thermally stable but can lead to issues with halide contamination in the films as well as problems with producing HCl acid as a reaction byproduct. Figure 3.3 introduces some of the ligand systems used in this work schematically. Figure 3.3**a** shows the mmp ligand; the mmp molecule is -1 electrical charge and is drawn in 3.3**a** attached to a H atom to produce a molecule of neutral charge. Figures 3.3**b** and 3.3**c** demonstrate the precursor molecules formed between this ligand and Hf and Ce respectively. The $Ce(mmp)_4$ molecule in 3.3**c** is the precursor used in cerium deposition as described in chapter 7. It can be noted that the two different central atoms form ligand systems of six and eight coordination respectively due to the differential in size between Hf and Ce. Ce forms four 'bidentate' bonds to the four ligands whereas the smaller Hf atom forms two bidentate and two regular bonds. Complexes of polydentate ligands (so-called 'chelating' ligand systems) tend to be more stable than mono dentate ligand systems [**ii**]. A higher coordination reduces the potential for oligomerisation of the precursor which means precursor molecules reacting together in the gas phase to form larger molecules. Figures 3.3**d**, 3.3**e** and 3.3**f** demonstrate the ^{i}OPr (isopropanol), Cp (cyclopentadienyl) and Me (methyl) ligand groups. These drawings are instructive in understanding the make up of some of the larger ligand structures described. Figures 3.3**g** and 3.3**h** show the structure of the $(MeCp)_2Hf(OMe)(Me)$ and $Ti(^{i}OPr)_4$ precursors used in chapter 6. Cyclopentadienyl precursors like $(MeCp)_2Hf(OMe)(Me)$ tend to be thermally stable but can have low reactivity and volatility as a result. Alkoxide precursors like $Ti(^{i}OPr)_4$ tend to be reactive to water vapour, and hence ideal for the formation of oxides, but can have limited thermal stability [107].

3.1.3 The OpAL® reactor

Figure 3.4 depicts the schematic layout of the Oxford Instruments plc OpAL® ALD reactor. The reactor has three lines that precursor bubblers can be connected to directly. The system has thermocouple-controlled heater jackets that surround the bubblers to accurately control precursor temperature. Vapour draw experiments can be used to

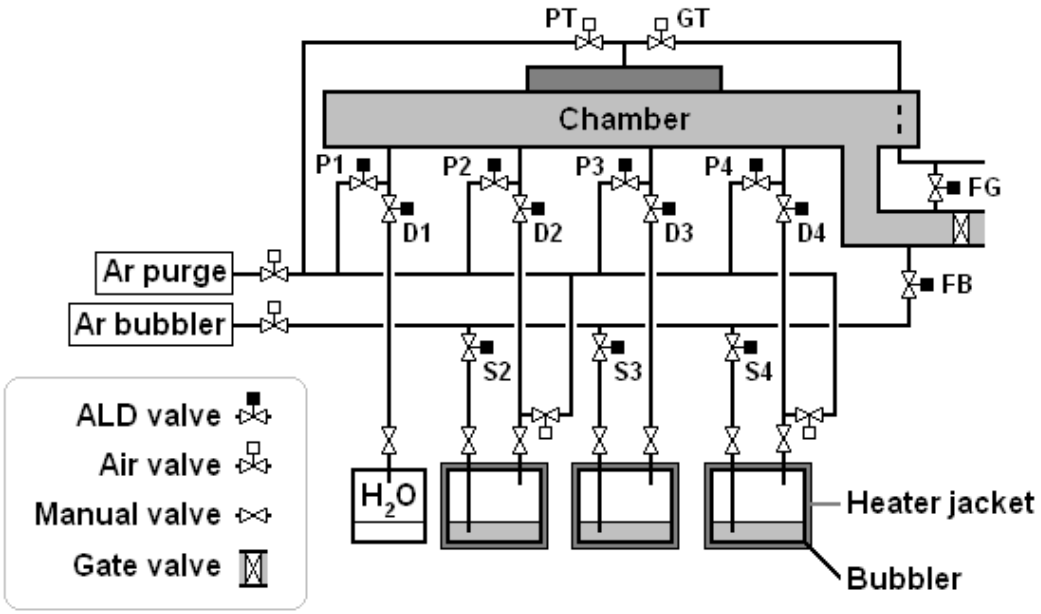

FIGURE 3.4: Schematic of the OpAL® ALD reactor.

gauge the amount of vapour being actively replaced in the bubbler headspace after the valve is opened. Depending on the volatility of the precursor, vapour draw might be enough to supply a dose of precursor into the reactor chamber. Usually a level of carrier gas (argon) is found to be necessary to transport the precursor. The level of carry and purge gas is another parameter that has to be altered and optimised. In the diagram the 'Ar purge' and 'Ar bubbler' lines that supply argon for both of these functions are depicted. The valves drawn with black squares are the ALD valves and on each precursor line the D and S valves are synchronised to open at the same time. As can be followed on the drawing this enables the S valve to allow Ar carrier gas from the Ar bubbler line into the bubbler via the dip leg on the left of each bubbler. ALD valves are precision pneumatic actuators that allow excellent control over timed release of vapour. The D valve on each line opens simultaneously to supply a dose of precursor vapour from the bubbler to the chamber. The P valves operate on the purge step after each dose of precursor has been delivered. The reactor has a baffle grille fitted above the chamber (not depicted in the diagram) intended to ensure a uniform delivery of incoming precursor material but which also potentially reduces the amount of material that reaches the chamber.

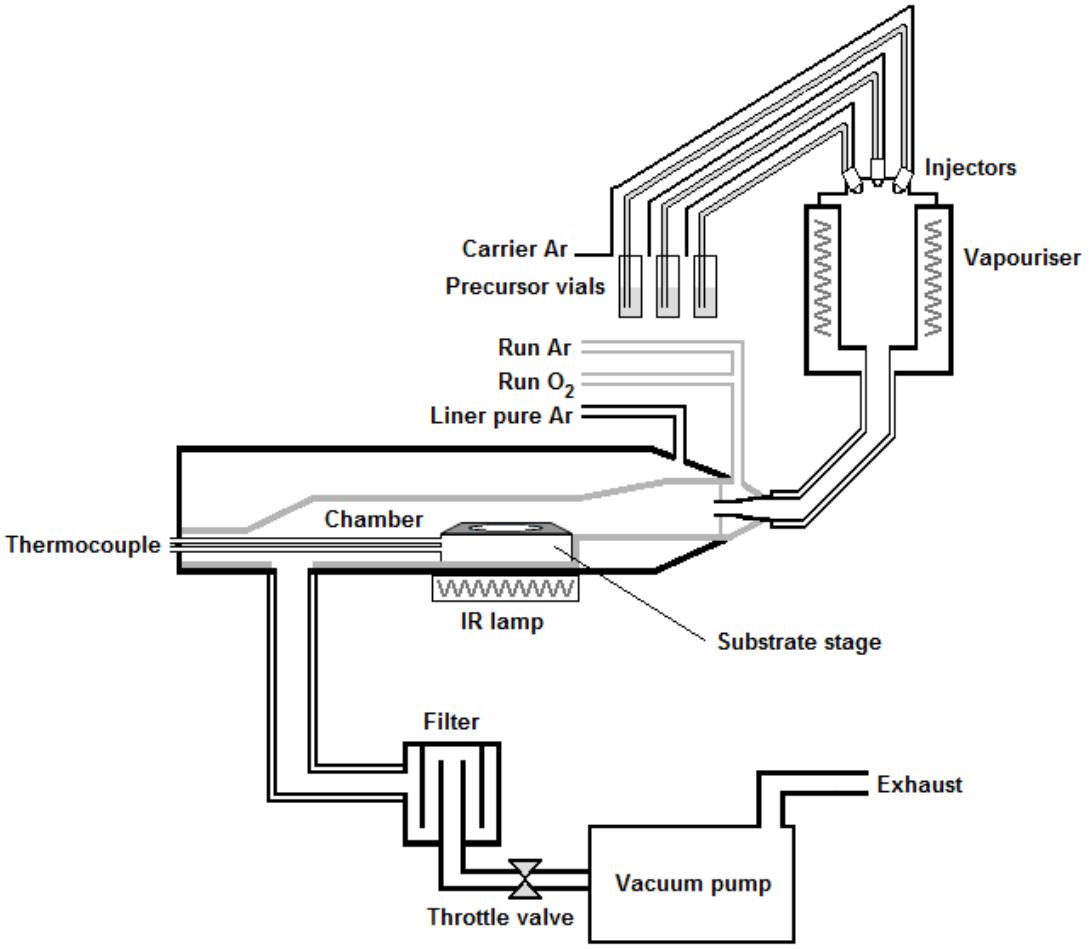

FIGURE 3.5: Schematic of the Trijet^{TM}ALD reactor.

3.1.4 The Trijet^{TM} reactor

Figure 3.5 is a schematic diagram of the Aixtron SE 200FE liquid injection Trijet^{TM} ALD reactor; a horizontal flow CVD reactor fitted with a liquid injection solvent delivery system. The substrate sits on a graphite heating stage, on a revolving sample holder facilitating uniform deposition. A bank of five electrically-tuneable infra-red lamps and a thermocouple are used to heat the sample stage and maintain its temperature. Precursors are dissolved or diluted in a suitable carrier solvent (typically hexane or toluene) and stored in graduated glass vials. Pressurised liquid transport then delivers the precursor solution through three separate injector nozzles into the vapouriser. The vapouriser includes five thermocouple-controlled temperature zones which have a maximum temperature of 250 °C. In turn the vapouriser supplies the horizontal reaction chamber

shown in grey in the schematic. The chamber is housed in a cylindrical quartz liner (black in the schematic) which is the vacuum vessel for the reactor. As shown in the diagram below the precursor vials this liner has a dedicated Ar supply and there is pipework to supply Ar or O_2 into the chamber, via a Venturi mixing system, during deposition runs. Post-run reaction gas mixtures are fed through a water-cooled filter system to condense non-volatile reaction products before leaving the system via an externally vented exhaust. The vacuum is supplied to the system from a five stage dry rotary pump, with pressure controlled by a throttle valve. The chamber pressure is maintained using a vacuum gauge (not drawn on the schematic).

3.2 Post-deposition treatments

3.2.1 'Standard' annealing

Specimens were annealed in a tube furnace to assess phase changes as a result of the heat treatment. This apparatus takes cleaved specimens in a ceramic crucible which is put into the centre of the furnace's heating tube. Temperatures up to ∼1000 °C were possible. Another option was to add a N_2 atmosphere anneal by flowing N_2 gas through the furnace tube before and during the heating of the specimen and during the cooling of the specimen in a cooler section of the tube. In the experimental chapters a **standard** anneal will refer to 30 minute anneals performed in the tube furnace in an N_2 atmosphere. This annealing technique was used to monitor phase changes in the films but not for specimens for which subsequent electrical measurements were taken. As the temperature ramp-rate was 5 °/min the furnace was brought to temperature first, the desired annealing atmosphere set and then the specimens were inserted into the tube.

3.2.2 Rapid thermal processing (RTP)

Specimens intended for electrical measurements were annealed in another furnace that could provide a much faster temperature ramp-rate. The film specimens subjected to electrical measurements in chapters 5, 6 and 7 involved two different annealing regimes. One set of each type of sample were heat treated at 500 °C for 30 minutes in a N_2

atmosphere while another was spike annealed up to 850 °C and back down to room temperature with a ramp-rate of 25 °/s. These two approaches might give different results depending on whether a phase change in an oxide is a temperature or time-dependent process. The rationale behind using these two heat treatments was to simulate the gate-first and gate-last annealing recipes used in microchip production [108, 109]. Gate-first integration involves deposition of the gate stack, patterning of the gate lines, and finally a high-temperature dopant activation anneal which our rapid thermal processing (RTP) is aimed to simulate. Gate-last integration is where some or all gate stack materials are deposited after the activation anneal and this is simulated in the 500 °C/30 minute annealing treatment. These annealing strategies will be referred to in the experimental chapters as gate-first: **850 °C/spike** and gate-last: **500 °C/30 min**.

Chapter 4

Experimental: analytical techniques

4.1 Film characterisation

4.1.1 X-ray diffraction (XRD)

X-ray diffraction (XRD) provides information on the crystalline phases present in a specimen.

XRD theory

XRD takes advantages of the physical dimensions of X-rays' wavelengths being in the same order of magnitude as interatomic spacing in order to probe a material's crystallographic geometry. Incident X-rays are scattered randomly by each atom they interact with in the crystal. As crystals are periodic arrays of atomic planes, diffraction results from phase differences between atoms in planes of different depths into the material.

$$sin\theta_{hkl} = \frac{\lambda}{2d_{hkl}} \tag{4.1}$$

Equation 4.1 is Bragg's law - a simple, scalar, relationship between scattering angle, θ_{hkl}, and d-spacing, d_{hkl}, for a crystallographic plane with index hkl. λ is the wavelength of the X-ray source. The d-spacing is a measure of the separation of the planes of atoms and the law describes maxima for diffraction from crystallographic planes at the

coherent superpositions of the X-rays scattered from the sample. Diffracted beams are those superpositions of a large number of scattered X-rays that reinforce each other by Bragg's geometry and where the law is satisfied the diffracted beam has an amplitude that is a sum of all the contributing scattering components. For measurement angles that don't satisfy the law the scattering cancels in a combination of X-rays with random phase differences. XRD results give the user a reciprocal lattice map where peaks in the intensity profile relate to crystallographic planes within the specimen. Another way to imagine the diffraction condition being satisfied is the geometry of the Ewald sphere in reciprocal space. For an incident X-ray beam with wavelength λ and vector $\mathbf{I}_0$ there would be an equivalent beam, $\mathbf{I}_0/\lambda$ parallel to $\mathbf{I}_0$ in reciprocal space. If $\mathbf{I}_0/\lambda$ is set up to terminate at a reciprocal lattice point the sphere centred at the origin of $\mathbf{I}_0/\lambda$, with a radius of $1/\lambda$, is the Ewald sphere. The sphere is the locus of possible scattering for wavelength λ from incident beam $\mathbf{I}_0$. For scattering to occur from a certain plane (hkl) the Ewald sphere must intersect the reciprocal lattice point hkl. This scattering condition is analogous to the Bragg law which can be developed directly from the sphere geometry.

Although Bragg's law is satisfied for a precise angle for a given plane the peaks have a Gaussian profile and can broaden with respect to the specific angle for several reasons: instrumental broadening, lattice strain, temperature factors and, in a given size regime, crystallite size; the peaks resulting from a diffraction experiment are convolutions of the contributions from each of these factors. Even defect-free powder specimen will still produce diffraction peaks of a certain width due to instrumental broadening from the X-ray source profile, the widths of the slits in the diffractor assembly and the size of the X-ray beam itself. Additional broadening effects are related to crystallite dimensions in polycrystalline materials. If reflections from the second layer into the crystal's depth differ only slightly from an integral number of wavelengths, the reflection that is completely out of phase with the first lies deep beneath the crystal surface. In very small crystal sizes this deep completely-out-of-phase reflection will not exist. The effect of this is a lack of cancelling out of the random scattering immediately around the Bragg angle

of a diffraction feature and an apparent broadening of the diffraction peak.

$$\tau = \frac{K\lambda}{\beta(cos\theta_{hkl})} \tag{4.2}$$

Equation 4.2 is the Scherrer equation which gives a measure of crystallite size, τ, for a θ value in degrees relating to the specific peak and β, a measure in radians of the width of the diffraction peak at half its intensity. K is a constant which varies depending on the model assumed for crystallite geometry. This calculation estimates crystal broadening in the direction perpendicular to the specific plane analysed, θ_{hkl}.

XRD apparatus/conditions

The X-ray diffraction (XRD) measurements throughout were made on a Rigaku Miniflex diffractometer using water-cooled Cu target Kα radiation (0.154051 nm wavelength, 40 kV, 50 mA). Scans between 5 ° and 150 ° 2θ are possible at speeds down to a minimum of 0.01 °/minute in continuous mode; though fixed-time scans are possible where an interval is set and the machine takes one measurement for every interval within a start and end point. The angle measured experimentally between incident beam and diffracted beam is 2θ rather than θ due to the geometry of the diffractor assembly. The diffractometer has a detector set on a goniometer arm and the specimen stage and detector arm move together to form the angles scanned. The technique results in no damage to the specimens but is limited to ∼5–15 mm^2 surface area and <∼3 mm thickness.

4.1.2 Raman spectroscopy

Raman spectroscopy provides information on a material's physical structure as a result of the scattering of light resulting from interactions with phonons in the material.

Raman theory

Raman is another powerful and non-destructive technique which can yield information on a specimen's molecular/crystallographic structure. As well as characteristic peak sets that can help identify a specific phase or material, the measurements, and particularly the mode line shape, can also lead to deductions about phonon distribution,

crystallite size, strain, crystallographic orientation, substitutional effects and other subtle properties of a sample. The Raman effect is the inelastic scattering of photons within the visible light wavelength range - specifically scattering from interactions with optical phonons; the analogous effect from interactions with acoustic phonons being Brillouin scattering. In a contrast with other spectroscopy techniques, Raman scattering covers a wide range of energies but is limited to phonon scattering processes with negligible change in scattering wave vector compared to the wave vector associated with the incident photon (k=0). On top of this, Raman-scattered phonons are those whose atomic displacements effect a change in lattice polarisability; hence *Raman-active* modes are the subset of k=0, normal optical modes that also associate with a change in polarisability[1]. The conditions that specify whether a normal mode makes it into this subset are to do with the symmetry of the material lattice and are determined by the selection rules that result from a group theory analysis.

In the case of the polarisability condition it is useful to remember that the polarisability is a constant of proportionality between electric dipole moment of a molecule, μ_i, and electric field strength, ϵ, when the molecule is subjected to the electric field:

$$\mu_i = \alpha\epsilon \tag{4.3}$$

This polarisability is a measure of how much the electron cloud around a molecule can be distorted by the application of an electric field. The electric field can be expressed as:

$$\epsilon = \epsilon^0 cos 2\pi t \upsilon_0 \tag{4.4}$$

where ϵ^0 is the equilibrium field strength and υ_0 is the angular frequency of the radiation. In the case of a diatomic molecule with a vibrational frequency υ_v that goes through simple, harmonic vibrations a coordinate q_v along the axis of vibration at time t is given by:

$$q_v = q_0 cos 2\pi \upsilon_v t \tag{4.5}$$

[1] There are occasionally phonon modes which appear to break these rules - the 325 nm Raman response of CeO_2 in the Ce-HfO_2 results chapter is one such example.

If the polarisability changes as a result of this vibration its value will be given by:

$$\alpha = \alpha^0 + \left(\frac{\partial \alpha}{\partial q_v}\right)_0 q_v \tag{4.6}$$

Substitution of 4.5 in 4.6 yields:

$$\alpha = \alpha^0 + \left(\frac{\partial \alpha}{\partial q_v}\right)_0 q_0 cos2\pi v_v t \tag{4.7}$$

Now if incident radiation v_0 interacts with the molecule in our example, from 4.3 and 4.4:

$$\mu_i = \alpha\epsilon = \alpha\epsilon^0 cos2\pi v_v t \tag{4.8}$$

Substituting 4.7 in 4.8 leads to:

$$\mu_i = \alpha^0\epsilon^0 cos2\pi v_v t + \left(\frac{\partial \alpha}{\partial q_v}\right)_0 \epsilon^0 q_0 cos2\pi v_v t cos2\pi v_0 t \tag{4.9}$$

Which can be rewritten:

$$\mu_i = \alpha^0 F^0 cos2\pi v_0 t + \left(\frac{\partial \alpha}{\partial q_v}\right)_0 \frac{\epsilon^0 q_0}{2}[cos2\pi(v_0 + v_v)t + cos2\pi(v_0 - v_v)t] \tag{4.10}$$

Equation 4.10 is useful in this discussion at it contains terms that relate to elastic (Rayleigh) scattering, v_0, and two terms that describe the so-called Stokes and anti-Stokes scattering contributions, $v_0 \pm v_V$, that occur either side of the elastic response. The Raman-shifted peaks used in this work are known as Stokes scattering where the molecule or lattice absorbs energy from the incident photon and produces a scattered photon of lower energy in the inelastic process. Mirrored at 0 cm^{-1} there would also be an 'anti-Stokes' scattering signal which cannot be seen in the axis chosen for the figure. Stokes scattering is used for Raman spectroscopy as statistically there are more molecules that exist in the lower energy state and result in this kind of response - resulting in higher intensities. Also in equation 4.10 is a demonstration that if

$$\left(\frac{\partial \alpha}{\partial q_v}\right)_0 = 0$$

then μ_i=0 and so the polarisability must change during the vibration event for Raman scattering to result.

Taking the relatively simple CeO_2 (space group Fm3m or O_h^5) as an example we can describe the group theory analysis and the repercussions for measurements in a particular scattering geometry. Calculating the irreducible representation for cubic Ce_2 yields the A_{1g}, E_g and F_{2g} modes. For the A_{1g} 2nd order mode:

$$\begin{pmatrix} a & \square & \square \\ \square & a & \square \\ \square & \square & a \end{pmatrix}$$

resulting in scattering geometry (xx), (yy), (zz) or $(\bar{x}\bar{x})$. For the the E_g 2nd-order mode:

$$\begin{pmatrix} b & \square & \square \\ \square & b & \square \\ \square & \square & -2b \end{pmatrix} \begin{pmatrix} -\sqrt{3b} & \square & \square \\ \square & -\sqrt{3b} & \square \\ \square & \square & 0 \end{pmatrix}$$

resulting in scattering geometry (xx), (yy), (zz), $(\bar{x}\bar{x})$ or $(\bar{x}\bar{y})$. And finally for the the F_{2g} triply-degenerate mode:

$$\begin{pmatrix} \square & \square & \square \\ \square & \square & d \\ \square & d & \square \end{pmatrix} \begin{pmatrix} \square & \square & d \\ \square & \square & \square \\ d & \square & \square \end{pmatrix} \begin{pmatrix} \square & \square & d \\ d & \square & \square \\ \square & \square & \square \end{pmatrix}$$

resulting in scattering geometry (zy), (yx) or $(\bar{x}\bar{x})$; (xz), (zx) or $(\bar{x}\bar{x})$; (xy), (xz) or $(\bar{x}\bar{x})$. Porto's notation [110] describes the experimental geometry of the Raman measurement: *excitation* [propagation direction] (*excitation* [polarisation direction] *scattering* [polarisation direction]) *scattering* [propagation direction]. Our experimental set up of $z(\bar{x}\bar{x})z$ means that our spectra would be expected to contain all three of the above modes for cubic ceria although only with the 325 nm source do the 2nd-order modes appear in the measurements.

Raman apparatus/conditions

Raman spectra were acquired on a Horiba Jobin-Yvon LabRam HR. The Raman apparatus consists of an optical microscope and several laser sources which are fitted to run through a series of optics and then coincide with the direction of visible light through the microscope. As such the lasers focus on a specimen surface at the same point that the visible light would come into focus. The lasers available are a 325 nm HeCd ultra-violet (UV), a variable Ar ion laser offering 488 nm blue/514 nm green, a 633 nm HeNe red and a diode laser that provides 785 nm infra-red. In general the shorter wavelength 325 nm source was found to be the most useful for thin film analysis. Each laser has its own refining filter in the optical path before the source is channelled into the microscope assembly. After incidence with the specimen surface the laser signal is returned through a notch filter, again specific to each source, which cuts out the elastic scattered light from the signal to leave only the Raman-shifted component. This part then falls onto a holographic grating which diffracts the signal to be then picked up by a Peltier-cooled charged-coupled device (CCD). The holographic gratings can be substituted and differ in notches per inch and are blazed (optimised) for a specific source wavelength. For the two sources used in this thesis the 1200 grooves/mm filter is blazed for the 325 nm, UV source and the 1800 grooves/mm grating is blazed for the 514 nm, green laser source.The system also has a confocal aperture which can effectively control the amount of signal from the lens that is allowed through into the rest of the light path; this can be set to values from tens of microns to 1 mm. As the spectrometer sweeps the wavenumber range the Raman measurement is made in acquisitions; the time spent and number of acquisitions per wavenumber band is set before operation. Before measurements are conducted the spectrometer is calibrated; first to an elastic, or Rayleigh, signal at 0 nm and then to a known Raman signal. Generally the first-order silicon peak at $\sim$520 cm^{-1} is used. The first stage of this calibration sets the spectrometer's zero return and is an iterative process of cycles of reset and measure. The second stage effectively sets in nanometers the width of a spectrometer motor-step; this doesn't need to be reset and repeated but a value should be set for each different source wavelength to be used. Standard Raman measurements performed in this work used two acquisitions of 30 seconds with an aperture setting of 300 μm.

4.1.3 Medium energy ion scattering (MEIS)

Medium energy ion scattering (MEIS) provides quantitative information on the thickness and composition of a thin film material with atomic layer depth resolution possible.

MEIS theory

Ion scattering spectroscopy techniques utilise an incident beam of ions hitting solid samples in an ultra-high vacuum (UHV) enclosure. Some of this incoming beam is scattered back into the vacuum after collisions with atoms in the sample, 'target atoms', near the surface. Incident ions are scattered elastically in one-on-one collisions with surface target atoms resulting in a range of scattering angles and energies; elastic energy loss is a result of the collision of incident and sample nuclei and the scattering angle and mass ratio between them. Measurements made on the subsequent energies of these backscattered ions can be used to deduce the atomic mass of the target atoms collided with in the scattering process. The energy after an elastic collision is written [111]:

$$K = \frac{E_1}{E_0}\left[\frac{(M_2^2 - M_1^2 sin^2\theta)^{1/2} + M_2 cos\theta}{M_2 + M_1}\right]^2 \tag{4.11}$$

where E_0 and E_1 are the incident and post-collision beam energy, M_1 and M_2 are the atomic masses of an incident ion and a target atom and θ is the experimental scattering angle. If all other values in equation 4.11 are known accurately M_2 can be calculated to determine the target element involved in the collision. Quantitative compositional analysis of a film can be performed by measuring the scattering counts for specific elements while taking scattering cross sections into account - in MEIS the scattering cross section is proportional to the square of the atomic number of a specific target atom. In the data interpretation this is normalised to give a relative atomic ratio [112]:

$$\frac{R_1}{R_2} = \frac{C_1}{C_2}\left(\frac{Z_2}{Z_1}\right)^2 \tag{4.12}$$

where R, C and Z are atomic fraction, relative scattering counts and atomic number respectively for two different elements. Scattering from ions from beneath the surface might also contain an additional inelastic component derived from interactions between

incident and target electrons which depends upon the path length travelled through the sample before rejoining the vacuum. Ions scattered from below the sample surface lose energy inelastically at a rate proportional to the distance the ion travels in the specimen. This extra energy loss can be used to calculate depth profiles in the sample and is often discussed in terms of the stopping power (eV/$\mathring{A}$). To make accurate depth assessments it is useful to have the film thickness available from another measurement type (ellipsometry, TEM, etc.) as otherwise the calculation involves assuming bulk materials densities which can differ significantly from thin film densities [113].

MEIS apparatus/conditions

The specifics of the Daresbury MEIS facility have been published by Bailey et al. [114]. The MEIS experimental station consists of interlocked UHV chambers, a specimen preparation/characterisation chamber and a scattering chamber, which are connected by a sample transfer system. The MEIS technique uses a beam of He^+ or H^+ ions with an energy of 200 keV provided by an accelerator. The beam line produced transports the streams of positively charged ions into the scattering chamber via collimating slits that ensure a beam divergence at the specimen of less than 0.1 °. The beam is aligned along a crystallographic orientation in the specimen. For the $TiHfO_2$ measurements the beam was aligned along the Si $[\bar{1}\bar{1}1]$ direction of the substrate, with the detector positioned to record data along the Si [112] blocking channel. This geometry produced a 90 ° scattering angle. For measurements on the Ce-HfO_2 samples a different geometry had to be chosen to ensure that the Hf and Ce peaks were not convoluted as this would make compositional analysis difficult. For Ce-HfO_2 the beam was aligned to the [111] axis of the substrate, with the detector positioned to record along blocking direction [100]. This experimental geometry produced a 125.3 ° scattering angle. Post incidence scattered ions are captured by a toroidal-sector electrostatic analyser before hitting a 2-D detector. MEIS experiments were not run on un-doped HfO_2 films but a set of such experiments was published recently [115].

4.1.4 Transmission electron microscopy (TEM)

Transmission electron microscopy (TEM) was used for lattice imaging of thin film crystallinity as well as providing information on interface and film thicknesses.

TEM theory

In TEM experiments a specimen is irradiated by an electron beam of uniform current density with an acceleration voltage of 200–500 kV. As TEM measurements work in transmission very thin specimens are necessary, ∼100 nm thickness, as the technique utilises interactions between the electron beam and the specimen atoms in elastic and inelastic scattering events. The beam is formed from the application of very high voltage to a filament which emits electrons by thermonic, in the case of a standard filament, or field emission as in the case of a LaB_6 single crystal tip. The filament is placed at the top of a vacuum column so that the emitted electron beam travels down though condenser, objective and projector lens arrangements on its way towards the specimen. These magnetic lenses serve to converge the beam so that the convergence is an experimental parameter that can be controlled via the applied current. The column contains an airlock system to allow the insertion of the specimen holder. The most common image mode of operation is bright field imaging whereby higher atomic number material, or thicker material, appears darker in the image due to occlusion and adsorption of electrons by these areas. The electron beam can also be used to gain diffraction data which appears as spots, in the case of a single crystal, or a series of ring traces in the case of a polycrystalline specimen.

TEM apparatus/conditions

Cross sectional transmission electron microscopy (XTEM) was carried out on a JEOL 3010 microscope fitted with a LaB_6 field emission gun to study the film thicknesses and the structure of the films. Specimens were constructed by fixing cleaved segments of specimen films face to face with a thin layer of epoxy and leaving them clamped on a heating stage to cure the adhesive. Usually some silicon sections were glued on the outside to act as housing for the films of interest. The specimen stacks were then attached to a grinding jig using superglue and ground perpendicular to the glue plane

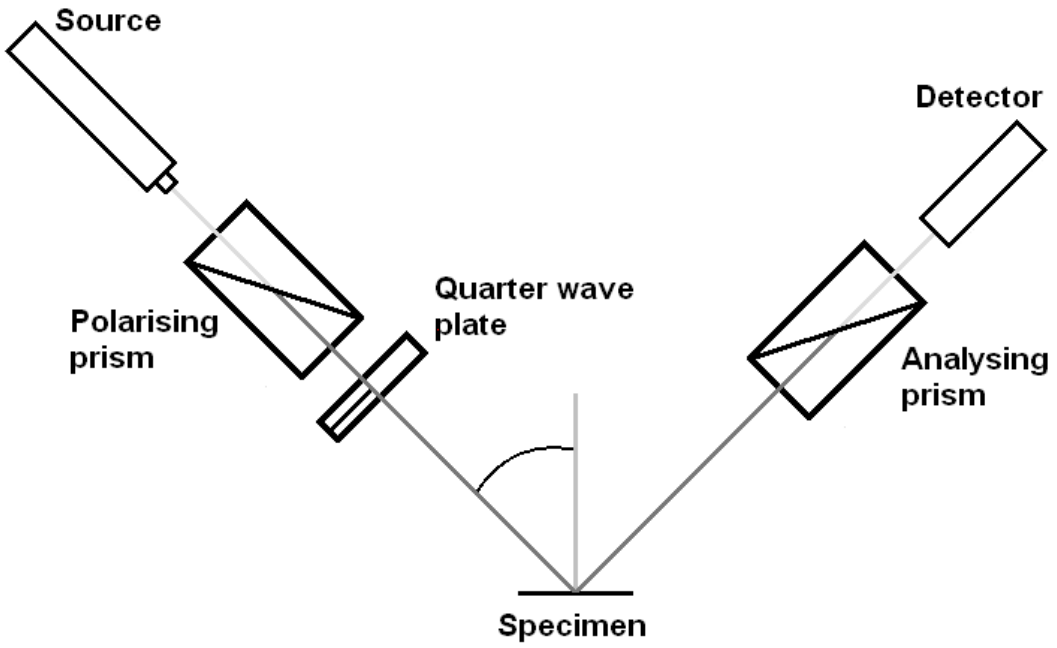

FIGURE 4.1: Schematic of the measurement geometry of nulling ellipsometer.

using successively finer grades of silicon carbide paper down to an 8 μm finish. They were then separated by soaking in acetone, reattached the opposite way round and the grinding repeated on the reverse of the specimen. Once thinned to a thickness of $\sim$50 μm copper slot grids were attached and the stacks were ion milled in a 10^{-5} mbar vacuum, from both sides, at a cone angle of 4 $^\circ$ to the grinding plane at a beam voltage of 5 keV until the instant a hole appeared at the glue interface. This was to leave areas of interest in the electron transparent thickness regime. After brief milling at a lower voltage/angle to effectively clean the surrounding area the specimens were transported to the microscope which used an operating voltage of 300 kV during the analysis.

4.1.5 Nulling ellipsometry

Nulling ellipsometry was used to estimate the thickness of thin films specimens.

Ellipsometry theory

The ellipsometer apparatus is set up in a linear optical plane as shown in the schematic in figure 4.1. From the source the monochromatic light is polarised via a polarising prism and then hits a quarter wave plate (QWP) which is mounted to be perpendicular

to the source direction and the angle indicated above the specimen. A QWP introduces a phase difference of 90 ° between two perpendicular components of the source and in practice is set at ±45 ° to the light path; this creates a circularly-polarised source which next hits the specimen. The ±45 ° setting is a standard configuration that makes the equations describing the light travelling through the machine much simpler. After incidence with the specimen the light travels through a second analysing prism and then into a photomultiplier detector. With the QWP set a measurement yields two numbers which are the settings of the polariser and analyser respectively when a zero, or null, magnitude of light is registered at the photomultiplier. The machine alters the polariser and analyser parameters to find sets of parameters for which a null results at the detector. The result of this measurement is a complex reflectance ratio, ρ, which can yield an amplitude constant, Ψ, and a phase difference, Δ.

$$\rho = tan(\Psi)e^{i\Delta} \tag{4.13}$$

Equation 4.13 demonstrates the relation between these parameters which must then be used in calculations to pull out numbers for the optical constants or, in this case, the film thickness.

Ellipsometry apparatus/conditions

A Rudolph Auto EL-IV null ellipsometer was used to measure specimens' film thickness which has 0.1 nm resolution and a measurement angle fixed at 70 °. The machine has three monochromatic sources of different wavelengths; the 632.8 nm source was generally used in the measurements in this work. The ellipsometer was calibrated daily with an Si calibration standard of precisely known thickness and refractive index. Specimens from a few millimetres to 4 inch wafers can be loaded and the method imparted no damage to specimens during the measurements. The general protocol during growth was to measure substrates pre-deposition using a program that assumes a single, transparent layer of set refractive index. This confirmed the presence and thickness of the native oxide before growth. A similar program was run after deposition and further measurements could be taken across the substrate surface to check the uniformity of the layer. The sensitivity of the machine proved to be vital in experimenting with new precursors; checking for

very slight growth after each of a series of parameter changes rather than having to grow an appreciable thickness of film which methods like weight gain measuring would necessitate.

4.2 Electrical measurements

Electrical measurements were performed on films to assess their capacitance-voltage (C-V), capacitance-frequency (C-f) and current-voltage (I-V) responses. From the C-V measurements a material's κ value can be extracted. MOS capacitor-like test structures were prepared from cleaved sections of substrate after deposition and annealing had taken place.

4.2.1 Electrical theory

Capacitance is the change in charge associated with a change in voltage. **C-V measurements** involve applying a DC bias across the test structure while making the capacitive current measurements with a 0.05 V AC signal. The AC voltage is of fixed magnitude and frequency while the DC bias is swept through a voltage range. It is the DC component that affects capacitance changes in the test structures and pushes the devices into the device modes typical of a MOS capacitor; accumulation, depletion and inversion (these were covered in the first chapter). As part of the measurement procedure a delay time is built in at each measurement voltage step as a MOS capacitor takes time to become fully charged at a given measurement voltage. If the gate bias is changed too quickly ($>\sim$100 mV/s) the equilibrium is not reached in the device leading to deep depletion. Figure 4.2 shows the shape of an ideal C-V measurement for a device built on a p-type substrate. The diagram is split into three sections that relate to the accumulation, depletion and inversion device regimes. At low frequencies the depletion regime results in high capacitance values as the test structures form quasi-capacitors of opposite plate polarity to that of accumulation. In a MOSFET, with its oppositely doped source and drain regions, the system has a ready injection from these areas of minority charge carriers. The concentration of minority carriers in a MOS, which is the device architecture of the test structures measured in this work, is limited by the speed

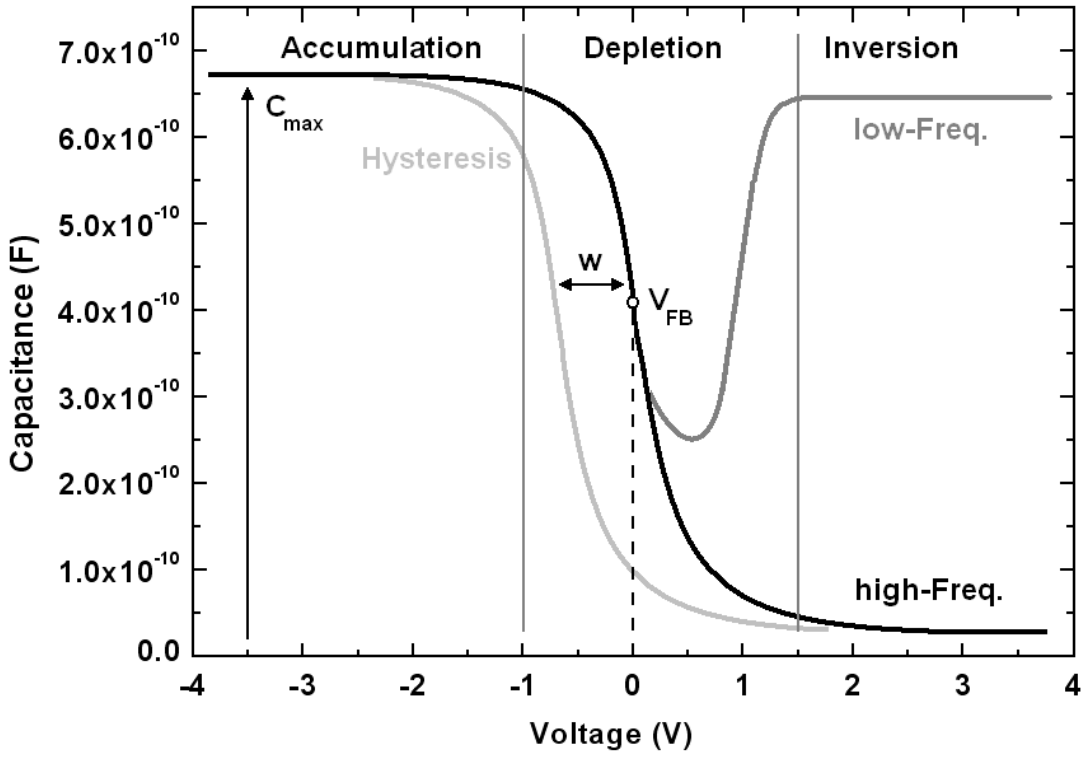

FIGURE 4.2: Example curve for capacitance-voltage (C-V) measurements.

at which minority carriers can be generated thermally at the interface[2] in the device mode of inversion. This places a frequency dependent limitation on the capacitance response when the device is in inversion (see figure 4.2 - dark grey and black curves). Due to this limitation the values for capacitance are extracted from the curves in the region of strong accumulation. The value taken from the chart, shown as C_{max} in figure 4.2, is the capacitance measurement for the whole test structure, including the interfacial layer from the substrate's native oxide. In order to calculate the capacitance of the dielectric material the value of C_{max} must be split into components that include the interfacial SiO_2 layer and the high-κ layer. Capacitances sum as reciprocals as demonstrated in equation 4.14.

$$\frac{1}{C_{max}} = \frac{1}{C_{SiO_2}} + \frac{1}{C_{high-\kappa}} \tag{4.14}$$

[2]The generations times for majority and minority carriers at a MOS interface are in the order of picoseconds and microseconds respectively [116].

Once the components from the SiO_2 and high-κ layers have been separated the value for C_k can be used to derive the permittivity, κ, from equation 4.15,

$$C_{high-\kappa} = \frac{\epsilon_0 \kappa A}{t_{high-\kappa}} \tag{4.15}$$

where ϵ_0 is the permittivity of free space (8.85×10^{-14} F/cm), A is the cross-sectional area of the quasi-capacitor structure through the film (using 0.3 mm as the diameter) and $t_{high-\kappa}$ is the thickness of the dielectric layer. The dark-grey/low-frequency curve in figure 4.2 has a representation of the threshold voltage, V_{th}, at its minima but this distinction is lost in the high-frequency curve with its lack of inversion response.

A number of charge phenomena relating to the deposition and heat treatment of thin

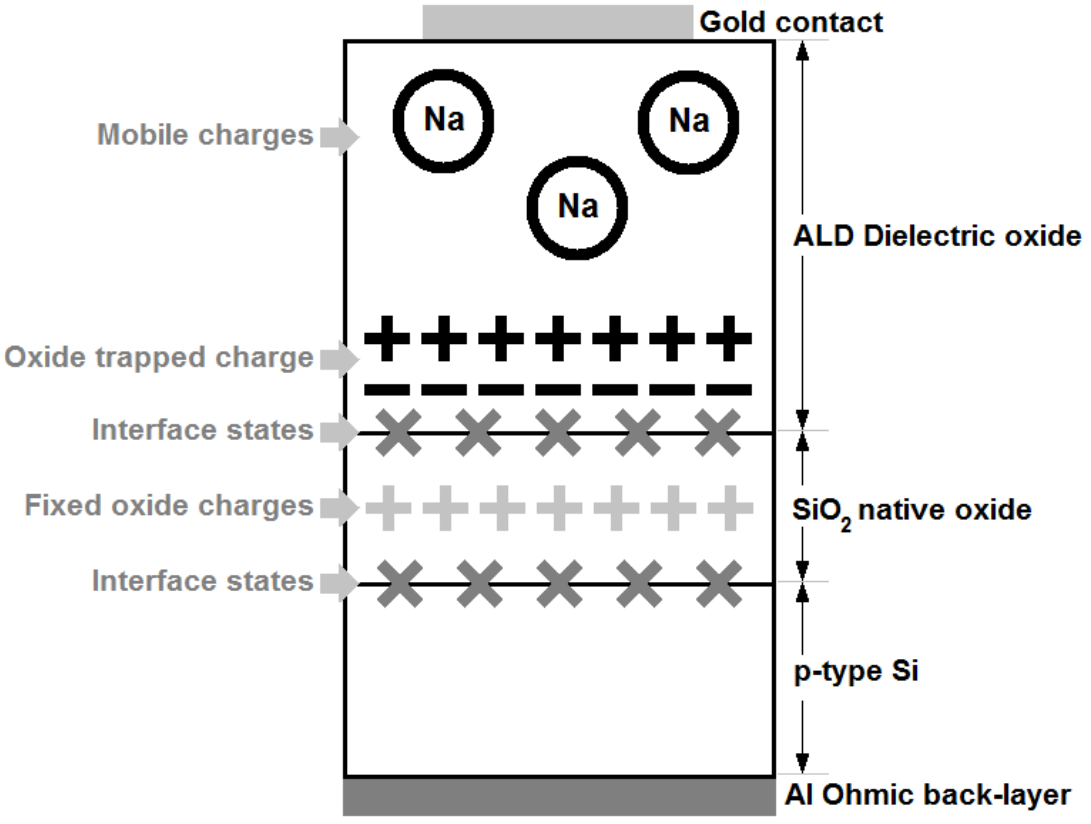

FIGURE 4.3: Schematic drawing of the test structures fabricated for electrical measurements on ALD dielectrics. The layers' thicknesses are not drawn to scale. Included and captioned on the left are the various forms of charge phenomena, also not to scale, that can exist in MOS capacitors as a consequence of fabrication or heat treatment effects. After [117]

films can affect subsequent electrical measurements. The types of charge and their positions relative to the MOS test structures used in the results chapters are shown schematically in figure 4.3. **Mobile charges** are ions in the lattice which diffuse into the oxide during deposition or heat treatment. It is frequently alkali ions that are considered problematic during MOS fabrication and so they are depicted in figure 4.3 as Na^+ ions in the dielectric oxide. The next type of charge in the diagram is **oxide trapped charge**. These charges are due to defects in the dielectric oxide and can be positive or negative depending on the type of defect and its electrical polarity. High-κ films have a much greater probability of high defect concentration compared to SiO_2 films. This is due to the ionic bonding character of the higher permittivity oxides and also their generally higher coordination compared to Si in SiO_2 [118]. SiO_2's low coordination makes it more likely that the network can re-bond and remove incomplete coordinations. In contrast the high-κ materials, with their higher coordination and ionic bonding character, tend to have a higher oxide defect concentration. High-κ oxides are poor glass formers and hence less able to re-bond and remove defects in the oxide network. Oxygen vacancies and interstitials in the lattice are the most commonly formed defect in high-*kappa* oxides. The effect of these types of defect in the lattice is to create charge states within the band gap of the material [119]. Oxygen vacancy defects can create charges states at an energy within the band gap of the substrate material [118]. The effect of mobile and oxide trapped charges in MOS test specimens is to provoke hysteresis in the up and down sweep of a C-V measurement.

SiO_2's low coordination (average $\sim$2.6 compared to HfO_2 $\sim$5.3 [118]), and covalent bonding character, means that its main defects are dangling bonds from incomplete atom coordination at the Si/SiO_2 interface. Electrically active defects at the Si/SiO_2 interface which form new energy levels within the band gap of the substrate are termed **interface states**. In our test structures there are two interfaces, the Si/SiO_2 and SiO_2/high-κ interfaces, which might both contribute interface states. Since these states have energies lower than the conduction band edge they can act as traps for electrons which would otherwise reside in the conduction band. The effect of these traps is to cause the carrier mobility to increase more slowly with gate voltage, which can be seen as a distortion in the shape of the C-V curve [120]. The last potential sources of charge in

the MOS test structure are **fixed oxide charges** which are trapped Si ions in the native oxide near the Si/SiO_2 interface. They occur as a result of deposition and annealing conditions. A positive fixed oxide charge shifts the C-V curve along the x-axis by an amount inversely proportional to the oxide capacitance [117].

Figure 4.4 shows the ideal shape of a **current density-field (J-E) measurement**. These curves have the same shape as current-voltage (I-V) curves and are readily produced from I-V measurements; J-E values are just the ones more often quoted/discussed in the literature. In the measurement procedure a 'staircase' voltage consisting of a fixed voltage step and delay time repeated up to a voltage limit were applied to the test structure. The resulting current response potentially contains components from any leakage current mechanisms; grain boundary leakage, F-N tunnelling and QM tunnelling. The dashed grey line in the figure represents a reading for J at -1 MV/cm; throughout the results sections values will be quoted in this way to make measurement-to-measurement comparisons.

4.2.2 Electrical apparatus/conditions

For the electrical assessment of dielectric materials, MOS capacitor test structures were fabricated utilising the material of interest as the insulating oxide. Gold film-side contacts were sputter coated onto the specimen surfaces through a precision mask. Figure 4.3 shows the layout of these test structures. The dots were circular with diameters of 0.3 mm. The specimens were then evaporation coated on their reverses with aluminium to form an Ohmic back-contact. The test structures form a quasi-capacitor structure with a cross-sectional area that equals the area of the gold dots; each gold dot can be thought of as a separate quasi-capacitor. As the Si substrate is a semiconducting material a capacitor is only formed with an applied bias across the structure. The charge carriers that collect under the dielectric oxide in accumulation or inversion effectively form the other plate of the capacitor.

C-V and C-f measurements were carried out using an Agilent E4980A precision LCR meter. Usually a C-V sweep is run between -1 V and 1 V to check that the specimen shows the expected switch between accumulation and depletion at $\sim$0 V that would be

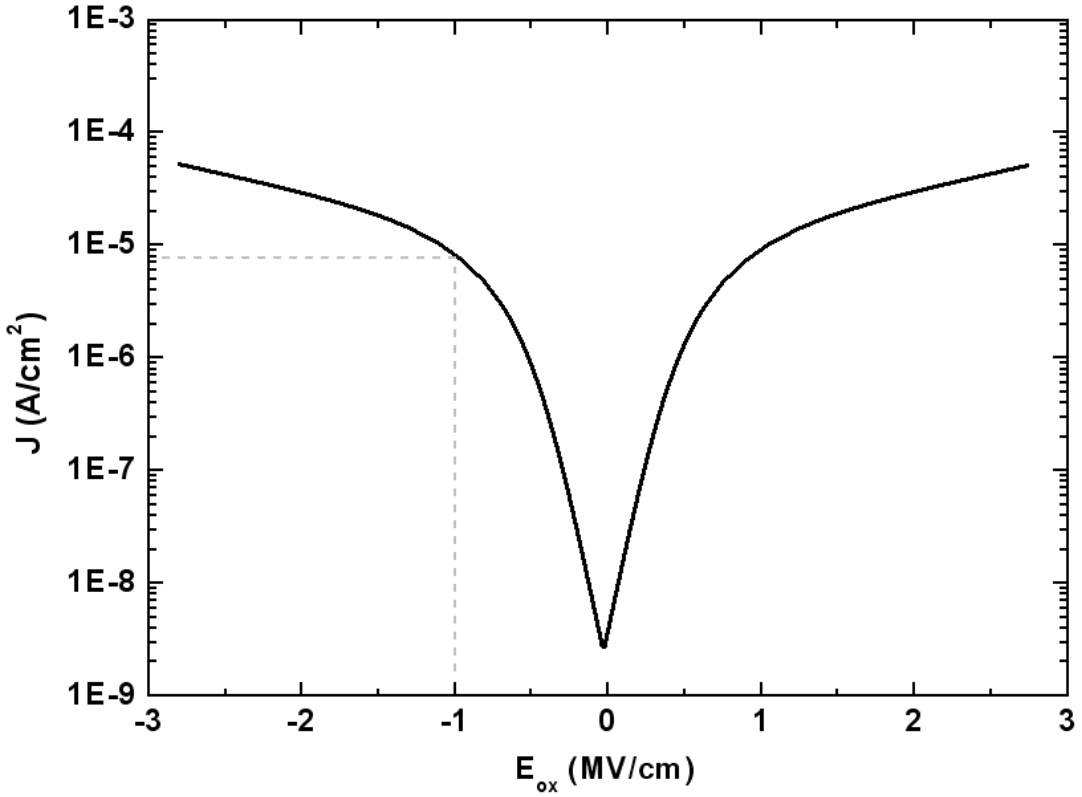

FIGURE 4.4: Example curve for current density-field (J-E) measurements. The dashed line demonstrates quoting a J value at -1 MV/cm.

expected from a functioning sample. A C-V run uses a 0.05 V DC current with an additional AC component swept across the voltage range specified. Subsequent experiments can be run to widen the voltage sweep while checking the specimen has not succumbed to breakdown. The C-V measurements are run for a designated frequency of applied voltage, a number of which are recorded to assess the character of the specimen across a range of frequencies: 10^6 Hz, 10^5 Hz, 10^5 Hz, 10^4 Hz and 10^3 Hz. C-f measurements use a set voltage and record the change in capacitance as the frequency of the applied voltage is altered, a few different voltages in the accumulation portion of the C-V response (-3.5 V to 0 V) are used. I-V measurements were performed using a Keithly 617 programmable electrometer and a Keithly 230 programmable voltage source. I-V measurements are set to run in two halves of the experimental voltage window, in the general case -3.5 V to 0 V and 0 V to 3.5 V. Once a set of measurements has been taken for a given dot more dots from the same specimen are assessed until 3–5 working measurements of each type can be compared.

Chapter 5

Results: HfO_2

5.1 Experimental rationale - HfO_2

The use of $HfCl_4/H_2O$ ALD in the MOSFET fabrication process has been in place since 2007 [1]. The key achievement was an EOT of 1 nm via a higher-κ material's introduction in the place of SiO_2. This meant that a physically thicker insulating layer was included with equivalent capacitance density to 1 nm thick SiO_2, leading to lower leakage current density by several orders of magnitude. As well as a HfO_2 dielectric layer it was necessary at the same time to implement a metal gate to negotiate the problems of 'soft' optical phonon degradation of carrier mobility associated with high-κ material integration [121, 122]. By 'soft phonon' we mean phonons that demonstrate negative frequency responses in the phonon frequency dispersion (see [123] for an example of the phonon frequency dispersion of cubic HfO_2 and the negative responses seen for certain sectors of the Brillouin zone). Such phonons are often linked directly to phenomena like phase transitions in materials. Unlike issues like interface trapped charges, which also affect the carrier mobility, the soft phonon scattering problem could not be addressed with adaptations in deposition and processing - hence a switch in production of both fabrication materials at once.

As hafnium oxide-based films are currently the industry standard dielectric thin film for nano transistor applications this chapter presents the deposition and analysis of HfO_2 thin films grown by ALD. These experiments provided both growth and categorisation data for ALD HfO_2 to help organise a doping strategy and also baseline electrical

measurements on HfO_2 films as benchmarks to assess the doped materials against.

5.2 HfO_2 deposition - OpAL®

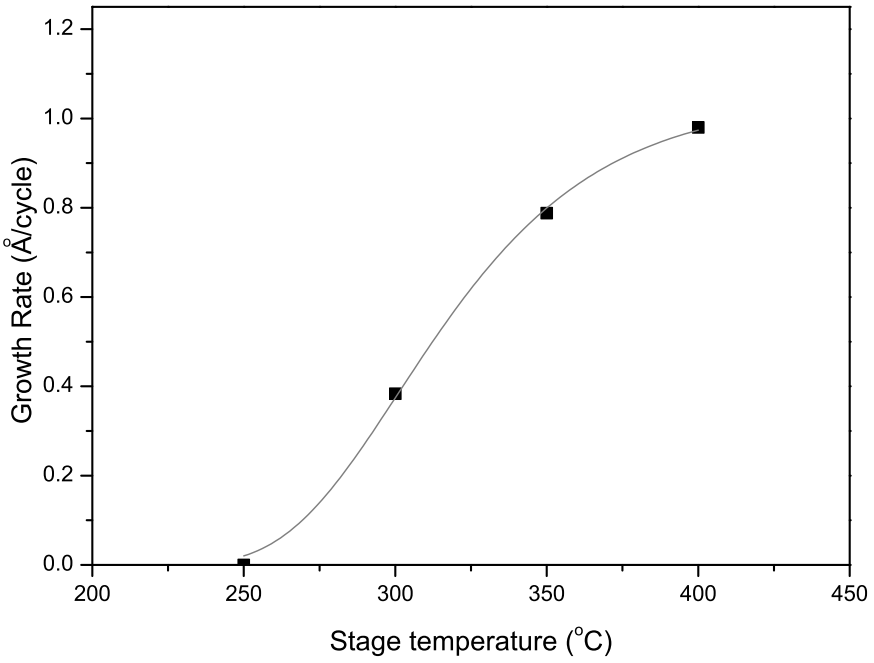

FIGURE 5.1: $(MeCp)_2Hf(OMe)(Me)/H_2O$ growth at different substrate temperatures.

Deposition experiments were carried out on the OpAL® reactor in thermal deposition mode. The substrates used for HfO_2 deposition were B-doped p-type Si (100) 4 inch wafers with a ∼2 nm native SiO_2 oxide on the surface as received. The hafnium precursor used was $(MeCp)_2Hf(OMe)(Me)$, heated to 100 °C, with H_2O, kept at room temperature, as the oxidant. Thin films of HfO_2 were deposited by ALD in the temperature range 250–400 °C using a 3 second pulse and 6 second purge to assess the growth rate by temperature. Figure 5.1 shows the growth rate of $(MeCp)_2Hf(OMe)(Me)$ in $\mathring{A}$/cycle over this temperature range. Negligible growth was obtained at 250 °C with the best deposition rates seen for ≥350 °C. These temperature figures are reasonable for cyclopentadienyl precursors via ALD [33]. Further deposition experiments were run at the deposition temperature of 350 °C altering the pulse length of the $(MeCp)_2Hf(OMe)(Me)$ in the recipe. Figure 5.2 presents growth rate of $(MeCp)_2Hf(OMe)(Me)$ in $\mathring{A}$/cycle over

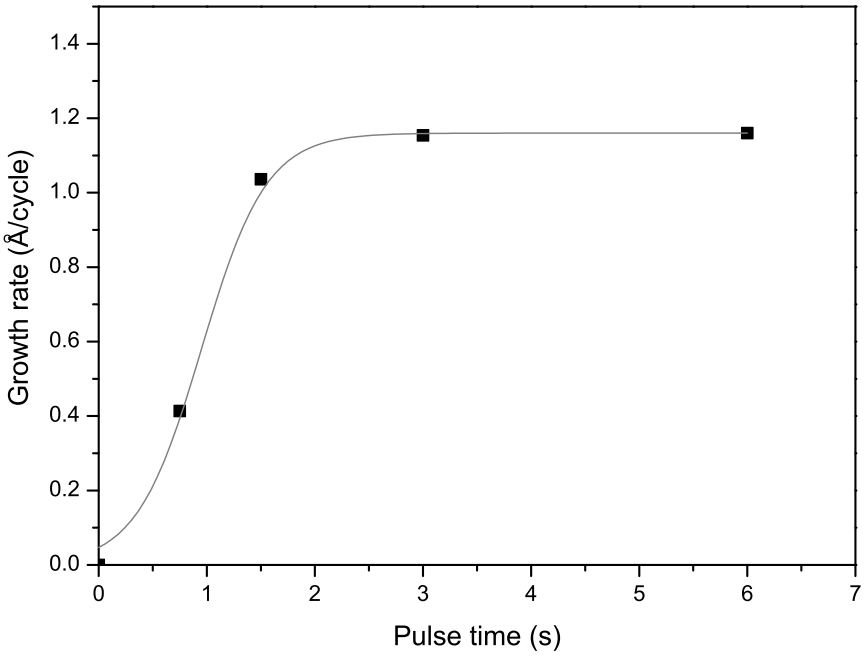

FIGURE 5.2: $(MeCp)_2Hf(OMe)(Me)/H_2O$ growth at 350 °C with different pulse lengths.

a range of pulse lengths from 0.8–6 seconds. There is a plateau in growth rate between 1.5–6 seconds suggesting self-limiting growth has been achieved. In the following characterisation sections the ∼100 nm films were grown at 350 °C whereas the ∼10 nm films were grown at 300 °C in order to give a direct comparison to the Ti-HfO_2 specimen set discussed in the next chapter.

5.3 HfO_2 characterisation

5.3.1 XRD

For structural characterisation of the HfO_2 films, thicker deposition specimens were grown, cleaved from the wafers and subjected to N_2-atmosphere anneals for 30 minutes at temperatures between 600 °C and 1000 °C. Figure 5.3 presents XRD measurements performed at 0.05 °/minute in the range 25–45°, the traces have background removed and are set arbitrarily apart in the y-axis. These measurements can be compared with figure 5.4 which shows similar measurements run on the specimen set used in subsequent

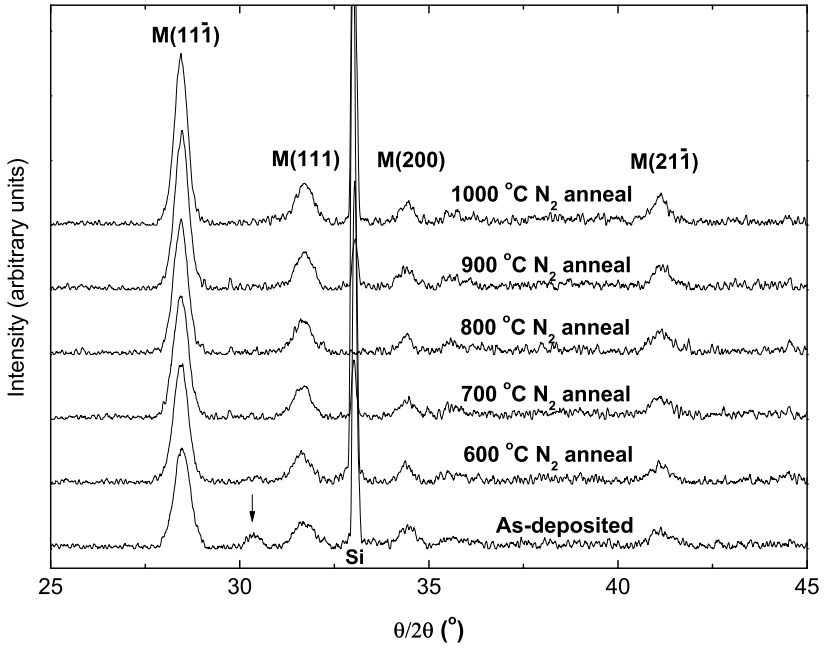

FIGURE 5.3: XRD measurements for ∼100 nm HfO_2 films after standard anneals at five temperatures. In the highest-temperature trace the monoclinic planes are indexed. The large peak at ∼33 ° is from the Si substrate. The arrow indicates a plane not expected for the monoclinic phase.

electrical measurements. The planes indexed are those expected for the monoclinic polymorph of HfO_2 [96] and the large peak at ∼33 ° is from the Si substrate. A slight peak can be seen in the as-grown measurement at ∼31 ° (arrowed) which suggests the as-grown films might have some mixed level of crystallinity with some tetragonal/orthorhombic character in a mostly monoclinic HfO_2 film [96]. As can be seen from the figure the as-grown specimen displayed the crystalline form without heat treatment and the films stay in monoclinic crystallinity over the full temperature range; the slight sharpening of the peaks towards the upper end of the scale could be due to grain growth at the higher temperatures. Grain growth is driven by a reduction in energy associated with reducing the grain boundary surface area in the films. This grain growth potentially has repercussions on subsequent electrical measurements; grain boundaries being lower resistance current paths through the films than conduction through the film bulk. The M(11$\bar{1}$) reflection at ∼28 ° is the strongest peak in the pattern across the heat treatment range suggesting that the films have a (11$\bar{1}$) texture, a preferential ordering for (11$\bar{1}$)

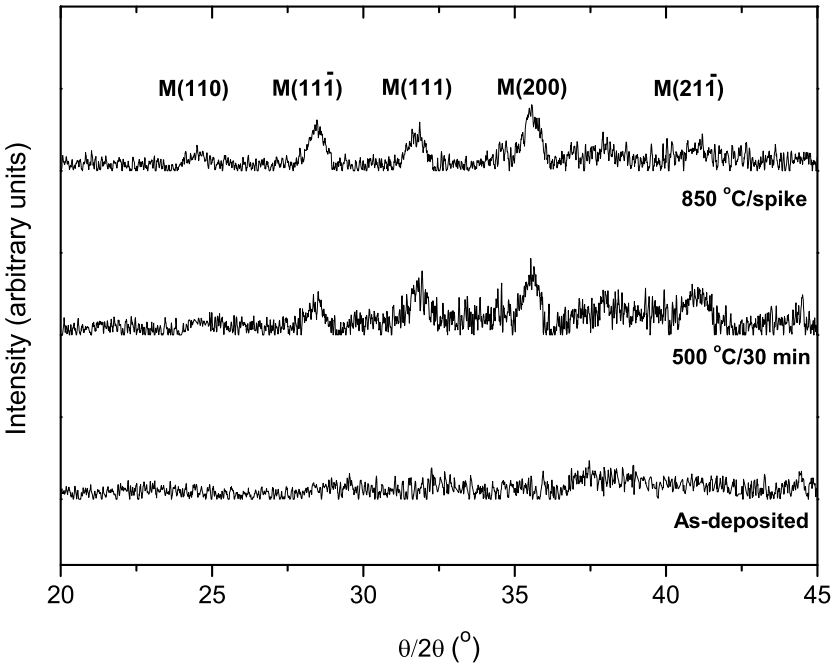

FIGURE 5.4: XRD measurements for ∼10 nm HfO_2 films after the gate-first and gate-last anneals in N_2. In the highest-temperature trace the monoclinic planes are indexed. The background signal is removed from the traces for clarity.

crystallites, as-grown and after annealing. This type of crystallographic ordering in ALD HfO_2 films has been noted before [34] though other orderings have been seen including preferential ordering on (111) at the expense of (11$\bar{1}$) [32]. The measurements made on the electrical specimen set in figure 5.4 show an as-deposited trace with no diffraction peaks and monoclinic diffraction peaks for the two anneals. In these thinner films the XRD patterns are much weaker than in the ∼100 nm film set used in figure 5.3.

5.3.2 Raman spectroscopy

Figure 5.5 shows Raman spectroscopy measurements, made on the same specimens as the XRD in figure 5.3, using the 325 nm UV laser source. The traces were taken between 150 cm^{-1} and 1250 cm^{-1} and each time a 30 second acquisition time was used with two acquisitions taken to remove spikes from cosmic radiation by comparison. The huge peak at ∼520 cm^{-1} and the modes seen in the 600–1100 cm^{-1} range are the first and second order Si modes from the substrate. Many of the Raman spectra discussed in this

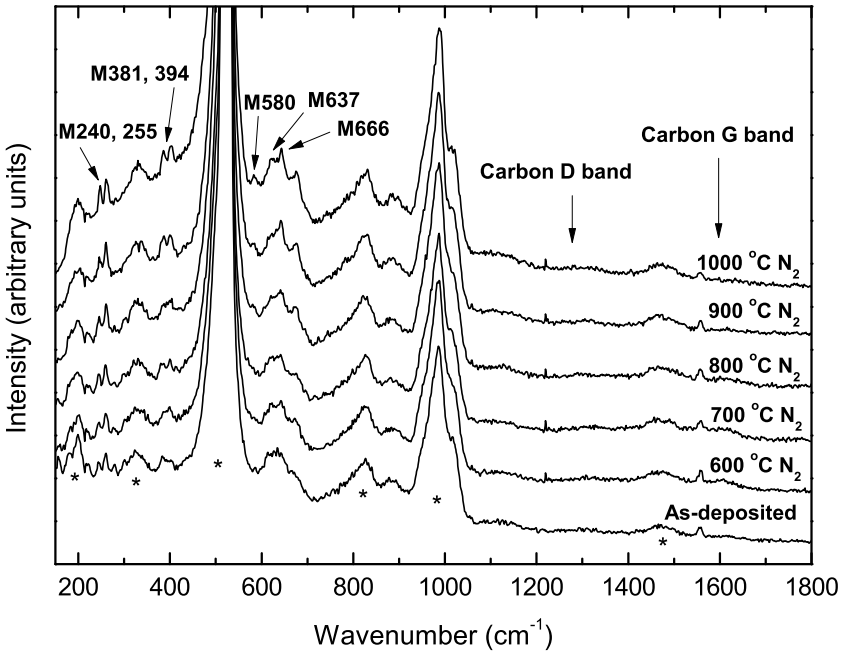

FIGURE 5.5: UV Raman measurements for ∼100 nm HfO_2 films after standard anneals in N_2 at five temperatures. In the highest-temperature trace the monoclinic phonon modes are indexed. The asterisks denote 1st and 2nd-order Si modes.

thesis will have these silicon contributions present. The strong feature at 520 cm^{-1} is the first-order, triply degenerate traverse optical phonon (TO). Other features asterisked in figure 5.5 are second-order modes; the 2TA (∼300 cm^{-1}), 2LA (∼600 cm^{-1}), 2LO (∼800 cm^{-1}) and 2TO (∼1000 cm^{-1}) bands respectively [124]. The measurements are un-altered other than arbitrary offsets in the y-axis. The seven modes highlighted are those expected for monoclinic HfO_2; a competitively weak Raman signal and hence the peaks are only clear in the higher temperature, more crystalline traces shown. No peaks were seen in the measurements representing the D and G carbon modes at ∼1300 cm^{-1} and ∼1600 cm^{-1} respectively which would have indicated carbon inclusion in the films during the deposition or annealing processes. This result suggests that the monoclinic Raman response is relatively weak; no useful Raman measurements could be taken for HfO_2 films of 10 nm thickness. Accounting for all the modes developed during the annealing means the films are unlikely to have suffered much in the way of oxygen vacancy formation which would have shown up as a broad mode developing in

the 600–700 cm^{-1} wavenumber range.

5.4 HfO_2 electrical measurements

Further specimens were cleaved and subjected to the 850 °C/spike and 500 °C/30 min annealing regimes outlined in chapter 3. After this they, and an as-deposited specimen, were prepared for electrical examination by evaporation coating an Al ohmic contact on their reverse and mask-sputter coating Au contacts on the film surface as described in chapter 4.

5.4.1 C-V

Figure 5.6 shows C-V measurements made on the prepared HfO_2 specimen set at 100 kHz. The curves display typical accumulation, depletion and inversion responses for a MOS capacitor grown on a p-type substrate. The films subjected to heat treatments show a reduction in their maximum capacitance, where the curves meet the y-axis,

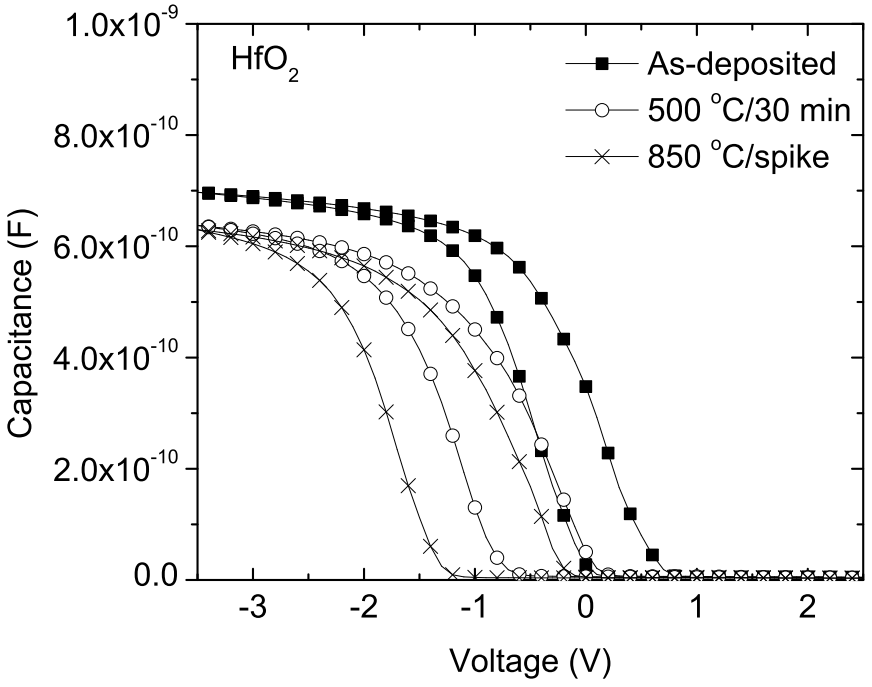

FIGURE 5.6: C-V measurements performed at 100 kHz for ∼10 nm HfO_2 films as deposited and after the 850 °C/spike and 500 °C/30 min anneals.

compared to the as-deposited specimen. This reduced capacitance corresponds to a reduced κ via the relationship in equation 4.15. The value for κ falls from 17 for the as-deposited specimen to ∼14 for the annealed specimens. A κ of 17 fits well with the values reported in the literature [97, 99]. There is a horizontal shift in the curves for the annealed specimens compared to the as-deposited specimen. This shift along the voltage axis is a result of trapped positive charges in the oxide incorporated during the heat treatment. The charges are positive as the corresponding shift is in the negative voltage direction. The hysteresis displayed in the sweeping measurements relates to mobile ionic charges in the films. The relative increase in hysteresis shown in the 850 °C/spike curve suggests more of these mobile ionic charges are incorporated into the films during the higher temperature, faster annealing method.

5.4.2 J-E

Figure 5.7 presents leakage current density measurements over a range of voltages for the same HfO_2 materials set. Taken from the graph at -1 MV/cm the three specimens have very similar values for leakage current density, $\sim 1.5\times10^{-7}$ A/cm^2, but at -2 MV/cm the 850 °C/spike specimen displays a clear increase in leakage compared to the as-deposited and 500 °C/30 min specimens: 1.09×10^{-6} A/cm^2 compared to $\sim 3\times10^{-7}$ A/cm^2 respectively. Reported leakage current density for HfO_2 varies enormously depending on deposition method and post-deposition treatment as well as the specific V/cm value quoted for. An offset of -0.27 MV/cm can be seen where the curve switches polarity at $\sim 10^{-9}$ A/cm^2. This relates to built-in charge in the MOS test structure, demonstrating that the flatband condition is not at zero applied volts.

The structure of the HfO_2 films can go some way to explaining the subsequent electrical measurements. Figure 5.3 showed that the as-deposited HfO_2 specimen had a peak at ∼31° suggesting some tetragonal/orthorhombic phase present as well as the monoclinic phase. This peak is barely visible in the 600 °C trace in the figure and is absent in the higher temperature anneals. From this observation the higher capacitance, and hence κ, value measured for the as-deposited sample is most likely due to some contribution from a higher permittivity phase like tetragonal HfO_2 being present in the film. After the different heat treatments the films are entirely monoclinic. The widening

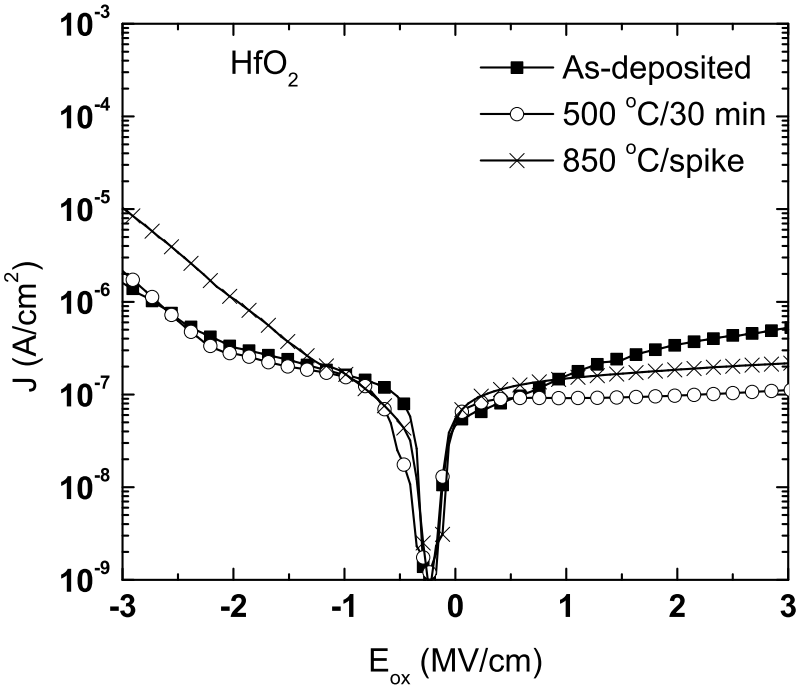

FIGURE 5.7: J-E measurements for ∼10 nm HfO_2 films as deposited and after the 850 °C/spike and 500 °C/30 min anneals.

in the 850 °C/spike trace's hysteresis suggests the faster annealing regime results in near-interfacial trapped charges in the specimen. The similarity in the leakage current density measurements in figure 5.7 suggest that the grain boundary volume through the films doesn't change significantly. This correlates with only slight sharpening seen in the XRD peaks seen in figure 5.3. Whether the higher leakage current density seen for the 850 °C/spike film measured at -2 MV/cm is related to the higher-anneal-temperature texture change seen in the higher intensity of the M($11\bar{1}$) plane in the XRD or in an effect from the difference between the annealing regimes is difficult to isolate.

5.5 Chapter summary

HfO_2 films have been prepared by thermal ALD using $(MeCp)_2Hf(OMe)(Me)$ at 100 °C and H_2O at room temperature. XRD and Raman measurements show the films have ($11\bar{1}$)-textured monoclinic crystallinity in the heat treatment ranges studied. The thicker (∼100 nm) films analysed were crystalline as-deposited, with the thinner films

either amorphous or too thin to glean structural data from. The permittivity at 100 kHz (17) and leakage current density values ($\sim 10^{-7}$ A/cm^2) measured are similar to the reported values in the literature.

Chapter 6

Results: Ti-HfO_2

6.1 Experimental rationale - Ti-HfO_2

As HfO_2 has been implemented in the fabrication of MOSFETs the challenge now is to improve and develop the dielectric materials system to continue the downscaling of MOSFET-based devices. One way to do this is to include additional elements in a HfO_2-based film and monitor the potential changes to film composition, morphology and dielectric response. The step-wise technique of ALD is ideal for precision control of proportions in a mixed oxide system. This chapter describes the inclusion of titanium in a hafnium oxide-based material in order to assess the effects on the physical structure and dielectric response of the films. The first section briefly describes some TiO_2 film deposition and characterisation and the second section describes the deposition and analysis of $Ti_xHf_{1-x}O_\delta$ films of varying composition.

The titanium oxide polymorphs trialled as dielectric films in the literature all demonstrate a relatively high dielectric constant but the material has a conduction band offset with silicon meaning its integration in silicon-based devices results in high leakage current density. The calculated conduction band offset between TiO_2 and Si is 0.05 eV, compared with 1.5 eV for HfO_2 and Si [125]. A band offset of at least 1 eV is necessary to prevent conduction of charge carriers by Schottky emission[1]. A consequence of the Schottky effect is that otherwise promising dielectric materials are limited in usefulness due to insufficient band offset - for example $SrTiO_3$ has been reported to have a κ value

[1]Enhanced thermionic emission of charge carriers operating in an electric field range ($<10^8$ Vm^{-1}) below the charge range in which F-N tunnelling becomes a significant contributed to leakage current

of ∼475 at 100 kHz [126] but its band gap of 3.2 eV on a Si substrate of band gap 1.1 eV makes it improbable that the bands can be arranged symmetrically enough to provide the necessary ∼1 eV offset at valance and conduction band.

6.2 TiO_2

6.2.1 TiO_2 deposition - OpAL®

TiO_2 samples were deposited via thermal ALD using the OpAL® reactor. The precursors were Ti(^{i}OPr)$_4$ heated to 50 °C and water kept at room temperature. The substrates used were boron-doped p-type Si(100) with a ∼2 nm native SiO_2 on the surface. Stage temperatures of 250 °C, 300 °C and 350 °C were trialled to assess the precursor's deposition in the temperature range in which the hafnium precursor functioned in the previous results chapter. Some TiO_2 growth data is included in the Ti-HfO_2 deposition section of this chapter. TiO_2 films deposited by ALD at 350 °C were analysed to

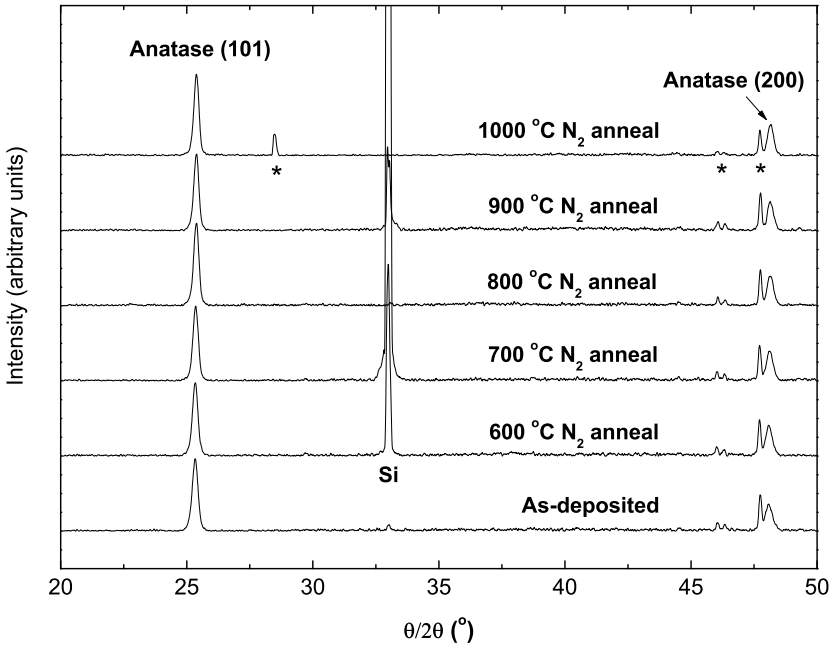

FIGURE 6.1: XRD measurements for ∼60 nm TiO_2 films as-deposited and after standard anneals at five temperature. Two anatase peaks are indexed. The large peak at ∼33 ° is from the Si substrate. The asterisks mark noise peaks from the apparatus.

determine structural information. These deposition runs used a Ti(^{i}OPr)$_4$ pulse/purge of 3 s/6 s and a water pulse/purge of 20 ms/10 s.

6.2.2 TiO_2 characterisation

XRD

Figure 6.1 shows XRD measurements for a ∼60 nm TiO_2 film as-deposited and after annealing at different temperatures in N_2 in the tube furnace. The two peaks highlighted are consistent with the anatase titania phase [127]. The plot demonstrates that the as-deposited specimen was crystalline and there is very little change in the traces with increasing temperature. This points to anatase being the equilibrium phase from the growth temperature up to a 1000 °C anneal condition for deposition with this precursor. The lack of any shifts in $\theta/2\theta$ peak position and only a slight sharpening in the peaks themselves suggests little in the way of grain growth during the annealing.

Raman spectroscopy

The tetragonal anatase form of titanium oxide has symmetry D_{4h}^{19} leading to the normal modes A_{1g}+2B_{1g}+3E_g to be present in Raman spectroscopy measurements. Figure 6.2 presents UV Raman measurements for the same annealed TiO_2 specimens used in the XRD plots in figure 6.1. The various phonon modes associated with the anatase structure are highlighted in the figure [128]. The first E_g mode is expected to be a much stronger signal than the others in anatase but is cut off here by the notch filter which limits the UV Raman low wavenumber region to >190 cm^{-1}. This plot confirms that anatase is the only phase present in these films in the temperatures regime assessed and that there is little in the way of peak shifting/sharpening that might suggest grain growth or lattice strain. What the XRD and Raman data show is that ALD deposition with Ti(^{i}OPr)$_4$ readily forms crystalline TiO_2 as-deposited and that the films are stable during subsequent heat treatment. This fits well with previous reports that find ALD TiO_2 via Ti(^{i}OPr)$_4$ to crystallise at deposition temperatures >180 °C [129]. There was some evidence of carbon inclusion with the carbon D and G bands highlighted in the Raman plots. 0.5 at.% carbon has been reported before as an impurity in CVD TiO_2 [130] and attributed to residual carbon from precursor decomposition. Certainly the

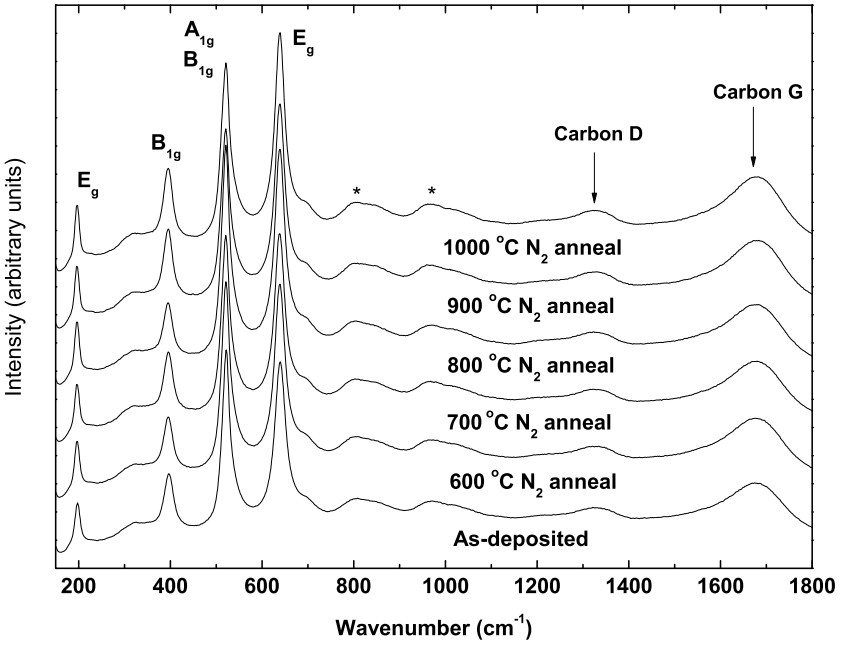

FIGURE 6.2: UV Raman measurements of ∼60 nm TiO_2 ALD films as-deposited and after standard anneals at five temperatures. The Phonon modes associated with anatase are indexed. The asterisks denote substrate contributions.

carbon indicated in figure 6.2 is not a result of the annealing process but incorporated during deposition at a substrate temperature of 350 °C.

6.2.3 TiO_2 Dielectric properties

Electrical measurements were not performed on TiO_2 films; there are several examples of TiO_2 thin film dielectric experiments in the literature [130–132]. CVD TiO_2 is reported to demonstrate a frequency-dependent κ, in the rutile and anatase polymorphs, which becomes almost constant at high frequencies ($>10^4$ Hz). The high frequency plateau coincides with the dielectric response from the polarisability of bulk TiO_2. Although TiO_2 can register very high κ values the main issue with it as a dielectric in MOSFET devices is its low band gap and hence unsuitable band off-set with a Si substrate as discussed at the beginning of this chapter.

6.3 Ti-HfO_2

6.3.1 Ti-HfO_2 deposition - OpAL®

Ti-doped HfO_2 films were deposited on the OpAL® reactor in thermal deposition on p-type Si(100). The plan was to deposit films of two nominal thicknesses, in a range of compositions to assess the effect on the material's dielectric response. Table 6.1 lists the reactor parameters utilised after initial experiments with the precursors used for Ti-HfO_2 deposition. The variation in the growth rate with deposition temperature is shown in figure 6.3 for the growth of TiO_2 and HfO_2. The optimum substrate temperature for TiO_2 deposition was found to be 250 °C. At this temperature a growth rate of 0.17 $\AA$/cycle was achieved. On increasing the precursor pulse duration, and hence the amount of precursor added to the system, the growth rate per cycle did not increase once the saturation point was reached at a 2 s duration. This confirms that the growth

TABLE 6.1: OpAL® reactor parameters for depositing $(MeCp)_2Hf(OMe)(Me)$ and $Ti(^iOPr)_4$ at a substrate temperature of 350 °C

$Ti(^iOPr)_4$ bubbler temp.	50 °C
Ar bubbler	300 sccm
Ar purge	200 sccm
pulse	3 s
purge	6 s
$(MeCp)_2Hf(OMe)(Me)$ bubbler temp.	130 °C
Ar bubbler	300 sccm
Ar purge	200 sccm
pulse	3 s
purge	6 s
H_2O pulse	20 ms
H_2O purge	10 s

was behaving in a true ALD fashion. Increasing the temperature to 300 °C and 350 °C substantially increased the growth rate suggesting that the precursor had started to thermally decompose or a CVD-type component of growth was contributing to the deposition. The non-saturative nature of growth rate with pulse length is illustrated in figure 6.4, for TiO_2 grown at 350 °C. For the HfO_2 growth the $(MeCp)_2Hf(OMe)(Me)$ precursor failed to grow at a substrate temperature of 250 °C. Optimal growth occurred at deposition temperatures ≥350 °C. A nearly saturative growth rate with

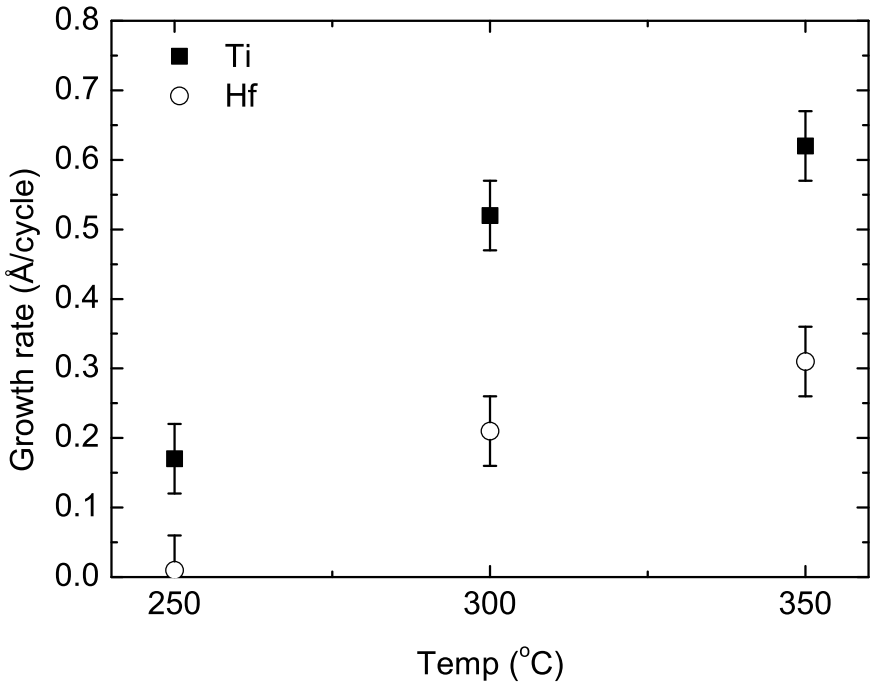

FIGURE 6.3: Deposition rates as a function of temperature for the two precursors in the Ti-HfO_2 series.

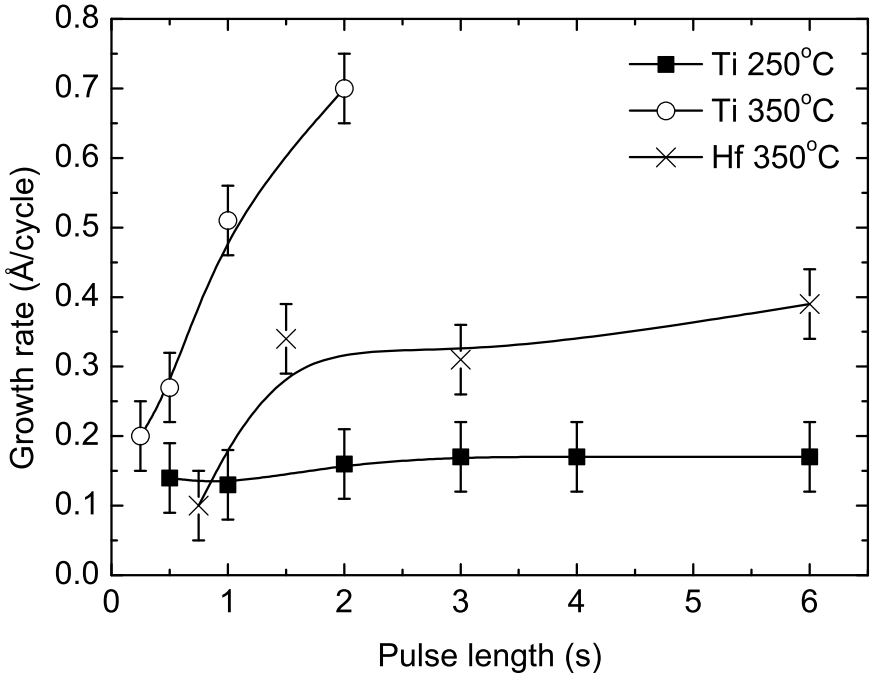

FIGURE 6.4: Deposition rates with changing pulse length for the two precursors in the Ti-HfO_2 series.

pulse length is illustrated in figure 6.4. For the $Ti_xHf_{1-x}O_{2-\delta}$ film deposition, a compromise deposition temperature of 300 °C was used. At this temperature neither the $(MeCp)_2Hf(OMe)(Me)$ growth or $Ti(^iOPr)_4$ growth is optimised. There is a small CVD component for the $Ti(^iOPr)_4$ growth and a sub-optimal HfO_2 growth rate. To create the different compositions different ratios of Ti and Hf pulses were used in a sequence of N[A(Ti/purge/H_2O/purge) + B(Hf/purge/H_2O/purge)], where N, A and B are integers. Based upon the growth rates at 300 °C which are 0.52 $\AA$/cycle and 0.21 $\AA$/cycle for the $Ti(^iOPr)_4$ and the $(MeCp)_2Hf(OMe)(Me)$ respectively, the ratio of precursor pulses was altered to try to obtain a 10% and 50% Titanium doping level. A composition of $Hf_{0.5}Ti_{0.5}O_2$ has been reported as the optimum dielectric response in density functional theory calculations [133]. The 10% titanium films were grown using a process of 23 Hf pulses to 1 Ti and the 50% titanium by 5Hf : 2Ti. Different numbers of overall ALD cycles were used to produce nominally 11nm and 6nm films of 10% and 50% Ti. 50 and 30 ALD cycles were used to produce the 50% Ti samples and 20 and 12 ALD cycles were used for the 10% Ti samples.

XRD

6.3.2 Ti-HfO_2 characterisation

Figure 6.5 shows the XRD patterns from the thickest 10% and 50% Ti films as-deposited, after the 500 °C/30 min and 850 °C/spike anneals. Both the as-deposited films show no diffraction features suggesting that they are amorphous. Diffraction patterns from both the annealed 10% samples show diffraction features at 24.9°, 28.7°, 32.0°, 35.8° and 41.4°. These features correspond to the monoclinic phase of HfO_2 [ICDS 6-318 34-104 43-1017] with a slight shift of approximately 0.3° due to a distortion of the lattice with the inclusion of the smaller Ti atom. With both types of annealing, the 50% Ti films remain amorphous. The retention of an amorphous microstructure has important consequences on the leakage current of the films as grain boundaries act as leakage current pathways in high-κ films. One concern was that due to an apparent growth rate limiting effect apparent with the Ti precursor inclusion (see MEIS data) the films were just too thin for the diffractometer to analyse. In order to alleviate these concerns further XRD scans were run on thicker specimens of various compositions (as

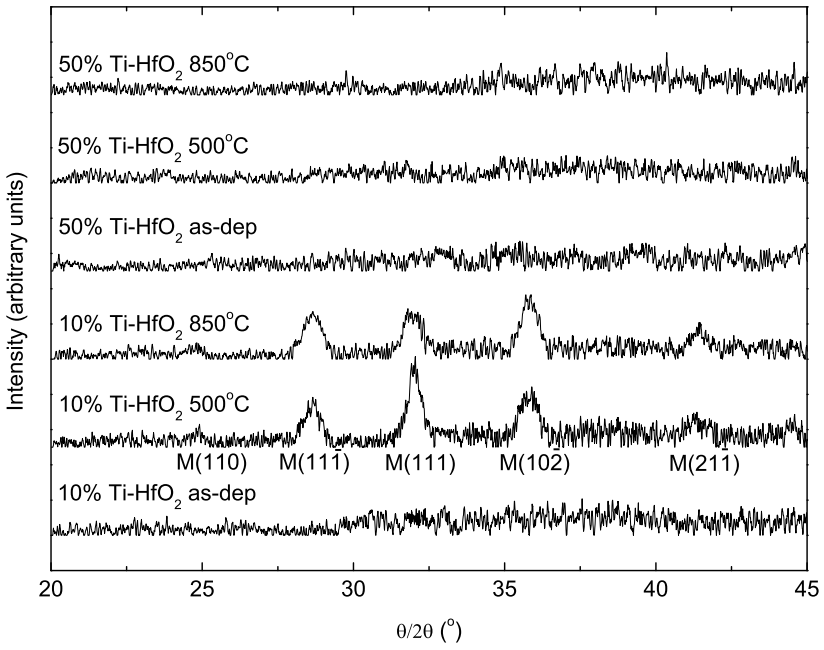

FIGURE 6.5: XRD measurements of $Ti_{0.1}Hf_{0.9}O_2$ and $Ti_{0.5}Hf_{0.5}O_2$ ALD films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals. The background has been subtracted from the raw data.

well as a TEM specimen being made from a critical sample, figure 6.11). Figure 6.6 presents XRD measurements performed on Ti-HfO_2 ALD films of a variety of doping levels after standard anneals at 500 °C. The films are all ∼12 nm from ellipsometry measurements. An undoped HfO_2 film is at the top of the figure with four monoclinic diffraction peaks indicated. The monoclinic character in the films appears to reduce in the 15%Ti specimen and for Ti additions ≥30%Ti the specimens display an amorphous structure. This demonstrates Ti acting as a network modifier when enough is added proportionally to the material.

Raman spectroscopy

Raman measurements for the $Ti_{0.5}Hf_{0.5}O_2$ specimen set annealed in N_2 for 30 minutes at various temperatures are presented in figure 6.7. The traces show the development of four modes which are highlighted in the top curve in a much longer measurement (120s acquisition time, 5 acquisitions). These four modes are similar to those attributed to

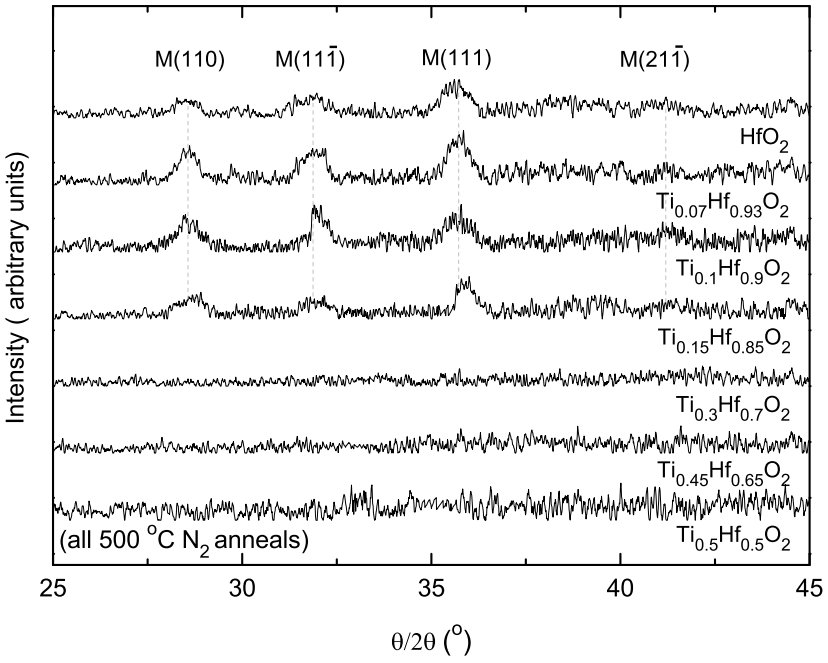

FIGURE 6.6: XRD measurements of ∼12 nm Ti-HfO$_2$ ALD films with different Ti addition levels after standard anneals at 500 °C. The background has been subtracted from the raw data.

HfTiO$_4$ in a 50:50 Ti:Hf material [134]. The modes seen for annealed monoclinic HfO$_2$ in figure 5.5 do not appear in this plot and the modes seen in this plot did not develop for HfO$_2$ films or the Ti$_{0.1}$Hf$_{0.9}$O$_2$ composition. This data would suggest that the film stoichiometry is in the ∼50:50 Ti:Hf proportion but that there is limited crystallinity present; only the long scan of the 1000 °C material had a convincing peak-set in it. Raman measurements on the 850 °C/spike and 500 °C/30 min annealed specimens (not shown) revealed no peaks. The 500 °C/30 min anneal is too low in temperature in comparison to the temperature for which peaks were seen in figure 6.7 and the spike anneal used for the electrical measurement specimens may be too quick an annealing regime to develop the crystalline phase. For clarity of the four highlighted modes the x-axis is limited to 900 cm^{-1} but the traces showed no sign of the carbon D and G bands seen for 350 °C-deposited TiO$_2$ in figure 6.2. This suggests that the appearance of carbon was due to a decomposition mechanism which is alleviated by conducting deposition at the lower temperature of 300 °C.

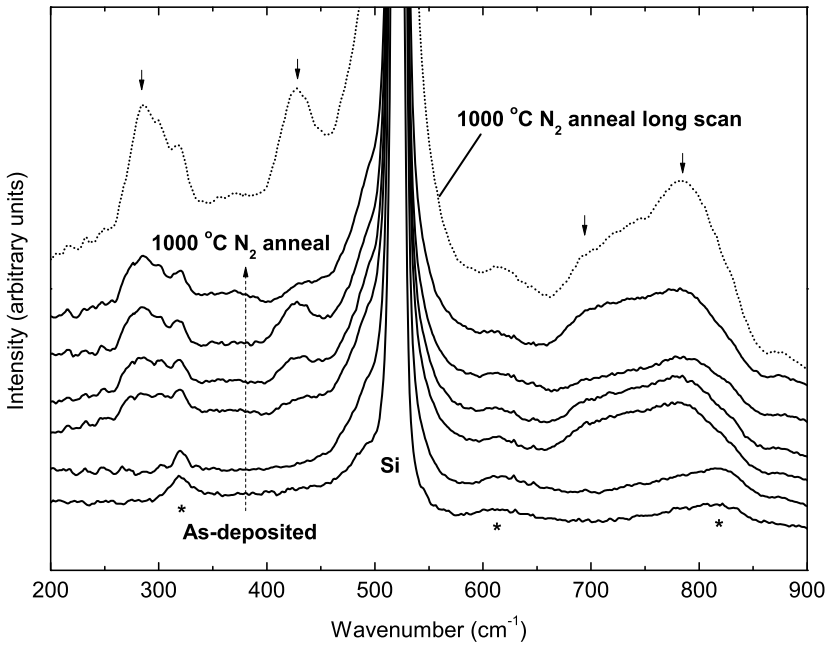

FIGURE 6.7: UV Raman measurements for $Ti_{0.5}Hf_{0.5}O_2$ samples as-deposited and after standard anneals at five temperatures. The asterisks denote substrate contributions.

MEIS

MEIS energy spectra for the two different compositions are given in figure 6.8 for nominally 6 nm and 11 nm thick films. The spectra contain peaks from He^+ ions that are scattered off Hf, Ti, Si and O atoms. Elastic energy loss processes in the collisions between the He^+ ions and target atoms results in the energy of the ions scattered off different atoms occurring at different positions on the energy spectra. The widths of the peaks relate to the thickness of the layer due to inelastic energy loss processes [135]. MEIS energy spectra can be converted into elemental depth profiles to accurately extract the film thicknesses. The intensity of a peak is related to both the scattering cross section for the ion/atom collision and the amount of atoms present in the sample. Integration of the area under the peak can be used to provide information on the composition. Integration of the Ti and Hf peaks shows that the desired composition was obtained for both the $Ti_{0.1}Hf_{0.9}O_2$ and $Ti_{0.5}Hf_{0.5}O_2$ Ti sample sets. From the energy

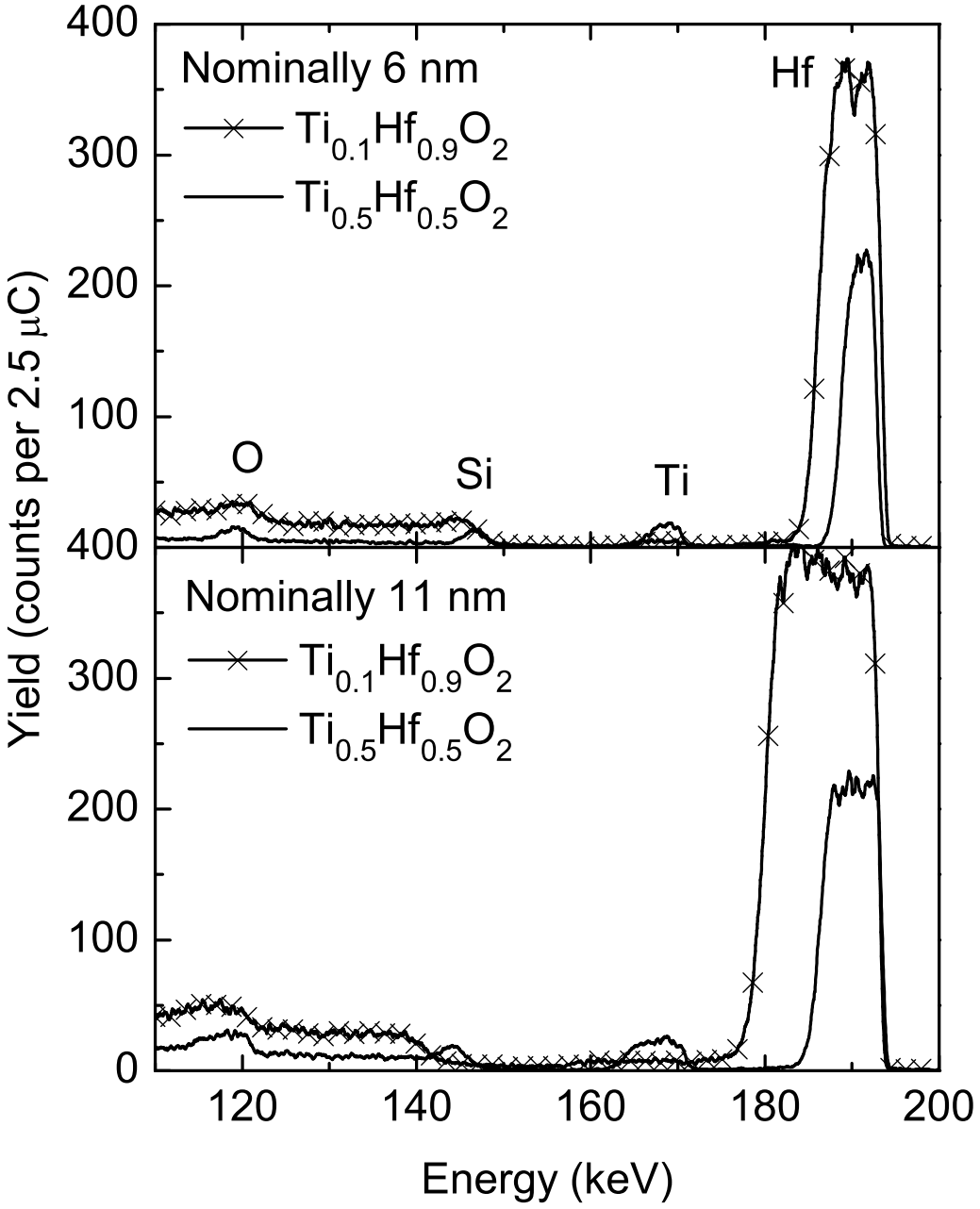

FIGURE 6.8: MEIS energy spectra for nominally 6 nm and 11 nm Ti-HfO$_2$ films.

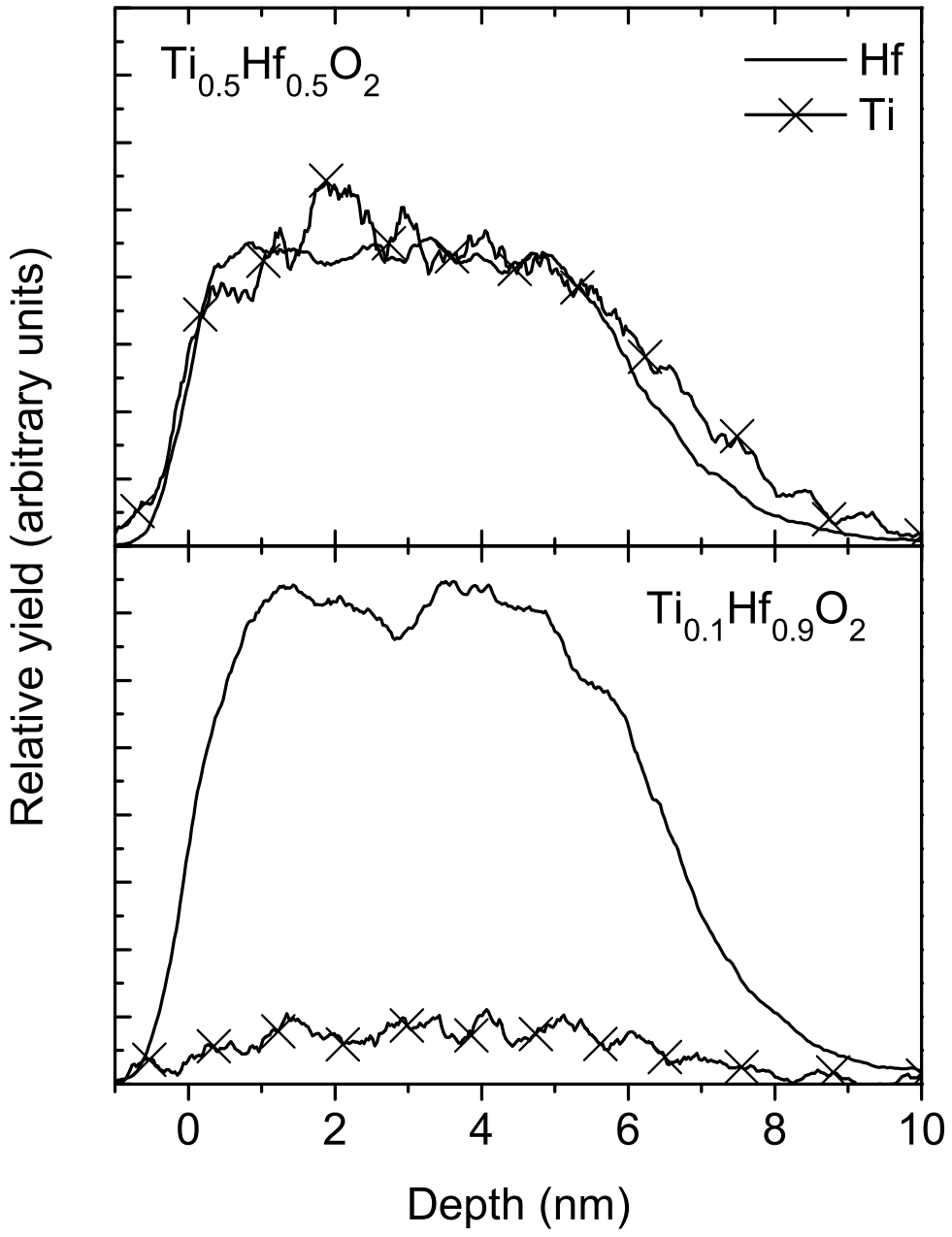

FIGURE 6.9: Ti and Hf MEIS depth profiles from 6.7 nm $Ti_{0.1}Hf_{0.9}O_2$ and $Ti_{0.5}Hf_{0.5}O_2$ composition films.

range of the peaks in figure 6.8 and the calibrated profiles, it is clear that the thicknesses of the layers in the 10% samples are very close to the nominal values. The thicker film is 12 nm and the thinner one 6.7 nm thick, c.f. 11 nm and 6.4 nm nominally. In comparison the $Ti_{0.5}Hf_{0.5}O_2$ samples are substantially thinner than the anticipated nominal values. At 6.8 nm and 3.6 nm thick they are approximately 60% of the anticipated thickness (10.5 nm and 6.3 nm respectively). The MEIS data indicate that there is a mechanism by which the Ti incorporation inhibits the growth rate of the film without affecting the composition. Similar effects where doping alters the growth rate of deposited films in ALD have been seen before [65]. In this case it is likely to be due to an etching effect [136]. A net effect is that similar thickness samples of $Ti_{0.5}Hf_{0.5}O_2$ (6.8 nm) and $Ti_{0.1}Hf_{0.9}O_2$ (6.7 nm) were deposited. Ti and Hf depth profiles from these as-deposited samples are given in figure 6.9. MEIS energy spectra taken from samples before and following the 850 °C/spike and 500 °C/30 min anneals are given in figure 6.10. The spectra show no perceptible difference before and after annealing, implying that annealing does not cause inter-diffusion of the high-κ layer into the substrate, or

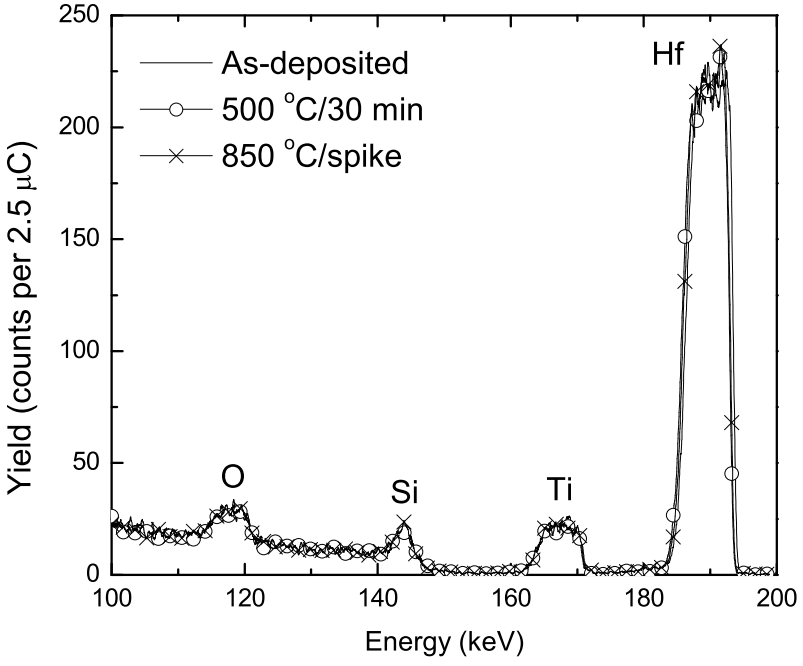

FIGURE 6.10: MEIS energy spectra for 6.7 nm $Ti_{0.5}Hf_{0.5}O_2$ samples as-deposited and after the 850 °C/spike and 500 °C/30 min anneals.

any increase in the SiO_2 interlayer thickness.

TEM

A XTEM image from the $Ti_{0.5}Hf_{0.5}O_2$ gate-last annealed sample is given in figure 6.11. Tilt checks were performed on-substrate-axis and 2 ° tilted in orthogonal directions; confirming that the alignment was close to the best edge-on condition.The silicon substrate can be seen on the left hand side ending in the 2 nm SiO_2 layer confirming the findings from the MEIS results that the interfacial oxide layer was unchanged by the annealing. The dark band is the $Ti_{0.5}Hf_{0.5}O_2$ layer corroborating the thickness measurements

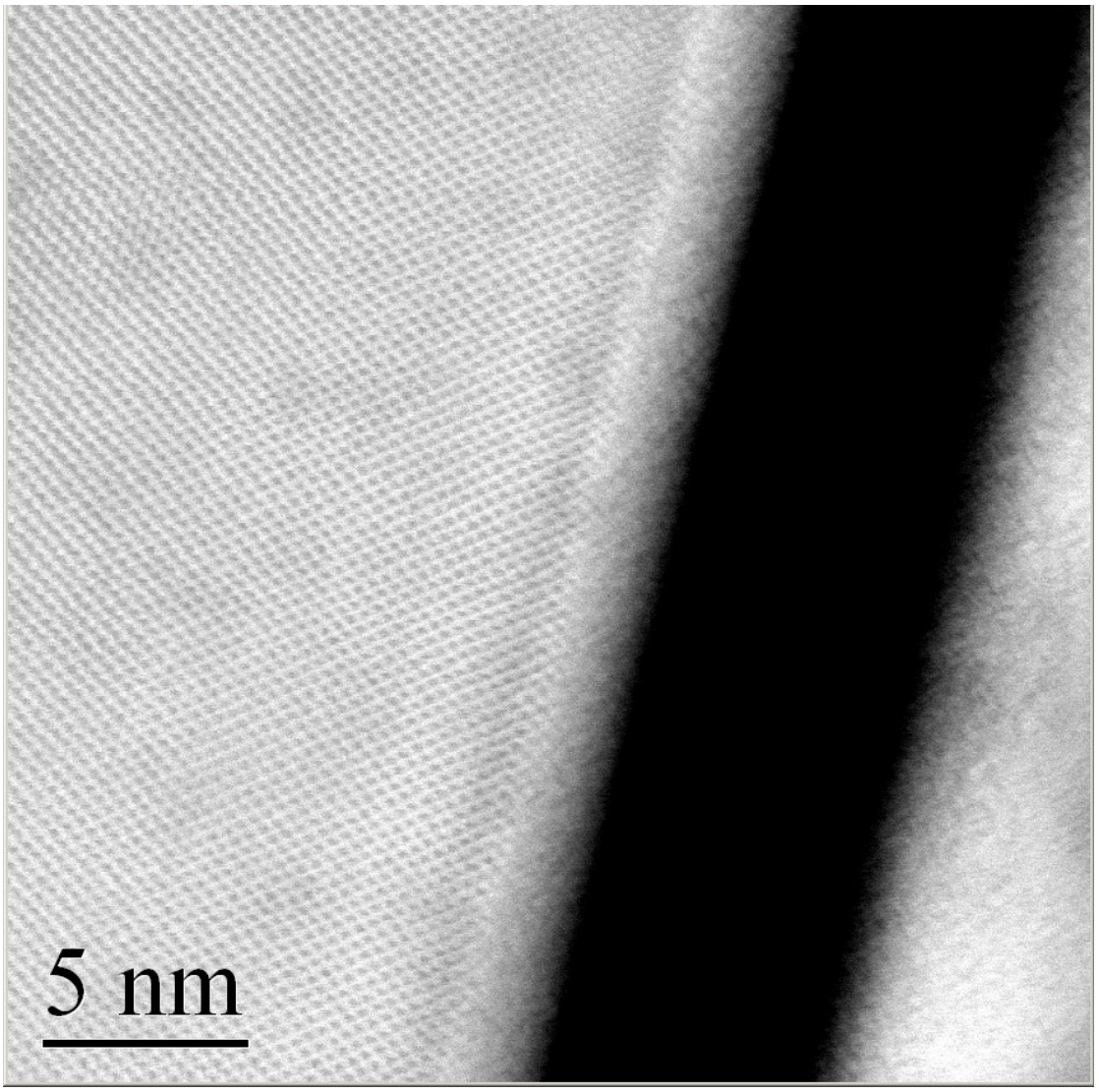

FIGURE 6.11: Cross-section TEM micrograph of $Ti_{0.5}Hf_{0.5}O_2$ film after the 500 °C/30 min anneal.

from the MEIS and ellipsometry data. The electron beam was manoeuvred onto several positions on this dark strip to see if diffractions spots resulted from the existence of crystalline material in the layer. As none were obvious it was concluded that the dark layer is comprised of amorphous material.

6.3.3 Ti-HfO_2 electrical measurements

C-V

C-V results taken at a measurement frequency of 100 kHz from a 6.8 nm thick 10% sample and a comparable 6.7 nm thick 50% sample are given in figures 6.12 and 6.13 respectively. The curves show measurement hysteresis of ∼1 V; slightly less than 1 V for the 10%Ti specimens examined. This hysteresis is indicative of trapped charges in the dielectric films, suggesting that the 50%Ti samples have a higher proportion of trapped charges than the crystalline 10%Ti films. The shift along the x-axis of the measurements made on annealed sample in both specimen sets is indicative of trapped charges in the dielectric stack. In both cases this effect appears more pronounced for the 500 °C/30 min annealed samples. The dielectric constant of each material can be extracted from the capacitance in strong accumulation (e.g. -4 V) when the 2 nm SiO_2 interfacial layer with a dielectric constant of 3.9 is taken into account. For the 50% sample the dielectric constant of the as deposited sample is 35, which reduces to 27 and 22 for the 500 °C/30 min and 850 °C/spike anneals respectively. These values are all higher than the ∼20 dielectric constant of undoped HfO_2 and competitive with measurements made on similar, differently-fabricated systems [73, 74]. For the as-deposited 10% sample the extracted dielectric constant is 20, which reduces to 12 following the 500 °C/30 min anneal. There is a marginal increase in the dielectric constant to 21 following 850 °C/spike annealing. The incorporation of Ti into an HfO_2 matrix is known to induce higher polarisability of the Hf and O ions leading to a softening of phonon modes and an increase in the dielectric constant [137]. Figure 6.13 is evidence of this effect when a relatively large proportion of Ti is included in a HfO_2 lattice.

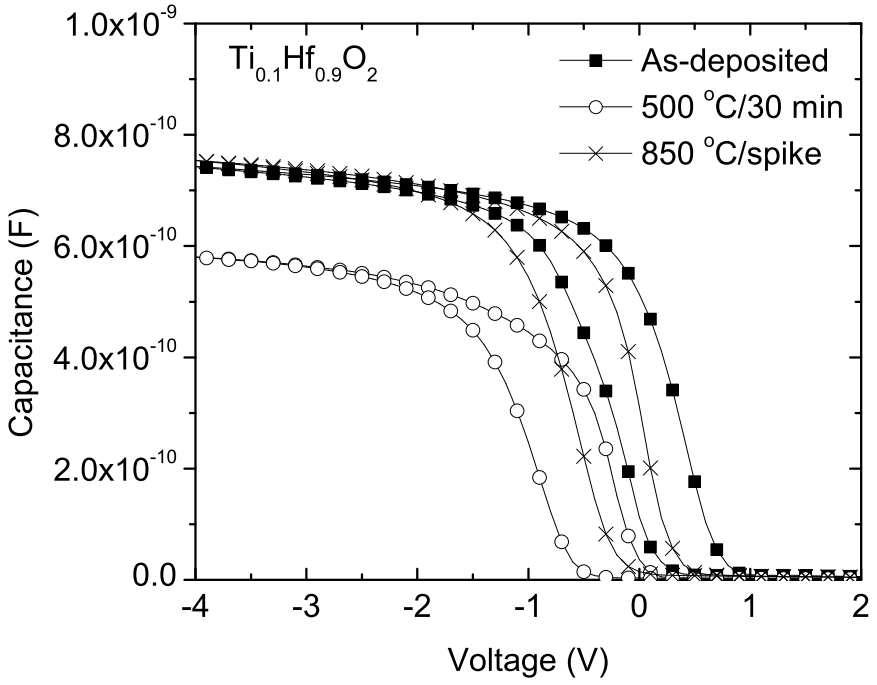

FIGURE 6.12: Capacitance-voltage measurements at 100 kHz for $Ti_{0.1}Hf_{0.9}O_2$ films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals.

J-E

Plots of the leakage current density with oxide field strength are given in figures 6.14 and 6.15 for the $Ti_{0.1}Hf_{0.9}O_2$ and $Ti_{0.5}Hf_{0.5}O_2$ samples respectively. The leakage current density is generally lower for the 50% Ti content samples compared to the 10% samples. For the 10% Ti as-deposited specimen in figure 6.14, the leakage current density is 1.1x10^{-5} A/cm^2 at a field-strength of -2 MV/cm. Annealing produces an increase in the leakage current density to ∼2.0x10^{-4} A/cm^2, which can be attributed to grain boundary surface area increase as the annealed samples crystallise and the grain boundaries act as paths for leakage current. The $Ti_{0.5}Hf_{0.5}O_2$ as-deposited sample has a leakage current density of 7.7x10^{-7} A/cm^2 at a field-strength of -2 MV/cm. The 500 °C/30 min anneal only makes a marginal difference to the leakage with a slight increase to 8.7x10^{-7} A/cm^2. The 850 °C/spike anneal increases the leakage current density by nearly two orders of magnitude to 3.6x10^{-5} A/cm^2. The asymmetry of the J-E curves in figures 6.14 and 6.15 is symptomatic of HfTiO-type dielectrics (in comparison to the relatively symmetrical J-E profile of un-doped HfO_2, see figure 5.7. Two trap levels at 0.7 and 0.9 eV below the

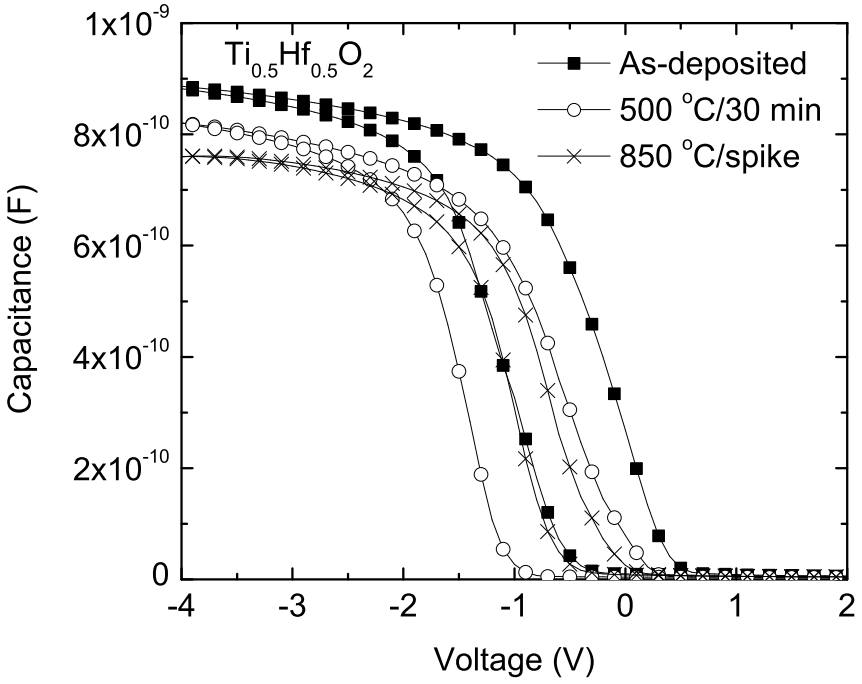

FIGURE 6.13: Capacitance-voltage measurements at 100 kHz for $Ti_{0.5}Hf_{0.5}O_2$ films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals.

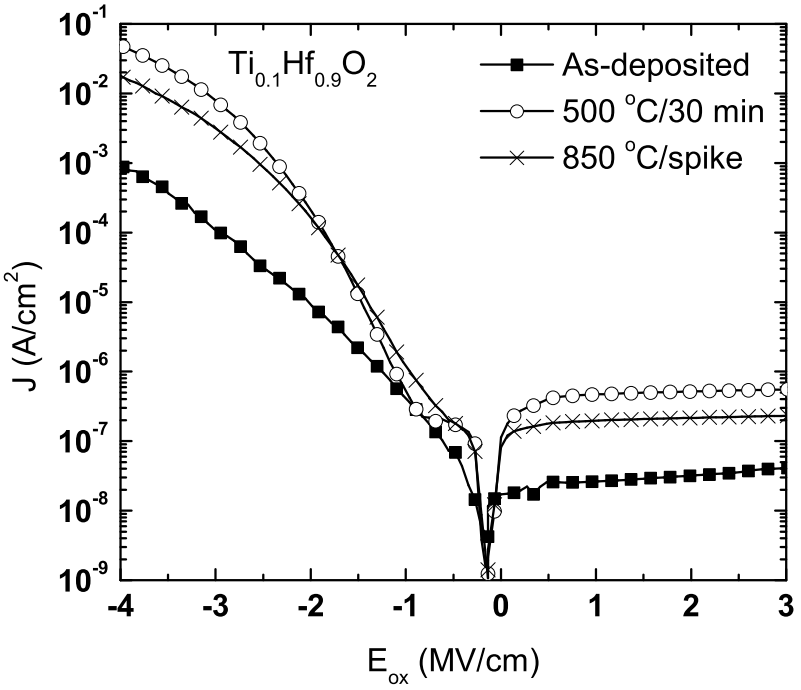

FIGURE 6.14: J-E measurements for $Ti_{0.1}Hf_{0.9}O_2$ films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals.

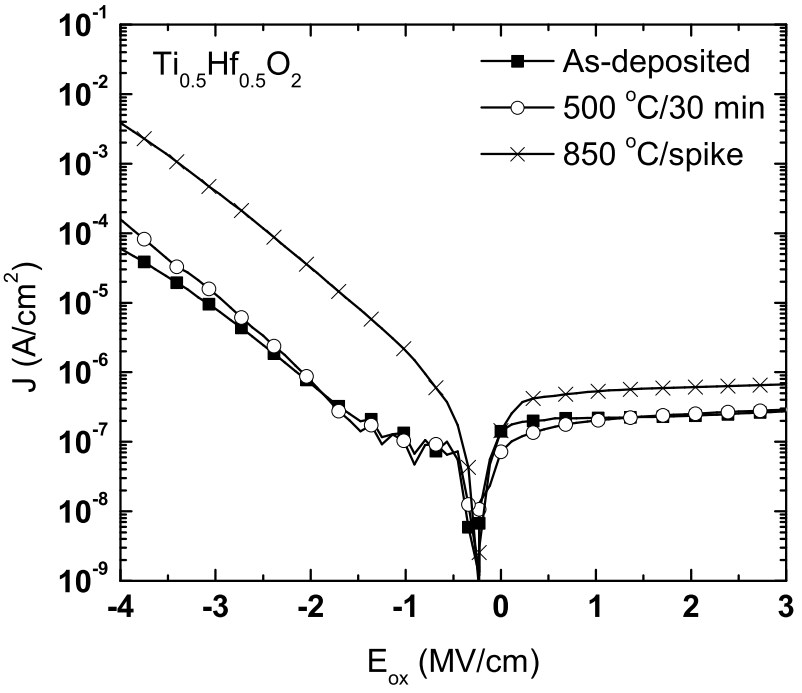

FIGURE 6.15: J-E measurements for $Ti_{0.5}Hf_{0.5}O_2$ films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals.

conduction band have been reported which participate in the conduction process [138]. These traps levels were found to be intrinsic to HfTiO - caused by the Ti incorporation into HfO-type layers - and so an unavoidable phenomenon is this kind of materials system. Offsets can be seen in both J-E plots where the curves switch polarity at $\sim 10^{-9}$ A/cm^2. These are -0.2 and -0.25 MV/cm for the 10%Ti and 50%Ti samples respectively. It is interesting to note the slightly larger offset seen for the composition richer in Ti. This seems to suggest that some source of built-in charge is being included as the Ti proportion is increased, perhaps linked to the amorphising effect seen in the structural characterisation. This reduction in film crystallinity must either result in a greater proportion of interface states, or trapped charges in the oxide itself, which result in the fixed offset highlighted.

The electrical performance of the 50%Ti sample represents a substantial improvement over the 10%Ti sample and undoped HfO_2. The dielectric constant suffers during the annealing step but is still much higher than the HfO_2 counterpart. The 500 °C/30 min, or 'gate-last', type of annealing is preferable. Because the films remain amorphous, the

leakage current is comparable with the undoped, crystalline HfO_2.

6.4 Chapter summary

Ti-HfO_2: In summary, additions of Ti to a HfO_2 matrix were shown to have an amorphising effect once the proportion of Ti was over ∼30%. This is most likely achieved through including an addition of smaller atomic radius in comparison to Hf; a comparatively fast-diffusing atom that acts as a network modifier under the heat treatment regimes studied here. The film thicknesses deposited (<10 nm) are in the right thickness range to promote an amorphous non-equilibrium phase in a thin film. Below the critical ∼30% addition proportion the Ti atoms are most likely accommodated in interstitial sites in the HfO_2 lattice, registering as slight peak shifts in the XRD measurements. The MEIS and TEM results in figures 6.10 and 6.11 were convincing evidence that the films and interfaces of annealed specimens were not significantly changed during the heat treatments. Of the two compositions examined in detail the $Ti_{0.5}Hf_{0.5}O_2$ demonstrated the highest permittivity value of 35 as-deposited. The increase in permittivity is attributed to Ti atoms effect on the polarisation of Hf and O ions in the material, and a related increase in permittivity as expected from the Clausius-Mossotti relation. The permittivity decreased to 27 after the 500 °C/30 min anneal and 22 after the 850 °C/spike anneal. Similarly the leakage current density measured for the $Ti_{0.5}Hf_{0.5}O_2$ films was higher after the 850 °C/spike anneal. This might be due to the higher temperature resulting in the nucleation of $TiHfO_3$ in a proportion that is too low for most of the analysis taken; the Raman measurements in figure 6.7 hint at the development of this phase, only looking convincing after a 1000 °C/30 min anneal and very long measurement time. The asymmetry of the J-E measurements is thought to be related to defect trap states at 0.7 and 0.9 eV below the conduction band of the material.

Chapter 7

Results: Ce-HfO_2

7.1 Experimental rationale - Ce-HfO_2

In attempting to maximise the properties of HfO_2-based dielectric films via ALD, one potential avenue is to dope the material with a different-atom-size addition to provoke the retention of a metastable crystallographic phase at room temperature. The addition atoms substitute for Hf atoms in the lattice and by modulating the molar volume of the mixed phase make a non-equilibrium phase more energetically favourable. Frequently the transformation of the films to the metastable phase requires post-deposition heat treatment so the structural alterations seen for each type of annealing regime are key to learning about the material produced. Also in comparison with the amorphous phase films produced in the previous chapter the effects of grain size and grain boundary volume on electrical properties might be important.

This chapter begins with a section on the deposition of CeO_2 films using $Ce(mmp)_4$ and water as precursors. The section goes on to present measurements made on CeO_2 films and discusses CeO_2's suitability as a dielectric material in its own right. The second section of the chapter describes the inclusion of cerium in a hafnium oxide-based material in order to assess the effects on the physical structure and dielectric response of the films compared to undoped HfO_2. The intention in the latter work was to produce specimens of a variety of thicknesses and compositions $Ce_xHf_{1-x}O_\delta$. Unfortunately, due to issues with the deposition, only one composition was produced but the experiments

were still profitable; both as a proof of concept for Ce-HfO_2/H_2O thermal ALD and as a comparison with other doped HfO_2 systems in the literature.

7.2 CeO_2

7.2.1 CeO_2 deposition - Trijet™

CeO_2 films were grown on the Trijet™ reactor at a variety of growth temperatures, 150–350 °C in ALD mode and 250–600 °C in CVD mode, using $Ce(mmp)_4$ and water. The substrates used were n-type Si(100) with a ∼2 nm native oxide as opposed to the p-type substrates used in the case of all other deposition experiments in this thesis. This was the first assessment of the $Ce(mmp)_4$ precursor for vapour deposition [**iv**]. Data on it and other cerium precursors was published together in an article on precursors for CeO_2 deposition [**ii**]. A materials structure-properties paper followed from subsequent analysis performed on the range of ALD samples grown utilising $Ce(mmp)_4$ and water [**iii**]. Figure 7.1 presents the thermal gravimetric analysis (TGA) plot of $Ce(mmp)_4$ over

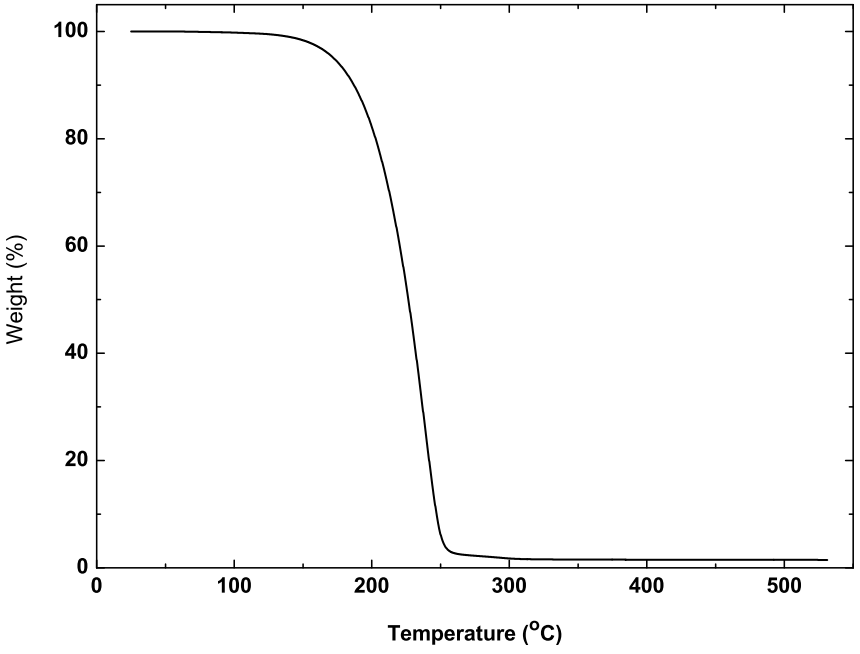

FIGURE 7.1: Thermal gravimetric analysis of $Ce(mmp)_4$ precursor carried out under atmospheric pressure.

a range of temperatures carried out under atmospheric pressure. The data suggest that the evaporation of the compound begins to take place in the region 100–150 °C. After ∼250 °C the dry residue is all but negligible. Under low pressure (0.8 Torr) $Ce(mmp)_4$ sublimes intact without deposition of residues [**iv**]. This information is vital with a new precursor to estimate the likely maximum working temperature over which decomposition will become unacceptable. The ideal temperature is high enough to provoke suitable volatility in the precursor to get vapour transport from its container to deposition chamber without causing decomposition at a rate that will seriously limit the lifetime of the precursor. Before use in the Trijet^{TM} reactor the $Ce(mmp)_4$ compound had to be dissolved in toluene to make a 0.05 M solution that could be fed into the liquid injection system. The precursor usage was assessed during deposition by recording the changes on the graduated precursor vials. Pre and post-deposition the wafers were weighed in order to calculate the thickness of layer grown each time. Figure 7.2 is a graph of deposition weight measurements from the first set of $Ce(mmp)_4$ experiments conducted on the Trijet^{TM} reactor. The ALD points are linear-fitted and the CVD data are fitted to a

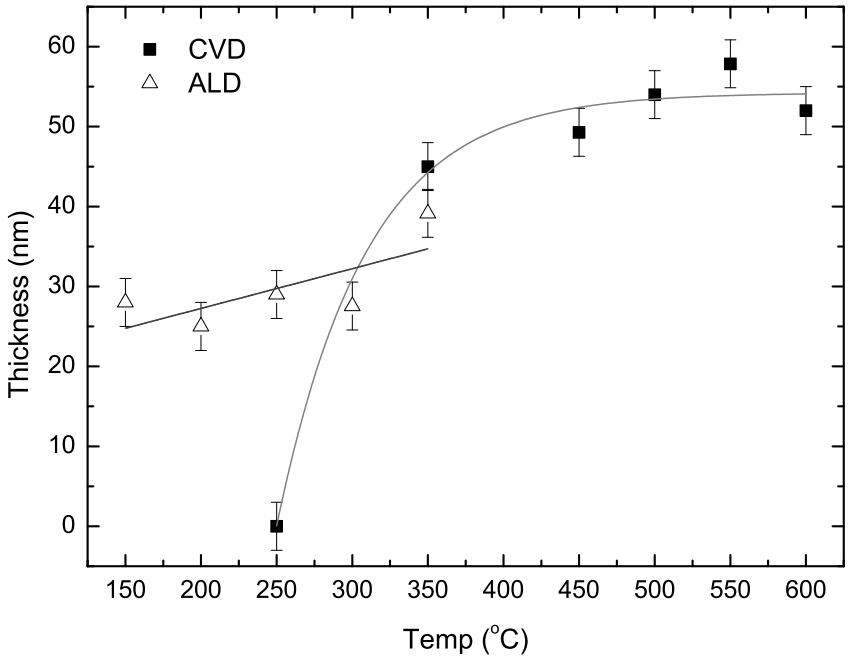

FIGURE 7.2: $Ce(mmp)_4/H_2O$ deposition by substrate temperature; the triangles denote the ALD growth window, the squares are the CVD growth.

Boltzmann function. The evaporator temperature was 100 °C. As ALD is a saturative two-step process it is expected to result in a plateau of very similar deposition rates within the ALD growth window. The measurements demonstrate a reasonably linear ALD plateau with the last point at 350 °C slightly higher - perhaps some some evidence of CVD-type deposition components during growth at this temperature.

7.2.2 CeO_2 characterisation

XRD

Figure 7.3 shows the XRD diffraction patterns recorded for films deposited at 150 °C, 250 °C and 350 °C. There is an arbitrary offset in the intensity axis between data sets and background features have been removed for clarity. At all temperatures the films have diffraction peaks centred about 28.6°, 33.1° and 47.5° corresponding to the cubic (111), (200) and (220) diffraction peaks respectively (ICDS card [43-1002]). The peaks show a broadening at lower deposition temperatures; most noticeably in the (111) peak. Diffraction scans with a slower scan speed were carried out in the region of the (111) peak to obtain full width at half-maximum (FWHM) data due to the (111) being the most distinct diffraction peak. In XRD peak broadening occurs due to effectively sampling fewer planes in a film of smaller average crystallite size and hence increasing the angular range of lesser intensity around the diffraction peak. Other factors that can have an impact on peak width are instrumental broadening effects and lattice strain contributions. Instrumental broadening is not a concern due to the small size of the grains and hence peaks that are considerably broader than the system resolution. The Scherrer formula [139], equation 4.2, was used to estimate the average crystallite diameters, τ, from the (111) X-ray diffraction features for each of the specimens. Here 0.9 is the Scherrer shape factor, λ the X-ray wavelength, β the FWHM of the sample peak (radians) and θ is the scattering angle at the centre of the peak being measured. Measurements performed have the grain size changing from ∼6 nm for the 150 °C sample, to ∼23 nm for the 350 °C sample. Larger grain size with increased deposition temperature is to be expected and is most likely due to increased mobility of the deposited atomic material with increased deposition temperature. An overestimation via XRD FWHM measurements can exist due to to the effect of lattice

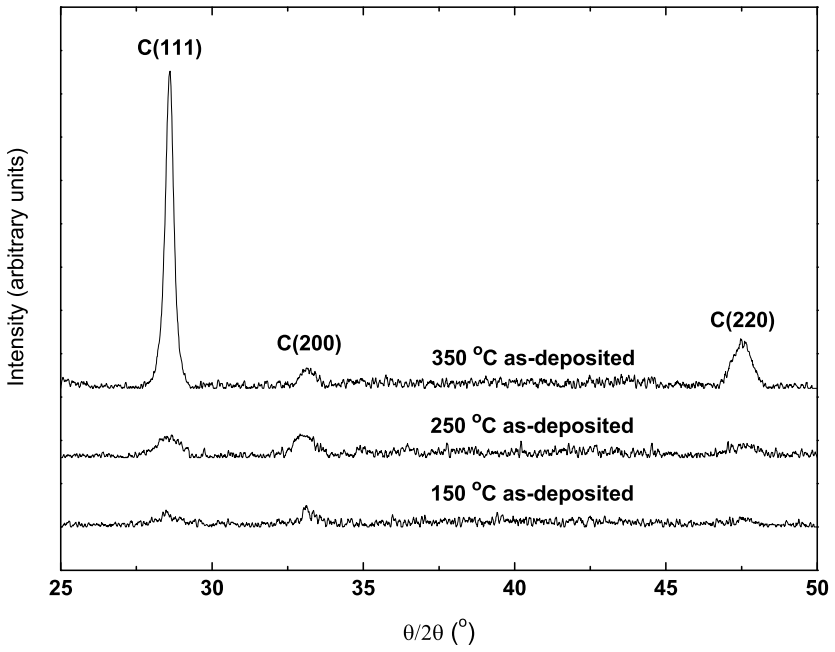

FIGURE 7.3: XRD measurements for ∼50 nm CeO_2 ALD film as-grown at three substrate deposition temperatures. The background has been removed for clarity and the peaks associated with cubic CeO_2 are indexed.

strain in the films. At higher temperatures and with larger grains there is less grain boundary surface area that would alleviate strain in the films.

Raman spectroscopy

Figure 7.4 shows the ultraviolet-excited Raman spectrum of CeO_2 films deposited at the same three substrate temperatures. A mode at ∼520 cm^{-1} is associated with the silicon substrate and has been removed for clarity (denoted with an asterisk). The measurements are otherwise unaltered except for an arbitrary shift on the intensity axis. The mode at ∼465 cm^{-1} is the first-order triply-degenerate F_{2g} mode associated with the fluorite crystal structure - a symmetrical stretching of the CeO_8 unit in the lattice. This mode confirms that the crystalline phase is cubic. The other mode seen is the second-order A_{1g} symmetry mode. Seven such second-order modes are predicted but two have additional contributions from the E_g (∼600 cm^{-1} mode) and F_{2g} (∼1178 cm^{-1} mode) symmetry elements [140]. The presence of second-order modes in the UV Raman

plot is testament to the resonance Raman process which samples phonon contributions away from the centre of the Brillouin zone. For example the two Raman sources used in figure 7.4 can have their wavelengths converted to electron volts: 514 nm $\rightarrow$ $\sim$2.41 eV, 325 nm $\rightarrow$ $\sim$3.82 eV. Bulk CeO_2 has a band gap of 3.15 eV with values as high as 4 eV recorded for thin films. From these values it can be seen that the band gap for CeO_2 is very close to the excitation energy of the UV laser source. Owing to this the appearance of the 2nd-order modes, and enhancement of the1st-order, is most likely a *resonance enhancement* effect where these phonon contributions are sensitive to excitation energy.

A clear shift of the F_{2g} mode to higher wavenumber values as well as a broadening of the band with decreasing temperature is seen. This broadening effect is due to reduced phonon lifetime with smaller grain size. The general peak shift is attributed to a softening of phonon modes for lower crystallite size at the lower deposition temperatures and an increase in lattice constant [141]. Below a grain size of 100 nm this mode is expected to show a width decrease with grain size following a cubic root dependency; above this

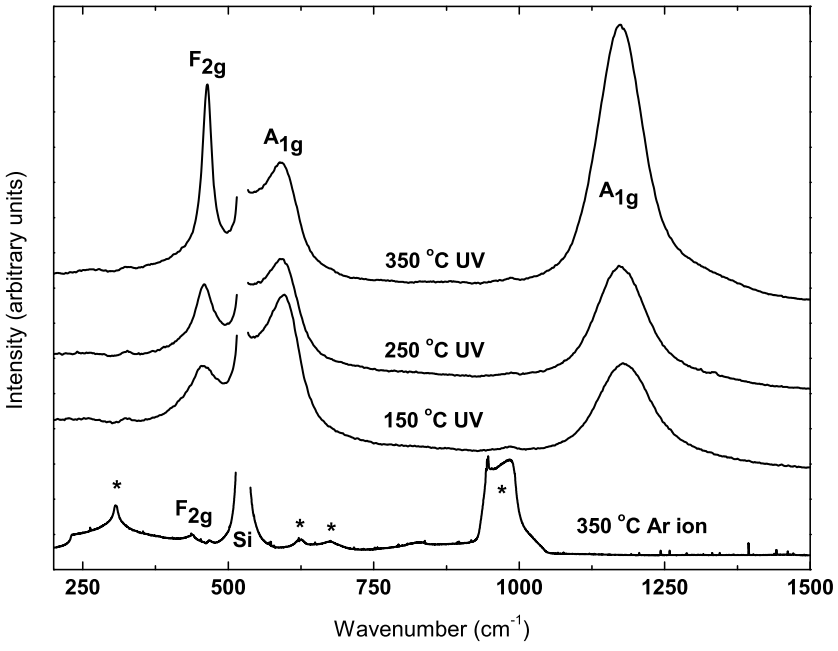

FIGURE 7.4: UV Raman measurement of CeO_2 ALD films as-grown at three deposition temperatures; the trace from a 514 nm Ar ion laser Raman measurement of the 350 °C film is included for comparison. The phonon modes indexed are associated with the cubic phase of CeO_2. The asterisks in the Ar ion trace denote substrate contributions.

size regime the modes sensitivity to oxygen sub-lattice disorder effects can result in broadening. The Raman results correlate with the XRD data and show that the films contain cubic crystallites and that the grain size increases with increasing deposition temperature. It is difficult to attach an accurate grain size to these measurements due to other factors, such as lattice strain, that affect the Raman line width. The general trend is the same as with the XRD results, showing larger grain sizes as the growth temperature increases.

Linear trend in feature widths

Figure 7.5 shows the change in measured F_{2g} Raman band half-width at half-maximum against the changing crystallite size as calculated from the XRD data. The least-squares fitted line can be adapted for a relation between Raman band width measurement and crystallite size of the form

$$\Gamma(cm^{-1}) = 6 + 72/D(nm) \tag{7.1}$$

where 6 and 72 are fitting coefficients, D is the XRD-derived crystallite size and Γ is Raman line half-width at half-maximum. It is interesting that the data fit well within the previously-reported ceria measurements even though the grain size control comes purely from substrate temperature during deposition and not from some subsequent heat treatment. Equation 7.1 is an empirical relation with similar coefficients to that developed in [142]; 5.48 and 98.4 in place of 6 and 72 respectively.

7.2.3 CeO_2 electrical measurements

C-V

Figure 7.6 shows capacitance-voltage (C-V) plots from films grown at 150 °C, 250 °C and 350 °C with thickness of 51 nm, 50 nm and 44 nm respectively obtained by ellipsometry. Curves for test frequencies between 1 kHz and 1 MHz are plotted. The curves are the opposite way round (reflections in the y-axis) to the others in this thesis owing to the n-type doping of the Si substrates used. The dielectric constant can be extracted from the capacitance values in strong accumulation taking into account the presence of

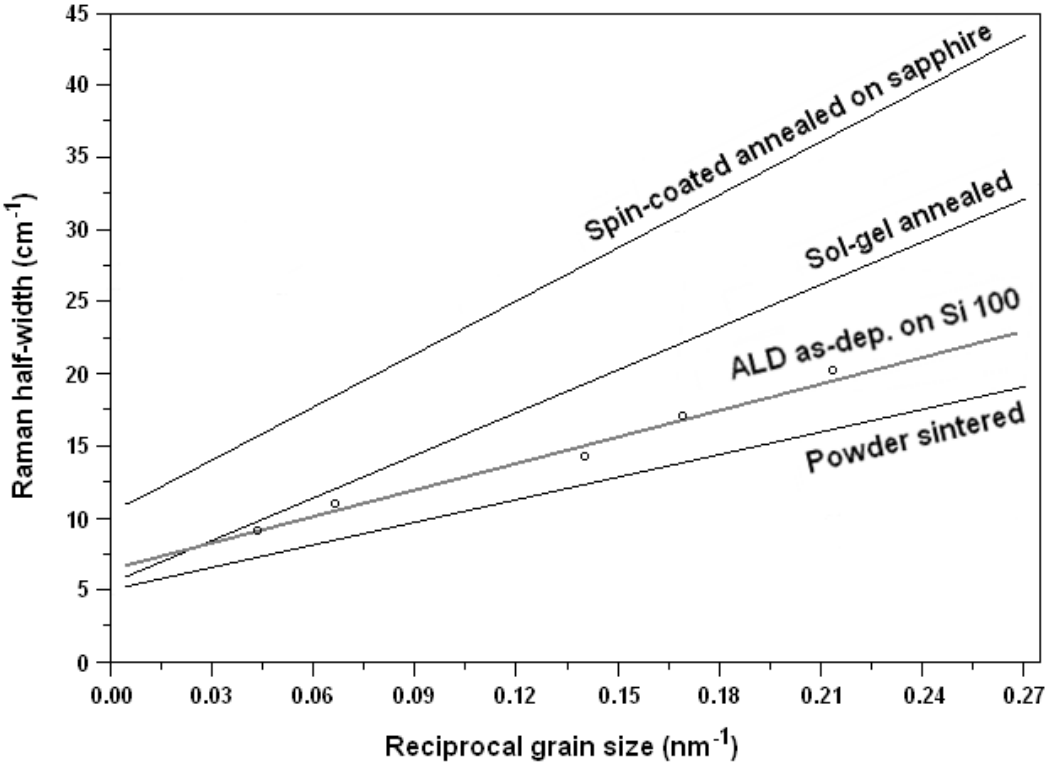

FIGURE 7.5: Raman band half-width plotted against XRD-measured particle size; three other experimental references are included for comparison. From the top down [143], [142], our data and [140]; superimposed on the data from [142].

a 1.6 nm thick native SiO_2 layer with a dielectric constant of 3.9. For the sample grown at 150 °C the extracted κ value at 1 MHz is 42 and for the sample grown at 350 °C the value at 1 MHz is 25. These are relatively high values in comparison to amorphous HfO_2. At the lower measurement frequency the capacitance increases, most markedly for the sample grown at 150 °C. For a given bias voltage the capacitance will generally increase as the measurement frequency is decreased [120]. The change in capacitance with frequency is better illustrated in the C-f plot given in figure 7.8 which summarises the accumulation capacitance (1 V bias) as a function of bias frequency for the CeO_2 films deposited at 150 °C and 350 °C.

J-E

Figure 7.7 presents leakage current density data for the films at three different deposition temperatures. A measure of the leakage current density for films grown at the three temperatures of 150 °C, 250 °C and 350 °C is 9.4×10^{-4}, 6.6×10^{-4} and 7.4×10^{-4}

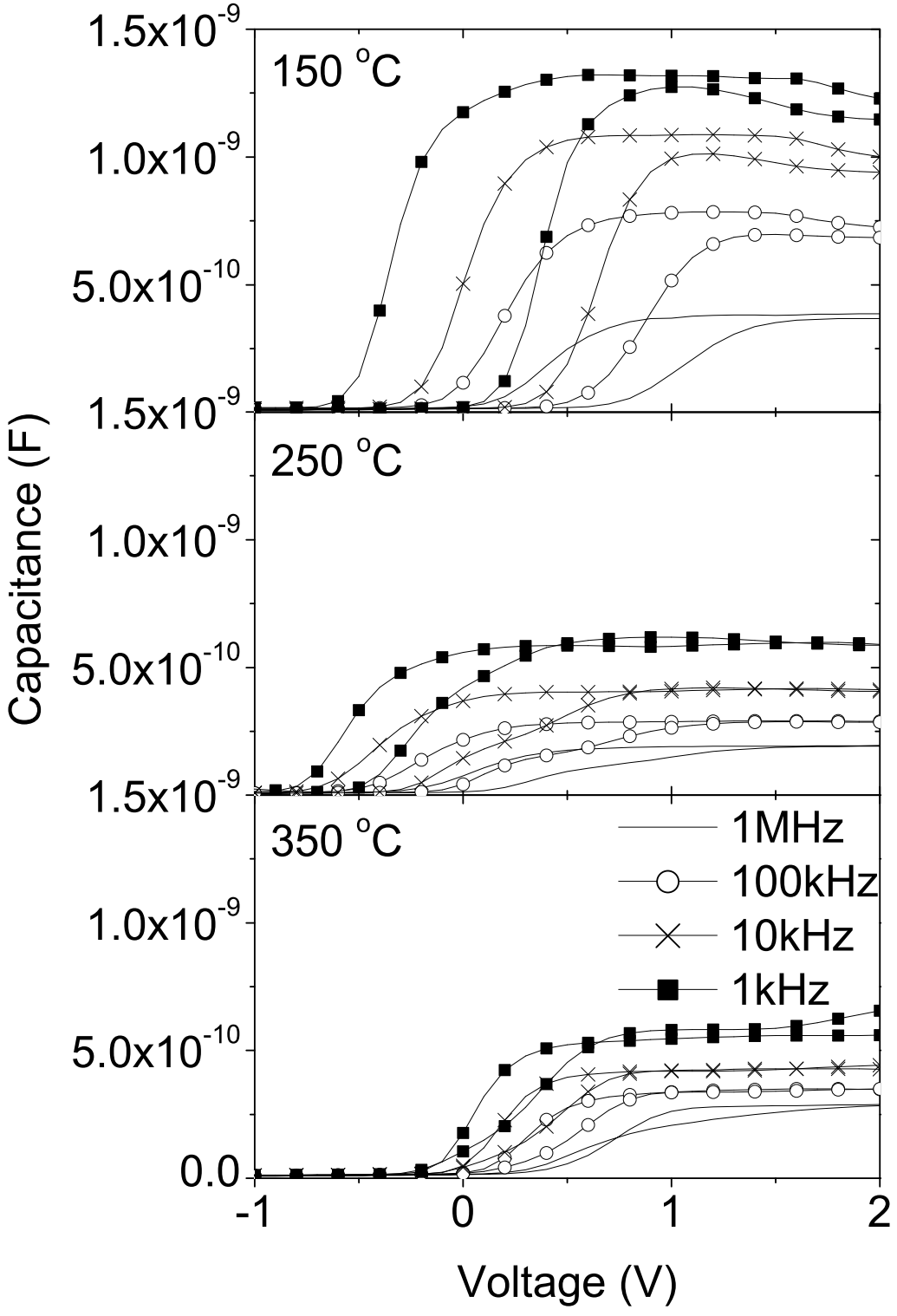

FIGURE 7.6: Capacitance-voltage measurements for CeO_2 films as-deposited for three deposition temperatures.

A/cm^2 respectively at a field of 0.5 MV/cm. The similarities in the data at voltages where the films are in strong accumulation (i.e. 0.4 to 0.6 MV/cm) between the different samples suggest that the changes in the C-V and C-f data are not due to leakage. In all cases the films were deposited on essentially identical Si wafers with a ∼2 nm native SiO_2 layer and hence should all have the same thickness of interfacial layer. An offset of between 0.07 and 0.16 MV/cm is noticeable where the curves switch polarity at $\sim 10^{-6}$ A/cm^2. This offset is in the opposite direction to that seen in all other measurements due to the CeO_2 samples set being grown on n-type Si rather than p-type. Interestingly, the offset changes with deposition temperature; the largest offset of +0.16 MV/cm is seen for the 150 °C sample. Deconvoluting these factors allows the material properties of the films to be ascertained.

One potential explanation for the different frequency dispersion, or dielectric relaxation, behaviour observed between the different growth temperatures relates to the different crystal grain sizes formed at the different growth temperatures. It has been reported that a decrease in crystal grain size can cause an increase in the dielectric relaxation in

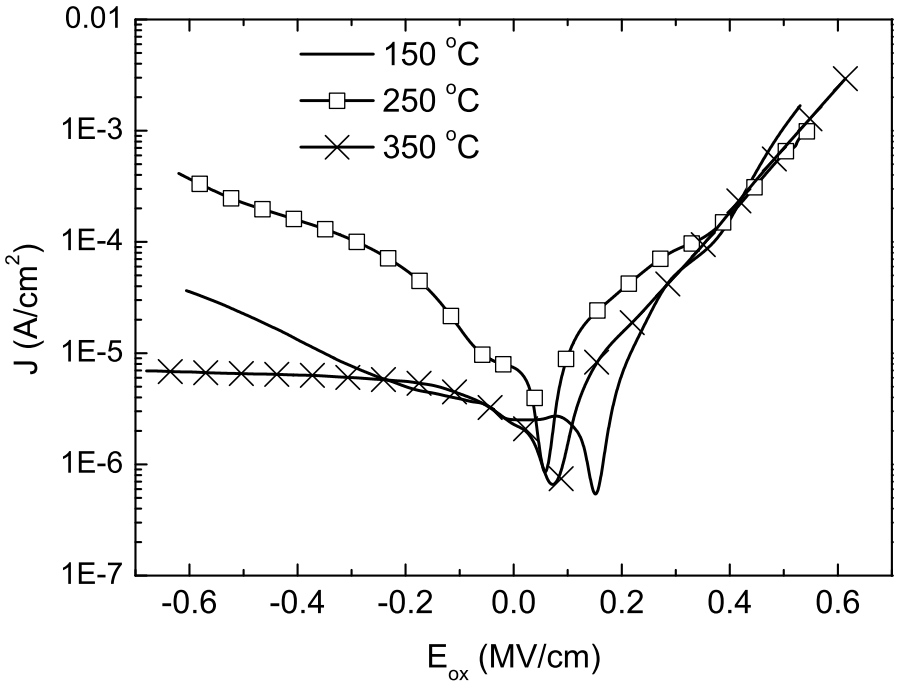

FIGURE 7.7: J-E measurements for CeO_2 films as-deposited for three deposition temperatures.

ferroelectric relaxor ceramics; most likely due to increased stress within smaller crystal grains [144, 145]. In addition to ferroelectric relaxor ceramics it has been reported that lanthanum-doped zirconium oxide high-κ dielectrics also suffer from a severe dielectric relaxation as the size of crystalline grains is reduced [146]. With these CeO_2 films the lower crystallite-size specimens suffer a much more severe dielectric relaxation than those with higher growth temperature and hence higher crystallite size. A reasonable conclusion is that the physical process behind the relaxation is dominated by the size of the crystallite grains formed during growth. It is clear that films consisting of smaller crystallites will contain a larger grain boundary network than one consisting of larger crystallites. As the polarisability of a dielectric grain is mainly from the surface this could account for the large increase in capacitance observed in the 150 °C sample at 1 kHz which then reduces with frequency due to the dielectric relaxation effects. It is apparent that the crystallite size increases over the temperature range 150 °C to 350 °C and hence the grain boundary network reduces. Grain boundaries are a well established source of leakage current pathways and consequently films with a smaller grain boundary surface area (e.g. larger average crystallite size) are expected to display lower leakage current densities in films of comparable thicknesses. In these samples the variation in leakage between samples is not very different but the leakage current density is relatively high in comparison with other crystalline hafnium oxide based dielectric materials measured under comparable conditions.

C-f

Figure 7.8 is capacitance-frequency measurements for specimens grown at 150 °C and 350 °C. The plot demonstrates significant frequency dispersion for the sample grown at 150 °C. There are five reasons which may cause the frequency dispersion observed: (i) series resistances, (ii) parasitic effects (including back contact imperfection and cables and connections), (iii) leakage currents, (iv) the interlayer between the high-κ layer and silicon substrate and (v) a κ value dependence on frequency of the CeO_2 film. To obtain the genuine intrinsic properties and permittivity of the CeO_2 dielectric from the CV measurements the first four effects must be eliminated. The effects of series resistances and parasitic effects have been reported previously [146]. To minimise the effects of

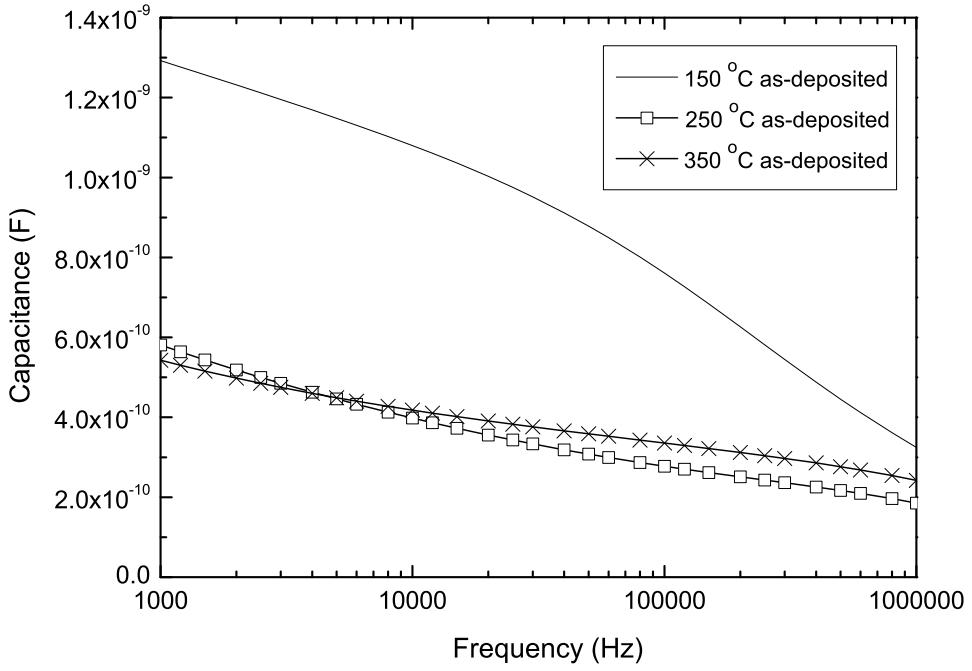

FIGURE 7.8: Capacitance-frequency measurements for CeO_2 films as-deposited for the growth temperatures 150 °C and 350 °C.

series resistances and back contact imperfections (including contact resistance R, contact capacitance C, or parasitic R-C coupled in series etc.) aluminium back contacts were deposited over a large area of the substrate wafer. The same procedure was carried out for all samples. All samples tested had the same or very similar substrate area ($\sim$2 cm^2) to ensure that the effects of series resistance and back contact imperfections were the same for all samples. Furthermore measurement cables and connections were kept short to further minimise parasitic capacitance effects and were the same for all samples.

7.3 Ce-HfO_2

7.3.1 Ce-HfO_2 deposition - OpAL®

Ce-doped HfO_2 films were deposited on the OpAL® reactor. The $Ce(mmp)_4$ precursor was used in conjunction with the $(MeCp)_2Hf(OMe)(Me)$ precursor described in the previous two results chapters, with H_2O as the oxidant. Though Ce-HfO_2 had been previously demonstrated by our group [46] the OpAL work offered some more insight into the materials system. The original Ce-HfO_2 paper describes using a solution-$Ce(thd)_4$ precursor as the cerium source. $X(thd)_4$ precursors tend to be very stable compounds with poor transport and surface mobility. Because of this using the more aggressive oxidant O_3 was necessary. In the growth described here the key differences are that a solid $Ce(mmp)_4$ precursor was used and that water was the oxidant. This deposition set up offers a less problematic route to Ce growth, without having to make up precursor solutions and without the need for an O_3 generator. A nominal doping level of 12.5% ($Hf_{0.875}Ce_{0.125}O_2$) was decided on to try to provide a suitable comparison to our group's previous work [46] and to the first principles experiments done by Fisher et al. [147]. Some binary oxide growth experiments served as preparatory work from which to get an approximate growth rate for each precursor on the OpAL® reactor before a doping strategy could be formed.

Thermal ALD deposition on the OpAL® reactor using $[Ce(mmp)_4]$ and water proved to be problematic. Initially the bubbler containing the precursor was heated to 100 °C as that temperature was used in the Aixtron reactor experiments described previously. At this temperature however negligible growth was recorded. The bubbler temperature was gradually increased in 5 °C increments with a deposition run each time and the wafer checked for any growth. At 130 °C the precursor was found to be transporting to the chamber and depositing cubic CeO_2 - this could be checked routinely by running Raman measurements similar to those in figure 7.4. This temperature was, however, very close to the slope in the TGA plot (figure 7.1) that indicated the onset of precursor decomposition. Owing to this the decision was made to establish a reliable growth rate for the precursor and start the Ce-HfO_2 work immediately. Table 7.1 presents the

TABLE 7.1: OpAL® reactor parameters for depositing $Ce(mmp)_4$ and $(MeCp)_2Hf(OMe)(Me)$ at substrate temperature of 350 °C.

$Ce(mmp)_4$ bubbler temp.	130 °C
Ar bubbler	200 sccm
Ar purge	100 sccm
pulse	0.05 s
purge	6 s
$(MeCp)_2Hf(OMe)(Me)$ bubbler temp.	130 °C
Ar bubbler	300 sccm
Ar purge	200 sccm
pulse	3 s
purge	6 s
H_2O pulse	20 ms
H_2O purge	10 s

parameter settings for optimum deposition of the two component precursors. Both precursors used a water pulse/purge of 0.02/10 seconds. A stage temperature of 350 °C was decided on as a compromise between the two precursors based on previous growth work on $(MeCp)_2Hf(OMe)(Me)$ and $Ce(mmp)_4$. After some growth experiments and measurements consistent rates for $(MeCp)_2Hf(OMe)(Me)$ ($\sim$0.42 $\AA$/cycle) and $Ce(mmp)_4$ ($\sim$0.15 $\AA$/cycle) were arrived at. Grown in a 1:1 ratio this would result in a ratio of 8.4:3, HfO_2:CeO_2 or a doping of $\sim$27%Ce in a 1:1 cycle deposition. To control the doping level of Ce in HfO_2 it remained to design supercycles of the correct ratios and then determine how many of the supercycles to deposit to result in the desired thickness of film. As the desired dopant percentage was 12.5% Ce the ratio of 5:2 was chosen; calculated to produce a dopant percentage 12.6% if the growth rates were accurate: 5:2 ratio$\rightarrow$41.5:6, 6/47.5=12.6%. To attain different thicknesses it was a case of calculating a deposition rate for the 5:2 supercycle and deciding on a number of supercycles for each desired thickness. 5:2 ratio$\rightarrow$5(0.42 $\AA$/cycle)+2(0.15 $\AA$/cycle)=2.4 $\AA$/cycle. For the desired 2 nm, 6 nm and 10 nm films this new deposition rate meant recipes of 8, 25 and 42 supercycles respectively.

7.3.2 Ce-HfO_2 characterisation

XRD

Figure 7.9 presents XRD measurements performed on the nominally 10 nm doped sample before and after the 500 °C and 850 °C anneals. The film is amorphous as deposited but develops features consistent with either cubic or tetragonal crystallinity after annealing. The cubic/tetragonal ambiguity is due to the XRD features for each polymorph being extremely similar. A measurement done on an annealed ∼10 nm HfO_2 film is included in the diagram demonstrating the monoclinic features usually seen for hafnium oxide after annealing at this temperature. The standard anneal temperature set of Ce-HfO_2 specimens presented in figure 7.10 shows that this metastable phase is stable in the material at least up to 1000 °C heat treatment.

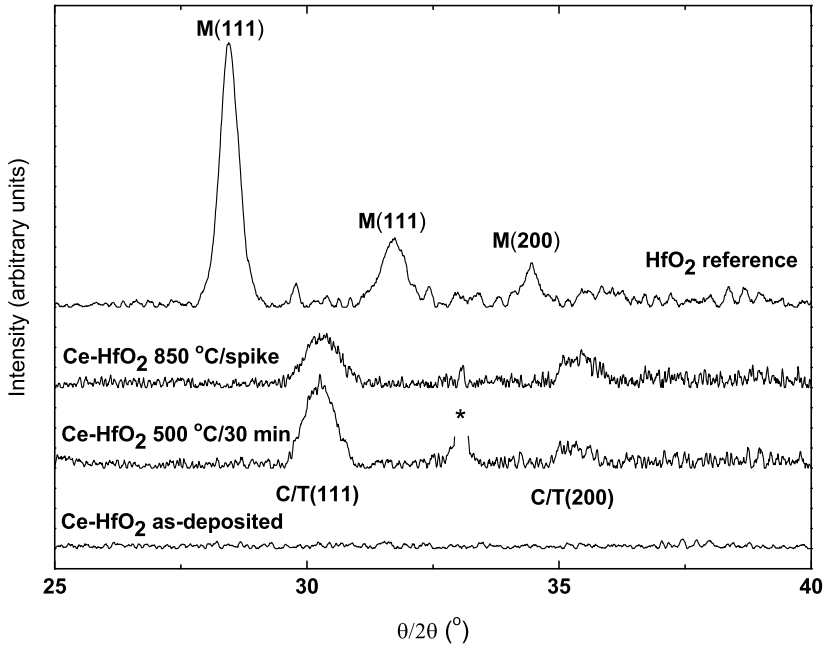

FIGURE 7.9: XRD measurements for Ce-HFO_2 films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals; a HfO_2 850 °C-annealed trace is included for comparison. The traces' backgrounds are removed for clarity and one trace has the Si peak removed (asterisked).

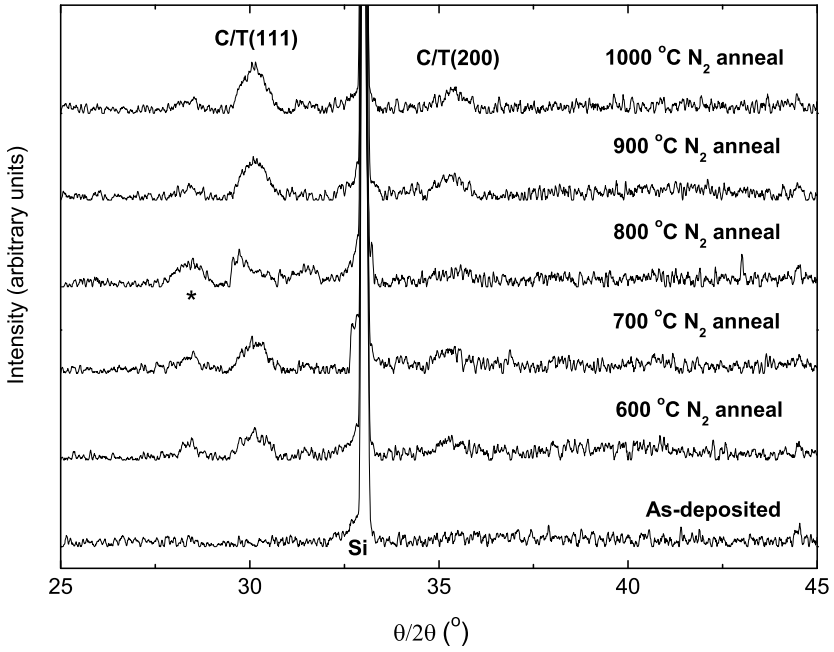

FIGURE 7.10: XRD measurements for the Ce-HFO$_2$ films as-deposited, and after standard anneals at five temperatures. The peak at ∼33 ° is from the Si substrate. The asterisked peak is monoclinic; suggesting some mixed crystallinity at lower annealing temperatures.

Raman spectroscopy

Raman measurements for the 11%Ce-HfO$_2$ specimen set annealed at in N$_2$ for 30 minutes at various temperatures are presented in figure 7.11. The traces show the development of modes which are arrowed in the top curve in a much longer measurement (120 s acquisition time, 5 acquisitions). The peaks seen fall at wavenumber values ∼266, ∼380/390 ∼627 ∼673 and ∼740 cm^{-1}. Raman modes are expected at 280, 460 and 656 cm^{-1} for tetragonal HfO$_2$ [148, 149] but these don't map convincingly to the lines seen in figure 7.11. The best match is probably monoclinic HfO$_2$, especially the double peak at 380/390 cm^{-1}, which along with the asterisked peak seen in the XRD in figure 7.10 suggests the films have mixed crystallinity.

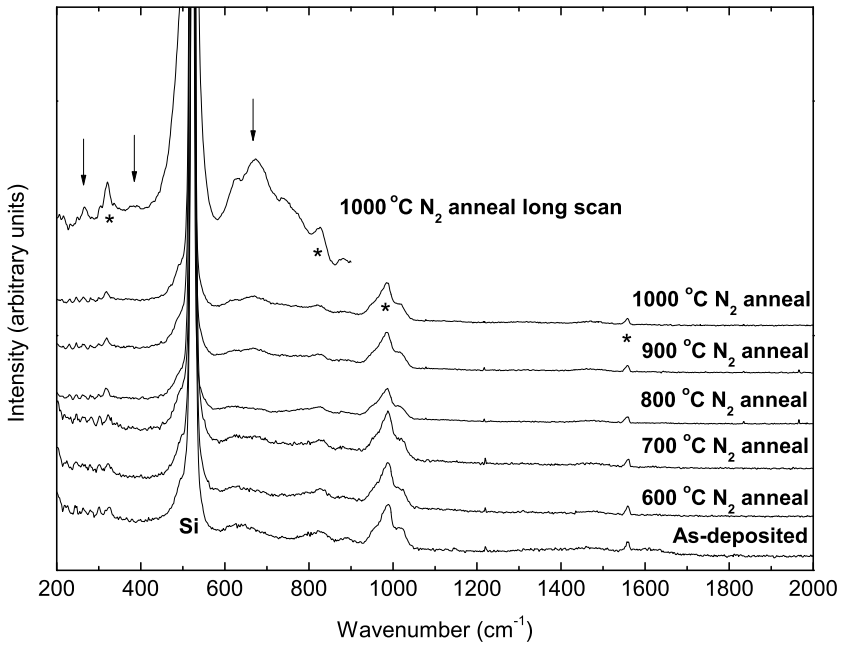

FIGURE 7.11: UV Raman measurements for Ce-HfO$_2$ films as-deposited and after standard anneals at five temperatures. The asterisks denote substrate contributions.

MEIS

Figure 7.12 shows the MEIS energy spectra from the 1–2 nm thick specimen deposited as-grown. The signatures associated with silicon, cerium and hafnium are highlighted; the reasoning behind growing a very thin layer was the separation of the Ce and Hf signatures which are convoluted in thicker specimens. Under these conditions the Ce and Hf content of the films can be separated. After accounting for elastic and inelastic energy loss processes the energy spectra can be converted into depth profiles and those for Ce and Hf are presented in the inset of figure 7.12. The composition of the film was obtained by integrating the peak areas of the depth profiles and adjusting for the the difference in relative scattering cross section of the two elements. The composition was found to be $Hf_{0.89}Ce_{0.11}O_2$. Figure 7.13 shows depth profiles for the hafnium matrix from the three specimen thicknesses grown. This data shows that the initial growth rate/supercycle calculations delivered films very close to the desired thicknesses aimed for, albeit with a slightly lower cerium doping percentage of 11% instead of the aimed-for

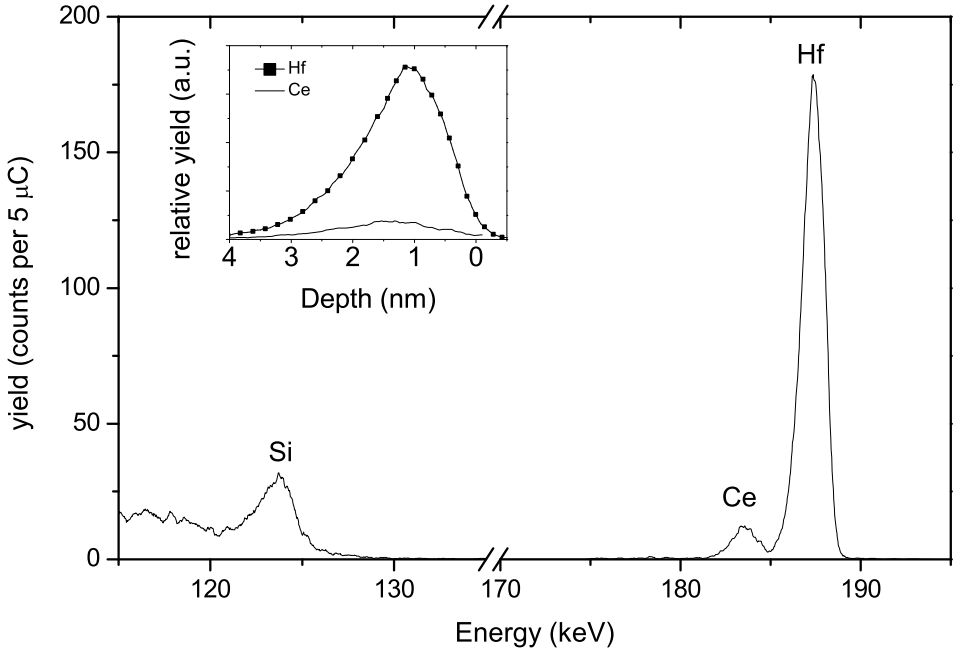

FIGURE 7.12: MEIS energy spectra for 1-2 nm thick Ce-HfO$_2$ specimen as-deposited; inset demonstrates Ce:Hf compositional proportion.

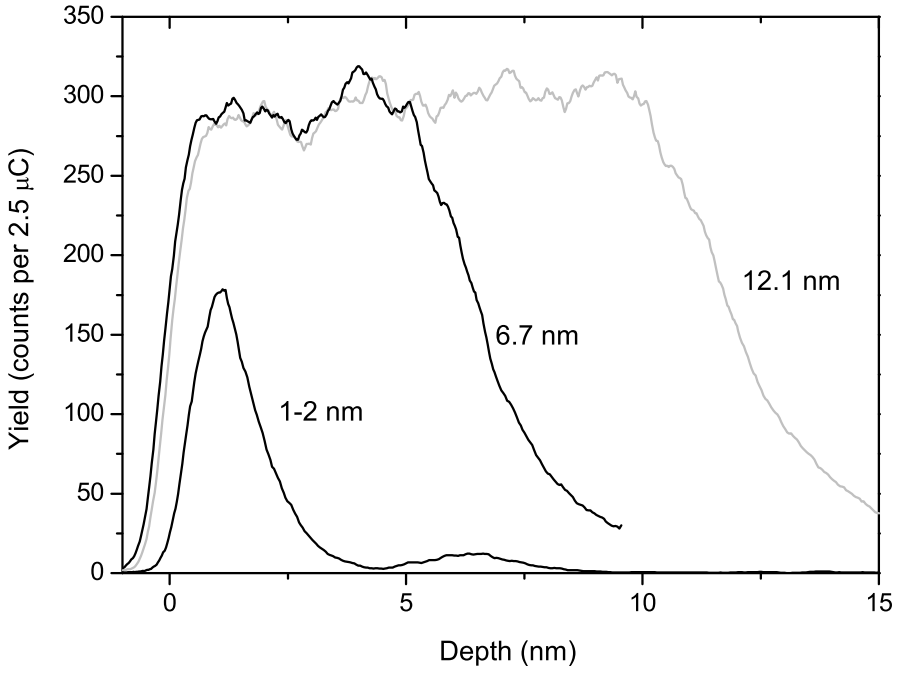

FIGURE 7.13: MEIS Hf depth profiles for Ce-HfO$_2$ films of three different thicknesses.

12.5%.

7.3.3 Ce-HfO$_2$ electrical measurements

C-V

Figure 7.14 shows the C-V measurements for Ce-HfO$_2$ films as-grown and after the two different vacuum anneals. The relative permittivity of the films was taken from the accumulation capacitance at 100 kHz assuming a ∼2 nm SiO$_2$ interlayer. The κ values extracted from the curves are 21, 26 and 31 for the 850 °C, as-grown and 500 °C specimens respectively. The 500 °C-treated specimen especially demonstrates a significant improvement in permittivity compared to un-doped HfO$_2$. The plots show that the molar volume modulation of the metastable phase retention provides a higher κ value and also that the metastable phase retained in the films was cubic Ce-HfO$_2$ as a higher κ would have been expected from the tetragonal phase. The Raman measurements of

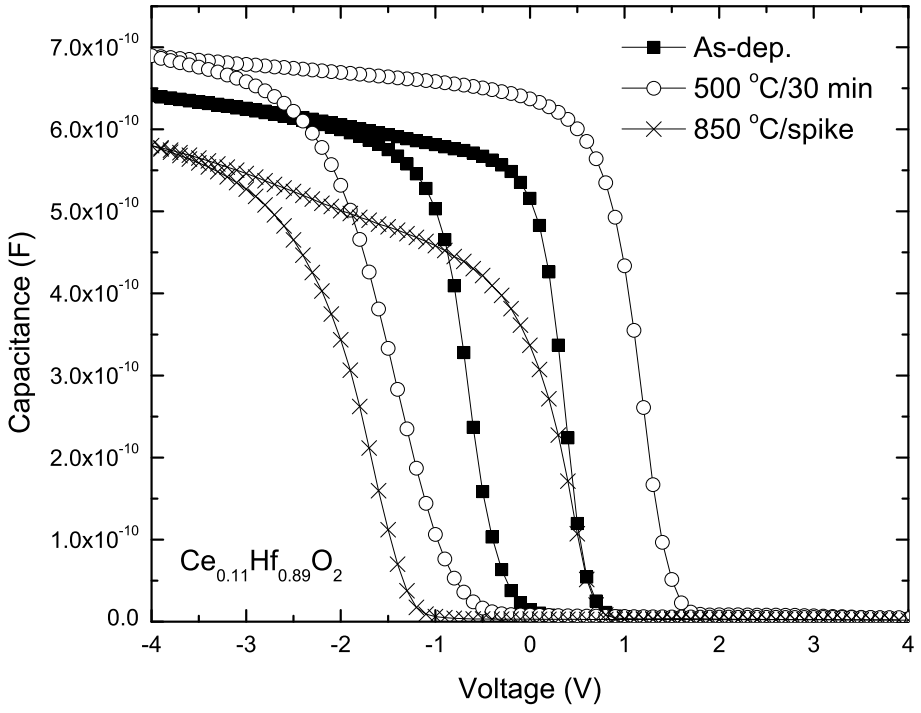

FIGURE 7.14: Capacitance-voltage measurements for Ce-HfO$_2$ films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals.

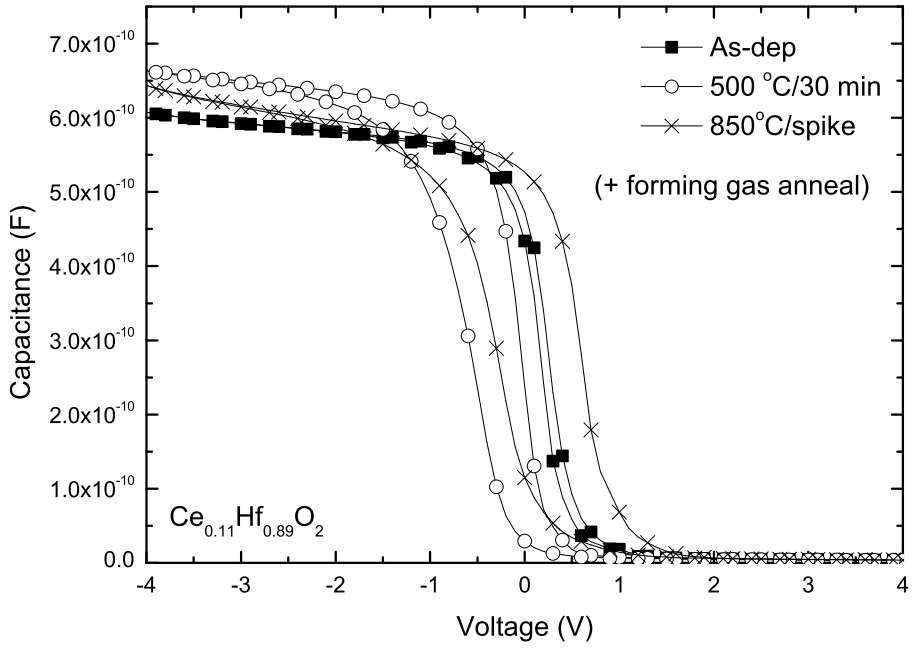

FIGURE 7.15: Capacitance-voltage measurements for Ce-HfO$_2$ films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals. These samples had a further forming gas anneal at 350 °C for 30 minutes

figure 7.11 that suggested some mixed cubic/tetragonal character were for specimens annealed at 1000 °C and it can't be assumed that similar crystallographic forms exist in the samples subjected to electrical assessment. The hysteresis of the curves clearly increases in width after annealing going from ∼1 V for the as-grown film to ∼2 V and ∼2.5 V for the 850 °C and 500 °C anneals respectively. The hysteresis is fairly large in comparison to the other specimens measured using the same methodology. This suggests an increase in trapped oxide charges; specifically as a result of post-deposition heat treatment. The greater hysteresis in comparison to measurements made on the Ti-HfO$_2$ films in the previous chapter (figures 6.12 and 6.13) demonstrate the higher capacity for oxide trapped charge in a crystalline film in comparison to an amorphous one. This indicates that the heat treatment and structural change seen for the Ce-HfO$_2$ films in this chapter are good conditions for defects to be introduced into the lattice. Figure 7.15 presents C-V measurements for films processed in the same way as in figure 7.14

but with an additional 350 °C forming gas[1] anneal performed on the films after the 850 °C/spike and 500 °C/30 min anneals. The effect of this extra heat treatment is to dramatically reduce the hysteresis width and V-axis shift previously seen in the Ce-HfO_2 C-V measurements. This type of forming gas treatment has been shown to reduce the hysteresis and voltage shift in HfO_2 film C-V plots by reducing the oxide trapped and interface charges in the films [150, 151]. Similar hysteresis and passivation has also been reported for Gd_2O_3 film on Si(100) substrates [152]. The capacitance values also become more similar after this further heat treatment with κ values extracted from the curves of 26, 23 and 28 for the 850 °C, as-grown and 500 °C specimens respectively. The application of a forming gas anneal can be said to slightly reduce the permittivity enhancement of this materials system while significantly reducing the C-V evidence of significant oxide trapped charges in the films.

J-E

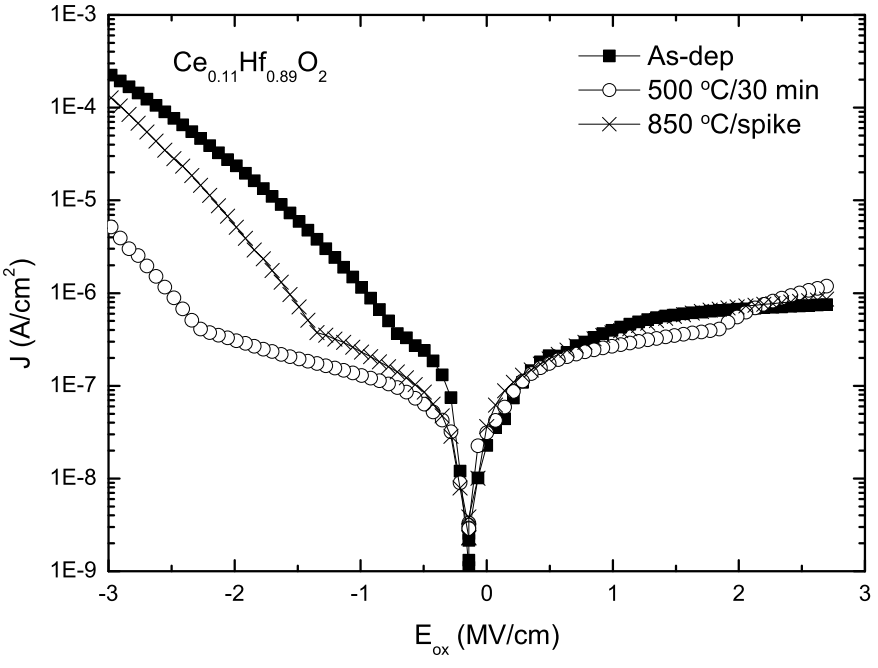

FIGURE 7.16: J-E measurements for $Ce_{0.11}Hf_{0.89}O_2$ films as-deposited and after the 850 °C/spike and 500 °C/30 min anneals.

[1]Forming gas is a H_2/N_2 mixture, the use of which is intended to provide reaction-ready H atoms.

Current voltage density measurements are shown in figure 7.16. The as-grown specimen has a leakage current density at a field of -1 MV cm^{-1} of 1.32×10^{-6} A/cm^2. After the 500 °C/30 min and 850 °C/spike anneals the leakage current density decreases to 1.34×10^{-7} A/cm^2 and 2.46×10^{-7} A/cm^2 respectively at -1 MV cm^{-1}. The values taken at -2 MV cm^{-1} are 2.56×10^{-5}, 3.17×10^{-7} and 5.94×10^{-6} for the as-deposited, 500 °C/30 min and 850 °C/spike specimens respectively. These values show an improved leakage current density for the 500 °C/30 min, or 'gate-last', type of annealing strategy. This observation appears to be connected to a difference in the crystallinity between the slower and faster annealing regimes as can be seen in the difference in the C/T(111) peaks in the XRD shown in figure 7.9. As with the previous J-E data an offset of -0.2 MV/cm is noticeable where the curve switches polarity at $\sim10^{-9}$ A/cm^2, demonstrating built-in charge in the MOS test structure.

7.4 Chapter summary

CeO_2: Cerium oxide deposition is reported via thermal ALD using [Ce(mmp)$_4$] and water as precursors. The films were shown to form a cubic crystalline phase as-deposited from XRD and Raman data (figures 7.3 and 7.4). Changes in the FWHM widths of the (111) XRD peak and triply degenerate F_{2g} Raman mode were related to grain size increase with deposition temperature, as well as a contribution in both related to lattice strain. C-V measurements performed at 1 MHz resulted in a permittivity of 42 and 25 for the 150 °C and 350 °C deposition temperatures respectively. C-f measurements (figure 7.8) demonstrated a large dielectric relaxation in the 150 °C deposition temperature specimen from 1 kHz to 1 MHz. This phenomenon is related to the contribution to capacitance from the larger grain boundary surface area of the smaller-grained 150 °C sample, and dielectric relaxation of this effect with increasing measurement frequency.

Ce-HfO_2: Thermal ALD using $(MeCp)_2Hf(OMe)(Me)$, Ce(mmp)$_4$ and water was shown to be a viable fabrication route for the deposition of Ce-HfO_2 films. This is potentially a preferable manufacturing route to the previous Ce-HfO_2 deposition reports that used O_3 as an oxidiser during ALD. Films of composition $Ce_{0.11}Hf_{0.89}O_2$ were deposited and shown to be amorphous as-deposited. This suggests that the $Ce_{0.11}Hf_{0.89}O_2$ system is

network modified at the deposition temperature of 350 °C as HfO_2 has shown to nucleate a predominantly monoclinic crystalline phase at this temperature. After the 850 °C/spike and 500 °C/30 min anneals the films were shown to form a metastable cubic/tetragonal phase from the XRD and Raman measurements in figures 7.9 and 7.11. The as-deposited and 500 °C/30 min annealed samples demonstrated higher permittivities than undoped HfO_2 of 26 and 31 respectively. These improvements are attributed to a molar volume modulation of the material by the retention of the metastable phase. The 850 °C/spike annealed specimen had a lower permittivity of 21; the sharper XRD peaks in figure 7.9 suggest the slower anneal attained a better crystallinity than the spike anneal which may explain the dielectric measurement difference. The leakage current density of both types of anneal were lower than the as-deposited sample showing that despite developing a crystalline form, with grain boundary paths for current, the permittivity and leakage current density are improved with annealing.

Chapter 8

Comparison and conclusions

8.1 Materials comparison

The specific goal of this thesis was to deposit and analyse thin film ALD materials based on a HfO_2 matrix and achieve a relative improvement in dielectric properties. Two material systems were produced that demonstrated superior dielectric properties to undoped HfO_2. The two types of addition were shown to contribute differently to the dielectric properties enhancement via different morphological mechanisms in the films. Ce was found to be a substitutional addition which enabled the retention of a metastable, higher-κ phase in the material after heat treatment. Ti was found to act as a network modifier, promoting the retention of an amorphous structure after heat treatment. Figures 8.1 and 8.2 sum up the figures of merit for the HfO_2-based materials systems analysed with the HfO_2 values included for reference. Figure 8.1 plots κ values at 100 kHz for the $Ti_{0.1}Hf_{0.9}O_2$, $Ti_{0.5}Hf_{0.5}O_2$ and $Ce_{0.11}Hf_{0.89}O_2$ systems split into post-deposition treatment columns. The box in the top left corner contains the material/treatment combinations that have resulted in significant permittivity improvements compared to un-doped HfO_2. These are the $Ce_{0.11}Hf_{0.89}O_2$ material, which is amorphous as-deposited and has cubic/tetragonal crystallinity after annealing, and the $Ti_{0.5}Hf_{0.5}O_2$ material which demonstrated an amorphous structure as-deposited and after annealing. The dielectric improvements are attributed to molar volume modulation in the former case and the effect of combining HfO_2 with a high proportion of a highly polarisable

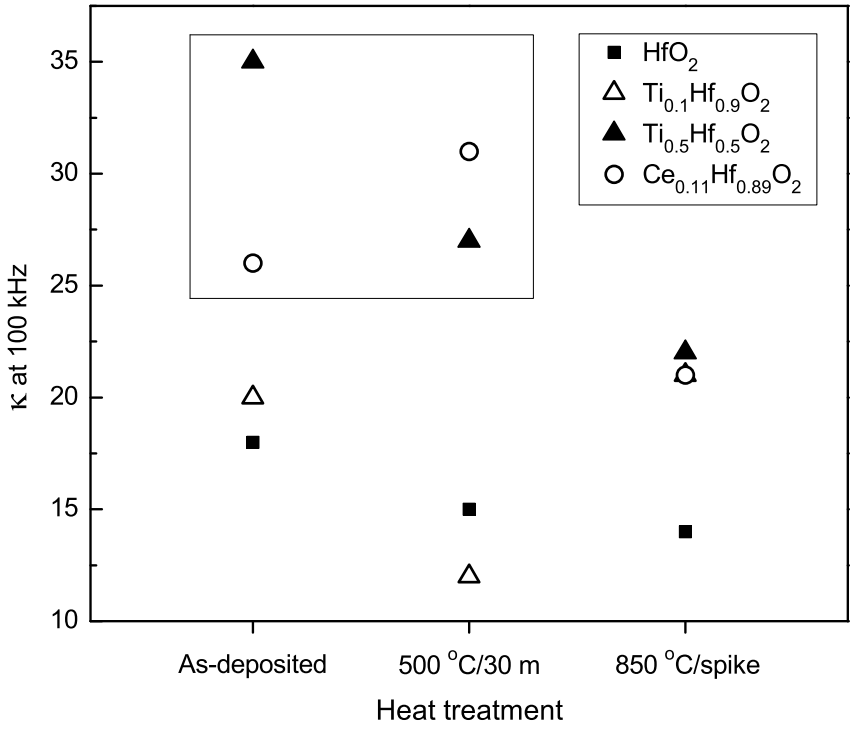

FIGURE 8.1: κ values at 100 kHz for the HfO_2-based materials covered in this thesis.

addition in the latter. Incorporating 10% Ti in a HfO_2 matrix has been shown not to make an improvement on the dielectric properties of un-doped HfO_2.

Figure 8.2 summarises leakage current density measurements for the same materials/heat treatments as in figure 8.1 taken at -1 MV/cm. This shows that the materials with impressive κ values named above also demonstrated excellent leakage current density values after the 500 °C/30 min annealing regime. The $Ce_{0.11}Hf_{0.89}O_2$ sample also shows a low leakage current density after the 850 °C/spike anneal, with the $Ti_{0.5}Hf_{0.5}O_2$ material showing an order of magnitude higher leakage current density after this treatment. The reason for this difference is unclear and it was not possible to produce a TEM specimen to closely examine the physical structure of the $Ti_{0.5}Hf_{0.5}O_2$ material after it had been subjected to the faster, higher temperature heat treatment. All J-E plots demonstrated an offset of around -0.2 MV/cm; with an opposite offset seen for the CeO_2 specimens fabricated on n-type substrates. One likely cause of the general offset seen for most of the samples is the work function difference between the doped substrates

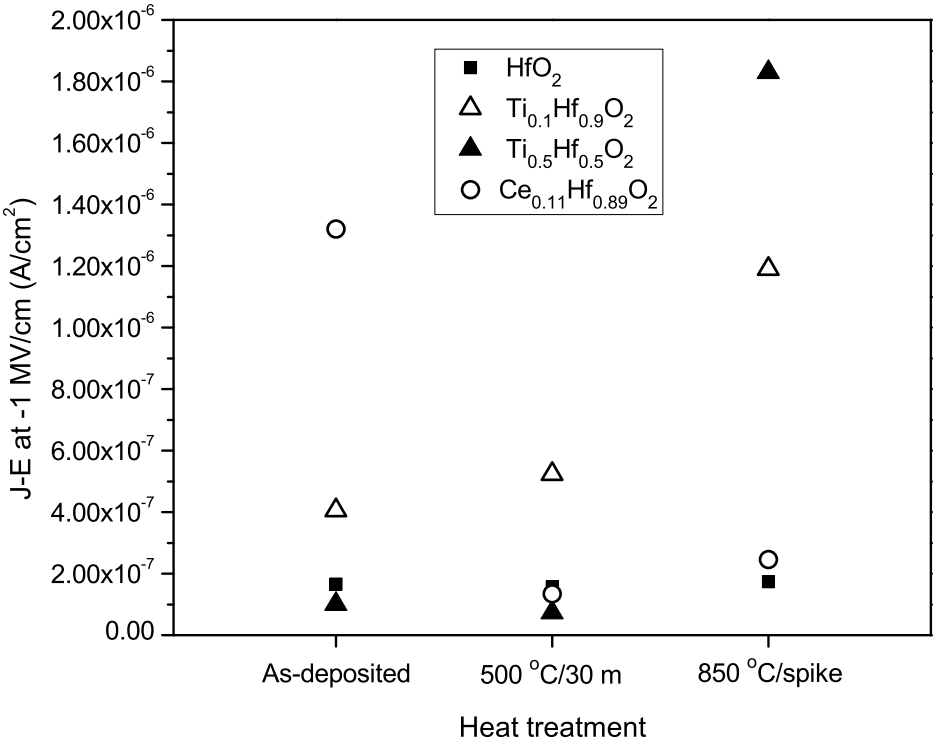

FIGURE 8.2: Current density measurements at -1 MV/cm for the HfO_2-based materials covered in this thesis.

and the gold contacts used in the MOS test structures. The change in offset seen for the CeO_2 samples is interesting as it occurs for the same material with different growth temperature and therefore different grain size and crystallinity. Similarly, the slight difference in this offset highlighted for the 10/50%Ti additions to HfO_2 show that some built-in charge is related to the change in crystallinity between these two specimen sets. The post-deposition anneals appeared to have no effect on these offsets. The C-V plot all demonstrated a large hysteresis; this was especially prevalent in the $Ce_{0.11}Hf_{0.89}O_2$ material. An additional forming gas anneal was found to alleviate the effect by reducing the oxide trapped and interfacial charges present in the specimens.

8.2 Main conclusions

These observations lead to the following conclusions:

1) the $Ti_{0.5}Hf_{0.5}O_2$ and $Ce_{0.11}Hf_{0.89}O_2$ materials, or similar compositions, are promising high-κ candidates for the next iteration of nanotransistors;

2) the 500 °C/30 minute annealing regime, which mimics the 'gate-last' manufacturing approach, has resulted in superior dielectric response, and leakage current density, to the 850 °C/spike anneal;

3) thermal ALD with advance precursors and water is a viable deposition technology to produce ternary dielectric oxide that improve on the properties of HfO_2;

4) amorphous and polycrystalline dielectric film options exist which deliver superior capacitance density along with acceptable leakage current density in comparison with HfO_2.

8.3 Further research opportunities

As the fabrication industry tend to report that a "hafnium based high-κ dielectric" are used in the latest high volume CMOS production [5] only speculation on the materials system used is possible. What can be said is that alongside 193 nm immersion photolithography, ALD hafnium based dielectrics represent the state of the art in fabrication technology. The successful materials systems developed in this thesis might demonstrate further progression that can be attained from the planar or Trigate-type transistor formats by way of higher capacitance density materials that can be used to prevent excessive leakage current density in the devices. An ALD solution is likely to be popular for the next technology node iteration being that full scale transistor fabs have adopted the technology. The industry switch to HfO_2 was a sea change in manufacturing, but still a stop-gap in the continuation of logic devices that demonstrate better

performance with each iteration. There are several areas in which future improvements could be made to the thin film dielectric using the HfO_2/metal gate fabrication switch as a springboard.

New materials development. Whichever hafnium based material is currently used, it is likely that more functionality can be gleaned from the system via a number of modifications. If the current system is a hafnium nitride then the employment of one of the addition elements summarised in chapter 2, or one of the materials developed in this work, could further develop the thin film dielectric from the current situation. Whichever ALD materials system is utilised, there are opportunities to develop new precursors that deliver conformal films with a very low defect concentration. Additionally there is the option of moving into a completely new material such as La_2O_3 [153] if its instability in air and hydroscopic nature could be circumnavigated. Experiments with precursors to deposit rare earth oxides might lead to solutions if the new materials can deliver properties that make another shift in manufacturing worthwhile [154]. Additionally the use of a germanium [155] or silicon-germanium [156] high mobility channel could be a way of improving device characteristics.

New device geometries. While the Trigate device maintains a quasi-planar geometry to be compatible with current manufacturing set ups, another avenue to enhanced device performance would be a switch to another type of geometry. The Trigate is a compromise on the idea of a FinFET, the first of which was proposed in 1999 [157]. These devices suppress short channel effects by utilising an ultra-thin Si channel capped with SiO_2, with a polycrystalline SiGe source and drain. Work on advancements to that original silicon-on-insulator design continues to the present day [158]. The concept of reducing the sub-threshold device performance, important in low power applications, has also opened up the idea of transistor structures that make use of 'negative capacitance'. The idea here is an effectively negative capacitance from the unstable field/polarisation of a ferroelectric material, stabilised by using the ferroelectric in tandem with a dielectric [159].

References

[1] K. Mistry et al., in *IEEE Int. El. Devices Meet.*, pages 247–250, 2007.

[2] M. T. Bohr, R. S. Chau, T. Ghani, and K. Mistry, IEEE Spect. **October**, 29 (2007).

[3] Private communication with C. Auth via email (24/07/2012).

[4] P. Packan et al., in *IEEE Int. El. Devices Meet.*, pages 1–4, 2009.

[5] C. Auth et al., in *VLSI Tech. Symp.*, pages 131–132, 2012.

[6] C. C. Hu, *Modern Semiconductor Devices for Integrated Circuits*, Prentice Hall, 1st edition, 2009.

[7] R. Waser, editor, *Nanoelectronics and Information Technology*, chapter 14, WILEY-VCH Verlag and Co., 3rd edition, 2012.

[8] J. Suné, P. Olivo, and B. Riccó, in *IEEE Trans. Electron Devices*, volume 39, pages 1732–1739, 1992.

[9] D. A. Muller et al., Nature **399**, 758 (1999).

[10] M. Schulz, Nature **399**, 729 (1999).

[11] K. Henson et al., in *IEEE Int. El. Devices Meet.*, pages 1–4, 2008.

[12] J. H. Choi, Y. Mao, and J. P. Chang, Mater. Sci. Eng.: R **72**, 97 (2011).

[13] M. Lundstrom, http://nanohub.org/resources/5363 "ECE 612 Lecture 3: MOS Capacitors" (2008).

[14] A. Callegari, E. Cartier, M. Gribelyuk, H. F. Okorn-Schmidt, and T. Zabel, J. Appl. Phys. **90**, 6466 (2001).

[15] S. C. Barron and R. B. van Dover, in *MRS Proc.*, volume 902, 2005.

[16] A. Toriumi and K. Kita, *Material Engineering of High-κ Dielectrics*, John Wiley & Sons Ltd., 2007.

[17] K. Tomida, K. Kita, and A. Toriumi, Appl. Phys. Lett. **89**, 142902 (2006).

[18] D. Fischer and A. Kersch, Microelectron. Eng. **84**, 2039 (2007).

[19] G. H. Chen, Z. F. Hou, X. G. Gong, and Q. Li, J. Appl. Phys. **104**, 074101 (2008).

[20] C.-K. Lee, E. Cho, H.-S. Lee, C. S. Hwang, and S. Han, Phys. Rev. B **78**, 012102 (2008).

[21] K. Tu, Mater. Sci. Eng. A **A134**, 1244 (1991).

[22] R. B. Schwarz and W. L. Johnson, Phys. Rev. Lett. **51**, 415 (1983).

[23] A. R. Yavari and P. J. Desré, Phys. Rev. Lett. **65**, 2571 (1990).

[24] R. D. Shannon, Acta. Cryst. **A32**, 751 (1976).

[25] W. Lur and L. J. Chen, Appl. Phys. Lett. **54**, 1217 (1989).

[26] J. Hergenrother et al., in *IEEE Int. El. Devices Meet.*, pages 3.1.1–3.1.4, 2001.

[27] Y. Kim et al., in *VLSI Tech. Symp.*, pages 167–168, 2003.

[28] R. Chau et al., IEEE Electron Device Lett. **25**, 408 (2004).

[29] R. Puthenkovilakam, M. Sawkar, and J. P. Chang, Appl. Phys. Lett. **86**, 202902 (2005).

[30] Y. F. Loo et al., Chem. Vapor Depos. **11**, 299 (2005).

[31] S. X. Lao, R. M. Martin, and J. P. Chang, J. Vac. Sci. Technol. A **23**, 488 (2005).

[32] R. J. Potter et al., Chem. Vapor Depos. **11**, 159 (2005).

[33] J. Niinistö et al., Chem. Mater. **19**, 3319 (2007).

[34] C. L. Dezelah et al., Chem. Vapor Depos. **14**, 358 (2008).

[35] K. Black et al., J. Mater. Chem. **18**, 4561 (2008).

[36] J. C. Kim, J. S. Heo, Y. S. Cho, and S. H. Moon, Thin Solid Films **517**, 5695 (2009).

[37] J. Niinistö et al., J. Cryst. Growth **312**, 245 (2010).

[38] H. Y. Yu, M. F. Li, and D. L. Kwong, Thin Solid Films **462-463**, 110 (2004).

[39] O. Buiu et al., Thin Solid Films **515**, 3772 (2007).

[40] G. D. Wilk et al., in *VLSI Tech. Symp.*, pages 88–89, 2002.

[41] M. S. Joo et al., Jpn. J. Appl. Phys. **42**, L220 (2003).

[42] S.-H. Kim and S.-W. Rhee, Chem. Vapor Depos. **12**, 125 (2006).

[43] G. Lupina et al., Chem. Vapor Depos. **15**, 167 (2009).

[44] N. Umezawa, Appl. Phys. Lett. **94**, 022903 (2009).

[45] H. Zhao, A. Chang, and Y. Wang, Physica B **404**, 2192 (2009).

[46] P. R. Chalker et al., Appl. Phys. Lett. **93**, 182911 (2008).

[47] C. Adelmann et al., Chem. Vapor Depos. **13**, 567 (2007).

[48] T. Lee et al., J. Vac. Sci. Technol. B **29**, 021209 (2011).

[49] K. B. Jinesh et al., J. Mater. Res. **25**, 1629 (2010).

[50] L. Wu et al., Electrochem. Solid St. Lett. **13**, G21 (2010).

[51] C. Adelmann et al., J. Electrochem. Soc. **157**, G105 (2010).

[52] X. Zhang et al., in *IEEE ICSICT*, pages 1036–1038, 2010.

[53] X. Wang et al., Mater. Sci. Forum **687**, 209.

[54] Z. Wang et al., in *IEEE Trans. Electron Devices*, volume 59, pages 1203–1208, 2012.

[55] Y. Yamamoto, K. Kita, K. Kyuno, and A. Toriumi, Appl. Phys. Lett. **89**, 032903 (2006).

[56] Y. F. Loo, S. Taylor, R. T. Murray, A. C. Jones, and P. R. Chalker, J. Appl. Phys. **99**, 103704 (2006).

[57] L.-Y. Huang et al., Appl. Surf. Sci. **256**, 2496 (2010).

[58] W.-S. Kim et al., J. Vac. Sci. Technol. B **26**, 1588 (2008).

[59] T. Wang and J. G. Ekerdt, Chem. Mater. **21**, 3096 (2009).

[60] T.-Y. Jang et al., Microelectron. Eng. **88**, 1373 (2011).

[61] C. Z. Zhao et al., J. Vac. Sci. Technol. B **27**, 333 (2009).

[62] T. S. Böscke et al., Appl. Phys. Lett. **91**, 072902 (2007).

[63] J. Kim, S. Lee, and K. Yong, Jpn. J. Appl. Phys. **45**, 7080 (2006).

[64] A. Abrutis, L. G. Hubert-Pfalzgraf, S. Pasko, N. Touati, and V. Kazlauskiene, Vacuum **81**, 13 (2006).

[65] K. Black, M. Werner, R. Rowlands-Jones, P. R. Chalker, and M. Rosseinsky, Chem. Mater. **23**, 2518 (2011).

[66] S. Mallik, C. Mahata, M. K. Hota, C. K. Sarkar, and C. K. Maiti, Thin Solid Films **520**, 101 (2011).

[67] I. Oja et al., Thin Solid Films **515**, 674 (2006).

[68] J. Aarik, A. Aidla, T. Uustare, and V. Sammelselg, J. Cryst. Growth **148**, 268 (1995).

[69] J. Aarik et al., Appl. Surf. Sci. **193**, 277 (2002).

[70] M. Ritala, M. Leskela, L. Niinisto, and P. Haussalo, Chem. Mater. **5**, 1174 (1993).

[71] F. Chen et al., Microelectron. Eng. **72**, 263 (2004).

[72] S. J. Rhee et al., in *VLSI Tech. Symp.*, pages 168–169, 2005.

[73] D. H. Triyoso et al., J. Appl. Phys. **98**, 054104 (2005).

[74] M. Li et al., J. Appl. Phys. **98**, 054506 (2005).

[75] K. Tomida et al., IOP C Ser. Mater. Sci. Eng. **8**, 012023 (2010).

[76] C. Ye et al., J. Appl. Phys. **107**, 104103 (2010).

[77] H. Mölsä, L. Niinistö, and M. Utriainen, Adv. Mater. Opt. Electr. **4**, 389 (1994).

[78] J. Niinistö, M. Putkonen, and L. Niinistö, Chem. Mater. **16**, 2953 (2004).

[79] P. de Rouffignac, J.-S. Park, and R. G. Gordon, Chem. Mater. **17**, 4808 (2005).

[80] P. Myllymaki et al., J. Mater. Chem. **16**, 563 (2006).

[81] K. Kita, K. Kyuno, and A. Toriumi, Appl. Phys. Lett. **86**, 102906 (2005).

[82] Z. K. Yang et al., Appl. Phys. Lett. **90**, 152908 (2007).

[83] L. Shi, Y. Zhou, J. Yin, and Z. Liu, J. Appl. Phys. **107**, 014104 (2010).

[84] C. Zhao et al., Microelectron. Reliab. **41**, 995 (2001).

[85] K. Kukli et al., J. Cryst. Growth **231**, 262 (2001).

[86] J. Niinistö et al., J. Appl. Phys. **95**, 84 (2004).

[87] M. Silinskas, M. Lisker, S. Matichyn, B. Kalkofen, and E. P. Burte, Mater. Sci. Semicon. Proc. **9**, 1037 (2006).

[88] J. M. Gaskell et al., Surf. Coat. Tech. **201**, 9095 (2007).

[89] J. Niinistö et al., J. Mater. Chem. **18**, 5243 (2008).

[90] Y. Kuo et al., ECS Trans. **1**, 447 (2006).

[91] D. H. Triyoso et al., Appl. Phys. Lett. **88**, 222901 (2006).

[92] J. Müller et al., Appl. Phys. Lett. **99**, 112901 (2011).

[93] T. S. Böscke, P. Y. Hung, P. D. Kirsch, M. A. Quevedo-Lopez, and R. Ramírez-Bon, Appl. Phys. Lett. **95**, 052904 (2009).

[94] S. P. Consiglio et al., ECS Trans. **28**, 125 (2010).

[95] W. Zhang, L. Huang, A. Li, Q. Shao, and D. Wu, in *ISNE*, pages 66–68, 2010.

[96] M.-Y. Ho et al., J. Appl. Phys. **93**, 1477 (2003).

[97] K. Kukli et al., Chem. Mater. **15**, 1722 (2003).

[98] K. Kukli et al., Chemical Vapor Deposition **10**, 91 (2004).

[99] Y.-K. Chiou, C.-H. Chang, and T.-B. Wu, J. Mater. Res. **22**, 1899 (2007).

[100] D. McNeill et al., J. Mater. Sci.: Mater. El. **19**, 119 (2008).

[101] W. Zhu, T. Tamagawa, M. Gibson, T. Furukawa, and T. Ma, IEEE Electron Device Lett. **23**, 649 (2002).

[102] J. Gluch, T. Rößler, S. Menzel, and J. Eckert, Microelectron. Eng. **88**, 561 (2011).

[103] M. Ritala and M. Leskelä, *Handbook of Thin Film Materials*, volume 1, chapter 2, pages 103–159, Academic Press, 2002.

[104] S. M. George, Chem. Rev. **110**, 111 (2010).

[105] P. D. Kirsch, M. A. Quevedo-Lopez, H.-J. Li, Y. Senzaki, and J. J. Peterson, J. Appl. Phys. **99**, 023508 (2006).

[106] C. B. Musgrave and R. G. Gordon, Future Fab Init. **18**, 126 (2005).

[107] R. G. Gordon, Tutorial 'Overview of ALD Precursors and Reaction Mechanisms' presented at AVS ALD (2011).

[108] M. M. Frank et al., Microelectron. Eng. **86**, 1603 (2009).

[109] H. Gottlob et al., J. Non-Cryst. Solids **351**, 1885 (2005).

[110] J. D. Gardiner, *Practical Raman Spectroscopy*, Springer, 1st edition, 1989.

[111] M. Werner, *Damage formation and annealing studies of low energy ion implants in silicon using medium energy ion scattering*, PhD thesis, University of Liverpool, 2006.

[112] Z. Fang, *Atomic layer deposition of tantalum, hafnium and gadolinium nitrides*, PhD thesis, The University of Liverpool, 2011.

[113] A. Coban, E. E. Khawaja, and S. M. A. Durrani, Nucl. Instrum. Meth. B **194**, 171 (2002).

[114] P. Bailey, T. C. Q. Noakes, and D. P. Woodruff, Surf. Sci. **426**, 358 (1999).

[115] M. A. Reading et al., J. Vac. Sci. Technol. B **28**, C1C65 (2010).

[116] N. Arora, *Mosfet Modeling for VLSI Simulation: Theory And Practice*, World Scientific Publishing, 2007.

[117] S. M. Sze, *Semiconductor Devices: Physics and Technology*, John Wiley & Sons Inc., 2nd edition, 2002.

[118] D. M. Fleetwood, S. T. Pantelides, and R. D. Schrimpf, *Defects in Microelectronic Materials and Devices*, CRC Press, 2008.

[119] j. Robertson, Rep. Prog. Phys. **69**, 327 (2006).

[120] D. W. Greve and V. R. Hay, J. Appl. Phys. **61**, 1176 (1986).

[121] R. Kotlyar et al., in *IEEE Int. El. Devices Meet.*, pages 391–394, 2004.

[122] J. R. Watling et al., J. Comput. Theor. Nanos. **5**, 1072 (2008).

[123] A. Debernardi and M. Fanciulli, Mats. Sci. Semicon. Proc. **9**, 1014 (2006).

[124] P. Mishra and K. P. Jain, Phys. Rev. B **64**, 073304 (2001).

[125] J. Robertson, J. Non-Cryst. Solids **303**, 94 (2002).

[126] F. M. Pontes, E. J. H. Lee, E. R. Leite, E. Longo, and J. A. Varela, J. Mater. Sci. **35**, 4783 (2000).

[127] R. Pheamhom, C. Sunwoo, and D.-H. Kim, J. Vac. Sci. Technol. A **24**, 1535 (2006).

[128] H. Rath et al., J. Appl. Phys. **105**, 074311 (2009).

[129] J. Aarik, A. Aidla, T. Uustare, M. Ritala, and M. Leskelä, Appl. Surf. Sci. **161**, 385 (2000).

[130] V. Bessergenev and H. L. Gomes, Phys. Status Solidi C **7**, 949 (2010).

[131] R. Thomas et al., Ferroelectrics **327**, 111 (2005).

[132] Q. Tao, G. Jursich, and C. Takoudis, in *IEEE Trans. Semicond. Manuf.*, volume 24, pages 139–144, 2011.

[133] G. Dutta, Appl. Phys. Lett. **94**, 012907 (2009).

[134] M. A. Krebs and R. A. Condrate, J. Mater. Sci. Lett. **7**, 1327 (1988).

[135] M. Werner et al., Nucl. Instrum. Meth. B **216**, 67 (2004).

[136] J. W. Elam and S. M. George, Chem. Mater. **15**, 1020 (2003).

[137] D. M. noz Ramo, A. L. Shluger, and G. Bersuker, Phys. Rev. B **79**, 035306 (2009).

[138] A. Paskaleva, M. Lemberger, E. Atanassova, and A. J. Bauer, J. Vac. Sci. Technol. B **29**, 01AA03 (2011).

[139] P. Scherrer, Gött Nachr **2**, 98 (1918).

[140] W. H. Weber, K. C. Hass, and J. R. McBride, Phys. Rev. B **48**, 178 (1993).

[141] F. Zhang et al., Appl. Phys. Lett. **80**, 127 (2002).

[142] S. Saitzek, J.-F. Blach, S. Villain, and J.-R. Gavarri, Phys. Status Solidi A **205**, 1534 (2008).

[143] I. Kosacki, T. Suzuki, H. U. Anderson, and P. Colomban, Solid State Ionics **149**, 99 (2002).

[144] H. Yu et al., Appl. Phys. Lett. **91**, 222911 (2007).

[145] N. Sivakumar, A. Narayanasamy, C. N. Chinnasamy, and B. Jeyadevan, J. Phys. Part C: Solid **19**, 386201 (2007).

[146] C. Z. Zhao et al., J. Appl. Phys. **105**, 044102 (2009).

[147] D. Fischer and A. Kersch, Appl. Phys. Lett. **92**, 012908 (2008).

[148] M. Villanueva-Ibañez, C. Le Luyer, O. Marty, and J. Mugnier, Opt. Mater. **24**, 51 (2003).

[149] M. Hartmanová, F. Hanic, K. Putyera, D. Tunega, and V. B. Glushkova, Mater. Chem. Phys. **34**, 175 (1993).

[150] A. S. Zoolfakar, H. Hashim, and S. Taylor, in *IEEE ICSICT*, pages 1268–1271, 2008.

[151] S. Y. Tan, J. Electron. Mater. **39**, 2435 (2010).

[152] Q.-Q. Sun et al., Appl. Phys. Lett. **92**, 152908 (2008).

[153] L. Chen et al., J. Vac. Sci. Technol. A **30**, 01A148 (2012).

[154] A. Milanov et al., Dalton Trans. **41**, 13936 (2012).

[155] C. Le Royer, Microelectron. Eng. **88**, 1541 (2011).

[156] C.-C. Li et al., Solid-State Electron. **78**, 17 (2012).

[157] X. Huang et al., IEEE Int. El. Devices Meet. , 3.4.1 (1999).

[158] E. X. Zhang et al., Solid State Electron. **78**, 75 (2012).

[159] A. I. Khan et al., Appl. Phys. Lett. **99**, 113501 (2011).