Modelling and Control of Power Inverters in Microgrids

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by
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Abstract

Power electronic converter systems play an important role in the interconnection of renewable energy sources in microgrids and utility grid. The interface between energy sources and microgrids is usually implemented by digitally controlled power inverters. This thesis provides a discrete modelling and design method for the digitally controlled inverters in microgrids.

The fundamentals and background of digital control of power inverters are introduced. The small-signal models for digital pulse-width-modulations (PWMs) with delay effects are derived. Based on the models, the controllers can be designed using several methods according to the block diagrams. The simulation software and experimental environment for the digitally controlled inverters are described.

For inverters operating in parallel, a linear voltage control scheme with duty-ratio feedforward is proposed. The control parameters are chosen according to the stable operating condition derived in z-domain. The closed-loop transfer function and output impedance for both the classical controller and the proposed controller are derived theoretically. A comparison reveals the advantages of the proposed control scheme: a unity closed-loop gain, no phase shift, good current sharing and low total harmonic distortion (THD) of the output voltage. The theoretical results are verified by the experimental setup of a system with two digitally controlled inverters connected in parallel.

For digitally controlled grid-connected inverters with LCL filters, new small-signal z-domain models are deduced. The proposed methods model the inverters including different delay effects under most possible circumstances, which allows a direct design for controllers in z-domain. The stability boundaries obtained from the root loci of the classic models and the proposed models are compared to the simulation results, showing that the proposed z-domain models are more accurate in predicting instabilities. Experimental results are presented, showing the proposed models are also capable of predicting the values of control variables at the true sampling instants.

The phase-shifted modulated multisampled multilevel inverter is studied. The filter current ripple frequency of the multilevel inverters is increased by the phase-shifted PWM. The small-signal z-domain model is derived. Compared to the bipolar switched inverter, the multisampled multilevel inverter is characterized by the capability of achieving higher feedback control gains, which improves the control performance. An experimental prototype based on a 10 kHz switching frequency, 80 kHz sampling frequency five-level single-phase H bridge inverter is tested to demonstrate the validity of the analysis.

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Chapter 1

Introduction

1.1 Power electronics in microgrids

The concept of distributed generation (DG) becomes promising when more and more renewable energy sources such as solar energy, wind energy and hydroenergy are available in reality. This is becoming important due to environmental, social and political interests. Energy from these resources can be transmitted via power electronics systems to local electric power networks. The local low-voltage electric power systems, including power generation, energy storage and loads, are connected to the conventional centralized grid and can also be disconnected from the grid. These local electric power systems are known as microgrids [1, 2, 3, 4, 5]. In such systems, dc-ac inverters (or ac-ac converters) are connected to local common bus. Due to the long distances between each inverter, these inverters are operating without intercommunications to provide power for local loads or remote loads in the grid.

For dc-ac inverters providing power to local loads without connecting to the grid, the inverters are operating in islanding mode. However, if the inverters provide power to remote loads in the grid, the inverters are operating in grid-connected mode. The islanding operation and the grid-connected operation are the main operation modes of microgrids. For the islanding operation, the inverters are disconnected from the grid and supply energy to their common loads in parallel, where a system of parallel inverters is a good paradigm. These parallel inverters provide energy only for local loads and are designed to share the power demanded by their loads. Moreover, if one unit fails to operate properly, it can quit the system of parallel inverters without causing instabilities. At the same time, the power required by the local loads will be retrieved from the other units. If the parallel inverters are not capable of maintaining the voltage level on the loads, more inverters can be connected to the point of common coupling (PCC). Consequently, such a system exhibits flexibility, reliability and redundancy while

supplying energy to the local loads.

However, when there are more energy generated than the demands from local loads, the inverters in microgrids can provide energy to the remote loads in the grid. In that case, each unit can be considered as an independent grid-connected inverter, as long as the grid voltage is not affected by the inverters in a microgrid. The grid-connected inverter usually injects a current according to the commanded current in phase with the grid voltage. In order to achieve a high power factor, phase locked loops (PLLs) are used for synchronization between the current reference and the grid. Therefore, each grid-connected inverter behaves as a grid voltage controlled current source. The voltage of grid-connected inverters follows the voltage on the PCC.

Generally, inverters with the two main functions mentioned above form a microgrid. Although there are many complicated topologies and structures, this thesis focuses on topics around the two classic operation modes (islanding and grid-connected) of H bridge inverters. Advanced topologies operating in a particular mode are also studied. Modelling methods and design regulations will be presented from the control point of view. Moreover, the main ideas in this thesis can also be extended to other applications in the control of power electronics.

1.2 Digital control of power inverters

Either the islanding operation mode or the grid-connected operation mode requires proper control techniques. As the controllers of the inverters usually have complicated functions to ensure reliability, implementing a controller using analog devices is difficult. Moreover, the flexibility is also limited if analog circuits are mainly used. Under such conditions, the analog controllers are usually used in low power applications to reduce the cost. On the other hand, as the performance/price ratio of digital signal processors (DSPs) is increasing rapidly, nowadays most switching converters are controlled by digital controllers. Digital controllers for medium and high power inverters have the advantages such as lower sensitivity to variation of control parameters, immunity to switching noises, high flexibility and complexity in control algorithms, programmability of controllers and reduction of hardware components.

Due to the advantages of digital controllers, the control algorithms for islanding inverters and/or grid-connected inverters are usually implemented in DSPs. In most cases, a controller for a power inverter can be implemented using a single DSP (e.g., TMS320F28xx, ADSP2199x, etc.). The digital controllers are designed according to the models of the inverters. If higher switching frequency is used to reduce the electromagnetic interference (EMI), the sampling frequency can

also be increased. In that case, high speed controllers are required and field programmable gate arrays (FPGAs) are usually combined with DSPs to implement the high sampling frequency.

For some practical limitations of switching devices, the switching frequency cannot be easily increased. However, the filter input voltage frequency can be increased by the structure of multilevel inverters. This achieves more or less the same filter input voltage frequency as that of the single H bridge inverter with higher switching frequencies. The EMI of the inverters can be reduced dramatically and higher sampling frequency can also be applied according to the level of the inverters. As a result, using the structure of multilevel inverters for islanding operation and grid-connected operation attracts great interests. Plenty of research work focuses on multilevel inverters controlled by one DSP plus one FPGA, with the phase-shifted carriers generated by the FPGA. This hardware arrangement provides sufficient feasibility of implementing complex digital control algorithms for multilevel inverters. The modelling of digitally controlled multilevel inverters are required for controller design.

1.3 Problems in digitally controlled power inverters

Unlike analog controlled power inverters, the knowledge of digitally controlled power inverters is still developing. A digital controller has significant influence on the dynamic behaviour of the control system. As a result, digitally controlled inverters have quite different dynamic behaviours from that of the analog controlled inverters. Accurate models are required for response predictions, since the classic averaged models for analog controlled inverters cannot be simply applied to digitally controlled inverters. The discrete-time models are applicable to digitally controlled systems, but these models cannot be obtained from the continuous-time models by using direct z-transform. More accurate modelling methods are needed for engineers when designing power inverters with the following practical considerations [6, 7, 8].

1.3.1 System stability

Classic average models have been used to evaluate the stability of switching converters [9] and are capable of predicting slow-scale oscillations. However, the fast-scale instabilities such as period-n bifurcation can not be predicted by using the average models [10].

For a digitally controlled system, the stability analysis cannot be performed

using the average model. The main reason is that the sample and hold effect in digital controllers cannot be properly modelled by average models. Moreover, the delay effect differs when different pulse-width-modulation (PWM) strategies are used. Therefore, stability analysis for digitally controlled power inverters should be performed based on z-domain models. Compared to s-domain analysis, z-domain analysis also brings convenience for modelling delay effect and sample and hold effect.

1.3.2 Controller design

Classic average models enables a direct design for controllers in analog controlled power inverters. Based on average models, the controllers can be obtained in s-domain and the control performance can be evaluated by using s-domain analysis. The average models are widely used to evaluate the low frequency control performances of digitally controlled power inverters. However, as the average models cannot predict instabilities in digitally controlled systems, the design of digital controllers based on s-domain analysis may not be able to guarantee an accurate gain margin. Therefore, the z-domain analysis is essential for design of digital controllers.

Based on the z-domain models, the design of digital controllers can be implemented using two strategies. One method is to design the controller directly in z-domain, which requires knowledge of the z-domain model of the inverter. This method allows to implement discrete control schemes such as deadbeat control scheme and repetitive-based control schemes. The other one is the indirect design strategy, which converts the well known classic analog controllers into z-domain. This method requires z-transform of s-domain transfer functions, where bilinear transform is usually used to obtain the z-domain expressions of controllers.

1.3.3 Performance of controller

Steady-state performance and transient performance are important factors for evaluating a controller. The steady-state performance of a digitally controlled system can be evaluated using average models with good accuracy, as long as the interested performance is in low-frequency range. However, the transient response contains signals in a wide frequency range. Using average models may reduce the accuracy in predicting high frequency components. In contrast, z-domain models can be used to evaluated both the steady-state performance and transient performance. z-domain analysis can precisely predict the rise time, settling time and overshot in the transient response.

Robustness is another specification of a controller. Usually a robust digital

controller should have a gain margin of two. Only using a z-domain model the gain margin of a controller can be obtained from the z-plane root locus.

1.3.4 Power quality requirements

Inverters should be designed to meet the power quality requirements. The normal voltage variation of islanding inverters should be within plus and minus 10% of the rated RMS value. The grid-connected inverters do not regulate the voltage, but they inject currents to the grid. Therefore, grid-connected inverters should have protection functions when the grid voltage is out of the normal operating range. The normal frequency range required for a inverter depends on the power level, which can be found in [11]. The standard [11] also provides regulations for the total harmonic distortion (THD) and individual harmonic current levels. These requirements applies to both islanding inverters and grid-connected inverters. The digitally control inverters described in this thesis are designed according to these requirements.

For grid-connected inverters, power factor is specified to be higher than 0.85 when output exceeds 10% of the power rating [12]. However, most grid-connected inverters are able to achieve a power factor close to unity. Another important requirement is that the injected dc current should be smaller than 0.5% of the rated output current [11, 12]. There are some techniques to minimize the dc current. For transformerless inverters, high resolution dc current sensor or auto-calibration [13] can be used to reduce the dc current injection. In our cases, isolation transformers are used to block the dc current injection into the grid. The grid-connected inverters in this thesis are designed according to the power quality requirements.

There are also functions and specifications on the interconnection of the electrical system, such as detection of islanding operation, automatic synchronization and grounding of the system. Moreover, voltage flicker is a subjective problem and has been discussed in IEEE Standard 519-1992, where the maximum borderline of the flicker has been defined. These requirements have to be taken into account in practice but are not included in the modelling of this thesis.

1.4 Overview of the thesis

This thesis focuses on the modelling and control of digitally controlled power inverters in microgrids. These inverters may operate in islanding mode or in grid-connected mode. For islanding operations, stand-alone inverters are used to provide energy in parallel. The stand-alone inverters are controlled as voltage sources. These controllers are always implemented by cascaded control loops with

an internal current control loop [2, 14]. Therefore, an accurate model for cascaded digital control loops has been proposed in this thesis. Based on the model, the controller design and analysis can be performed.

When inverters operate in grid-connected mode, they should behave as current sources. Inductive filters and LCL filters are usually used for grid-connected inverters. The controller of an inverter with inductive filter is easy to design, but for inverters with LCL filter, the design needs to be carefully considered. Moreover, the delay effects significantly affect the dynamic behaviour of the system. The LCL resonance in the high frequency range may lead to instabilities when the controller is not well designed. Hence, a new modelling method for grid-connected LCL inverters with accurately modelled delay effect is proposed in the thesis.

More stand-alone and grid-connected inverters tend to use the multilevel structure to lower the EMI. Many modulation techniques have been proposed for multilevel inverters, but the modelling of the phase-shifted PWM is still not available. Therefore, a general method of modelling digitally controlled multilevel inverters is presented in the thesis, which is also extendible to other modulation technologies.

The thesis is organized as follows. In Chapter 1, a brief introduction about digitally controlled power inverters in microgrids and the problems in this topic are given. Chapter 2 illustrates background and state of the art of the modelling and control for digitally controlled power inverters. Based on Chapter 1 and 2, Chapter 3 first provides the details of discrete modelling, with delay effects taken into account. Then, the block diagrams are derived for single switched switching converters. The model is also extended to H bridge inverters. To demonstrate the feasibility of the proposed model, a design example is provided. Furthermore, preparations for simulation and experimental work are presented.

An example of controller design for stand-alone inverters is shown in Chapter 4. The inverters are designed for parallel operation. The controllers are designed in z-domain, based on the proposed model. The aim of the design is to achieve good current sharing between inverters and to guarantee good power quality. To demonstrate the advantage of the proposed controller, the performance of the proposed controller has been compared to that of the conventional controller.

Chapter 5 gives an example of z-domain modelling for inverter with a third-order filter, i.e., grid-connected inverter with an LCL filter. Inverters with two typical control schemes have been modelled in the z-domain. Compared to the conventional s-domain models, the proposed models accurately predict the stability boundaries of control gains. Moreover, comparison between predictions of

models, simulation and experimental results is provided to verify the capability of the models in predicting stabilities and retrieving time-domain waveforms.

Chapter 6 models the multilevel inverter, which is sampled with a frequency multiple of the switching frequency. These multilevel inverters become quite interesting in many microgrids' applications to increase power rating or to reduce the EMI. However, due to the complexity of the PWM, exact models for multilevel inverters are still not available. Therefore, the modelling method for the multisampled multilevel inverter is proposed. The chapter gives a concise way of modelling and proves that multisampled multilevel inverters can achieve better control performance compared to uniformly-sampled inverters.

Finally, conclusions are made in Chapter 7, which also highlights possible future work that would combine with this research.

Chapter 2

Background

2.1 Introduction

Conventional switching converters are controlled by analog controllers. For modelling and analysis of the switching converters, averaged switching characteristics are usually used [9]. The average modelling method has been widely applied to determine the control performance at low frequency range. However, even for analog controlled switching converters, average models fail to predict rapid dynamics [15]. Therefore, discrete-time maps have been developed as a more accurate modelling strategy [16, 17]. These methods successfully predict the nonlinear behaviour of naturally-sampled switching converters, but usually require solving transcendental equations every cycle to find the switching instants. As a result, approximated discrete-time models are proposed to reduce the computation load involved.

As analysis of digitally controlled switching converters has attracted wide interests in the last decade, the discrete-time mapping has also been applied to this topic [18, 19, 20, 21]. Moreover, for digitally controlled switching converters with sample and hold effect, it is easier to find the switching instants. Bilinear discrete-time mapping has been proposed to show the capability of accurate prediction of instabilities such as bifurcation, strange attractor and chaos [22]. However, for practical controller design and performance analysis, it is more convenient to implement design and analysis in the Laplace domain.

The quantization effect of digitally controlled switching converters has been first studied in [23], where conditions of the limit cycle has been given. Based on these results, a describing function method has been proposed to model the quantization effect [24]. As the performance of DSPs improves and the resolution of analog-to-digital (AD) converters and digital pulse-width-modulators (DPWMs) becomes much greater than before, quantization effects can be neglected from the dynamic point of view [25]. Then, a more accurate model, i.e., small-signal

z-domain model has been derived for DPWMs. This model enables the controller to be directly designed in the z-domain, and provides an evaluation of the controller in Laplace domain [25, 26]. Based on this accurate model, the classic design and analysis methods [27] for digitally controlled switching converters become applicable.

This chapter introduces the fundamentals of digital control for power electronics. Basic principles of sample and hold and z-transform are illustrated. The modelling methods and controller design techniques in the Laplace domain are reviewed. Most commonly used models regardless of quantization effects are provided. Based on the z-domain models, typical digital control strategies are presented.

2.2 Fundamentals of digital control in power electronics

A typical digital controller for a single switched converter is shown in Figure 2.1. The quantities of $q_1, ..., q_m$ represent the analog variables which are required to be measured. Through an analog-to-digital converter (ADC), these quantities are converted to digital signals by ideal samplers, which are represented by $q_1^*, ..., q_m^*$. The digital controller implemented by using a cluster of difference equations, is equivalent to a control block comprised of z-domain transfer functions. The ratio of the switch on time duration to the switching period is defined as the duty-ratio. When a digital duty-ratio is calculated and updated in the PWM compare register as u^*, the zero-order-hold (ZOH) is used to convert u^* into a continuous modulation signal which compares with the carrier to generate the switch drive signals. Hence, the digital PWM is described by a pulse-to-continuous transfer function with a digital input but with an analog output. The fundamental of the

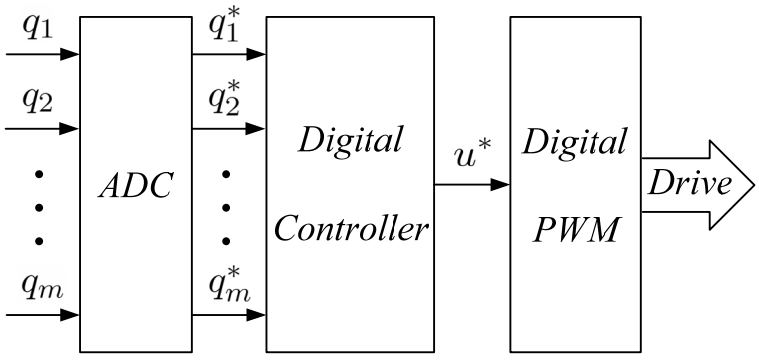


Figure 2.1: The schematic of a typical digital controller.

digital control of switching converters is introduced in the following subsections.

2.2.1 Ideal sampler and ZOH

This subsection explains the conversions and transfer functions between continuous to discrete signals. The principle of sampling and hold in digital controllers can be found in [27]. To convert an analog signal into a digital signal, an ideal sampler is used. The conversion from digital signals to analog signals requires a ZOH. In the digitally controlled system [27], the ideal sampling process is to multiply the analog signal by a Dirac comb constructed from a series of Dirac delta functions, which is written as

$$\delta_T(t) = \sum_{k=-\infty}^{\infty} \delta(t - kT_s) \tag{2.1}$$

with t the time, T_s the sampling period and k the integers. Assuming e^* is the ideally sampled digital signal in respect to the analog error signal e, it can be represented as

$$e^*(t) = e(t)\delta_T(t). \tag{2.2}$$

On the other hand, the Dirac comb is a periodic function, whose Fourier series can be derived as

$$\delta_T(t) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} e^{jk\frac{2\pi}{T_s}t}. \tag{2.3}$$

In order to describe the function of the ideal sampler, Laplace-domain analysis is used. Substituting (2.3) into (2.2), the Laplace transform of $e^*(t)$ becomes

$$e^*(s) = \frac{1}{T_s} \sum_{k=-\infty}^{\infty} e(s + jk\frac{2\pi}{T_s}). \tag{2.4}$$

If an input signal contains frequency lower than $\frac{1}{2T_s}$ (the Nyquist frequency), it can be approximated from (2.4) that the transfer function of the ideal sampler is equivalent to a gain of $\frac{1}{T_s}$.

In contrast, the ZOH keeps an impulse for one sampling period with the amplitude equivalent to the area of the impulse, which is a pulse-to-continuous transfer function known as

$$G^*_{ZOH}(s) = \frac{1 - e^{-sT_s}}{s}. \tag{2.5}$$

Therefore, an ideal sampler cascaded by a ZOH with the same frequencies is represented by a continuous-to-continuous transfer function, whose Laplace-domain transfer function is written as

$$G_{ZOH}(s) = \frac{1 - e^{-sT_s}}{sT_s}. \tag{2.6}$$

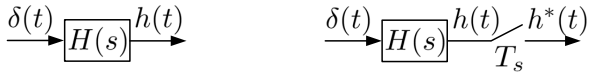
It is interesting to mention that, in the digital controller with a fixed frequency, a ZOH followed by an ideal sampler behaves as a unity gain. From the transfer function point of view, the pulse transfer function in z-domain describing the ZOH followed by the ideal sampler is derived as

$$\mathcal{Z}\{G^*_{ZOH}(s)\} = \frac{z}{z-1} - \frac{1}{z-1} = 1. \tag{2.7}$$

The principle of z-transform is illustrated in the following subsection.

2.2.2 z-Transform

In a continuous-time system, the impulse response is used to obtain the s-domain transfer function. The Laplace transform of the impulse response is the transfer function. In the discrete-time system, if a block is cascaded by a sampler, z-transform is used to describe the transfer function [27].



(a) (b)

Figure 2.2: Block diagrams of the transfer functions. (a) Continuous-time system. (b) Discrete-time system.

Fig. 2.2(a) and (b) show the block diagrams of the transfer function in a continuous-time system and in a discrete-time system, respectively. In Fig. 2.2(a), the impulse response of the block is $h(t)$, whose Laplace transform $H(s)$ represents the transfer function. However, as the block $H(s)$ in Fig. 2.2(b) is followed by a sampler, the transfer function describing output $h^*(t)$ as a function of input $\delta(t)$ is obtained by the Laplace transform of $h^*(t)$. If

$$H(s) = \int_{-\infty}^{\infty} h(t)e^{-st}dt, \tag{2.8}$$

$H^*(s)$ can be written as

$$\begin{aligned} H^*(s) &= \int_{-\infty}^{\infty} h^*(t)e^{-st}dt \\ &= \int_{-\infty}^{\infty} (\sum_{n=0}^{\infty} h(nT_s)\delta(t-nT_s))e^{-st}dt \\ &= \sum_{n=0}^{\infty} h(nT_s)(\int_{-\infty}^{\infty} \delta(t-nT_s)e^{-st}dt). \end{aligned} \tag{2.9}$$

Since $\int_{-\infty}^{\infty} \delta(t-nT_s)e^{-st}dt = e^{-snT_s}$, Equation (2.9) can be expressed as

$$H^*(s) = \sum_{n=0}^{\infty} h(nT_s)e^{-snT_s}. \tag{2.10}$$

Therefore, by letting $z = e^{sT_s}$, the transfer function $H^*(s)$ can be written as

$$H(z) = H^*(s)|_{e^{sT_s}=z} = \sum_{n=0}^{\infty} h(nT_s)z^{-n}. \tag{2.11}$$

Finally, the z-transform is defined as

$$H(z) = \mathcal{Z}\{H^*(s)\} \tag{2.12}$$

and the table of commonly used Laplace transform and z-transform pairs can be found in [27].

2.2.3 Discretization of controller

The digital controller comprised of difference equations can be represented by z-domain transfer functions. These transfer functions should achieve the required frequency response. As the conventional controllers designed in s-domain are well known, converting an s-domain controller into its z-domain equivalent is used. Since $z = e^{sT_s}$, the z-domain equivalent controller can be obtained by substituting $s = \frac{1}{T_s} \ln z$ into the s-domain controller. However, the rational expression in z-domain is more practical. Hence, Padé approximation is used to derive the z-domain controller, which is written as

$$s = \frac{2}{T_s} \frac{z-1}{z+1}. \tag{2.13}$$

For the transfer function of a controller $G(s)$ in continuous-time system, the digital controller in discrete-time system is derived as

$$G(z) = G(s)|_{s=\frac{2}{T_s}\frac{z-1}{z+1}}. \tag{2.14}$$

This transform method is named as bilinear transform which is most commonly used in digital controller design. There is another method which is called the impulse invariance. The method is to insert an ideal sampler after the s-domain controller $G(s)$, whose z-domain transfer function becomes $\mathcal{Z}\{G(s)\}$. Since an ideal sampler is introduced with an approximated gain of $\frac{1}{T_s}$, the equivalent transfer function of the controller in z-domain is

$$G(z) = T_s\mathcal{Z}\{G(s)\}. \tag{2.15}$$

Note that the impulse invariance method should be only used for digitalization when the z-transform of the s-domain controller exists. For a proportional controller in the s-domain, its digitalized transfer function in the z-domain should maintain the same format.

2.3 State of the art of modelling techniques for digitally controlled switching converters

2.3.1 Classic average model

Before digital controllers were widely used, most switching converters were implemented by using analog controllers. The input signal of the PWM is naturally-sampled by the carrier. Therefore, the controller behaves as a non-delay controller from signal sampling to duty-ratio updating. The gain of the PWM is modelled as unity. This strategy has been extended for a digitally controlled system, with quantization, sample and hold effects being neglected. The delay of the PWM generation is considered as a half or one switching cycle, but the computation in digital controller results in a half or one switching cycle delay [28, 29, 30]. Although the digital controller is implemented in z-domain, it is transformed from the s-domain controller during the design procedure. Therefore, the s-domain transfer function of the controller is used for analysis. As the switch voltage is represented by the voltage averaged in the switching period, the model is named as average model. By using the s-domain transfer functions of power circuit and controller circuit, the average model for the entire control loop can be obtained.

2.3.2 Small-signal s-domain model

Small-signal s-domain model is developed with the PWM well modelled. This is a more accurate model compared to the classic average model as the sample and hold effect and PWM delay effect are considered. For analog controlled switching converters, the PWM does not bring any delay in the control loop. For uniformly-sampled switching converters, the PWM delay depends on the shape of the carriers [31]. When triangle carriers are used, the PWM delay can also be approximated by a half switching period [32]. The quantization effect has been neglected since it brings nonlinearity which is difficult to model. However, the sample and hold effect has been taken into consideration. The approximated transfer function of the sampler is written as $\frac{1}{T_s}$ as explained in the previous section. The transfer function of the ZOH is $\frac{1-e^{-sT_s}}{s}$. As a result, the sample and hold effect is represented by a block with the transfer function of

$$G_{ZOH}(s) = \frac{1 - e^{-sT_s}}{sT_s}. \tag{2.16}$$

The ZOH block is usually placed in the control loop preceded by the digital controller block which is represented in s-domain [33]. The digital controller is modelled in the same way as that in the classic average model. The advantage of the small-signal s-domain model compared to the average model is that PWM

delay and sample and hold effect are included. However, Due to the accuracy of the s-domain represented sampler and digital controller is only guaranteed in low frequency range, this model may fail to predict the system dynamic close to half of the sampling frequency.

2.3.3 Classic z-domain model

As the s-domain models are not capable of predicting fast-scale instabilities, discrete models are required as a solution. The discrete-time maps can be used to predict instabilities such as bifurcation and chaos [16, 34]. Although these maps can be used to find the gain boundaries, they are not convenient for controller design due to the weak link between the maps and the frequency response characteristics. Therefore, some papers propose the z-domain model for digitally controlled switching converters, but the sample and hold effect is treated as a unity gain [35, 36, 37]. The delay effect is estimated using the same method as that in the classic average model. The continuous transfer functions describing the output filter are transformed into the z-domain by using the impulse invariance method [38]. The transfer functions of the controllers retain their z-domain expressions. This modeling method neglects the type of PWM used. It works fine when simple filters and controllers are used, but the accuracy is not very good when the modulation strategy changes or the system's order increases.

2.3.4 Small-signal z-domain model

Small-signal z-domain model is proposed for synchronously-sampled PWM. This enables more accurate modelling for different types of PWMs, as the delay effects of DSP and PWM are carefully considered. This method is based on the technique that sampling is triggered by the PWM carrier, also called uniform-sampling. As the uniformly-sampled digital PWM contains high nonlinearity, the Laplace transform is not applicable to exact modelling in large signal. However, the exact small-signal PWM models depending on the average duty-ratio D have been proposed. By combining the ZOH and PWM together, the pulse-to-continuous transfer functions of the PWM models are obtained. The continuous-to-continuous and pulse-to-continuous transfer functions of the PWM models are shown in Table 2.1 [25].

The transfer functions of the filter followed by a sampler is transformed into the z-domain. The controllers are designed and expressed in the z-domain. This modelling method provides a good way of evaluating a digital controller for single switched converters, but some limitations exist:

1. The delay effect is dependent of the carrier and the duty-ratio update mode.

Table 2.1: Transfer functions of the PWM model

Carrier	$G_{PWM}(s)$	$G^*_{PWM}(s)$
End-of-on-time	e^{-sDT_s}	$T_s e^{-sDT_s}$
Begin-of-on-time	$e^{-s(1-D)T_s}$	$T_s e^{-s(1-D)T_s}$
Symmetric-off-time	$\frac{1}{2}(e^{-s\frac{DT_s}{2}} + e^{-s\frac{(2-D)T_s}{2}})$	$\frac{T_s}{2}(e^{-s\frac{DT_s}{2}} + e^{-s\frac{(2-D)T_s}{2}})$
Symmetric-on-time	$\frac{1}{2}(e^{-s\frac{(1-D)T_s}{2}} + e^{-s\frac{(1+D)T_s}{2}})$	$\frac{T_s}{2}(e^{-s\frac{(1-D)T_s}{2}} + e^{-s\frac{(1+D)T_s}{2}})$

However, the previous model only discusses the delay when different carriers are used.

2. The uniformly-sampled PWM model is proposed for single switched converter. For converters with more switches and different modulation techniques, extending the model is needed.

3. The example of the z-transform for the converter with single loop controller and first-order filter is provided in that model. However, most converters have a filter with higher order and/or cascaded control loops.

In order to apply the small-signal z-domain model to digitally controlled switching converters, more work has to be done to overcome the limitations mentioned above. This thesis provides a general way of detailed modelling of digitally controlled power inverters in the z-domain. Based on the proposed models, the controllers design can be implemented and tested by simulation and experimental work.

2.4 State of the art of digital control techniques for power inverters

2.4.1 Classic controllers

The classic controllers are derived from conventional analog controllers. They are represented in the s-domain and transformed into the z-domain for digital controllers. The most commonly used controller for dc-dc converters is the proportional plus integral (PI) controller. This control scheme has also been used for dc-ac inverters [39, 40]. A typical PI controller can be expressed in the s-domain as

$$G_{PI}(s) = k_p + \frac{k_i}{s} \tag{2.17}$$

with k_p the proportional gain and k_i the integral gain. As the integral compensator achieves high gain in the low frequency range and low gain in the high

frequency range, the proportional coefficient of the integrator can be quite high without causing instabilities. However, the gain of the integrator at the fundamental frequency will be insufficient in some applications with high line frequency such as in 400 Hz power systems. In that environment, the duty-ratio feedforward strategy is required to improve the control performance [28].

In the synchronous reference frame, it is confirmed that the PI controller is equivalent to the proportional plus resonant (PR) controller in the stationary reference frame [41]. The typical proportional plus resonant controller in the s-domain is given by

$$G_{PR}(s) = k_p + k_r \frac{s}{s^2 + \omega_1^2} \tag{2.18}$$

with k_r the resonant gain and ω_1 the fundamental angular frequency. The controller achieves infinite gain at the fundamental frequency, and the tracking performance at the fundamental frequency is theoretically very good. However, this controller cannot be physically implemented in analog circuits. Hence, a more practical solution becomes

$$G_{PR}(s) = k_p + k_r \frac{2\xi\omega_1 s}{s^2 + 2\xi\omega_1 s + \omega_1^2} \tag{2.19}$$

with ξ the damping factor. The gain of (2.19) is with an amplitude of k_r at the fundamental frequency. By changing the value of k_r, the gain with the required value can be achieved. Moreover, for analog control circuits, (2.19) can be easily implemented by second-order filters. For a digital controller, the relevant z-domain expression can be obtained from (2.19) by using bilinear transform. The PR controller has good tracking capability only at the fundamental frequency, but does not provide compensation for harmonic frequencies components. As a result, more complicated control methods are proposed for harmonic components compensation.

2.4.2 Repetitive-based controllers

Repetitive-based controllers are proposed for precise tracking at selected frequencies [42, 43]. To implement a controller it requires the sampling rate to be an integer multiple of the fundamental frequency, which can be written as

$$G_{Rep}(s) = \frac{1}{1 - z^N}. \tag{2.20}$$

The tracking performance for fixed periodical signals is very good, but additional filters have to be used to suppress the gain in the high frequency range [44]. Otherwise, it may lead to instability problems because of the high gain at high-order harmonic frequencies. When an additional filter is used, the gain of the

compensator is infinite at the selected harmonic frequencies. As long as the filter is well designed, the compensator has low gain in high frequency range without causing instabilities.

2.4.3 Deadbeat controllers

The deadbeat controllers are based on the discrete model of a control object. It aims for an output signal following the reference signal [45, 46]. For Nth-order linear system, the minimum delay may be written as NT_s, with T_s the sampling period. The closed-loop transfer function of the deadbeat controlled system is

$$G_{DB}(z) = z^{-N}. \tag{2.21}$$

By solving (2.21) with the known transfer function of the plant, the transfer function of the deadbeat controller can be obtained. However, most deadbeat controllers have delay of more than two sampling cycles. To compensate for the delay introduced by computation and the deadbeat controller, [47] proposed a solution with feedforward action. As a result, a fast controller is obtained with the delay eliminated.

2.4.4 Linear controllers

Linear current controllers have been proposed for selective harmonic compensations [30, 48]. These control strategies are based on a cluster of bandpass filters in PR controller. By turning the bandpass filters resonating at odd harmonic frequencies, the suppression of harmonic components is very effective. The general expression of linear controllers can be written as [6]

$$G_L(s) = k_p + \sum_{h=1,\text{odd}}^{h_{max}} k_h \frac{2\xi\omega_h s}{s^2 + 2\xi\omega_h s + \omega_h^2} \tag{2.22}$$

with k_p the proportional gain, h_{max} the highest order of the compensator, k_h the gain at the specific frequency, ξ the damping factor and ω_h the hth harmonic frequency. At each harmonic frequency, the gain magnitude is equal to k_h. Therefore, by carefully choosing the coefficients of the harmonic compensators, a good tradeoff between stability and control performance can be achieved.

As linear control schemes exhibit flexibility in choosing gains at selected frequencies, this thesis uses linear control schemes as the main control method. Moreover, to reduce the difference between control reference and target, duty-ratio feedforward is involved. The design of the controller and selection of control parameters are implemented based on the proposed exact discrete model in z-domain. The following chapters will provide examples on implementing the modelling and control of digitally controlled power inverters.

Chapter 3

Digitally Controlled Switching Converters with Synchronously Sampled Pause-Width-Modulators

3.1 Introduction

For most power inverters in renewable energy systems, the entire controller of each module is always implemented digitally. In classical digital control methods, synchronized sampling and switching is a good solution to avoid the sampling disturbance in the vicinity of the switching instant [49, 50]. The PWM updates the calculated duty-ratio into the compare register in each switching period. The duty-ratio is compared to the digital carrier to generate drive signals. Hence, the PWM is actually equivalent to a sampling process on itself. For this reason, the switching frequency and sampling frequency are always chosen to be the same, known as the technique of uniform-sampling [25].

A digitally controlled inverter usually has an internal control loop with converter current feedback. To guarantee stable operation, the maximum proportional gain in the internal loop is limited by the sampling frequency and the converter side inductance. Therefore, a precise model is required to determine the feedback gains of the digital controller. Moveover, the model is also used for controller design. The control performance can be evaluated based on the model of the entire closed-loop control system. The time-domain and frequency-domain analysis can be performed. The model is capable of predicting waveforms in either steady-state or transient response.

In this chapter, the procedure of modelling and controller design is given. The delay effect of uniformly-sampled PWMs is discussed. The delay effect is dependent of the carrier waveshape and duty-ratio update mode. Furthermore,

the PWM model is extended for bipolar and unipolar switched H bridges. Based on the PWM model, general block diagrams for single digital control loop and cascaded digital control loops are presented in both s-domain and z-domain. The design of digital controllers can be implemented based on the block diagrams. Examples of classic design methods using simulation, root locus and frequency response tools are applied, which indicate the feasibility of the proposed model. Finally, the simulation and experimental setup work throughout the thesis is described.

3.2 Small-signal modelling of uniformly-sampled digital PWMs with delay effects

The conventional PWM model assumes the sampled input is synchronized to the peaks of the carriers and combines all delay effects in the controller as a total DSP delay [25]. However, this is not always accurate when different duty-ratio update modes are used. In a practical digital controller, different types of delay exist and the delay effects should be discussed according to the duty-ratio update techniques. In order to obtain exact models of the digital PWMs containing DSP delay, two duty-ratio update modes are studied.

3.2.1 Digital PWM models in shadow mode

When a new duty-ratio is calculated, it is required to update this new value into the PWM compare register. The time for update can be set in many different ways. The most commonly used method is to load the duty-ratio into PWM compare register at the instants which is synchronized to the carrier peaks. This update mode is defined as the shadow mode. If the duty-ratio is updated in shadow mode, the time-domain waveforms of the sawtooth PWM [25] are shown in Fig. 3.1.

The ideally sampled quantity and calculated duty-ratio are represented by q^* and x^* in Fig. 3.1, respectively. In practice, the digital duty-ratio calculated with time delay is d^*. The delay from x^* to d^* is required by the ADC conversion time and duty-ratio computation time, represented by τ_{d1} and τ_{d2}, respectively. This delay must be smaller than one sampling period, otherwise it will lead to an erroneous disorder in the controller. When the calculated duty-ratio d^* is ready, it can be updated into the PWM controller as u^*. The delay from signals sampling to duty-ratio updating is defined as the DSP delay in this thesis. When using sawtooth carriers in shadow mode, the duty-ratio is updated at each sampling instant. Therefore, the DSP delay is equal to one switching period.

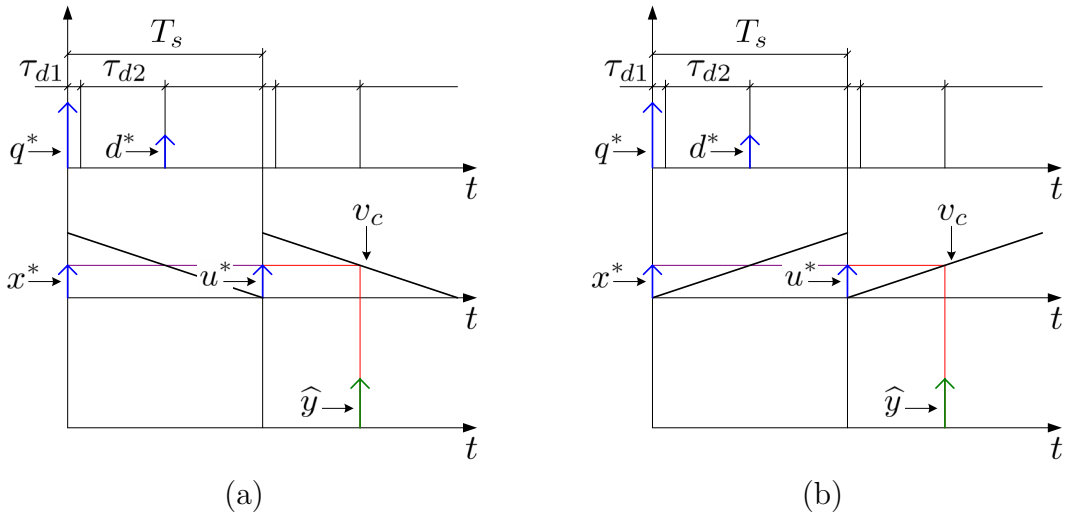


Figure 3.1: Key waveforms of the sawtooth PWM in shadow mode. (a) Begin-of-on-time modulator. (b) End-of-on-time modulator.

On the other hand, the small-signal PWM delays from updated duty-ratio u^* to switching output y can be found in Table 2.1. For the begin-of-on-time modulator and the end-of-on-time modulator, the PWM delays are $(1-D)T_s$ and DT_s, respectively. Therefore, the transfer functions describing the small-signal switching output $\widehat{y}$ as a function of the small-signal ideal duty-ratio $\widehat{x}^*$ for the begin-of-on-time modulator and the end-of-on-time modulator are [25]

$$G^*_{PWM}(s) = T_s e^{-s(2-D)T_s} \tag{3.1}$$

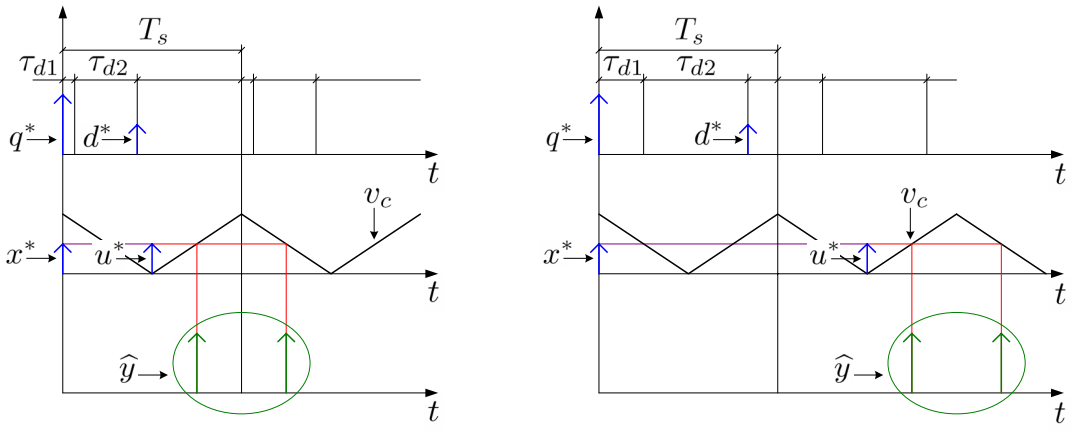
and

$$G^*_{PWM}(s) = T_s e^{-s(1+D)T_s}, \tag{3.2}$$

respectively.

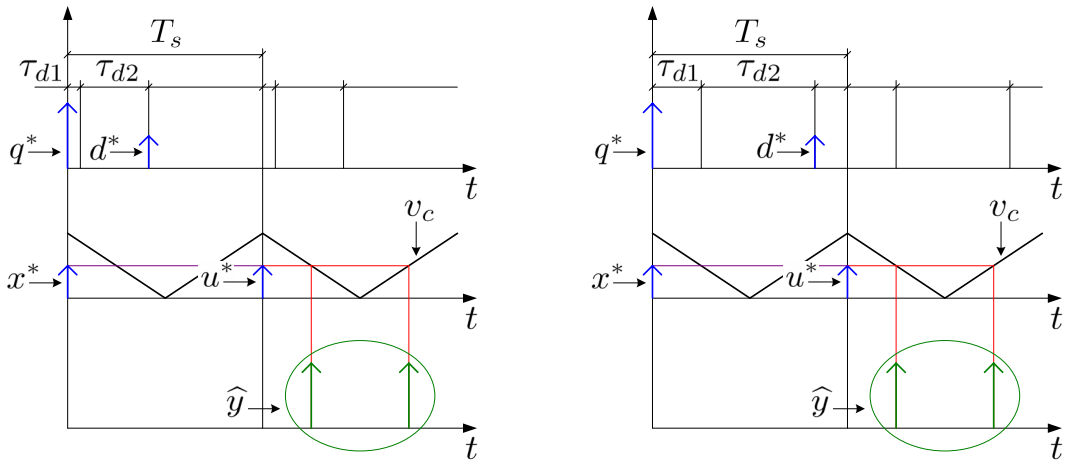
When the triangle PWMs are used in shadow mode, the delay effects are more complicated. The small-signal transfer functions from $\widehat{x}^*$ to $\widehat{y}$ are derived for the symmetric-on-time modulator, which can be also extended to the symmetric-off-time modulator.

For the symmetric-on-time modulator, the sampling is started at the time when the PWM counter reaches its period value. The duty-ratio can be updated into the PWM compare register when the PWM counter reaches its zero value, period value, or both. The time-domain key waveforms of the symmetric-on-time PWM in shadow mode when the duty-ratio is updated at the counter's zero value and updated at the counter's period value are shown in Fig. 3.2 and Fig. 3.3, respectively. In Fig. 3.2(a), if the processor is fast and the duty-ratio d^* is calculated before the counter reaches zero value, the DSP delay from x^* to u^* is half switching period. However, if the processor is slow and the duty-ratio d^* is



(a) (b)

Figure 3.2: Key waveforms of the symmetric-on-time PWM in shadow mode with duty-ratio updated when counter reaches zero value. (a) $\tau_{d1} + \tau_{d2} < \frac{T_s}{2}$. (b) $\frac{T_s}{2} < \tau_{d1} + \tau_{d2} < T_s$.



(a) (b)

Figure 3.3: Key waveforms of the symmetric-on-time PWM in shadow mode with duty-ratio updated when counter reaches period value. (a) $\tau_{d1} + \tau_{d2} < \frac{T_s}{2}$. (b) $\frac{T_s}{2} < \tau_{d1} + \tau_{d2} < T_s$.

calculated after the counter reaches zero value, the DSP delay becomes one and a half switching periods, as is shown in Fig. 3.2(b). In this case, the maximum DSP delay results in a poor dynamic performance. The small-signal transfer functions describing $\widehat{y}$ as a function of $\widehat{x}^*$ for modulators in Fig. 3.2(a) and Fig. 3.2(b) are [25]

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}} + e^{-s\frac{(3-D)T_s}{2}}) \tag{3.3}$$

and

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3+D)T_s}{2}} + e^{-s\frac{(5-D)T_s}{2}}), \tag{3.4}$$

respectively.

When the duty-ratio is updated at the counter's period value, as is shown in Fig. 3.3, the DSP delay does not depend on the speed of processor but remains as one switching period. Therefore, it can be derived from Fig. 3.3(a) and Fig. 3.3(b) that the small-signal transfer function describing $\widehat{y}$ as a function of $\widehat{x}^*$ is [25]

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}}). \tag{3.5}$$

This update method is widely used in digital controller design since the DSP delay effect is fixed as one switching period.

When the duty-ratio is double-updated in shadow mode, i.e., on both the counter's zero and period value, the time-domain key waveforms of the symmetric-on-time PWM are shown in Fig. 3.4. If the processor is fast and the duty-ratio d^* is calculated before the counter reaches zero value, the DSP delay from x^* to u^* is half a switching period. If the processor is slow and the duty-ratio d^* is calculated after the counter reaches the period value, the DSP delay becomes one switching period. Hence, the minimum DSP delay in shadow mode is achieved under all circumstance. The small-signal transfer functions describing $\widehat{y}$ as a function of $\widehat{x}^*$ for modulators in Fig. 3.4(a) and Fig. 3.4(b) are [25]

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}} + e^{-s\frac{(3-D)T_s}{2}}) \tag{3.6}$$

and

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}}), \tag{3.7}$$

respectively.

3.2.2 Digital PWM models in immediate mode

When a new duty-ratio is calculated, the value can be immediately loaded into the PWM compare register. If the duty-ratio is updated into the PWM compare register immediately after it is calculated, the update mode is defined as the

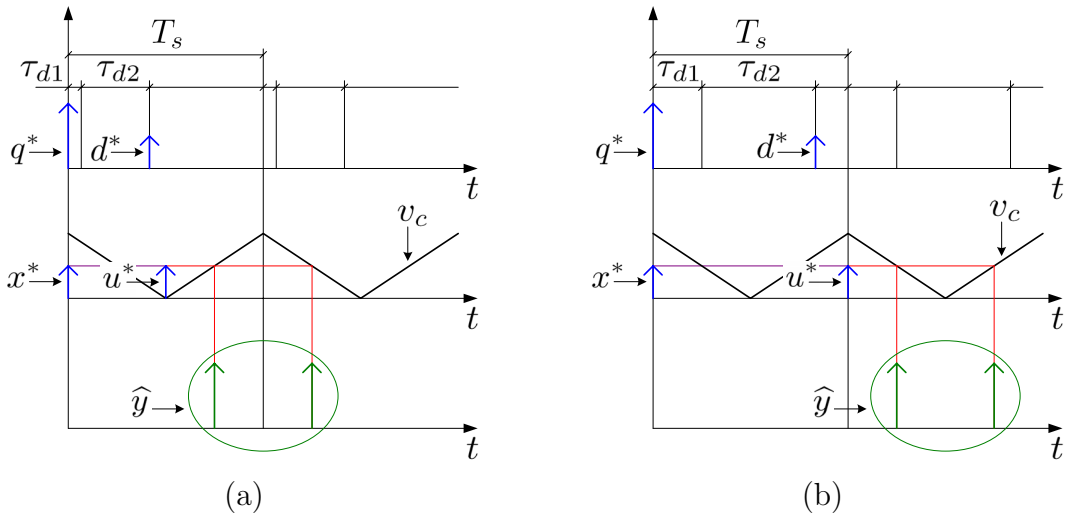


Figure 3.4: Key waveforms of the symmetric-on-time PWM in shadow mode with double update. (a) $\tau_{d1} + \tau_{d2} < \frac{T_s}{2}$. (b) $\frac{T_s}{2} < \tau_{d1} + \tau_{d2} < T_s$.

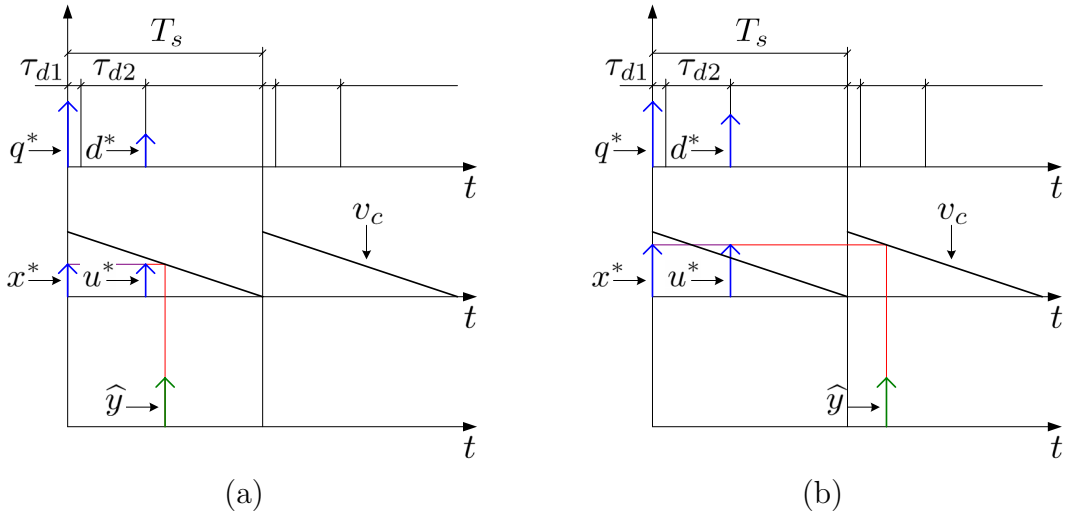


Figure 3.5: Key waveforms of the begin-of-on-time PWM in immediate mode. (a) $\tau_{d1} + \tau_{d2} < (1 - D)T_s$. (b) $(1 - D)T_s < \tau_{d1} + \tau_{d2} < T_s$.

immediate mode. The time-domain waveforms of the begin-of-on-time PWM in immediate mode are shown in Fig. 3.5.

In immediate mode the delay is strongly dependent on the average duty-ratio D. For the begin-of-on-time PWM, if $\tau_{d1}+\tau_{d2} < (1-D)T_s$, the transfer function describing the small-signal switching output $\widehat{y}$ as a function of the small-signal ideal duty-ratio $\widehat{x}^*$ is written as [25]

$$G^*_{PWM}(s) = T_s e^{-s(1-D)T_s}. \tag{3.8}$$

On the other hand, if $(1-D)T_s < \tau_{d1}+\tau_{d2} < T_s$, the transfer function becomes [25]

$$G^*_{PWM}(s) = T_s e^{-s(2-D)T_s}. \tag{3.9}$$

Similarly, the time-domain waveforms of the end-of-on-time PWM in immediate mode are shown in Fig. 3.6. For the conditions of $\tau_{d1}+\tau_{d2} < DT_s$ and $DT_s < \tau_{d1}+\tau_{d2} < T_s$ (see Fig. 3.6 (a) and (b)), the small-signal transfer functions from $\widehat{x}^*$ to $\widehat{y}$ are [25]

$$G^*_{PWM}(s) = T_s e^{-sDT_s} \tag{3.10}$$

and

$$G^*_{PWM}(s) = T_s e^{-s(1+D)T_s}, \tag{3.11}$$

respectively.

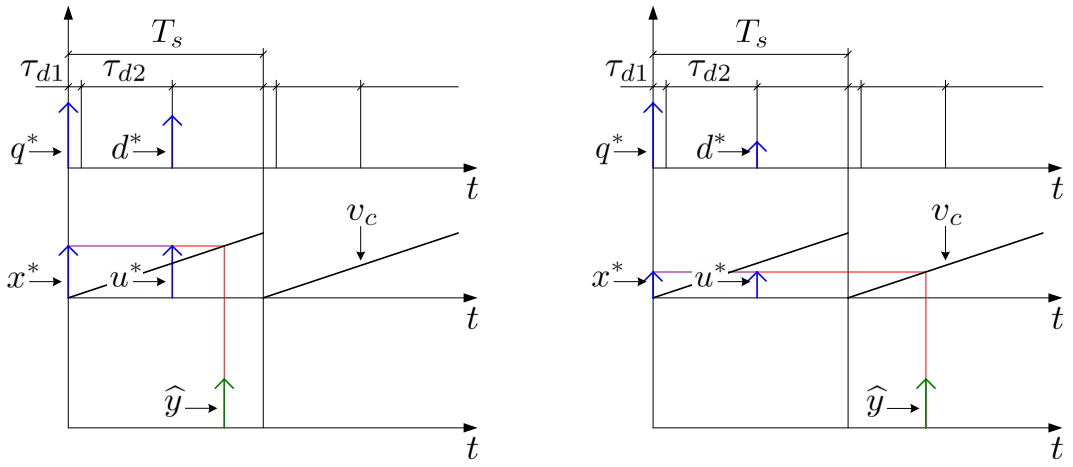


Figure 3.6: Key waveforms of the end-of-on-time PWM in immediate mode. (a) $\tau_{d1}+\tau_{d2} < DT_s$. (b) $DT_s < \tau_{d1}+\tau_{d2} < T_s$.

More complicated delay effects exist when using triangle PWMs in immediate mode. The small-signal transfer functions from $\widehat{x}^*$ to $\widehat{y}$ are derived for the immediate mode symmetric-on-time modulator. However, the results can be extended to the symmetric-off-time modulator. If the processor is fast and the duty-ratio

d^* is calculated within a half switching period, the time-domain key waveforms of the symmetric-on-time modulator in immediate mode are shown in Fig. 3.7. The small-signal transfer functions from $\widehat{x}^*$ to $\widehat{y}$ are [25]

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1-D)T_s}{2}} + e^{-s\frac{(1+D)T_s}{2}}) \tag{3.12}$$

when $\tau_{d1} + \tau_{d2} < \frac{(1-D)T_s}{2}$ (see Fig. 3.7(a)) and

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}} + e^{-s\frac{(3-D)T_s}{2}}) \tag{3.13}$$

when $\frac{(1-D)T_s}{2} < \tau_{d1} + \tau_{d2} < \frac{T_s}{2}$ (see Fig. 3.7(b)).

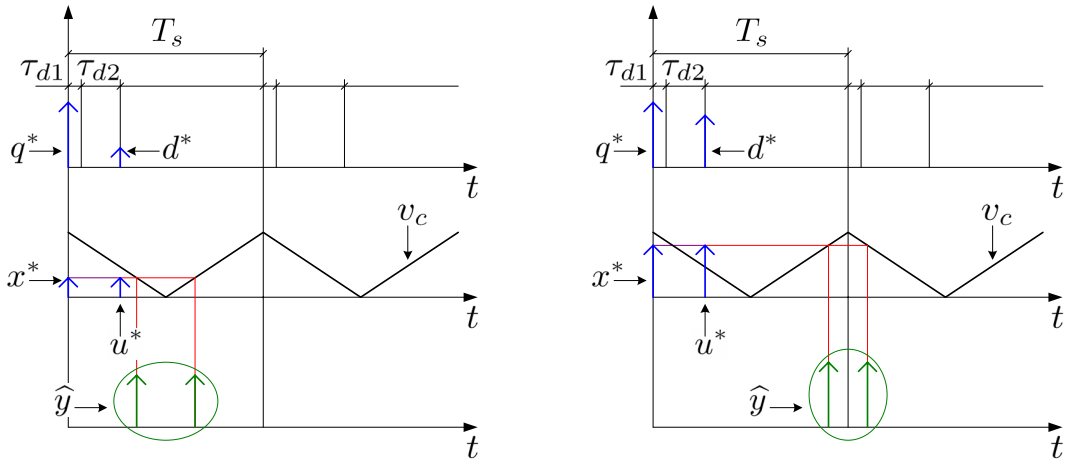


Figure 3.7: Key waveforms of the symmetric-on-time PWM in immediate mode with a fast processor. (a) $\tau_{d1} + \tau_{d2} < \frac{(1-D)T_s}{2}$. (b) $\frac{(1-D)T_s}{2} < \tau_{d1} + \tau_{d2} < \frac{T_s}{2}$.

On the other hand, if the processor is slow and the duty-ratio d^* is calculated during the rising slope of the triangle carrier, the time-domain key waveforms of the symmetric-on-time modulator in immediate mode are shown in Fig. 3.8. The small-signal transfer functions from $\widehat{x}^*$ to $\widehat{y}$ are [25]

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}} + e^{-s\frac{(3-D)T_s}{2}}) \tag{3.14}$$

when $\frac{T_s}{2} < \tau_{d1} + \tau_{d2} < \frac{(1+D)T_s}{2}$ (see Fig. 3.8(a)) and

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}}) \tag{3.15}$$

when $\frac{(1+D)T_s}{2} < \tau_{d1} + \tau_{d2} < T_s$ (see Fig. 3.8(b)).

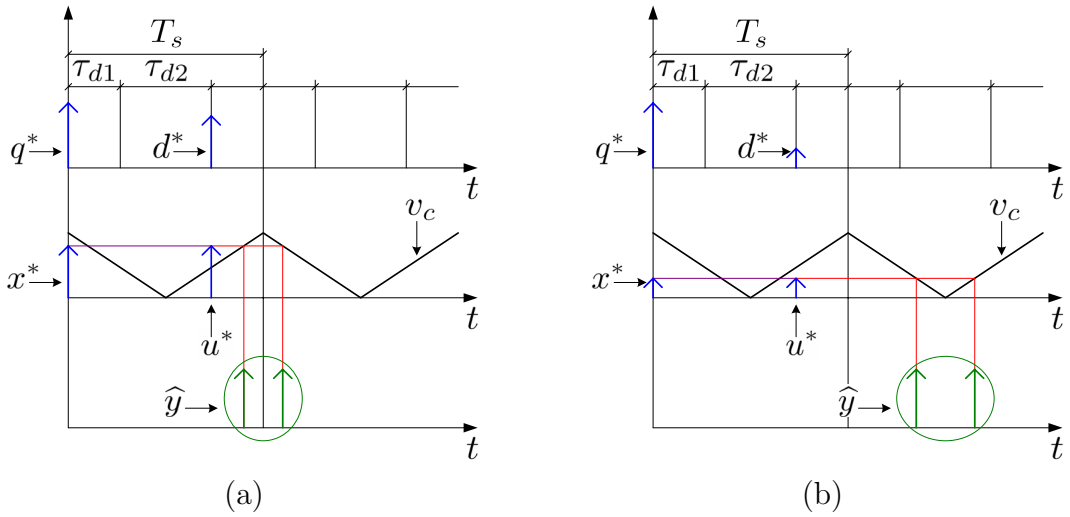


Figure 3.8: Key waveforms of the symmetric-on-time PWM in immediate mode with a slow processor. (a) $\frac{T_s}{2} < \tau_{d1} + \tau_{d2} < \frac{(1+D)T_s}{2}$. (b) $\frac{(1+D)T_s}{2} < \tau_{d1} + \tau_{d2} < T_s$.

3.3 Modelling H bridges with synchronously sampled PWMs

The digital PWM models in the previous sections are derived for the output voltage of single switch. As power inverters are usually implemented by using H bridges, describing the output voltage of H bridges as a function of the modulation signal is required. The transfer function of PWM model varies when different carriers and modulation techniques are used.

The typical circuit diagram of an H bridge is shown in Fig. 3.9. The output of the H bridge is the filter input voltage v_{in}. The switching output is defined as $y = v_{in}/V_{dc}$. The switching output varies significantly when different modulation strategies are used. In this section we only provide examples with end-of-on-time carriers and symmetric-on-time carriers. Both bipolar switched and unipolar switched PWMs are studied.

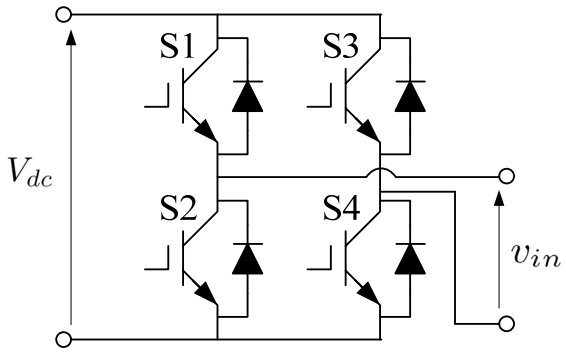


Figure 3.9: A typical H bridge circuit.

3.3.1 Bipolar switched H bridges

If there are two voltage levels produced on the switch voltage v_{in}, i.e., V_{dc} and $-V_{dc}$, the H bridge is bipolar switched. In order to provide the model for a single-update-mode bipolar switched H bridge, we assume that the duty-ratio is updated at each sampling instant. Therefore, the DSP delay is one sampling cycle. When the sampling frequency is equal to the switching frequency, the key waveforms of bipolar switched H bridge are shown in Fig. 3.10.

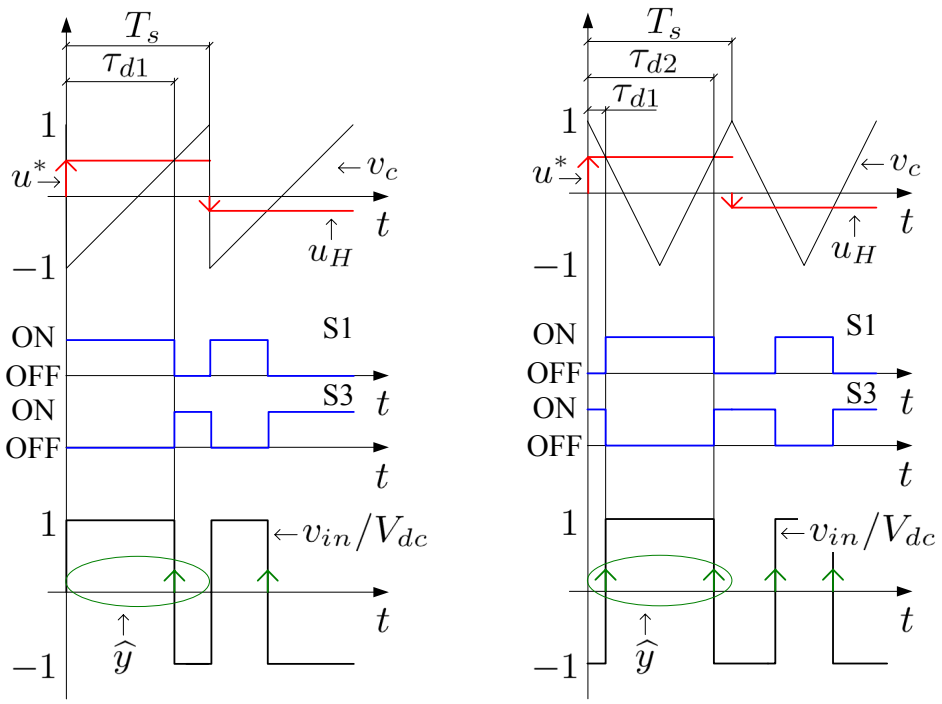


Figure 3.10: Key waveforms of single-update-mode uniformly-sampled bipolar switched H bridge. (a) End-of-on-time modulator. (b) Symmetric-on-time modulator.

It can be seen from Fig. 3.10 that the filter input voltage frequency of the bipolar switched H bridge is equivalent to the switching frequency. The duty-ratio can be updated only once when using sawtooth carriers. However, for triangle carriers, the duty-ratio can be updated twice a switching cycle. As the DSP delay from x^* to u^* is T_s, the small-signal transfer function describing $\widehat{y}$ as a function of $\widehat{x}^*$ for end-of-on-time modulator is written as [25]

$$G^*_{PWM}(s) = T_s e^{-s(1+D)T_s}. \tag{3.16}$$

On the other hand, for symmetric-on-time modulator, the small-signal transfer

function $G^*_{PWM}(s)$ can be expressed as [25]

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}}). \tag{3.17}$$

For double-update-mode PWM where the sampling frequency and updating rate is as twice as the switching frequency, the triangle carriers are usually used. To provide the double-update-mode PWM model, the symmetric-on-time modulator is used as the example. The key waveforms of double-update-mode bipolar switched H bridge are shown in Fig. 3.11.

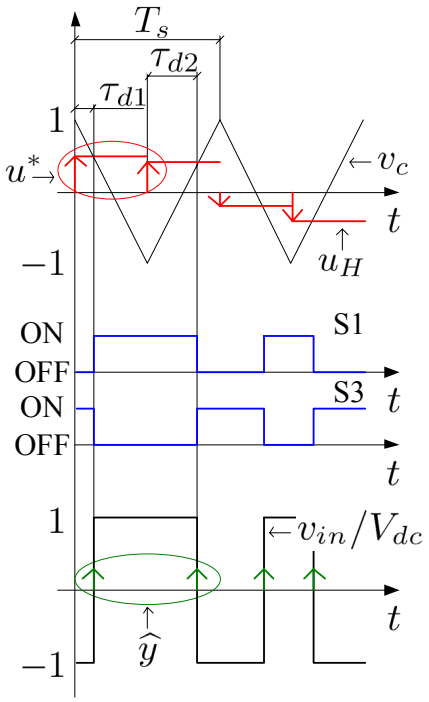


Figure 3.11: Key waveforms of double-update-mode uniformly-sampled bipolar switched H bridge.

For bipolar switched H bridges, each switching cycle contains two updated samples with two relevant switching actions. If the sample is updated at the upper peak of the carrier, the delay from u^* to $\widehat{y}$ is $\frac{(1-D)T_s}{2}$. On the other hand, if the sample is updated at the lower peak of the carrier, the delay from u^* to $\widehat{y}$ becomes $\frac{DT_s}{2}$. During each switching cycle, the possibilities of the two situations are equal. As the exact analytical expression of the double-update-mode PWM model is not easy to obtain, the approximation can be applied by averaging the two delay effects. With half switching cycle DSP delay from x^* to u^*, the double-update-mode PWM model of the bipolar switched H bridge is given by [25]

$$G^*_{PWM}(s) = \frac{T_s}{4}(e^{-s\frac{(2-D)T_s}{2}} + e^{-s\frac{(1+D)T_s}{2}}). \tag{3.18}$$

3.3.2 Unipolar switched H bridges

If there are three voltage levels produced on the switch voltage v_{in}, i.e., V_{dc}, 0 and $-V_{dc}$, the H bridge is unipolar switched. When the H bridge is unipolar switched, the key waveforms with single-update are shown in Fig. 3.12. For end-of-on-time modulator, the duty-ratio can be updated twice a switching cycle. The filter input voltage frequency of the unipolar switched H bridge is equivalent to the switching frequency. However, for symmetric-on-time modulator, the duty-ratio can be updated quadruply a switching cycle since the filter input voltage frequency is as twice as the switching frequency. Hence, the modulation method of using unipolar switched H bridge inverter with symmetric triangle carriers is a good way to reduce the electromagnetic interference.

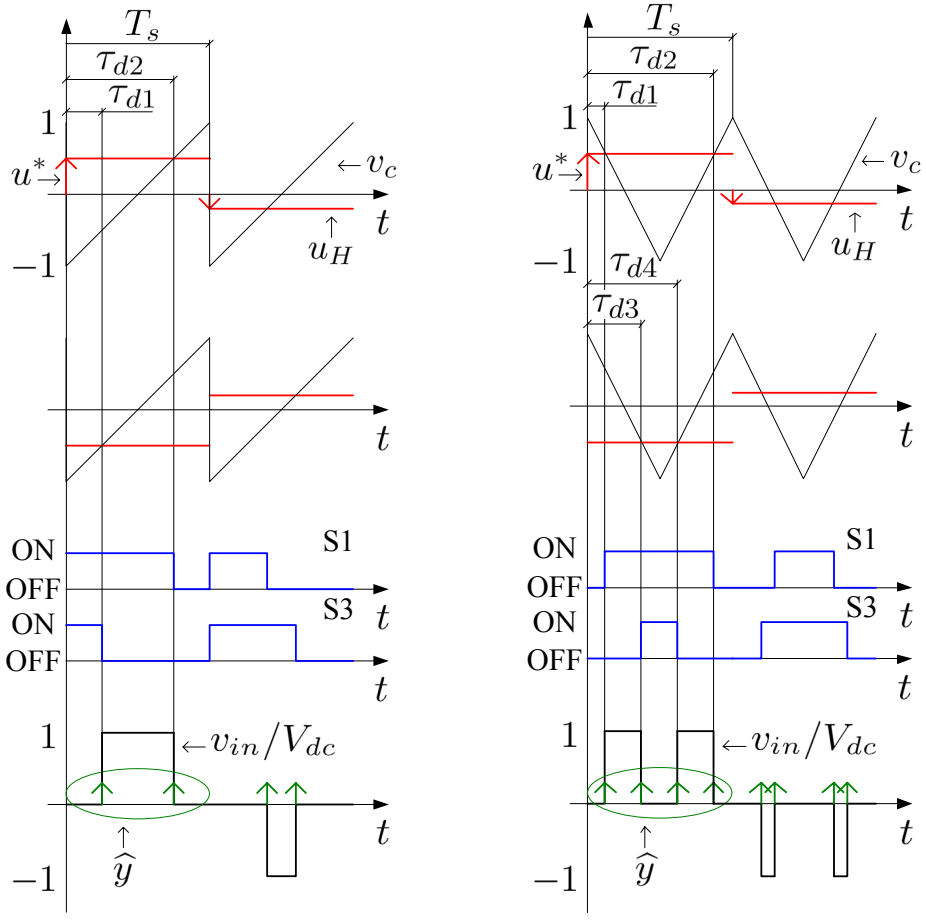


Figure 3.12: Key waveforms of uniformly-sampled single-update-mode unipolar switched H bridge. (a) End-of-on-time modulator. (b) Symmetric-on-time modulator.

Similarly, the small-signal transfer function describing $\widehat{y}$ as a function of $\widehat{x}^*$ for single-update-mode unipolar switched H bridge with end-of-on-time modulator is

written as [25]

$$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s(1+D)T_s} + e^{-s(2-D)T_s}). \tag{3.19}$$

For single-update-mode unipolar switched H bridge with symmetric-on-time modulator, the transfer function is given by [25]

$$G^*_{PWM}(s) = \frac{T_s}{4}(e^{-s\frac{(2+D)T_s}{2}} + e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}} + e^{-s\frac{(4-D)T_s}{2}}). \tag{3.20}$$

The key waveforms of double-update-mode unipolar switched H bridge is shown in Fig. 3.13.

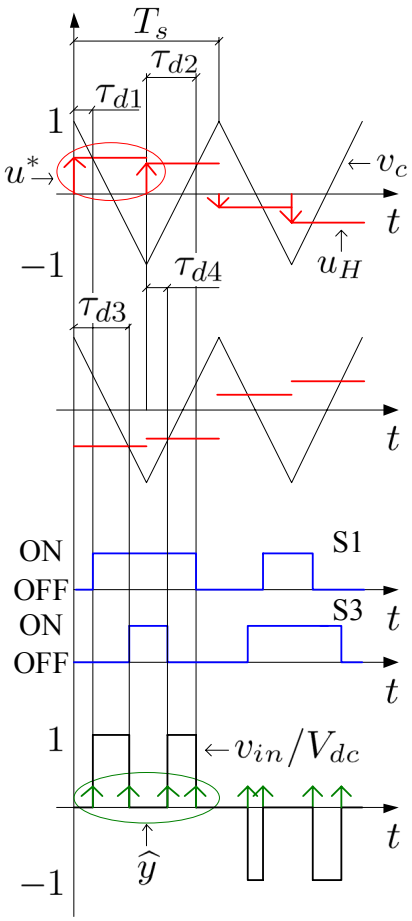


Figure 3.13: Key waveforms of uniformly-sampled unipolar switched H bridge with double-update-mode.

For unipolar switched H bridges containing two updated samples in each switching cycle, four relevant switching transients are generated (see Fig. 3.13). Two situation are discussed to obtain the PWM model. If the sample is updated at the upper peak of the carrier, the delay terms from u^* to $\widehat{y}$ are represented by $\tau_{d1} = \frac{DT_s}{2}$ and $\tau_{d3} = \frac{(1-D)T_s}{2}$. On the other hand, if the sample is updated at the lower peak of the carrier, the delay terms becomes $\tau_{d2} = \frac{(1-D)T_s}{2}$ and $\tau_{d4} = \frac{DT_s}{2}$.

Therefore, no matter whether the sampling starts at the upper peak or lower peak of the carrier, the delay effect does not change. As a result, the small-signal double-update-mode PWM model for the unipolar switched H bridge is [25]

$$G^*_{PWM}(s) = \frac{T_s}{4}(e^{-s\frac{(2-D)T_s}{2}} + e^{-s\frac{(1+D)T_s}{2}}). \tag{3.21}$$

Comparing double-update-mode PWMs to the uniformly-sampled PWMs, it can be seen that the double-update-mode PWMs result in a minimum delay time. Hence, the double-update-mode is usually the recommended PWM strategy. In practice, more sampling methods rather than uniform-sampling may be used, such as asynchronous sampling, multisampling and hybrid sampling. In those cases, the small-signal PWM model should be modified to accommodate the sampling methods. However, the strategy of developing the transfer functions in this section can be used in other cases.

3.4 Block diagrams of digitally controlled switching converters

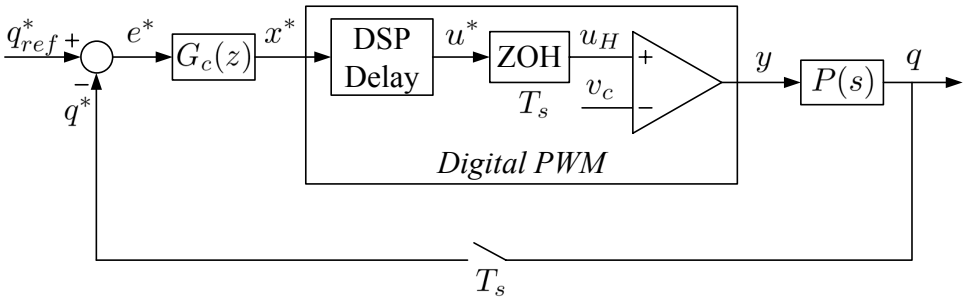
3.4.1 Block diagram of a single control loop in s-domain

Based on the previous results, the block diagram of a switching converter with a single loop digital controller can be schematically represented in Fig. 3.14 (a), where the block of a switch with sampling period T_s represents the ideal sampler and $G_c(z)$ represents the digital compensator. The meanings of the variables in Fig. 3.14 (a) are the same as those in Fig. 3.8 and Fig. 3.10. The output of this block diagram is the measurable quantity q (usually representing the output voltage or current). Fig. 3.14 (a) can be rearranged as is shown in Fig. 3.14 (b), with the switching output y defined as the output of the block diagram. This arrangement is convenient for obtaining the block diagrams of the cascaded control loops in the following subsections. The switching converter output q as a function of the switching output y is described by the block transfer function $P(s)$.

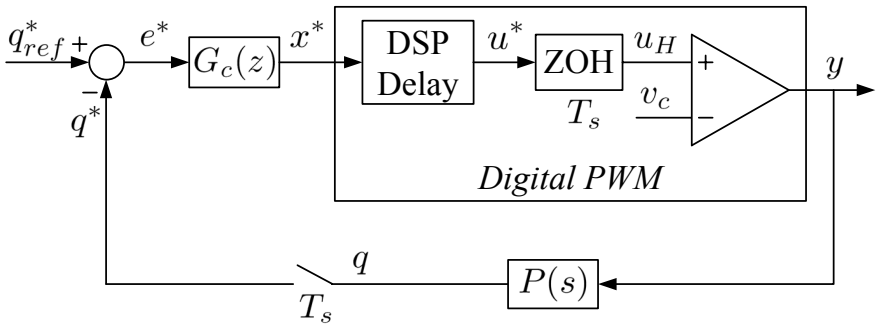
In order to analyze the frequency response, the s-domain model in large signal is required. Instead of using the sampled reference q^*_{ref}, q_{ref} is used as the analog reference input. The compensator $G_c(z)$ should be converted into s-domain by using $z = e^{sT_s}$, which when approximated, can be written as

$$G_c(s) = G_c(z)|_{z=e^{sT_s}} \approx G_c(z)|_{z=\frac{1+sT_s/2}{1-sT_s/2}}. \tag{3.22}$$

The ZOH block is moved to be in front of the DSP delay block so that the DSP delay and the comparator can be modeled as a delay block $G_{PWM}(s)$. When triangle carriers are used, the approximation of large signal transfer function



(a)



(b)

Figure 3.14: Block diagram of a single loop digitally controlled switching converter. (a) Original block diagram. (b) Rearranged block diagram.

of $G_{PWM}(s)$ can be derived by averaging the delay effects. Therefore, the block diagram of the single control loop in s-domain can be shown in Fig. 3.15. Analysis in s-domain can be performed based on this model. In most cases, the transfer function of the sampler can be regarded as $\frac{1}{T_s}$ with good accuracy under the Nyquist frequency.

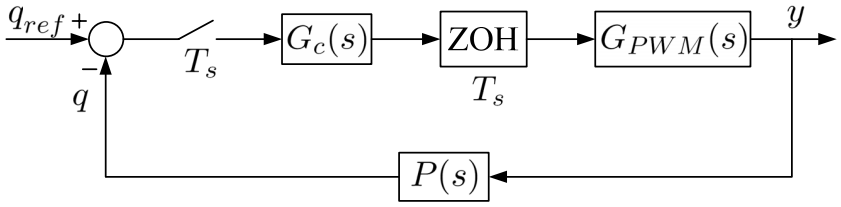


Figure 3.15: Block diagram of the single control loop in large signal s-domain.

3.4.2 Block diagram of a single control loop in small-signal z-domain

The digital PWM is a block described by a small-signal pulse-to-continuous transfer function $G^*_{PWM}(s)$. Hence, from $\widehat{x}^*$ to $\widehat{q}$, the pulse-to-continuous transfer

function becomes

$$H(s) = G^*_{PWM}(s)P(s). \tag{3.23}$$

To obtain the small-signal pulse transfer function describing the sample $\widehat{q}^*$ as a function of $\widehat{x}^*$, z-transform is used. Combining $H(s)$ with the sampler, the pulse transfer function can be derived as

$$H(z) = \mathcal{Z}\{H(s)\}. \tag{3.24}$$

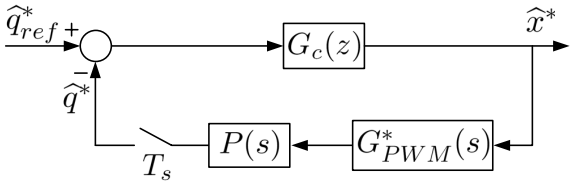


Figure 3.16: Block diagram of the single control loop in small-signal z-domain.

Therefore, the feedback path including the sampler can be described by the z-domain transfer function. The block diagram of the single control loop can be represented in Fig. 3.16, based on which the z-domain analysis can be implemented.

3.4.3 Block diagram of cascaded control loops in s-domain

In many second or higher order control systems, controllers with cascaded feedback loops are widely used. For a controller with two cascaded control loops, the internal control loop usually has a faster dynamic performance than that of the external one. The simplified block diagram can be schematically shown in Fig. 3.17. The plant transfer functions for internal control loop and external control loop are represented by $P_1(s)$ and $P_2(s)$, respectively.

In order to analyze the frequency response, the s-domain model in large signal is required. Instead of using q^*_{ref2}, q_{ref2} is used as the reference input. As a result, the sampler for the external feedback loop can be placed in front of the controller of the external loop. The compensators $G_{c1}(z)$ and $G_{c2}(z)$ are converted into s-domain using bilinear transforms. In a digital control loop, the transfer function of a sampler preceded by a ZOH is 1. Therefore, a virtual ZOH followed by a virtual sampler can be placed after the compensator $G_{c2}(s)$ in the external control loop. Moreover, the virtual sampler and the sampler in the internal feedback loop are moved in front of the controller of the internal loop. Therefore, the block diagram of the cascaded control loops in s-domain can be expressed as in Fig. 3.18.

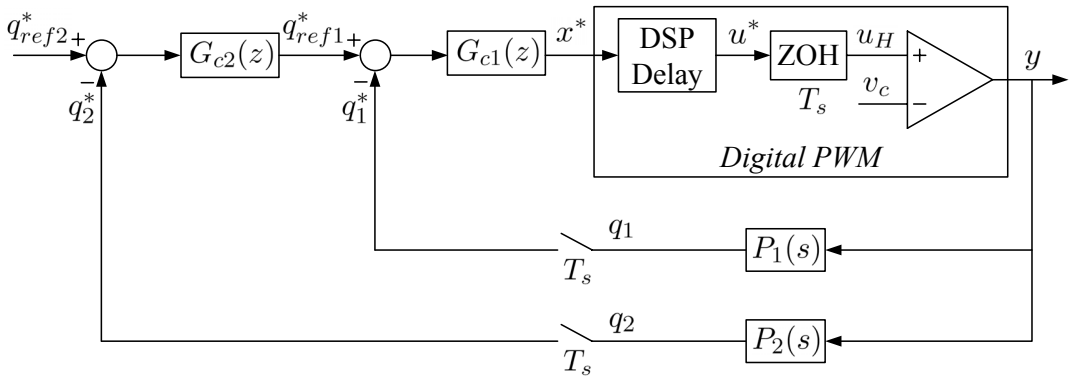


Figure 3.17: Block diagram of digitally controlled switching converter with cascaded loops.

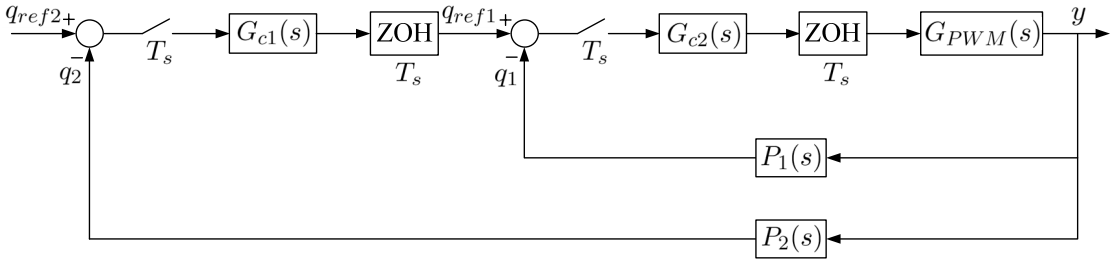


Figure 3.18: Block diagram of the cascaded control loops in large signal s-domain.

3.4.4 Block diagram of cascaded control loops in small-signal z-domain

Based on the z-domain modelling method for the single control loop, the block diagram of the two cascaded control loops can be arranged as in Fig. 3.19.

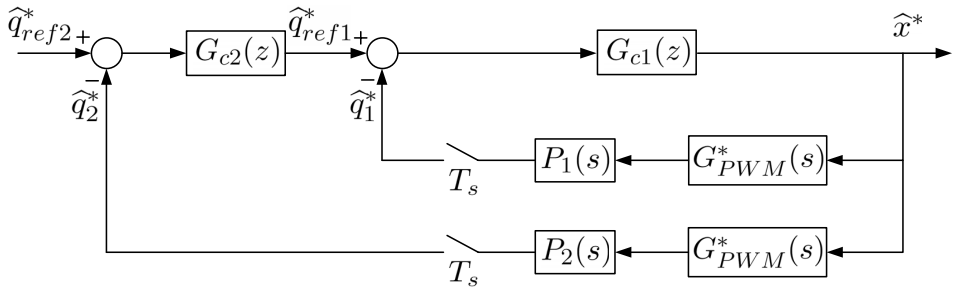


Figure 3.19: Block diagram of the cascaded control loops in small-signal z-domain.

Since the output of the PWM block is an analog signal, this block should be placed in each feedback path, where the sampler can convert the output into digital signal. The transfer functions for the feedback paths of the internal loop

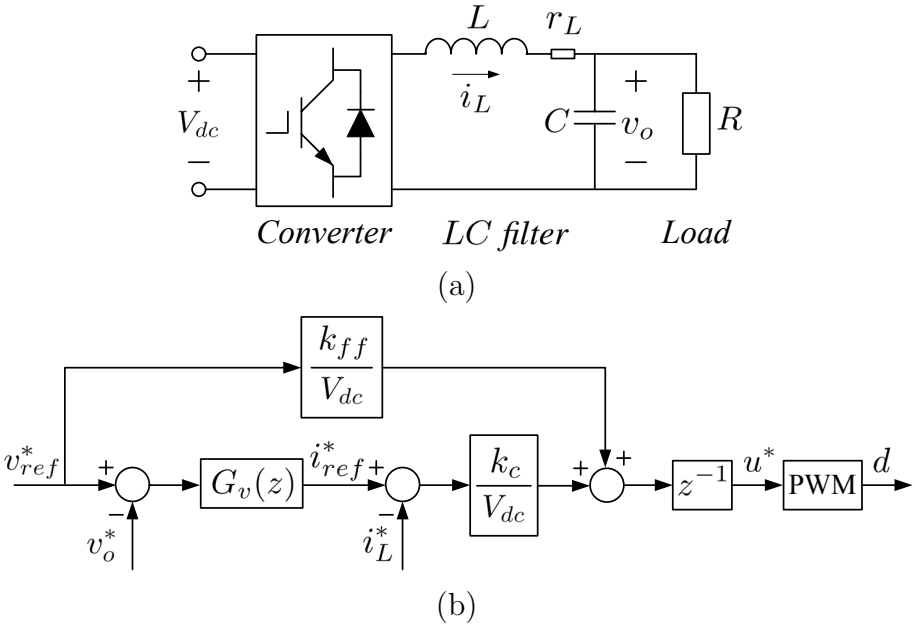


Figure 3.20: The digitally controlled buck inverter. (a) Power circuit. (b) Voltage and current controller.

and the external loop are given by

$$H_1(z) = \mathcal{Z}\{G^*_{PWM}(s)P_1(s)\} \tag{3.25}$$

and

$$H_2(z) = \mathcal{Z}\{G^*_{PWM}(s)P_2(s)\}, \tag{3.26}$$

respectively. Thus, the z-domain analysis of the cascaded control loops can be performed according to the block diagram.

3.5 Design of digital controllers

For a digitally controlled power inverter, the design of controller is according to the system specifications. Achieving good transient and steady-state performance and sufficient robustness are the main concerns for design. Robustness is required for the system to have enough stability margin. A typical robustness requirement is that a system should have a gain margin of two before reaching the stability boundary. Several methods can be used to implement the design, such as simulation, root locus and frequency response [27]. This section provides an example of the controller design for a digitally controlled power inverter to explain these methods. A voltage and current controlled bipolar switched H bridge buck inverter is exemplified and shown in Fig. 3.20.

The controller is comprised of cascaded feedback control loops with duty-ratio feedforward. The internal current compensator is a proportional compensator,

Table 3.1: Parameters of the Inverter

Symbol	Quantity	Value
V_{dc}	DC voltage amplitude	200 V
T_s	Sampling period	50 μs
L	Inductor	1642 μH
r_L	Inductor parasitic resistance	0.4 Ω
C	Capacitor	10 μF
R	Resistor	30 Ω

and the external voltage compensator is a PI compensator. The voltage PI controller is represented in z-domain as

$$G_v(z) = k_v(1 + \frac{k_i T_s}{z-1}). \tag{3.27}$$

The voltage and current are synchronously sampled and the DSP delay is assumed to be one switching cycle. Symmetric-on-time modulator is used to generate the drive signals. The parameters of the system are shown in Table 3.1. These parameters are extracted from the experimental system and used for the design example in this section.

3.5.1 Design by simulation

The first direct method to design and evaluate the controller is based on simulation [27]. A control system can be built in software such as MATLAB/Simulink with continuous-time and discrete-time models. The block diagram of the digitally controlled buck inverter is shown in Fig. 3.21.

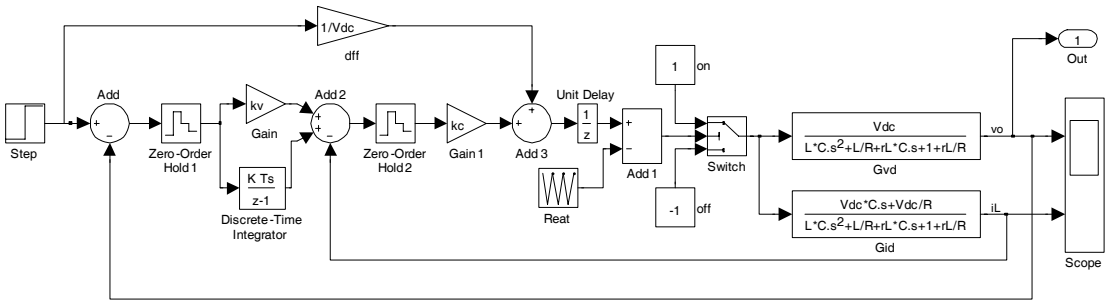


Figure 3.21: Simulink block diagram of digitally controlled buck inverter.

The reference voltage is set to step from zero to 100 V at 0.004 s. The transient response can be obtained from the simulation of the inverter model. When the parameters of the PI controller are chosen as $k_i = 5000$ and $k_v = 0.05$, the simulated voltage waveform is shown in Fig. 3.22. The transient response is evaluated by the rise time t_r, the settling time t_s and the overshoot M_p. These values

can be measured from the simulation results and the design can be implemented according to the time-domain specifications.

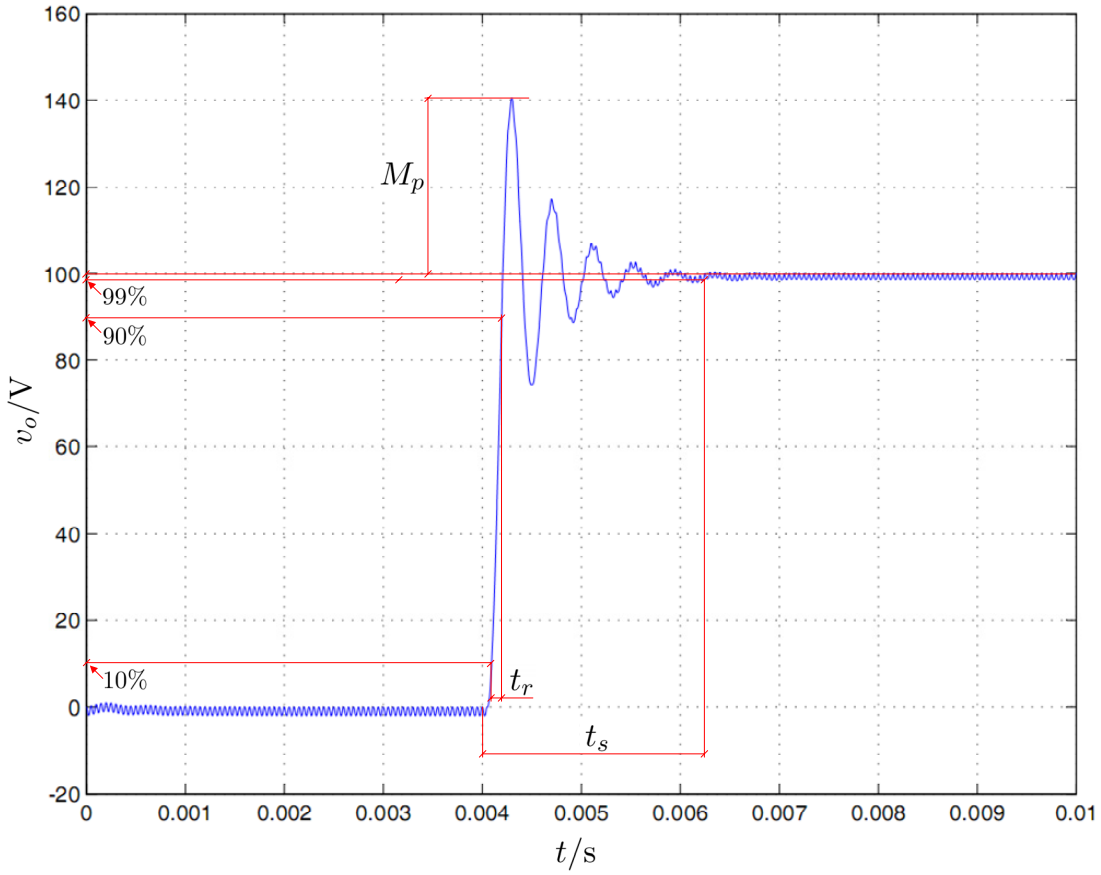


Figure 3.22: Simulation retrieved voltage waveform of the digitally controlled buck inverter.

The values measured for the transient response from the simulation are $t_r = 0.0001$ s, $t_s = 0.0024$ s, and $M_p = 42\%$. The overshoot appears with a oscillatory frequency of 2.44 kHz. As is shown in Fig. 3.22, the measured average steady-state error is 0.7%. In the following subsections, these results will be compared with the analytical results.

3.5.2 Design by root locus

The second method for controller design is based on the root locus of the discrete system [27]. For the PI controller of the buck inverter, the root locus is derived when the proportional gain k_v varies. The z-domain model of the buck inverter can be schematically shown in Fig. 3.23.

The discrete transfer functions $G_{i_Lx}(z)$ and $G_{v_ox}(z)$ can be obtained by

$$G_{i_Lx}(z) = \mathcal{Z}\{G^*_{PWM}(s)G_{i_Ly}(s)\} \tag{3.28}$$

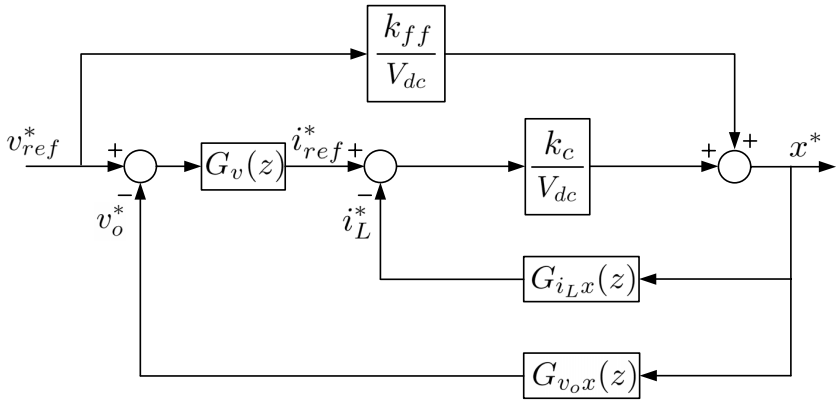


Figure 3.23: z-domain model of digitally controlled buck inverter.

and

$$G_{v_ox}(z) = \mathcal{Z}\{G^*_{PWM}(s)G_{v_oy}(s)\}, \tag{3.29}$$

respectively. The discrete transfer functions $G_{i_Lx}(z)$ and $G_{v_ox}(z)$ can be simplified to

$$G_{i_Lx}(z) = \frac{N_{i1}z + N_{i0}}{z^3 + D_1z^2 + D_0z} \tag{3.30}$$

and

$$G_{v_ox}(z) = \frac{N_{v1}z + N_{v0}}{z^3 + D_1z^2 + D_0z}, \tag{3.31}$$

respectively, with $N_{i0} = -\frac{V_{dc}T_sD_0}{2}(A_ie^{a\tau_1} + A_ie^{a\tau_2} + B_ie^{b\tau_1} + B_ie^{b\tau_2})$,
$N_{i1} = \frac{V_{dc}T_s}{2}(A_ie^{-a(T_s-\tau_1)} + A_ie^{-a(T_s-\tau_2)} + B_ie^{-b(T_s-\tau_1)} + B_ie^{-b(T_s-\tau_2)})$,
$N_{v0} = -\frac{V_{dc}T_sD_0}{2}(A_ve^{a\tau_1} + A_ve^{a\tau_2} + B_ve^{b\tau_1} + B_ve^{b\tau_2})$,
$N_{v1} = \frac{V_{dc}T_s}{2}(A_ve^{-a(T_s-\tau_1)} + A_ve^{-a(T_s-\tau_2)} + B_ve^{-b(T_s-\tau_1)} + B_ve^{-b(T_s-\tau_2)})$,
$D_1 = -e^{-aT_s} - e^{-bT_s}$, $D_0 = e^{-(a+b)T_s}$, $a = \frac{1}{2}(\frac{1}{CR} + \frac{r_L}{L} + \sqrt{\Delta})$, $b = \frac{1}{2}(\frac{1}{CR} + \frac{r_L}{L} - \sqrt{\Delta})$,
$\Delta = (\frac{1}{CR} + \frac{r_L}{L})^2 - \frac{4(R+r_L)}{LCR}$, $A_i = \frac{aCR-1}{LCR(a-b)}$, $B_i = \frac{1-bCR}{LCR(a-b)}$, $A_v = -\frac{1}{LC(a-b)}$, $B_v = \frac{1}{LC(a-b)}$, $\tau_1 = \frac{(1-D)T_s}{2}$ and $\tau_2 = \frac{(1+D)T_s}{2}$.

Therefore, when $k_c = 16$ and $k_{ff} = 1$, the open-loop transfer function can be obtained based on the z-domain model and the root locus versus k_v is shown in Fig. 3.24.

When $k_v = 0.05$, it can be obtained from Fig. 3.24 that the conjugate pole pairs have a damping ratio of $\zeta = 0.136$ and a natural frequency (angular) of $\omega_n = 15.5$ kHz. Thus, the rise time and settling time are given by

$$t_r \approx \frac{1.8}{\omega_n} = 0.00012 \tag{3.32}$$

and

$$t_s \approx \frac{4.6}{\zeta\omega_n} = 0.0023, \tag{3.33}$$

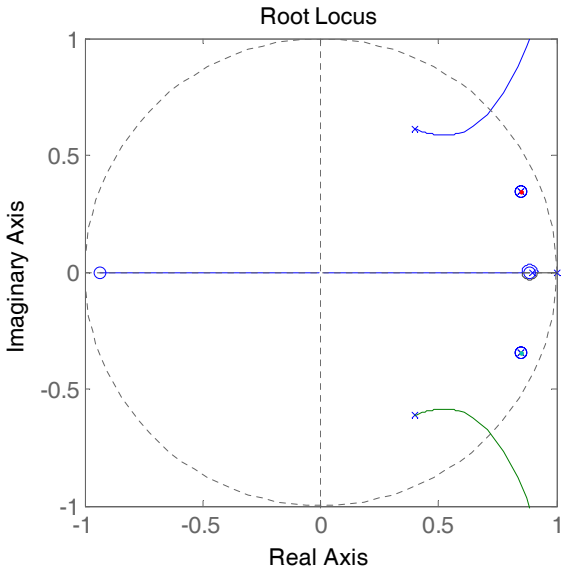


Figure 3.24: Root locus of digitally controlled buck inverter.

respectively. The overshoot can be crudely approximated by

$$M_p \approx e^{-\pi\zeta/\sqrt{1-\zeta^2}} = 67\%. \tag{3.34}$$

Compared to the previous subsection, the rise time and settling time results retrieved from root locus are almost in accordance with the simulation results. The conjugate poles ($0.622 \pm j0.645$) have a oscillatory frequency of 2.44 kHz (This is different from the natural frequency). However, as (3.34) is a crude approximation [27], the overshoot results of the two methods are not in good agreement.

3.5.3 Design by frequency response

Frequency response design based on the Bode plot has attracted wide interests [27]. The Bode plot can be obtained by either mathematical model or experimental measurement. By using frequency response method, the gain and phase at required frequency of the system can be directly obtained from the Bode diagram. Nyquist's stability condition such as gain and phase margins can be retrieved. The steady-state error, resonant peak and bandwidth can also be observed from the frequency response.

Following on from the example of the buck inverter, based on Fig. 3.23, the closed-loop transfer function can be written as

$$G_{close}(z) = \frac{(k_{ff} + G_v(z)k_c)G_{v_ox}(z)}{V_{dc} + G_v(z)k_cG_{v_ox}(z) + k_cG_{i_Lx}(z)}. \tag{3.35}$$

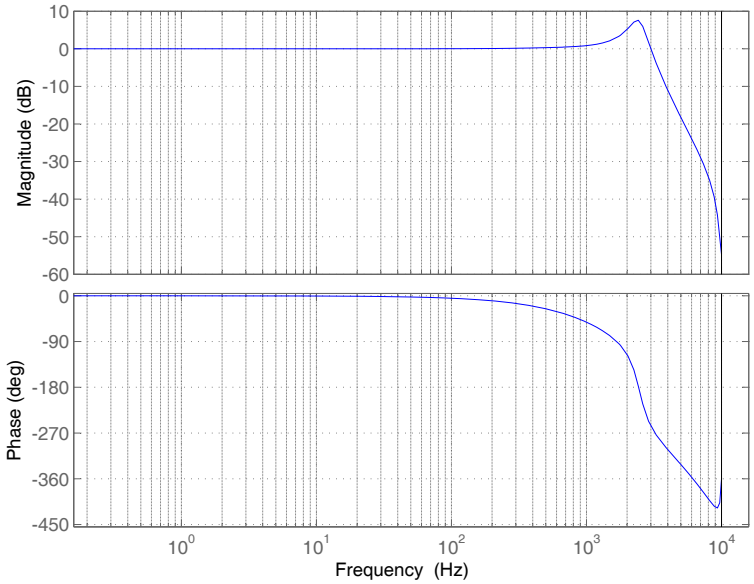


Figure 3.25: Bode diagram of closed-loop transfer function of the buck inverter.

The Bode diagram of the closed-loop transfer function is shown in Fig. 3.25. The Bode curve stops at Nyquist frequency which is 10 kHz. As can be measured from the Bode diagram, the gain in low frequency range is almost unity. The resonant peak appears at the frequency of 2.43 kHz and the steady-state error is less than 0.01%. The bandwidth of the system is about 3.22 kHz. Compared to the simulation result, the resonant frequency on Bode diagram is in accordance with the simulated oscillatory frequency in the transient response.

3.6 Simulation and experimental preparations

3.6.1 Simulation environment

The simulation work of the thesis is implemented in MATLAB/Simulink and PLECS. The digital controllers can be built up by commonly used classic Simulink models. The power circuit is comprised of PLECS elements. PLECS is a Simulink toolbox developed by Plexim GmbH for fast simulation of power electronic circuits. A typical example of PLECS circuit is shown in Fig. 3.26.

3.6.2 Experimental setup

Experimental systems in the thesis are comprised of power inverters, filters, measurement circuits and digital signal processors. Each power inverter printed circuit board (PCB) is composed of Mitsubishi Intelligent Power Modules (IPM) PM30CSJ060 with a heat sink and optical couplers for drive. This board con-

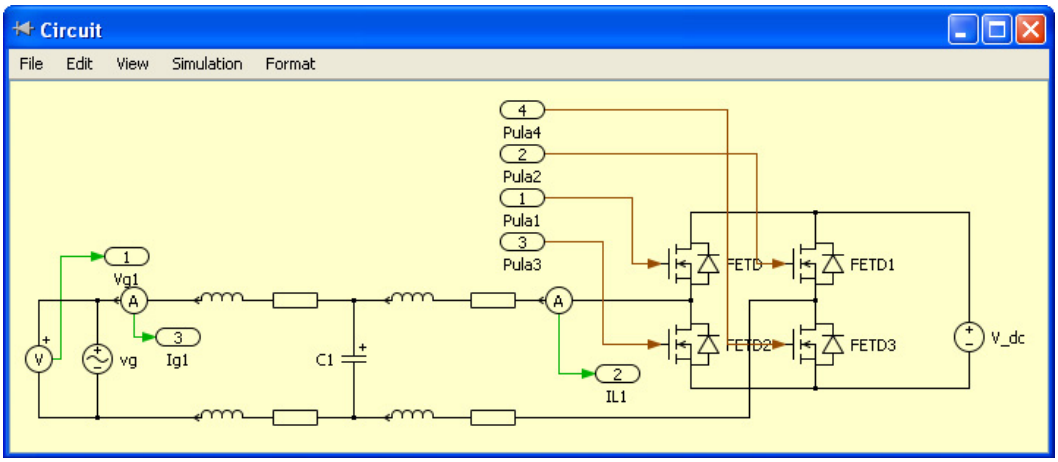


Figure 3.26: A grid-connected inverter power circuit composed by PLECS elements.

tains a three-phase inverter but is only used as a single-phase inverter (one leg is not used). The input of this board is a dc power from a voltage source for inverters' dc-link and PWM signals for driving switches. The output of this board is the voltage between two legs of the H bridge and the fault signal of IPM. The PCB layout is shown in Fig. 3.27.

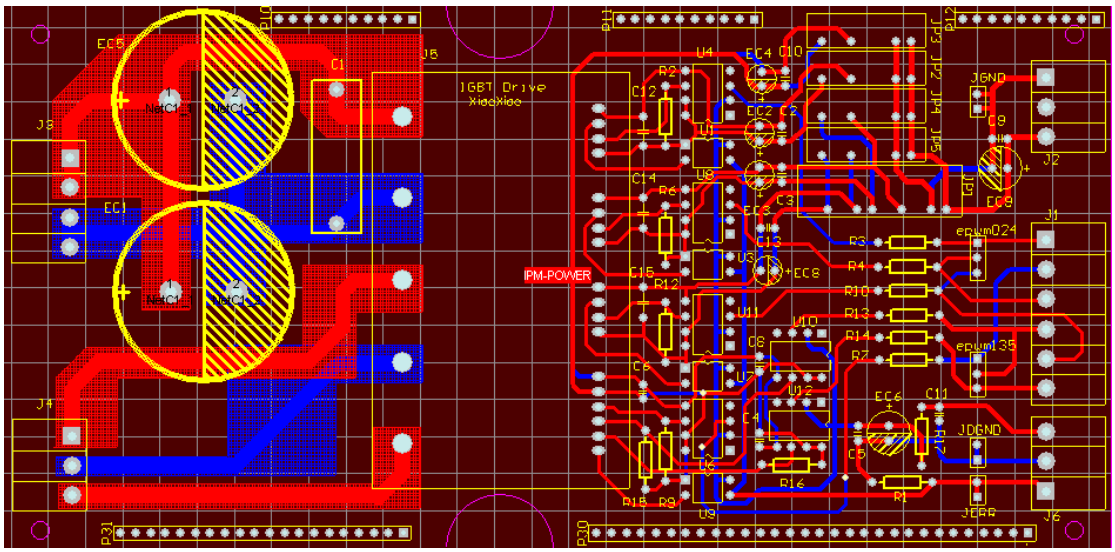


Figure 3.27: The PCB layout of a power inverter and drive circuit.

The output filter and measurement circuit for voltage and current signals are designed on one board, which PCB layout is shown in Fig. 3.28. The filter is an LCL filter which can also be used as an LC filter. The currents of the two inductors are measured by Hall sensors and converted to an analog signal ranging from 0 to 3 V. The voltages of the capacitor and the output terminal are measured and converted as well. The input of this board is the switch voltage. The output

of this board is the output voltage of the capacitor, the output current of grid side inductor, and the measured signals for ADCs.

The TMS320F28335 Experimenter Kits are used as the main controllers. The controller boards are designed by Texas Instrument. Each controller board provides drive signals for inverter board. The controller board also monitors the fault signal from IGBTs for protection. The measured signals of voltages and currents are provided to ADC channels on the controller board. The picture of the TMS320F28335 Experimenter Kit is shown in Fig. 3.29.

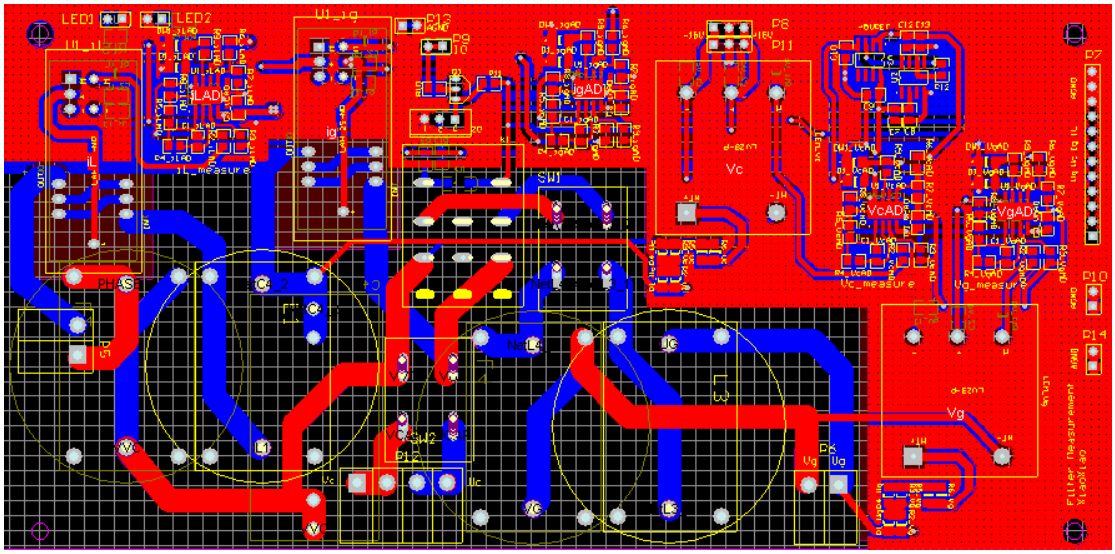


Figure 3.28: The PCB layout of a filter and measurement circuit.

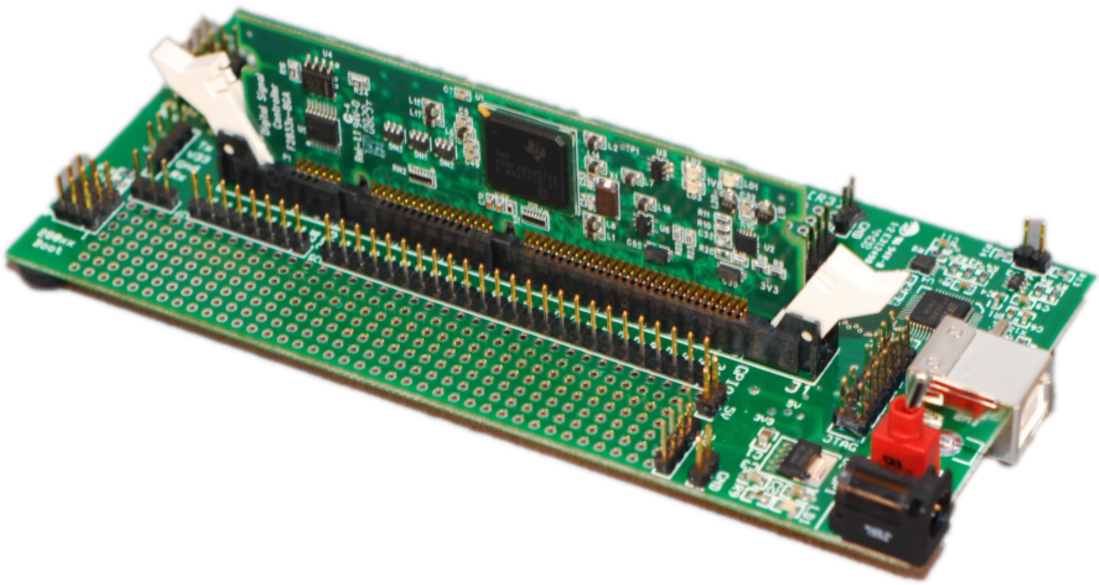


Figure 3.29: The picture of the controller board.

A single-phase inverter can be comprised of a power inverter board, a filter and measurement board and a controller board. This inverter system can operates in either stand-alone mode or grid-connected mode. By arranging more power inverter boards together without changing the filter and measurement board and the controller board, the multilevel cascade inverter can be constructed.

3.7 Conclusions

This chapter presents a general modelling technique for digitally controlled switching converters. The chapter analyzes the delay effect of uniformly-sampled PWMs in detail. The delay effect varies when different carriers and duty-ratio update methods are used. The small-signal PWM model precisely describes the delay effect in a digital controller. This model is also extended to bipolar and unipolar switched H bridges. The approximated models for double-update-mode PWMs are also obtained. Block diagrams for digital control systems are obtained in both s-domain and z-domain based on the proposed model. Therefore, a digital controller can be designed either in s-domain or in z-domain. An example of controller design based on z-domain model is provided. This controller is directly designed in z-domain and the control performance is evaluated based on the z-domain analysis. A comparison between different design methods reveals the validity of the proposed model. Finally, the simulation software and experimental setup for the rest the thesis are presented, which shows the methods used in this thesis for validation of the proposed models.

Chapter 4

Design of Digitally Controlled Parallel Inverters

4.1 Introduction

This chapter provides an example of designing digital controllers for voltage controlled inverters in renewable energy system. As is known, the load sharing performance of digitally controlled parallel inverters is influenced by the output filter and the line impedance between each inverter. Hence, designing the controller usually determines how accurately the inverters share the load. For inverters with the same circuit and control parameters, it seems that the load can be shared equally. However, the filter inductors and capacitors and the feedback circuits of the parallel inverters usually have notable difference. Due to the inconsistencies of the filter and measurements parameters, guaranteeing accurate sharing between each inverter under all circumstances is not straightforward. For this reason, droop control methods have been developed [51]–[52], which are suitable for parallel inverters with considerable unknown differences of the filter parameters and line impedance between each module. This strategy is based on the conventional frequency and voltage droop according to the output power, which achieves accurate active power sharing but inaccurate reactive power sharing due to the mismatched line impedances [51], [53].

Since the frequency droop method achieves good accuracy in sharing loads, it has been extended to improve the sharing accuracy of the reactive current or any order of harmonic current [54]. However, injecting a series of harmonic signals and calculating the power for each component is not practical. More realistic methods are proposed in [40], [55] and [56], which enforce the output impedance of the inverters. Output current feedback is used as a virtual impedance loop in these methods. To suppress the harmonic distortion when nonlinear loads are connected, the voltage reference is generated with a droop according to each har-

monic component of the output current [2],[57]. This harmonic sharing method is similar to the scheme proposed in [58], which can be considered as decreasing the magnitude of output impedance at harmonic frequencies. These control strategies are combined with the droop methods to obtain a good sharing accuracy.

Usually, power sharing is mainly implemented by using droop control methods. For high performance parallel inverters system, droop controller may result in poor transient response performance [59] or reduced voltage regulation due to the frequency variation. For digitally controlled parallel inverters connected with short cables, the droop controller can be removed if the voltage controller is capable of overcoming the mismatched hardware parameters. Without droop controller, synchronizing inverters to the grid is straightforward. However, if the controller is insufficient to achieve accurate load sharing, the droop controller must be used to compensate the error. In order to achieve a good control performance, the feedback gains of the inverters at the fundamental and harmonic frequencies should be relatively high. The proportional gains of each inverter are usually limited since it will reduce the stability margin significantly in digitally controlled systems [60]. Therefore, an additional resonant compensator is proposed to enhance the gain at the fundamental frequency [14], [61]. The proportional plus resonant (PR) compensator can achieve high gain at selected frequencies, reducing the sensitivity versus the circuit parameters. Nevertheless, when PR controller is applied, trade off between stability, dynamic performance and control accuracy has to be made. With higher proportional gains applied, the steady-state error is reduced, but the system may become unstable. On the other hand, a compensator with a high gain resonating at the fundamental frequency has little influence on stability, but it brings significant phase error especially when the line frequency varies.

In this chapter, the z-domain model is derived for digitally controlled inverter, based on which the stability is investigated. The limitation of the proportional gains in feedback loops is obtained which must be followed during the design. A good trade off between stability and control accuracy is achieved by using a linear voltage control scheme [30], [48] with duty-ratio feedforward [28]. Compared to the classic PR controller, the proposed linear voltage control scheme with duty-ratio feedforward highlights advantages such as: simple structure, low sensitivities, good sharing performance and higher output voltage quality. The theoretical analysis have been verified by the simulation and experimental results of two digitally controlled inverters connected in parallel.

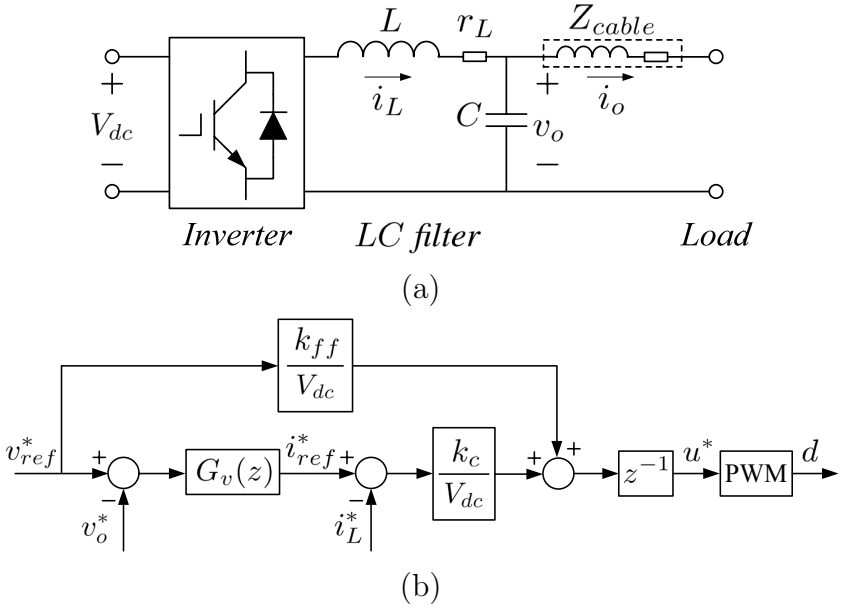


Figure 4.1: The single phase digitally controlled inverter. (a) The power circuit. (b) The controller.

4.2 Small-signal z-domain analysis of digitally controlled inverters

The typical power circuit prototype and controller for a voltage controlled inverter are shown in Fig. 4.1. The power circuit consists of a bipolar switched H bridge and an output LC filter. The controller, as shown in Fig. 4.1(b), is a cascaded digital controller consisting of a capacitor voltage and an inductor current feedback with duty-ratio feedforward. The inductor current is sensed for the internal current feedback loop, where i^*_L is the ideally sampled quantity. Although the capacitor current feedback is an alternative solution, since the load usually has a negligible dynamic behaviour, the two feedback schemes are equivalent [44]. The capacitor voltage is sensed for the external voltage feedback loop, where v^*_o is the ideally sampled quantity. Both the sampling period and the switching period are $T_s = \frac{1}{f_s}$. The duty-ratio calculated from the samples is updated at each sampling instant, therefore the duty-ratio update delay[1] is z^{-1}. In digitally controlled systems, using the s-domain model for stability analysis will lead to inaccurate results. Therefore, in order to choose the control parameters in the feedback path, the stability of the system is studied in small-signal z-domain.

The current control loop with a digital PWM modeled by a pulse-to-continuous

[1]Once the circuit variables are sampled, the digital processor calculates the duty-ratio value, which needs some time. In the same time, the PWM compare register is waiting for the next sampling instant to update the duty-ratio value. Hence, the computation delay has already been included in the duty-ratio update delay.

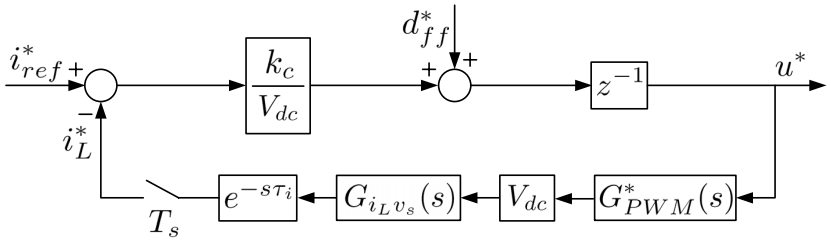


Figure 4.2: Model for the current control loop of the digitally controlled inverter.

transfer function $G^*_{PWM}(s)$ is represented as in Fig. 4.2. If the average duty-ratio D is scaled into the range of $0 \leq D \leq 1$, where $D = 0$ and $D = 1$ represent the inverter achieving minimum output $-V_{dc}$ and maximum output V_{dc}, respectively, the transfer function of the ZOH and PWM in small-signal model can be represented as [25]

$$G^*_{PWM}(s) = T_s(\alpha e^{-s\tau_1} + (1-\alpha)e^{-s\tau_2}), \tag{4.1}$$

where ratio α $(0 \leq \alpha \leq 1)$ is the duration of the falling edge of the carrier relative to the sampling period T_s, which can result in end-of-on-time sawtooth, begin-of-on-time sawtooth and symmetric-on-time triangle carriers. $\tau_1 = (\alpha - \alpha D)T_s$ and $\tau_2 = (\alpha + D - \alpha D)T_s$. In (4.1), the gain T_s and the delay $e^{-s\tau_{1,2}}$ are introduced by the ZOH and the PWM generator, respectively. Assuming the total delay of the switches drive and signals transport is τ_i, when the cable resistance is negligible and a pure resistor R is loaded in Fig. 4.1(a), the transfer function from u^* to i^*_L in z-domain can be derived as [6]

$$G_{iu}(z) = \mathcal{Z}\{G^*_{PWM}(s)V_{dc}G_{i_L v_s}(s)e^{-s\tau_i}\} \tag{4.2}$$

with

$$G_{i_L v_s}(s) = \frac{s/L + 1/LCR}{s^2 + s(1/CR + r_L/L) + (R + r_L)/LCR}. \tag{4.3}$$

This z-transform can be derived by splitting $G_{iu}(z)$ to

$$\begin{aligned} G_{iu}(z) = {} & \alpha V_{dc}T_s\left(\frac{A_i e^{a(\tau_1+\tau_i-T_s)}}{z - e^{-aT_s}} + \frac{B_i e^{b(\tau_1+\tau_i-T_s)}}{z - e^{-bT_s}}\right) \\ & + (1-\alpha)V_{dc}T_s\left(\frac{A_i e^{a(\tau_2+\tau_i-T_s)}}{z - e^{-aT_s}} + \frac{B_i e^{b(\tau_2+\tau_i-T_s)}}{z - e^{-bT_s}}\right) \end{aligned} \tag{4.4}$$

with $a = \frac{1}{2}(\frac{1}{CR} + \frac{r_L}{L} + \sqrt{\Delta})$, $b = \frac{1}{2}(\frac{1}{CR} + \frac{r_L}{L} - \sqrt{\Delta})$, $\Delta = (\frac{1}{CR} + \frac{r_L}{L})^2 - \frac{4(R+r_L)}{LCR}$, $A_i = \frac{aCR-1}{LCR(a-b)}$ and $B_i = \frac{1-bCR}{LCR(a-b)}$. Hence, the transfer function $G_{iu}(z)$ becomes

$$G_{iu}(z) = \frac{N_{i1}z + N_{i0}}{z^2 + D_1 z + D_0} \tag{4.5}$$

with $N_{i1} = V_{dc}T_s(\alpha A_i e^{-a(T_s-\tau_1-\tau_i)} + (1-\alpha)A_i e^{-a(T_s-\tau_2-\tau_i)} + \alpha B_i e^{-b(T_s-\tau_1-\tau_i)} + (1-\alpha)B_i e^{-b(T_s-\tau_2-\tau_i)})$,
$N_{i0} = -V_{dc}T_s D_0(\alpha A_i e^{a(\tau_1+\tau_i)} + (1-\alpha)A_i e^{a(\tau_2+\tau_i)} + \alpha B_i e^{b(\tau_1+\tau_i)} + (1-\alpha)B_i e^{b(\tau_2+\tau_i)})$, $D_1 = -e^{-aT_s} - e^{-bT_s}$ and $D_0 = e^{-(a+b)T_s}$. The discrete-time closed-loop transfer function from i^*_{ref} to u^* without feedforward is written as

$$G_1(z) = \frac{\frac{k_c}{V_{dc}} z^{-1}}{1 + \frac{k_c}{V_{dc}} z^{-1} G_{iu}(z)}. \tag{4.6}$$

The characteristic equation of (4.6) is

$$z^3 + D_1 z^2 + (D_0 + \frac{N_{i1}k_c}{V_{dc}})z + \frac{N_{i0}k_c}{V_{dc}} = 0. \tag{4.7}$$

Since $a+b = \frac{1}{CR} + \frac{r_L}{L}$, it can be derived that $D_0 = e^{-(1/RC + r_L/L)T_s}$ and $A_i + B_i = \frac{1}{L}$. If $f_s \gg \frac{1}{\sqrt{LC}}$, $f_s \gg \frac{r_L}{L}$ and delay τ_i is very small compared to one switching period, in the extreme condition of no load ($R = \infty$), it can be approximated that $a = j\sqrt{\frac{1}{LC}}$, $b = -j\sqrt{\frac{1}{LC}}$ (the real parts of a and b are much smaller than their imaginary parts), $D_0 = 1$ and $D_1 = -2$ (the absolute value of D_1 reduces if $f_s\sqrt{LC}$ is close to 1). When the sawtooth carriers are used, e.g. the end-of-on-time carrier with $\alpha = 0$ and $\tau_2 = DT_s$, N_{i1} and N_{i0} becomes

$$N_{i1} = V_{dc}T_s((A_i + B_i)\cos(\sqrt{\frac{1}{LC}}(1-D)T_s) - j(A_i - B_i)\sin(\sqrt{\frac{1}{LC}}(1-D)T_s)) \tag{4.8}$$

and

$$N_{i0} = -V_{dc}T_s D_0((A_i + B_i)\cos(\sqrt{\frac{1}{LC}}DT_s) + j(A_i - B_i)\sin(\sqrt{\frac{1}{LC}}DT_s)), \tag{4.9}$$

respectively.

If the assumption of the $\cos(\sqrt{\frac{1}{LC}}DT_s) \approx 1$ is used, $(A_i + B_i)\cos(\sqrt{\frac{1}{LC}}DT_s)$ is much bigger than $(A_i - B_i)\sin(\sqrt{\frac{1}{LC}}DT_s)$. Then the approximation of $N_{i1} = \frac{V_{dc}T_s}{L}$ and $N_{i0} = -\frac{V_{dc}T_s}{L}$ can be obtained. Similarly, when the triangle carriers are used, e.g. the symmetric-on-time carrier with $\alpha = \frac{1}{2}$, $\tau_1 = \frac{(1-D)T_s}{2}$ and $\tau_2 = \frac{(1+D)T_s}{2}$, the approximation of $N_{i1} = \frac{V_{dc}T_s}{L}$ and $N_{i0} = -\frac{V_{dc}T_s}{L}$ can be derived using the same approach. Substituting the approximated values of $D_0 = 1$, $D_1 = -2$, $N_{i1} = \frac{V_{dc}T_s}{L}$ and $N_{i0} = -\frac{V_{dc}T_s}{L}$ into (4.7), the equation becomes

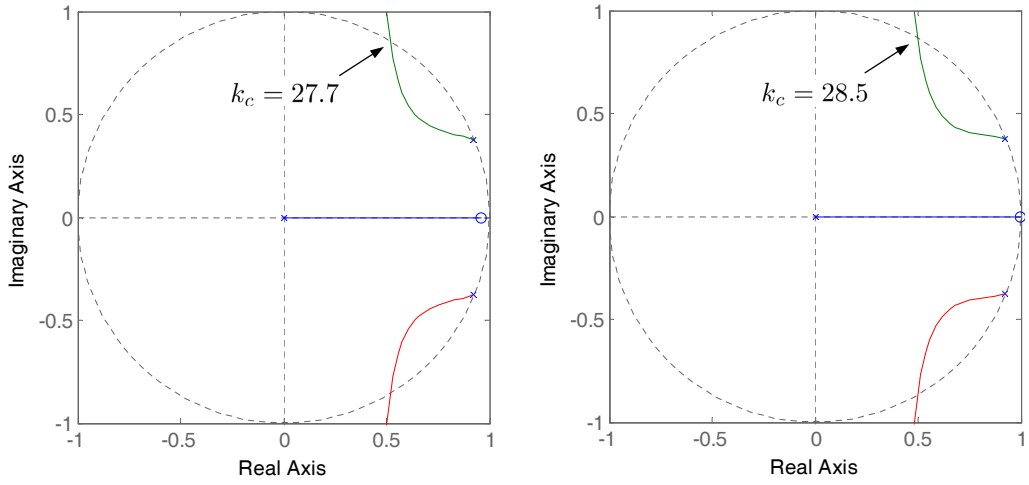
$$(z^2 - z + \frac{T_s k_c}{L})(z-1) = 0. \tag{4.10}$$

If $\frac{T_s k_c}{L} < 0$, the pole $z = \frac{1}{2} + \frac{1}{2}\sqrt{1 - \frac{4T_s k_c}{L}}$ will be out of the unit circle. If $\frac{T_s k_c}{L} > 1$, there will be two conjugated poles out of the unit circle. Therefore, the internal loop stable condition is

$$0 < k_c < \frac{L}{T_s}. \tag{4.11}$$

Table 4.1: Parameters of the Islanding Inverters

Symbol	Quantity	Value
V_{dc}	DC voltage amplitude	200 V
T_s	Switching and sampling period	50 μs
L	Inductance	1642 μH
C	Capacitance	10 μF
r_L	Inductor parasitic resistance	0.4 Ω



(a) (b)

Figure 4.3: Root loci of the internal current loop. (a) End-of-on-time modulator with $D = 0.75$. (b) Symmetric-on-time modulator with $D = 0.5$.

Numerical results are also provided to verify the approximated analytical stability condition (4.11). By using the parameters in Table 4.1, the root loci of the internal loop with different carriers are shown in Fig. 4.3. The accurate results for maximum k_c can be obtained. In Fig. 4.3(a) and (b), the maximum gain values are $k_c = 27.7$ and $k_c = 28.5$, respectively, which are smaller than the analytical result of $\frac{L}{T_s} = 32.8$ in (4.11). This is because that the numerical result of $D_0 = -1.83$ ($f_s\sqrt{LC} = 2.55$) is quite different from the approximation of $D_0 = -2$ ($f_s\sqrt{LC} \gg 1$). However, regardless of the carriers and average duty-ratio, the approximated result in (4.11) is acceptable and k_c is usually much smaller than the critical value $\frac{L}{T_s}$ in practice. This k_c is also related to the external voltage loop stability. In order to find proper control parameters, the entire model of the cascaded control loops is required [59].

The digitally controlled inverter with cascaded control loops is schematically represented in Fig. 4.4 [6], where

$$G_{v_o v_s}(s) = \frac{1/LC}{s^2 + s(1/CR + r_L/L) + (R + r_L)/LCR}. \tag{4.12}$$

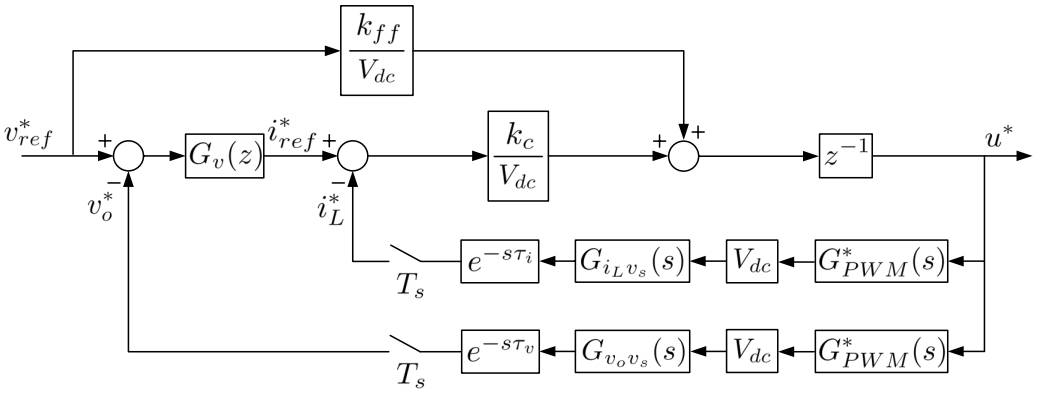


Figure 4.4: Model for the cascaded control loops of the digitally controlled inverter.

The discrete transfer function from u^* to v_o^* is written as

$$G_{vu}(z) = \mathcal{Z}\{G^*_{PWM}(s)V_{dc}G_{v_o v_s}(s)e^{-s\tau_v}\} \tag{4.13}$$

with τ_v a negligible delay introduced by the drivers and transport of signals. The transfer function $G_{vu}(z)$ can be derived as

$$\begin{aligned} G_{vu}(z) = {} & \alpha V_{dc}T_s\left(\frac{A_v e^{a(\tau_1+\tau_v-T_s)}}{z-e^{-aT_s}} + \frac{B_v e^{b(\tau_1+\tau_v-T_s)}}{z-e^{-bT_s}}\right) \\ & + (1-\alpha)V_{dc}T_s\left(\frac{A_v e^{a(\tau_2+\tau_v-T_s)}}{z-e^{-aT_s}} + \frac{B_v e^{b(\tau_2+\tau_v-T_s)}}{z-e^{-bT_s}}\right) \end{aligned} \tag{4.14}$$

with $A_v = -\frac{1}{LC(a-b)}$ and $B_v = \frac{1}{LC(a-b)}$. Therefore, $G_{vu}(z)$ can be written in a shorter form as

$$G_{vu}(z) = \frac{N_{v1}z + N_{v0}}{z^2 + D_1 z + D_0} \tag{4.15}$$

with

$N_{v1} = V_{dc}T_s(\alpha A_v e^{-a(T_s-\tau_1-\tau_v)} + (1-\alpha)A_v e^{-a(T_s-\tau_2-\tau_v)} + \alpha B_v e^{-b(T_s-\tau_1-\tau_v)} + (1-\alpha)B_v e^{-b(T_s-\tau_2-\tau_v)})$

and

$N_{v0} = -V_{dc}T_s D_0(\alpha A_v e^{a(\tau_1+\tau_v)} + (1-\alpha)A_v e^{a(\tau_2+\tau_v)} + \alpha B_v e^{b(\tau_1+\tau_v)} + (1-\alpha)B_v e^{b(\tau_2+\tau_v)})$.

Hence, according to Fig. 4.4, the closed-loop transfer function from v^*_{ref} to v^*_o without feedforward can be written as

$$G_2(z) = \frac{G_v(z)G_1(z)G_{vu}(z)}{1 + G_v(z)G_1(z)G_{vu}(z)}. \tag{4.16}$$

The stability usually limits the proportional gains in the digitally controlled converters [60]. Root loci are used to find the proper value of k_v. To ensure enough stability, the control parameter k_c should be smaller than the maximum value in Fig. 4.3. In our case, $k_c = 8$ is chosen. Then the external voltage loop

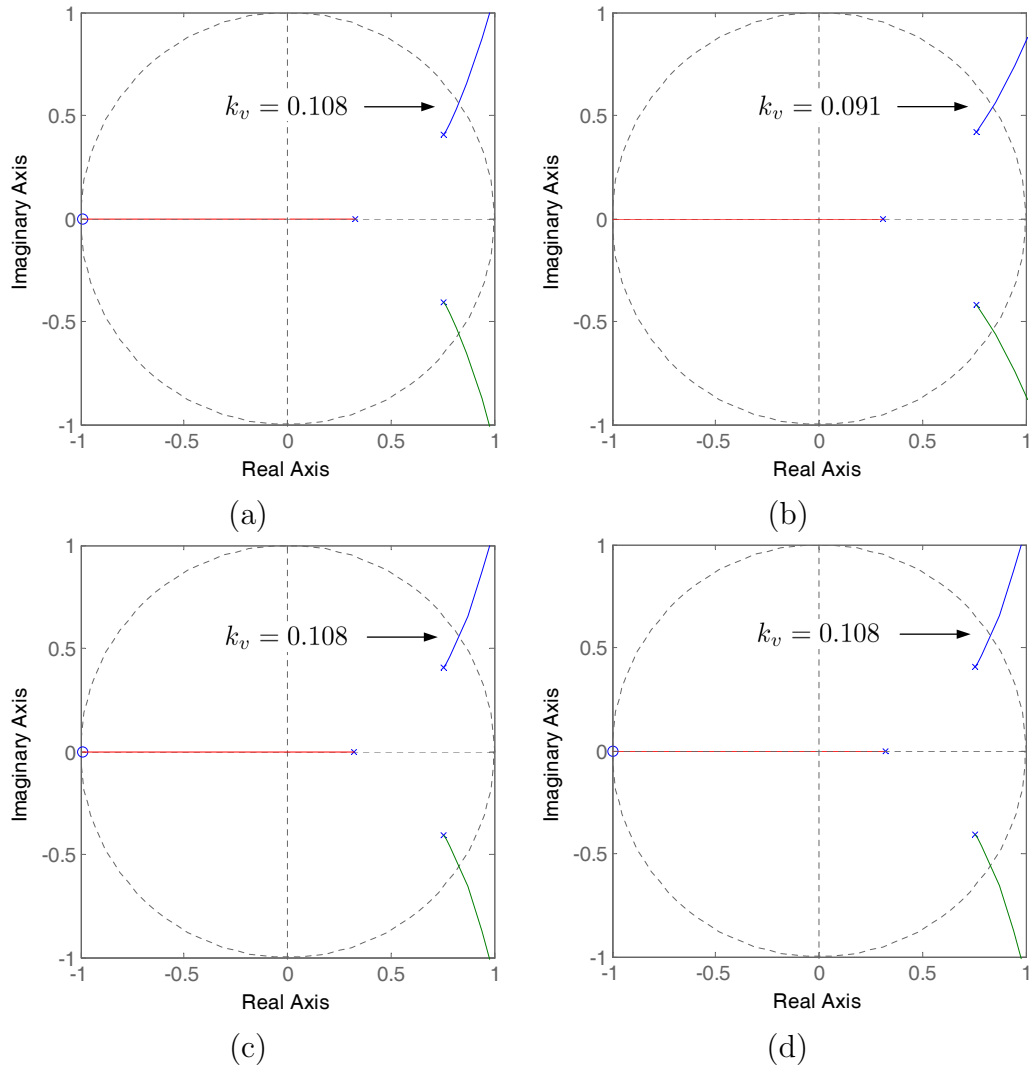


Figure 4.5: Root loci of the external voltage loop. (a) End-of-on-time modulator with $D = 0.5$. (b) End-of-on-time modulator with $D = 0.75$. (c) Symmetric-on-time modulator with $D = 0.5$. (d) Symmetric-on-time modulator with $D = 0.75$.

stability can be studied based on the z-domain closed-loop transfer function of (4.16). With the parameters in Table 4.1, when the inverter is not loaded, the root loci of the external voltage loop with different carriers and average duty-ratios are shown in Fig. 4.5.

It can be seen in Fig. 4.5 (a) and (b) that the external voltage loop stability condition for the end-of-on-time modulator is dependent on D. When $D = 0.5$ and $D = 0.75$, the critical values are given by $k_v = 0.108$ and $k_v = 0.091$, respectively. However, for the symmetric-on-time modulator, the stable condition is always $k_v < 0.108$. This is because when the end-of-on-time carrier is used, the transfer function of $G^*_{PWM}(s) = T_s e^{-sDT_s}$ is dependent on D, and consequently the closed-loop transfer function of (4.16) is also dependent on D. When D is

bigger, the delay is bigger and the stable range of k_v is reduced, which is a big disadvantage for its application in an ac system. On the other hand, when the triangle carriers are used, the approximation of $G^*_{PWM}(s) = T_s e^{-\frac{sT_s}{2}}$ [59] results in an average duty-ratio independent transfer function. The delay is as half as the switching period. In this case, the closed-loop transfer functions are almost the same with different D values. Therefore, the stability condition differs slightly while D is changing. The stability condition for triangle carriers is also equivalent to the condition when sawtooth carriers are used with $D = 0.5$ (half switching period delay). As uniform-sampling with sawtooth carriers can not obtain the average values of the inductor current and avoid switching noise [49, 32], in this chapter the symmetric-on-time modulator is used. The proportional gains are chosen as $k_c = 8$ and $k_v = 0.05$ to ensure stability and these gains are also associated with the inverter output impedance, which will be illustrated in the next section.

4.3 Controller design for power sharing

The closed-loop transfer function and output impedance are investigated in this section. The analysis is performed in large signal to obtain duty-ratio independent transfer functions. However, the analysis should be restricted to the frequency range under the half sampling frequency $\frac{f_s}{2}$. The exact model of the digitally controlled inverter is shown in Fig. 4.6, where the PWM equivalent delay $G_{PWM}(s)$ is comprised of the duty-ratio update delay and the switching delay. Since the duty-ratio is updated at each sampling instant, the duty-ratio update delay is one switching period. If the symmetric-on-time carrier is used, the switching delay is approximately equivalent to a half switching period [32]. As a result, $G_{PWM}(s)$ can be written as

$$G_{PWM}(s) = e^{-\frac{3}{2}sT_s}. \tag{4.17}$$

In Fig. 4.6, the ideal samplers are used to take the samples into the digital controller. On the other hand, the samples are converted to continuous-time signals by ZOHs. The transfer function of the ideal sampler is $\frac{1}{T_s}$, if the input signal contains frequencies lower than the $\frac{f_s}{2}$. The transfer function of the ZOH is known as $G^*_{ZOH}(s) = \frac{1-e^{-sT_s}}{s}$. Moreover, the transfer functions of $G_{i_L d}(s)$, $G_{v_o d}(s)$, $G_{i_L i_o}(s)$ and $G_{v_o i_o}(s)$ in Fig. 4.6 are expressed as

$$G_{i_L d}(s) = \frac{sCV_{dc}}{s^2LC + sr_LC + 1}, \tag{4.18}$$

$$G_{v_o d}(s) = \frac{V_{dc}}{s^2LC + sr_LC + 1}, \tag{4.19}$$

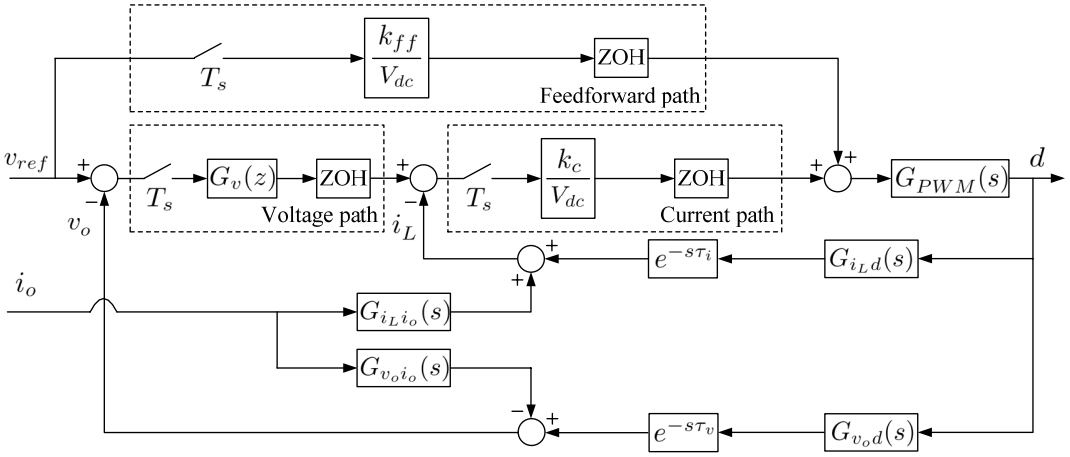


Figure 4.6: Model of the digitally controlled inverter.

$$G_{i_Li_o}(s) = \frac{1}{s^2LC + sr_LC + 1} \tag{4.20}$$

and

$$G_{v_oi_o}(s) = \frac{sL + r_L}{s^2LC + sr_LC + 1}, \tag{4.21}$$

respectively.

The digital compensator in the voltage control loop is a function of z. There are two design strategies for digital controllers. One is direct digital design [25] based on the z-domain model. The other one is indirect design which converts the known s-domain controller into z-domain [32]. For ac systems where resonant controllers are used, the indirect design is very good at implementing the continuous-time transfer functions. Hence, in this chapter the indirect design is used and the compensator is designed into z-domain by using bilinear transform. The voltage compensator is obtained from a known $G_v(s)$ by

$$G_v(z) = G_v(s)\big|_{s=\frac{2}{T_s}\frac{z-1}{z+1}}. \tag{4.22}$$

In reverse, mathematically, $G_v(s) = G_v(z)\big|_{z=\frac{1+sT_s/2}{1-sT_s/2}}$. As $z = e^{sT_s} \approx \frac{1+sT_s/2}{1-sT_s/2}$, therefore $G_v(z) = G_v(z)\big|_{z=e^{sT_s}} \approx G_v(z)\big|_{z=\frac{1+sT_s/2}{1-sT_s/2}} = G_v(s)$. Similarly, k_c and k_{ff} in digital controller are also equivalent to their continuous-time transfer function for the frequency lower than $\frac{f_s}{2}$. Therefore, the transfer function of the voltage path in Fig. 4.6 is equivalent to

$$G_{vp}(s) = G_v(s)G_{ZOH}(s) \tag{4.23}$$

with $G_{ZOH}(s)$ the transfer function of the ideal sampler and the ZOH. It is approximated that $G_{ZOH}(s) = \frac{1-e^{-sT_s}}{sT_s}$. The transfer functions of the current path and the feedforward path are

$$G_{cp}(s) = \frac{k_c}{V_{dc}}G_{ZOH}(s) \tag{4.24}$$

and

$$G_{ffp}(s) = \frac{k_{ff}}{V_{dc}} G_{ZOH}(s), \tag{4.25}$$

respectively. Hence, the continuous equivalent transfer functions for the entire digital controller are derived and the analysis of load sharing performance can be studied. According to Fig. 4.6, the closed-loop transfer function from v_{ref} to v_o is

$$G(s) = \frac{(G_{vp}(s)G_{cp}(s) + G_{ffp}(s))V_{dc}G_{PWM}(s)}{s^2LC + sC(G_{cp}(s)V_{dc}G_{PWM}(s) + r_L) + G_{vp}(s)G_{cp}(s)V_{dc}G_{PWM}(s) + 1} \tag{4.26}$$

and the output impedance transfer function from i_o to v_o is

$$Z(s) = \frac{sL + (G_{cp}(s)V_{dc}G_{PWM}(s) + r_L)}{s^2LC + sC(G_{cp}(s)V_{dc}G_{PWM}(s) + r_L) + G_{vp}(s)G_{cp}(s)V_{dc}G_{PWM}(s) + 1}. \tag{4.27}$$

4.3.1 Proportional plus resonant feedback control

As described in the previous section, for digitally controlled converters, the proportional gains are limited by the stability conditions. In practice, the integral compensator, resonant compensator or repetitive compensator, etc., are used together with the proportional compensator to improve the steady-state performance. For ac system operating at the fundamental frequency, the integral compensator is not usually used since it has high gain in low frequency range. However, the resonant compensator has high gain at resonant frequency and low gain at other frequencies. Therefore, the PR compensator is widely used to enhance the control accuracy in ac systems. This compensator implemented in a digital controller is derived by using bilinear transform, which is written as

$$G_{v_{PR}}(z) = k_v + k_1 \frac{a_{z1}z^2 + b_{z1}z + c_{z1}}{A_{z1}z^2 + B_{z1}z + C_{z1}}, \tag{4.28}$$

with $A_{z1} = \frac{4}{T_s^2} + \frac{4\xi\omega_1}{T_s} + \omega_1^2$, $B_{z1} = -\frac{8}{T_s^2} + 2\omega_1^2, C_{z1} = \frac{4}{T_s^2} - \frac{4\xi\omega_1}{T_s} + \omega_1^2$, $a_{z1} = \frac{4\xi\omega_1}{T_s}$, $b_{z1} = 0$ and $c_{z1} = -\frac{4\xi\omega_1}{T_s}$. The continuous equivalent s-domain transfer function of $G_{v_{PR}}(z)$ is

$$G_{v_{PR}}(s) = k_v + k_1 \frac{2\xi\omega_1 s}{s^2 + 2\xi\omega_1 s + \omega_1^2}. \tag{4.29}$$

To evaluate the PR compensator, the performance at the fundamental frequency is studied. It can be derived that $\omega_1^2 LC = 0.0016$ and $\omega_1 C = 0.0031\ \Omega^{-1}$. Therefore, at the fundamental frequency, the denominators of (4.26) and (4.27) are mainly determined by $G_{vp}(s)G_{cp}(s)V_{dc}G_{PWM}(s) + 1$. When the PR compensator without feedforward ($k_{ff} = 0$) is used [61], the gain of the closed-loop transfer function approaches unity when the gain in the feedback path, i.e.

$G_{vp}(s)G_{cp}(s)$ is high enough. Since $\omega_1 L = 0.515\ \Omega$, at the fundamental frequency, $G_{cp}(s)V_{dc}G_{PWM}(s)$ is much higher compared to sL in (4.27). Therefore, with a relative big k_1, the output impedance magnitude at the fundamental frequency is close to $\frac{1}{k_1}$. At harmonic frequencies, the output impedance magnitude of the proportional plus resonant compensator controlled inverter is nearly $\frac{k_c}{k_v k_c+1}$. As described in the previous section, k_v should be small enough to ensure the inverter stability, which will lead to big output impedances at harmonic frequencies. When nonlinear loads are connected, the current containing harmonic frequencies on the respective considerable output impedance will result in voltage distortion. In order to be able to trade off between voltage distortion and sharing performance, additional feedback has to be used [57].

4.3.2 Linear voltage feedback scheme using duty-ratio feedforward

Since the voltage drop across the filter inductor is usually very small, the average switch voltage $V_{dc}d$ and the output voltage v_o are almost identical. Therefore, by adding the voltage reference value directly to the PWM generator (see Fig. 4.1), the compensator only has to compensate for the small difference between $V_{dc}d$ and v_o instead of compensating for v_o entirely [28]. With duty-ratio feedforward, the tracking error will be much smaller. According to Fig. 4.1, the feedforward duty-ratio is

$$d_{ff} = k_{ff}\frac{v_{ref}}{V_{dc}}. \tag{4.30}$$

As illustrated in the previous subsection, when a classic PR compensator without feedforward ($k_{ff} = 0$) is used, the gain of $G(s)$ close to unity is achieved by a large numerator of Equation (4.26), i.e., by choosing a large gain of $G_v(s)k_c$. Resonant compensator with high gain can achieve large $G_v(s)$ at the fundamental frequency. However, high resonant gains will bring big phase error around the resonant frequency, which is not acceptable in practice. When feedforward ($k_{ff} = 1$) is applied, the gain of $G(s)$ is always close to unity. Hence, in the case of feedforward, steady-state accuracy does not depend on a high gain in the feedback path. On the other hand, the classic PR compensator arrangement is designed for linear load sharing [61]. In this case, additional compensation has to be used for nonlinear load sharing. In [57] and [2], an additional output current feedback scheme is proposed to achieve the required virtual impedance at hth harmonic frequency, where the measurement of output current is necessary. Therefore, to avoid using additional measurements, the linear voltage compensator [6] written

Table 4.2: Parameters of the Controller

Symbol	Quantity	Value
k_c	Current proportional gain	8
k_v	Voltage proportional gain	0.05
ω_1	Fundamental angular frequency	$2\pi\cdot 50$ rad/s
ξ	Damping factor	0.01
k_1	Fundamental gain	1
k_3	Third harmonic gain	1
k_5	Fifth harmonic gain	1
k_7	Seventh harmonic gain	1
k_9	Ninth harmonic gain	1
k_{11}	Eleventh harmonic gain	1
k_{13}	Thirteenth harmonic gain	1

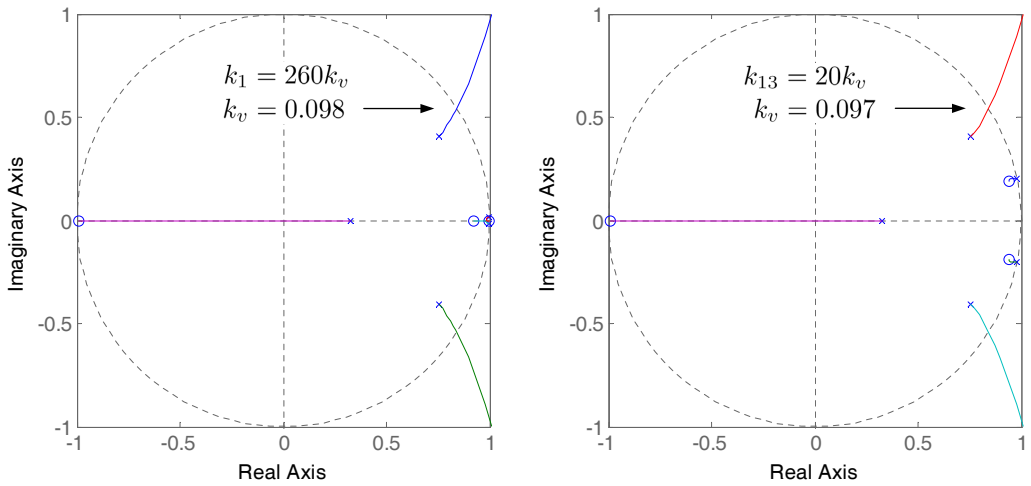
as

$$G_v(z) = k_v + \sum_{h=1,\text{odd}}^{13} k_h \frac{a_{zh}z^2 + b_{zh}z + c_{zh}}{A_{zh}z^2 + B_{zh}z + C_{zh}} \tag{4.31}$$

is used, with $A_{zh} = \frac{4}{T_s^2} + \frac{4\xi\omega_h}{T_s} + \omega_h^2$, $B_{zh} = -\frac{8}{T_s^2} + 2\omega_h^2, C_{zh} = \frac{4}{T_s^2} - \frac{4\xi\omega_h}{T_s} + \omega_h^2$, $a_{zh} = \frac{4\xi\omega_h}{T_s}$, $b_{zh} = 0$ and $c_{zh} = -\frac{4\xi\omega_h}{T_s}$. The respective continuous equivalent voltage compensator is

$$G_v(s) = k_v + \sum_{h=1,\text{odd}}^{13} k_h \frac{2\xi\omega_h s}{s^2 + 2\xi\omega_h s + \omega_h^2}. \tag{4.32}$$

It can be approximated from (4.27) that the output impedance at hth harmonic frequency is comprised of two parts in parallel, i.e. $\frac{k_c}{k_v k_c+1}$ and $\frac{1}{k_h}$. Compared to the classic PR compensator ($h_{3,\text{odd}} = 0$), the proposed linear voltage compensator has fixed the impedance at each harmonic frequency (less than 13th). The advantage of choosing a small k_v is that the output impedance in the low frequency range is large. With a large output impedance in the low frequency range, it has good suppression of low frequency and dc current circulating in the parallel inverters. On the other hand, at hth harmonic frequencies, the output impedance magnitude is approximately equal to $\frac{1}{k_h}$, which can be adjusted according to the requirement. The most important parameters of the linear voltage compensator are ξ and k_h. Again, the stability condition should be satisfied first. As is shown in (4.31), the absolute values of a_{zh} and c_{zh} are almost $\xi\omega_h T_s$ times greater than the absolute values of A_{zh} and C_{zh}. If the value of $k_h\xi\omega_h T_s$ is much smaller than k_v, proportional gain is more dominant for stability condition. Normally, it is true that $k_h\xi\omega_h T_s \ll k_v$. Fig. 4.7 shows the root loci of voltage loop when resonant compensators are used with the proportional compensator. When the additional compensator resonates at fundamental frequency, the root loci are



(a) (b)

Figure 4.7: Root loci of the external voltage loop when resonant compensators are used. (a) Proportional compensator plus fundamental frequency resonant compensator. (b) Proportional compensator plus thirteenth harmonic frequency resonant compensator.

derived by increasing k_v while maintaining $k_1 = 260k_v$. When the additional compensator resonates at 13th harmonic frequency, the root loci are derived by maintaining $k_{13} = 20k_v$. With $\xi = 0.01$ [30], in both cases $k_h\xi\omega_h T_s = 0.041k_v$ is satisfied. It can be seen from Fig. 4.7(a) and (b) that the stability boundaries are reduced to $k_v < 0.098$ and $k_v < 0.097$, respectively. However, it can be seen that in practice with relative small resonant gains, the proportional gain is the most important factor for stability. Note that the harmonic resonant frequency can not approach the sampling frequency. If a very high ω_h is required, the relevant gain k_h should be reduced to maintain the stability. The frequency domain response with different k_h, ξ and ω_h has been studied in [48] for compensators design. These results can also be used for the design of the resonant compensators. A bigger ξ results in a wider passband, but there is a trade off between passband and stability. A bigger k_h results in higher tracking capability and lower output impedance, but the sharing accuracy will decline if the cable impedance is large. Usually, k_h is chosen according to the output power level. When the system is designed for high output current, k_h should be big and although the circular current increases, it is small compared to the high output current. On the contrary, if the system is operating in low power level, k_h should be relatively small to suppress the circular current. Although the output impedance is then increased, such small output current results in acceptable voltage droop and distortion. With properly adjusted k_h and k_v according to the output power level, a good trade off of current sharing and output voltage quality can be achieved.

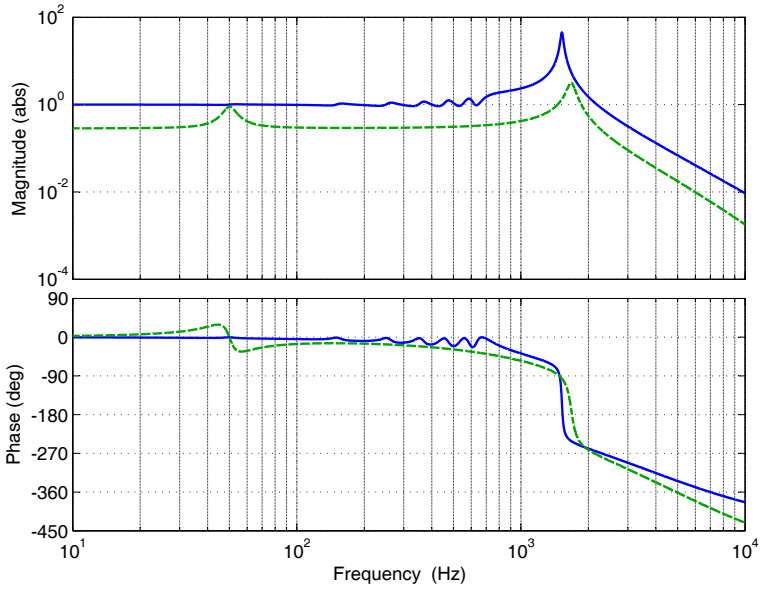


Figure 4.8: Bode diagram of closed-loop transfer function (full line: linear voltage control scheme with duty-ratio feedforward; dashed line: classic PR control scheme).

The control parameters are chosen as listed in Table 4.2. Fig. 4.8 and Fig. 4.9 show the Bode diagrams of the closed-loop transfer function and the output impedance, respectively. It can be seen from Fig. 4.8 that as a relative small resonant gain ($k_1 = 20k_v$) is used, the gain of the closed-loop transfer function at the fundamental frequency for the classic PR control scheme is close to unity ($|G(j\omega_1)| = 0.89$). However, there is a large phase error when the frequency varies around the fundamental frequency, which will be increased by higher resonant gains. In contrast, by using the proposed linear voltage control scheme with duty-ratio feedforward, the gain of the closed-loop transfer function is unity ($|G(j\omega_1)| = 1.0$) and the phase error around the fundamental frequency is close to zero, achieving good tracking performance. On the other hand, the feedforward does not affect the system stability, since the structure of the feedback loop is not changed by the feedforward.

The output impedance Bode diagram (see Fig. 4.9) shows that the classic PR compensator has a resistive output impedance with magnitude close to $\frac{1}{k_1} = 1.0$ at the fundamental frequency. However, the magnitude of the output impedance at other harmonic frequencies is close to $\frac{k_c}{k_v k_c + 1} = 5.7$. In contrast, the output impedance magnitude of the proposed linear voltage compensator at each harmonic frequency is almost equal to $\frac{1}{k_h} = 1.0$. With a relative large value of k_h, the output voltage distortion can be suppressed by the linear voltage compensator.

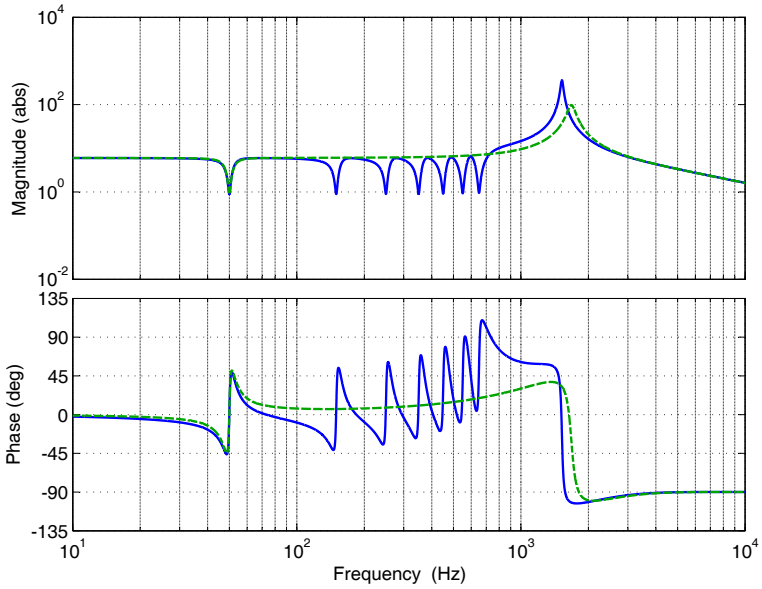


Figure 4.9: Bode diagram of output impedance (full line: linear voltage control scheme with duty-ratio feedforward; dashed line: classic PR control scheme).

4.3.3 Sensitivities

In practical parallel inverter systems, there are small differences between the parameters for each module. Normally, the drivers, switches and digital signal processors have negligible difference, the main difference usually comes from measurements and filters. By using calibrated ADC, the measurements deviations can be eliminated. However, the parameters of the filters are fixed and the differences cannot be eliminated. Then, a good controller means, by using this controller in each inverter, the parameters differences between different modules are negligible in the power sharing point of view. Since there is no additional droop control, the sensitivities of the closed-loop transfer function and output impedance versus filter parameters should be reduced. The sensitivities versus the capacitance of the LC filter are not of interest since the capacitors poles are connected in parallel through short cables to the PCC. These capacitors can be considered as a lumped capacitor. Therefore, the sensitivities versus the inductance and the parasitic resistance of the filter determine the sharing accuracy. By using the proposed linear voltage compensator with duty-ratio feedforward, the sensitivity of the closed-loop transfer function versus the inductance and the parasitic

resistance is

$$\frac{\partial G(s)}{\partial(sL+r_L)} = -\frac{sC(G_{vp}(s)G_{cp}(s)+G_{ffp}(s))V_{dc}G_{PWM}(s)}{(s^2LC+sC(G_{cp}(s)V_{dc}G_{PWM}(s)+r_L)+G_{vp}(s)G_{cp}(s)V_{dc}G_{PWM}(s)+1)^2}. \tag{4.33}$$

On the other hand, the sensitivity of the output impedance versus the inductance and the parasitic resistance is

$$\frac{\partial Z(s)}{\partial(sL+r_L)} = -\frac{G_{vp}(s)G_{cp}(s)V_{dc}G_{PWM}(s)+1}{(s^2LC+sC(G_{cp}(s)V_{dc}G_{PWM}(s)+r_L)+G_{vp}(s)G_{cp}(s)V_{dc}G_{PWM}(s)+1)^2}. \tag{4.34}$$

It can be seen from (4.33) and (4.34) that at any harmonic frequency, when higher gain of $G_v(j\omega_h)k_c$ is achieved, the sensitivities of the closed-loop transfer function and the output impedance will be significantly reduced. Fig. 4.10 and Fig. 4.11 show the Bode diagrams of the closed-loop transfer function and the output impedance with filter parameters in two cases, respectively. When a large difference exists in filter parameters (case 1: $L = 1642$ μH and $r_L = 0.4$ Ω; case 2: $L = 2100$ μH and $r_L = 1$ Ω), the gains of the closed-loop transfer function at the fundamental frequency are almost identical (see Fig. 4.10). Although the output impedances have magnitude difference (see Fig. 4.11), this difference does not affect the sharing performance too much (error is less than 10%). Since the linear voltage compensator achieves high gains at resonant frequencies, the filter parameters discordance can be neglected from sharing accuracy point of view.

4.4 Simulation results

The simulation of parallel inverters controlled by classic PR controller and by the proposed controller is performed in MATLAB/Simulink environment. The power circuit of the inverters is built by PLECS components, as is shown in Fig. 4.12. There is one nonlinear load consisting a diode bridge, a capacitor in parallel with a resistive load connected to the PCC. The load resistance is 27 Ω. The whole digitally controlled system comprised of two parallel inverters is shown in Fig. 4.13. The yellow block in Fig. 4.13 is the subsystem which contains the circuit of Fig. 4.12. The controllers in the simulation are expressed in z-domain according to the experimental system.

The sharing performances achieved by the classic PR controller with droop method and the proposed controller are compared. Two inverters commanded

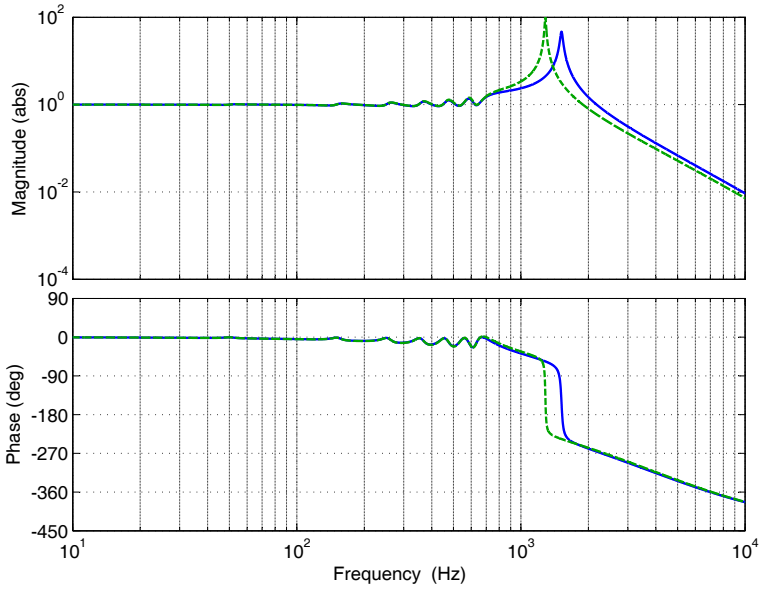


Figure 4.10: Sensitivities of the closed-loop transfer function versus filter parameters (full line: case 1; dashed line: case 2).

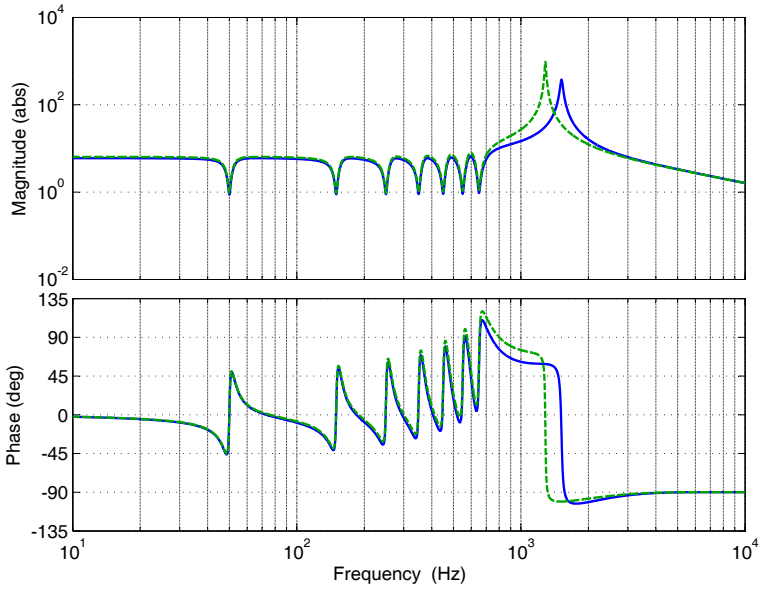


Figure 4.11: Sensitivities of the output impedance versus filter parameters (full line: case 1; dashed line: case 2).

by 115 V reference voltage are connected in parallel. The circuit parameters in Table 4.1 are used. The resistance of the resistive load is 27 Ω. The voltage references of the two inverters are synchronized. The line impedances of Inverter 1 and Inverter 2 are 0.171 Ω and 0.147 Ω, respectively.

The simulated waveforms of the classic PR controller with a droop method are shown in Fig. 4.14. The parameters in Table 4.2 are used, without harmonic

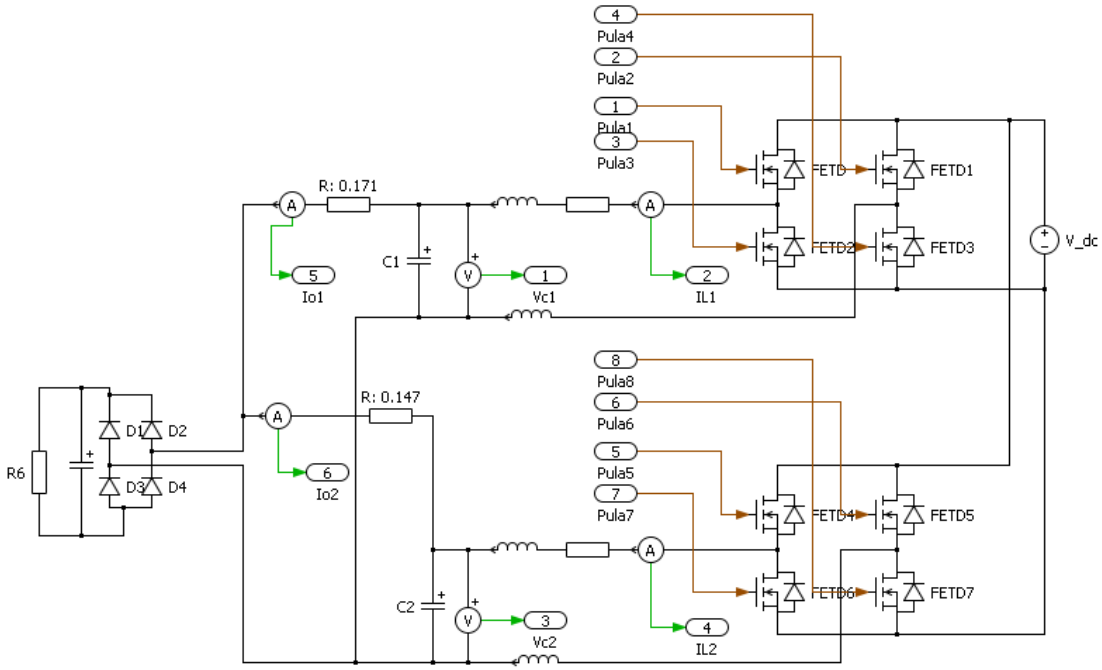


Figure 4.12: Simulink block diagram of the power circuit of two parallel inverters.

compensators and feedforward. The droop method of $P - V$ droop and $Q - \phi$ boost is used [2], with the droop coefficient and boost coefficient of 1×10^{-5} and 1×10^{-4}, respectively.

Although the current sharing (3.6 A) is good when linear loads are connected (see Fig. 4.14(a)), the output voltage amplitude is only 99 V. When a nonlinear load is connected, the output voltage is severely distorted (Fig. 4.14(b) and (c)). The calculated results of output voltage THD when a nonlinear load is connected (Fig. 4.14(b) and (c)) show that the output voltage has much higher distortion compared to the results when only linear loads are connected (Fig. 4.14(a)). When a linear load and a nonlinear load are connected, the THD is 2.9%. When one nonlinear load is connected, the THD is 3.1%. The output voltage distortion is not well suppressed by the classic PR controller without additional compensation.

To obtain a fair comparison between the two control schemes, the same parameters listed in Table 4.2 are used for the proposed controller. The simulation retrieved output currents and voltage waveforms of the proposed control scheme are shown in Fig. 4.15. The output currents of the two inverters are clearly equal (3.9 A) with linear loads connected. Moreover, the output voltage is pure sinusoidal and the RMS value is 111 V (see Fig. 4.15(a)). When a nonlinear load is connected, the output voltage is distorted (Fig. 4.15(b) and (c)) due to the existence of the line impedances and output impedances. When a linear load and a nonlinear load are connected, the output voltage THD is 1.2%. When a nonlinear

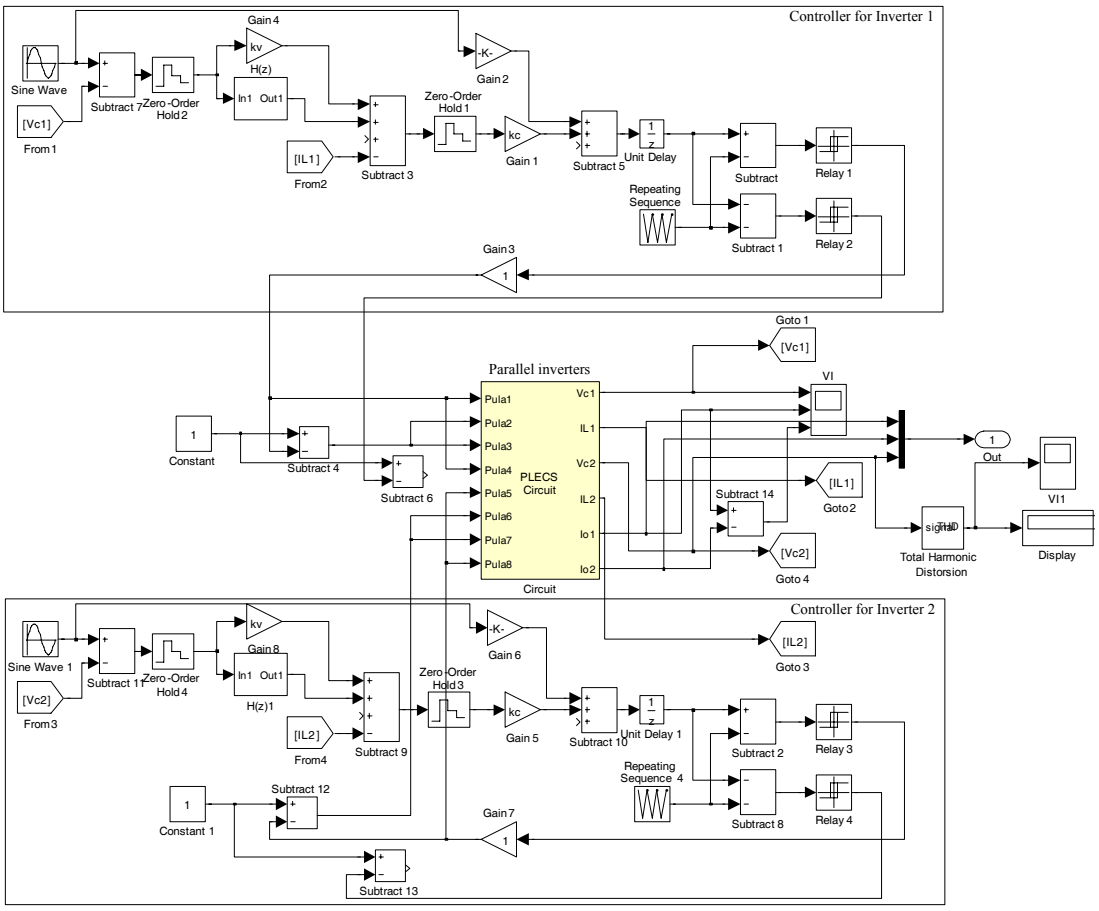


Figure 4.13: Simulink block diagram of two digitally controlled inverters in parallel.

load is connected, the THD is 1.4%. A comparison of the simulated performance of the two control schemes is summarized in Table 4.3. It can be seen that in an environment with a highly distorted output current, the proposed linear voltage control scheme with duty-ratio feedforward is more capable of providing a better voltage tracking capability and a lower output voltage distortion.

4.5 Experimental results

The sharing performance is experimentally evaluated by two 115 V, 1 kW inverters connected in parallel. The circuit parameters in Table 4.1 are used. The experimental setup of the parallel inverters system is shown in Fig. 4.16. Two inverters are synchronized to the grid and connected to the common loads through HO5VV-F cables. The resistances of the cables of Inverter 1 and Inverter 2 are 0.071 Ω and 0.047 Ω, respectively. The inductances of the cables are negligible (less than 0.1 μH). The inductors parameters of Inverter 1 and Inverter 2 are

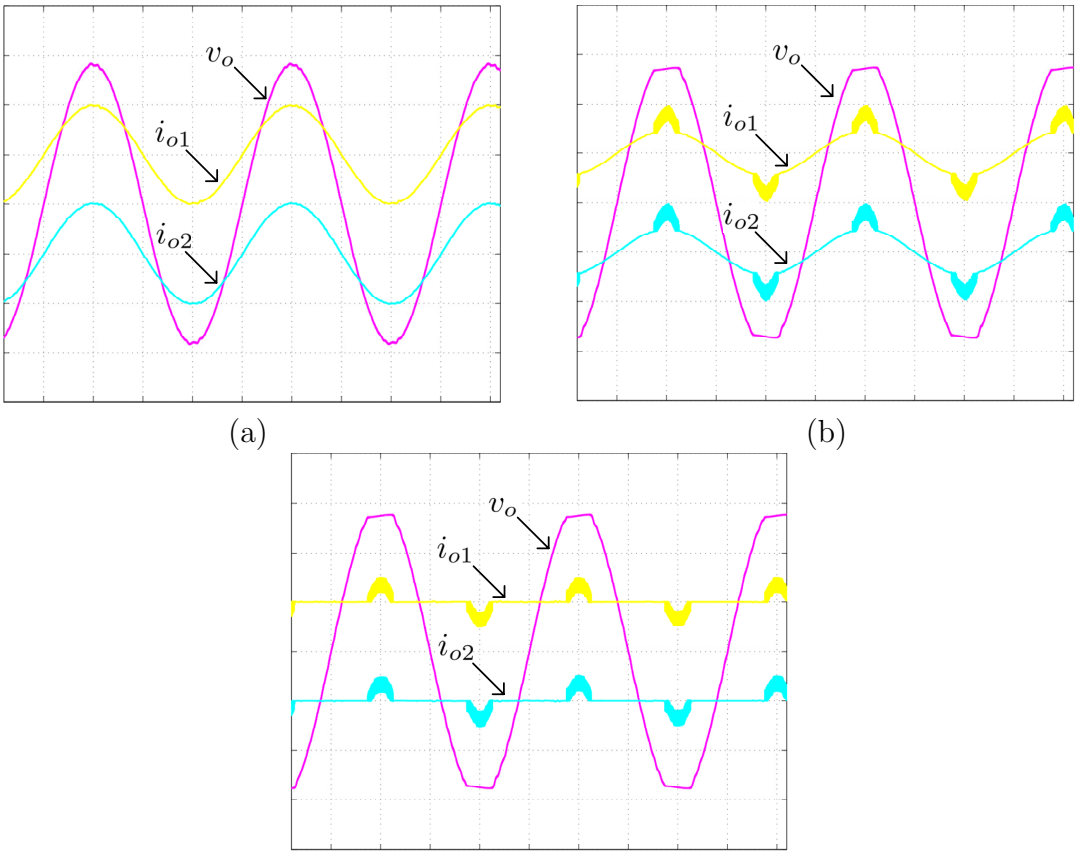


Figure 4.14: Simulated output voltage and currents of the two parallel inverters with the PR and droop controller (X–axis: Time, 5 ms/div; Y–axis: Magnitude of output currents and voltage; output currents, 5 A/div; output voltage, 50 V/div). (a) Linear loads. (b) Linear load and nonlinear load. (c) Nonlinear load.

$L_1 = 1632$ μH (and $r_{L1} = 0.38$ Ω) and $L_2 = 1623$ μH (and $r_{L2} = 0.39$ Ω), respectively. The filter capacitances are $C_1 = 10.3$ μF and $C_2 = 10.2$ μF, respectively. Due to the experimental condition, the output currents are measured by two shunt resistors (with $r_{sh1,2} = 0.1$ Ω, $\pm 1\%$ resistance tolerance). The oscilloscope is Tektronix TDS 2014B with 4 non-isolated channels.

The control method is implemented using two TMS320F28335 from Texas Instruments. The H bridges of the buck inverters are Mitsubishi IPM. The switches are driven indirectly via optical couplers and the deadband time is 2.67 μs. The symmetric-on-time modulator is used and the duty-ratio is updated at each sampling instant. The measurements are calibrated from power circuit side to ADC side. By producing a group of reference dc current or voltage signals on measurements input $(x_1, x_2, ..., x_n)$, there are a group of digital output values from the ADC $(y_1, y_2, ..., y_n)$. In our case, $n = 8$ and the measured data of the two inverters are shown in Table 4.4 and Table 4.5. For example, the first column of

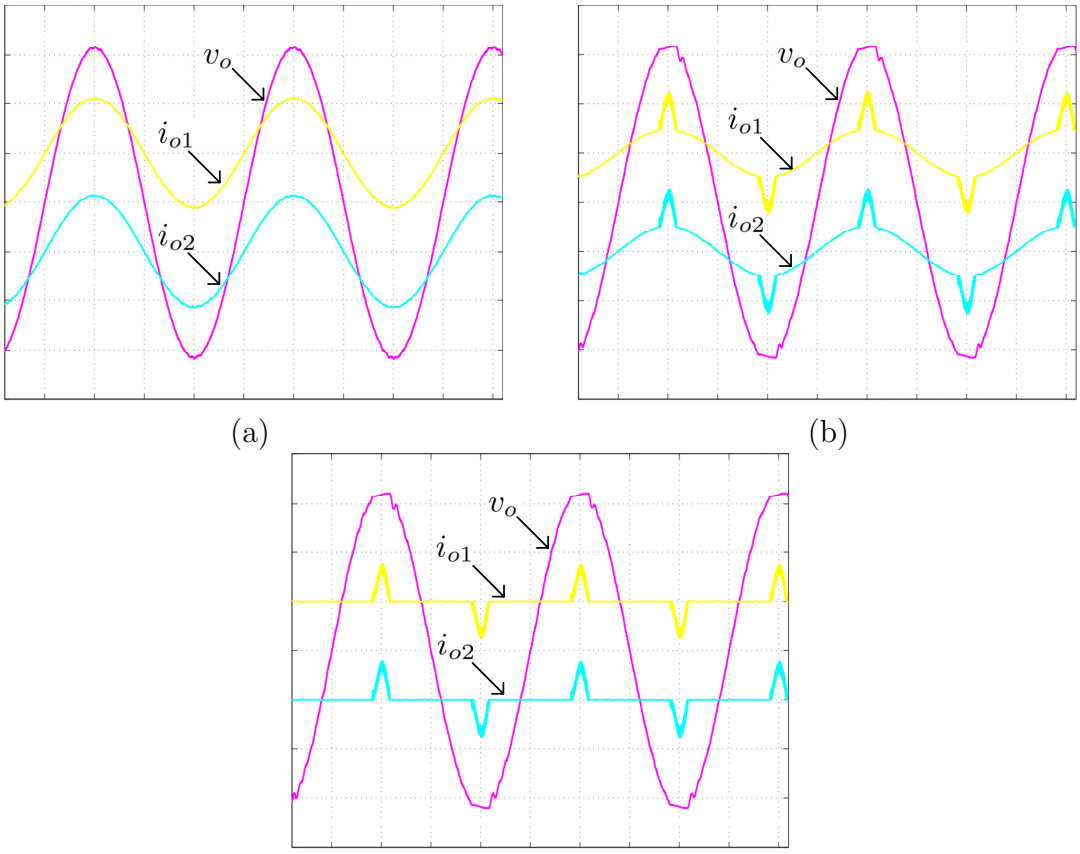


Figure 4.15: Simulated output voltage and currents of the two parallel inverters with the proposed controller (X–axis: Time, 5 ms/div; Y–axis: Magnitude of output currents and voltage; output currents, 5 A/div; output voltage, 50 V/div). (a) Linear loads. (b) Linear load and nonlinear load. (c) Nonlinear load.

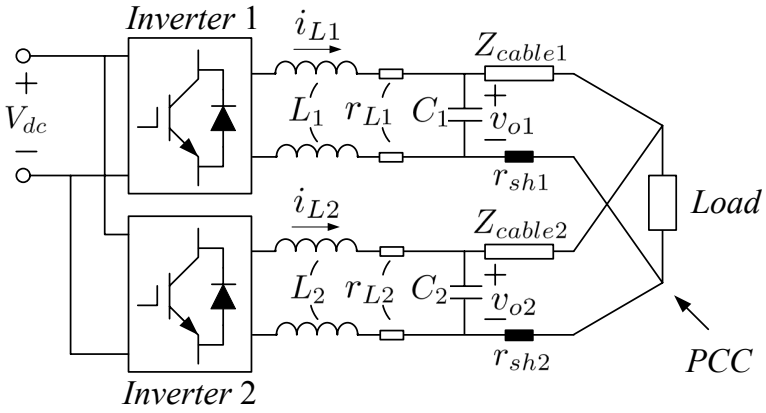


Figure 4.16: Schematic of the experimental setup of the parallel inverters system.

Table 4.4 represents the current values provided from a power source, while the second column adjacent to it represents the value read from the relevant memory of DSP. When the linear combination of polynomial basis functions is used, these

Table 4.3: Simulated Output Performance Comparison of the Classic Controller and the Proposed Controller

	Load(s)	Classic controller	Proposed controller
Current RMS	Linear	3.6 A	3.9 A
Voltage RMS	Linear	99 V	111 V
Voltage THD	Linear	0.7%	0.5%
	Linear and nonlinear	2.9%	1.2%
	Nonlinear	3.1%	1.4%

Table 4.4: Measured Data for Calibration of Inverter 1

I_L (Source)	I_L (DSP)	I_g (Source)	I_g (DSP)	V_c (Source)	V_c (DSP)	V_g (Source)	V_g (DSP)
6.00 A	473.1	6.00 A	508.1	160.1 V	3848.4	161.0 V	3863.6
4.50 A	860.3	4.50 A	884.0	129.3 V	3499.7	120.7 V	3400.3
3.00 A	1246.6	3.00 A	1260.4	84.3 V	2988.6	80.6 V	2939.3
1.50 A	1636.1	1.50 A	1638.2	41.6 V	2501.9	40.6 V	2480.6
0.00 A	2025.2	0.00 A	2016.8	0.00 V	2028.2	0.00 V	2015.1
−1.50 A	2411.6	−1.50 A	2394.3	−41.1 V	1559.5	−40.5 V	1551.4
−3.00 A	2797.7	−3.00 A	2770.3	−84.0 V	1072.2	−80.1 V	1096.8
−4.50 A	3184.2	−4.50 A	3146.5	−129.4 V	555.1	−120.2 V	636.6
−6.00 A	3569.6	−6.00 A	3522.6	−160.1 V	206.7	−161.1 V	166.5

overdetermined equations related to the ADC output values and real circuit values are solved with least square method. For an analog current or voltage value of x, the measured digital value of ADC is y. The required linear function is assumed to be $p(y) = \beta_1 y + \beta_0$, where the result of $p(y)$ should approach the value of x. Define $\mathbf{x} = (x_1, x_2, \cdots, x_n)^{\mathrm{T}}$, $\boldsymbol{\beta} = (\beta_1, \beta_0)^{\mathrm{T}}$, $\mathbf{y} = (y_1, y_2, \cdots, y_n)^{\mathrm{T}}$ and

$$\mathbf{M} = \begin{bmatrix} y_1 & y_2 & \cdots & y_n \\ 1 & 1 & \cdots & 1 \end{bmatrix}. \tag{4.35}$$

The coefficients β_1 and β_0 are related to the overdetermined equation $\mathbf{M}^{\mathrm{T}}\boldsymbol{\beta} = \mathbf{x}$. However, β_1 and β_0 can be solved by the least square method

$$\boldsymbol{\beta} = (\mathbf{M}\mathbf{M}^{\mathrm{T}})^{-1}\mathbf{M}\mathbf{x}. \tag{4.36}$$

The calibration has been accomplished with the measured data in Table 4.4 and Table 4.5. Based on Equation (4.36), the coefficients of the linear functions are obtained. The numerical results for coefficients of Inverter 1 and 2 are shown in Table 4.6 and Table 4.7, respectively. These coefficients are fixed and used for inverters with other applications in the following chapters.

The experimental waveforms and the relevant fast Fourier transform (FFT) results of the classic PR controller with droop method are shown in Fig. 4.17 and

Table 4.5: Measured Data for Calibration of Inverter 2

I_L (Source)	I_L (DSP)	I_g (Source)	I_g (DSP)	V_c (Source)	V_c (DSP)	V_g (Source)	V_g (DSP)
6.00 A	519.3	6.00 A	518.0	161.0 V	3846.3	160.5 V	3880.7
4.50 A	896.3	4.50 A	896.5	129.4 V	3509.9	120.2 V	3419.5
3.00 A	1275.7	3.00 A	1276.2	84.2 V	2997.5	80.9 V	2970.0
1.50 A	1655.0	1.50 A	1655.5	41.3 V	2512.3	40.7 V	2513.6
0.00 A	2037.7	0.00 A	2037.0	0.00 V	2046.4	0.00 V	2047.8
−1.50 A	2418.1	−1.50 A	2418.7	−41.2 V	1581.8	−40.3 V	1585.0
−3.00 A	2797.7	−3.00 A	2799.7	−84.2 V	1095.5	−80.6 V	1123.8
−4.50 A	3175.6	−4.50 A	3179.0	−129.5 V	582.9	−120.1 V	672.0
−6.00 A	3552.9	−6.00 A	3558.4	−160.1 V	237.2	−161.0 V	203.8

Table 4.6: Coefficients of Calibration for Inverter 1

	I_L	I_g	V_c	V_g
β_1	−0.0038734	−0.0039785	0.087883	0.087153
β_0	7.8348	8.0195	−178.23	−175.65

Table 4.7: Coefficients of Calibration for Inverter 2

	I_L	I_g	V_c	V_g
β_1	−0.0039509	−0.0039440	0.088729	0.087443
β_0	8.0460	8.0366	−181.40	−178.90

Fig. 4.18, respectively. The parameters in Table 4.2 are used, without harmonic compensators and feedforward. Since changing operating frequency may result in a poor resonant control performance, the droop method of $P-V$ droop and $Q-\phi$ boost is used [2], with the droop coefficient and boost coefficient of 1×10^{-5} and 1×10^{-4}, respectively. Although the current sharing (3.6 A) is good when linear loads are connected (see Fig. 4.17(a)), the output voltage amplitude is only 99 V. When a nonlinear load is connected, the output voltage is severely distorted (Fig. 4.17(b) and (c)). The FFT results of the output voltage when a nonlinear load is connected (Fig. 4.18(b) and (c)) show that the output voltage has much higher distortion compared to the results when only linear loads are connected (Fig. 4.18(a)). The distortion on the output voltage also affects the output current waveforms. When a linear load and a nonlinear load are connected, the calculated output voltage THD result is 2.9%. When one nonlinear load is connected, the THD is 5.3%. Note that the maximum THD 5% limit is established by the international regulations [11]. The output voltage distortion is not well suppressed by the classic controller without additional compensation.

To obtain a relatively fair comparison between the two control schemes, the same parameters listed in Table 4.2 are used for the proposed controller. The experimental output currents and voltage waveforms of the proposed control scheme are shown in Fig. 4.19. The relevant output voltage FFT results are shown in Fig. 4.20. The output currents of the two inverters are clearly equal (3.9 A) with linear loads connected. Moreover, the output voltage is pure sinusoidal and the RMS value is 112 V (see Fig. 4.19(a)). When a nonlinear load is connected, the output voltage is distorted (Fig. 4.19(b) and (c)) due to the existence of the line impedances and output impedances. However, with properly designed output impedance, the distortion can be suppressed under acceptable tolerance. When a linear load and a nonlinear load are connected, the output voltage THD is 1.2%. When a nonlinear load is connected, the THD is 1.5%. A comparison of the experimentally measured performance of the two control schemes is summarized in Table 4.8. It can be seen that in an environment with a highly distorted output current, output voltage distortion is inevitable. However, compared to the classic PR controller, the proposed linear voltage control scheme with duty-ratio feedforward is more capable of providing a better voltage tracking capability and lower output voltage distortion to improve the output voltage quality. Comparing the simulation results with the experimental results, it can be seen that they are almost in accordance. These results confirm the advantages of the proposed control scheme in load sharing performance.

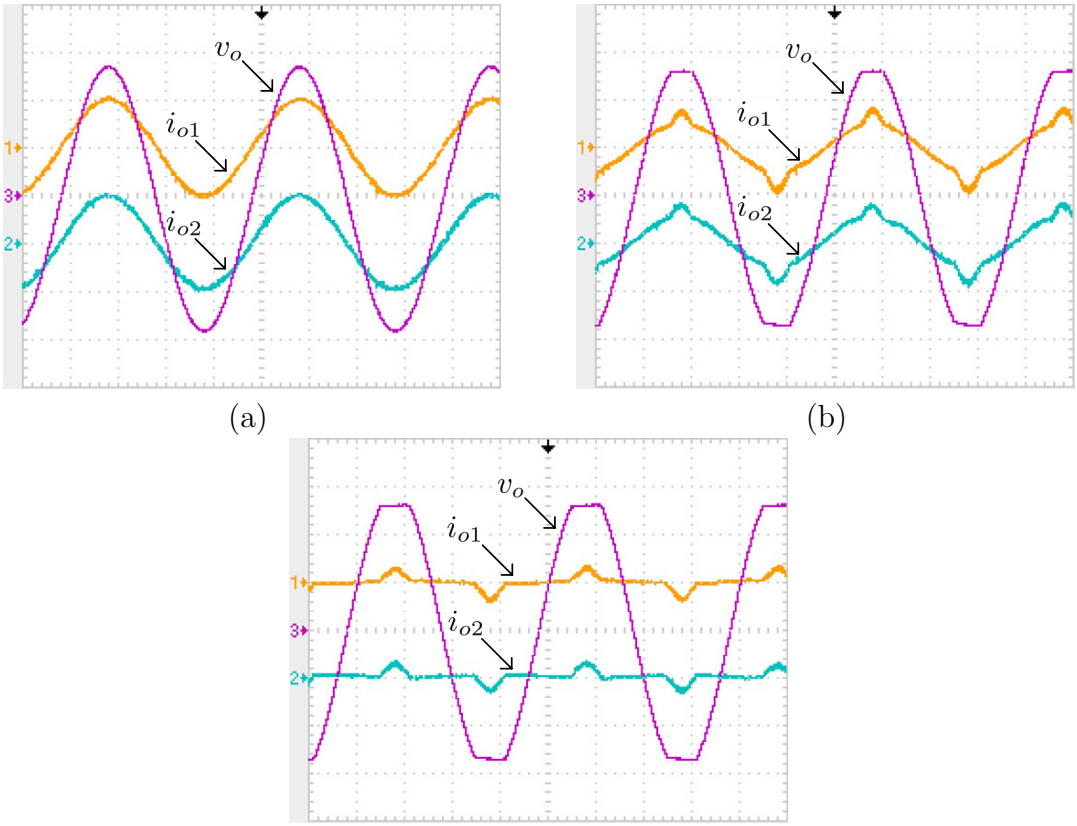


Figure 4.17: Experimental output voltage and currents of the two parallel inverters with the PR and droop controller (X–axis: Time, 5 ms/div; Y–axis: Magnitude of output currents and voltage; Channel 1: output current of Inverter 1, 5 A/div; Channel 2: output current of Inverter 2, 5 A/div; Channel 3: output voltage, 50 V/div). (a) Linear loads. (b) Linear load and nonlinear load. (c) Nonlinear load.

4.6 Conclusion

For parallel inverters connected through short cables, high sharing accuracy can be achieved by using a properly designed controller without droop control. The design of the controller is very important. In digitally controlled inverters, the internal current loop proportional gain is limited by the filter inductance and the sampling frequency, while the external voltage loop proportional gain is also limited by stability conditions. To improve the sharing accuracy and voltage quality, the control scheme of the linear voltage compensator with duty-ratio feedforward is used. The theoretical analysis shows that the closed-loop transfer function using the proposed control scheme remains unity gain over a wide frequency range. Compared to a classic PR control scheme, the closed-loop transfer function of the proposed control scheme has better voltage tracking performance and less phase error around the fundamental frequency. The virtual output impedance

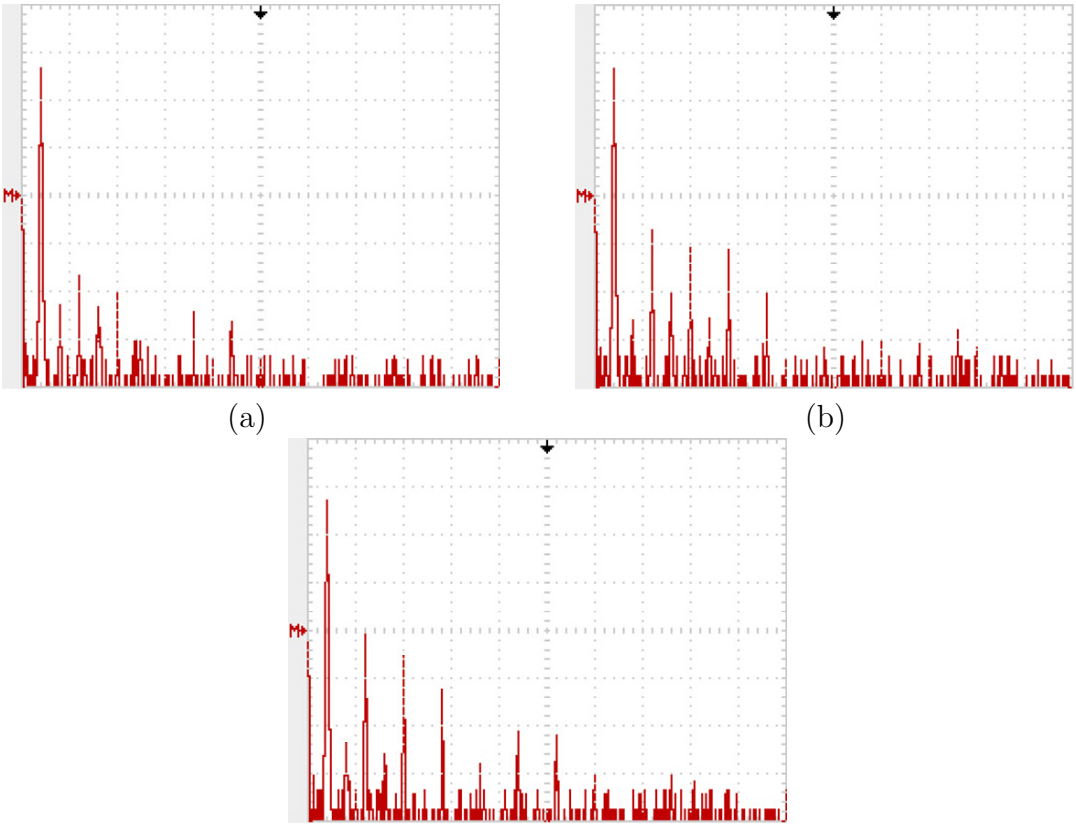


Figure 4.18: Experimental output voltage FFT results of the two parallel inverters with the PR and droop controller (X–axis: Frequency, 125 Hz/div; Y–axis: Magnitude, 10 dB/div; Window: Flattop). (a) Linear loads. (b) Linear load and nonlinear load. (c) Nonlinear load.

resonated at harmonic frequencies suppresses the harmonic distortion when nonlinear loads are connected. The simulation and experimental comparison between the proposed control scheme and the classic PR control scheme reveals the main features of the parallel inverters using the linear voltage compensator with duty-ratio feedforward: i.e., good sharing accuracy, better voltage tracking capability and lower THD of the output voltage.

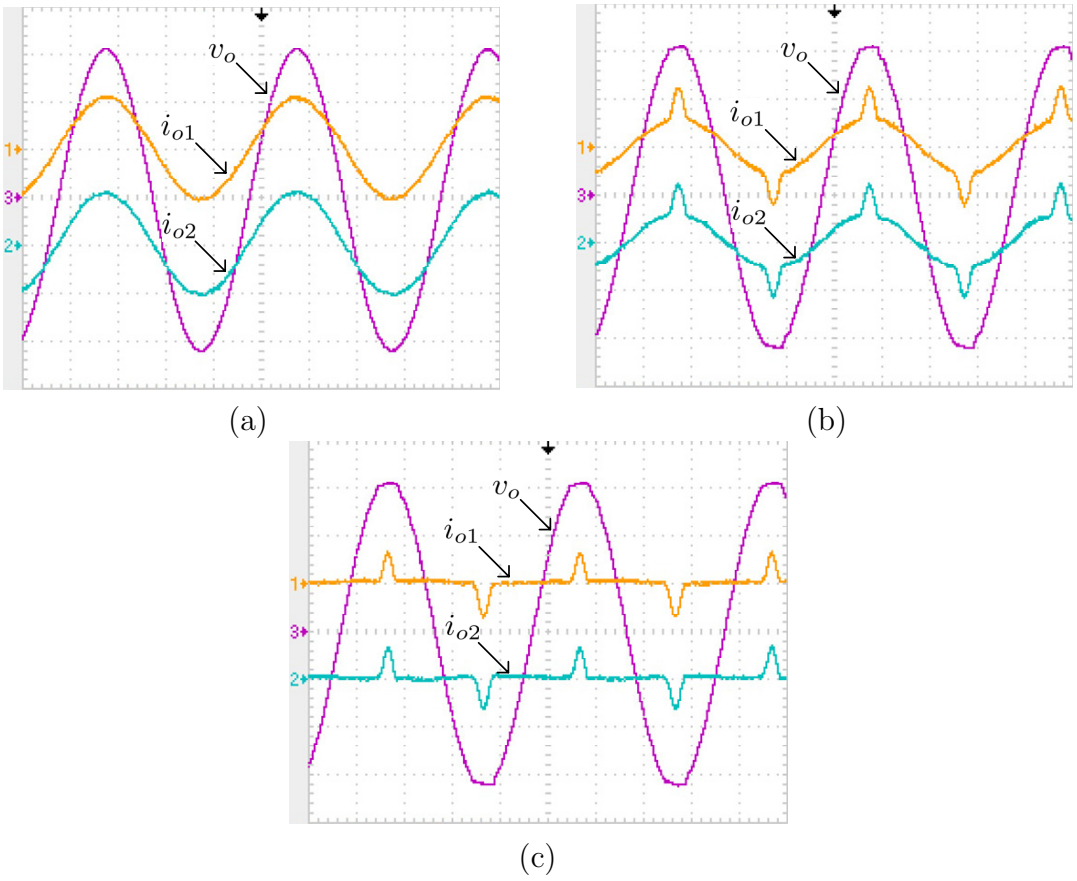


Figure 4.19: Experimental output voltage and currents of the two parallel inverters with the proposed controller (X–axis: Time, 5 ms/div; Y–axis: Magnitude of output currents and voltage; Channel 1: output current of Inverter 1, 5 A/div; Channel 2: output current of Inverter 2, 5 A/div; Channel 3: output voltage, 50 V/div). (a) Linear loads. (b) Linear load and nonlinear load. (c) Nonlinear load.

Table 4.8: Experimental output Performance Comparison of the Classic Controller and the Proposed Controller

	Load(s)	Classic controller	Proposed controller
Current RMS	Linear	3.6 A	3.9 A
Voltage RMS	Linear	99 V	112 V
Voltage THD	Linear	1.0%	0.6%
	Linear and nonlinear	2.9%	1.2%
	Nonlinear	5.3%	1.5%

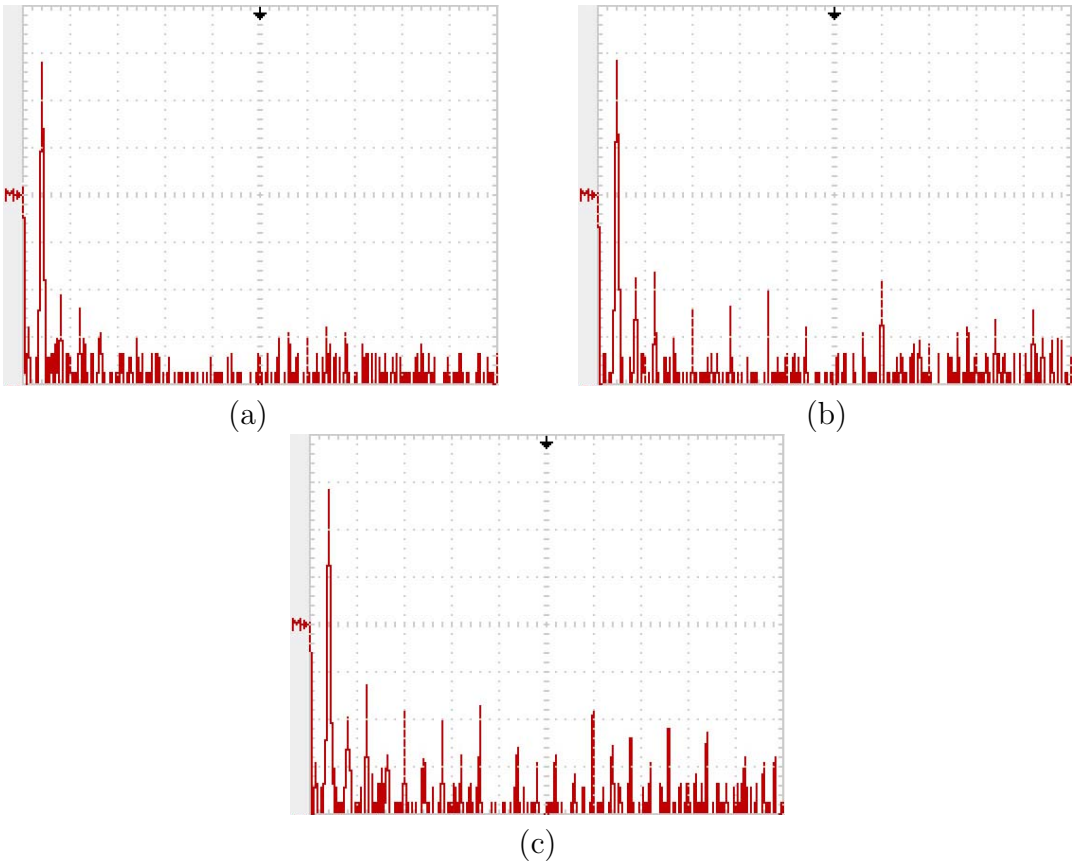


Figure 4.20: Experimental output voltage FFT results of the two parallel inverters with the proposed controller (X–axis: Frequency, 125 Hz/div; Y–axis: Magnitude, 10 dB/div; Window: Flattop). (a) Linear loads. (b) Linear load and nonlinear load. (c) Nonlinear load.

Chapter 5

Modelling of Digitally Controlled Grid-Connected Inverters with LCL Filters

5.1 Introduction

Voltage source converters (VSCs) with LCL filters are widely used in many grid-connected applications such as PWM rectifiers [29, 62], uninterruptible power supplies (UPSs) [61, 63] and photovoltaic (PV) inverters [60, 35, 30, 48, 64, 65, 66] for the advantages of power factor controllability and bidirectional energy supply capability. Compared to L filters, LCL filters employ much smaller size and lower cost inductors. There is a good chance that the LCL filters will be employed for all the grid-connected inverters in the future [67]. The design for the parameters of the LCL filter has already been addressed [29]. However, the controller design is still the issue: the LCL filter resonance has to be carefully taken into account to maintain the system stability.

As the price/performance ratio of DSPs is decreasing dramatically, there is the trend towards using entire digital control in high power switching converters. Using floating-point DSPs embedding high resolution fast ADCs and enhanced PWM generators, the application of more complicated control algorithms becomes feasible. Moreover, although the signals measured from the power circuits contain considerable disturbance around switching instants, sampling algorithms can be used to guarantee an average current reproduction with the rejection of switching ripple and noise [47, 49].

Fig. 5.1 shows a typical circuit diagram of a digitally controlled grid-connected inverter with an LCL filter. The analog variables (usually the converter current i_L, the grid current i_g and the grid voltage v_g) are converted into digital quantities via appropriate measurement circuits and ADCs. The process of converting signals into the specified range of ADCs can be ideally represented by scaling

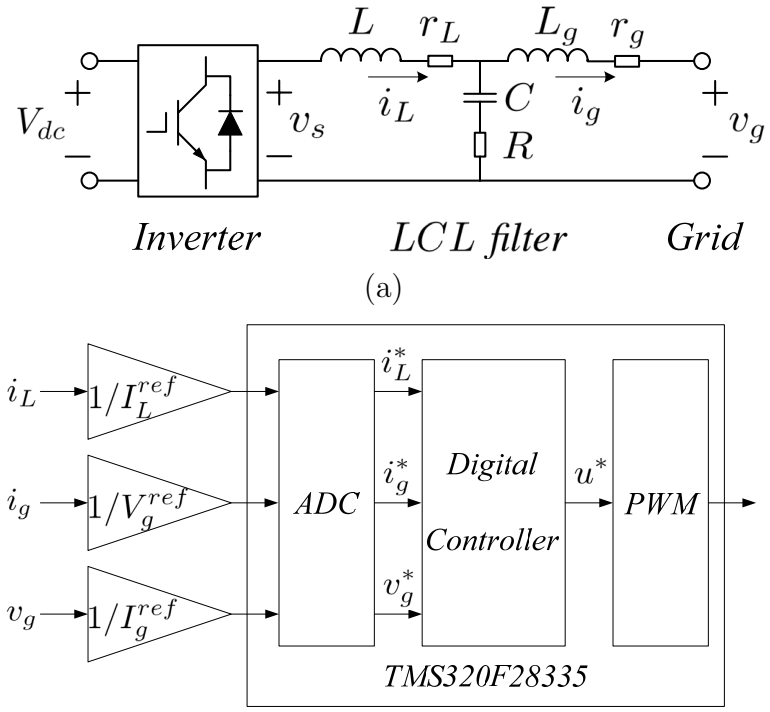


Figure 5.1: Single phase inverter. (a) Power circuit. (b) Control circuit.

factors ($1/I_L^{ref}$, $1/V_g^{ref}$ and $1/I_g^{ref}$) [28]. To avoid the erroneously sampled value in the vicinity of the switching instant, the conversion of ADC is started when the PWM counters reach to zero or period values [49]. The digital quantities (i_L^*, i_g^* and v_g^*) converted from ADCs are scaled to be numerically equivalent to the relevant analog variables. By using a digital control algorithm, the duty-ratio is calculated and updated into the PWM controller (represented as u^*) to generate the drive signals.

The design of a digital controller and evaluation of the control performance for grid-connected inverters are usually implemented by using classic average models. In average models, the transfer function of the PWM is represented by an unity gain with half or one switching cycle delay [32, 35, 62, 66]. In a more precise model, the AD conversion delay, the computation delay, the PWM delay and the transport delay are modeled together as a total delay [25]. However, a practical digital system using synchronous sampling method has complex behaviours with different delay effects [50]. The duty-ratio update modes may result in different delay effects. Therefore, an accurate model including delay effects should first take account of the processing delay and the duty-ratio update delay, after which the switching delay and transport delay can be modeled.

With properly modeled delay effects, the new small-signal z-domain models can be derived for digitally controlled grid-connected inverters with single control

loop and cascaded control loops. The classic s-domain models accurately represent the interested control performance which is around the grid fundamental frequency and low order harmonic frequencies. However, for stability analysis, using s-domain models will lead to erroneous results. The maximum proportional gains which are only attainable in z-domain analysis are limited in sampled-data systems. With proposed z-domain models, the design of the digital controllers can be implemented. These models are capable of predicting the steady-state and transient responses for control variables at sampling instants, which are validated by the relevant simulation and experimental tests.

5.2 Classic average models for grid-connected inverters

In classic average models, the power circuit is modeled by s-domain transfer functions using an averaged switch voltage. The control circuit, although implemented digitally, is represented by continuous equivalent transfer functions. There are plenty of control structures for the grid-connected inverters with LCL filters [30, 35, 36, 37, 48, 60, 66, 67, 68, 69]. However, in this chapter two typical control structures are provided as shown in Fig. 5.2. The first, (see Fig. 5.2(a)), is the converter current feedback scheme [30, 70, 71]. The second, (see Fig. 5.2(b)), is the converter current plus grid current feedback scheme [72], which is a typical controller with cascaded control loops. Although many papers use the converter current plus capacitor current feedback scheme [37, 60, 69], this strategy is equivalent to the converter current plus grid current feedback scheme from the dynamic point of view. Both controllers have the same total delay (processing delay and PWM delay) from the command signal to drive signals, which is expressed as $G_d(s) = e^{-s\tau_d}$. The delay effect with three typical values for τ_d can be used, i.e., with $\tau_d = T_s/2$ defined as the minimum delay, with $\tau_d = T_s$ defined as the medium delay and with $\tau_d = 3T_s/2$ defined as the maximum delay. Regardless of the carrier waveshape and the delay of PWM, the switch voltage in the average model is represented by $v_s = V_{dc}d$. Duty-ratio feedforward (expressed as $d_{ff} = v_g/V_{dc}$) is included [28]. In order to model the two control structures, the classic PR compensator (represented by $G_c(s)$) and the proportional compensator (represented by k_L) are used as examples. However, the modelling methods in this chapter are also applicable when other types of controllers are used.

Define the following as $f_a = LL_gC$, $f_b = C(L_g(R + r_L) + L(R + r_g))$, $f_c = L + L_g + C(r_Lr_g + Rr_L + Rr_g)$ and $f_d = r_L + r_g$. The transfer functions describing the converter current i_L and the grid current i_g as a function of the switch voltage

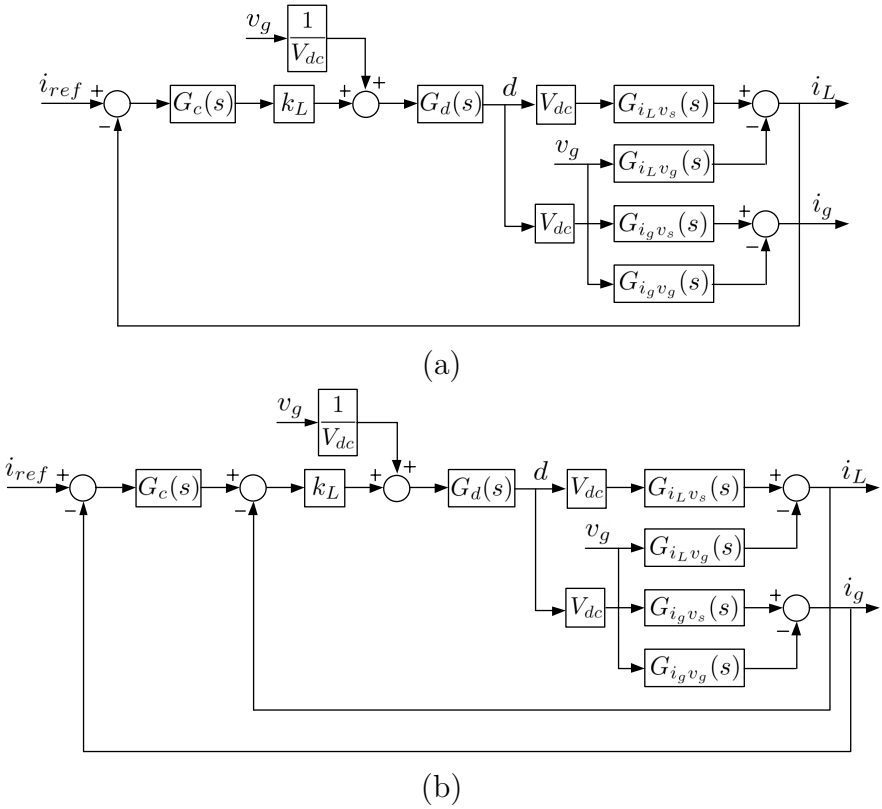


Figure 5.2: The s-domain block diagrams of grid-connected inverters. (a) Converter current feedback scheme. (b) Converter current plus grid current feedback scheme.

v_s are given by

$$G_{i_L v_s}(s) = \frac{s^2 L_g C + sC(R + r_g) + 1}{s^3 f_a + s^2 f_b + s f_c + f_d} \tag{5.1}$$

and

$$G_{i_g v_s}(s) = \frac{sCR + 1}{s^3 f_a + s^2 f_b + s f_c + f_d} \tag{5.2}$$

respectively. The transfer functions describing i_L and i_g as a function of the grid voltage v_g are expressed as

$$G_{i_L v_g}(s) = \frac{sCR + 1}{s^3 f_a + s^2 f_b + s f_c + f_d} \tag{5.3}$$

and

$$G_{i_g v_g}(s) = \frac{s^2 LC + sC(R + r_L) + 1}{s^3 f_a + s^2 f_b + s f_c + f_d} \tag{5.4}$$

respectively.

The closed-loop transfer function $\frac{i_g(s)}{i_{ref}(s)}$ and the grid voltage to grid current transfer function $\frac{i_g(s)}{v_g(s)}$ of the converter current feedback scheme are written as

$$G_{cl1}(s) = \frac{G_c(s) k_L G_d(s) V_{dc} G_{i_g v_s}(s)}{1 + G_c(s) k_L G_d(s) V_{dc} G_{i_L v_s}(s)} \tag{5.5}$$

Table 5.1: Parameters of the Grid-Connected Inverters

Symbol	Quantity	Value
V_{dc}	Input voltage amplitude	200 V
V_g	Grid voltage RMS value	110 V
T_s	Sampling period	50 μs
ω_1	Fundamental angular frequency	$2\pi\cdot 50$ rad/s
L	Converter side Inductor	1642 μH
r_L	Converter side inductor parasitic resistance	0.4 Ω
C	Capacitor	10 μF
L_g	Grid side Inductor	1642 μH
r_g	Grid side inductor parasitic resistance	0.4 Ω
k_L	Proportional gain	0.08
k_p	PR compensator proportional gain	0.5
k_r	PR compensator resonant gain	40
ξ	Damping factor	0.01

and

$$G_{gd1}(s) = \frac{1 + G_c(s)k_L V_{dc} G_{i_L v_g}(s)}{1 + G_c(s)k_L G_d(s) V_{dc} G_{i_L v_s}(s)} G_d(s) G_{i_g v_s}(s) - G_{i_g v_g}(s) \tag{5.6}$$

respectively.

The closed-loop transfer function describing i_g as a function of i_{ref} and the transfer function describing i_g as a function of v_g of the converter current plus grid current feedback scheme are given by

$$G_{cl2}(s) = \frac{G_c(s)k_L G_d(s) V_{dc} G_{i_g v_s}(s)}{1 + k_L G_d(s) V_{dc} G_{i_L v_s}(s) + G_c(s)k_L G_d(s) V_{dc} G_{i_g v_s}(s)} \tag{5.7}$$

and

$$G_{gd2}(s) = \frac{(1 + k_L V_{dc} G_{i_L v_g}(s)) G_d(s) G_{i_g v_s}(s) - (1 + k_L G_d(s) V_{dc} G_{i_L v_s}(s)) G_{i_g v_g}(s)}{1 + k_L G_d(s) V_{dc} G_{i_L v_s}(s) + G_c(s)k_L G_d(s) V_{dc} G_{i_g v_s}(s)} \tag{5.8}$$

respectively.

For a classic PR compensator[1], the transfer function can be expressed as

$$G_c(s) = k_p(1 + k_r \frac{2\xi\omega_1 s}{s^2 + 2\xi\omega_1 s + \omega_1^2}) \tag{5.9}$$

in s-domain. When there is no damping resistor, by using the parameters in Table 5.1 and first order Padé approximations of $e^{sT_s} = \frac{1+sT_s/2}{1-sT_s/2}$ [73] for $G_d(s)$ with the maximum delay, the Bode diagrams of the closed-loop transfer functions $G_{cl1}(s)$ and $G_{cl2}(s)$ are shown in Fig. 5.3. The Bode diagrams of the grid voltage

[1]In practice, the compensators resonating at harmonic frequencies are also included to suppress the current THD. In order to achieve a better performance while maintaining the stability, the respective gains for the harmonic compensators are reduced when the resonant frequency increases.

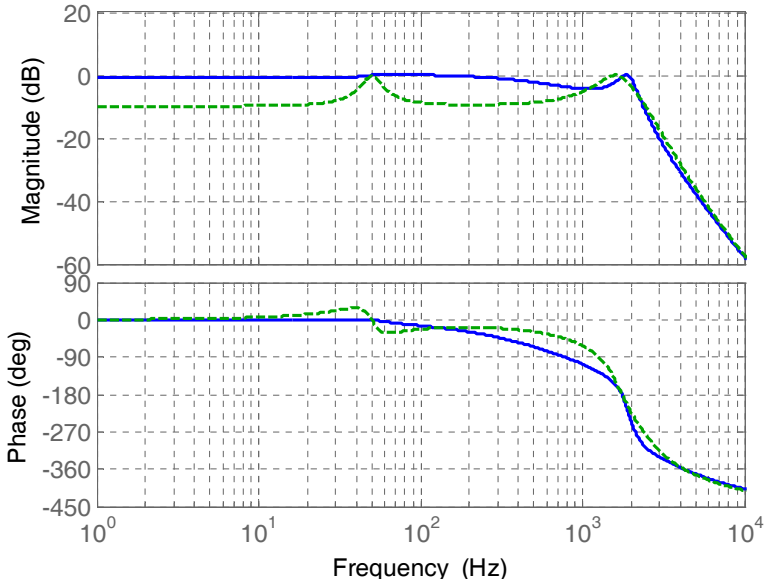
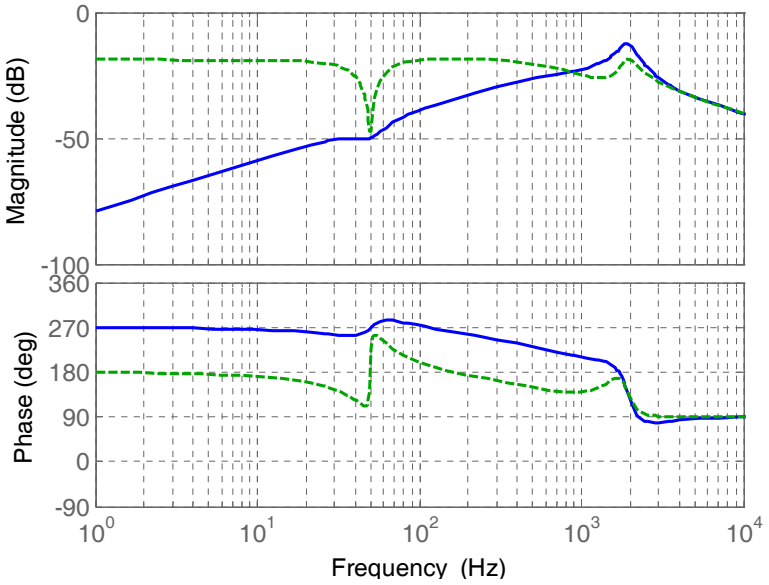


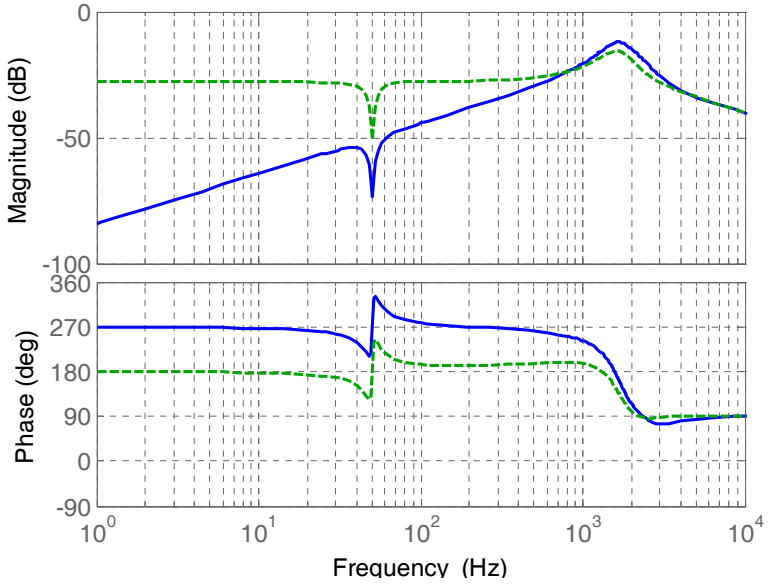
Figure 5.3: Bode diagrams of closed-loop transfer functions from i_{ref} to i_g (full line: converter current feedback control scheme; dashed line: converter current plus grid current control scheme).

to grid current transfer functions $G_{gd1}(s)$ and $G_{gd2}(s)$ in the converter current feedback scheme and in the converter current plus grid current feedback scheme are shown in Fig. 5.4.

The Bode diagrams of the closed-loop transfer functions show that the converter current control scheme has an unity closed-loop gain ($G(j\omega_1) = 1.0$) at the fundamental frequency. If the grid frequency deviates slightly from the nominal fundamental frequency (within ± 1 Hz), the closed-loop gain is almost constant and the phase error is zero. When the converter current plus grid current control scheme is applied, the closed-loop gain ($G(j\omega_1) = 0.95$) at the fundamental frequency approaching unity is achieved by the high gain of the resonant compensator. The phase error in this control scheme is considerable when the grid frequency varies (see Fig. 5.3). The converter current control scheme achieves a faster dynamic response since it has higher gain over a wide frequency range. On the other hand, the Bode diagrams in Fig. 5.4(a) shows that even when duty-ratio feedforward is applied, the grid voltage has considerable disturbance on the grid current. When the filter capacitance increases, the current error becomes bigger. However, the converter current plus grid current control scheme with duty-ratio feedforward has a relative good suppression on the grid voltage disturbance (see Fig. 5.4(b)). Both of the two control schemes are possible solutions for practical implementation. The control performance around the fundamental frequency and low order harmonic frequencies can be studied using s-domain models with good accuracy, but the instabilities with high oscillatory frequencies can not be pre-



(a)



(b)

Figure 5.4: Bode diagrams of the grid voltage to grid current transfer functions (full line: with duty-ratio feedforward; dashed line: without duty-ratio feedforward). (a) Converter current feedback control scheme. (b) Converter current plus grid current feedback control scheme.

cisely predicted. The root loci of the average models for the two control schemes are shown in Fig. 5.5 and Fig. 5.6. These root loci give the stability boundaries under different delay conditions. In the next section, the root loci of z-domain models will also be obtained to predict the stability boundaries. The z-domain models will be derived, which allows a full comparison between the classic models and the proposed models.

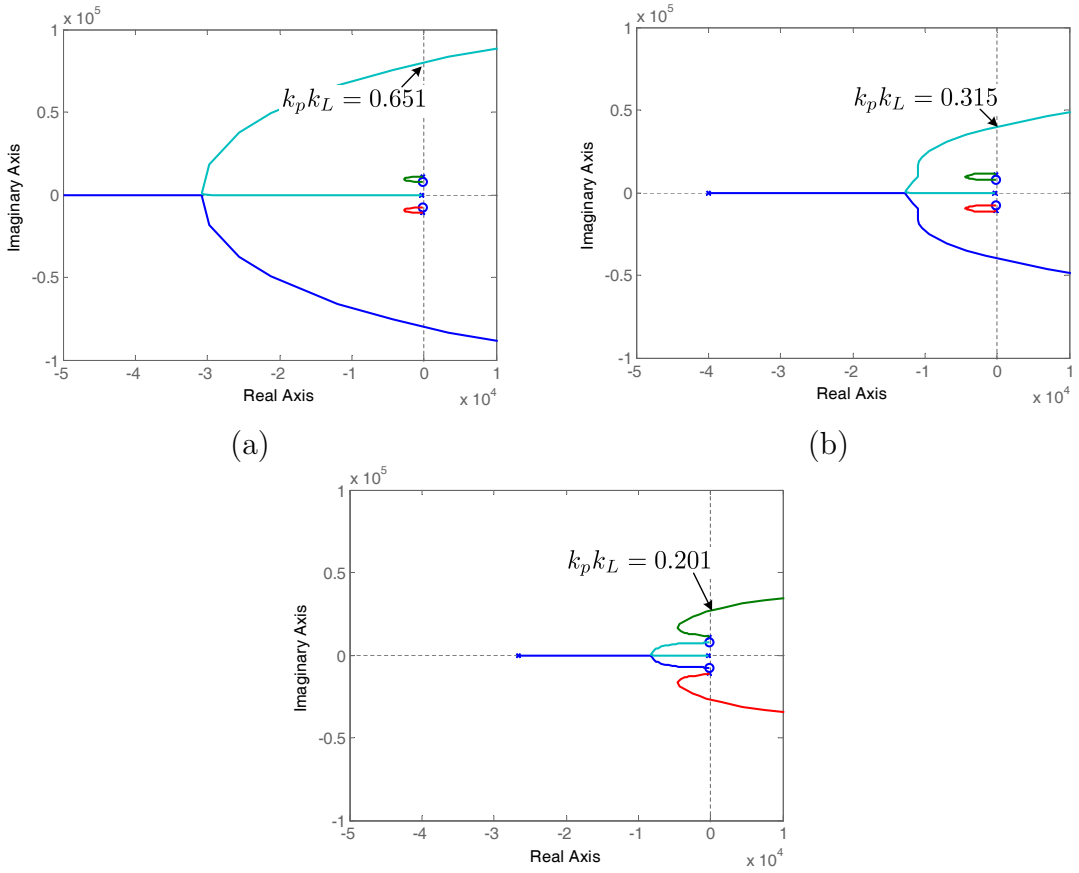


Figure 5.5: Root loci of the converter current feedback controlled grid-connected inverters in s-plane . (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

5.3 Small-signal z-domain models for digitally controlled grid-connected inverters

For digitally controlled grid-connected inverters, the two feedback control schemes are studied in z-domain. The converter current feedback scheme is a commonly used control strategy in switching converters. The z-domain model in [25] is extended for this third-order system. The converter current plus grid current feedback scheme, which is used in the control of grid-connected inverters, is a typical structure with converter current control in cascaded control loops. The z-domain model for the cascaded digital control loops is derived in this chapter as the modelling method in [25] is not directly applicable. Since the analysis is implemented with small-signal models, the transfer functions in this section represent the behaviour when signals have small excursions to their steady-state values.

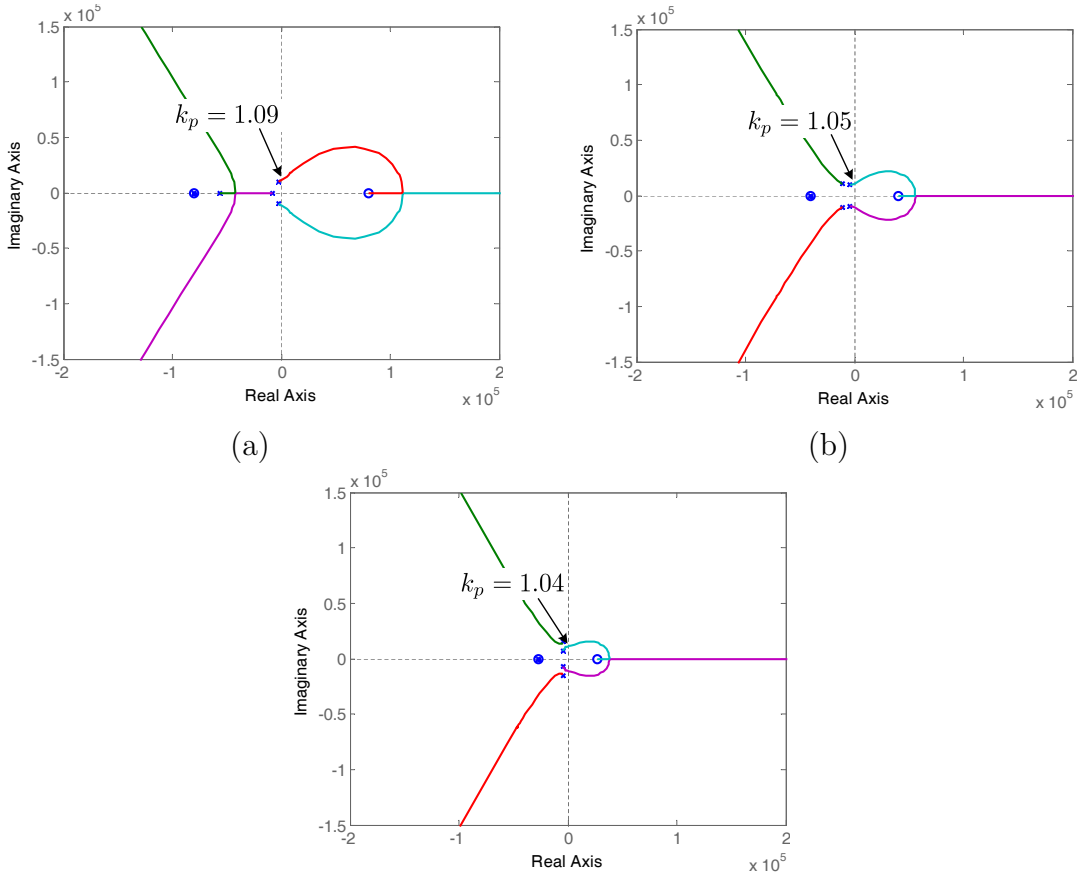


Figure 5.6: Root loci of the converter current plus grid current feedback controlled grid-connected inverters in s-plane with $k_L = 0.08$. (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

5.3.1 Discrete models for grid-connected inverters

As the gain of the delay e^{-sT_s} is almost unity at the fundamental frequency ($e^{-j\omega_1 T_s} \approx 1$), the continuous-time models can be used to investigate the control performance in low frequency range. However, in order to design digital controllers, discrete models are required. To simplify the analysis, the disturbances of grid voltage are removed from the models without affecting the closed-loop transfer functions. Hence, by modelling the digital processing delay τ_{d1} and τ_{d2} into the PWM, the block diagrams of the digitally controlled grid-connected inverters can be precisely represented in Fig. 5.7, where $\tau_{\triangle}$ is the total time delay of the switches drive, signals transport and measurements. Compared to the digital PWM delay, this delay is negligible.

If a classic PR compensator is used for control, the digitalized compensator is represented as $G_c(z)$ in z-domain [30]. Usually, $G_c(z)$ is derived as the discrete equivalent of $G_c(s)$ in Fig. 5.3 by using bilinear transform. For the PR

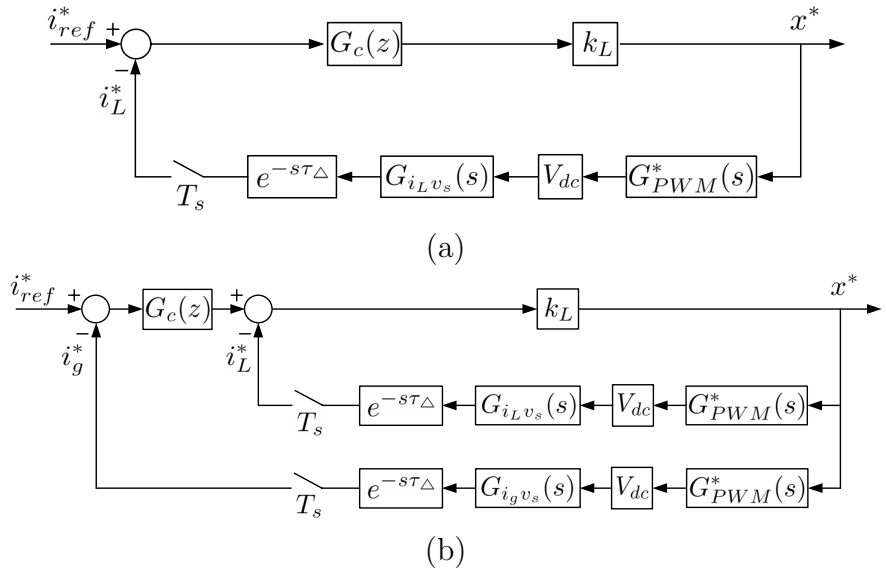


Figure 5.7: Block diagrams of grid-connected inverters. (a) Converter current feedback scheme. (b) Converter current plus grid current feedback scheme.

compensator $G_c(s)$ in s-domain, its discrete equivalent $G_c(z)$ is written as

$$G_c(z) = k_p(1 + k_r \frac{a_{z1}z^2 + b_{z1}z + c_{z1}}{A_{z1}z^2 + B_{z1}z + C_{z1}}), \tag{5.10}$$

with $A_{z1} = \frac{4}{T_s^2} + \frac{4\xi\omega_1}{T_s} + \omega_1^2$, $B_{z1} = -\frac{8}{T_s^2} + 2\omega_1^2, C_{z1} = \frac{4}{T_s^2} - \frac{4\xi\omega_1}{T_s} + \omega_1^2$, $a_{z1} = \frac{4\xi\omega_1}{T_s}$, $b_{z1} = 0$ and $c_{z1} = -\frac{4\xi\omega_1}{T_s}$.

To obtain the closed-loop discrete transfer functions of the two control structures, the feedback paths in Fig. 5.7 should be represented in z-domain. Hence, z-transform is used to obtain discrete transfer functions of the feedback paths which contain continuous plants followed by ideal samplers. The discrete transfer functions describing $\widehat{i}^*_L$ and $\widehat{i}^*_g$ as a function of $\widehat{x}^*$ in small signal are derived as

$$G_{i_L x}(z) = \mathcal{Z}\{G^*_{PWM}(s)V_{dc}G_{i_L v_s}(s)e^{-s\tau_\triangle}\} \tag{5.11}$$

and

$$G_{i_g x}(z) = \mathcal{Z}\{G^*_{PWM}(s)V_{dc}G_{i_g v_s}(s)e^{-s\tau_\triangle}\}, \tag{5.12}$$

respectively. The exact expressions of transfer functions $G_{i_L x}(z)$ and $G_{i_g x}(z)$ can be obtained by defining
$f_Q = \sqrt{(2f_b^3 - 9f_af_bf_c + 27f_a^2f_d)^2 - 4(f_b^2 - 3f_af_c)^3}$,
$f_C = \sqrt[3]{\frac{1}{2}(f_Q + 2f_b^3 - 9f_af_bf_c + 27f_a^2f_d)}$,
$a = \frac{f_b}{3f_a} + \frac{f_C}{3f_a} + \frac{(f_b^2 - 3f_af_c)}{3f_af_C}$,
$b = \frac{f_b}{3f_a} - \frac{(1+j\sqrt{3})f_C}{6f_a} - \frac{(1-j\sqrt{3})(f_b^2-3f_af_c)}{6f_af_C}$ and
$c = \frac{f_b}{3f_a} - \frac{(1-j\sqrt{3})f_C}{6f_a} - \frac{(1+j\sqrt{3})(f_b^2-3f_af_c)}{6f_af_C}$.

The transfer function $G_{i_L v_s}(s)$ can be split to

$$G_{i_L v_s}(s) = \frac{A_L}{s+a} + \frac{B_L}{s+b} + \frac{C_L}{s+c} \tag{5.13}$$

with $A_L = \frac{a^2 L_g C - aC(R+r_g)+1}{(a-b)(a-c)LL_gC}$, $B_L = \frac{b^2 L_g C - bC(R+r_g)+1}{(b-a)(b-c)LL_gC}$ and $C_L = \frac{c^2 L_g C - cC(R+r_g)+1}{(c-b)(c-a)LL_gC}$. For the PWM model with $G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}})$, the z-transform of $G_{i_L x}(z)$ can be deduced using the method as

$$Z\{G^*_{PWM}(s)V_{dc}\frac{A_L}{s+a}e^{-s\tau_\triangle}\} = \frac{V_{dc}T_s A_L}{2}\frac{e^{a(\tau_\triangle - \frac{1+D}{2}T_s)} + e^{a(\tau_\triangle - \frac{1-D}{2}T_s)}}{z^2 - e^{-aT_s}z}. \tag{5.14}$$

Defining
$e_a = \frac{1}{2}(e^{a(\tau_\triangle - \frac{1+D}{2}T_s)} + e^{a(\tau_\triangle - \frac{1-D}{2}T_s)})$,
$e_b = \frac{1}{2}(e^{b(\tau_\triangle - \frac{1+D}{2}T_s)} + e^{b(\tau_\triangle - \frac{1-D}{2}T_s)})$,
$e_c = \frac{1}{2}(e^{c(\tau_\triangle - \frac{1+D}{2}T_s)} + e^{c(\tau_\triangle - \frac{1-D}{2}T_s)})$,
$D_2 = -e^{-aT_s} - e^{-bT_s} - e^{-cT_s}$,
$D_1 = e^{-(a+b)T_s} + e^{-(b+c)T_s} + e^{-(a+c)T_s}$ and
$D_0 = -e^{-(a+b+c)T_s}$,
the discrete transfer function $G_{i_L x}(z)$ can be written as

$$G_{i_L x}(z) = \frac{N_{L2}z^2 + N_{L1}z + N_{L0}}{z^4 + D_2 z^3 + D_1 z^2 + D_0 z} \tag{5.15}$$

with
$N_{L2} = V_{dc}T_s(A_L e_a + B_L e_b + C_L e_c)$,
$N_{L1} = -V_{dc}T_s(A_L e_a(e^{-bT_s} + e^{-cT_s}) + B_L e_b(e^{-aT_s} + e^{-cT_s}) + C_L e_c(e^{-aT_s} + e^{-bT_s}))$
and
$N_{L0} = V_{dc}T_s(A_L e_a e^{-(b+c)T_s} + B_L e_b e^{-(a+c)T_s} + C_L e_c e^{-(a+b)T_s})$.

Similarly, the transfer function $G_{i_g v_s}(s)$ can be split to

$$G_{i_g v_s}(s) = \frac{A_g}{s+a} + \frac{B_g}{s+b} + \frac{C_g}{s+c} \tag{5.16}$$

with $A_g = \frac{1-aCR}{(a-b)(a-c)LL_gC}$, $B_g = \frac{1-bCR}{(b-a)(b-c)LL_gC}$ and $C_g = \frac{1-cCR}{(c-b)(c-a)LL_gC}$. Then the discrete transfer function $G_{i_g x}(z)$ can be written as

$$G_{i_g x}(z) = \frac{N_{g2}z^2 + N_{g1}z + N_{g0}}{z^4 + D_2 z^3 + D_1 z^2 + D_0 z} \tag{5.17}$$

with
$N_{g2} = V_{dc}T_s(A_g e_a + B_g e_b + C_g e_c)$,
$N_{g1} = -V_{dc}T_s(A_g e_a(e^{-bT_s} + e^{-cT_s}) + B_g e_b(e^{-aT_s} + e^{-cT_s}) + C_g e_c(e^{-aT_s} + e^{-bT_s}))$ and
$N_{g0} = V_{dc}T_s(A_g e_a e^{-(b+c)T_s} + B_g e_b e^{-(a+c)T_s} + C_g e_c e^{-(a+b)T_s})$.

With the discrete transfer functions of the feedback paths, the z-domain closed-loop transfer function $\frac{\widehat{i_g^*}(z)}{\widehat{i_{ref}^*}(z)}$ of the converter current feedback scheme can be obtained according to Fig. 5.7(a) as

$$G_{cl1}(z) = \frac{G_c(z)k_L G_{i_g x}(z)}{1 + G_c(z)k_L G_{i_L x}(z)}. \tag{5.18}$$

The closed-loop transfer function $\frac{\widehat{i_g^*}(z)}{\widehat{i_{ref}^*}(z)}$ in respect to Fig. 5.7(b) is written as

$$G_{cl2}(z) = \frac{G_c(z)k_L G_{i_g x}(z)}{1 + k_L G_{i_L x}(z) + G_c(z)k_L G_{i_g x}(z)}. \tag{5.19}$$

Using the same parameters listed in Table 5.1 and $D = 0.5$, the Bode diagrams of $G_{cl1}(z)$ and $G_{cl2}(z)$ are shown in Fig. 5.8. Comparing to the average models derived Bode diagrams in s-domain (see Fig. 5.3), it can be seen that in the low frequency range, s-domain models results and z-domain models results are almost identical. When the control performance is interested in the low frequency range, s-domain models can be used with good accuracy. However, s-domain models fail to describe the dynamic behaviours of the digitally controlled systems apart from low frequency range. z-domain models are necessary for dynamic performance analysis. When frequency response specifications are given, controllers design can be performed according to the z-domain models. For example, resonant peaks in the frequency domain can be directly measured from the Bode diagrams. Frequency response design can be implemented when required, according to the Bode plots of the z-domain transfer functions.

5.3.2 Stability analysis for internal current loop

As most digital control strategies involve an internal converter current control loop, the stability of the internal loop is studied first. A pure proportional feedback control in the internal loop is usually used to imitate the peak current control in naturally-sampled switching converters. Even if a PR or a PI control may be used in the internal loop, the proportional gains are most important for the stability issue [60]. Assuming that the voltage on the filter capacitor has a much slower dynamic behaviour compared to the PWM output, the small-signal transfer function from PWM output to converter current can be approximated by

$$P(s) = \frac{V_{dc}}{sL + r_L} e^{-s\tau_\triangle}. \tag{5.20}$$

The simplified control loop for the converter current regulator of a buck inverter is schematically represented in Fig. 5.9. The PWM model has three typical expressions, i.e.,

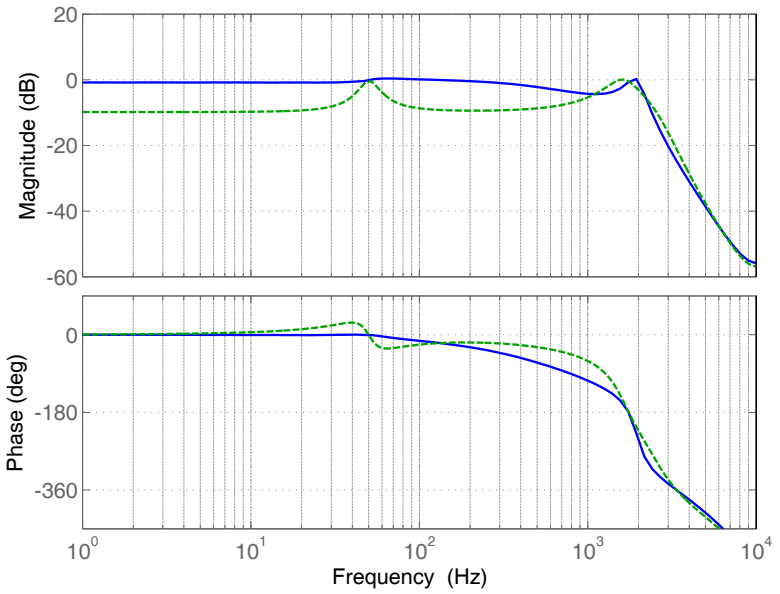


Figure 5.8: Bode diagrams of closed-loop transfer functions from i^*_{ref} to i^*_g with maximum delay (full line: converter current feedback control scheme; dashed line: converter current plus grid current control scheme).

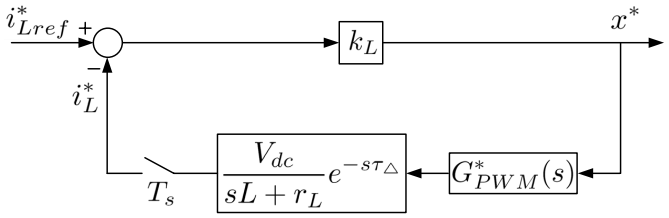


Figure 5.9: Block diagram for the simplified converter current control loop of a grid-connected inverter.

$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1-D)T_s}{2}} + e^{-s\frac{(1+D)T_s}{2}})$,
$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(1+D)T_s}{2}} + e^{-s\frac{(3-D)T_s}{2}})$ and
$G^*_{PWM}(s) = \frac{T_s}{2}(e^{-s\frac{(3-D)T_s}{2}} + e^{-s\frac{(3+D)T_s}{2}})$,
corresponding to the cases of minimum delay, medium delay and maximum delay, respectively. In the case of the minimum delay, the discrete transfer function from $\widehat{x}^*$ to $\widehat{i}^*_L$ is derived as

$$G_{i_Lx}(z) = \frac{V_{dc}T_s}{2L}\frac{e^{\frac{r_L}{L}(\tau_\triangle+\frac{-1-D}{2}T_s)} + e^{\frac{r_L}{L}(\tau_\triangle+\frac{-1+D}{2}T_s)}}{z - e^{-\frac{r_L}{L}T_s}}. \tag{5.21}$$

Similarly, in the cases of the medium delay and the maximum delay, $G_{i_Lx}(z)$ can be expressed as

$$G_{i_Lx}(z) = \frac{V_{dc}T_s}{2L}\frac{e^{\frac{r_L}{L}(\tau_\triangle+\frac{-1+D}{2}T_s)}z + e^{\frac{r_L}{L}(\tau_\triangle+\frac{-1-D}{2}T_s)}}{z^2 - e^{-\frac{r_L}{L}T_s}z} \tag{5.22}$$

and

$$G_{i_L x}(z) = \frac{V_{dc}T_s}{2L} \frac{e^{\frac{r_L}{L}(\tau_\triangle + \frac{-1-D}{2}T_s)} + e^{\frac{r_L}{L}(\tau_\triangle + \frac{-1+D}{2}T_s)}}{z^2 - e^{-\frac{r_L}{L}T_s}z}, \tag{5.23}$$

respectively. As $\frac{r_L T_s}{L} \ll 1$, the exponent terms in (5.21)–(5.23) can be approximated by 1. Hence, the pole of the converter current control loop with the minimum PWM delay can be derived by solving equation

$$z - 1 + \frac{k_L V_{dc} T_s}{L} = 0, \tag{5.24}$$

which gives the stable operating condition of

$$0 < k_L < \frac{2L}{V_{dc}T_s}. \tag{5.25}$$

Similarly, in the cases of medium and maximum delay, the characteristic equations are given by

$$z^2 + (\frac{k_L V_{dc} T_s}{2L} - 1)z + \frac{k_L V_{dc} T_s}{2L} = 0, \tag{5.26}$$

and

$$z^2 - z + \frac{k_L V_{dc} T_s}{L} = 0, \tag{5.27}$$

respectively, yielding the relevant stable operating conditions of

$$0 < k_L < \frac{2L}{V_{dc}T_s}, \tag{5.28}$$

and

$$0 < k_L < \frac{L}{V_{dc}T_s}, \tag{5.29}$$

respectively. Note that in the case of the maximum delay, the stable operating range of the proportional gain is dramatically reduced, resulting in a more limited achievable bandwidth. While designing controllers, the proportional gain for the converter current loop is usually chosen to be smaller than $\frac{L}{V_{dc}T_s}$. The similar result related to the gain setting in a digital proportional current regulator can also be found in [38].

5.3.3 Discrete root loci design

While designing a controller, a typical specification evaluating the robustness of a system is the gain margin in root locus. For digitally controlled grid-connected inverters, more precise stability boundaries can be obtained from discrete root loci. Based on root loci, the dynamic performance in time-domain (rise time, settling time and percent overshoot, etc.) can be evaluated according to the conjugate pole pairs in z-plane.

Using the same parameters listed in Table 5.1 and $D = 0.5$ (or any other values for D between 0 and 1), the root loci[2] of the converter current feedback controlled inverter are shown in Fig. 5.10. The real poles of the converter current feedback scheme with minimum and medium delay will move across the unit circle when the total proportional gain equals to 0.324 and 0.306 (see Fig. 5.10(a) and (b)), respectively. When the maximum delay is employed, the two conjugate poles will move across the unit circle when the proportional gain equals to 0.139 (see Fig. 5.10(c)). Even when the minimum delay is involved, a gain higher than 0.167 may result in a ringing dynamic response. Note that $\frac{2L}{V_{dc}T_s} = 0.328$. As is illustrated in the previous subsection, the internal current loop proportional gain is usually chosen to be much smaller than $\frac{L}{V_{dc}T_s}$. When $k_L = 0.08$ and $k_p = 0.5$ with the maximum delay, it can be seen from Fig. 5.10(c) that the closed-loop system still has a gain margin of 3.46. The longest settling time and the highest overshoot in percentage of the conjugate pole pairs are 3.1 ms and 68%, respectively.

The root loci of converter current plus grid current feedback controlled inverter are shown in Fig. 5.11. The conjugate poles in the cases of minimum delay, medium delay and maximum delay will move across the unit circle when the proportional gain k_p equals to 1.04, 1.04 and 1.02, respectively. These results are very dependent on the damping of the LCL resonance, for which an analytical expression is difficult to obtain. However, the PWM delay can reduce the stable operating range dramatically when the damping resistance increases. In this chapter where the maximum PWM delay is achieved in experiment, the proportional gain is chosen as $k_p = 0.5$. Hence, a stable gain margin of 2 is guaranteed[3].

5.4 Simulation Results

For safety issue reasons, computer simulations are used to verify the capability of the small-signal z-domain models in predicting stability boundaries. The power circuit of the grid-connected inverter is constructed in PLECS, as is shown in Fig. 5.12. Based on the power circuit of Fig. 5.12, the converter current controlled grid-connected inverter and the converter current plus grid current controlled

[2]The root loci are derived when using pure proportional compensators. However, under the condition of $k_r \ll \frac{1}{\xi\omega_1 T_s}$, the root loci in z-plane do not differ even if additional resonant compensators are used. The only difference introduced by the resonant compensators is that a pair of conjugate poles moving within the unit circle appears in the root loci.

[3]Though the discrete closed-loop transfer functions are average duty-ratio D dependent, the root loci are derived with duty-ratio fixed as $D = 0.5$. These results have very little difference when D is changing within $(0, 1)$. This conclusion is only valid when the symmetric triangle carriers are used for PWM generation.

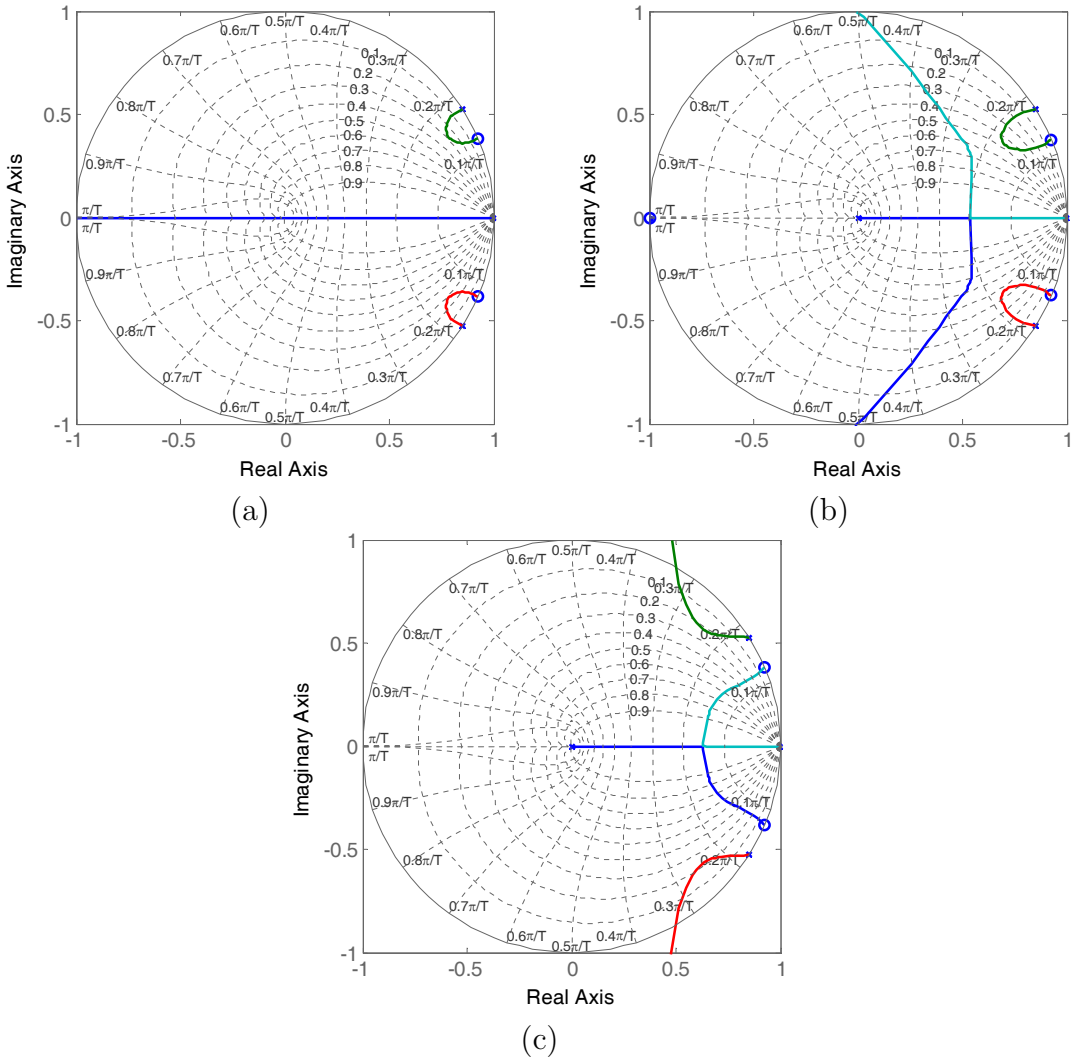


Figure 5.10: Root loci of the converter current feedback controlled grid-connected inverters in z-plane. (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

grid-connected inverter are shown in Fig. 5.13 and Fig. 5.14, respectively.

The s-domain models predictions are also used for comparison to show the advantage of proposed models. The predicted maximum proportional gains of the two control schemes with different delay effects are summarized from Fig. 5.5, Fig. 5.6, Fig. 5.10 and Fig. 5.11. These predicted results are shown in Table 5.2. For the converter current feedback control scheme, the actual proportional gain is equal to $k_p k_L$. For the converter current plus grid current feedback control scheme, the proportional gain k_p in the grid current control loop is investigated with $k_L = 0.08$.

Fig. 5.15 shows the simulation results of the converter current controlled grid-connected inverter when the actual proportional gain steps over the stability boundaries. Under the condition of the minimum delay, the root locus

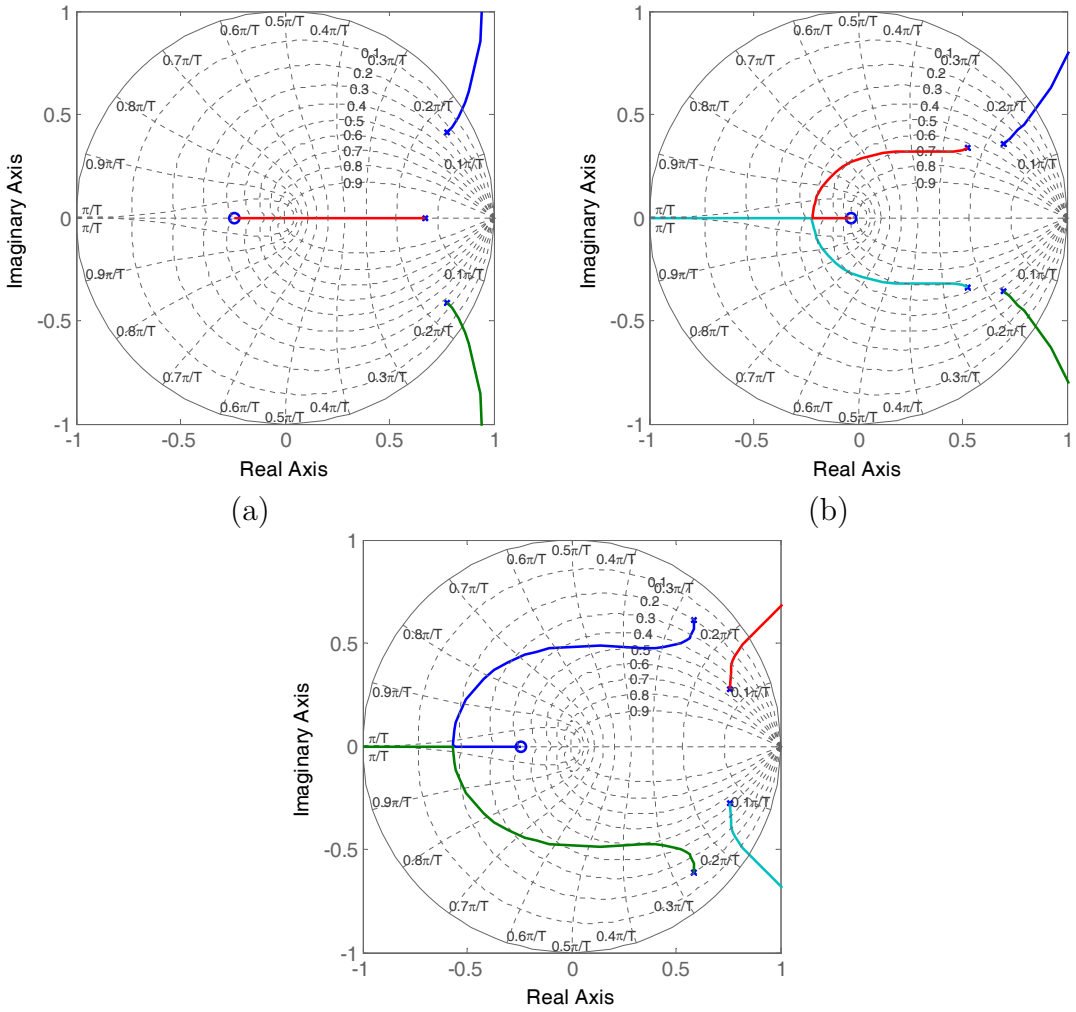


Figure 5.11: Root loci of the converter current plus grid current feedback controlled grid-connected inverters in z-plane with $k_L = 0.08$. (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

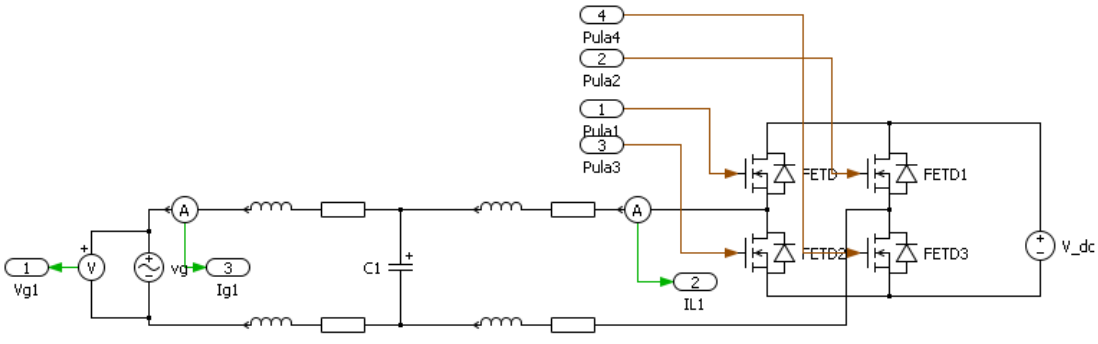


Figure 5.12: Simulink block diagram of the power circuit of the grid-connected inverter.

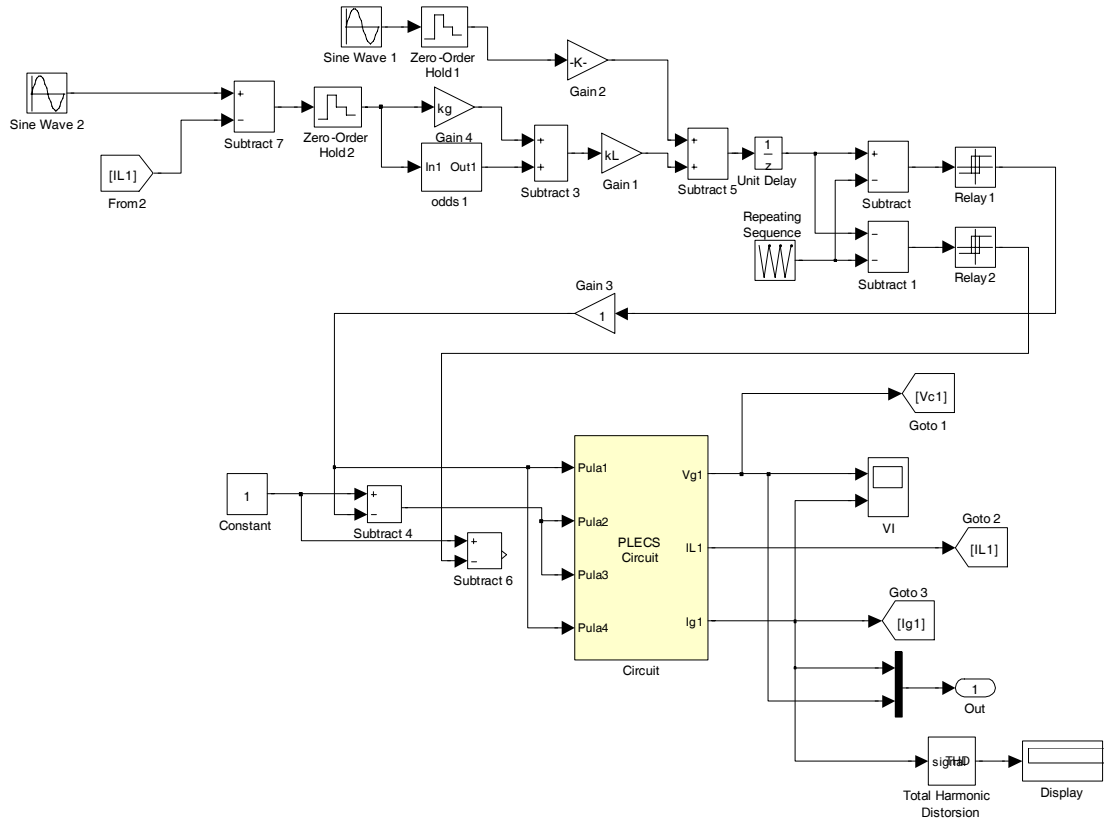


Figure 5.13: Simulink block diagram of the converter current controlled grid-connected inverter.

Table 5.2: Predicted Maximum Proportional Gains

	Control loop	Minimum delay	Medium delay	Maximum delay
Average models predictions	Converter current loop	0.651	0.315	0.201
	Grid current loop	1.09	1.05	1.04
Proposed models predictions	Converter current loop	0.324	0.306	0.139
	Grid current loop	1.04	1.04	1.02
Simulation results	Converter current loop	0.33	0.30	0.14
	Grid current loop	1.0	1.0	1.0

in Fig. 5.10(a) shows that a real pole will move across the unit circle when the proportional gain increases. As $\frac{\pi}{T_s}$ represents half of the sampling frequency, the oscillation frequency is $\frac{1}{2T_s}$ and period-2 bifurcation may appear. After the converter current passes through the CL filter, the bifurcation of the grid current is not obvious. To give a clear view of the bifurcation, the simulated converter current i_L is shown in Fig. 5.15(a), where period-2 bifurcation can be seen after $k_p k_L$ steps higher than 0.33. In contrast, with the medium delay and the maximum delay (see Fig. 5.10(b) and (c)), conjugate pole pairs will move across the unit cir-

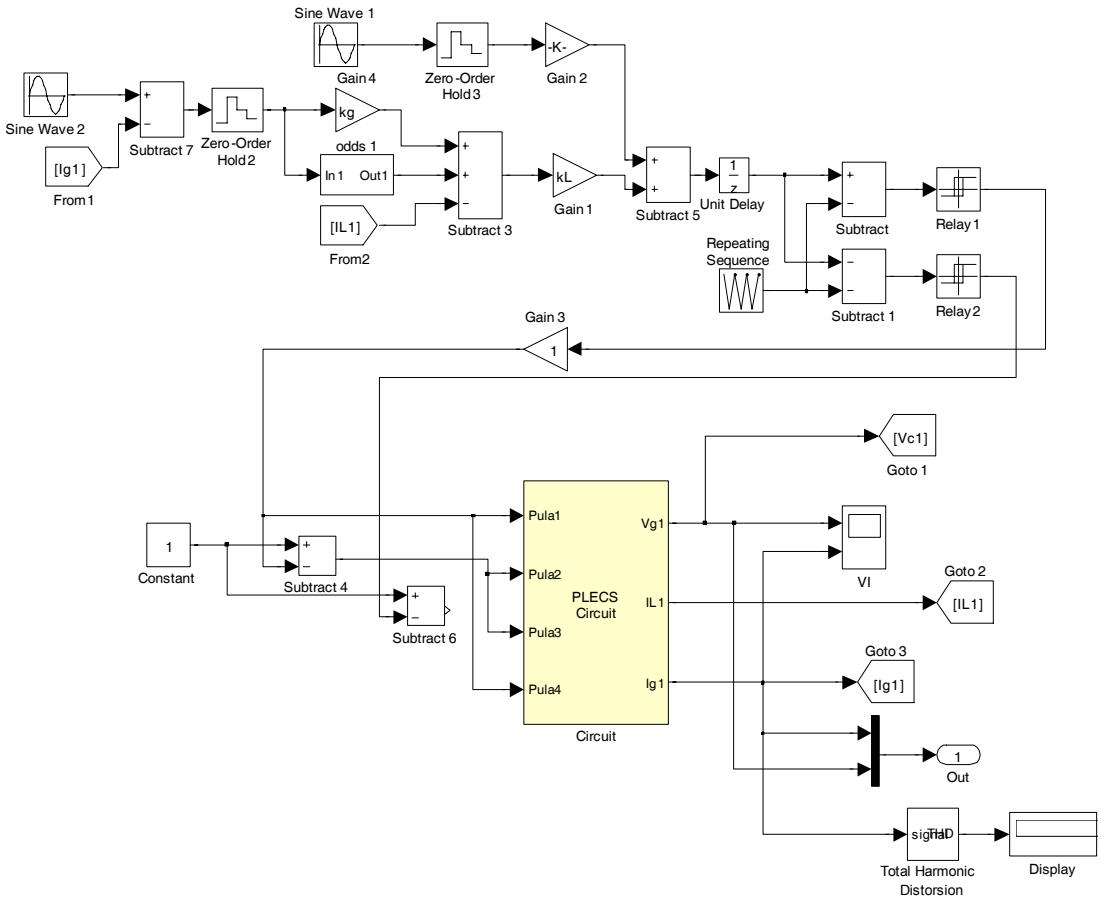


Figure 5.14: Simulink block diagram of the converter current plus grid current controlled grid-connected inverter.

cle when $k_p k_L$ is higher than 0.30 and 0.14, respectively. Hence, oscillations with lower frequencies may occur. The relevant simulation results obviously show that the converter current becomes unstable with lower oscillatory frequencies after the steps (see Fig. 5.15(b) and (c)). Comparing the simulated stability boundaries to the predicted boundaries of the average model and the proposed model, it can be seen in Table 5.2 that the accuracy of the proposed model is much better than that of the average model. The proposed model for the converter current control loop is capable of predicting the fast-scale instabilities while the classic average model is not.

Fig. 5.16 shows the simulation results of the converter current plus grid current controlled grid-connected inverter when the proportional gain of the external control loop steps over the stability boundaries. It can be clearly observed that the grid current i_g becomes unstable after each step. Slow-scale instabilities appear on the grid current. The oscillation frequencies observed in the simulation are around 1.7 kHz, which are very low compared to the sampling frequency of 20 kHz.

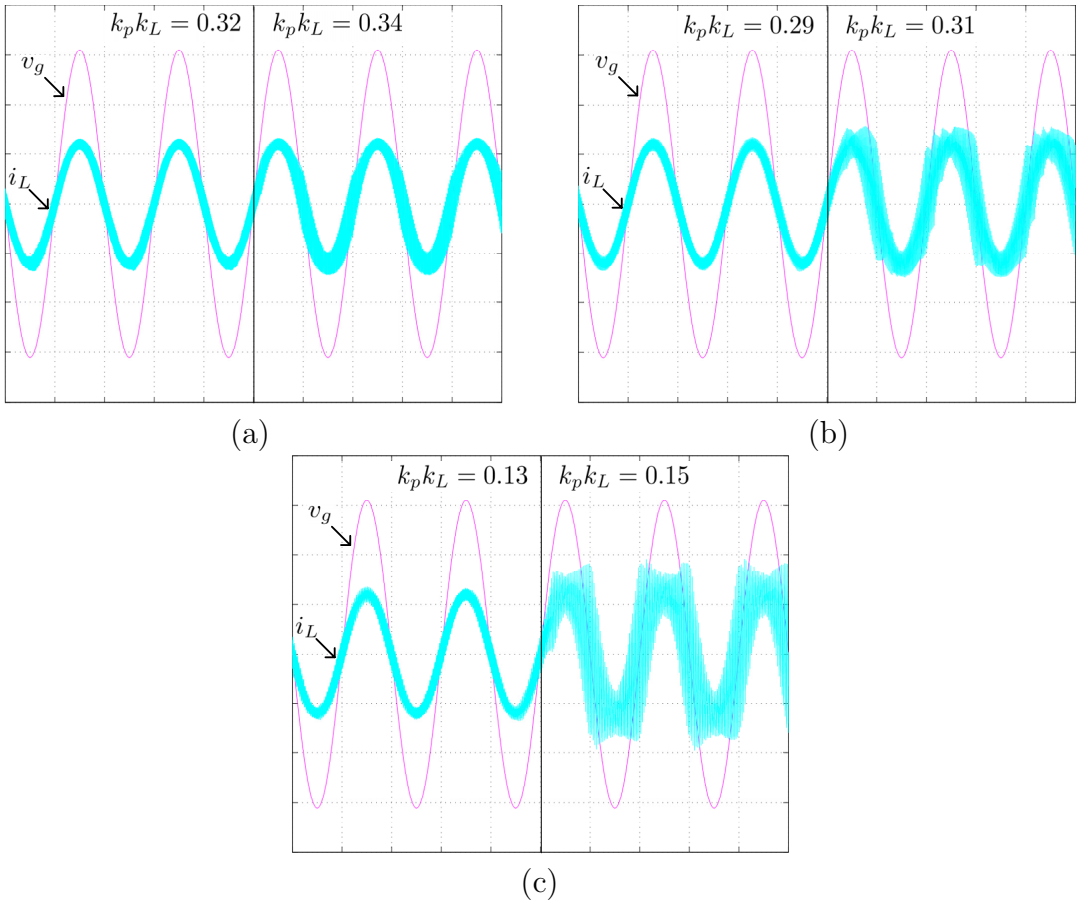


Figure 5.15: Simulated waveforms of the converter current controlled grid-connected inverter (X–axis: Time, 5 ms/div; Y–axis: Magnitude of converter current: 5 A/div; and grid voltage: 50 V/div). (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

All the conjugated pole pairs in the s-plane root loci (see Fig. 5.6) and z-plane root loci (see Fig. 5.11) move across the unit circle with oscillation frequencies around 1.77 kHz. It can be seen from Table 5.2 that the simulation results are in good agreement with the average model predictions and the proposed model predictions for the grid current control loop. This is because that the slow-scale instabilities in the external control loop are mainly caused by the LCL resonance. When the damping resistance increases, the difference between s-domain results and z-domain results becomes bigger, since the sample and hold effect will play an important role. However, the high accuracy of z-plane root loci predictions for the two control schemes verified in Table 5.2 shows that the proposed models are capable of evaluating robustness of controllers.

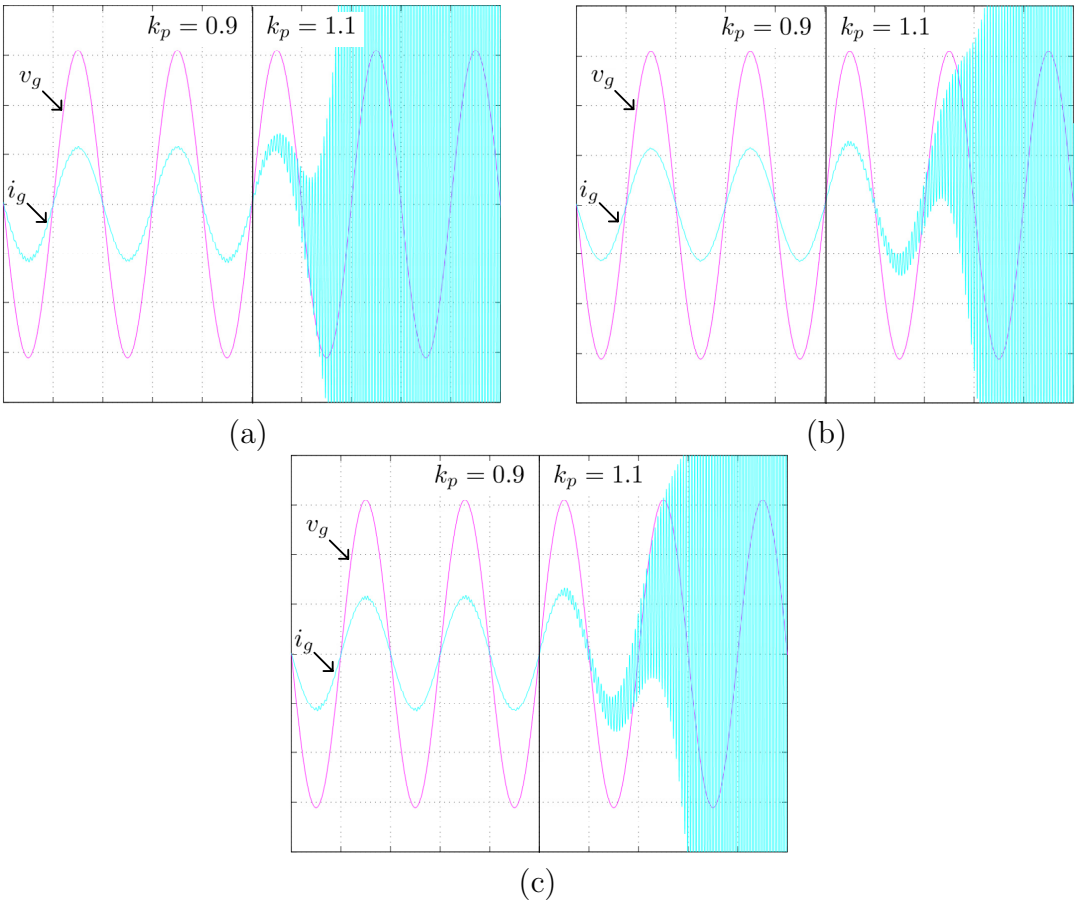


Figure 5.16: Simulated waveforms of the converter current plus grid current controlled grid-connected inverter (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current: 5 A/div; and grid voltage: 50 V/div). (a) Minimum delay. (b) Medium delay. (c) Maximum delay.

5.5 Experimental Results

To show the validity of the proposed models, both the classic s-domain models and small-signal z-domain models are used to predict time-domain waveforms of grid current and grid voltage of the inverter. The z-domain models with maximum PWM delay and the parameters listed in Table 5.1 are used for predictions. Although the z-domain models are dependent of the average duty-ratio D, the predictions are retrieved with a time-variant D.

According to the proposed modelling methods, the single loop controller and cascaded loops controller are experimentally implemented on an 110 V, 600 W grid connected inverter, as is shown in Fig. 5.17. A phase-locked loop (PLL) is used for the grid synchronization. The current reference is generated from the PLL. The experimental grid current and grid voltage are retrieved from the shunt and the left side of the transformer in Fig. 5.17, respectively. To compare the

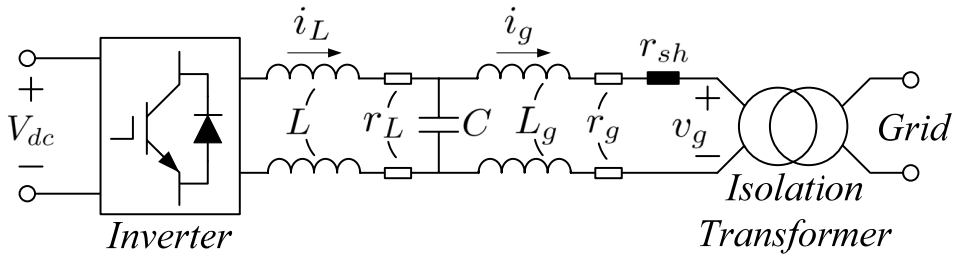


Figure 5.17: Experimental grid connected inverter.

experimental results with the model predicted results, the same compensators are used with the same parameters listed in Table 5.1. The digital controller is performed in TMS320F28335. The H bridge of the inverter is implemented by IPM. The inverter is bipolar switched with the deadband time of 2.67 μs. The uniformly-sampled symmetric-on-time triangle PWM is applied. The duty-ratio value is loaded to the PWM compare register at each sampling instant, therefore the processing delay is one switching period and the maximum PWM delay is achieved.

5.5.1 Steady-state responses

The steady-state responses are performed using a sinusoidal current reference with an RMS value of 4.6 A. The classic average models, z-domain models, simulation and experimental tests retrieved waveforms of the converter current controlled and converter current plus grid current controlled grid-connected inverters are shown in Fig. 5.18 and Fig. 5.19, respectively.

The classic average model and the z-domain model retrieved steady-state responses of the converter current controlled grid-connected inverter are almost identical (see Fig. 5.18(a) and Fig. 5.18(b)). The predicted current amplitudes (I_g) and phase angles ($\Delta\phi$) are 4.6 A and 4.5°, respectively. These predictions are in very good agreement with the simulation result shown in Fig. 5.18(c). However, it is shown in Fig. 5.18(d) that under the practical condition of a weak grid, a larger phase lag exists in the current with a phase angle of $\Delta\phi = 13.3°$. The experimental current amplitude has difference with the models predicted results. Moreover, when the grid voltage contains considerable harmonic components (THD $\approx$ 2.0%), the grid current THD is about 2.7%. The performance of this control scheme is severely affected by the quality of the grid voltage.

The steady-state responses of the converter current plus grid current controlled grid-connected inverter show that the predictions of the classic average model and the z-domain model are almost the same (see Fig. 5.19(a) and Fig. 5.19(b)). The current amplitudes and phase angles in models predictions are

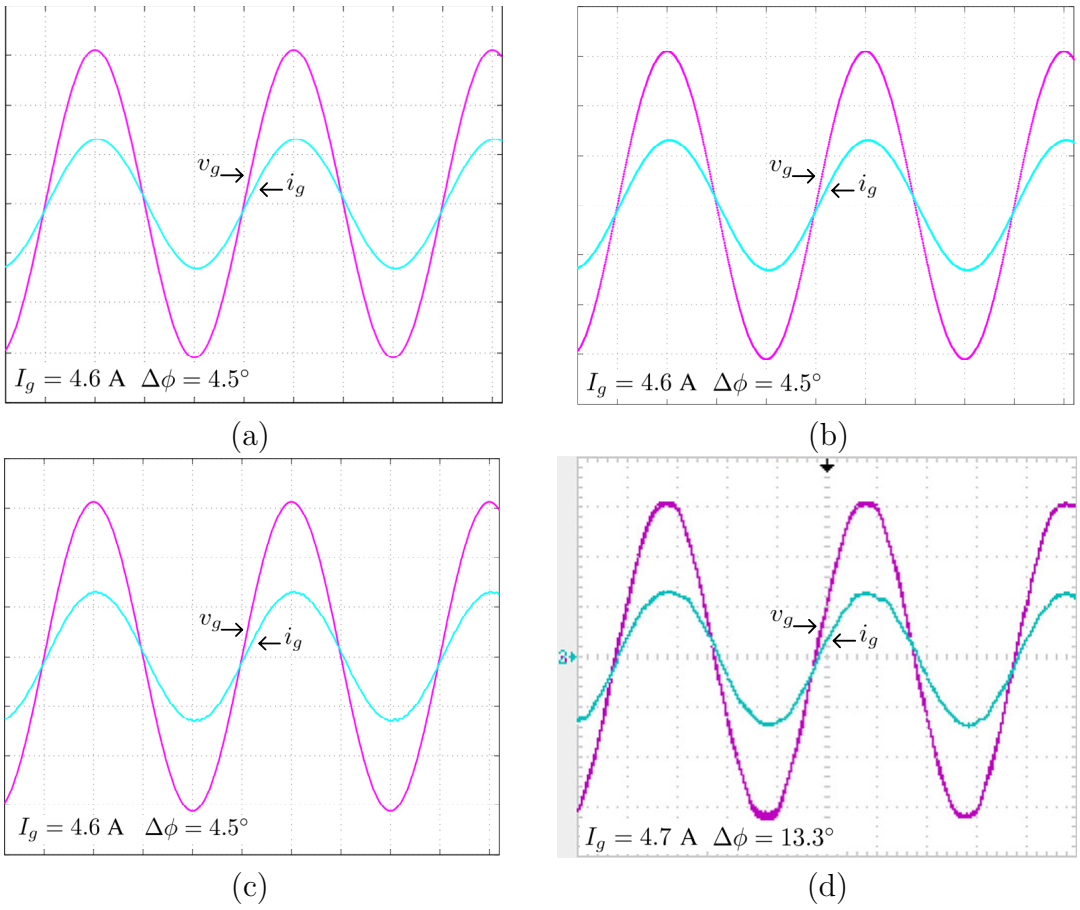


Figure 5.18: Steady-state response of the converter current controlled grid-connected inverter (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current: 5 A/div; and grid voltage: 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Simulation result (d) Experimental result.

4.4 A and 0.45°, respectively. The simulation result is in accordance with the models predictions (see Fig. 5.19(c)). However, in the experimental results (see Fig. 5.19(d)), the current amplitude is 4.5 A and the phase angle is 6.9°. The experimental grid current has a relative larger phase lag than the predicted results and the simulation result. Compared to the converter current control scheme, the experimental current distortion remains low (THD $\approx$ 2.1%) in this control scheme.

Since the converter current control scheme achieves a higher closed-loop gain, the amplitude of grid current in Fig. 5.18 is higher than that in Fig. 5.19. It can be seen from Fig. 5.18 that when the converter current feedback scheme is used, the grid current has a larger lagging phase angle. In contrast, when the converter current plus grid current feedback scheme is used, a smaller grid current phase error is achieved (see Fig. 5.19). In the environment when a distorted grid voltage appears, exact predictions for experimental tests are not guaranteed. However,

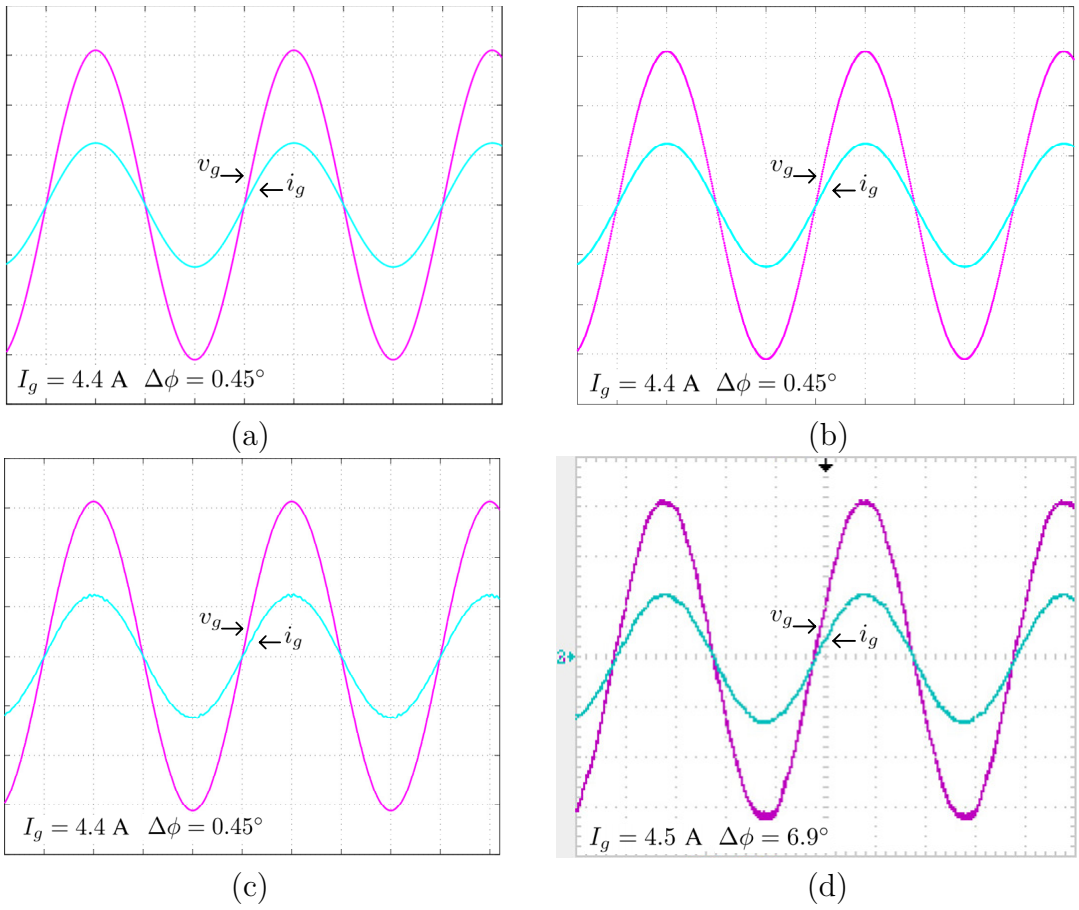


Figure 5.19: Steady-state response of the converter current plus grid current controlled grid-connected inverter (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current: 5 A/div; and grid voltage: 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Simulation result (d) Experimental result.

it is concluded that both the classic average models and z-domain models can be used with good accuracy.

5.5.2 Transient responses

Fig. 5.20 and Fig. 5.21 show the transient responses of the converter current controlled grid-connected inverter when the reference current steps at its peak. The grid current achieves steady-state operation within two line cycles after the step. The dynamic response time of this control scheme is short. The average model and z-domain model predicted waveforms after the step are almost identical. The predicted results are similar to the simulation and experimental results. However, the experimental results are more different. This is because that in this control scheme, the grid voltage adds significant harmonic components to the experimental data. When the amplitude of the grid current is small, this disturbance is more obvious. To a first approximation, the agreement between predicted results

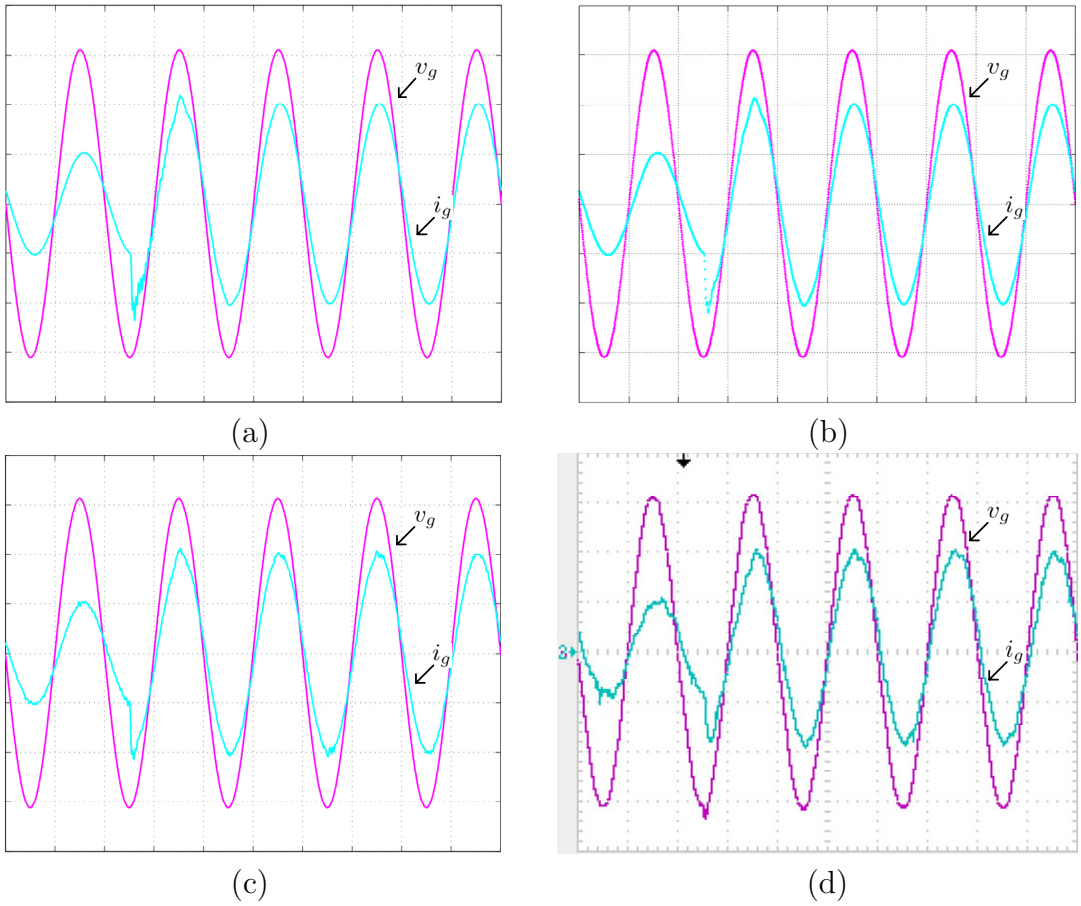


Figure 5.20: Transient response of the converter current controlled grid-connected inverter with a step in the commanded current peak value from 2 A to 4 A (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current and grid voltage; Channel 2: grid current, 2 A/div; Channel 3: grid voltage, 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Simulation result (d) Experimental result.

and experimental results is good.

The transient responses of the converter current plus grid current controlled grid-connected inverter are shown in Fig. 5.22 and Fig. 5.23, where the disturbance from grid in this control scheme is quite small. The average model predicted results exhibit obvious oscillatory transitions (see Fig. 5.22(a) and Fig. 5.23(a)). However, the z-domain model predicted transitions (see Fig. 5.22(b) and Fig. 5.23(b)) are very similar to the simulation results (see Fig. 5.22(c) and Fig. 5.23(c)) and experimental results (see Fig. 5.22(d) and Fig. 5.23(d)), where no much transient oscillation is visible. After the step, the grid current achieves steady-state in more than four line cycles. During this time, both of the average model and the z-domain model predicted results are similar to the simulation and experimental results. As this control scheme has a good suppression on harmonic

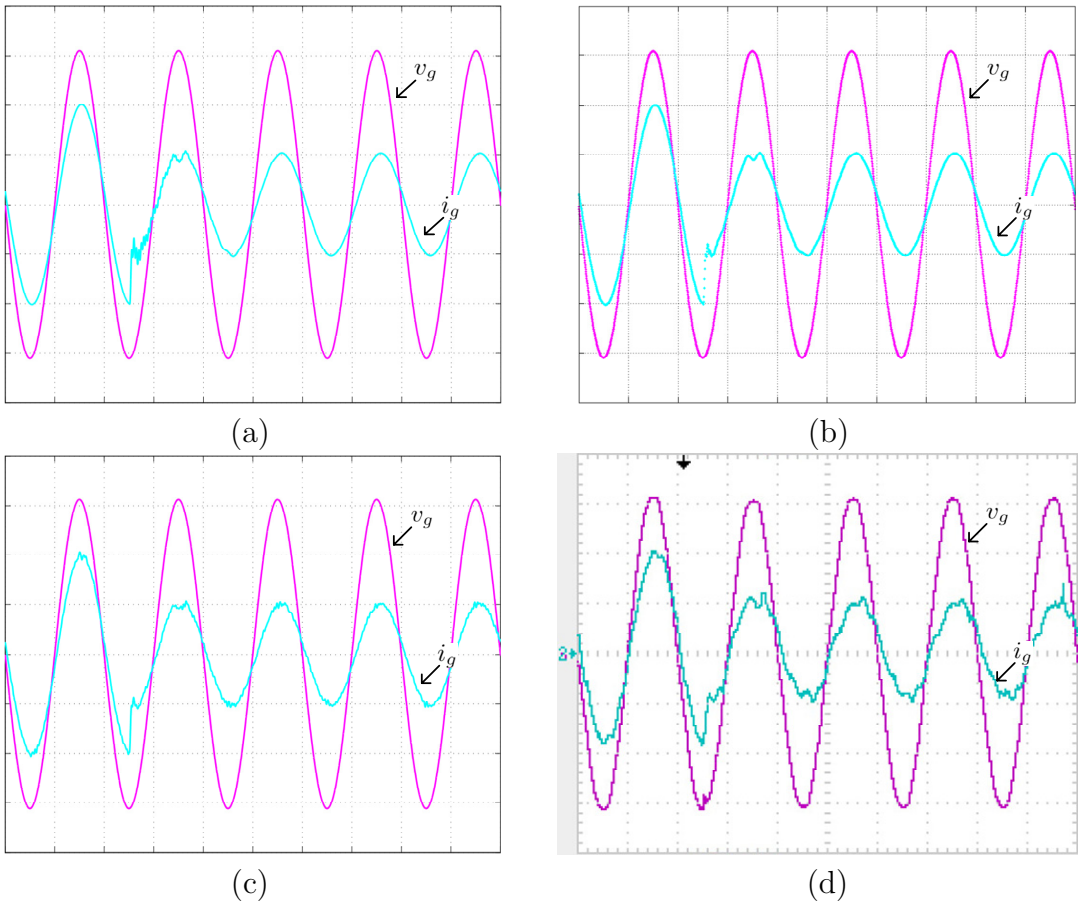


Figure 5.21: Transient response of the converter current controlled grid-connected inverter with a step in the commanded current peak value from 4 A to 2 A (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current and grid voltage; Channel 2: grid current, 2 A/div; Channel 3: grid voltage, 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Simulation result (d) Experimental result.

current components, the agreement between predictions and experimental results is good. A longer transition exist in the converter current plus grid current control scheme since the closed-loop gain on Bode plot is always lower than that of the converter current control scheme.

An obvious disadvantage existing in the z-domain models is the duty-ratio dependent instinct. When triangle carriers are used, the sum of the two PWM delay terms is equivalent to an averaged delay with half switching period [59]. The error of this approximation when duty-ratio varies is negligible. This error is only unacceptable if sawtooth carriers are used. However, in sampled-data ac systems, sawtooth PWMs which cannot guarantee an average current sampling are rarely used.

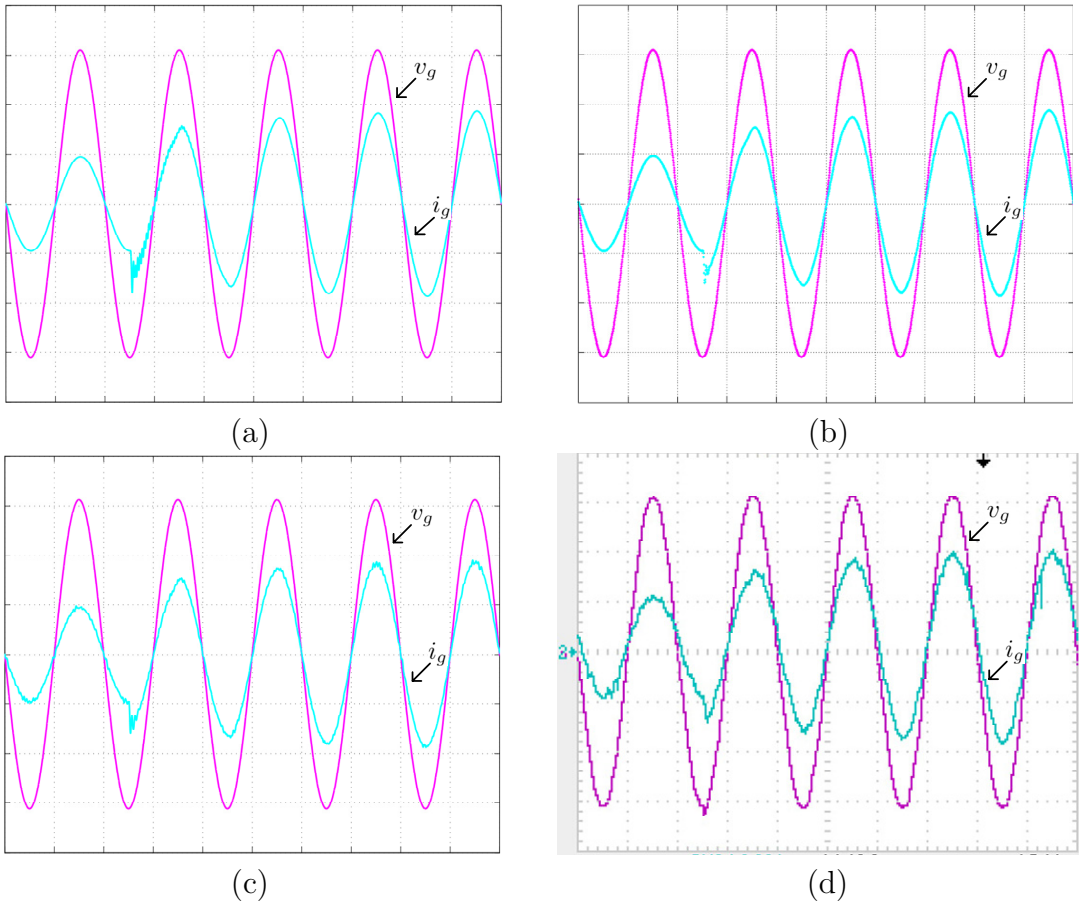


Figure 5.22: Transient response of the converter current plus grid current controlled grid-connected inverter with a step in the commanded current peak value from 2 A to 4 A (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current and grid voltage; Channel 2: grid current, 2 A/div; Channel 3: grid voltage, 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Simulation result (d) Experimental result.

5.6 Conclusion

In this chapter, typical digitally controlled grid-connected inverters with a single control loop and cascaded control loops are studied. The classic average models derived in s-domain for the two control schemes are described without including the effect of sample and hold. In contrast, new small-signal z-domain models are produced considering possible delay effects under most possible circumstances. The small-signal z-domain models including different delay effects are precisely modeled for digitally controlled converters with a single control loop and cascaded control loops. This permits a direct design of the digital compensators in z-domain. The internal converter current loop stability condition is analytically derived based on the z-domain models. Furthermore, the proposed models are capable of predicting the dynamic responses and the steady-state values of the

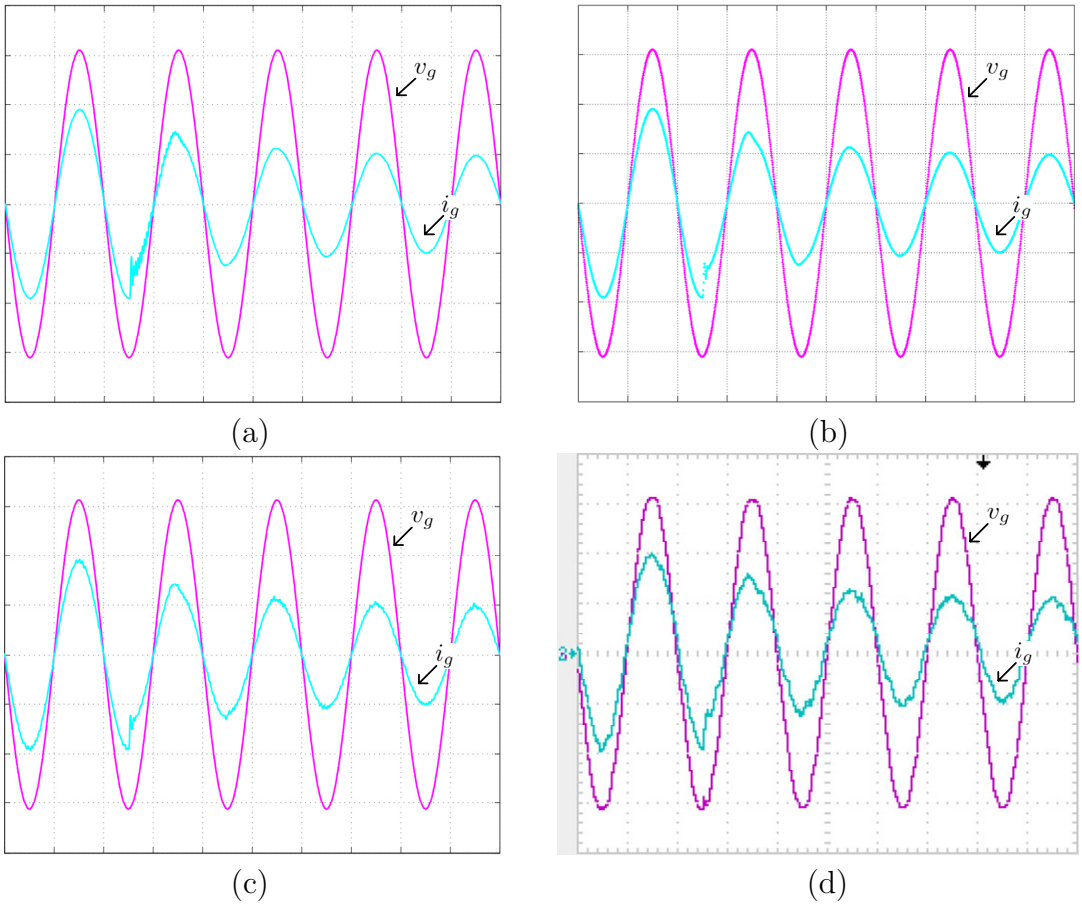


Figure 5.23: Transient response of the converter current plus grid current controlled grid-connected inverter with a step in the commanded current peak value from 4 A to 2 A (X–axis: Time, 5 ms/div; Y–axis: Magnitude of grid current and grid voltage; Channel 2: grid current, 2 A/div; Channel 3: grid voltage, 50 V/div). (a) Average model prediction. (b) z-domain model prediction. (c) Simulation result (d) Experimental result.

control variables at the sampling instants. The frequency responses and root loci of the two control schemes are obtained, resulting in the relevant design specifications. The experimental prototype is implemented according to the proposed models. The comparison between the predictions of the models and the experimental results with the two control schemes confirms the validity of the proposed models.

Chapter 6

Modelling of Multisampled Multilevel Inverters with Improved Control Performance

6.1 Introduction

In classic digital control methods, synchronized sampling and switching is a good solution to avoid noise and ripple in the vicinity of the switching instants [47, 49], with the uniformly-sampled converter current representing the current value averaged in each switching cycle. The controller usually employs an internal converter current loop with proportional (or plus integral) feedback control [50, 74]. To guarantee a stable operation, the maximum proportional feedback gain in the current loop is limited by the sampling frequency and the converter side inductance [38]. As is reported in [32], if the current sampling frequency is halved, the control gain has to be reduced by the factor of two, which results in a degraded control performance. Apparently, if both the sampling frequency and the switching frequency can be increased, larger control gains and better performance are achievable.

The rapid performance improvement of DSPs, or when combined with additional FPGAs means that applying high sampling frequency of exact multiples of the switching frequency becomes feasible [75], [76], [77]. This new approach is known as multisampling and has the purpose of reducing the delay of the PWM and improving the control bandwidth. However, this approach has a major drawback that the multisampling also samples the current ripple. If the samples are not acquired at the peaks of the triangle PWM carrier, an average current is not guaranteed for the digital controller. In the dc-ac or ac-ac converters with a multisampling factor N, current distortion may appear when the duty-ratio is equal to the integer multiples of $\frac{1}{N}$. Hence, a digital filter is required to remove the switching ripple from the sampled current [78]. Moveover, when multisampling

is used without increasing the switching frequency, the control gains and performance are still limited by the switching frequency. Therefore, a high switching frequency [32] or a high converter current ripple frequency [38] is still necessary to improve the control performance.

The application of multilevel inverters has attracted wide interests in medium voltage management markets [79, 80]. Many topologies have been proposed such as diode clamped inverter [81, 82, 83], capacitor clamped inverter [84], generalized multilevel inverter [85], cascaded multilevel inverters [86, 87, 88, 89] and hybrid topologies. These multilevel inverters can significantly reduce the harmonic current components where lower size filter can be used. To maximise the number of voltage levels, asymmetric cascaded inverters have been proposed [90, 91]. Although the dc sources with different voltages are required, capacitors can be used in stead of dc sources with proper control strategy [92].

There are two typical modulation strategies for single-phase multilevel inverters, i.e., level-shifted PWM and phase-shifted PWM. Due to practical limitations of the switching devices, the switching frequency can not be easily increased. However, with the multilevel inverter structures [79, 87, 93, 94, 95], the filter current ripple frequency can be increased by the phase-shifted PWM modulation strategy [95, 96, 97, 98, 99]. Without changing the switching frequency of each switch, the ripple frequency can be increased in respect to the number of inverter levels. The multisampling is performed according to the number of the phase-shifted carriers [100, 101, 102, 103]. A classic voltage controller with cascaded control loops for the multilevel inverter system, behaving as a typical linear control system, is given as an example. In order to study the improved control performance of multisampled multilevel inverters, the small-signal z-domain model is derived for the analysis. The analysis reveals that higher feedback gains can be employed in the controller, which improves the control performance. Experimental results of a five-level inverter with octuple sampling frequency are provided to validate the analysis.

6.2 Uniformly-sampled bipolar switched single-phase H bridge inverter

Fig. 6.1 shows the power circuit of a single-phase H bridge inverter. The LC filter is connected to smooth the filter input voltage v_{in}. The controller of the stand-alone inverter is a cascaded linear controller composed of an internal current control loop and an external voltage control loop with duty-ratio feedforward ($k_{ff} = 1$), as is shown in Fig. 6.2. The ideally sampled output voltage and inductor current are represented by v_o^* and i_L^*, respectively. A proportional feedback

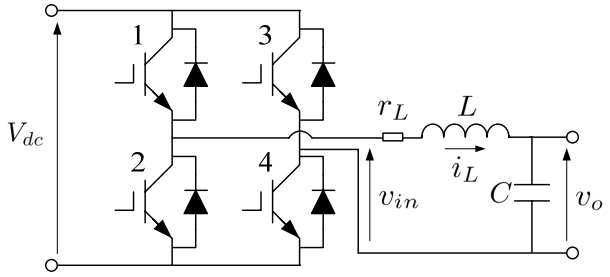


Figure 6.1: A single-phase H bridge inverter.

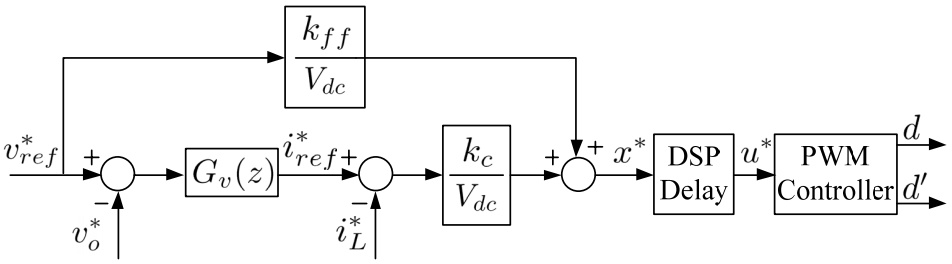
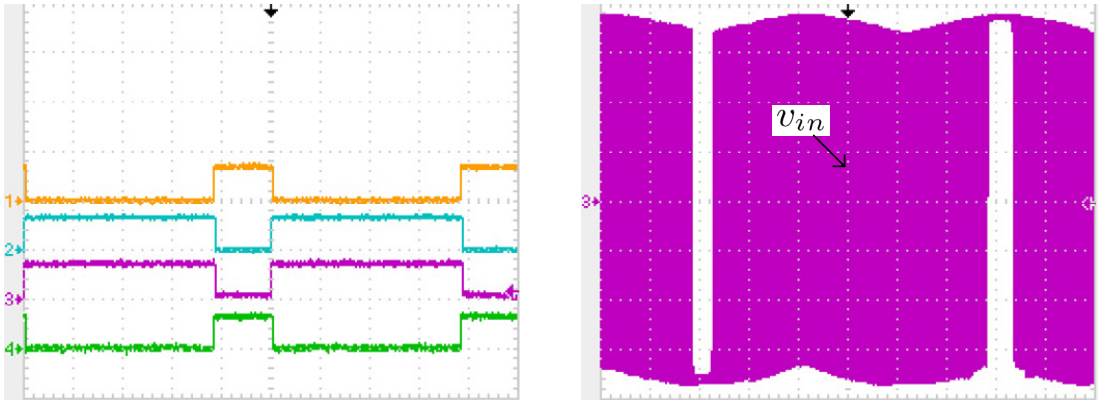


Figure 6.2: Digital controller of the single-phase H bridge inverter.

controller is used in the internal loop with the gain of k_c, while a PR controller is applied to the external voltage loop. The compensator of the voltage control loop is $G_v(z) = k_v + k_r \sum_{k=1}^{h} H_k(z)$, where $H_k(z)$ is the digitalized band-pass filter resonating at kth odd harmonic frequency. The ideally calculated (without delay) digital duty-ratio is x^*, which is updated into the PWM controller with a DSP delay period (ADC delay and computation delay). The PWM controller's updated duty-ratio signal u^* is then converted to the level signal u_H by a ZOH and compared with the triangle carrier v_c to generate the drive signals d and d'. For a bipolar switched single-phase H bridge inverter, the drive signal for IGBT 1 and 4 is d, whereas for IGBT 2 and 3 is d'. Signals d and d' are complementary but with a deadband. The waveforms of drive signals and the filter input voltage v_{in} are shown in Fig. 6.3.

In order to select the feedback control gains, the model describing the digital control loops is needed. The key waveforms of the bipolar PWM inverter is shown in Fig. 6.4, where the triangle carrier is represented by v_c with a switching frequency of $f_s = \frac{1}{T_s}$. The sampling is synchronized to the time when the PWM counter equals period value. Assuming the total time of ADC conversion and duty-ratio computation is less than half sampling period, then the calculated duty-ratio can be updated into the compare register at the time when the counter equals zero. Therefore, the DSP delay from x^* to u^* is a half sampling period. As u^* is converted to u_H by a ZOH and the drive signals are generated by comparing u_H with v_c, the PWM delays from u^* to the relevant drive signals in small signal



(a) (b)

Figure 6.3: Waveforms of drive signals and filter input voltage of a bipolar switched inverter. (a) Drive signals for IGBT 1, 2, 3 and 4 (X–axis: Time, 10 μs/div; Y–axis: Magnitude, 5 V/div). (b) Filter input voltage v_{in} (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/div).

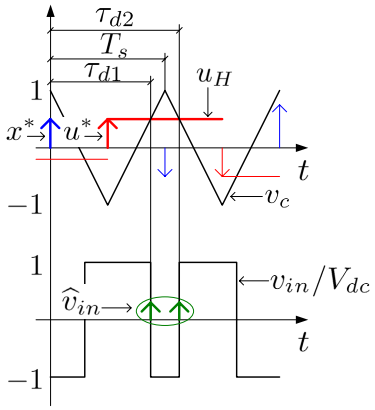


Figure 6.4: Key waveforms of the bipolar switched inverter.

are described by $e^{-s\frac{DT_s}{2}}$ and $e^{-s\frac{(2-D)T_s}{2}}$, where D is the average duty-ratio scaled in the range of $(0, 1)$. Assuming there is no delay from the drive signals to the filter input voltage v_{in}, the small-signal pulse-to-continuous transfer function describing $\widehat{v}_{in}$ as a function of $\widehat{x}^*$ can be written as [25]

$$G_{v_{in}x^*}(s) = \frac{V_{dc}T_s}{2}(e^{-s\tau_{d1}} + e^{-s\tau_{d2}}) \tag{6.1}$$

with $\tau_{d1} = \frac{(1+D)T_s}{2}$ and $\tau_{d2} = \frac{(3-D)T_s}{2}$.

When the inverter has no load, the transfer functions describing the inductor current i_L and output voltage v_o as a function of the filter input voltage v_{in} are

$$G_{i_L v_{in}}(s) = \frac{s/L}{s^2 + sr_L/L + 1/LC} \tag{6.2}$$

and

$$G_{v_o v_{in}}(s) = \frac{1/LC}{s^2 + sr_L/L + 1/LC}, \tag{6.3}$$

respectively. Hence, the pulse transfer functions from x^* to the sampled signals i_L^* and v_o^* in small signal are

$$G_{i_L^* x^*}(z) = \mathcal{Z}\{G_{v_{in}x^*}(s) G_{i_L v_{in}}(s)\} \tag{6.4}$$

and

$$G_{v_o^* x^*}(z) = \mathcal{Z}\{G_{v_{in}x^*}(s) G_{v_o v_{in}}(s)\}, \tag{6.5}$$

respectively.

The z-transform of (6.4) can be derived by splitting $G_{i_L^* x^*}(z)$ into

$$G_{i_L^* x^*}(z) = \frac{V_{dc}T_s}{2}\mathcal{Z}\{\frac{s/Le^{-s\tau_{d1}}}{s^2 + sr_L/L + 1/LC} + \frac{s/Le^{-s\tau_{d2}}}{s^2 + sr_L/L + 1/LC}\}. \tag{6.6}$$

Equation (6.6) can be written in a simplified form as

$$G_{i_L^* x^*}(z) = \frac{V_{dc}T_s}{2}\mathcal{Z}\{\frac{A_i e^{-s\tau_{d1}}}{s+a} + \frac{B_i e^{-s\tau_{d1}}}{s+b} + \frac{A_i e^{-s\tau_{d2}}}{s+a} + \frac{B_i e^{-s\tau_{d2}}}{s+b}\} \tag{6.7}$$

with $a = \frac{1}{2}(\frac{r_L}{L} + \sqrt{\Delta})$, $b = \frac{1}{2}(\frac{r_L}{L} - \sqrt{\Delta})$, $\Delta = (\frac{r_L}{L})^2 - \frac{4}{LC}$, $A_i = \frac{a}{L(a-b)}$ and $B_i = -\frac{b}{L(a-b)}$. Note that $\tau_{d1} < T_s$ and $T_s < \tau_{d2} < 2T_s$. The delay of the third and fourth terms of the right side of (6.7) should be treated differently, i.e.,

$$\begin{aligned} G_{i_L^* x^*}(z) =& \frac{V_{dc}T_s}{2}\mathcal{Z}\{\frac{A_i e^{-s\tau_{d1}}}{s+a} + \frac{B_i e^{-s\tau_{d1}}}{s+b}\} \\ &+ \frac{V_{dc}T_s z^{-1}}{2}\mathcal{Z}\{\frac{A_i e^{-s(\tau_{d2}-T_s)}}{s+a} + \frac{B_i e^{-s(\tau_{d2}-T_s)}}{s+b}\}. \end{aligned} \tag{6.8}$$

Based on the z-transform theory, the z-transforms in (6.8) can be obtained as

$$\begin{aligned} G_{i_L^* x^*}(z) =& \frac{V_{dc}T_s}{2}(\frac{A_i e^{a(\tau_{d1}-T_s)}}{z - e^{-aT_s}} + \frac{B_i e^{b(\tau_{d1}-T_s)}}{z - e^{-bT_s}}) \\ &+ \frac{V_{dc}T_s z^{-1}}{2}(\frac{A_i e^{a(\tau_{d2}-2T_s)}}{z - e^{-aT_s}} + \frac{B_i e^{b(\tau_{d2}-2T_s)}}{z - e^{-bT_s}}), \end{aligned} \tag{6.9}$$

which can be written as

$$\begin{aligned} G_{i_L^* x^*}(z) &= \frac{N_{i11}z + N_{i10}}{z^2 + D_1 z + D_0} + \frac{N_{i21}z + N_{i20}}{z^3 + D_1 z^2 + D_0 z} \\ &= \frac{N_{i11}z^2 + (N_{i10} + N_{i21})z + N_{i20}}{z^3 + D_1 z^2 + D_0 z} \end{aligned} \tag{6.10}$$

with

$N_{i11} = \frac{V_{dc}T_s}{2}(A_i e^{-a(T_s - \tau_{d1})} + B_i e^{-b(T_s - \tau_{d1})})$,

$N_{i10} = -\frac{V_{dc}T_s D_0}{2}(A_i e^{a\tau_{d1}} + B_i e^{b\tau_{d1}})$,

Table 6.1: Parameters of the Bipolar Switched Inverter

Symbol	Quantity	Value
V_{dc}	DC voltage amplitude	200 V
T_s	Switching and sampling period	100 μs
L	Inductor	1642 μH
C	Capacitor	10 μF
r_L	Inductor parasitic resistance	0.4 Ω

$N_{i21} = \frac{V_{dc}T_s}{2}(A_i e^{-a(2T_s-\tau_{d2})} + B_i e^{-b(2T_s-\tau_{d2})})$,
$N_{i20} = -\frac{V_{dc}T_sD_0}{2}(A_i e^{a(\tau_{d2}-T_s)} + B_i e^{b(\tau_{d2}-T_s)})$,
$D_1 = -e^{-aT_s} - e^{-bT_s}$ and $D_0 = e^{-(a+b)T_s}$. Similarly, the z-transform of (6.5) can be derived as

$$\begin{aligned} G_{v_o^* x^*}(z) &= \frac{N_{v11}z + N_{v10}}{z^2 + D_1 z + D_0} + \frac{N_{v21}z + N_{v20}}{z^3 + D_1 z^2 + D_0 z} \\ &= \frac{N_{v11}z^2 + (N_{v10} + N_{v21})z + N_{v20}}{z^3 + D_1 z^2 + D_0 z} \end{aligned} \tag{6.11}$$

with
$N_{v11} = \frac{V_{dc}T_s}{2}(A_v e^{-a(T_s-\tau_{d1})} + B_v e^{-b(T_s-\tau_{d1})})$,
$N_{v10} = -\frac{V_{dc}T_sD_0}{2}(A_v e^{a\tau_{d1}} + B_v e^{b\tau_{d1}})$,
$N_{v21} = \frac{V_{dc}T_s}{2}(A_v e^{-a(2T_s-\tau_{d2})} + B_v e^{-b(2T_s-\tau_{d2})})$,
$N_{v20} = -\frac{V_{dc}T_sD_0}{2}(A_v e^{a(\tau_{d2}-T_s)} + B_v e^{b(\tau_{d2}-T_s)})$,
$D_1 = -e^{-aT_s} - e^{-bT_s}$ and $D_0 = e^{-(a+b)T_s}$.

Therefore, according to Fig. 6.2, the closed-loop transfer function from i^*_{ref} to x^* without feedforward can be written as

$$G_1(z) = \frac{\frac{k_c}{V_{dc}}}{1 + \frac{k_c}{V_{dc}} G_{i_L^* x^*}(z)}. \tag{6.12}$$

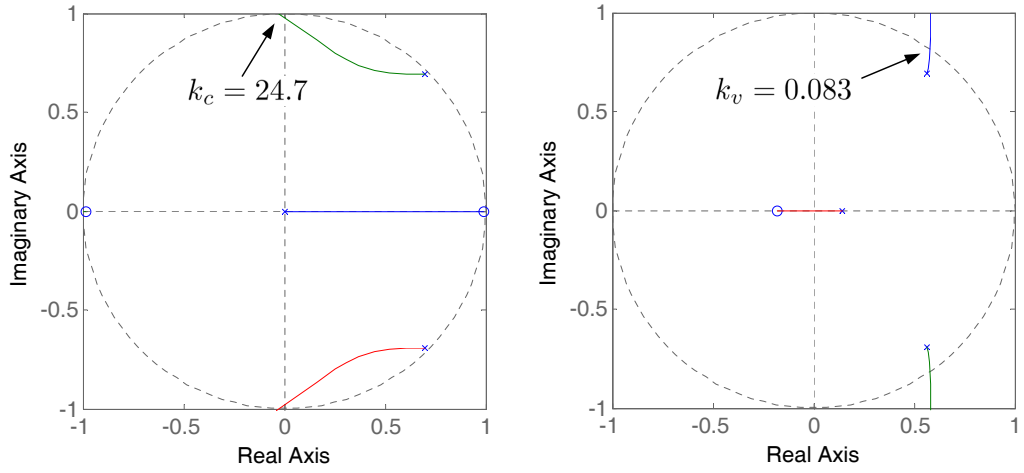
The closed-loop transfer function from v^*_{ref} to x^* without feedforward is

$$G_2(z) = \frac{G_v(z)G_1(z)}{1 + G_v(z)G_1(z)G_{v_o^* x^*}(z)}. \tag{6.13}$$

By using the parameters listed in Table 6.1, the root loci of the internal current control loop and the external voltage control loop are shown in Fig. 6.5. According to in Fig. 6.5, to ensure stable operation in the experimental tests, k_c should be smaller than 24.7 and k_v should be smaller than 0.083. In our case, the proportional gains are chosen as $k_c = 4$ and $k_v = 0.05$.

6.3 Multisampled multilevel inverters

To demonstrate the improved control performance as a result of the multisampled multilevel inverter, this section provides a detailed analysis of the system's



(a) (b)

Figure 6.5: Root loci of the control loops. (a) Internal current loop. (b) External voltage loop with $k_c = 4$.

operation compared to the bipolar switched inverter. A system comprised of two cascaded H bridges inverters and modulated by four phase-shifted PWMs with octuple-sampling frequency is modeled. The analysis is undertaken to assess the performance advantages of the multisampled multilevel inverter.

6.3.1 System configuration

The power circuit of multilevel inverters with two cascaded H bridges topology is shown in Fig. 6.6. Compared to the single H bridge inverter, the dc voltage to each is halved. The drive signals for the upper and lower switches in each leg are complementary. Therefore, four independent drive signals are generated from the digital controller which block diagram is shown in Fig. 6.7.

6.3.2 Phase-shifted PWM

Two typical modulation strategies are usually used for multilevel inverters [98, 96]. The level-shifted modulation method requires the same switching frequency as the filter current ripple frequency [104]. To achieve higher ripple frequency than switching frequency, the phase-shifted PWM strategy can be employed for the multilevel inverters. This modulation method is characterized by its capability of improving the control performance of the filter voltage and current [105]. Since the filter input voltage frequency is increased as multiples of the switching frequency, achieving an enhanced dynamic performance is evident. However, a precise model for the digital modulator which can be used to design the controller has not been proposed to date.

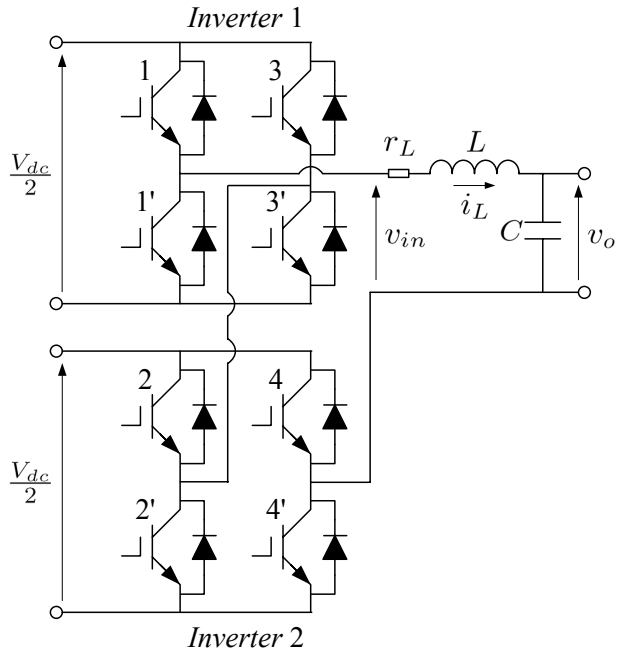


Figure 6.6: The five-level H bridge inverters.

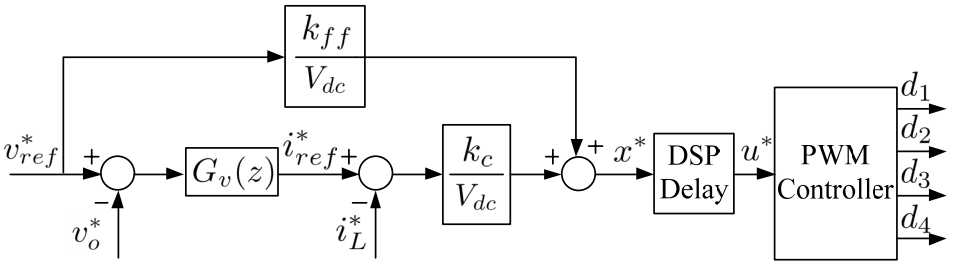


Figure 6.7: Digital controller of the five-level H bridge inverters.

For the case when there is no vertical crossing between the modulating signals and the carriers, the time-domain diagram explaining the phase-shifted PWM is shown in Fig. 6.8. To generate the drive signals, two opposite duty-ratios are updated into PWM comparator as u_H and u'_H. The carriers v_{c1} and v_{c2} are used to compare with u_H to drive switches 1 and 2 in Fig. 6.6, respectively, with v_{c2} leading v_{c1} by a phase angle of 90°. The carriers v_{c3} and v_{c4} are used to compare with u'_H to drive switches 3 and 4, respectively, with v_{c4} leading v_{c3} by a phase angle of 90°. Moreover, v_{c1} and v_{c3} are synchronized. The sampling is synchronized to the peaks of the carriers with the sampling frequency being eight times of the switching frequency. The waveforms of the drive signals and the filter input voltage of a multilevel inverter are shown in Fig. 6.9.

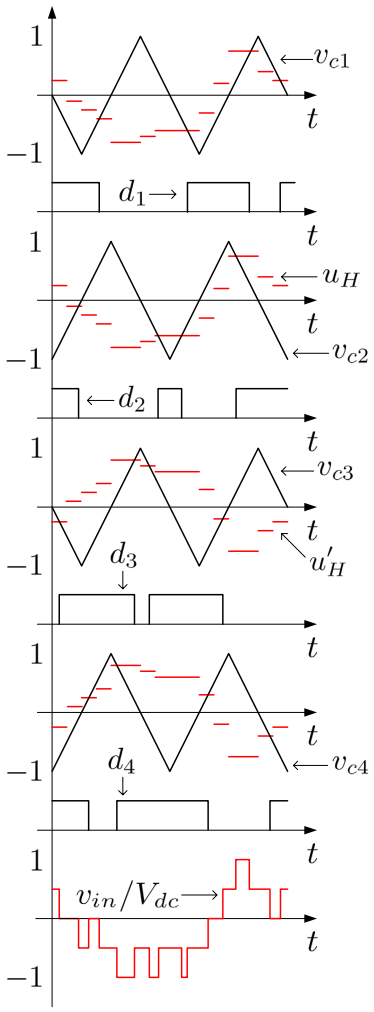


Figure 6.8: Time-domain waveforms of the phase-shifted PWM.

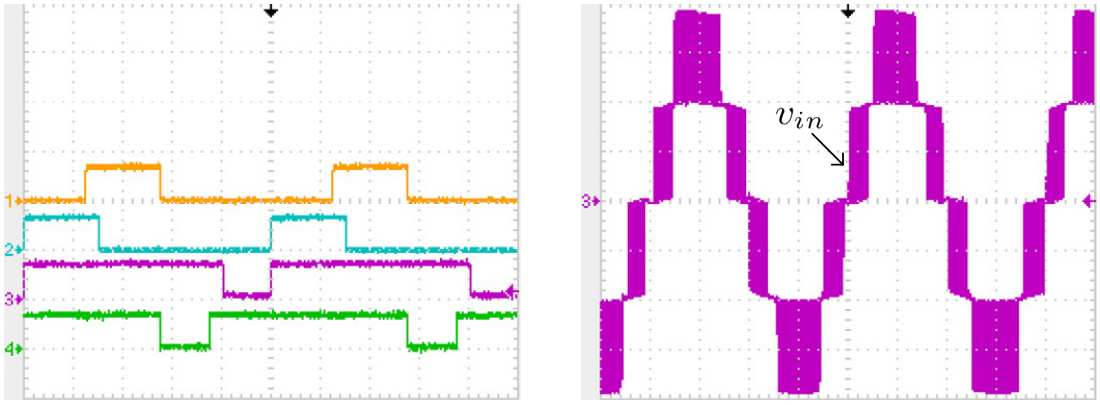
6.3.3 Current ripple reduction

Multilevel inverters also provide an effective way of suppressing the filter current ripple reduction [106]. For comparison, the ripple amplitude of the bipolar switched inverter is derived first. To simplify the analysis, we assume the inductor has no parasitic resistance and the capacitor voltage v_o has a relative slow dynamic behaviour. Then, the voltage on the filter inductor is

$$V_{dc} - v_o = L\frac{\Delta i_L}{DT_s} \tag{6.14}$$

during the rising edge of the inductor current, with Δi_L the peak-to-peak amplitude of the current ripple. When the current is falling, the inductor voltage is written as

$$-V_{dc} - v_o = L\frac{-\Delta i_L}{(1-D)T_s}. \tag{6.15}$$



(a) (b)

Figure 6.9: Waveforms of drive signals and filter input voltage of five-level phase-shifted PWM multilevel inverters. (a) Drive signals for IGBT 1, 2, 3 and 4 (X–axis: Time, 10 μs/div; Y–axis: Magnitude, 5 V/div). (b) Filter input voltage v_{in} (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/div).

Subtracting (6.15) from (6.14), it can be derived that

$$\Delta i_L = \frac{2V_{dc}T_sD(1-D)}{L}. \tag{6.16}$$

Therefore, the maximum inductor current ripple Δi_{Lmax} of bipolar switched inverter is obtained when $D = 0.5$, i.e., $\Delta i_{Lmax} = \frac{V_{dc}T_s}{2L}$.

In the example of the five-level phase-shifted PWM multilevel inverter (see Fig. 6.10), the input voltage frequency is increased to $4f_s$ and the voltage amplitude variation is reduced to $\frac{V_{dc}}{2}$. Hence, the amplitude of the current ripple in the multilevel inverter can be written as

$$\Delta i_L = \frac{V_{dc}T_sD'(1-D')}{4L} \tag{6.17}$$

with $D' = 4D - \text{floor}(4D)$. The maximum value of the ripple amplitude can be derived as $\Delta i_{Lmax} = \frac{V_{dc}T_s}{16L}$. Compared to the bipolar switched inverter, the multilevel inverter has reduced the filter current ripple amplitude by a factor of 8. An inductive filter with much smaller size can be used to suppress the ripple in multilevel inverter.

6.3.4 Small-signal z-domain modelling for switching function

The waveforms in the last switching period in Fig. 6.8 are enlarged and shown in Fig. 6.10. The modulation model can be obtained by describing the small-signal filter input voltage $\widehat{v}_{in}$ as a function of $\widehat{x}^*$. It is shown in Fig. 6.10 that when x^* is changing slowly compared to the carriers, the delay effect can be determined by

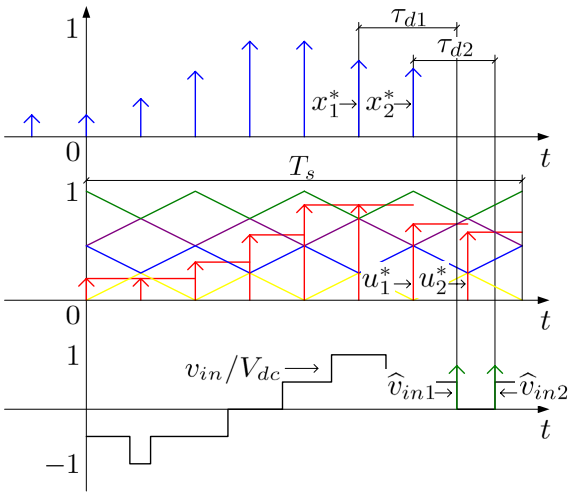
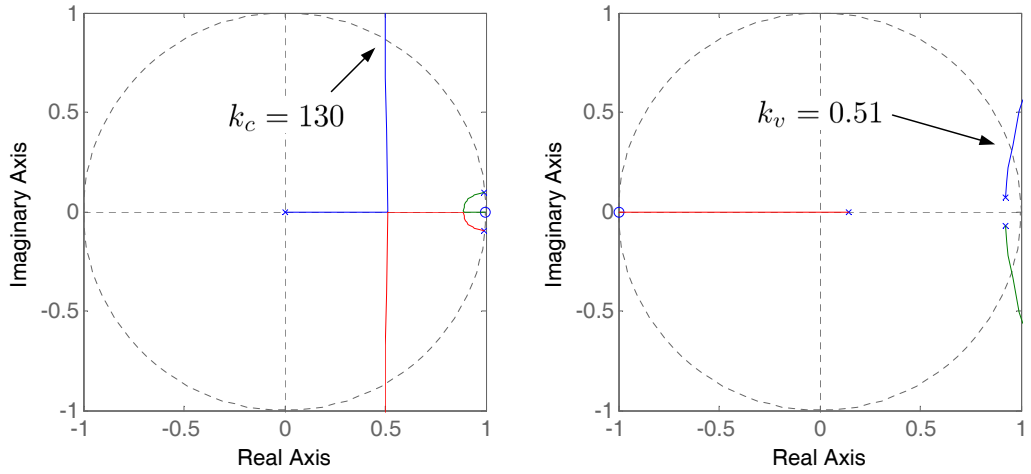


Figure 6.10: Time-domain enlarged view of the equivalent waveforms in phase-shifted PWM multilevel inverters.



(a) (b)

Figure 6.11: Root loci of the control loops. (a) Internal current loop. (b) External voltage loop with $k_c = 16$.

the average duty-ratio D. If the drive signal is generated in the duration of the rising edge of the carriers (e.g. $\widehat{v}_{in1}$), the delay effect is expressed as $e^{-s\tau_{d1}}$, where $\tau_{d1} = \frac{DT_s}{2} - \frac{\text{floor}(ND/2)T_s}{N} + \frac{T_s}{N}$ with the multisampling factor $N = 8$. On the other hand, when the drive signal is generated during the falling edge of the carriers (e.g. $\widehat{v}_{in2}$), the delay effect is written as $e^{-s\tau_{d2}}$, with $\tau_{d2} = \frac{(1-D)T_s}{2} - \frac{\text{floor}(N(1-D)/2)T_s}{N} + \frac{T_s}{N}$.

Since the exact PWM model in the double-update-mode can not be obtained straightforwardly [25], an approximation can be derived by averaging the delay effects and the small-signal transfer function is written as

$$G_{v_{in}x^*}(s) = \frac{V_{dc}T_s}{2N}(e^{-s\tau_{d1}} + e^{-s\tau_{d2}}). \tag{6.18}$$

To obtain the small-signal transfer functions of $G_{i_L^* x^*}(z)$ and $G_{v_o^* x^*}(z)$, the similar theoretical method in the previous section is used. By using the z-transform with the sampling frequency Nf_s, The z-transform of $G_{i_L^* x^*}(z)$ can be written as

$$G_{i_L^* x^*}(z) = \frac{V_{dc}T_s}{2N}\mathcal{Z}\{\frac{s/Le^{-s\tau_{d1}}}{s^2 + sr_L/L + 1/LC} + \frac{s/Le^{-s\tau_{d2}}}{s^2 + sr_L/L + 1/LC}\}, \tag{6.19}$$

and the z-transform result is given as

$$G_{i_L^* x^*}(z) = \frac{V_{dc}T_s z^{-1}}{2N}(\frac{A_i e^{a(\tau_{d1}-2T_s)}}{z - e^{-aT_s}} + \frac{B_i e^{b(\tau_{d1}-2T_s)}}{z - e^{-bT_s}} + \frac{A_i e^{a(\tau_{d2}-2T_s)}}{z - e^{-aT_s}} + \frac{B_i e^{b(\tau_{d2}-2T_s)}}{z - e^{-bT_s}}). \tag{6.20}$$

The transfer function $G_{i_L^* x^*}(z)$ can be written in a short form as

$$G_{i_L^* x^*}(z) = \frac{N_{i1}z + N_{i0}}{z^3 + D_1 z^2 + D_0 z} \tag{6.21}$$

with $N_{i1} = \frac{V_{dc}T_s}{2N}(A_i e^{-a(2T_s-\tau_{d1})} + B_i e^{-b(2T_s-\tau_{d1})} + A_i e^{-a(2T_s-\tau_{d2})} + B_i e^{-b(2T_s-\tau_{d2})})$ and $N_{i0} = -\frac{V_{dc}T_s D_0}{2N}(A_i e^{a(\tau_{d1}-T_s)} + B_i e^{b(\tau_{d1}-T_s)} + A_i e^{a(\tau_{d2}-T_s)} + B_i e^{b(\tau_{d2}-T_s)})$.

Similarly, the transfer function $G_{v_o^* x^*}(z)$ can be derived as

$$G_{v_o^* x^*}(z) = \frac{N_{v1}z + N_{v0}}{z^3 + D_1 z^2 + D_0 z} \tag{6.22}$$

with $N_{v1} = \frac{V_{dc}T_s}{2N}(A_v e^{-a(2T_s-\tau_{d1})} + B_v e^{-b(2T_s-\tau_{d1})} + A_v e^{-a(2T_s-\tau_{d2})} + B_v e^{-b(2T_s-\tau_{d2})})$ and $N_{v0} = -\frac{V_{dc}T_s D_0}{2N}(A_v e^{a(\tau_{d1}-T_s)} + B_v e^{b(\tau_{d1}-T_s)} + A_v e^{a(\tau_{d2}-T_s)} + B_v e^{b(\tau_{d2}-T_s)})$.

Therefore, the closed-loop transfer function from i_{ref}^* to x^* for the multisampled multilevel inverter without feedforward can be written as

$$G_{N1}(z) = \frac{\frac{k_c}{V_{dc}}}{1 + \frac{k_c}{V_{dc}} G_{i_L^* x^*}(z)} \tag{6.23}$$

with the sampling period of T_s/N ($z = e^{sT_s/N}$). The closed-loop transfer function from v_{ref}^* to x^* for the multisampled multilevel inverter without feedforward is

$$G_{N2}(z) = \frac{G_v(z)G_1(z)}{1 + G_v(z)G_1(z)G_{v_o^* x^*}(z)} \tag{6.24}$$

with the sampling period of T_s/N. Based on the closed-loop transfer functions, the root loci of the internal current loop and the external voltage loop are shown in Fig. 6.11. As the sampling frequency is increased, the driving delay becomes significant, which may slightly affect the stability boundaries in the root loci. Hence, according to Fig. 6.11, the proportional gains should be smaller than the boundaries in root loci and are chosen as $k_c = 16$ and $k_v = 0.2$ to ensure stable operation. Higher control gains result in a higher accurate voltage tracking capability. However, the gain k_v is also related to the output impedance. Compared

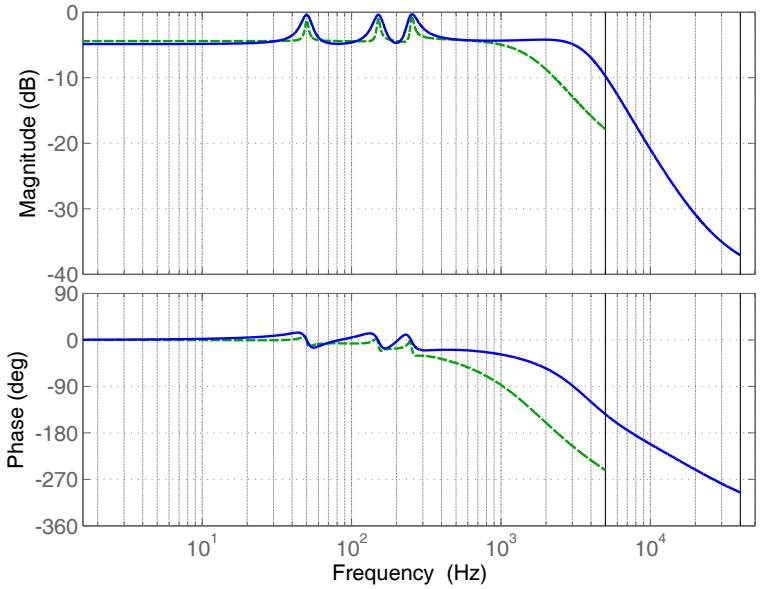


Figure 6.12: Bode diagrams of closed-loop transfer functions (dashed line: bipolar switched inverter; full line: multisampled multilevel inverter).

to the gains of the bipolar switched inverter, much higher feedback gains are achieved and the control performance is improved in the multisampled multilevel inverter. The closed-loop transfer functions describing v_o^* as a function of v_{ref}^* for the two systems are compared. With a heave resistive load ($R = 5\ \Omega$), the bode diagrams of the closed-loop transfer functions are shown in Fig. 6.12. It can be seen from Fig. 6.12 that the closed-loop gain of the multisampled multilevel inverter at selected frequencies is higher than that of the bipolar switched inverter. At the fundamental frequency, the gains of the multisampled multilevel inverter and the bipolar switched inverter are 0.956 and 0.869, respectively. Therefore, the control performance has been improved by the multisampled multilevel inverter. The experimental tests are implemented based on the previous analysis.

6.3.5 Modulation error

Note that the small-signal model (6.18) assumes that there is no vertical crossing during multisampling, in which case the phase-shifted PWM is equivalent to the alternative phase opposition (APO) level-shifted PWM with quadruple-switching frequency. Since the frequency of the level-shifted carriers is half of the sampling frequency, no vertical crossing exists when using the level-shifted modulation. However, when the phase-shifted PWM is applied, the vertical crossing may occur when $D = 0.25$, $D = 0.5$ and $D = 0.75$ where the phase-shifted carriers have intersections. Fig. 6.13 shows the waveforms when vertical crossing occurs at $D = 0.75$. It can be seen that if the intersection of two carriers is between the levels of

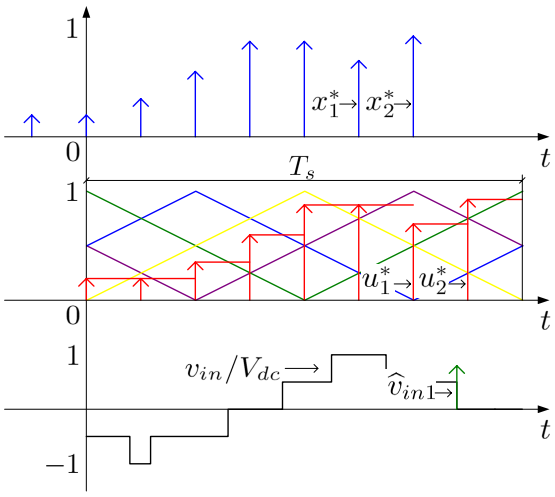


Figure 6.13: Key waveforms of phase-shifted PWM multilevel inverter when vertical crossing occurs.

two adjacent duty-ratios, a vertical crossing appears on one carrier and a double horizontal crossing appears on the other. Therefore, a switching action is missing at that sampling period and the gain of the PWM in small signal becomes zero. As is addressed in [38, 78], the vertical crossing results in a modulation nonlinearity which may affect regulating performance of the digital controller. The number of carriers intersections will significantly increase according to the number of inverters, where more vertical crossing may occur. Hence, the modulation error is a disadvantage existing in the multisampled multilevel inverters which limits the inverters level.

6.4 Simulation results

The simulation of the bipolar switched inverter and multisampled multilevel inverter is preformed in Simulink. The block diagram of the power circuit of the bipolar switched inverter is shown in Fig. 6.14. The digitally controlled system is shown in Fig. 6.15, where the subsystem has been described in Fig. 6.14.

The power circuit of the multisampled multilevel inverter is comprised by two H bridges, as is shown in Fig. 6.16. Based on this topology of multilevel inverter, the block diagram of the digitally controlled multilevel inverter is shown in Fig. 6.17.

The bipolar switched single-phase H bridge inverter and the system with multilevel cascaded H bridge inverters are simulated with the circuit parameters in Table 6.1 and control parameters in the previous section. The highest harmonic order is $h = 5$ and the resonant gain is $k_r = 20k_v$. The reference voltage is given

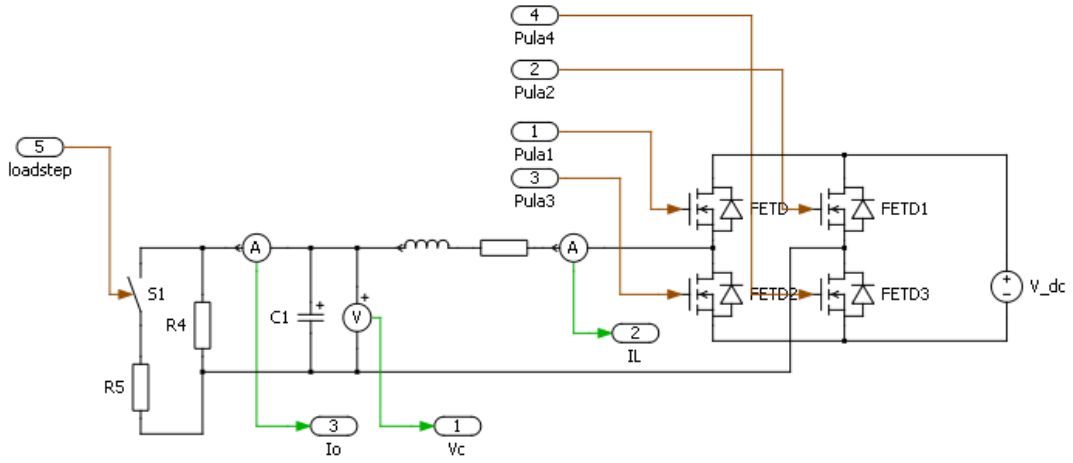


Figure 6.14: Simulink block diagram of the power circuit of the bipolar switched inverter.

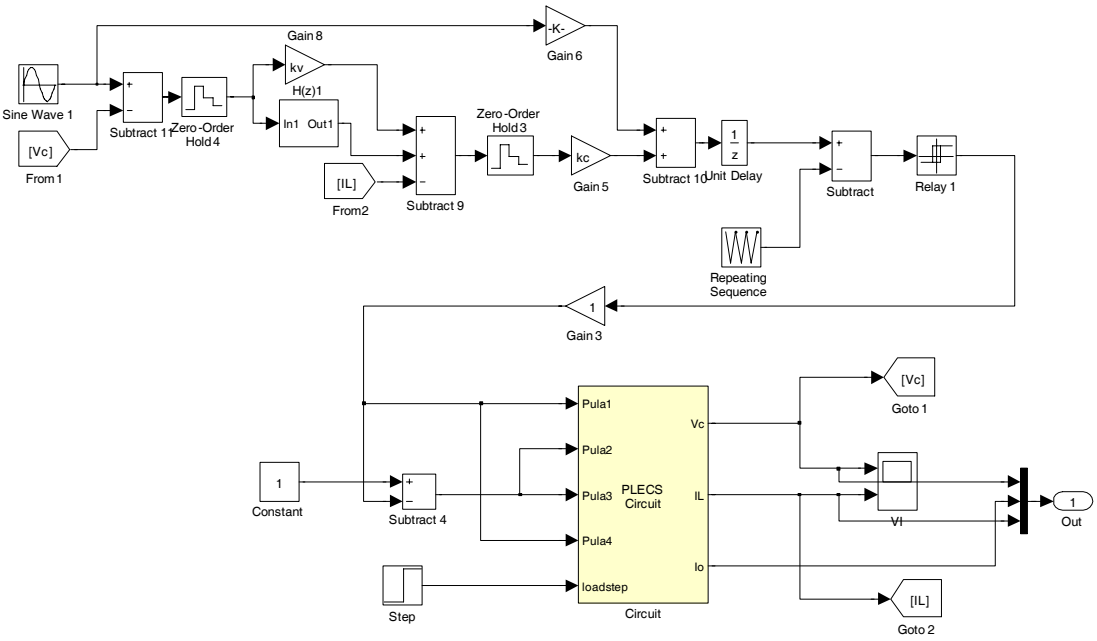


Figure 6.15: Simulink block diagram of the digitally controlled bipolar switched inverter.

as 110 V. The H bridges are driven without deadband in simulation.

Fig. 6.18(a) shows the simulation retrieved waveforms of the output voltage and current of the bipolar switched inverter. As the control gains are low, the output voltage is only 106 V. The inductor current waveform is shown in Fig. 6.18(b). It can be seen from Fig. 6.18(b) that the current contains considerable switching noises with a frequency of 10 kHz. The peak-to-peak value of the inductor current ripple is very high (6.5 A when $D = 0.5$).

When octuple-sampling frequency is used and quadruple filter input voltage

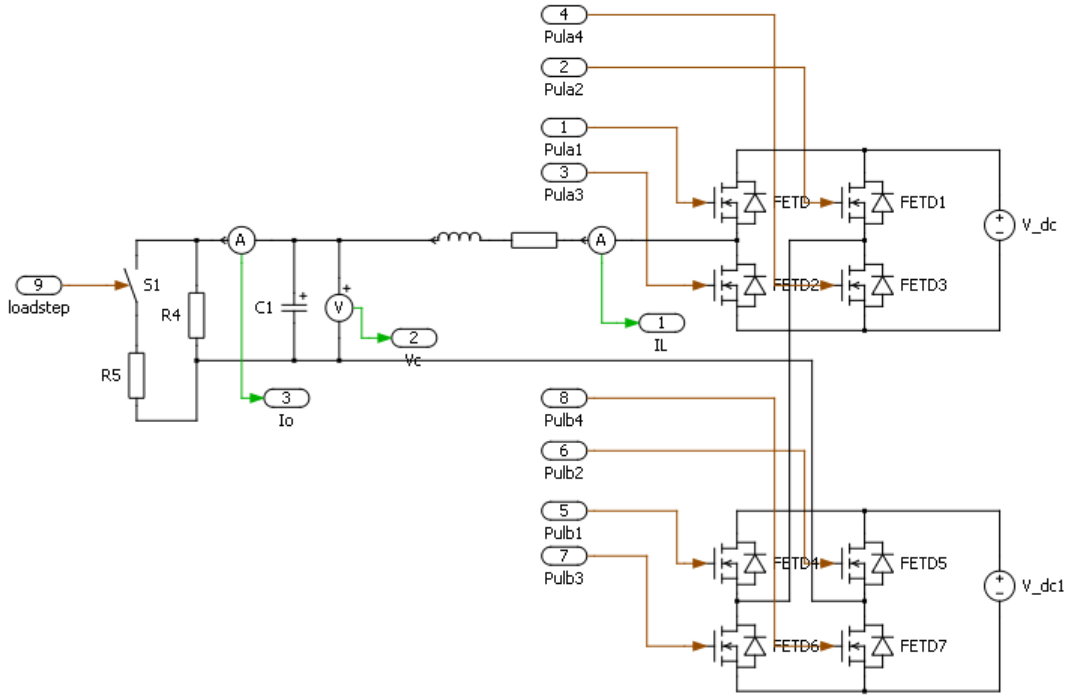


Figure 6.16: Simulink block diagram of the power circuit of the multisampled multilevel inverter.

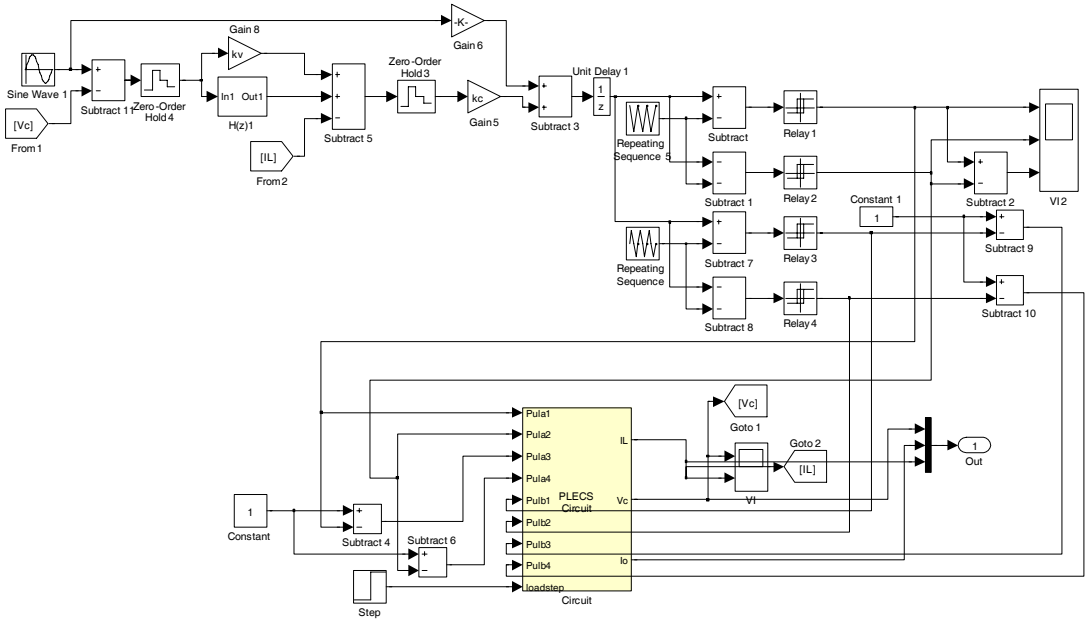


Figure 6.17: Simulink block diagram of the digitally controlled multisampled multilevel inverter.

frequency is achieved for the multilevel inverter, the feedback control gains are quadrupled. Fig. 6.19(a) shows the simulation waveforms of the output voltage and current of the multisampled multilevel inverter. As the control gains are

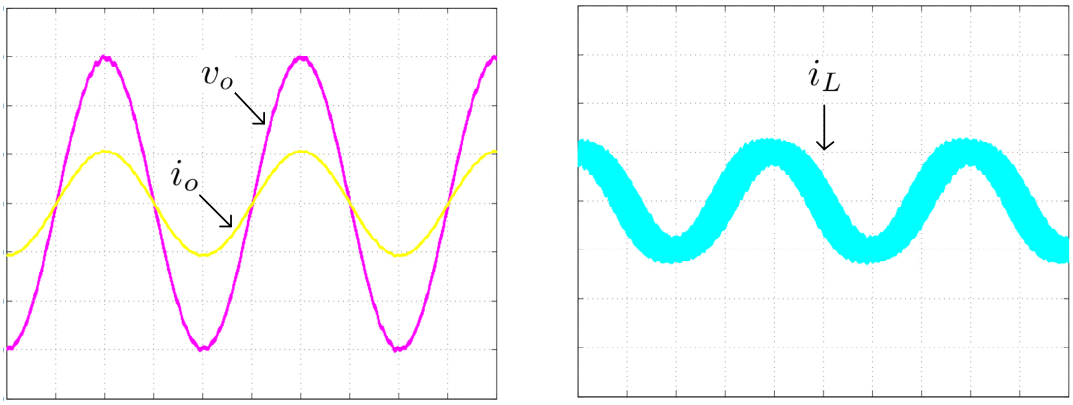


Figure 6.18: Simulation retrieved waveforms of the conventional bipolar switched inverter with a resistive load. (a) Output voltage and output current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/div, 5 A/div). (b) Inductor current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 5.33 A/div).

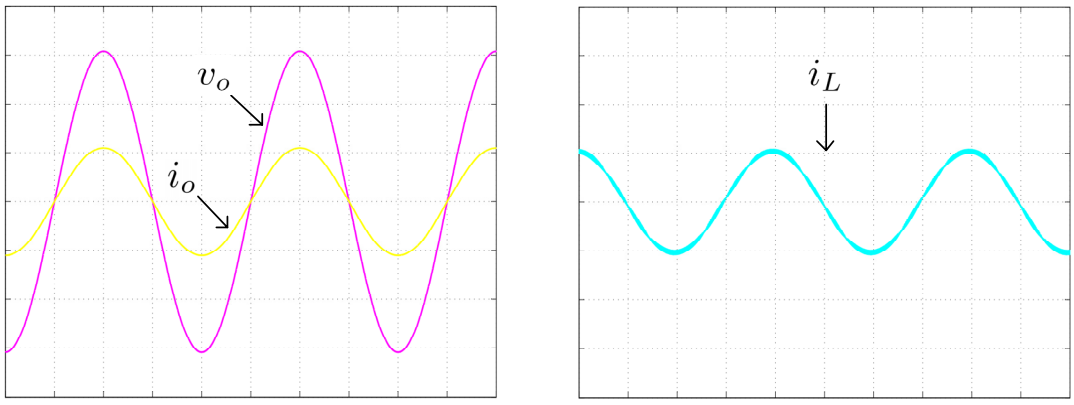


Figure 6.19: Simulation retrieved waveforms of the multisampled multilevel inverter with a resistive load. (a) Output voltage and output current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/div, 5 A/div). (b) Inductor current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 5.33 A/div).

much higher, the control accuracy has been improved and the RMS value of the output voltage is 109 V. The inductor current waveform is shown in Fig. 6.19(b), where the amplitude of the ripple is significantly suppressed (less than 0.4 A) and the frequency is higher (40 kHz). Compared to the bipolar switched inverter, a much better control performance is achieved by the multisampled multilevel inverter.

Fig. 6.20 and Fig. 6.21 shows the transient responses of the bipolar switched inverter and the multilevel inverter, respectively. The resistive load steps from 108 Ω to 21.6 Ω. After the load step of the bipolar switched inverter, the output voltage drops. It takes at least seven line cycles for the output voltage to

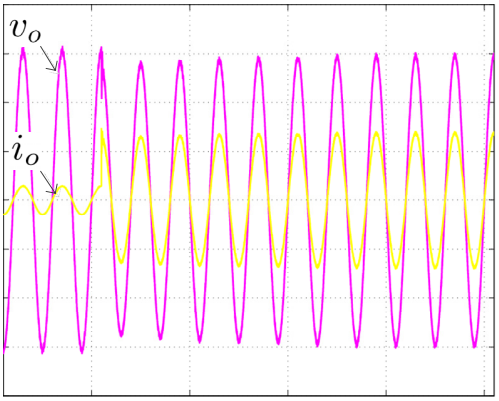


Figure 6.20: Simulation results of dynamic response of the conventional bipolar switched inverter when the load steps (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/div, 5 A/div).

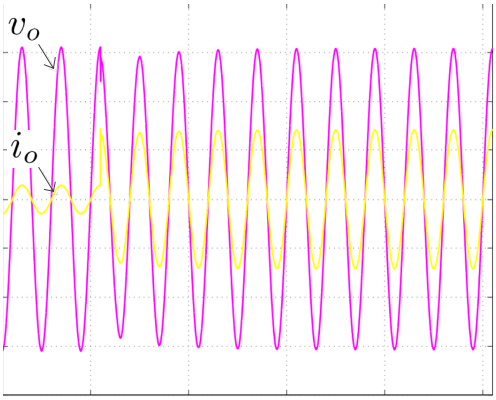


Figure 6.21: Simulation results of dynamic response of the multisampled multilevel inverter when the load steps (X–axis: time, 5 ms/div; Y–axis: magnitude of output voltage, 50 V/div; magnitude of output current, 5 A/div).

achieve steady-state. In contrast, for the multisampled multilevel inverter, the output voltage reaches the steady-state within five line cycles after the load step (see Fig. 6.20). Hence, a much better dynamic performance is achieved by the multisampled multilevel inverter.

6.5 Experimental results

The two digital controllers are experimentally tested in a bipolar switched single-phase H bridge inverter and a multilevel system of cascaded H bridge inverters. The intelligent power modules PM30CSJ060 are used as H bridges with the dead-band of 2.67 μs. The same circuit parameters in Table 6.1 are used and the control parameters are chosen according to the analysis, with the highest harmonic order $h = 5$ and the resonant gain of $k_r = 20k_v$.

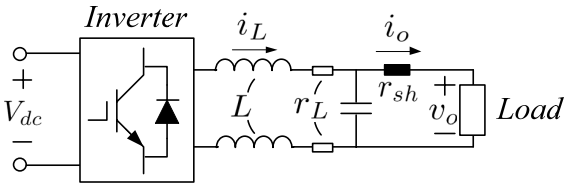
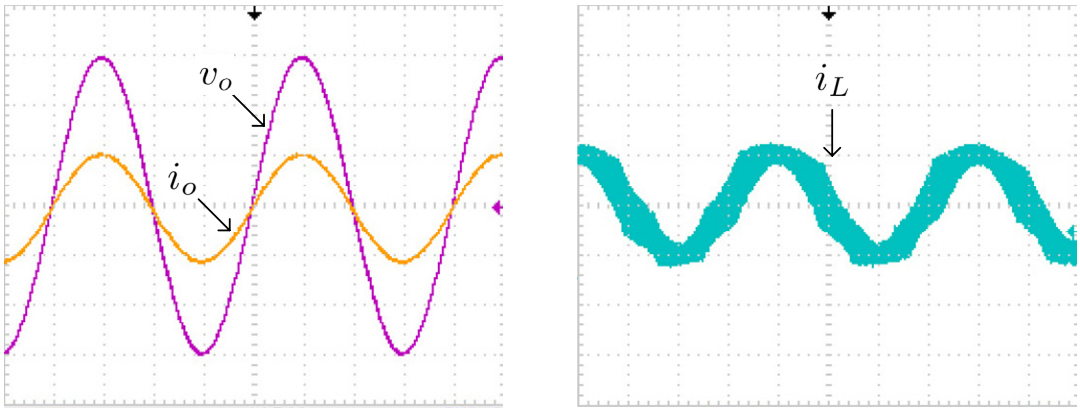


Figure 6.22: Experimental setup of the uniformly-sampled bipolar switched stand-alone inverter.



(a) (b)

Figure 6.23: Experimentally retrieved waveforms of the conventional bipolar switched inverter with a resistive load. (a) Output voltage and output current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/div, 5 A/div). (b) Inductor current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 5.33 A/div).

The experimental setup of the single-phase bipolar switched inverter is shown in Fig. 6.22. A shunt is used to measure the output current. With a reference voltage of 110 V (RMS value), Fig. 6.23(a) shows the experimental waveforms of the output voltage and current of the bipolar switched inverter. As the control gains are limited by the sampling frequency, the measured output voltage is 106 V. The inductor current waveform is measured on the ADC input channel, as is shown in Fig. 6.23(b). It can be seen from Fig. 6.23(b) that the current contains considerable switching noises with a frequency of 10 kHz. The maximum peak-to-peak value of the experimentally measured inductor current ripple is 7.5 A (when $D = 0.5$), where a well designed filter must be used to suppress the switching ripple.

Compared to the bipolar switched inverter, octuple-sampling frequency is used and quadruple filter input voltage frequency is achieved for the multilevel inverter. The feedback control gains are quadrupled. The experimental setup of the multisampled multilevel inverter is shown in Fig. 6.24. Two inverter PCBs are used to implement the system. Fig. 6.25(a) shows the experimental waveforms of the output voltage and current of the multisampled multilevel inverter. As much

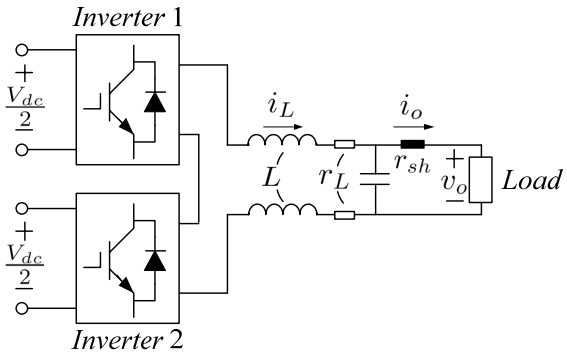
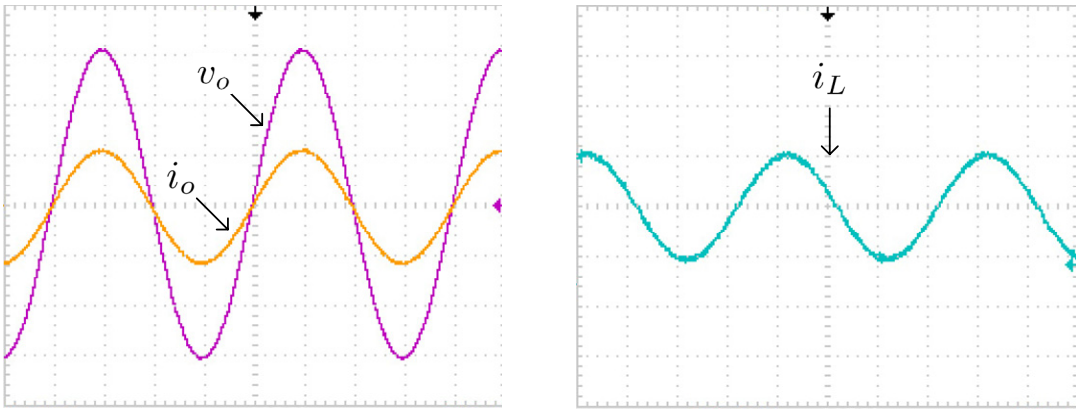


Figure 6.24: Experimental setup of the multisampled multilevel inverter.



(a) (b)

Figure 6.25: Experimentally retrieved waveforms of the multisampled multilevel inverter with a resistive load. (a) Output voltage and output current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/div, 5 A/div). (b) Inductor current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 5.33 A/div).

higher control gains are guaranteed, the control accuracy has been improved and the measured RMS value of the output voltage is 109 V. The inductor current waveform is shown in Fig. 6.25(b), where the ripple is significantly suppressed. The inductor current contains a ripple with a frequency of 40 kHz and a peak-to-peak amplitude less than 1 A. Hence, a much better dynamic performance is achieved by the multisampled multilevel inverter.

The dynamic responses of the bipolar switched inverter and the multisampled multilevel inverter are also compared. The experimental waveforms are retrieved during the transition of a load step. Fig. 6.26 and Fig. 6.27 show the dynamic responses when the load steps from 108 Ω to 21.6 Ω. After the load step of the bipolar switched inverter, the output voltage drops significantly within the first line cycle. The lowest peak value of output voltage is close to 130 V. It takes at least seven line cycles for the output voltage to achieve steady-state. In contrast, the output voltage drop of the multisampled multilevel inverter after

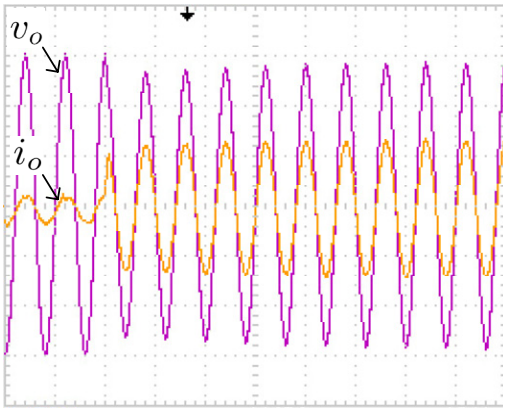


Figure 6.26: Experimental dynamic response of the conventional bipolar switched inverter when the load steps (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/-div, 5 A/div).

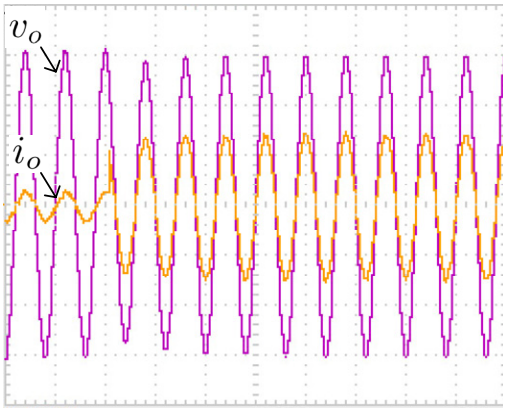
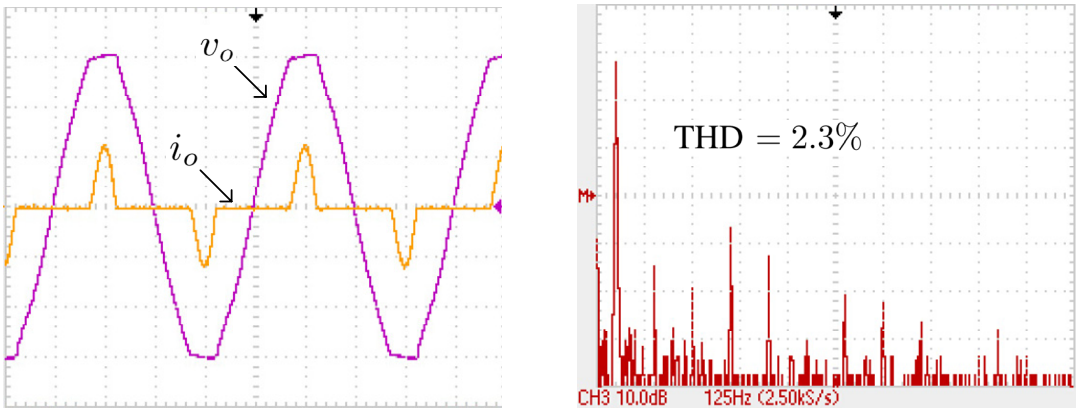


Figure 6.27: Experimental dynamic response of the multisampled multilevel inverter when the load steps (X–axis: time, 5 ms/div; Y–axis: magnitude of output voltage, 50 V/div; magnitude of output current, 5 A/div).

the load step is smaller. The lowest peak value of the output voltage during the transition period is almost 140 V. Moveover, after the load step, the output voltage reaches the steady-state within five line cycles. Hence, a much better dynamic performance is achieved by the multisampled multilevel inverter.

However, there are also some disadvantages of the multisampled multilevel inverters. The deadband is usually mandatorily required by the H bridges. When the number of the levels or the switching frequency increases, the phase-shift time reduces. In that case, the deadband time is no longer negligible and it may introduce considerable modulation error which leads to waveforms distortion. Another drawback of the multisampled multilevel inverters is that the complexity of the control algorithm is limited. As the computation load of the digital controller in our system is almost saturated, the highest harmonic order of the resonant compensator is $h = 5$. When a nonlinear load is connected, the output voltage



(a) (b)

Figure 6.28: Experimental results of the multisampled multilevel inverter with a nonlinear load. (a) Output voltage and output current (X–axis: Time, 5 ms/div; Y–axis: Magnitude, 50 V/div, 5 A/div;). (b) Output voltage FFT result.

distortion is obvious.

Fig. 6.28(a) shows the output voltage and current waveforms of the multisampled multilevel inverter with a nonlinear load connected. The relevant FFT result of the output voltage is shown in Fig. 6.28(b), where the THD is about 2.3%. The THD of the output voltage remains low as long as the current is low. Nevertheless, the current waveshape also differs when different distortion shapes exist on the output voltage. In an environment with a high current injected to the nonlinear load, guaranteeing low output voltage THD without sufficient harmonic compensators is difficult. However, higher proportional feedback gains can provide a low output impedance over a wide frequency range.

6.6 Conclusion

As increasing sampling and switching frequency of switching converters is becoming more and more interesting, switching devices which can afford higher operating frequency are required. There are still practical limitations for switches running at high frequency. However, by using the phase-shifted PWM method in multilevel inverters, the filter current ripple frequency is increased, which allows the controller to achieve better performance. This chapter discusses the digital control of the multisampled multilevel inverter with a comparison to the control of uniformly-sampled bipolar switched inverter. The uniform-sampling is used for the bipolar switched inverter, while the octuple-sampling is used for the five-level inverters system. A standard digital controller with cascaded control loops is applied to the two inverter(s) configurations.

By developing the small-signal transfer function from the duty-ratio to the

filter input voltage, the z-domain model for the multisampled multilevel inverters is theoretically derived. Based on the closed-loop pulse transfer functions of the two systems, the root loci are obtained. The control parameters are chosen according to the root loci. It is shown that the control gains of the multisampled five-level inverter can be increased as quadruple as the gains of the conventional uniformly-sampled bipolar switched inverter. Therefore, a better control accuracy and dynamic performance is achieved. Following on from the theoretically obtained control parameters, the experimental systems are implemented. Experimental results have validated the analysis, showing that the feasibility of employing higher gains to achieve better control performance in multisampled multilevel inverters. Hence, compared to the classic uniformly-sampled inverter, the multisampled multilevel inverter, which keeps the same switching frequency, is an alternative way of effectively implementing higher sampling frequency.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

Three different classes of digitally controlled power inverters in microgrids have been studied and modelled. Based on the proposed z-domain models, the design method for digital controllers of the inverters has been demonstrated.

The fundamentals and state of the art of the digital control of power electronics are introduced first. Modelling methods and control techniques are presented. The thesis focuses on the digitally controlled switching converters with synchronously sampled PWMs. Therefore, the small-signal modelling for uniformly-sampled digital PWMs is presented. The digital PWM models with delays in shadow mode and in immediate mode are developed. These models can be extended to bipolar switched and unipolar switched H bridges. Based on the PWM models, the s-domain block diagrams and z-domain block diagrams for control systems can be obtained. Design methods for the controllers by using the simulation, the root locus and the frequency response are demonstrated. For further validation of the modelling, the simulation software and the experimental arrangement are prepared and described.

The stand-alone inverter with an LC filter and cascaded control loops is modelled in z-domain. Small-signal PWM models are used. By using the z-transform, the internal current control loop is analyzed in z-domain. The z-domain analysis shows that the proportional gain is limited by the product of the filter inductance and the sampling frequency. Using similar method, the z-domain model for the cascaded control loops is obtained. The analysis shows that the proportional gain of the external voltage control loop is also limited. The maximum gain of the external loop is related to the proportional gain of the internal loop. However, it should never exceed the product of the filter capacitance and the sampling frequency. Based on the block diagram of the stand-alone inverter, the design of the controller is implemented. The s-domain analysis can be performed on digi-

tally controlled power inverters. The closed-loop gain and the output impedance can be obtained from the s-domain analysis. To achieve an expected closed-loop gain and the output impedance, new linear control scheme with duty-ratio feedforward has been proposed for parallel inverters in islanding operation mode. In contrast to the classic PR controller, the analysis shows that the proposed controller achieves a better capability of voltage tracking and a lower output THD of voltage. The simulation and experimental comparisons have validated the advantages of the proposed control scheme compared to the conventional PR controller: higher tracking capability and lower THD of the output voltage. Moreover, the proposed control scheme can also be used for other control systems with ac references. Linear controller can be used for either ac voltage control or ac current control since it achieves a high gain with adjustable magnitudes at the fundamental frequency and harmonic frequencies. On the other hand, duty-ratio feedforward is a good method to improve the tracking capability. The combination of linear controller and duty-ratio feedforward may be used for many ac systems.

For grid-connected inverters with LCL filters, many digital control schemes have been proposed. Some controllers only regulate the converter side current, but some controllers have cascaded control loops. Accurate models for these grid-connected inverters are not available. As a result, the design of controllers has to be carefully performed since the LCL resonance may leads to instability problems. Since the high frequency oscillation exists in grid-connected inverters, using classic average models may lead to wrong stability analysis results. Usually, the control parameters are chosen by experience to guarantee stability. Therefore, accurate discrete models are required to predict the stability boundaries. New small-signal z-domain models are proposed for digitally controlled grid-connected inverters with single control loop and cascaded control loops. The modelling of grid-connected inverters with PR controllers is presented. Two control schemes are studied: converter current control scheme and converter current plus grid current control scheme. Different delay effects have been carefully taken into account in the modelling. It shows that when synchronously-sampled triangle carriers are used, there are usually three typical delay times, i.e., half switching period delay, one switching period delay and one and a half periods delay. Based on the possible delays, classic average models and small-signal z-domain models are developed. The frequency responses show that the response of the s-domain models and that of the z-domain models in low frequency range are almost identical. However, big difference exists when the frequency approaches the Nyquist frequency. The s-domain root loci and z-domain root loci are also compared. For the converter current control scheme, the stability boundaries predicted by

s-domain root loci are quite different from the boundaries predicted by z-domain root loci. For the converter current plus grid current control scheme, the stability boundaries predicted by s-domain root loci and by z-domain root loci are almost the same. This is because the instability of the grid current control loop is mainly caused by the resonance of the LCL filter. The analysis also shows that the proportional gain of the converter current control loop should be smaller than the product of the converter side inductance and the sampling frequency. The simulation results have verified that the z-domain models are more accurate in predicting the instabilities compared to the classic average models. Based on the z-domain models, the controller can be designed and the parameters can be selected. The PR controller for the grid-connected inverters are shown as an example. The s-domain models and the z-domain models are used to predict the time-domain waveforms of the grid-connected inverters. Steady-state responses and transient responses are presented. By comparing the models predicted responses to the simulation and experimental results, it reveals that the proposed z-domain models are also capable of predicting the values of control variables at the true sampling instants. Therefore, the proposed new z-domain models are capable of predicting stability, guiding the controller design and predicting steady-state and transient responses.

At last, the multilevel inverters are modelled and compared to the single H bridge inverter. Since the multilevel inverters modulated by level-shifted carriers can be easily modelled using the similar method to that of the bipolar or unipolar switched inverters, the modelling procedure is not shown in that chapter. However, models of multilevel inverters modulated by phase-shifted carriers can be hardly found to date. Therefore, the modelling of multilevel inverters modulated by phase-shifted carriers have been proposed in this thesis. It shows that when phase-shifted carriers are used, the ripple frequency of filter input current is increased. This filter input current is almost equivalent to that of a bipolar switched inverter with a higher switching frequency. Under this condition, the sampling frequency can be increased according to the ripple frequency. By using a higher sampling frequency, a multisampled multilevel inverter can be implemented. The single bridge bipolar switched inverter and the five-level multisampled multilevel inverter are compared. Both inverters use the same switching frequency, but the sampling frequency of the multilevel inverter is eight times of the sampling frequency of the single H bridge inverter. The small-signal transfer function from the duty-ratio to the filter input voltage of the phase-shift PWM multilevel inverter has been derived. The z-domain models for the uniformly-sampled bipolar switched inverter and for the multisampled multilevel inverter are developed. The z-domain analysis shows that the control gains of multisam-

pled multilevel inverter can be quadruple of the gains of the bipolar switched inverter without causing instability problems. As a result, the steady-state and transient performances of the multilevel inverter are better than that of the bipolar switched inverter. Moreover, the analysis shows that the amplitude of the current ripple in the multilevel inverter is reduced by the factor of eight. The EMI of the multilevel inverter is significantly suppressed. The simulation and experimental results are shown to verify the analysis. The steady-state responses and transient responses of both the bipolar switched inverter and the multisampled multilevel inverter are provided, which reveals that the multisampled multilevel inverter achieves better tracking capability and faster dynamic response.

7.2 Future work

Based on the research achievements, various tasks for future work can be done and they are mentioned below.

The previous work focuses on modelling and control of single-phase inverters. This could be extended to three-phase inverters and verified by the relevant experimental work. The modelling and control method for single-phase inverters can be used for sinusoidal PWM based three-phase inverters with control in abc frame or $\alpha\beta$ frame. However, for space-vector PWM based three-phase inverters with control in dq frame, the modelling becomes more complicated. There could be lots of work around the topic of modelling and controller design of the space-vector PWM based three-phase inverters in dq frame. The result can demonstrate whether it is practical to use z-domain analysis for space-vector PWM based three-phase inverters. The result of z-domain analysis may be very complicated, and may not straightforwardly give a design guideline. However, it is worth to undertake the research and find out whether the z-domain analysis is practical under this circumstance.

The parallel inverters and grid-connected inverters in the thesis are all controlled by linear voltage/current controllers with fixed resonant frequencies. This is because the controller cannot afford further computation load when resonant frequencies are adjustable. In practice, the grid frequency is varying all the time. If we use a fixed resonant frequency, the control performance may not be good all the time. To improve the performance of the controller, the resonant frequencies should be changed based on the grid fundamental frequency. The parameters of the resonant controller should be adjusted according to the grid frequency measured by the PLL. In the current experimental system, the processing capability of the DSP is not enough for calculating parameters periodically. However, DSPs with higher processing speed could be used to solve the problem, where

linear controllers with variable resonant frequencies can be implemented in the controller.

There are only two H bridges for the multilevel inverter. The level of the multilevel inverter could be increased, and higher frequency of filter input voltage and higher sampling frequency can be achieved. This can be solved by using controllers comprised of FPGAs and DSPs. The computation can be performed in the FPGA, which could guarantee a short time of the calculation of duty-ratios. When the computation time is quite short compared to the sampling period, more complicated control algorithms can therefore be used to improve the performance of the control. Moreover, increasing the level of the multilevel inverters brings the possibilities of reducing the switching frequency of each switch, which allows high current going through the switching devices without causing low frequency noise in the filter. The high sampling frequency high-level inverters can be experimentally studied, where the modulation error can be observed. Moreover, more interesting applications of multilevel inverters can be developed and tested.

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Appendix A

z-Transforms for Stand-Alone Inverters

The flow chart of the z-transform program for a stand-alone inverter is shown in Fig. A.1.

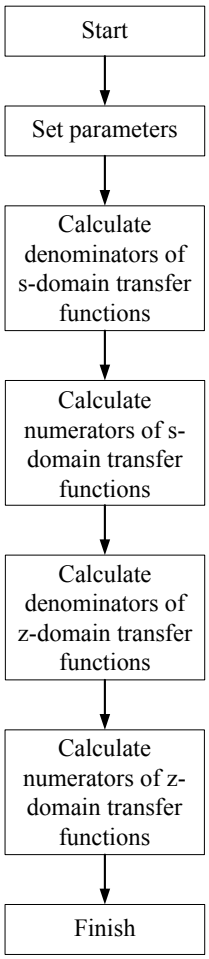

Figure A.1: The flow chart of the program.

The calculation code is shown below.

```
%% z-transforms
clear all;
carrier=2;
Vin=200;
Ts=1/10000;
Tc=1/10000;
L=1.64e-3;
rL=0.4;
rC=0;
C=10e-6;
R=1000;
kesi=0;
Vref=156;
D=100/Vin;
kc=4/200;
kv=00.05;
a=1/2*(1/R/C+(rL+rC)/L...
    +sqrt(1/R^2/C^2-4/L/C+2*(rL+rC)/R/L/C+(rL+rC)^2/L^2));
b=1/2*(1/R/C+(rL+rC)/L...
    -sqrt(1/R^2/C^2-4/L/C+2*(rL+rC)/R/L/C+(rL+rC)^2/L^2));
A=-(1-R*C*a)/(a-b)/L/C/R*Vin;
B=(1-R*C*b)/(a-b)/L/C/R*Vin;
A_1=-1/(a-b)/L/C*Vin;
B_1=1/(a-b)/L/C*Vin;

if carrier==1 %%end of on time
    N1=Ts*(A*exp(a*(kesi+D-1)*Ts)...
        +B*exp(b*(kesi+D-1)*Ts));
    N0=Ts*(-A*exp((a*(kesi+D-1)-b)*Ts)...
        -B*exp(b*(kesi+D-1)-a)*Ts));
    D1=-exp(-a*Ts)-exp(-b*Ts);
    D0=exp(-(a+b)*Ts);
    N1_1=Ts*(A_1*exp(a*(kesi+D-1)*Ts)...
        +B_1*exp(b*(kesi+D-1)*Ts));
    N0_1=Ts*(-A_1*exp((a*(kesi+D-1)-b)*Ts)...
        -B_1*exp(b*(kesi+D-1)-a)*Ts));
end

if carrier==2 %%symmetric on time
    N1=Ts/2*(A*(exp(a*(kesi-D/2-1/2)*Ts)...
        +exp(a*(kesi+D/2-1/2)*Ts))...
        +B*(exp(b*(kesi-D/2-1/2)*Ts)...
        +exp(b*(kesi+D/2-1/2)*Ts)));
    N0=Ts/2*(-A*(exp(a*(kesi-D/2-1/2)*Ts)...
        +exp(a*(kesi+D/2-1/2)*Ts))*exp(-b*Ts)...
```

```
        -B*(exp(b*(kesi-D/2-1/2)*Ts)...
        +exp(b*(kesi+D/2-1/2)*Ts))*exp(-a*Ts));
    D1=-exp(-a*Ts)-exp(-b*Ts);
    D0=exp(-(a+b)*Ts);
    N1_1=Ts/2*(A_1*(exp(a*(kesi-D/2-1/2)*Ts)...
        +exp(a*(kesi+D/2-1/2)*Ts))...
        +B_1*(exp(b*(kesi-D/2-1/2)*Ts)...
        +exp(b*(kesi+D/2-1/2)*Ts)));
    N0_1=Ts/2*(-A_1*(exp(a*(kesi-D/2-1/2)*Ts)...
        +exp(a*(kesi+D/2-1/2)*Ts))*exp(-b*Ts)...
        -B_1*(exp(b*(kesi-D/2-1/2)*Ts)...
        +exp(b*(kesi+D/2-1/2)*Ts))*exp(-a*Ts));

    Nm2=Ts/2*A*exp(a*(kesi+D/2-1/2)*Ts)...
        +Ts/2*B*exp(b*(kesi+D/2-1/2)*Ts);
    Nm1=Ts/2*A*(exp(a*(kesi-D/2-1/2)*Ts)...
        -exp(a*(kesi+D/2-1/2)*Ts)*exp(-b*Ts))...
        +Ts/2*B*(exp(b*(kesi-D/2-1/2)*Ts)...
        -exp(b*(kesi+D/2-1/2)*Ts)*exp(-a*Ts));
    Nm0=-Ts/2*A*exp(a*(kesi-D/2-1/2)*Ts)*exp(-b*Ts)...
        -Ts/2*B*exp(b*(kesi-D/2-1/2)*Ts)*exp(-a*Ts);
    Nm2_1=Ts/2*A_1*exp(a*(kesi+D/2-1/2)*Ts)...
        +Ts/2*B_1*exp(b*(kesi+D/2-1/2)*Ts);
    Nm1_1=Ts/2*A_1*(exp(a*(kesi-D/2-1/2)*Ts)...
        -exp(a*(kesi+D/2-1/2)*Ts)*exp(-b*Ts))...
        +Ts/2*B_1*(exp(b*(kesi-D/2-1/2)*Ts)...
        -exp(b*(kesi+D/2-1/2)*Ts)*exp(-a*Ts));
    Nm0_1=-Ts/2*A_1*exp(a*(kesi-D/2-1/2)*Ts)*exp(-b*Ts)...
        -Ts/2*B_1*exp(b*(kesi-D/2-1/2)*Ts)*exp(-a*Ts);
end
```

Appendix B

z-Transforms for Grid-Connected Inverters

The flow chart of the z-transform program for a grid-connected inverter is shown in Fig. B.1.

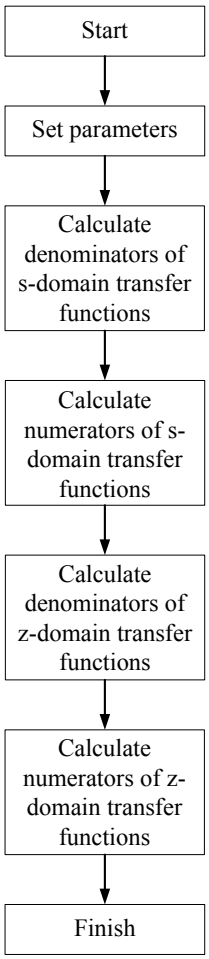

Figure B.1: The flow chart of the program.

The calculation code is shown below.

```
%%
clear all;
carrier=2;
Vin=200;
Vg=155;
Ts=1/20000;
L=1.64e-3;
Lg=1.64e-3;
rL=0.40;
rg=0.40;
C=10e-6;
R=00.0;
D=0.5;
kg=0.5;kr=20;
kL=16/Vin;

%%%          s^2 Lg C + s C (R+rg) + 1      AL        BL        CL
% G_iLd=-----------------------------------=------ + ------ + ------
%%%          fa s3 + fb s2 + fc s + fd      (s+a)     (s+b)     (s+c)

%%%                   s C R + 1             Ag        Bg        Cg
% G_igd=-----------------------------------=------ + ------ + ------
%%%          fa s3 + fb s2 + fc s + fd      (s+a)     (s+b)     (s+c)

fa=L*Lg*C;
fb=C*(Lg*(R+rL)+L*(R+rg);
fc=L+Lg+C*(rL*rg+R*rL+R*rg);
fd=rL+rg;
fQ=(2*fb^3-9*fa*fb*fc+27*fa^2*fd)^2-...
    4*(fb^2-3*fa*fc)^3)^0.5;
fC=(1/2*(fQ+2*fb^3-9*fa*fb*fc+27*fa^2*fd)^(1/3);
a=-(-fb/fa/3-fC/fa/3-(fb^2-3*fa*fc)/fa/fC/3);
b=-(-fb/fa/3+fC*(1+j*3^0.5)/fa/6+...
    (1-j*3^0.5)*(fb^2-3*fa*fc)/fa/fC/6);
c=-(-fb/fa/3+fC*(1-j*3^0.5)/fa/6+...
    (1+j*3^0.5)*(fb^2-3*fa*fc)/fa/fC/6);
AL=Vin*(a^2*Lg*C-a*C*(R+rg)+1)/(a-b)/(a-c)/L/Lg/C;
BL=Vin*(b^2*Lg*C-b*C*(R+rg)+1)/(b-a)/(b-c)/L/Lg/C;
CL=Vin*(c^2*Lg*C-c*C*(R+rg)+1)/(c-b)/(c-a)/L/Lg/C;
Ag=Vin*(1-a*C*R)/(a-b)/(a-c)/L/Lg/C;
Bg=Vin*(1-b*C*R)/(b-a)/(b-c)/L/Lg/C;
Cg=Vin*(1-c*C*R)/(c-b)/(c-a)/L/Lg/C;


if carrier==1 %%end of on time
```

```
    ea=exp(a*(kesi+D-1)*Ts);
    eb=exp(b*(kesi+D-1)*Ts);
    ec=exp(c*(kesi+D-1)*Ts);
    NL2=Ts*(AL*ea+BL*eb+CL*ec);
    NL1=-Ts*(AL*ea*(exp(-b*Ts)+exp(-c*Ts)+...
        BL*eb*(exp(-a*Ts)+exp(-c*Ts)...
        +CL*ec*(exp(-a*Ts)+exp(-b*Ts));
    NL0=Ts*(AL*ea*exp(-(b+c)*Ts)...
        +BL*eb*exp(-(a+c)*Ts)+CL*ec*exp(-(a+b)*Ts);
    D2=-exp(-a*Ts)-exp(-b*Ts)-exp(-c*Ts);
    D1=exp(-(a+b)*Ts)+exp(-(b+c)*Ts)+exp(-(a+c)*Ts);
    D0=-exp(-(a+b+c)*Ts);
    Ng2=Ts*(Ag*ea+Bg*eb+Cg*ec);
    Ng1=-Ts*(Ag*ea*(exp(-b*Ts)+exp(-c*Ts)+...
        Bg*eb*(exp(-a*Ts)+exp(-c*Ts)...
        +Cg*ec*(exp(-a*Ts)+exp(-b*Ts));
    Ng0=Ts*(Ag*ea*exp(-(b+c)*Ts)...
        +Bg*eb*exp(-(a+c)*Ts)+Cg*ec*exp(-(a+b)*Ts);
end



if carrier==2 %%symmetric on time
    ea=(exp(a*(kesi-1/2-D/2)*Ts)...
        +exp(a*(kesi-1/2+D/2)*Ts)/2;
    eb=(exp(b*(kesi-1/2-D/2)*Ts)...
        +exp(b*(kesi-1/2+D/2)*Ts)/2;
    ec=(exp(c*(kesi-1/2-D/2)*Ts)...
        +exp(c*(kesi-1/2+D/2)*Ts)/2;
    ea1=exp(a*(kesi-1/2+D/2)*Ts)/2;
    ea2=exp(a*(kesi-1/2-D/2)*Ts)/2;
    eb1=exp(b*(kesi-1/2+D/2)*Ts)/2;
    eb2=exp(b*(kesi-1/2-D/2)*Ts)/2;
    ec1=exp(c*(kesi-1/2+D/2)*Ts)/2;
    ec2=exp(c*(kesi-1/2-D/2)*Ts)/2;
    D2=-exp(-a*Ts)-exp(-b*Ts)-exp(-c*Ts);
    D1=exp(-(a+b)*Ts)+exp(-(b+c)*Ts)+exp(-(a+c)*Ts);
    D0=-exp(-(a+b+c)*Ts);
    NL2=Ts*(AL*ea+BL*eb+CL*ec);
    NL1=-Ts*(AL*ea*(exp(-b*Ts)+exp(-c*Ts)+...
        BL*eb*(exp(-a*Ts)+exp(-c*Ts)...
        +CL*ec*(exp(-a*Ts)+exp(-b*Ts));
    NL0=Ts*(AL*ea*exp(-(b+c)*Ts)...
        +BL*eb*exp(-(a+c)*Ts)+CL*ec*exp(-(a+b)*Ts);
    Ng2=Ts*(Ag*ea+Bg*eb+Cg*ec);
    Ng1=-Ts*(Ag*ea*(exp(-b*Ts)+exp(-c*Ts)+...
```

```
        Bg*eb*(exp(-a*Ts)+exp(-c*Ts)...
        +Cg*ec*(exp(-a*Ts)+exp(-b*Ts));
    Ng0=Ts*(Ag*ea*exp(-(b+c)*Ts)...
        +Bg*eb*exp(-(a+c)*Ts)+Cg*ec*exp(-(a+b)*Ts);

    NLm2=Ts*(AL*ea1+BL*eb1+CL*ec1);
    NLm1=Ts*(AL*(ea2-ea1*(exp(-b*Ts)+exp(-c*Ts))+...
        BL*(eb2-eb1*(exp(-a*Ts)+exp(-c*Ts))+...
        CL*(ec2-ec1*(exp(-a*Ts)+exp(-b*Ts));
    NLm0=Ts*(AL*(ea1*exp(-(b+c)*Ts)...
        -ea2*(exp(-b*Ts)+exp(-c*Ts))+...
        BL*(eb1*exp(-(a+c)*Ts)...
        -eb2*(exp(-a*Ts)+exp(-c*Ts))+...
        CL*(ec1*exp(-(a+b)*Ts)...
        -ec2*(exp(-a*Ts)+exp(-b*Ts));
    NLm_1=Ts*(AL*ea2*exp(-(b+c)*Ts)...
        +BL*eb2*exp(-(a+c)*Ts)+CL*ec2*exp(-(a+b)*Ts);
    Ngm2=Ts*(Ag*ea1+Bg*eb1+Cg*ec1);
    Ngm1=Ts*(Ag*(ea2-ea1*(exp(-b*Ts)+exp(-c*Ts))+...
        Bg*(eb2-eb1*(exp(-a*Ts)+exp(-c*Ts))+...
        Cg*(ec2-ec1*(exp(-a*Ts)+exp(-b*Ts));
    Ngm0=Ts*(Ag*(ea1*exp(-(b+c)*Ts)...
        -ea2*(exp(-b*Ts)+exp(-c*Ts))+...
        Bg*(eb1*exp(-(a+c)*Ts)...
        -eb2*(exp(-a*Ts)+exp(-c*Ts))+...
        Cg*(ec1*exp(-(a+b)*Ts)...
        -ec2*(exp(-a*Ts)+exp(-b*Ts));
    Ngm_1=Ts*(Ag*ea2*exp(-(b+c)*Ts)...
        +Bg*eb2*exp(-(a+c)*Ts)+Cg*ec2*exp(-(a+b)*Ts);

end

NCRs2=Ts*(Ag+Bg+Cg);
NCRs1=-Ts*(Ag*(exp(-b*Ts)+exp(-c*Ts)+...
    Bg*(exp(-a*Ts)+exp(-c*Ts)...
    +Cg*(exp(-a*Ts)+exp(-b*Ts));
NCRs0=Ts*(Ag*exp(-(b+c)*Ts)...
    +Bg*exp(-(a+c)*Ts)+Cg*exp(-(a+b)*Ts);

NLCs22=Ts*(AL+BL+CL);
NLCs21=-Ts*(AL*(exp(-b*Ts)+exp(-c*Ts)+...
    BL*(exp(-a*Ts)+exp(-c*Ts)...
    +CL*(exp(-a*Ts)+exp(-b*Ts));
NLCs20=Ts*(AL*exp(-(b+c)*Ts)...
    +BL*exp(-(a+c)*Ts)+CL*exp(-(a+b)*Ts);
```

Appendix C

z-Transforms for Multilevel Inverters

The flow chart of the z-transform program for multilevel inverters is shown in Fig. C.1.

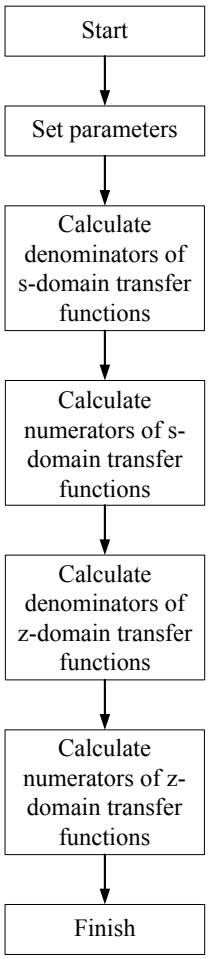

Figure C.1: The flow chart of the program.

The calculation code is shown below.

```
%% 10 kHz sampling
clear all;
carrier=2;
Vin=200;
Ts=1/10000;
Tc=1/10000;
L=1.64e-3;
rL=0.4;
rC=0;
C=10e-6;
R=1000;
Vref=156;
D=100/Vin;
kc=4/200;
kv=00.05;
a=1/2*(1/R/C+(rL+rC)/L...
    +sqrt(1/R^2/C^2-4/L/C+2*(rL+rC)/R/L/C+(rL+rC)^2/L^2));
b=1/2*(1/R/C+(rL+rC)/L...
    -sqrt(1/R^2/C^2-4/L/C+2*(rL+rC)/R/L/C+(rL+rC)^2/L^2));
A=-(1-R*C*a)/(a-b)/L/C/R*Vin;
B=(1-R*C*b)/(a-b)/L/C/R*Vin;
A_1=-1/(a-b)/L/C*Vin;
B_1=1/(a-b)/L/C*Vin;

if carrier==1 %%end of on time
    N1=Ts*(A*exp(a*(kesi+D-1)*Ts)...
        +B*exp(b*(kesi+D-1)*Ts));
    N0=Ts*(-A*exp((a*(kesi+D-1)-b)*Ts)...
        -B*exp((b*(kesi+D-1)-a)*Ts));
    D1=-exp(-a*Ts)-exp(-b*Ts);
    D0=exp(-(a+b)*Ts);
    N1_1=Ts*(A_1*exp(a*(kesi+D-1)*Ts)...
        +B_1*exp(b*(kesi+D-1)*Ts));
    N0_1=Ts*(-A_1*exp((a*(kesi+D-1)-b)*Ts)...
        -B_1*exp((b*(kesi+D-1)-a)*Ts));
end

if carrier==2 %%symmetric on time
    N1=Ts/2*(A*(exp(a*(kesi-D/2-1/2)*Ts)...
        +exp(a*(kesi+D/2-1/2)*Ts))...
        +B*(exp(b*(kesi-D/2-1/2)*Ts)...
        +exp(b*(kesi+D/2-1/2)*Ts)));
    N0=Ts/2*(-A*(exp(a*(kesi-D/2-1/2)*Ts)...
```

```
        +exp(a*(kesi+D/2-1/2)*Ts))*exp(-b*Ts)...
        -B*(exp(b*(kesi-D/2-1/2)*Ts)...
        +exp(b*(kesi+D/2-1/2)*Ts))*exp(-a*Ts));
    D1=-exp(-a*Ts)-exp(-b*Ts);
    D0=exp(-(a+b)*Ts);
    N1_1=Ts/2*(A_1*(exp(a*(kesi-D/2-1/2)*Ts)...
        +exp(a*(kesi+D/2-1/2)*Ts))...
        +B_1*(exp(b*(kesi-D/2-1/2)*Ts)...
        +exp(b*(kesi+D/2-1/2)*Ts)));
    N0_1=Ts/2*(-A_1*(exp(a*(kesi-D/2-1/2)*Ts)...
        +exp(a*(kesi+D/2-1/2)*Ts))*exp(-b*Ts)...
        -B_1*(exp(b*(kesi-D/2-1/2)*Ts)...
        +exp(b*(kesi+D/2-1/2)*Ts))*exp(-a*Ts));

    Nm2=Ts/2*A*exp(a*(kesi+D/2-1/2)*Ts)...
        +Ts/2*B*exp(b*(kesi+D/2-1/2)*Ts);
    Nm1=Ts/2*A*(exp(a*(kesi-D/2-1/2)*Ts)...
        -exp(a*(kesi+D/2-1/2)*Ts)*exp(-b*Ts))...
        +Ts/2*B*(exp(b*(kesi-D/2-1/2)*Ts)...
        -exp(b*(kesi+D/2-1/2)*Ts)*exp(-a*Ts));
    Nm0=-Ts/2*A*exp(a*(kesi-D/2-1/2)*Ts)*exp(-b*Ts)...
        -Ts/2*B*exp(b*(kesi-D/2-1/2)*Ts)*exp(-a*Ts);
    Nm2_1=Ts/2*A_1*exp(a*(kesi+D/2-1/2)*Ts)...
        +Ts/2*B_1*exp(b*(kesi+D/2-1/2)*Ts);
    Nm1_1=Ts/2*A_1*(exp(a*(kesi-D/2-1/2)*Ts)...
        -exp(a*(kesi+D/2-1/2)*Ts)*exp(-b*Ts))...
        +Ts/2*B_1*(exp(b*(kesi-D/2-1/2)*Ts)...
        -exp(b*(kesi+D/2-1/2)*Ts)*exp(-a*Ts));
    Nm0_1=-Ts/2*A_1*exp(a*(kesi-D/2-1/2)*Ts)*exp(-b*Ts)...
        -Ts/2*B_1*exp(b*(kesi-D/2-1/2)*Ts)*exp(-a*Ts);
end
%% 80 kHz sampling
clear all;
carrier=2;
Vin=200;
Ts=1/10000;
Tc=1/10000;
L=1.64e-3;
rL=0.4;
rC=0;
C=10e-6;
R=1000;
Vref=156;
D=175/Vin;
kc=16/200;
kv=00.2;
```

```
a=1/2*(1/R/C+(rL+rC)/L...
     +sqrt(1/R^2/C^2-4/L/C...
     +2*(rL+rC)/R/L/C+(rL+rC)^2/L^2));
b=1/2*(1/R/C+(rL+rC)/L...
     -sqrt(1/R^2/C^2-4/L/C...
     +2*(rL+rC)/R/L/C+(rL+rC)^2/L^2));
A=-(1-R*C*a)/(a-b)/L/C/R*Vin;
B=(1-R*C*b)/(a-b)/L/C/R*Vin;
A_1=-1/(a-b)/L/C*Vin;
B_1=1/(a-b)/L/C*Vin;
% (D-floor(8*D)-1)*Ts/8
% (1-D-floor(8*(1-D))-1)*Ts/8
if carrier==2 %%symmetric on time
     N1=Ts/16*(A*(exp(a*(kesi+(4*D-floor(4*D)-1))*Ts/8)...
          +exp(a*(kesi+(4*(1-D)-floor(4*(1-D))-1))*Ts/8))...
          +B*(exp(b*(kesi+(4*D-floor(4*D)-1))*Ts/8)...
          +exp(b*(kesi+(4*(1-D)-floor(4*(1-D))-1))*Ts/8)));
     N0=Ts/16*(-A*(exp(a*(kesi+(4*D-floor(4*D)-1))*Ts/8)...
          +exp(a*(kesi+(4*(1-D)...
          -floor(4*(1-D))-1))*Ts/8))*exp(-b*Ts/8)...
          -B*(exp(b*(kesi+(4*D-floor(4*D)-1))*Ts/8)...
          +exp(b*(kesi+(4*(1-D)...
          -floor(4*(1-D))-1))*Ts/8))*exp(-a*Ts/8));
     D1=-exp(-a*Ts/8)-exp(-b*Ts/8);
     D0=exp(-(a+b)*Ts/8);
     N1_1=Ts/16*(A_1*(exp(a*(kesi+(4*D-floor(4*D)-1))*Ts/8)...
          +exp(a*(kesi+(4*(1-D)-floor(4*(1-D))-1))*Ts/8))...
          +B_1*(exp(b*(kesi+(4*D-floor(4*D)-1))*Ts/8)...
          +exp(b*(kesi+(4*(1-D)-floor(4*(1-D))-1))*Ts/8)));
     N0_1=Ts/16*(-A_1*(exp(a*(kesi+(4*D-floor(4*D)-1))*Ts/8)...
          +exp(a*(kesi+(4*(1-D)...
          -floor(4*(1-D))-1))*Ts/8))*exp(-b*Ts/8)...
          -B_1*(exp(b*(kesi+(4*D...
          -floor(4*D)-1))*Ts/8)...
          +exp(b*(kesi+(4*(1-D)...
          -floor(4*(1-D))-1))*Ts/8))*exp(-a*Ts/8));
end
```