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A Current-Mode Buck-Boost DC-DC Converter with Fast Transient Response

Andreas Ehrhart, Bernhard Wicht, Ke-Horng Chen

***Abstract*—A fast transient current-mode buck-boost DC-DC converter for portable devices is presented. Running at 1 MHz the converter provides stable 3 V from a 2.7 V to 4.2 V Li-Ion battery. A small voltage under-/overshoot is achieved by fast transient techniques: (1) adaptive pulse skipping (APS) and (2) adaptive compensation capacitance (ACC). The proposed converter was implemented in a 0.25 µm CMOS technology. Load transient simulations confirm the effectiveness of APS and ACC. The improvement in voltage undershoot and response time at light-to-heavy load step (100 mA to 500 mA), are 17 % and 59 %, respectively, in boost mode and 40 % and 49 %, respectively, in buck mode. Similar results are achieved at heavy-to-light load step for overshoot and response time.**

***Index Terms*—DC-DC converter, buck-boost converter, fast transient, adaptive pulse skipping, adaptive compensation capacitance.**

I. Introduction

Nowadays, there are lots of portable devices, such as mobile phones, notebooks, smartphones etc. and the number of them is still increasing. To have a competitive device, it is necessary to provide efficient power management to ensure a long battery life time. Therefore, DC-DC converters are used to power battery-operated portable systems. These converters can provide a constant output voltage (e.g. 3 V). To be able to use the whole battery voltage (e.g. Li-Ion battery with a voltage from 2.7 V to 4.2 V), buck-boost converters get more and more interesting [1]-[4]. To realize three different operation modes, buck, boost and buck-boost, the H-bridge topology of Fig. 1, consisting of switches M_A to M_D, is widely used in the design of buck-boost converters.

Fig. 2 shows the current paths in the different modes. *Path I* and *II* are used in the buck mode and *path III* and *IV* are used in the boost mode. Besides, the signals of the duty cycle *D* and its complement *D'* are shown with the inductor current I_L.

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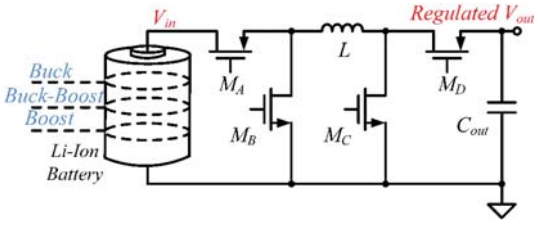

Fig. 1: Topology of the H-bridge buck-boost DC-DC converter.

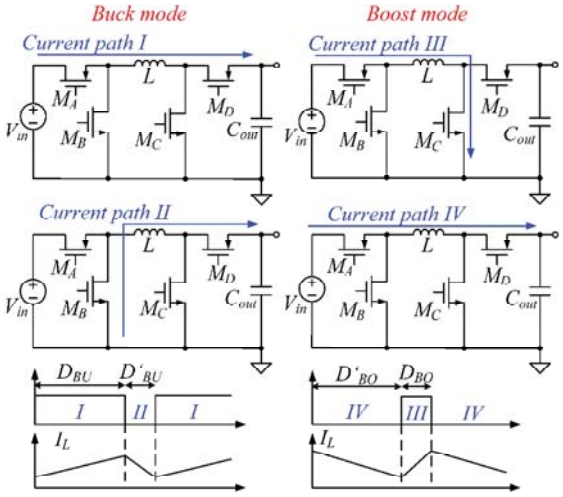

Fig. 2: Current paths and duty cycle in buck and boost mode.

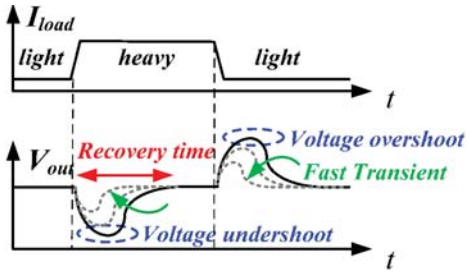

Fig. 3: Output voltage variations at load transition from light-to-heavy and vice versa.

The challenge for buck-boost converters is to have a high-quality and stable power management. For example if the supply voltage might get unstable due to load variations, it might cause abnormal operation or deteriorate the performance of the portable device. Therefore, a good transient response is a critical point of the design specifications. Also, it is necessary to

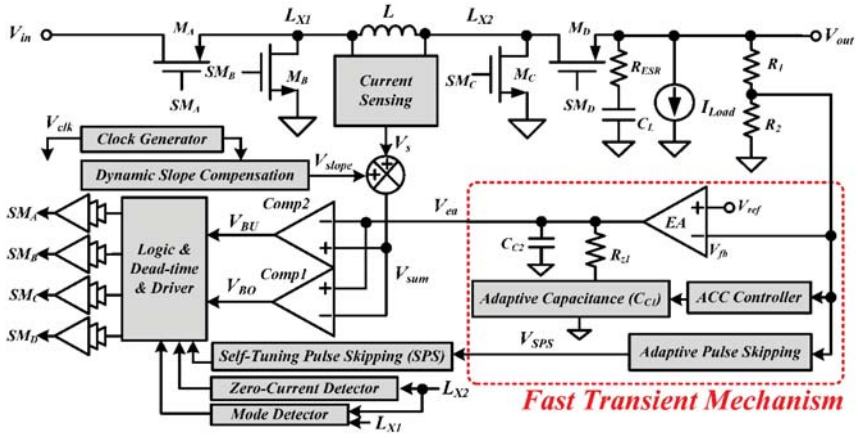

Fig. 4: Structure of the proposed current-mode buck-boost DC-DC converter with APS and ACC.

have a low voltage over-/undershoot at load variations, to improve the transient time.

Fig. 3 shows the effect of a load transition from light-to-heavy load and vice versa. There exist several techniques to improve the transient time, but they are only either for buck or for boost converters [5]-[7]. In buck-boost converters, it is much more complex to achieve fast transient response because the converter can work in three different modes, buck, boost and buck-boost. For each operation mode, the system stability has to be ensured. That means in steady state, the output voltage has to be kept always at its regulated value. Further, if there is a load variation, either from light-to-heavy load or vice versa, the output voltage has to be brought back to its regulated value without causing oscillations.

In [5] and [6], fast transient techniques for buck converters are presented. In these cases, fast transient is reached with an adaptive phase margin (APM) and an adaptive pole-zero position (APZP) technique. The compensation pole-zero pair can be dynamically moved towards high frequencies during transient period. After the output voltage is regulated to its steady-state value, the compensation pole-zero pair is smoothly moved back to the steady-state position. Thus, the overshoot/undershoot voltage can be decreased. Besides, owing to the techniques, the compensation zero is moved to nearly close to the position of the system pole to achieve the pole-zero compensation.

In [7], a fast transient technique for boost converters is presented. This modified hysteretic current control (MHCC) provides the limits for the output voltage. These limits can be adjusted at load changes, to achieve fast transient. Further, the system is able to regulate the output of the error amplifier and provide a good phase margin in steady state. In addition, the compensation technique is also adaptively, with the result that the compensation poles and zeros can be adaptively adjusted in the load transient and steady-state.

In this paper, a current-mode buck-boost DC-DC converter with adaptive pulse skipping (APS) and adaptive compensation capacitance (ACC) is proposed to realize a fast transient response. In Section II, the structure of the proposed converter with the fast transient techniques is described. Section III shows the circuit implementation. Simulation results are presented in Section IV and finally conclusions are made in Section V.

II. Proposed Buck-Boost Converter With Fast Transient Techniques APS And ACC

A. System Overview of the Proposed Converter

Fig. 4 shows the proposed current mode buck-boost converter with the APS and the ACC (red box). The power stage contains four power switches, M_A to M_D, in an H-bridge structure. The feedback resistors, R_1 and R_2, are used to regulate V_{out}. In the feedback loop, a high-gain error amplifier, realized with a cascode high-gain transconductance operational amplifier (OTA) with a single-ended output, generates the error signal V_{ea}. This signal is compared to a summation signal V_{sum} to realize the duty cycles for buck, V_{BU}, and boost, V_{BO}, mode. V_{sum} is the sum of the current-sensing signal V_s and the slope compensation signal V_{slope}. For the slope, the dynamic slope compensation is used to avoid sub-harmonic oscillation. This buck-boost converter utilizes the dual-mode operation, where the peak current control (PCC) and the valley current control (VCC) are used for buck and boost mode, respectively. To ensure a smooth transition between the two modes, a master/slave control scheme is implemented. The master is the traditional mode detector, which compares V_{out} with V_{in}. If $V_{in} < V_{out}$, boost mode is required and if $V_{in} > V_{out}$, buck mode is needed. The slave circuit is used if V_{in} comes close to V_{out}. In that case the self-tuning pulse skipping (SPS) mechanism is applied. The clock generator provides the system clock V_{clk} with 1 MHz. The Zero-Current Detector (ZCD) is used to detect, whether the inductor current I_L is negative. Dead time and driver circuits are implemented in order to control switches M_A to M_D, with the driving signals SM_A to SM_D.

B. Adaptive Pulse Skipping -APS

According to Fig. 2, *path I* and *path II* are used in buck mode and *path III* and *path IV* are used in boost mode. Besides, the signals of the duty cycle D and its complement D' are shown with the inductor current I_L. Self-tuning pulse skipping (SPS) is utilized to extend the effective duty cycle. With the SPS, the duty cycle of the converter cannot be larger than 16.7 %. This value is large enough to ensure a smooth transition, when V_{in} comes close to V_{out} and not too large to unnecessarily enlarge the inductor current and output voltage ripple. But this limit slows down the charging or discharging performance of the inductor. If it would be possible to change the duty cycle to higher values, it could be also possible to charge or discharge the inductor for a longer time. Thereby, the required charge in the inductor can be reached faster.

To realize the adaptive duty cycle in case of load transition, the APS is used. To activate the APS a the feedback signal V_{fb} is compared to a higher and lower limit. If V_{fb} exceeds one of these limits the APS starts. Fig. 5 shows the difference with and without the APS. The main interest of the APS is to vary the duty cycle and its complement, since they control the charge and discharge pulse of the inductor by varying the skipping number of the pulses. Fig. 5 shows that the waveform with APS can reach the required inductor current level faster than the waveform without the APS. The reason is that with the APS, the controller is able to remain the system for a longer time in the charge or discharge path.

Further, ω_{RHP} is dependent of D' in boost mode (1),

$$\omega_{RHP} = \frac{(D')^2 R_L}{L} \text{ with } R_L = \frac{v_{out}}{i_{out}} \qquad (1)$$

which means, with varying the complement of the duty cycle, the ω_{RHP} can be affected. Higher values of ω_{RHP} make the system slower and more stable and lower values make the system faster and improve the transient response. In buck mode, the ω_{RHP} does not occur.

First, there is the load jump from light-to-heavy in boost mode. The pre-defined value of the SPS mechanism is 90 %. With this duty cycle, the system can only remain in the charging path (*path III*) for 10 % of a period T_s. Hence, the controller is not able to vary the duty cycle to remain longer in *path III* and to reach a higher inductor current level faster. When there is the load change, the voltage at the output V_{out} drops down and a voltage controlled current source (VCCS) detects the variation. In that case the SPS signal V_{SPS} changes the effective duty cycle to a value of 60 %. Therefore, the SPS mechanism is able to skip more discharging phases and the inductor can be charged for a longer time. Consequently, more current is stored into the inductor through *path III*. The result is a lower undershoot voltage because ω_{RHP} is brought to lower frequencies and the system is faster. Further, it is possible to reach the required energy level in the inductor faster. Second, if there is a load change from heavy-to-light load, the SPS signal also sets the duty cycle to a value of 60 %. In that case, the skipping number is also higher, so the charging phase of the inductor is skipped and the energy in the inductor is brought to the output. Hence, it is possible to use the energy in the inductor first, before recharging it again. But however, in total D' is shorter and ω_{RHP} is also at low frequencies. The result is a lower overshoot, because the system is fast again. Similarly, there is the load jump from light-to-heavy and heavy-to-light in buck mode.

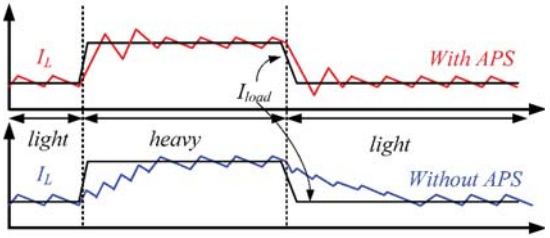

Fig. 5: Effect of the APS on the inductor current.

C. Adaptive Compensation Capacitance - ACC

Current mode regulation is used to get a better line rejection and on-chip system compensation. Therefore, the system compensation is a proportional integral (PI) compensator. This PI compensator has a pole-zero pair, where the ω_{zc1} is used to cancel the load-dependent system pole ω_{p1} located at the output. However, ω_{zc1} affects the performance of the current mode buck-boost converter at different load conditions. The fixed compensation pole-zero pair of the PI compensator can only ensure the system stability but not a good transient response. Therefore, an adaptive compensation is proposed. This requires to analyze the relevant transfer functions of the converter. The control-to-output transfer function (2) of the current mode buck-boost converter has a real pole ω_{p1}, located at the output of the regulator.

$$G_{vc} = \frac{\hat{v}}{\hat{i}_c} = \frac{D'R}{2R_i} \frac{\left(1 - s\frac{L}{(D')^2 DR}\right)(1 + sR_{ESR}C_o)}{\left(1 + s\frac{RC_o}{2}\right)} \qquad (2)$$

$$\omega_{p1} = \frac{2}{RC_o},\ \omega_{z(RHP)} = \frac{(D')^2 R}{L},\ \omega_{z(ESR)} = \frac{1}{R_{ESR}C_o} \qquad (3)$$

The pole ω_{p1}, where C_o is the output filter capacitor and R is the load resistance (3), is proportional to the load current I_{load}. D' is the complement of the duty cycle. R_i is the current sensing gain and R_{ESR} is the equivalent series resistance of C_o. The control-to-output function contains two zeros. One is the right-half-plane zero $\omega_{z(RHP)}$, and the other one is $\omega_{z(ESR)}$.

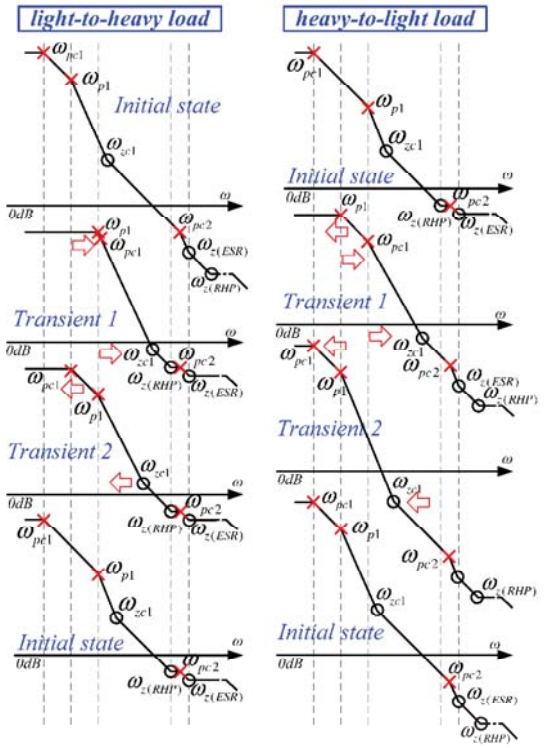

Fig. 6: Compensation poles and zeros with the ACC mechanism and a load change from light-to-heavy and heavy-to-light.

The zero $\omega_{z(RHP)}$ is the critical parameter in boost operation and it is dependent on the load. The zero $\omega_{z(ESR)}$ comes from the output capacitor C_o and it is at high frequencies, which makes it easier to handle than the $\omega_{z(RHP)}$. The transfer function of the PI compensator is

$$G_C(s) = -g_m R_o \frac{1 + sKC_C R_{Z1}}{1 + sKC_C (R_{z1} + R_o)} \quad (4)$$

$$\omega_{pc1} = \frac{1}{KC_C R_o},\ \omega_{zc1} = \frac{1}{KC_C R_{z1}}, KC_C = C_{C1} \quad (5)$$

R_{z1} and C_{C1}, are the on-chip compensation resistor and capacitor, respectively. R_o is the output resistance of the error amplifier and its value is much higher than that of R_{z1}, hence the simplification in (5). G_m is the transconductance of the error amplifier and K is the multiplication factor of the on-chip capacitor. The current generated by the error amplifier can be redirected to charge/discharge the on-chip capacitor C_{C1}. Further, the fast transient mechanism can be realized in case of a load current change [8]. In (4) and (5), the capacitance, which has to be adaptive, can be found. By varying the value of C_{C1}, a good performance can be implemented. Further, a large system bandwidth and an adequate PM are realized at any load condition.

The frequency response can be described in case of a load change with (2), (4) and Fig. 6. When the load current changes from light-to-heavy load, the output pole ω_{p1} moves from lower to higher frequencies. This happens because ω_{p1} is inversely dependent on the load resistance. The RHP zero, $\omega_{z(RHP)}$, is also dependent on the load resistance. With a lower value of the load resistance, $\omega_{z(RHP)}$ is also at lower frequencies. With the first step of the fast transient mechanism the pole-zero pair ω_{pc1} and ω_{zc1} are moved far away from their initial state towards higher frequencies by adjusting the value of the adaptive capacitance C_{C1}. This value is brought, for example, from 400 pF to 4 pF. As a result the unity gain frequency ω_c is also at higher frequencies and the phase margin PM is deteriorated. Thus the system might get unstable, but it improves the transient response because of the small equivalent compensation capacitance and large system bandwidth. To get the system stable again, the second step of the fast transient mechanism gets initiated. In the second step, the pole-zero pair is pulled back to their initial state, by increasing the value of the adaptive capacitance again, so that the ω_c is decreased. Further, the PM is improved again to get the system stable. After the second step is over, the pole-zero pair is brought back to their initial position by setting the value of the adaptive capacitance back to the steady-state value. The pole ω_{pc2} and the zero $\omega_{z(ESR)}$, are not dependent on the load resistance or the adaptive capacitance. Therefore, their position remains always at the same point. The mechanism is similar for the change from heavy-to-light load.

III. Circuit Implementation

For the Adaptive Pulse Skipping (APS) it is necessary to detect the voltage undershoot/overshoot if there is an output load change. Therefore, a voltage controlled current source (VCCS) circuit is used as shown in Fig. 7. This circuit can be used as a suitable differentiator to improve the sensing accuracy and the transient response time. The on-chip capacitor C_d can be kept small because of the current mirror ration k. The output voltage V_{VCCS} of the VCCS is the differentiated value of V_{fb} and it is used to detect the overshoot or undershoot. With this information, a signal for the SPS mechanism can be provided to realize the right SPS value V_{SPS}. At the beginning, V_{fb} is in steady state. If there is a load change, V_{fb} starts to fall or rise. The VCCS detects the change in the V_{fb} signal and the signal V_{VCCS} falls or rises, too. The slope of the V_{VCCS} depends on the change of the V_{fb}. The larger the change in V_{fb}, the larger the slope of the V_{VCCS}. The V_{VCCS} signal is compared to a lower V_{low} and a higher V_{high} limit. If it exceeds one of the limits, the V_{APS} signal is set to high. When V_{APS} is set high, the SPS value is set to a different value, to allow the controller to skip more charging or discharging phases. The value is set to an effective duty cycle of 60 %.

The adaptive compensation capacitance is used to multiply the small on-chip capacitor C_C, Fig. 8. Two modes are possible, first, to multiply the capacitor to an adequate value for system stability in steady state and second, to adjust it to a small value to realize a fast transient response [8].

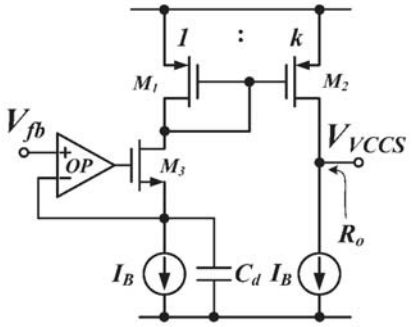

Fig. 7: Schematic of the VCCS.

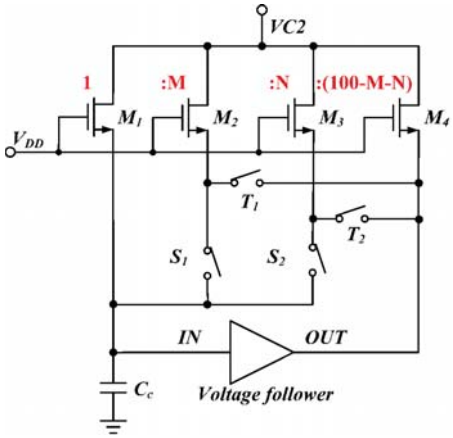

Fig. 8: Compensation Capacitance Multiplier.

In normal operation, the system is in *Steady State*. In that case, switches S_1 and S_2 are off (T_1 and T_2 are on), so that the current cannot flow through the small on-chip capacitor C_C. The current is flowing to the output of the voltage follower, which keeps its input voltage and output voltage at the same level. It is achieved that the small on-chip capacitor is multiplied to an adequate value to stabilize the system. In *Steady State*, the on-chip capacitor is equivalent to an off-chip capacitor, with a larger fixed value. If there is a load change, the fast transient technique gets started and S_1 and S_2 are switched on and T_1 and T_2 are switched off. This state is called the *Transient 1*. Now, it is possible to redirect the current to the output capacitor C_C of the error amplifier, what allows a fast discharge or charge of it. Therefore, the value of the equivalent capacitance is decreased to speed up the transient response. Though, a large current can cause oscillation. Therefore, the *Transient 1* has to have an adequate duration and the current, which is directed to C_C has to be decreased. Simulations showed that a time of 5 µs to 8 µs is enough to get a good transient response without causing oscillations.

After *Transient 1* is over, the mechanism goes into *Transient 2*. In that step, switches S_2 and T_1 are on and S_1 and T_2 are switched off. This results in a lower current, which is directed into the small on-chip capacitor. Thereby, C_C cannot be discharged or charged as fast as in *Transient 1*. This is done, in order to increase the PM and to stabilize the system again, by pulling the compensation zero ω_{zc1} back to its origin state. After V_{out} is brought back to its regulated value, *Transient 2* is over and S_1 and S_2 are off and T_1 and T_2 are on again. Now, the system is in *Steady State* and the equivalent capacitor is at its amplified value.

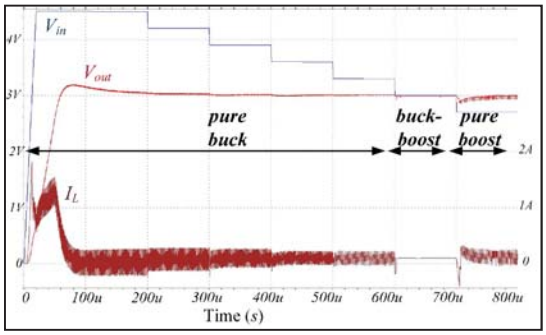

Fig. 9: Input voltage variation from 4.5 V to 2.7 V with an increment of 300 mV @ I_{load} = 100 mA.

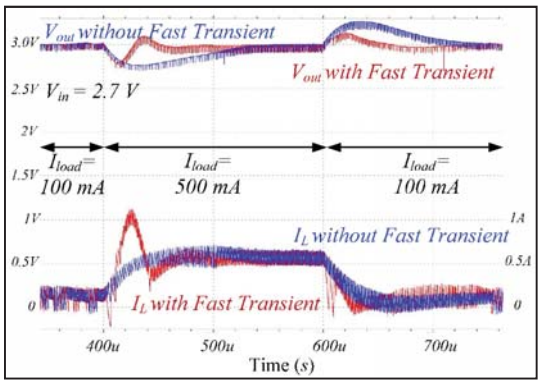

Fig. 10: Load transient (boost), 100 mA to 500 mA and vice versa.

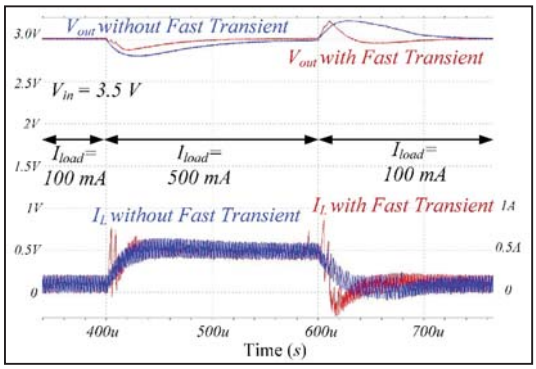

Fig. 11: Load transient (buck), 100 mA to 500 mA and vice versa.

IV. Simulation Results

The proposed fast transient concepts were implemented in a 250 nm CMOS technology for an output voltage of 3 V and a load range of 10 mA to 900 mA at 2.7-4.5 V input. The switching frequency is 1 MHz, the inductor value 2.2 µH and the output capacitor 20 µF with 30 mΩ ESR.

Fig. 9 shows the simulation results at an input voltage variation from 4.5 V to 2.7 V with an increment of

Table 1: Comparison of the performance of the converter, with and without the fast transient techniques

		100mA – 500mA		500mA –100mA	
		ΔV_{out} in mV	Response time	ΔV_{out} in mV	Response time
Boost	FT	200	54 µs	130	59 µs
	no FT	240	131 µs	270	137 µs
Buck	FT	120	94 µs	190	41 µs
	no FT	200	185 µs	220	130 µs
Buck-Boost	FT	180	56 µs	150	69 µs
	no FT	200	155 µs	250	133 µs

300 mV. Fig. 10 and Fig. 11 show the simulation results at a load transient from 100 mA to 500 mA and vice versa in boost and buck mode, respectively. Table 1 shows the comparison of the performances with and without the new fast techniques in the current mode buck-boost DC-DC converter. In boost mode, the improvements, in the voltage undershoot and the response time from light-to-heavy load, are 16.7 % and 58.8 %, respectively. In buck mode the improvements are 40 % and 49.2 % and in buck-boost mode, 10 % and 63.9 %, respectively. The improvements in the voltage overshoot and the response time from heavy-to-light load are, in boost mode, 51.9 % and 56.9 %, in buck mode, 13.6 % and 68.5 % and in buck-boost mode, 40 % and 48.1 %, respectively. The efficiency of the converter is at 60 % at light load (10 mA) and 91 to 95 % at heavy load (50-900 mA). At light load, the efficiency suffers from the switching losses of the power switches M_A to M_D. Obviously, the proposed fast transient mechanism shows better results.

V. CONCLUSIONS

A fast transient current mode buck-boost DC-DC converter with a good power management and a good transient performance is presented to realize a stable supply voltage for portable devices. The critical points in a buck-boost converter are the stability and a constant output voltage. Therefore, the adaptive pulse skipping APS and the adaptive compensation capacitance ACC are proposed as a new fast transient mechanism. Not only the transient response is improved, but also the overshoot/undershoot voltage of V_{out}. Further, the system stability can be ensured by the ACC, due to its adjustable value. Simulation results demonstrated the potential of the fast transient techniques. With the presented fast transient current mode buck-boost DC-DC converter, a solution for an efficient power management was found. This way, it is possible to lower the risk of deteriorations, e.g. unwanted resets, to the powered micro-controller (µC).

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