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Dynamic element matching in digital-to-analog converters with non-linear output resistance

School of Electrical Engineering

Thesis submitted for examination for the degree of Master of Science in Technology.

Espoo 13.02.2017

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ABSTRACT OF THE
MASTER'S THESIS

Author: Muhammad Ammad Siddique

Title: Dynamic element matching in digital-to- analog converters with non-linear output resistance

Date: 13.02.2017 Language: English Number of pages:7+56

Department of Electronics and Nanoengineering

Professorship: Electronic Circuit Design Code: S-87

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This thesis focuses on evaluating the performance of dynamic element matching in digital-to-analog converters, when the unit conversion cells of the converter have finite output resistance. The main goal of this thesis is to see the effect of the non-linearity introduced in the digital-to-analog converter's output, by the finite value of the output resistance and the mismatches in it and to realize if this non-linearity can be corrected by using the DEM encoder.

This thesis considers the tree DEM encoder which is well known, in the literature, to be effective against amplitude and timing mismatches among different conversion cells. The available literature however doesn't consider the impact of finite output resistance. This thesis theorizes that since the DEM encoder scrambles the conversion cell order to correct the non-linearities, it will be ineffective against the output resistance as it is common to all the conversion cells. However, in the presence of output resistance mismatches, which exist between different conversion cells, DEM is again able to shape their non-linearity by scrambling.

This thesis presents three conversion cell models with varying degrees of mismatches among the finite output resistances and derives the corresponding total output current expressions. In addition a MATLAB implementation of the most comprehensive model among the three derived models is also presented.

The MATLAB simulation results show that the non-linearity caused by the output resistance, in the absence of any mismatches, is not shaped by the DEM encoder, however, in the presence of mismatches, the DEM encoder is able to shape the non-linearity. Also evident from the simulation results is that even very high order of mismatch in the output resistance doesn't significantly degrade the performance of the practical system we are using.

Keywords: CMOS, Digital-to-Analog Converter (DAC), Dynamic Element Matching (DEM), Finite Output Resistance, mismatches

Preface

This thesis was carried out in the Electronic Circuit Design group of the Electronics and Nanoengineering Department at the Aalto University, School of Electrical Engineering. The thesis was funded, as part of a larger project, by Huawei Technologies.

I would like to thank Prof. Jussi Ryynänen for giving me the opportunity to work in his research group, D.Sc. Marko Kosunen for all his guidance, insight and humor during the weekly meetings and D.Sc. Kari Stadius for managing everything behind the scenes.

I would also like thank my advisor, M.Sc. Enrico Roverato for his constant and unwavering help and guidance on every step of this thesis and for taking the time to explain some of the most complex concepts. I know it couldn't have been easy. Thanks are also in order for every one at the Electronic Circuit Design group for all their help and interesting coffee time chats.

A special shout out to all the J Team boys for making Finland my home away from home and for keeping me sane with their hang-outs, jokes, awesome trips and cricket and volleyball.

And finally, I would like to thank my family. My deepest and sincerest gratitude goes out to my parents who have always believed in me and made me what I am today. I would also like to thank my brothers for all their help and support.

Otaniemi, January 2016

Muhammad Ammad Siddique

Contents

Symbols and Abbreviations

Symbols

dB	Decibels
$e_{DAC}[n]$	Additive error in the DAC output due to static mismatches
f_N	Nyquist frequency
f_s	Sampling frequency
G_{OFF}	Off Conductance
G_{OFF-n}	Ideal Off Conductance of n sub-cells
G_{OFF-p}	Ideal Off Conductance of p sub-cells
$G_{OFF-nmism}$	Real Off Conductance contributed by n sub-cells
$G_{OFF-pmism}$	Real Off Conductance contributed by p sub-cells
G_{ON}	On Conductance
G_{On-n}	Ideal On Conductance of n sub-cells
G_{On-p}	Ideal On Conductance of p sub-cells
$G_{ON-nmism}$	Real On Conductance contributed by n sub-cells
$G_{ON-pmism}$	Real On Conductance contributed by p sub-cells
I_{LSB}	Current through LSB cell
I^-	Toatl n sub-cell current
I_{out}	Total output current
I^+	Total p sub-cell current
$MM\%$	Percentage mismatch in the conductance
n_M	Number of conversion cells switched to -1
n_p	Number of conversion cells switched to +1
R_o	Output Resistance of digital-to-analog converter
r_o	Output Resistance of conversion cell
R_{OFF}	Off Resistance
R_{ON}	On Resistance
R_L	Load Resistance
$S_{k,r}[n]$	Switching sequence of non-segmenting switching blocks
$S_{k,1}[n]$	Switching sequence of segmenting switching blocks
W_c	Conversion cell weights
ϵ	Static mismatch of 1-bit DACs
σ	Standard deviation of generated mismatch profile

Abbreviations

CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
DEM	Dynamic Element Matching
DNL	Differential Non-Linearity
INL	Integral Non-Linearity

LSB	Least Significant Bit
LTE	Long Term Evolution (Cellular communication standard)
MATLAB	MATrix LABoratory (Software used for modeling of matrix based systems)
MSB	Most Significant Bit
OSR	Over Sampling Ratio
RF	Radio Frequency
RF-DAC	Radio Frequency Digital-to-Analog Converter
RX	Receiver
SB	Switching Block
SFDR	Spurious-Free Dynamic Range
SNR	Signal-to-Noise Ratio

1 Introduction

1.1 Motivation

Modern wireless communication systems have been continuously evolving, moving towards standards that require high data rates and flexibility. This has been fueled by the constant advancements in the CMOS technologies that keep on moving towards smaller transistor sizes. As a result we are moving towards what can be called as the digital RF, where the digital circuits, providing easier implementation of the required high data rates and flexibility and also continuously improving as a result of CMOS scaling are replacing the previously used analog circuits that don't improve with scaling CMOS. A classical example is the use of digital interpolater to replace the baseband filter. This trend also helps in improving the performance of the remaining analog blocks, for example, using DEM encoder to boost the linearity of the DAC. The general trend in modern communication world is to carry out most of the signal processing in the digital part of the system with the analog part being used more for transmission and reception. This evolution has placed more stress on the digital-to-analog converters used as an interface between the digital and the analog worlds. These converters now have tighter constraints placed on their performance and their outputs have to be highly linear, in order to fully utilise the potentials of digital circuits.

The current steering architecture is the most common choice for digital-to-analog converters used in communication systems. Current steering digital-to-analog converters use CMOS transistors for implementing current sources and switches. In this thesis we will restrict ourselves only to the discussion of current steering digital-to-analog converters and hence any conclusions drawn here will only apply to these converters.

One of the main sources of non-linearity in the current steering digital-to-analog converters are the timing, amplitude and output resistance mismatches among the conversion elements. These mismatches occur because in real systems any two identical components will always have random differences among them. These differences arise due to the stochastic nature of the fabrication process [1]. The nature and causes of these mismatches are discussed in detail in literature [2–6]. The timing mismatches occur due to the imperfect synchronization between the switching elements [2, 3]. The amplitude mismatches are caused due to different current levels of the current elements [4] and the output resistance mismatches are due to differences

in the output resistance values of the conversion cells, both switching and current elements [5, 6]. Since, the digital input to the converter determines the selection of the conversion cells, these mismatches result in a non-linearity in the output.

There are a number of methods available to deal with these mismatches [7, 8]. The most common ones are the dynamic element matching (DEM) techniques [9–12]. The basic idea behind these techniques is to switch between the the conversion cells, on a sample-by-sample basis, at a fast enough rate to convert the non-linearity into pseudo random noise. Among these encoding techniques, the tree DEM encoder architecture [11–13], will be considered in this thesis.

There is a lot of literature discussing the ability of the DEM encoders to shape mismatches in the digital-to-analog converters. There is also literature dealing with the output resistance and its mismatches and the non-linearity they cause. However, these two topics are always discussed separately. There is a general lack of literature discussing the impacts of output resistance and its mismatches on the performance of DEM encoders. This thesis is aimed at further discovering this topic. The aim of this thesis is to see the impact of output resistance and its mismatches on the performance of the tree DEM encoder and how much the non-linearity they produce in the output impacts the digital-to-analog converter's performance.

The timing and amplitude mismatches, grouped as static mismatches, by nature exist between different conversion cells. The output resistance, in the absence of mismatches, on the other hand is common for all the conversion cells [14]. As will be discussed in the subsequent chapters, DEM encoding (relying on scrambling the order of the conversion cells) is unable to deal with the non-linearity caused by the output resistance (which is common to all the conversion cells). However, in the presence of output resistance mismatches, which like the static mismatches exist between different conversion cells, DEM is again able to use scrambling to shape their non-linearity. It will also become clear in Chapter 4, that the non-linearity caused by the output resistance and its mismatches doesn't have an adverse impact on our practical system.

1.2 Organisation of the thesis

A brief explanation of the contents of each chapter in the thesis is as follows:

Chapter 2 is focused on the available research in how a finite output resistance and its mismatches cause non-linearity in the DAC output and how a DEM encoder is able to correct the static mismatches but is unable to deal with the non-linearity caused by the the output resistance and its mismatches.

Chapter 3 focuses on the mathematical modeling and analysis of the output resistance and its mismatches. The chapter starts with a simple conversion cell model and continues on to present three different models with varying degrees of finite output resistance and its mismatches. The total output current expressions are

derived for all these models and their implications discussed. Finally, the MATLAB implementation of the most comprehensive model among the derived models, is presented.

Chapter 4 presents the results of the simulations carried out using the MATLAB model. These simulations include INL and output spectra comparison plots, MSB segmentation and statistical INL simulations. The chapter also discusses theses simulation results and their implications.

And finally, Chapter 5 concludes the thesis by summarizing the whole discussion.

2 Background

In this chapter the focus is on the available research pertaining to the output resistance and tree DEM encoders. In section 2.1, we will present a simple overview of the available research on how a finite output resistance causes non-linearity in the DAC output and the effects of this non-linearity. In the section 2.2, there will be a discussion on how the DEM encoder corrects the timing and amplitude non-linearities. Section 2.3 considers the impacts of the output resistance and its mismatches on the DEM encoder.

2.1 Output resistance overview

The output resistance for a digital-to-analog converter is defined as the parallel combination of the output resistances contributed by all the conversion cells that are connected to the output. The number of conversion cells connected to the output is signal-dependent. Fig. 2.1 shows a DAC, for a given arbitrary signal, with k conversion cells connected to output. The output resistances of the individual conversion cells are shown labeled as: r_{Ok}, where k denotes the number of conversion cells connected to output. In this case the total output resistance of the converter, denoted as R_O, is the parallel combination of these k individual conversion cell resistances, given as:

$$R_O \;=\; r_{O1} \parallel r_{O2} \ldots \parallel r_{Ok}$$

The load resistance is also shown in the Fig. 2.1. The internal structure of the conversion cells will be discussed in Chapter 3.

Since we are considering a CMOS implementation in a current steering converter, the output resistance for conversion cells comes down to the contributions from the switching transistors, current source transistors and cascoded transistors(if any). Since the contributions by these transistors are resistive in nature and dominate the output impedance we will limit ourselves to output resistance discussion only. Another reason for limiting ourselves to output resistance is that we are only interested in the behavior at low frequency.

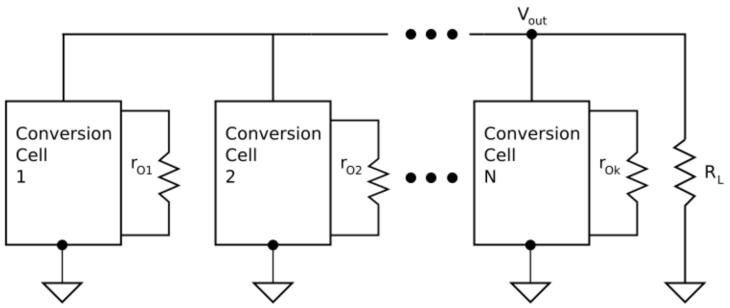


Figure 2.1: DAC with N conversion cells connected to output. Also shown is the load resistance.

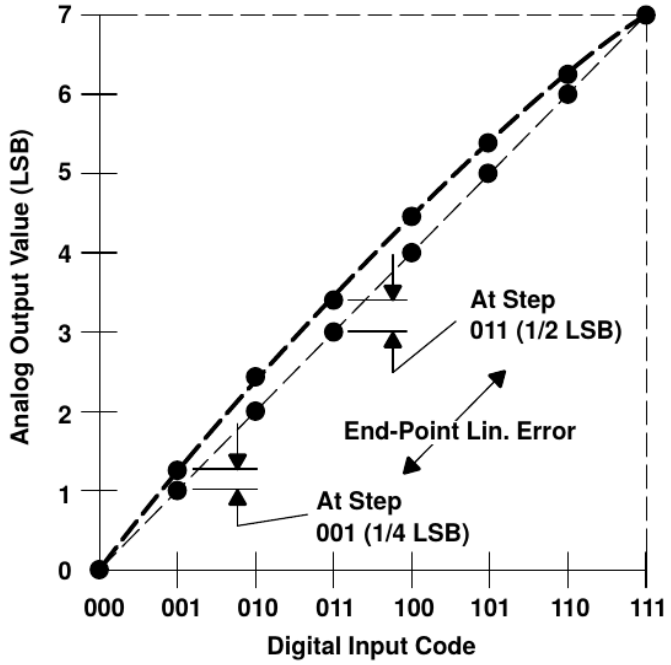


Figure 2.2: INL calculation for a 3-bit binary DAC [15]

The digital-to-analog converters used in modern communication systems have strict restrictions placed on their INL (Integral non-linearity), DNL (Differential non-linearity), SNR (Signal-to-noise ratio) and SFDR (Spurious-free dynamic range) specifications [6]. In order to meet these specifications it is necessary to consider the output resistance requirements for these converters.

INL is defined in [15] as the deviation of the actual converter transfer curve from the best fit straight line. The best fit line can also be replaced by a straight line joining the start and the end points after removing the gain and the offset errors. Fig. 2.2, taken again from [15], shows the graphical representation of INL for a 3-bit binary coded DAC. INL is presented here in terms of LSB.

Depending on the application, practical systems might require investigation of a number of specifications, to ensure proper functionality. However, since our focus

is on the non-linearity caused by the output resistance and the mismatches in it, it is safe to consider INL specifications as the only and sufficient quantitative measure of non-linearity in the output of digital-to-analog converter.

The general idea when designing digital-to-analog converters is to make the output resistance value higher in order to reduce the INL in the output. [5]. The relationship between the maximum INL and the output resistance is given in [16] as:

$$INL_{max} = \frac{I_{LSB} R_L^2 N^2}{4R_o}$$

Where:

I_{LSB} = *Current through LSB cell.*

R_L = *Load resistance.*

N = *Number of unit current sources.*

R_o = *Output resistance.*

Here I_{LSB} and N are used for unary weighted conversion cells. However, they can easily be extended for binary or higher weighted conversion cells since a higher weighted cell, say a cell with weight k, can simply be implemented by a parallel combination of k unary weighted cells.

2.2 DEM encoder overview

Dynamic element matching, as explained earlier, refers to techniques used for converting the non-linearity in the output to pseudo random noise [14]. For this thesis, we will use the tree DEM architecture among the DEM techniques. The tree DEM encoder has been extensively studied in the literature [11–13].

In a typical tree DEM encoder implementation the DAC following the encoder is divided into its 1-bit counterparts, as shown in Fig. 2.3. This is done to ensure that the encoder output is scrambled [11]. Let us consider a general DAC implemented using N 1-bit DACs. The tree DEM encoder in this case produces N 1-bit control signals, denoted as: $c_k[n]$, where k = 1,2,3...N, in Fig. 2.3, with each signal controlling a 1-bit DAC. The use of these single bit control signals allows the encoder to scramble its output from period to period by giving it the flexibility of choosing, pseudo randomly, among the available single bit outputs. This pseudo random choosing converts the non-linearity arising in the output, due to the mismatches among the 1-bit DACs, into pseudo random noise. As shown in Fig. 2.3, the 1-bit DAC outputs are summed together to obtain the final analog output. The number

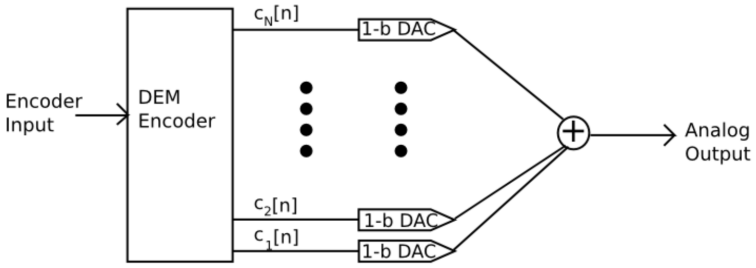


Figure 2.3: A general DAC, made up of N 1-bit DACs, with DEM encoder.

of bits in the general DAC, presented in Fig. 2.3, is not N but rather depends on the encoding scheme implemented by the tree DEM encoder.

The internal structure of a tree DEM encoder consists of switching blocks (SBs) that are arranged into layers. The number of layers and the arrangement of switching blocks depends on the number of bits in the DAC and the encoding scheme used. The most common encoding schemes are binary and thermometer ones while a mixture of these two schemes is possible as well. Depending on the type of the encoding scheme used the switching blocks can be divided into non-segmenting and segmenting types. Non-segmenting switching blocks are used for thermometer encoding DEMs whereas both segmenting and non-segmenting types are used for binary encoding DEMs. DEM encoder for a 3-bit DAC, using thermometer encoding, has been discussed in [12, 13] whereas [17] discusses a 14-bit DAC driven by binary encoded DEM. A general method of designing DEMs for an arbitrary number of DAC bits, using either thermometer or binary encoding is presented in [11]. A hybrid structure for tree DEM encoder, using 10 bit binary encoded LSB and 4 bit thermometer encoded MSB, for a 14 bit DAC is discussed in [9]. For this thesis we will consider the DEM implemented in [14] where a 10-bit DAC is implemented by segmenting the DEM encoder into 4-bit thermometer encoded MSB and 6-bit binary encoded LSB parts. The internal structure of the DEM encoder, taken directly from [14], is presented in Fig. 2.4. The non-segmenting switching blocks are labeled, $S_{k,r}$ where k represents the layer of the block and also the number of bits in the output of the block and r represents the location of block within the layer. The segmenting switching blocks are labeled $S_{k,1}$ with k again representing the layer of the block. The two outputs in segmenting switching blocks do not have the same number of bits. In segmenting switching blocks k represents the number of bits for the output with higher number of bits.

2.2.1 Internal structure of switching blocks

The internal structure and operation of the switching blocks have been thoroughly studied in the above mentioned literature [9,11–14,17]. A simple explanation, based on this literature will be presented here. Fig. 2.5, taken again from [14], presents the internal structure of the switching blocks used in the encoder of Fig. 2.4. The

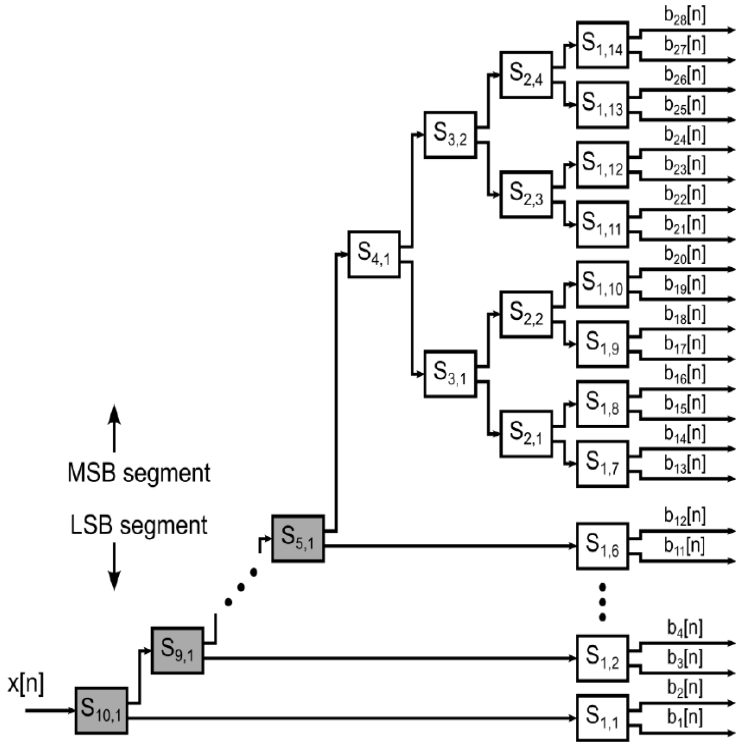


Figure 2.4: Internal structure of tree DEM encoder [14].

$s_{k,r}[n]$ and $s_{k,1}[n]$ are the switching sequences for the non-segmenting and the segmenting switching blocks respectively. These sequences are generated within each switching block and depend on the input to the switching block. These sequences are mathematically given as:

$$s_{k,r}[n] = \begin{cases} 0 & \text{if } x_{k,r}[n] \text{ is even} \\ \pm 1 & \text{if } x_{k,r}[n] \text{ is odd} \end{cases}$$

and

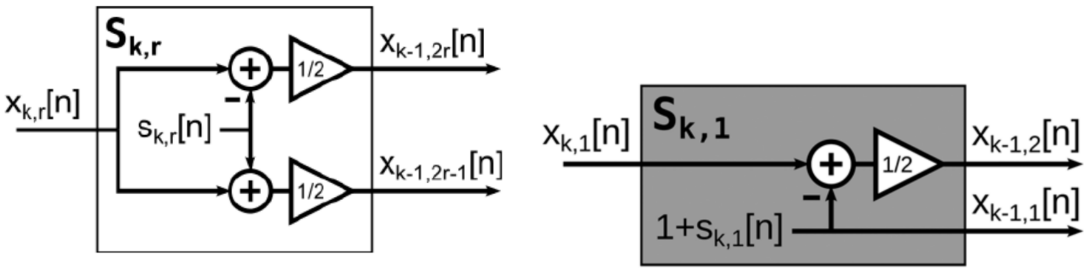
$$s_{k,1}[n] = \begin{cases} 0 & \text{if } x_{k,1}[n] \text{ is odd} \\ \pm 1 & \text{if } x_{k,1}[n] \text{ is even} \end{cases}$$

The actual generation process of switching sequence is out of the scope of this text. The only important thing to note here is that for non-zero outputs the switching sequence can select between two equal magnitude but opposite signed outputs. If the selection is done at a fast enough rate and in a random enough manner the average value will be zero.

The outputs of the non-segmenting switching blocks, from [14] and [12], are:

$$x_{k-1,2r}[n] = \frac{1}{2}\big(x_{k,r}[n] - s_{k,r}[n]\big)$$

$$x_{k-1,2r-1}[n] = \frac{1}{2}\big(x_{k,r}[n] + s_{k,r}[n]\big)$$



(a) non-segmenting (b) segmenting

Figure 2.5: Switching blocks for the DEM encoder [14].

And the outputs of the segmenting switching blocks, from [14] and [9], are:

$$x_{k-1,2}[n] \;=\; \frac{1}{2}\big(x_{k,r}[n] \;-\; 1 \;-\; s_{k,1}[n]\big)$$

$$x_{k-1,1}[n] \;=\; 1 \;+\; s_{k,1}[n]$$

It is clear from the figures and equations above that each switching block has the ability to select between a number of possible output combinations on its two outputs. The selection of these combinations is dictated by the switching sequence generated within each switching block. This constitutes the basic scrambling operation of the DEM encoder, where a fast enough switching sequence makes the average of mismatch errors equal to zero resulting in converting the non-linearity due to mismatches in the digital-to-analog converter into pseudo random noise.

2.2.2 A simple operation example

In order to understand the complete operation of how a DEM encoder converts the non-linearity arising due to static mismatches into pseudo random noise let us consider a simple operation example. This example is taken from [18] and explains intuitively the working of a DEM encoder. Fig. 2.6 presents a 2-bit DAC along with a generic thermometer encoding DEM. This example applies to all the DEM encoders and is not limited only to tree DEM encoding architecture. Hence, the internal structure of DEM encoder in Fig. 2.6 could be any DEM encoding architecture including the switching blocks used for tree DEM case.

The encoder input signal, $x[n]$, can take on three values given as: $[-\Delta,\, 0,\, +\Delta]$. The equations governing different signal values shown on Fig. 2.6 are given below. Starting from encoder outputs:

$$c[n] \;=\; c_1[n]\,,\; c_2[n] = \begin{cases} 0\,0 & \text{if } x[n] \;=\; -\Delta \\ 0\,1 \;\vee\; 1\,0 & \text{if } x[n] \;=\; 0 \\ 1\,1 & \text{if } x[n] \;=\; +\Delta \end{cases}$$

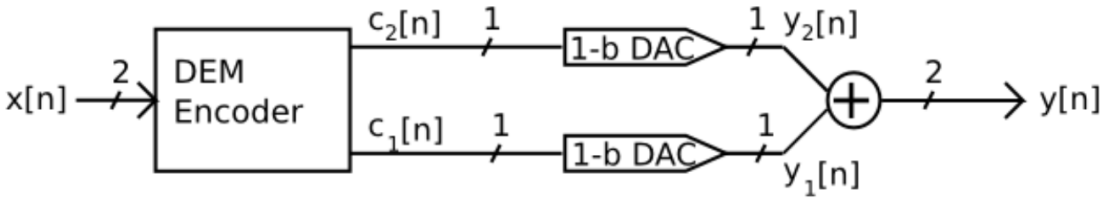


Figure 2.6: 2-bit DAC with a generic DEM encoder [18].

The outputs of 1-bit DACs are:

$$y_1[n] = \begin{cases} -\frac{\Delta}{2} & \text{if } c_1[n] \ = \ 0 \\ +\frac{\Delta}{2} & \text{if } c_1[n] \ = \ 1 \end{cases}$$

And:

$$y_2[n] = \begin{cases} -\frac{\Delta}{2} & \text{if } c_2[n] \ = \ 0 \\ +\frac{\Delta}{2} & \text{if } c_2[n] \ = \ 1 \end{cases}$$

And finally the DAC output is:

$$y[n] \ = \ y_1[n] \ + \ y_2[n]$$

The static mismatches among the 1-b DACs will result in an error term being added to the total DAC output. This additive error term, represented as $e_{DAC}[n]$, is given in [18] as:

$$e_{DAC}[n] = \begin{cases} \epsilon & \text{if } x[n] \ = \ 0 \\ 0 & \text{if } x[n] \ = \ -\Delta \ \vee \ x[n] \ = \ +\Delta \end{cases}$$

Where ϵ is the static mismatch error introduced by the 1-bit DACs. Fig. 2.7, taken again from [18], shows the input and the output plotted against each other. In the Fig. 2.7 input to output conversion is not exact, this difference or error is due to the gain and offset errors. However, since these errors don't cause non-linearity their discussion is not of interest here.

It is clear, from the above mentioned equations and Fig. 2.7, that whenever the input, $x[n]$, is zero the output will have an error ϵ in it. As a result of this error, all the DAC output values don't lie on a straight line, as shown in Fig. 2.7, meaning that the output is non-linear. This mismatch error could either be added or subtracted to the output since the DEM encoder has the option of selecting which of the two 1-bit DACs will be set to high output state. Now if the DEM encoder chooses among the 1-bit DACs, in a pseudo random manner and it does so fast enough that the average output value, for the case of zero input, lies on the straight

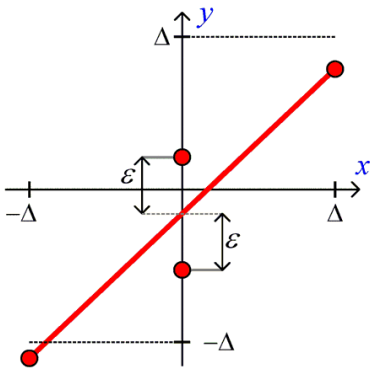


Figure 2.7: Output vs input plot for Fig. 2.6. Image courtesy of [18]

line joining the outputs, the non-linearity in the output will be converted to noise. The concept discussed in this simple example can easily be extended to multibit DACs, as has been done in [9–14, 17].

2.3 DEM encoder with non-linear output resistance

The nature of the non-linearity caused by the output resistance is different from the non-linearity caused by the static mismatches like timing and amplitude mismatches. The difference being that the static mismatches exist between different conversion cells whereas the output resistance exists for all the conversion cells [14].

For the case of a finite value of output resistance without any mismatches, the output resistance will be common to all the conversion cells and hence scrambling the order of the conversion cells will not effect the equivalent output resistance resulting in DEM being ineffective in dealing with the resulting non-linearity.

For the case when there are mismatches in the output resistance, DEM encoder again becomes relevant as scrambling the order of the conversion cells can change the parallel resistance combination resulting in a different value of equivalent output resistance.

3 Analysing and modeling the non-linear output resistance

This chapter is mainly focused on the discussion related to the analysis of non-linear output resistance and its mismatches. In section 3.1, there is a simple explanation of the current steering DAC conversion cell model and some discussion about the non-linearity caused by the output resistance and the mismatches in it. In the section 3.2, three non-linear output resistance models are derived, along with individual output current expressions.These derivations are used to infer the non-linearity, caused by the output resistance and its mismatches, in the output of the digital-to-analog converters. In the section 3.3 two MATLAB models implementing the digital-to-analog converter, with focus on the non-linear output resistance model, are discussed.

3.1 DAC conversion cell model

The simplified internal structure of a current steering digital-to-analog converter, along with a digital encoder is presented in Fig. 3.1. This figure focuses on the structure of the conversion cells that make up the converter. The entire digital-to-analog converter can be obtained by the parallel combination of these conversion cells (as visible from the output node in Fig. 3.1).

The conversion cells are divided into p and n sub-cells. The internal structure of the sub-cells is similar but there can still be mismatches among these similar components, as will be discussed later in the chapter.

The current controlled current source is the basic conversion element in the current steering digital-to-analog converters. These current sources are practically implemented using CMOS transistors and are controlled by means of their respective switches again implemented using CMOS transistors. The current of the source is multiplied by a factor depending on the arbitrary weight (most commonly binary or unary) assigned to each conversion cell. A conversion cell of any weight, lets say, k can be implemented by the parallel combination of a total of k number of conversion cells with each conversion cell being weighted 1.

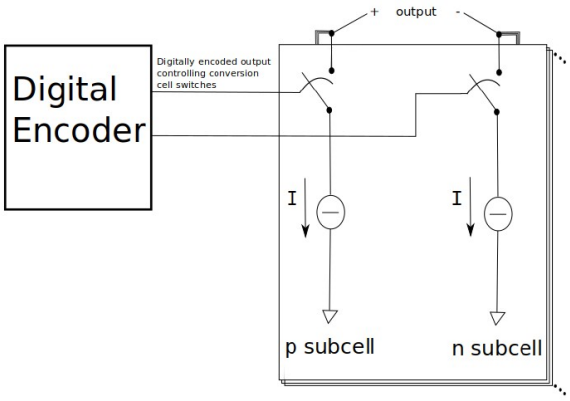


Figure 3.1: Current steering DAC along with an encoder. The internal structure of conversion cells is shown.

It is advisable to use cascode configuration of the current sources, especially in the modern high speed digital-to-analog converters, since such current sources have a higher output resistance. This helps in reducing the INL (integral non-linearity) in the converter output.

Please note that the structure presented in Fig. 3.1 is by no means the only exclusive implementation of conversion cells for current steering digital-to-analog converters. This structure is just a simple and easy to understand implementation and the actual conversion cells can also be implemented with quite a few modifications. For example, the separate current sources in the p and n sub-cells can be merged into a single current source or the position of switches and current sources can be swapped. All these modifications, however don't impact the working principle and basic concepts involved in digital-to-analog converter design and hence any single one of these implementations (including the one in Fig. 3.1) can be studied and analyzed.

The output of the digital encoder block controls the switches of the conversion cells. The digital encoder represented here could implement any encoding scheme, with a division of bits among the binary and thermometer encoding schemes being the most common one in the modern communication systems. The exact decision of encoding scheme depends upon the application, circuit complexity and converter resolution required. Some of the modern multibit digital-to-analog converters however use one of the dynamic element matching (DEM) encoding techniques to enhance their performance and boost linearity.

The digital-to-analog converter used in the scope of this discussion is operating in the fully differential mode only. The conversion cell of a fully differential digital-to-analog converter can only have two output states. These states are high, for when the p sub-cell is conducting and low for when the n sub-cell is conducting. Fig. 3.2 shows these two output states. There is no zero output state, when neither p nor n sub-cells are conducting.

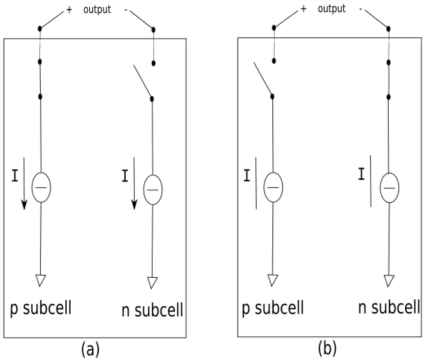


Figure 3.2: Conversion cell output states (a) high and (b) low for a fully differential DAC.

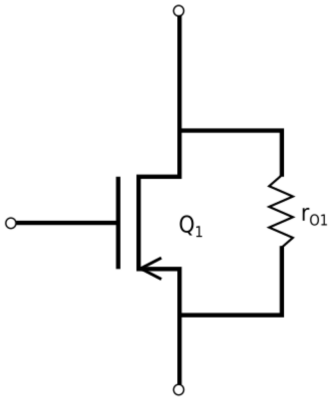


Figure 3.3: Pulling output resistance out of the transistor.

As already discussed, the non-linearity caused in the digital-to-analog converter by the output resistance is not scrambled or corrected by the DEM encoder because the output resistance exists for all the conversion cells and hence can't be corrected by scrambling. We have already had an overview of the available research in how a finite output resistance causes non-linearity in the converter's output and the effects of this non-linearity. In this chapter we will see the practical application of this finite output resistance to the conversion cell model.

We will start with the conversion cell model represented in Fig. 3.1. The easiest way to show the non-linear output resistance in this model is to make use of the "pull resistance out" method. This method is commonly used in literature, for example in [19], especially in the introductory chapters of transistor behavior when the focus is only on the resistance. This helps us in skipping the unwanted intricacies of the small signal models. Such a case is presented in Fig. 3.3, where a NMOS transistor (Q_1) is shown with its output resistance (r_{o1}) pulled out of the transistor. This makes the output resistance easier to visualize and avoids going into unwanted and irrelevant details.

Using the same "pull resistance out" method discussed above, the model in

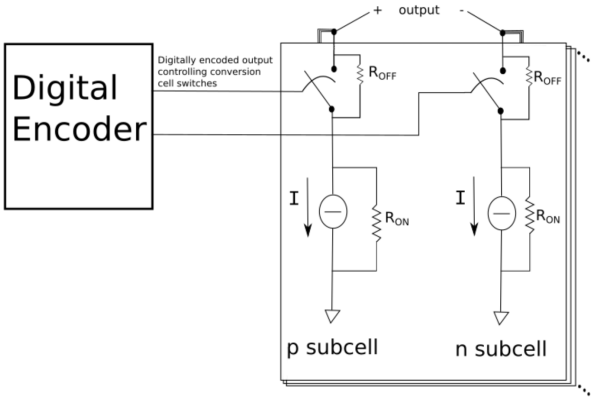


Figure 3.4: DAC conversion cell model with pulled out resistances.

Fig. 3.1 is now modified into the model presented in Fig. 3.4. The output resistance has been divided into two parts, the on resistance, marked as R_{ON} on the model and the off resistance, marked as R_{OFF} on the model. This division has been done for both p and n sub-cells.

This division of output resistance into on and off resistances is carried out to cater for the dependency of the conversion cells on the digital encoder output (input to the conversion cells) which turns the switches on or off. This dependency also explains the non-linear behavior of the output resistance. It is clear from the Fig. 3.4 that for a given sub-cell, R_{OFF} will only contribute to output resistance if the corresponding sub-cell switch is turned off. In the case the switch is turned on, R_{OFF} will be skipped or bypassed. Hence the output resistance changes with change in the input to the conversion cells which necessitates the output resistance division into on and off resistance values.

Splitting the output resistance into on and off resistance also has the added benefit of making the mathematical modeling of the output resistance easier and results in an intuitive and compact expression, as well be shown in the next section.

The model presented in Fig. 3.4 doesn't take into account any mismatches that might occur among the resistances. These mismatches can not only occur among different conversion cells but also among the p and n sub-cells within a single conversion cell. A model that caters for all these mismatches will be presented in the next section.

3.2 Non-linear output resistance models

A total of three different non-linear output resistance models will be presented in this section. The idea here is to start the discussion with quite a simple model operating under the assumption that there is no mismatch among the on and off resistances and deriving the output current expression for this simple model. We

can then move on to more complex models with mismatch among the resistors and deriving their output current expressions. This approach makes derivation process for output current expression more intuitive and also makes moving on to more complex models easier.

3.2.1 No resistance mismatch

The simplest non-linear output resistance model, with no mismatch of any sort among the resistors, is presented in Fig. 3.5. One of the most evident change from the previous discussions is the use of on and off conductances instead of the corresponding resistances. This is done for the sake of simplicity, since it is mathematically much more easier to combine parallel conductances than it is to combine parallel resistances. This results in a compact mathematical expression for the output current as will be evident shortly.

The earlier mentioned point regarding the no resistance (or conductance) mismatch in the model of Fig. 3.5, is evident from the use of single variables, G_{ON} and G_{OFF}, to denote on and off conductances respectively, for all the conversion cells.

The model used above is only meant for a simple performance evaluation, particularly to see the non-linearity caused by the output resistance and its mismatches and hence is by no means an accurate replacement of circuit level simulations. In addition, the model presented in Fig. 3.5, assumes no frequency dependence, which means that the conductances, G_{ON} and G_{OFF}, have only pure conductive behavior regardless of the frequency at which the digital-to-analog converter is operating. These rough performance evaluation and no frequency dependence assumptions also hold true for other models that will be presented in this section.

The model of Fig. 3.5 implements conversion cells that are weighted '1'. However, as already discussed, higher order cells with an arbitrary weight say 'k', can be implemented by the parallel combination of a total of k number of such conversion cells weighted '1'.

The model presented in Fig. 3.5 represents all the conversion cells unlike the model of Fig. 3.4 where the internal structure of a single conversion cell is shown with the output being generated as the parallel combination of all the conversion cells. This necessitates the use of n_P and n_M parameters as defined above. These parameters help us in representing all the conductances of individual conversion cells into four simple values. These four values being the conductances of p and n sub-cells with each sub-cell conductance being further divided into on and off conductances.

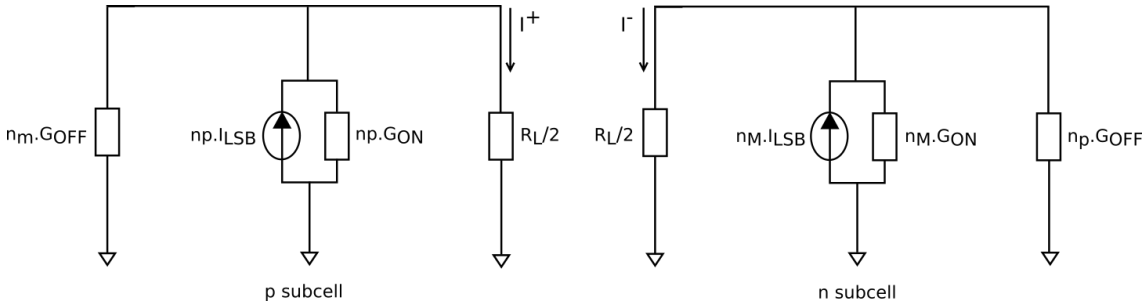


Figure 3.5: Non-linear output resistance model with no resistance mismatch.

Where:

n_P = *Number of conversion cells switched to +1*

n_M = *Number of conversion cells switched to -1*

G_{ON} = *On conductance of a single conversion cell*

G_{OFF} = *Off conductance of a single conversion cell*

R_L = *Load resistance (differential)*

I_{LSB} = *Current through LSB cell*

The total output current is the combination of currents in the p and n sub-cells.

Hence:

$$I_{out} = I^+ - I^-$$

Using the current divider formula sub-cell currents can be found easily. For p sub-cell.

$$I^+ = I_{LSB}.n_P.\left[\frac{1}{n_M G_{OFF}.\frac{R_L}{2} + n_P G_{ON}.\frac{R_L}{2} + 1}\right]$$

and similarly for the n sub-cell we get

$$I^- = I_{LSB}.n_M.\left[\frac{1}{n_P G_{OFF}.\frac{R_L}{2} + n_M G_{ON}.\frac{R_L}{2} + 1}\right]$$

We can simplify the sub-cell currents by substituting:

$$g_{OFF} = \frac{G_{OFF}.R_L}{2} \quad and \quad g_{ON} = \frac{G_{ON}.R_L}{2}$$

This results in sub-cell currents given as:

$$I^{+} = I_{LSB}.n_P.\left[\frac{1}{n_M g_{OFF} + n_P g_{ON} + 1}\right]$$

and

$$I^{-} = I_{LSB}.n_M.\left[\frac{1}{n_P g_{OFF} + n_M g_{ON} + 1}\right]$$

Finally the total output current expression comes out to be:

$$I_{out} = I_{LSB}.\left[\frac{n_P}{n_M g_{OFF} + n_P g_{ON} + 1} - \frac{n_M}{n_P g_{OFF} + n_M g_{ON} + 1}\right]$$

According to the expression derived above the output current depends on the on and off conductances in the p and n sub-cells with the exact values of conductances depending on the number of conversion cells turned to '+1' or '-1', determined by the n_P and n_M parameters. The n_P and n_M are dictated by the input to the digital-to-analog converter and change with each digital input sample. Hence, this dependence of output current on the digital input indicates that there will be a non-linearity in the output.

3.2.2 Resistance mismatch across conversion cells

The model presented in Fig. 3.5 had no conductance (or resistance) mismatches. Lets move on to a more complex model, presented in Fig. 3.6, where conductance mismatches exist among different conversion cells. This means that a given conductance value, G_{ON} or G_{OFF} applies only to a single conversion cell. The G_{ON} and G_{OFF} values of every other conversion cell will not only be different but also unique only to that specific cell.

It must be kept in mind here that the rough performance evaluation and no frequency dependence assumptions applied to the model of Fig. 3.5 also hold true for the model of Fig. 3.6, as has been mentioned earlier. Also true is the fact that higher order arbitrarily weighted conversion cells can be achieved by the parallel combination of conversion cells presented in Fig. 3.6 according to the weight requirements.

Since in the model of Fig. 3.6 there is mismatch among the G_{ON} and G_{OFF} values of different conversion cells, there is a need to modify the four on and off conductances in such a way that in addition to original values (the ones from the

model of Fig. 3.5) we add or subtract the mismatches of those conductances that are being used. For example, if n_M number of p sub-cells are turned off then in addition to the original n_M number of off conductances ($n_M.G_{OFF}$) we also need to add (or subtract) together the mismatches of all these n_M off conductances, mathematically represented as:

$$G_{OFF-pmism} = \sum_{i=1}^{n_M} G_{OFF-mism-i}$$

Where:

$G_{OFF-mism-i}$ = *Mismatch in off conductance of ith off conversion cell*

Similarly for other conductances we can write:

$$G_{ON-pmism} = \sum_{i=1}^{n_P} G_{ON-mism-i}$$

$$G_{ON-nmism} = \sum_{i=1}^{n_M} G_{ON-mism-i}$$

$$G_{OFF-nmism} = \sum_{i=1}^{n_P} G_{OFF-mism-i}$$

Where:

$G_{ON-mism-i}$ = *Mismatch in on conductance of ith on conversion cell*

The mismatches in the conductances could increase or decrease the values of individual conductances which means that the mismatch contribution could be positive or negative and hence it either needs to be added to or subtracted from the original values.

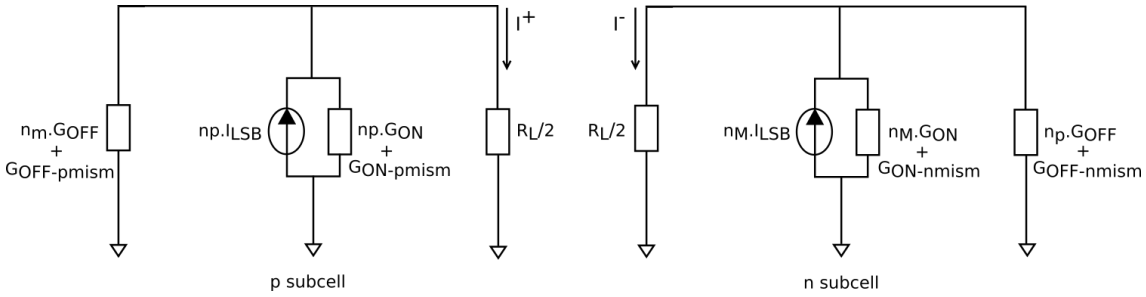


Figure 3.6: Non-linear output resistance model with resistance mismatch among different conversion cells.

Also:

$$G_{OFF-pmism} = \textit{Sum of } G_{OFF} \textit{ mismatches of turned off p sub-cells } (n_M \textit{ such elements})$$

$$G_{ON-pmism} = \textit{Sum of } G_{ON} \textit{ mismatches of turned on p sub-cells } (n_P \textit{ such elements})$$

$$G_{ON-nmism} = \textit{Sum of } G_{ON} \textit{ mismatches of turned on n sub-cells } (n_M \textit{ such elements})$$

$$G_{OFF-nmism} = \textit{Sum of } G_{OFF} \textit{ mismatches of turned off n sub-cells } (n_P \textit{ such elements})$$

The output current equation can now be found out quite easily since the only difference from the previous derivation is the addition to conductance values.

Following the previous procedure and starting with the current divider formula for the sub-cell currents, we get:

$$I^+ = I_{LSB}.n_P.\left[\frac{1}{n_M G_{OFF}.\frac{R_L}{2} + G_{OFF-pmism}.\frac{R_L}{2} + n_P G_{ON}.\frac{R_L}{2} + G_{ON-pmism}.\frac{R_L}{2} + 1}\right]$$

and

$$I^- = I_{LSB}.n_M.\left[\frac{1}{n_P G_{OFF}.\frac{R_L}{2} + G_{OFF-nmism}.\frac{R_L}{2} + n_M G_{ON}.\frac{R_L}{2} + G_{ON-nmism}.\frac{R_L}{2} + 1}\right]$$

Again the sub-cell currents can be simplified by substituting:

$$g_{OFF} = \frac{G_{OFF}.R_L}{2} \quad and \quad g_{ON} = \frac{G_{ON}.R_L}{2}$$

Since the load resistance (R_L) also exists in other terms we will need more substitutions.

These substitutions for p sub-cells are:

$$g_{OFF-pmism} = \frac{G_{OFF-pmism}.R_L}{2} \quad and \quad g_{ON-pmism} = \frac{G_{ON-pmism}.R_L}{2}$$

and for n sub-cells they are:

$$g_{OFF-nmism} = \frac{G_{OFF-nmism}.R_L}{2} \quad and \quad g_{ON-nmism} = \frac{G_{ON-nmism}.R_L}{2}$$

Back plugging these substitutions into the sub-cell current expressions, we get the output current expression given as:

$$I_{out} = I_{LSB}.\left[\frac{n_P}{n_M g_{OFF} + g_{OFF-pmism} + n_P g_{ON} + g_{ON-pmism} + 1} - \frac{n_M}{n_P g_{OFF} + g_{OFF-nmism} + n_M g_{ON} + g_{ON-nmism} + 1}\right]$$

This output current expression is quite similar to the one for the no resistance mismatch case with the only difference being the additional on and off conductance mismatches. These additional conductance mismatches, like the original conductance values, also depend on the exact conversion cells which are turned on or off, governed by the n_P and n_M parameters which in turn depend on the digital-to-analog converter's input.

3.2.3 Mismatch among all resistances

In the model of Fig. 3.6 there was resistance (or conductance) mismatch among the on and off conductances of different conversion cells. The only components without any mismatch were the on and off conductances within a given conversion cell. This means that the G_{ON} and G_{OFF} values were same for both the p and n sub-cells in a single conversion cell. In practise, there can be mismatches among the conductances within a conversion cell. The model of Fig. 3.7 presents this situation.

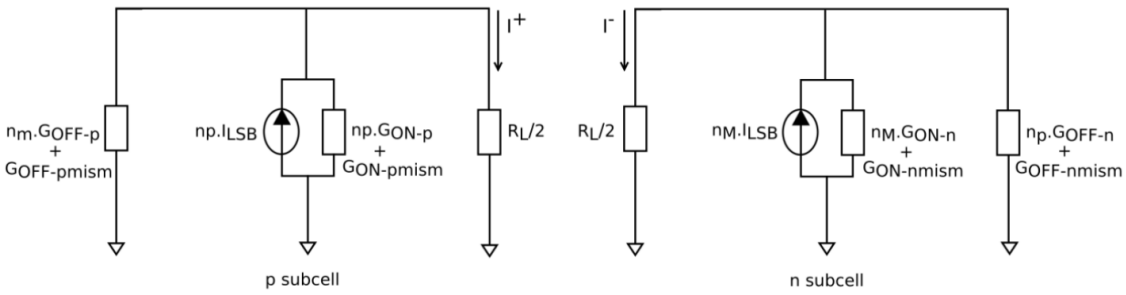


Figure 3.7: Non-linear output resistance model with resistance mismatch among all the conductances.

Where:

G_{OFF-p} = *Off conductance of p sub-cells.*
Ideal value around which the mismatches exist.

G_{ON-p} = *On conductance of p sub-cells.*
Ideal value around which the mismatches exist.

G_{ON-n} = *On conductance of n sub-cells.*
Ideal value around which the mismatches exist.

G_{OFF-n} = *Off conductance of n sub-cells.*
Ideal value around which the mismatches exist.

In addition to the conductance mismatches within a given conversion cell, the model of Fig. 3.7 also implements the mismatches among the conductances of different conversion cells like the model of Fig. 3.6. The model of Fig. 3.7 is thus the most complex mismatch model as it implements mismatches among all the conductances (or resistances) of all the conversion cells.

There is no need to divide the mismatches being added to the above mentioned conductances into p and n sub-cell values, since these mismatches have already been divided into their respective sub-cells because they are a summation based on which exact sub-cells are turned on and off.

The assumptions of rough performance evaluation and no frequency dependence and the ability to implement arbitrarily weighted conversion cells by the parallel combination of unary weighted ones also, naturally, applies here as well.

Moving on to the output current expression derivation, a process quite familiar

to us by now.

The sub-cell currents are given as:

$$I^{+} = I_{LSB}.n_P.\left[\frac{1}{n_M G_{OFF-p}.\frac{R_L}{2} + G_{OFF-pmism}.\frac{R_L}{2} + n_P G_{ON-p}.\frac{R_L}{2} + G_{ON-pmism}.\frac{R_L}{2} + 1}\right]$$

and

$$I^{-} = I_{LSB}.n_M.\left[\frac{1}{n_P G_{OFF-n}.\frac{R_L}{2} + G_{OFF-nmism}.\frac{R_L}{2} + n_M G_{ON-n}.\frac{R_L}{2} + G_{ON-nmism}.\frac{R_L}{2} + 1}\right]$$

Using the substitutions of previous model in addition to the following ones:

$$g_{OFF-p} = \frac{G_{OFF-p}.R_L}{2} \quad and \quad g_{ON-p} = \frac{G_{ON-p}.R_L}{2}$$

and:

$$g_{OFF-n} = \frac{G_{OFF-n}.R_L}{2} \quad and \quad g_{ON-n} = \frac{G_{ON-n}.R_L}{2}$$

The output current expression comes out to be:

$$I_{out} = I_{LSB}.\left[\frac{n_P}{n_M g_{OFF-p} + g_{OFF-pmism} + n_P g_{ON-p} + g_{ON-pmism} + 1} - \frac{n_M}{n_P g_{OFF-n} + g_{OFF-nmism} + n_M g_{ON-n} + g_{ON-nmism} + 1}\right]$$

The non-linearity in the output can easily be inferred using arguments used in the previous models. The only difference is the different values of off and on conductances for sub-cells.

3.3 MATLAB model

MATLAB was used to model the digital-to-analog converter, with the main implementation focus being on the non-linearity caused by the output resistance and its mismatches. The exact implementation architecture of the converter will be discussed in a subsequent subsection.

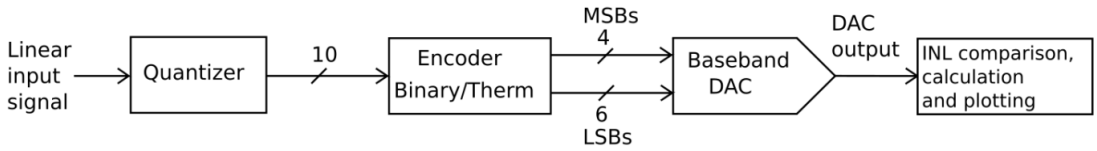


Figure 3.8: Block diagram of MATLAB implemented system for INL comparison.

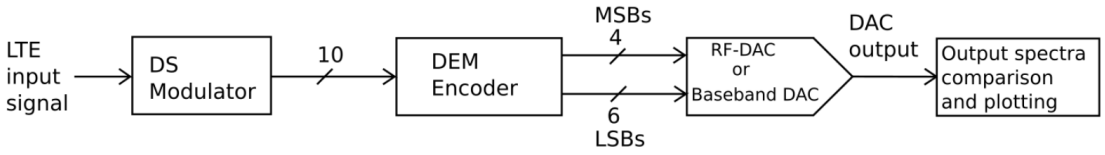


Figure 3.9: Block diagram of MATLAB implemented system for output spectra comparison.

The digital-to-analog converter model was used in two different systems for obtaining INL and output spectra comparison plots. The block diagram of these implemented systems have been presented in Fig. 3.8 and Fig. 3.9. The idea here is to use different real and ideal values for output resistance and its mismatches and to compare the resulting INLs and output spectra. A brief discussion of both the systems follows.

The system of Fig. 3.8 is used to compare the INL plots. The input to the system is a sweep signal with equally spaced values. The total number of values is $2^N + 1$, where N is the number of bits in the converter which from Fig. 3.8 is 10 (4 MSBs and 6 LSBs). The MSBs are thermometer encoded and the LSBs are binary encoded. The internal architectures of all the blocks of Fig. 3.8 will be discussed in more details in the subsequent subsections, right now the important thing to note here is the ability of the implemented model to produce different DAC output INLs by setting the output resistance and its mismatch to ideal and different real values.

The model of Fig. 3.8 only uses baseband DAC and doesn't work with an RF-DAC. The reason for this is that we cannot directly measure the INL of an RF-DAC because of the integrated upconversion, hence in this thesis we will circumvent this problem by simply using a baseband DAC.

The system implementation of Fig. 3.9 models the digital part of an LTE transmitter. The idea here is to see the impact of output resistance and its mismatches on the output of a working system where the converter is the final stage. Since we have a clearly defined idea of what the output from spectrum of the transmitter should look like, any additional distortion or noise will hence be a result of the non-linearity caused by the output resistance and its mismatches. This implementation is also a good example of the practical use and importance of the extensive discussion regarding the impact of output resistance and its mismatches on the non-linearity in the converter output,carried out in this text.

The model of Fig. 3.9 is quite similar to the model of Fig. 3.8 with only small differences, that are listed as follows:

1. The input to the system is an LTE signal instead of a linear one.
2. The encoding is carried out using a DEM encoder. This is done because we want to use the same architecture as used in [14]. The idea is to see how the resistance mismatches impact the performance since they are not modelled in [14]. On the other hand, the DEM encoder can't be used in the model of Fig. 3.8 because of the scrambling nature of the encoder which will destroy the proper sequence and hence make the comparison of input and output, for INL calculation, meaningless.
3. Both RF and Baseband DACs can be used for simulations since only the output spectra are being compared(no INL comparison).

Following is a brief descriptions of the blocks used in the models of Fig. 3.8 and Fig. 3.9.

3.3.1 Quantizer

The Quantizer block implements linear quantization for the case of INL comparison model of Fig. 3.8 and implements an ideal error-feedback $\Delta\Sigma$ modulator for the case of output spectra comparison model of Fig. 3.9. The in depth discussion of the quantizer and the error-feedback $\Delta\Sigma$ quantization it implements has been thoroughly studied in [14].

3.3.2 Binary/Thermometer encoder

The structure of binary/thermometer encoder is quite simple. The 10 bit input from the quantizer is split into 4 bit MSB and 6 bit LSB segments. The MSB segment is thermometer encoded while the LSB segment is binary encoded. The two encoded segments are then separately input to the DAC. The efficient matrix manipulation ability of MATLAB makes this process quite simple and easy.

3.3.3 DEM encoder

The DEM encoder block used for the output spectra comparisons implements the tree encoder structure. The general structure used in the MATLAB model has been presented in Fig. 3.10. The tree DEM encoder implemented here is just a simple usage example of the extensive discussion carried out in the previous chapters. The structure implemented here doesn't add anything new to the discussion and the reader is encouraged to go through the previous chapters and especially the references mentioned there for a good and thorough understanding of the implemented DEM encoder and its operation.

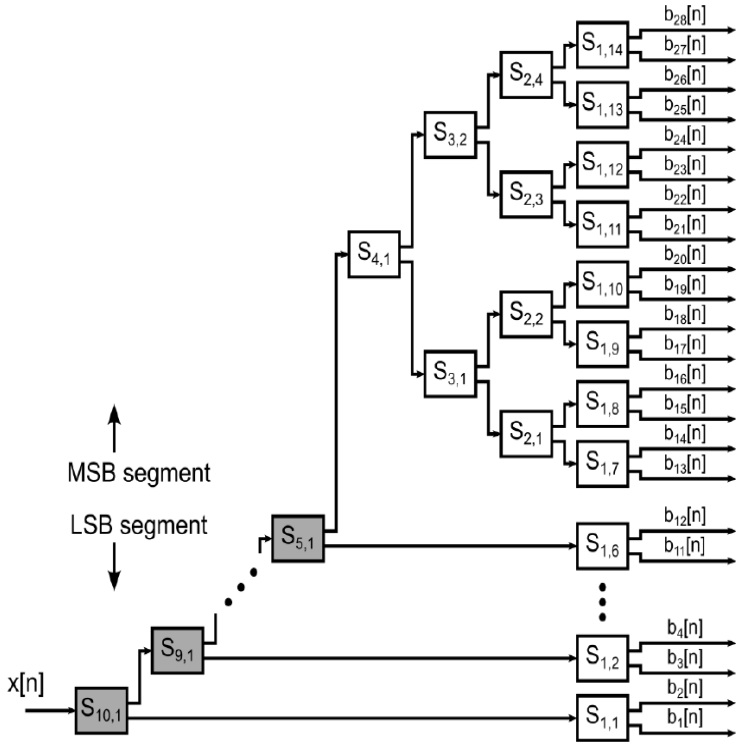


Figure 3.10: Internal structure of MATLAB implemented DEM encoder.

3.3.4 DAC

The digital-to-analog converter (or DAC, for simplicity) is the most important and the most processing intensive part of the system. Fig. 3.11 presents the DAC model as implemented in MATLAB. The model shows the conversion cells, with internal structures as discussed earlier in the Fig. 3.1, The individual conversion cell weights are also shown.

The model of Fig. 3.11 represents both the baseband DAC and the RF-DAC since they operate on the same basic principle with only notable difference being the use of upconversion in the RF-DAC case. The RF-DAC, for all intents and purposes, can be considered to be made up of an upconversion block followed by a baseband DAC. Since we are operating in the discrete time domain, the whole process of upconversion comes down to the repetition of the encoder output values based on RF-DAC parameters of over sampling ratio (OSR), duty cycle and the carrier to sampling frequency ratio of the RF-DAC. The OSR and the carrier to sampling frequency ratio are briefly discussed below. The duty cycle is not separately considered since, throughout this thesis, the duty cycle will always be kept at 50% which means half of the values will be set to high output and the other half will be set to low output.

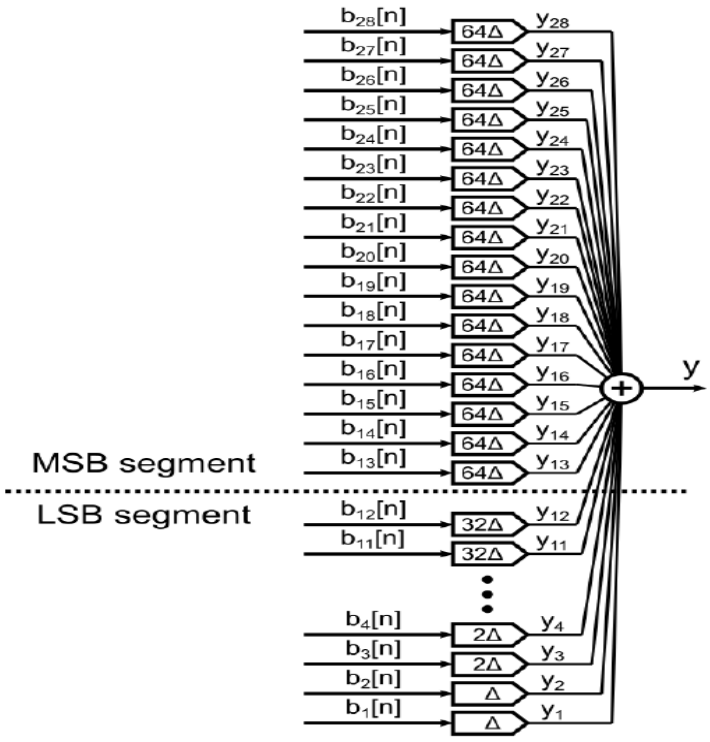


Figure 3.11: Internal structure of MATLAB implemented DAC.

Oversampling ratio

The oversampling ratio is classically defined as a measure of how many times higher is a signal sampled as compared to the minimum sampling rate required to avoid aliasing as defined by the Nyquist criteria. Mathematically represented as:

$$OSR = \frac{f_s}{f_N}$$

Where:

f_s = *Sampling frequency.*

f_N = *Nyquist frequency. Equals twice the signal bandwidth.*

OSR, in the context of this implementation, is the ratio between the sampling rate of the analog signal and that of the digital signal. In reality the analog signal should of course be continuous but, because we are using MATLAB, in practice the analog signal is also in discrete-time.

For all intents and purposes, the oversampling can be simply achieved by repeating a single signal value OSR number of times. Hence an RF-DAC with an OSR value of 10 would require an upconversion in such a way as to repeat each value of the signal ten times. It must be kept in mind that OSR only determines the number

of times each value has to be repeated it doesn't define the exact values that have to be repeated. This is done by the input value and the carrier to sampling frequency ratio.

Carrier to sampling frequency ratio

The carrier to sampling frequency ratio defines the number of jumps between high (or +1) and low (or -1) values within a single sampling period of the digital input signal. For this implementation, we are only using carrier to sampling frequency ratios of 1 and 2. A ratio of 1 means jumping from high (or low) value to a low (or high) only once during a single sampling period of the digital input signal. A ratio of 2 would mean making two such jumps. The direction of the first jump is defined by the input to the upconverter. An input value of +1 would mean a first jump from high to low value and an input value of -1 would mean a first jump from low to high value.

As an example, to properly understand the working of the upconverter and meaning of the RF-DAC parameters, let us consider a simple RF-DAC with an OSR of 8, duty cycle of 50% and a carrier to sampling frequency ratio of 2. The input to the upconverter, which is the encoder (bin/therm or DEM) output can only be +1 or -1. So for simplicity, lets say that the upconverter input is:

$$\text{upconverter input} = \left[\ +1\ -1\ \right]$$

Since the OSR value is 8, each of these input values will be converted into 8 values at the output. The duty cycle of 50%, dictates that half of the output values will be set to +1 and the other half will be set to -1. Also a carrier to sampling frequency ratio of 2 means jumping twice between the extreme values within a single OSR repetition(8 values). For +1 input we will start with high (+1) values, make first jump from high to low values and for -1 input the opposite will be true (starting with -1 and making first jump from low to high). Hence the total converter output will be:

$$\text{upconverter output} = \left[\ +1\ +1\ -1\ -1\ +1\ +1\ -1\ -1\ \middle|\ -1\ -1\ +1\ +1\ -1\ -1\ +1\ +1\ \right]$$

The above mentioned example is a simplified case as it only considers a vector input. In practise, the upconverter input is a matrix and hence for the RF-DAC parameters of above example the upconverter output may look something like:

$$\left[\begin{array}{cccccccc|cccccccc|ccc}
+1 & +1 & -1 & -1 & +1 & +1 & -1 & -1 & -1 & -1 & +1 & +1 & -1 & -1 & +1 & +1 & . & . & . \\
-1 & -1 & +1 & +1 & -1 & -1 & +1 & +1 & +1 & +1 & -1 & -1 & +1 & +1 & -1 & -1 & . & . & . \\
+1 & +1 & -1 & -1 & +1 & +1 & -1 & -1 & -1 & -1 & +1 & +1 & -1 & -1 & +1 & +1 & . & . & . \\
. & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . \\
. & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . \\
. & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & . & .
\end{array}\right]$$

Moving on to the actual digital-to-analog conversion process, which is same for both the RF-DAC and the baseband DAC. The conversion process is divided into the

ideal output calculation process and the output resistance and its mismatches calculation process. The output is calculated as a combination of theses two processes, a combination of the ideal component and the non-linear component.

The ideal output calculation process is quite simple and straight forward. Each conversion cell weight is multiplied by the LSB current to calculate the contribution of each conversion cell to the output. These contributions of the individual conversion cell, depending upon the input to the DAC are set to produce either a high value(by turning on the p sub-cell) or a low value(by turning on the n sub-cell). These high and low value contributions from the individual cells are then combined to produce the ideal output. In MATLAB the whole process comes down to simple matrix multiplications and comparison operators.

The output resistance and its mismatches calculation process starts with the generation of the mismatch profiles. The mismatch profiles are generated for both on and off conductances, using normally distributed random numbers with the standard deviation given as:

$$\sigma = \frac{MM\%}{100} * \sqrt{W_c} * G$$

Where:

$MM\%$ = *Percentage mismatch in the conductance.*

W_c = *Weights of conversion cells*

G = *Conductance of sub-cell. Could be* G_{ON} *or* G_{OFF}

σ = *Standard deviation of the generated mismatch profile.*

The percentage mismatch dictates the maximum amount of mismatch that can exist in a single conductance with relation to the base (or ideal) value. The percentage mismatch is adjustable according to the requirements. Since the total conductance is a sum of random independent variables (individual cell conductances), the standard deviation of the generated mismatches is directly proportional to the square root of the individual conversion cell weights and the mismatches themselves are centered at the weighted conductance values. Hence, every conversion cell has its own mismatch with a standard deviation proportional to the square root of its weight and is centered at the weight times the conductance value. As already mentioned, the mismatch profiles are generated for both on and off conductances and since we are considering the model with mismatch among all the conductances each conversion cell will hence have four mismatch components: two for each of its sub-cells which are further individually divided into two values, for on and off conductances of individual sub-cells, bringing the total to four per conversion cell.

The next step is the implementation of the output current expression as derived in the sub section 3.2.3. In MATLAB, the output current expression is implemented

using vectors. These vectors store the conductance values of all the conversion cells (four conductance values for each conversion cell for a given input in the signal). Also stored in the vectors is the information about which exact conversion cells are set to high or low outputs (again for a given input of the signal). These are the n_P and the n_M values. For the whole signal these vectors are converted into matrices with each row corresponding to a single input of the whole signal and each column corresponding to a single conversion cell. Matrix multiplications, as defined by the output current expression are then carried out to calculate the non-linear output component. The use of vectors and matrices makes this implementation simple and compact.

Since we now have both the ideal output current and the non-linear contribution by the output resistance and its mismatches we can find the real output by a simple multiplication.

4 Results

This chapter presents the results obtained from the simulations of the MATLAB models, discussed in the previous chapter. Most of the results presented here show a comparison between outputs. The idea, behind showing these output comparisons, is to intuitively realize the non-linearity caused by the output resistance and its mismatches.

Section 4.1 presents the results from the simulations of the baseband DAC models. The INL and output spectra comparison plots are shown. In the section 4.2, results from the simulations of the RF-DAC models are presented. This section only shows the output spectrum comparison plots. The INL comparison plots are complex to derive for the continuous time model due to the upconversion in RF-DAC, as discussed in the previous chapter, and their discussion is hence outside the scope of this text. Section 4.3 presents the impacts of MSB segmentation on RX-band noise values of the output and section 4.4 presents a statistical simulation run for 20 INLs. And finally, section 4.5 shows the impact of changing duplex distance on RX-band noise for different values of mismatch.

The simulation results show that the non-linearity caused by the output resistance doesn't have an adverse impact on the output. This is especially visible in the output spectra comparison plots where the non-linear output tends to follow the same general output spectrum as the output with ideal resistance values. The difference in the RX-band noise, of the two outputs is also not large. For the case of mismatches in the output, the resulting non-linearity, although more pronounced, still doesn't adversely impact the general behavior. Even at the mismatch values of 100% the non-linear output tends to follow the general ideal output spectrum with no significantly great differences in the RX band noise values. The simulation results will also verify the previous discussion about the inability of the DEM encoder to correct the non-linearity caused by the output resistance in the absence of any mismatches and in case the mismatches do exist the DEM encoder is able to shape the non-linearity caused by these mismatches.

4.1 Baseband DAC results

In this section the simulation results for the baseband DAC models implemented in MATLAB will be presented.

4.1.1 INL comparison plots

The INL comparison model has been presented in Fig. 3.8 and discussed in section 3.3. Simulations using real resistance values of 0.4MΩ (for both R_{ON} and R_{OFF}) will be shown here. The idea here is use combinations of real and ideal values of on and off resistances and compare the outputs for the cases of resistances with and without mismatches, with changing percentage mismatch.

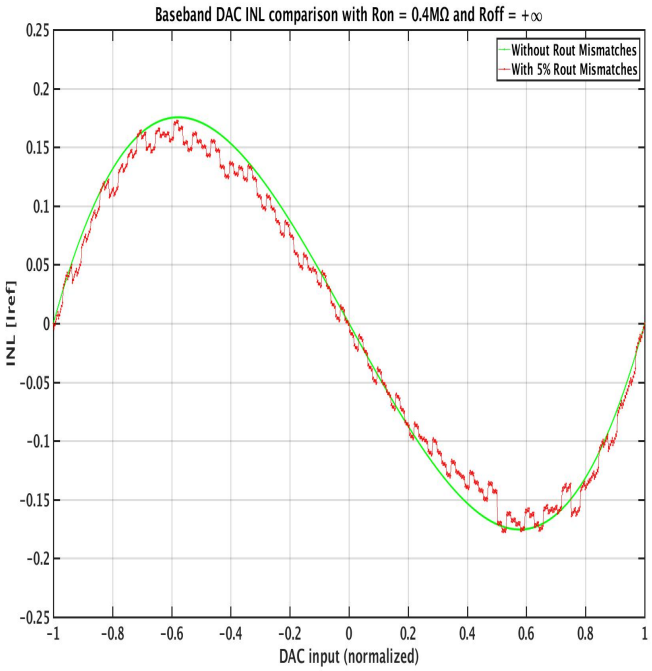
When using the ideal resistance values we will assume that there aren't any mismatches in that resistance. The mismatches will only exist for a real value of resistance. This means that if, for example, we use an ideal resistance value for R_{ON} and a real resistance value for R_{OFF}, when adding mismatches we will only add them to the R_{OFF} and no mismatches will be added to the R_{ON}.

Fig. 4.1 shows the INL comparisons for 5% output resistance mismatch using combinations of ideal and real(0.4MΩ) values for R_{ON} and R_{OFF}. It is quite evident form the figure that adding mismatch distorts the previously smooth INL curve.

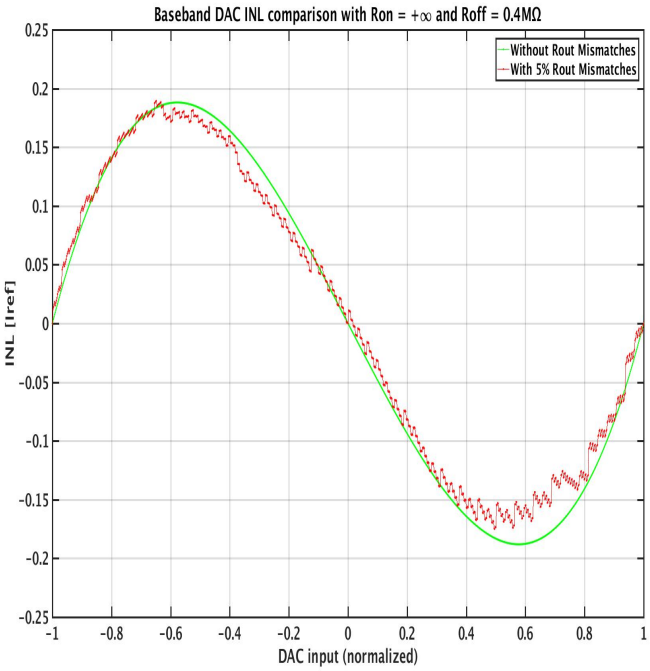
Fig. 4.1(c) shows an interesting result with a zero INL (straight line) for the case of both R_{ON} and R_{OFF} having a real and equal value (0.4MΩ) with no mismatch among the resistors. This result is actually quite easy to justify since using the same value for both R_{ON} and R_{OFF} and assuming no mismatches among the resistances results in a situation where all the conversion cells will have the same output resistance at all times and hence regardless of whichever conversion cell the input selects the output resistance remains the same. This removes the dependence of output resistance on the input and hence results in a zero INL. However, in practise the assumption of all the conversion cells having the same output resistance at all the times is not a realistic one. There will always be mismatches among the resistors which will result in non-zero INL values.

Increasing the mismatch to 20% produces results presented in the Fig. 4.2. The vertical scale has now been changed to ensure that all the values are visible since the mismatch increases make the INL values jump more haphazardly. Also visible from Fig. 4.2(c), is the case of zero INL for equal on and off resistance values with no mismatch.

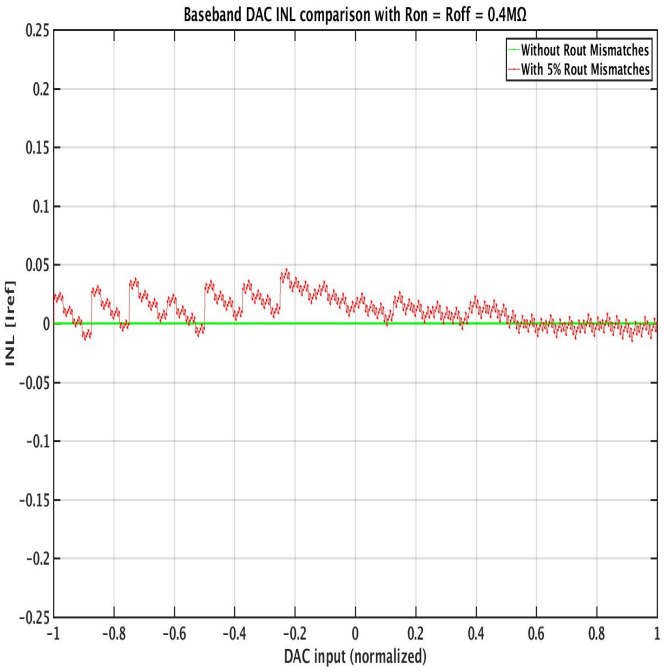
Moving on to the case of 100% mismatch. The results are now presented in Fig. 4.3. The vertical scales have again been changed due to an increase in the mismatch. Note that the vertical scales are now changing even among the figures that already have 100% mismatch since the mismatch is now high. Fig. 4.3(c) shows a similar zero INL value behavior, just like the Figs. 4.1(c) and 4.2(c), for equal and no mismatch values of R_{ON} and R_{OFF}.



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$

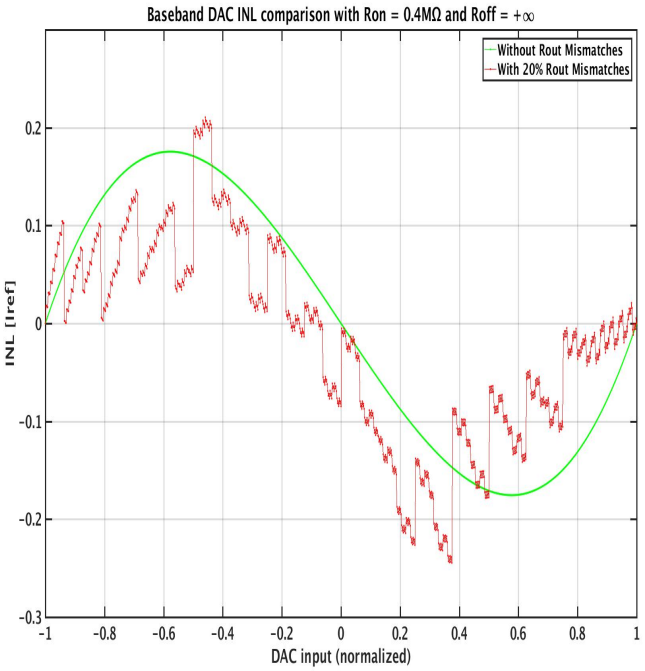


(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$

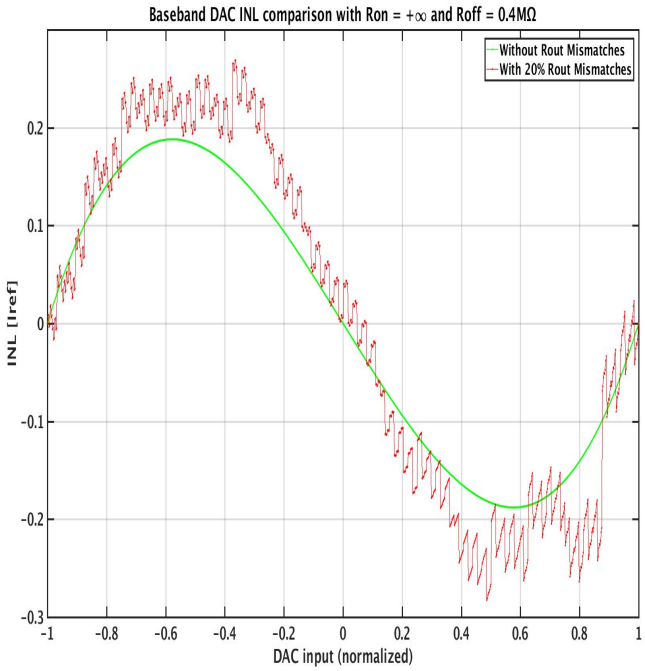


(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

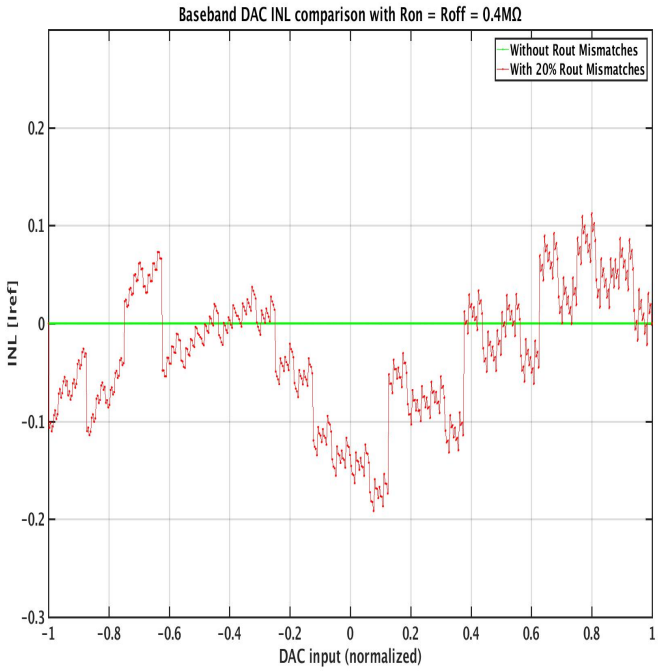
Figure 4.1: Baseband DAC INL comparison plot for $MM\% = 5\%$



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$

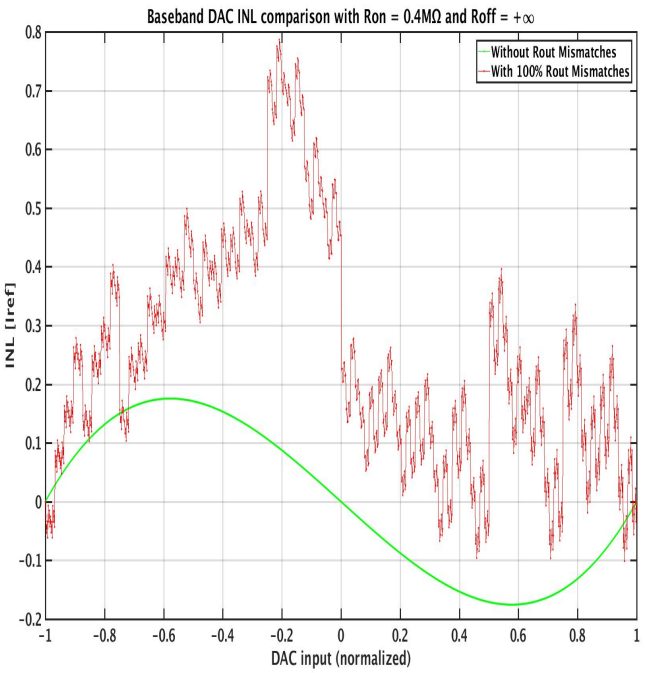


(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$

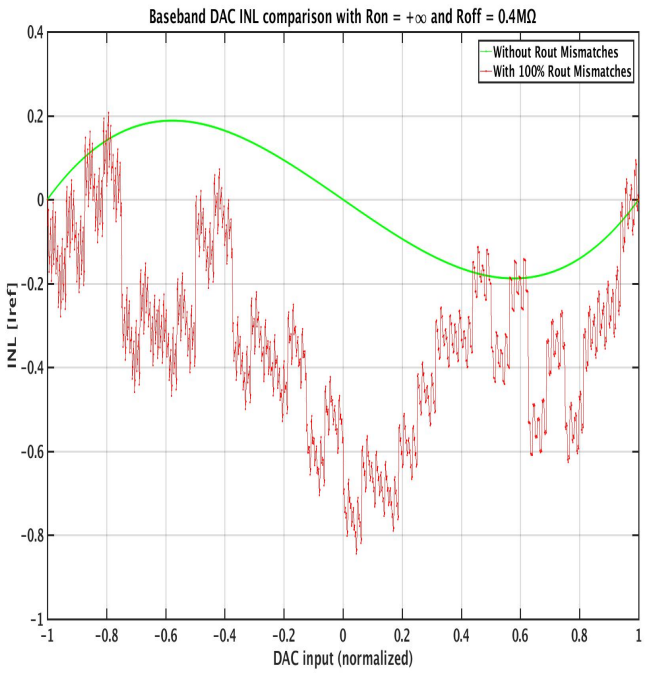


(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

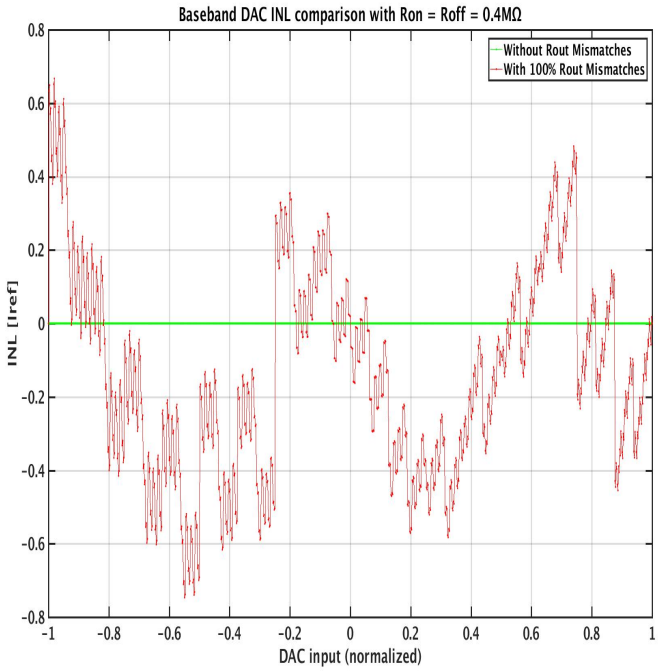
Figure 4.2: Baseband DAC INL comparison plot for $MM\% = 20\%$



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$



(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$



(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

Figure 4.3: Baseband DAC INL comparison plot for $MM\% = 100\%$

4.1.2 Output spectra comparison plots

The output spectra comparison model is presented in Fig. 3.9 and discussed in section 3.3. Here we are considering the baseband DAC implementation. The assumption of no mismatch among the resistances for an ideal resistance value also holds here. The vertical and horizontal scales are same for all the baseband DAC output spectra comparison plots.

The LTE signal used as input has a bandwidth of 20MHz ,a duplex distance of 190 MHz and is sampled at 921.6 MHz. The system simulates 25% of the the signal length taking normalized real part.

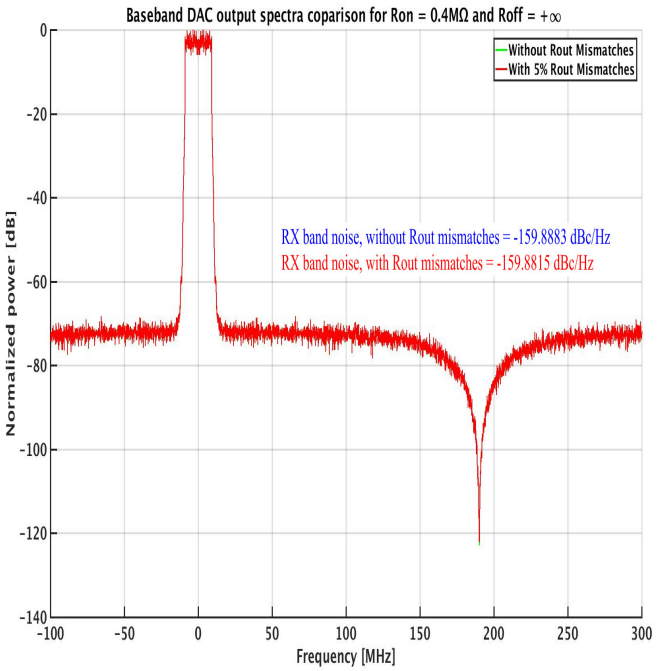
Fig. 4.4 shows the DAC output spectra comparisons for 5% output resistance mismatch using combinations of ideal and real(0.4MΩ) values for R_{ON} and R_{OFF}. It is quite evident from the figures, and the RX band noise values, that there is not much difference among the two spectra. This is because of the relatively small value of percentage mismatch.

Fig. 4.5 shows the same results for 20% output resistance mismatch. The figures and the RX band noise values again show that the non-linearity caused by the output resistance mismatch, although more than the previous case(5%), is still not drastically impacting the DAC output.

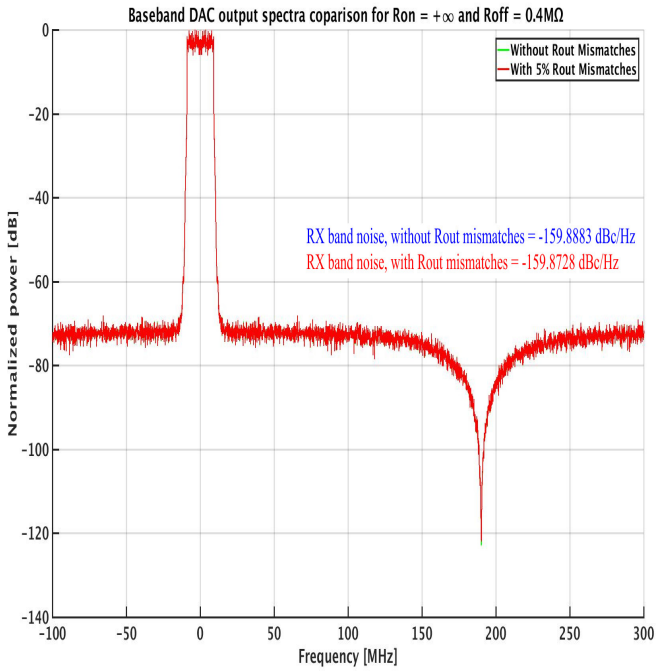
Fig. 4.6 shows the DAC output spectra comparisons for 100% output resistance mismatch. Again evident from the figures and the RX band noise values is that the non-linearity is now more pronounced. The DAC output however, is still looking quite good and tends to follow the no resistance mismatch output. The RX-band noise values, as indicated on the figures, are decreased, due to the use of $\Delta\Sigma$ modulator and DEM encoder.

These simulation results show that even at very high mismatch (100%), the output tends to follow the ideal case and the RX-band noise values are also not greatly deteriorated. This leads to the conclusion that the non-linearity caused by the output resistance and its mismatches don't adversely impact our system in practise.

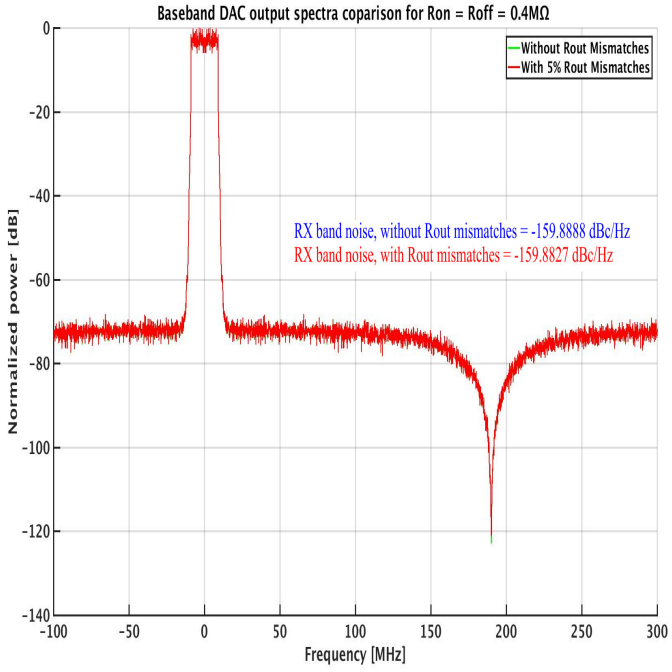
This relative immunity of our system is due to large difference between the load and the output resistance. For our transmitter the load resistance is set to 50Ω where as the on and off resistances are both set to 0.4MΩ. In actual systems it is the relative value of output and load resistance that matters. This can also be seen from the models derived in Chapter 3, where substitutions were made to replace the on and off conductances and load resistance products. Fig. 4.7 simulates this situation. The mismatches are set to zero (MM% = 0%) and R_{OFF} is set to infinite value. In Fig. 4.7(a) R_L is kept constant at 50Ω and R_{ON} is changed from 0.4MΩ to 40Ω. In Fig. 4.7(b) R_{ON} is kept constant at 0.4MΩ and R_L is changed from 50Ω to 0.5MΩ. For both of these figures, as the R_{ON} and R_L values become comparable the non-linearity in the output increases as visible from the bandwidth increase around the transmission band. However, this case is just a test simulation



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$

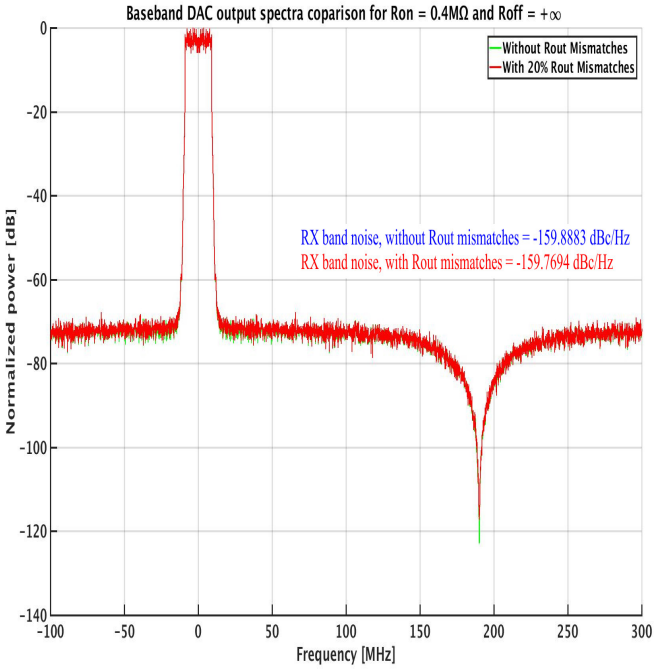


(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$

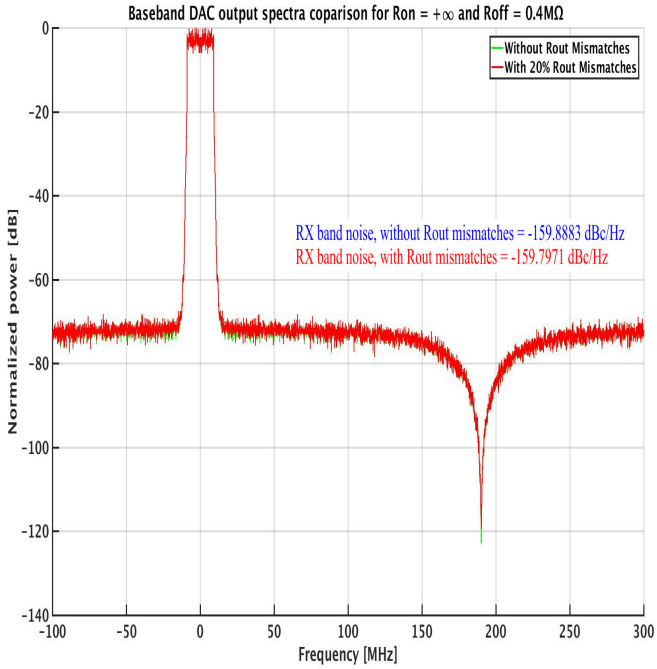


(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

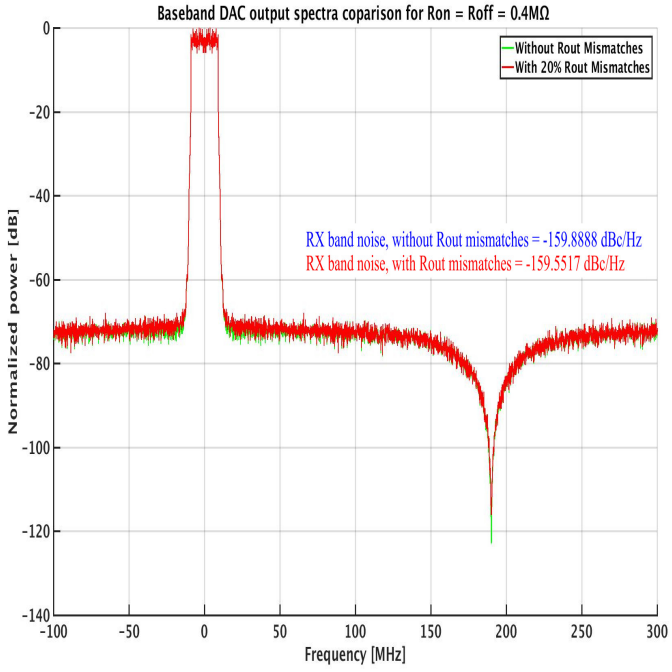
Figure 4.4: Baseband DAC output spectra comparison plot for $MM\% = 5\%$



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$

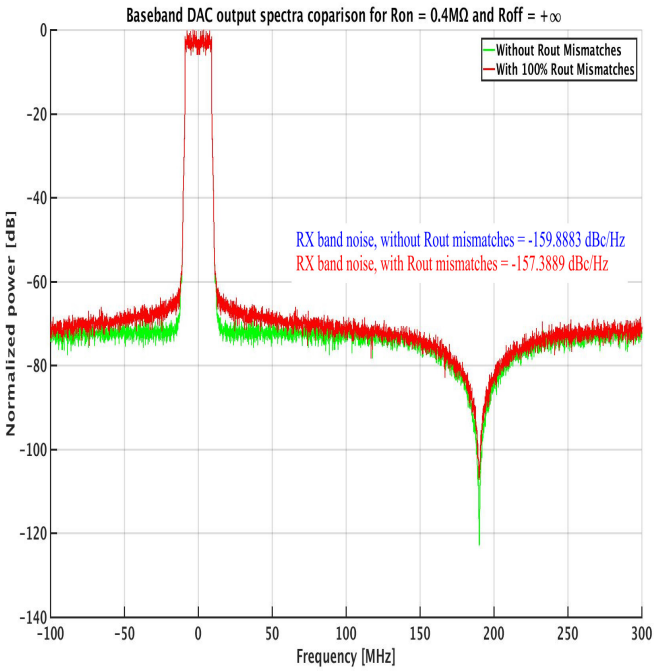


(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$

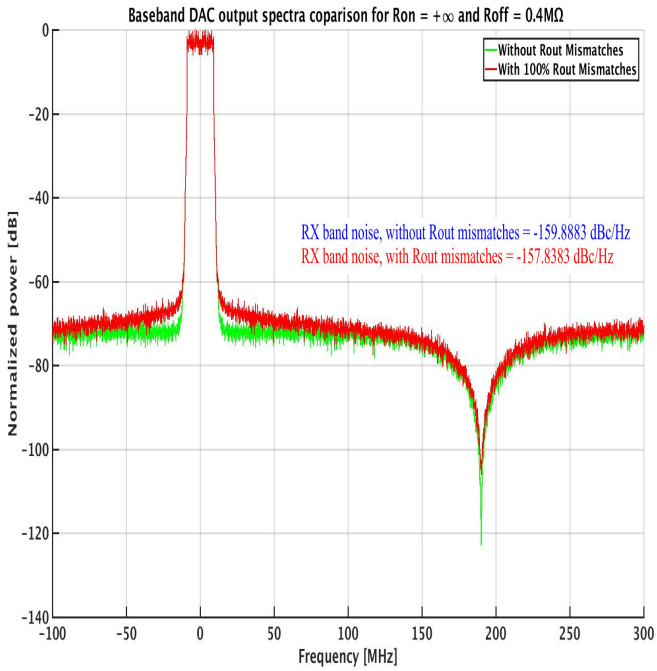


(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

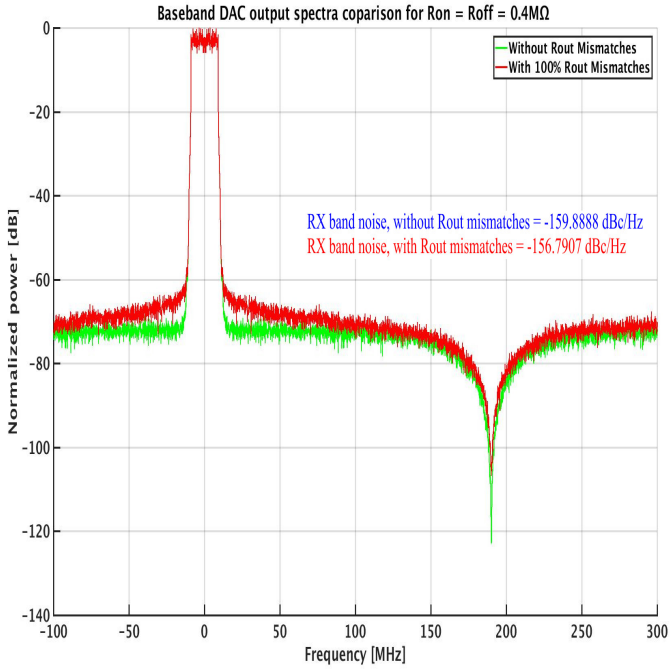
Figure 4.5: Baseband DAC output spectra comparison plot for $MM\% = 20\%$



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$

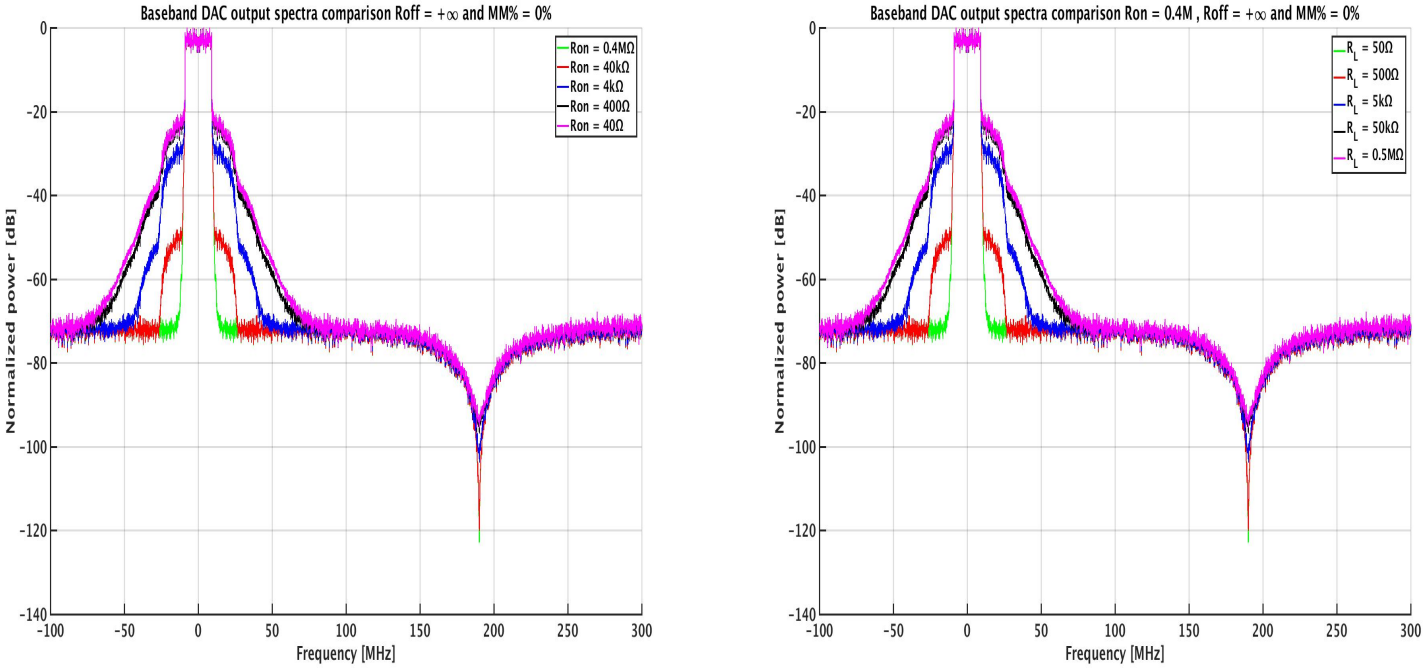


(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$



(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

Figure 4.6: Baseband DAC output spectra comparison plot for $MM\% = 100\%$

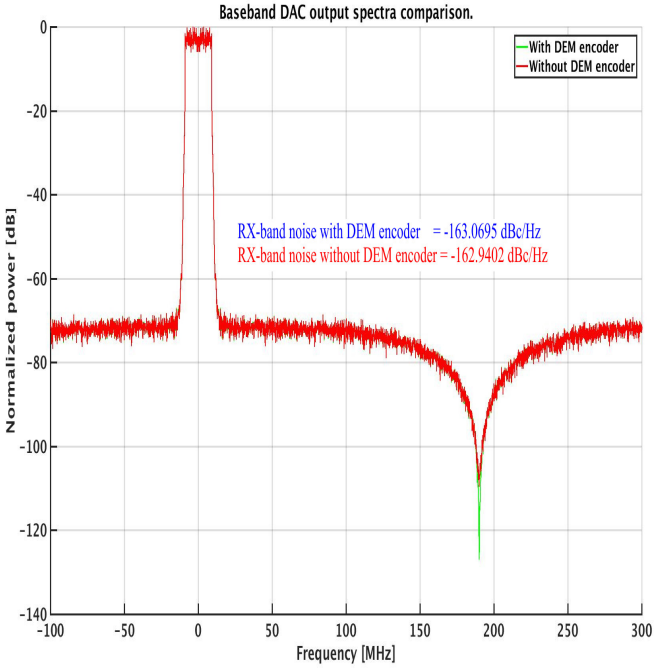


(a) $R_L = 50\Omega$ (b) $R_{ON} = 0.4\text{M}\Omega$

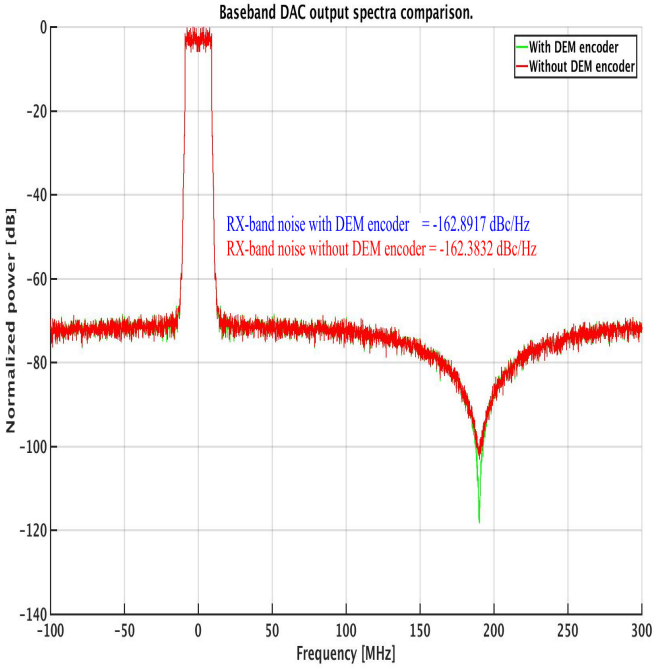
Figure 4.7: Baseband DAC output spectra for changing R_{ON} and R_L.

to show the importance of relative value of output and load resistances. For our system the load resistance is kept constant at 50Ω and hence it is safe to conclude that our system is not adversely impacted by the output resistance. Since in this simulation we are using the DEM encoder, the existence of significant non-linearities in the output confirms our previous theory about the inability of the DEM encoder to correct the output resistance non-linearity when no mismatches are present.

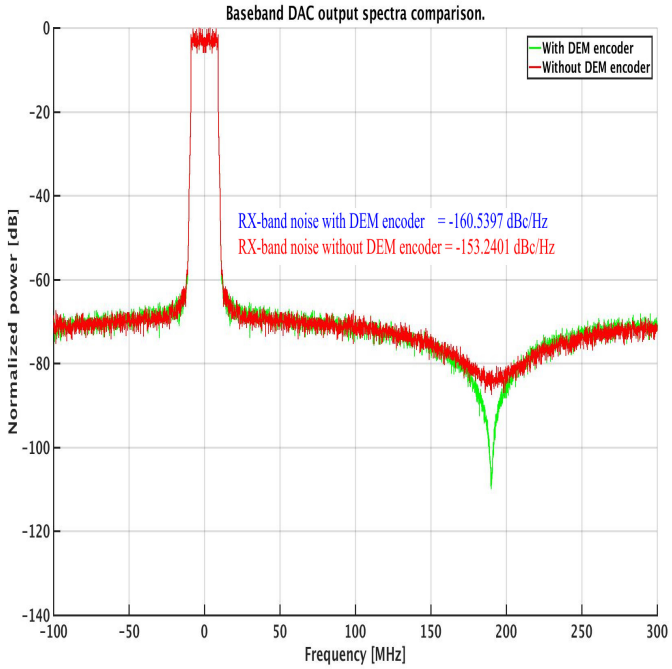
Fig 4.8 shows the impact of using DEM encoder to shape the output resistance mismatches. R_{ON} is set to 0.4MΩ and R_{OFF} to infinite value. This combination is used to take into account the impact of finite output resistance value and its mismatches since using real value for both would mean an output non-linearity arising purely from mismatches which is not a realistic case. The baseband DAC output spectra when DEM encoder is used and when it is not used (in this case bin/therm encoder is used) are presented in Figs. 4.8a, 4.8b and 4.8c for 5%, 20% and 100% mismatch cases respectively. The results show that by using the DEM encoder the mismatches can be shaped quite effectively. This proves our previous theory about the ability of DEM encoder to shape the output resistance mismatches.



(a) MM% = 5%



(b) MM% = 20%



(c) MM% = 100%

Figure 4.8: Using DEM encoder to shape output resistance mismatches.

4.2 RF-DAC results

In this section MATLAB simulation results for RF-DAC are presented. We will only discuss the results for output spectra since upconversion complicates the INL result simulation, as already mentioned.

4.2.1 Output spectra comparison plots

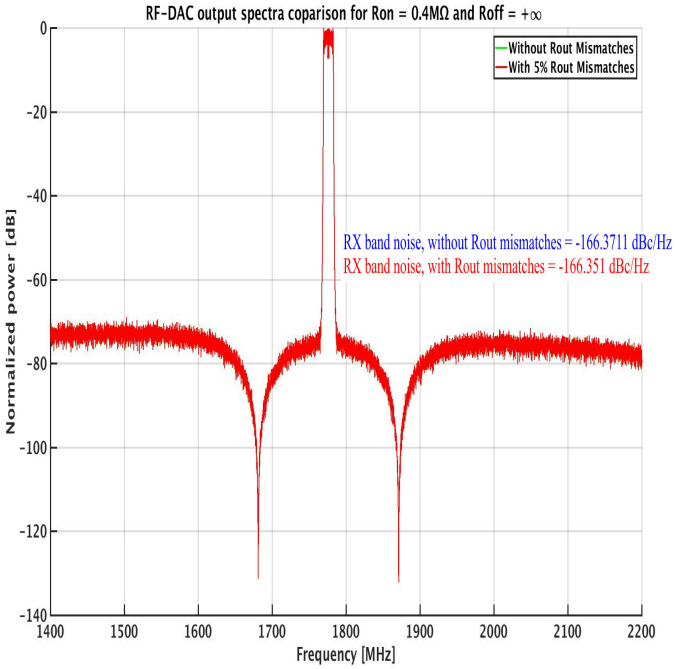
The output spectra comparison model is presented in Fig. 3.9 and discussed in section 3.3. Here we are considering only the RF-DAC implementation. The simulations in this section will follow the same general output comparison format as used for the baseband DAC case.

The LTE signal used as input has a bandwidth of 15MHz, a duplex distance of 95MHz and is sampled at 888MHz. The carrier frequency is 1776MHz (twice the sampling frequency). The system simulates 35% of the signal length taking normalized real part. The OSR of RF-DAC is set to 1000 with a duty cycle of 50% and a carrier to sampling frequency ratio of 2. The context and discussion of these RF-DAC parameters can be found in sub section 3.3.4.

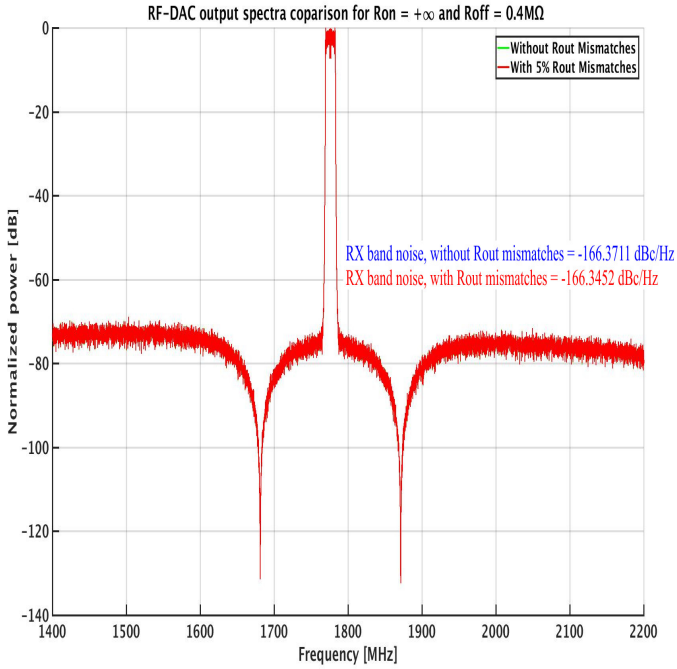
Figs. 4.9, 4.10 and 4.11 show the DAC output spectra comparisons for 5%, 20% and 100% output resistance mismatch respectively. The 5% resistance mismatch case (Fig. 4.9) has the lowest and the 100% resistance mismatch case (Fig. 4.11) has the maximum non-linearity with even the output with maximum mismatch (100% resistance mismatch) following the general spectrum of no resistance mismatch output. Again, the RX-band noise values are decreased, due to the use of $\Delta\Sigma$ modulator and DEM encoder.

Just as was the case in baseband DAC, the relative immunity of our system is due to large difference between the load resistance and output resistance values. Fig. 4.12 shows this case, by setting mismatches to zero (MM% = 0%), R_{OFF} to an infinite value and showing the impact of either changing R_{ON} or R_L while keeping the other one constant. For comparable values of R_{ON} and R_L the non-linearity is quite pronounced as can be seen from the figure but this non-linearity is not a cause for concern for our system since we are using R_L set to 50Ω. Another conclusion that can be drawn from this simulation is the inability of the DEM encoder to correct the non-linearity caused by the output resistance in the absence of mismatches.

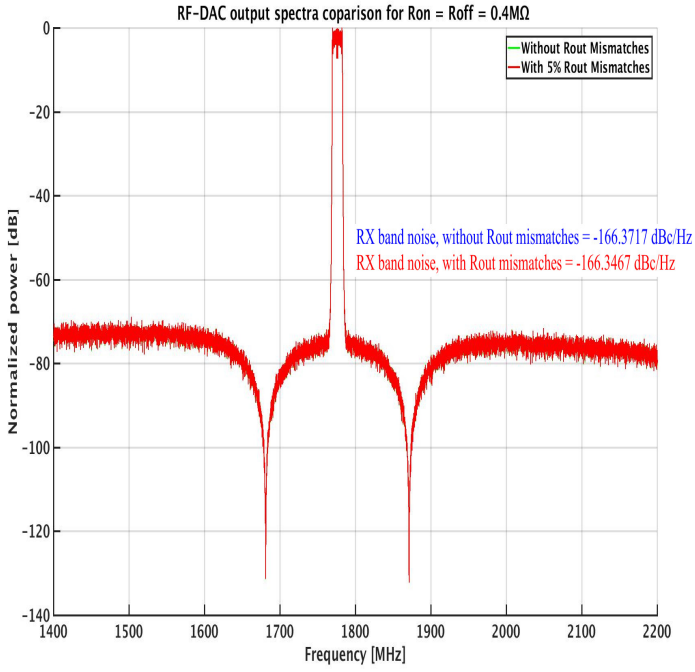
Fig 4.13 shows the impact of using DEM encoder to shape the output resistance mismatches. R_{ON} is set to 0.4MΩ and R_{OFF} to infinite value. The output spectra are presented in Figs. 4.8a, 4.8b and 4.8c for 5%, 20% and 100% mismatch cases respectively. The results show that by using the DEM encoder the mismatches can be shaped quite effectively. This again proves our previous theory about the ability of DEM encoder to shape the output resistance mismatches.



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$

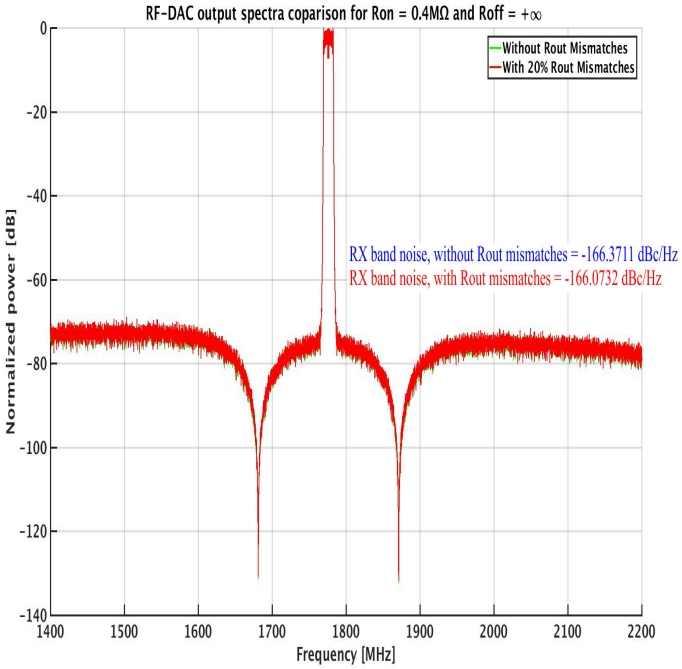


(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$

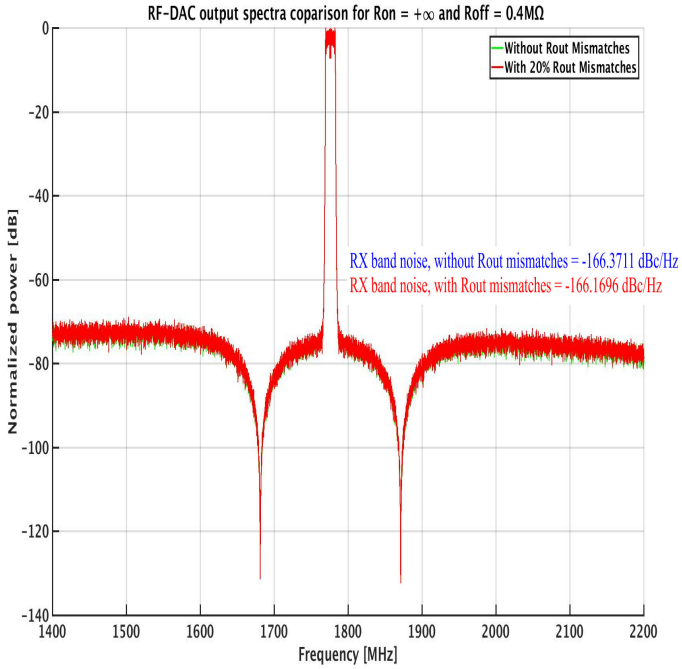


(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

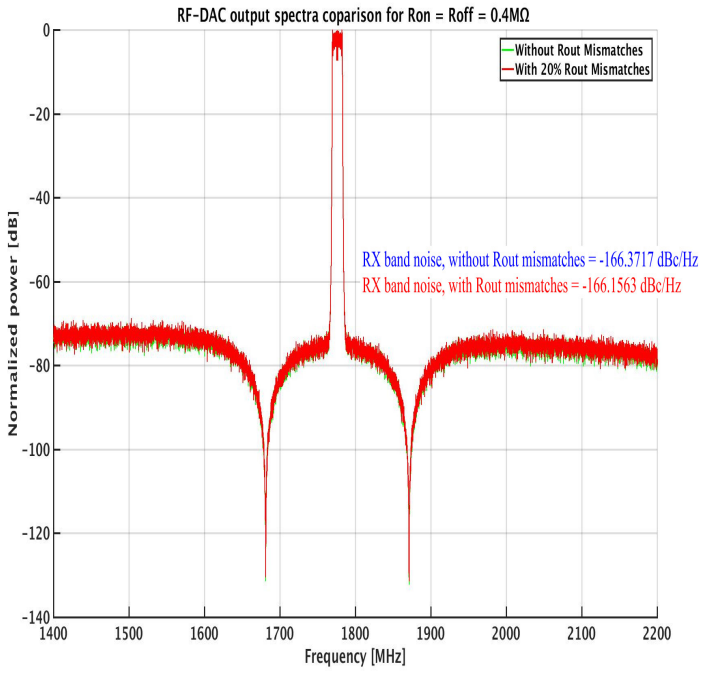
Figure 4.9: RF-DAC output spectra comparison plot for $MM\% = 5\%$



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$

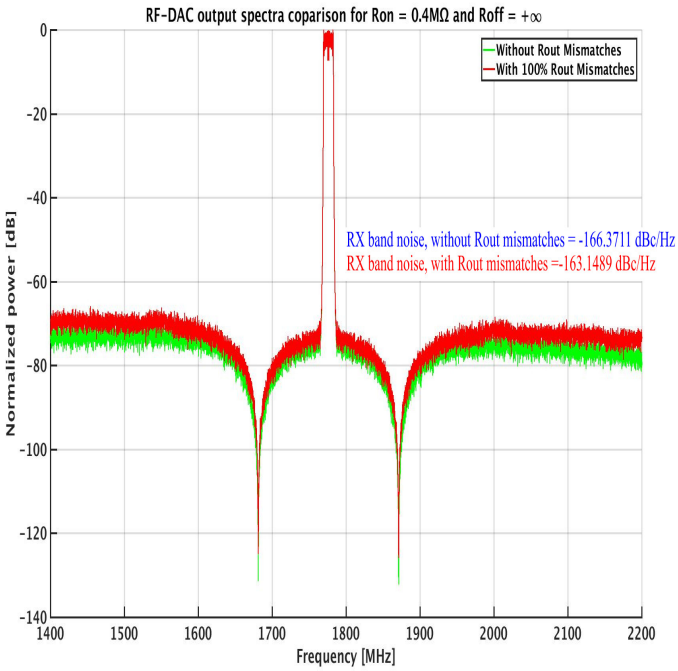


(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$

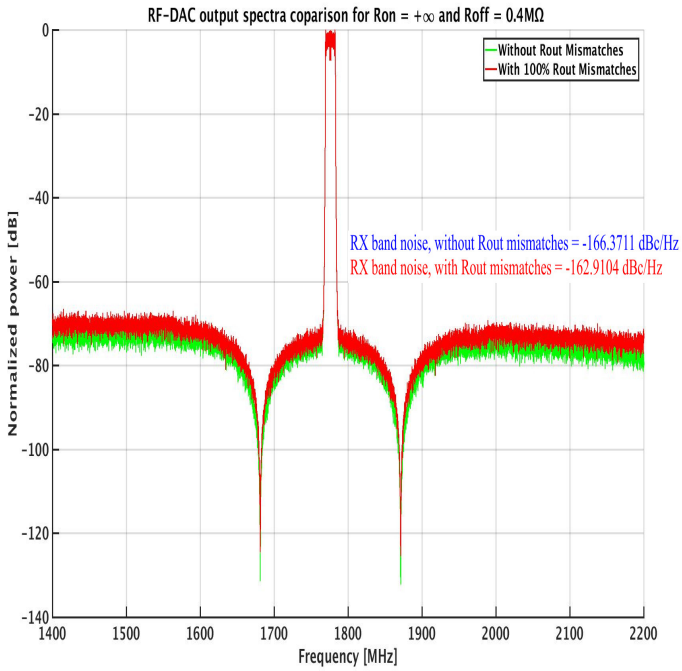


(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

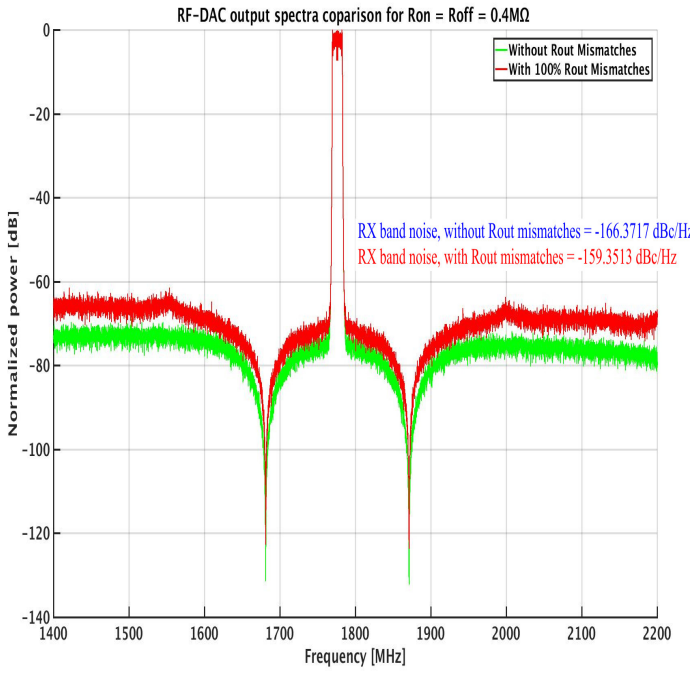
Figure 4.10: RF-DAC output spectra comparison plot for $MM\% = 20\%$



(a) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = \infty$

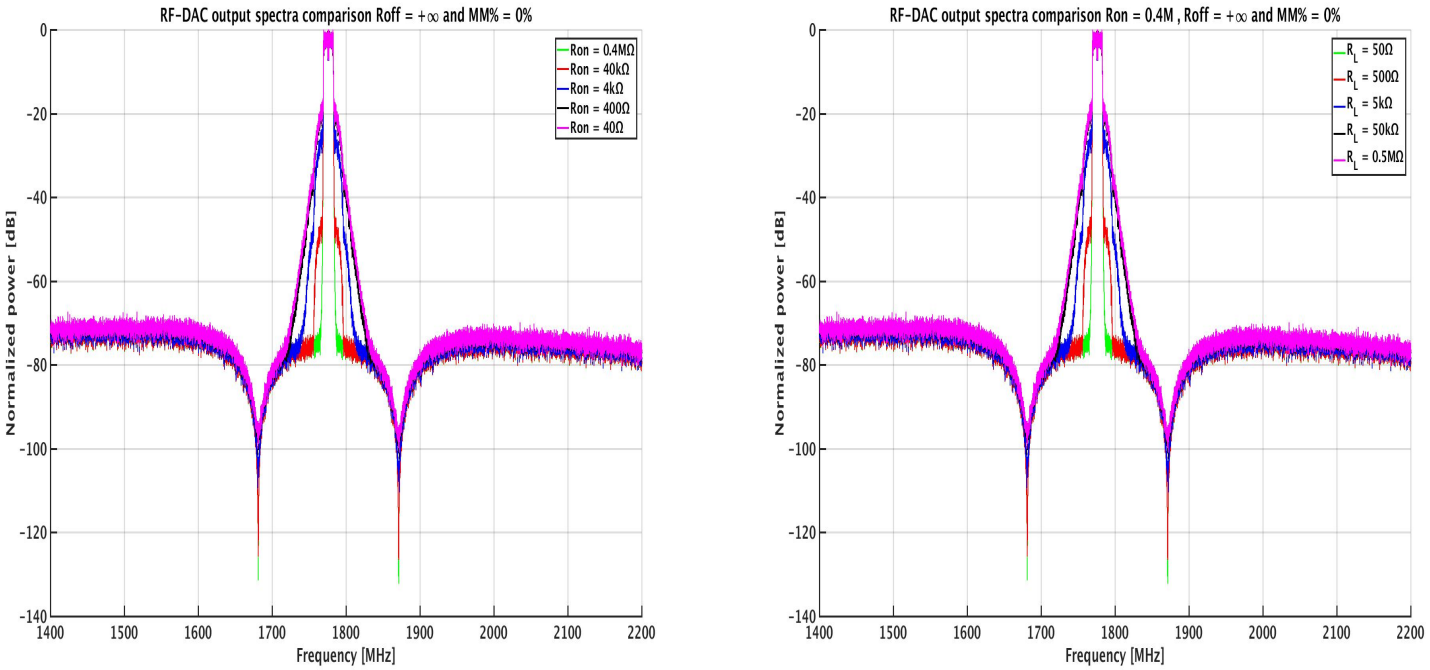


(b) $R_{ON} = \infty$, $R_{OFF} = 0.4\text{M}\Omega$



(c) $R_{ON} = 0.4\text{M}\Omega$, $R_{OFF} = 0.4\text{M}\Omega$

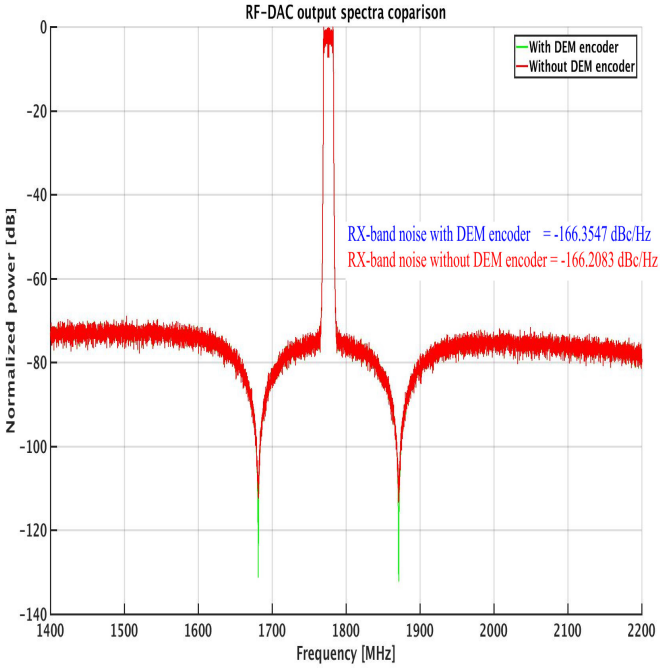
Figure 4.11: RF-DAC output spectra comparison plot for $MM\% = 100\%$



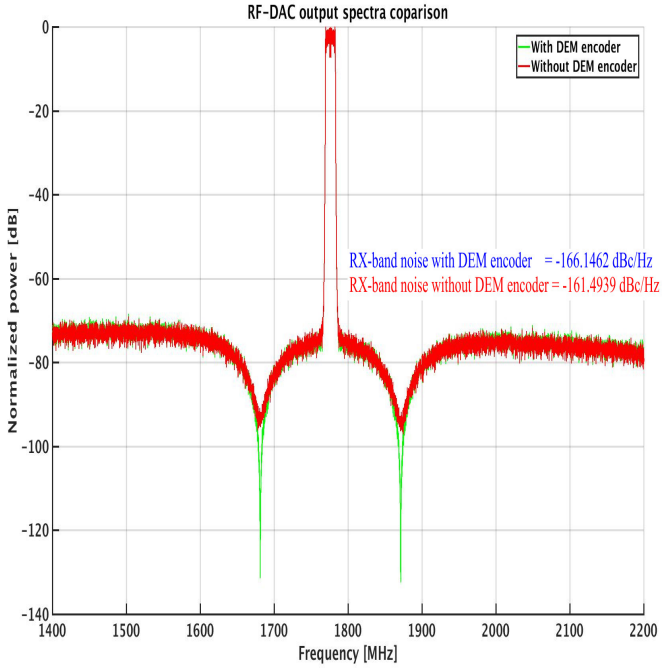
(a) $R_L = 50\Omega$ (b) $R_{ON} = 0.4\text{M}\Omega$

Figure 4.12: RF-DAC output spectra for changing R_{ON} and R_L.

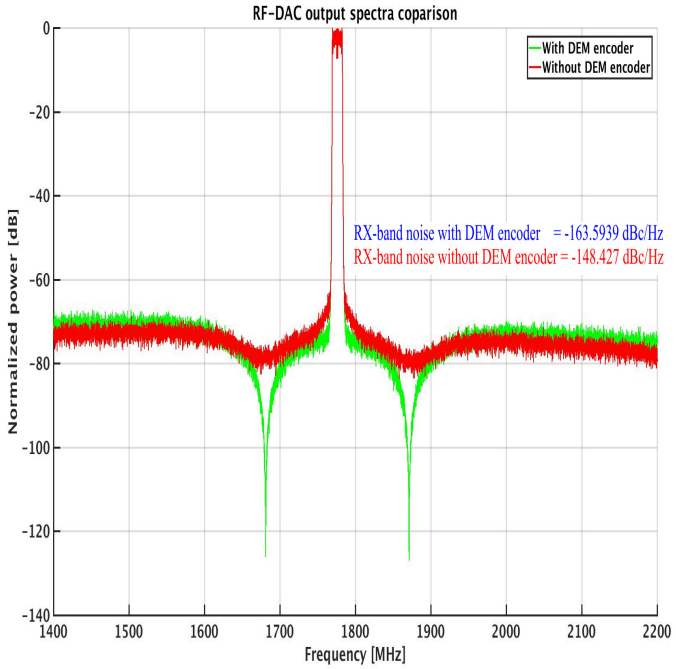
It is quite evident from the above discussion, the obtained figures and the RX-band noise values that the RF-DAC model behaves in a way that is quite similar to the baseband DAC, as is to be expected, since only upconversion is involved in moving from baseband DAC to RF-DAC. The simulation results, for both the baseband DAC and RF-DAC, show that for our system the output resistance and its mismatches don't adversely impact the output. These simulations also show that the DEM encoder is unable to correct the non-linearity caused by the output resistance in the absence of mismatches however, if the mismatches exist then DEM is able to correct the non-linearity they cause by turning it into shaped noise.



(a) MM% = 5%



(b) MM% = 20%



(c) MM% = 100%

Figure 4.13: Using DEM encoder to shape output resistance mismatches.

4.3 MSB segmentation

Fig. 4.14 shows the RX-band noise values plotted against different lengths of the MSB segment. This simulation is useful for comparing the cases of using DEM encoder and not using it. Fig. 4.14(a), 4.14(b), 4.14(c) and 4.14(d) repeat these simulations for varying degrees of output resistance mismatch. All these simulation were carried out using finite R_{ON} ($0.4M\Omega$) and infinite R_{OFF} values. The input to the system was an LTE signal with a bandwidth of 20MHz and a duplex distance of 190MHz sampled at 921.6MHz. The simulation was carried out using a baseband DAC, for simplicity, since the RX-band noise values are comparable for both baseband and RF-DAC.

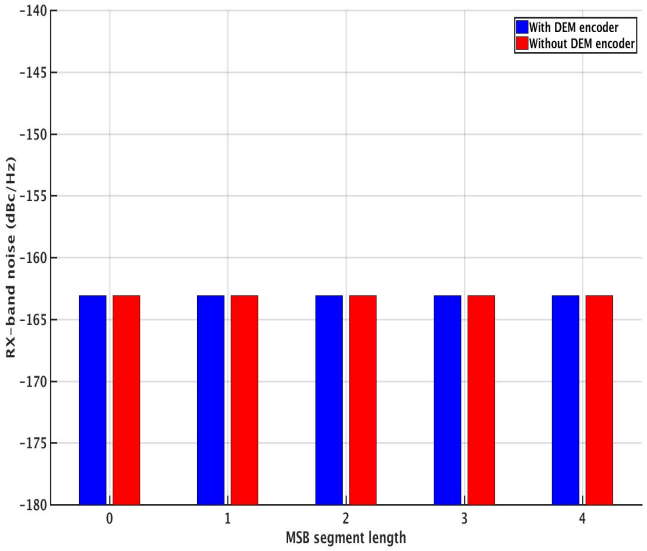
In this simulation, there is no practical difference between the MSB segment lengths of 0 and 1, because there is no difference between binary and thermometer encoding when it comes down to a single bit. So for the cases when mismatches do exist, the RX-band noise for MSB segment length of 1 might be greater then the corresponding noise for MSB segment length of 0. This might seem counter intuitive but can be explained with above discussion and remembering that the mismatch profiles are created using normally distributed random numbers. For the case when DEM encoder is not used the RX-band noises are effectively random regardless of the MSB segment length used since we are not applying any mismatch shaping techniques.

The simulation results show a decrease in the RX-band noise whenever the DEM encoder is used except when mismatches are set to zero. In this case there is no difference in the RX-band noise regardless of whether the DEM encoder is used or not. This result is consistent with our previous discussion regarding the inability of the DEM encoder to deal with output resistance non-linearity. For the cases when mismatches do exist there is a clear difference in RX-band noise values when DEM encoder is used especially at higher values of MM% (100%). This result is also consistent with our previous theory stating the ability of DEM encoder to shape the output resistance mismatches.

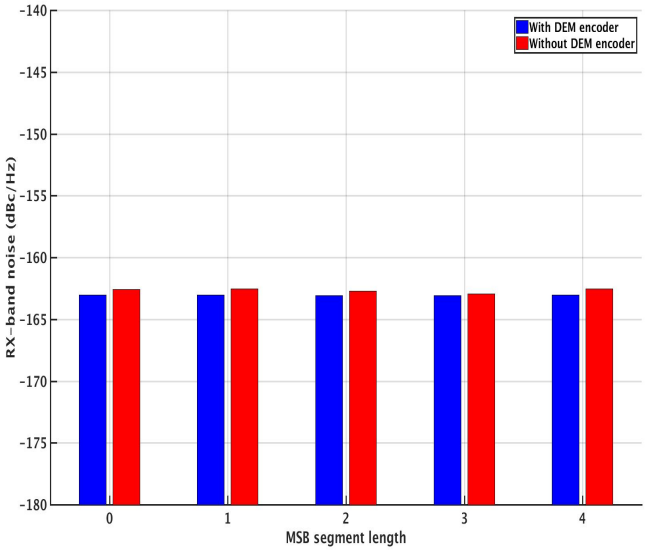
All the simulation results of Fig. 4.14 also show a trade-off between circuit complexity and output linearity when DEM encoding is used. Increasing the length of MSB segment makes the output more linear (as evident by decreasing RX-band noise values) at the cost of adding more complexity to the system and vice versa. A trade-off will hence have to be reached depending upon the noise floor and complexity requirements of the system.

4.4 Statistical INL simulation

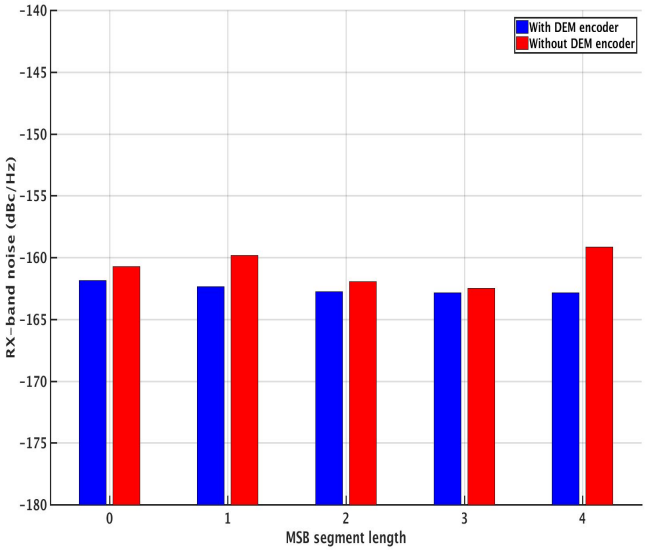
Fig. 4.15 shows the statistical INL simulation with 20 INLs plotted for a baseband DAC. The simulation again used the maximum mismatch (MM% of 100%) and finite R_{ON} and R_{OFF} values ($0.4M\Omega$). The input to the system was a linear sweep signal



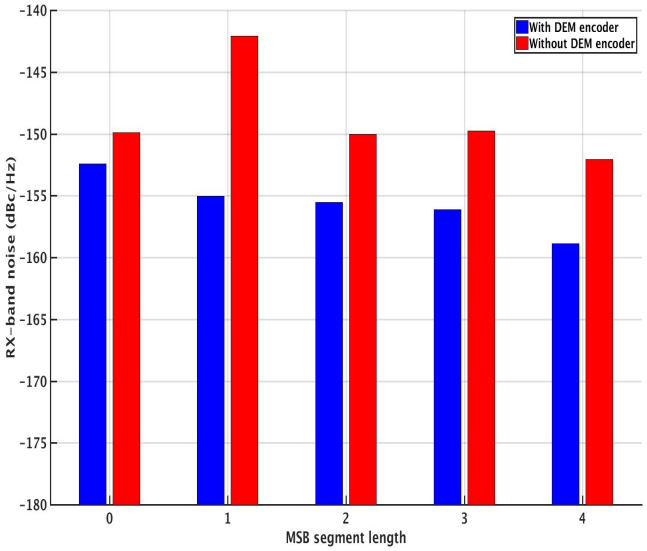
(a) MM% = 0%



(b) MM% = 5%



(c) MM% = 20%



(d) MM% = 100%

Figure 4.14: MSB segmentation.

with $2^N + 1$ samples equally spaced between +1 and -1. Where N equals 10 and is the total number of bits in the digital-to-analog converter. As already explained, the DEM encoder was replaced with a bin/therm encoder when simulating for INL, due to the scrambling nature of DEM encoder which would result in a lost one to one correspondence between input and output.

Fig. 4.15 shows that majority of the INL values lie closer to the line joining the

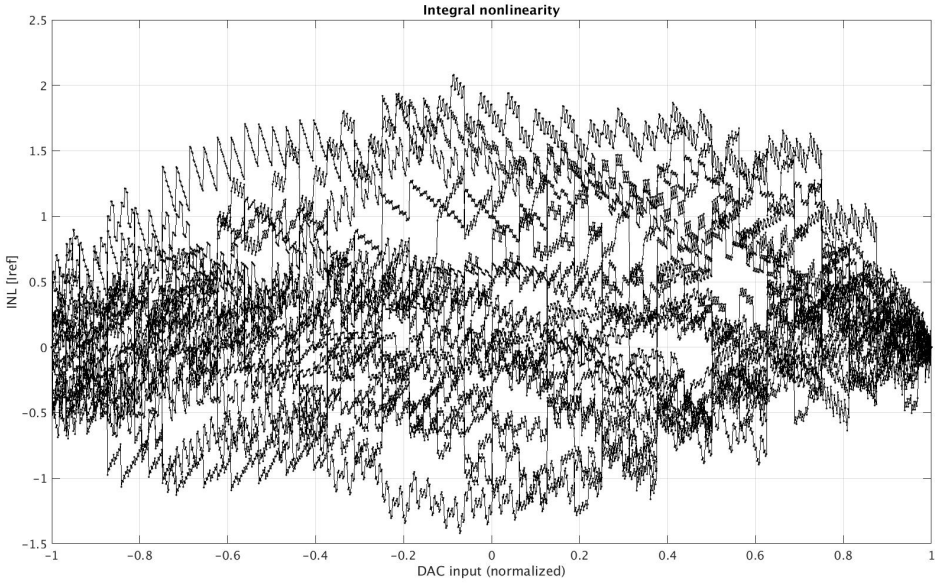


Figure 4.15: Baseband DAC 20 INLs.

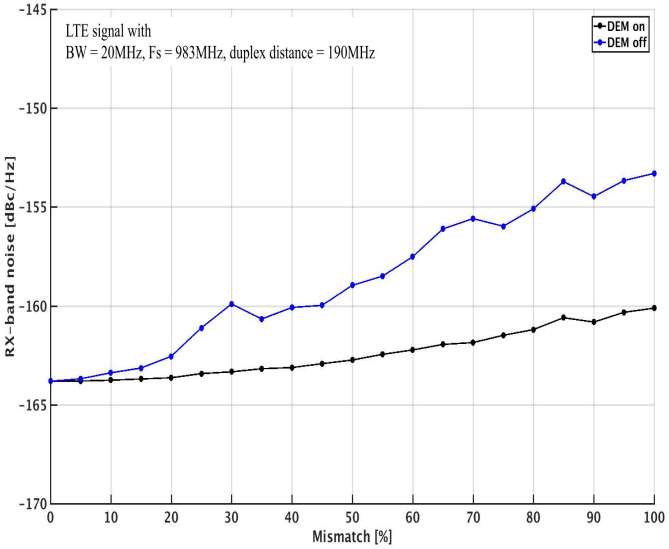
start and the end points. This is due to the fact that normally distributed random numbers are used for the generation of mismatch profiles. Since this mismatch profile generation process models the random errors introduced in the real life fabrication process, the statistical simulations of this type are useful for approximating the non-linearity that can be expected in a given practical system.

4.5 RX-band noise for changing duplex distance

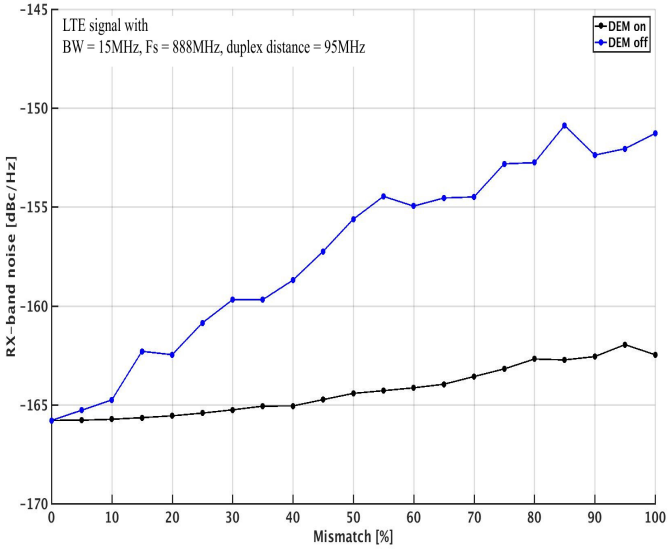
Fig. 4.16 shows the impact of changing duplex distance on RX-band noise for different values of mismatch. Fig. 4.16(a) uses an LTE signal with bandwidth of 20MHz and a duplex distance of 190 MHz, Fig. 4.16(b) uses an LTE signal with bandwidth of 15MHz and a duplex distance of 95MHz and Fig. 4.16(c) uses the same signal as Fig. 4.16(b) with duplex distance now being set to 50MHz. The figure plots mismatch percentage (MM%) from 0% to 100% in steps of five against RX-band noise. The results plotted are averaged for 10 values, to get smoother curves. Also shown in Fig. 4.16 is the impact of using DEM encoder.

The simulation results show that as the duplex distance decreases the the RX-band noise difference between the DEM encoded and bin/therm encoded values increases. This trend is clear in Figs. 4.16(b) and 4.16(c) where at a given mismatch percentage decrease in the duplex distance increases the RX-band noise.

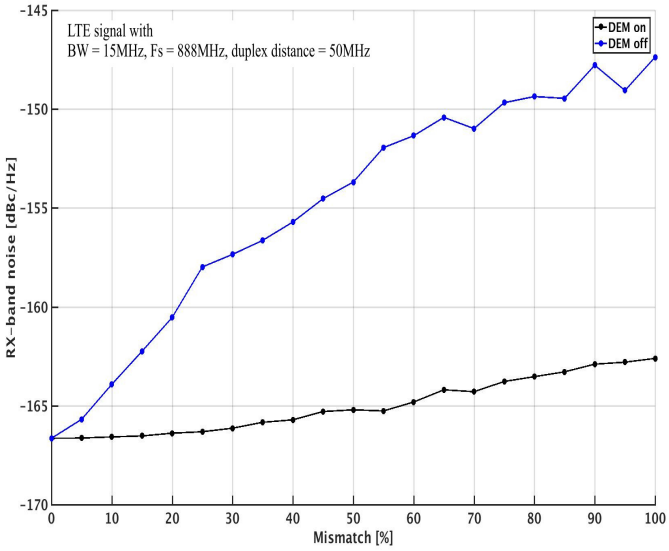
The differences in the noise values with changing duplex distances are more pronounced for higher mismatch percentages (MM% close to 100%) since in these cases there is not only increased non-linearity in the output but there is also an



(a) Duplex distance = 190MHz



(b) Duplex distance = 95MHz



(c) Duplex distance = 50MHz

Figure 4.16: MM% vs RX-band noise

increased potential of scrambling by the DEM encoder.

5 Conclusion

The thesis starts the discussion by stressing on the need of high speed digital-to-analog converters in the modern communication systems. The discussion then continues on to the nature and types of mismatches in the conversion cells of these converters and how these mismatches produce non-linearity in the output.

A brief literature review is then presented, focusing on the nature and causes of non-linearity introduced by the finite output resistance. The literature review then continues on to present the DEM encoding techniques with focus on the tree DEM architecture. The tree DEM encoder deals with the non-linearity in the converter's output by scrambling the conversion cell order on sample to sample basis which removes the dependence on input, resulting in non-linearity being converted into pseudo random noise. The thesis then theorizes that the DEM encoder will be unable to remove the non-linearity caused by a finite output resistance, in the absence of mismatches. This theory is based on the nature of output resistance and the DEM encoding process since DEM encoder uses scrambling of the conversion cell order to remove the non-linearity but the output resistance is common to all the conversion cells and its non-linearity is hence not removed by scrambling. In addition this thesis also theorizes that if output resistance has mismatches, which exist between different conversion cells, the DEM encoder is able to shape their non-linearity by scrambling.

The thesis then moves on to the process of modeling and analysing the finite output resistance. The process starts with a simple conversion cell model, showing the output resistance being split into on and off resistance. Three conversion cell models with varying amount of mismatches among their on and off resistances are then presented. The total output current expressions for each of these models are derived and their implications are discussed. The thesis then presents a MATLAB model implementation for the most comprehensive model among the three derived models. The digital-to-analog converter implemented in MATLAB is discussed in more detail and its baseband and RF versions are also discussed.

Finally, the thesis presents the simulation results of the implemented MATLAB model. The simulations carried out include:

1. INL comparison plots for finite output resistance with and without mismatches

for the baseband DAC.

2. Output spectra comparison plots for both baseband DAC and RF-DAC.
3. RX-band noise values for different MSB segment lengths.
4. Statistical simulation for INL.
5. Impact of changing duplex distance on RX-band noise

The simulation results show that the finite output resistance even with very high order of mismatch doesn't drastically impact the performance of our practical system. Also, verified from the simulation results is the earlier theory regarding the inability of tree DEM encoder to remove the non-linearity caused by the output resistance, in the absence of mismatches. In addition, simulation results also show that when there are mismatches in the output resistance the DEM encoder again becomes relevant and is able to shape their non-linearity by scrambling the conversion cell order.

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