Applicability of CMOS Digital Isolators in Variable-Frequency Drives

Mikael Lumio

School of Electrical Engineering

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Thesis supervisors:

Prof. Seppo Ovaska

Thesis advisor:

M.Sc. Jari Mäkilä

Aalto University
School of Electrical
Engineering

AALTO UNIVERSITY
SCHOOL OF ELECTRICAL ENGINEERING

ABSTRACT OF THE
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Author: Mikael Lumio

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Supervisor: Prof. Seppo Ovaska

Advisor: M.Sc. Jari Mäkilä

In the last 10 years CMOS digital isolators have emerged, and they are challenging the optocouplers. However, there are concerns regarding the new technology. The development of CMOS digital isolators has been rapid. During the last 10 years many of the concerns have been solved. For example, surge voltage rate was below 10kV/µs preventing the use as a reinforced isolator, but current CMOS digital isolators exceed this limit and are able to fill the requirements for reinforced isolator. Designers are still having concern about the long-term reliability, the EMC characteristics, and the price of the new technology.

Measurements to attain insight about the EMC characteristics of the modern CMOS digital isolators are made in the thesis. The measurements measure the immunity to different EM phenomena. The main goal is to gain knowledge about the differences in EMC characteristics between different manufacturers. In addition, a partial discharge test is made with a goal of finding differences between manufacturers. To understand the cost of the technology, the cost of implementing an isolation function with digital isolators versus a comparison technology is discussed.

The measurements show that there are big differences in the EMC characteristics between manufacturers. The absolute levels indicate that the digital isolators can be used in the variable-frequency drives with caution, but designers are suggested to make more measurements to assess the immunity withstand capabilities in their design. Digital isolators can be cost effective in isolation functions. Optocouplers have a cost advantage if the required turn on/turn off speed is low, such as 3000ns. But if the required speed is at a range of 200ns, digital isolators begin to be more cost effective if the digital isolator volume is high enough.

Keywords: CMOS digital isolator, isolation, EMC, immunity

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Viimeisen kymmenen vuoden aikana digitaaliset CMOS-erottimet ovat tulleet markkinoille haastamaan optoerottimet. Uutta teknologiaa kohtaan on kuitenkin epäilyksiä. Digitaalisten CMOS-erottimien kehitys on ollut nopeaa. Viimeisten kymmenen vuoden aikana monet näistä epäilyistä on saatu ratkaistua. Esimerkkinä, syöksyaaltoluokka oli aiemmin alle 10kV/µs tason, mikä on estänyt käytön vahvistettuna erottimena. Nykyiset digitaaliset CMOS-erottimet ylittävät kuitenkin tämän tason ja täyttävät vaatimukset vahvistetulle erottimelle. Suunnittelijoita epäilyttävät yhä pitkän ajan luotettavuus, EMC-ominaisuudet sekä teknologian hinta.

Työssä tehdään mittauksia uusien digitaalisten CMOS-erottimien EMC-ominaisuuksista. Mittaukset mittaavat erottimien immuniteettia erilaisille sähkömagneettisille ilmiöille. Mittausten päätavoitteena on saada tietoa eroista EMC-ominaisuuksista valmistajien kesken. EMC-testien lisäksi suoritetaan osittauspurkaustesti, jolla haetaan myös tietoa eroista valmistajien kesken. Uuden teknologian hintaa havainnollistetaan tarkastelemalla isolointitoiminnallisuuden toteuttamisen hintoja digitaalisten CMOS-erottimien sekä vertailuteknologian välillä.

Mittaustuloksista nähdään että EMC-ominaisuuksissa on suuria eroja eri valmistajien kesken. Mittauksista saadut absoluuttiset tasot osoittavat että CMOS digi erottimet ovat tietyin varauksin solvetuvia taajuusmuuttajasovelluksiin. Suunnittelijoita kuitenkin suositellaan suorittamaan tarvittavat mittaukset varmistuakseen, että immuniteetti on riittävällä tasolla heidän käytössään. Digitaaliset CMOS-erottimet voivat olla kustanustehokas vaihtoehto toteuttaa eristystarve. Optoerottimet ovat vahvoilla, jos hitaampi nopeus on riittävä, esimerkiksi luokassa “päälle meno/sulkeutumis aika” 3000ns optoerottimet ovat merkittävästi halvempia. Kuitenkin, jos nopeustarve on esimerkiksi luokkaa 200ns, digi isolaattorit alkavat olla kustannustehokkaampi vaihtoehto, jos niiden voluumi on riittävän suuri.

Avainsanat: digitaalinen CMOS-erotin, eristys, EMC, immuniteetti

Preface

The thesis was written for ABB. I want to thank my advisor Jari Mäkilä for the interesting subject. The guidance provided during the thesis aided to understand the needs of ABB for the thesis. Also, I want to thank Jari Mäkilä for taking care of the administrative tasks included in the process. The administrative processes were smooth and did not require a lot of time from me. I also want to thank my Professor Seppo Ovaska for showing interest in the subject.

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Otaniemi, 21.6.2016

Mikael Lumio

Contents

Symbols and abbreviations

Symbols

V_{IOTM}	Maximum transient isolation voltage
V_{ISO}	Isolation withstand voltage
V_{IORM}	Maximum repetitive peak voltage
V_{IOWM}	Working voltage
V_{IOSM}, V_{surge}	Maximum surge isolation voltage
I_{SUPPLY}	Supply current
V_{DD}	Supply voltage
t_{prop}	Propagation delay
$GaAs$	Gallium arsenide
SiO_2	Silicon dioxide
PI	Polyimide

Abbreviations

AC	Alternating Current
BOM	Bill of Materials
CAN	Controller Area Network
CDM	Charged Device Model
CMOS	Complementary Metal–Oxide–Semiconductor
CMR, CMRL, CMRH	Common-Mode Rejection, - Low, - High
CMTI	Common-Mode Transient Immunity
CTI	Comparative Tracking Index
CTR	Current Transfer Ratio
DC	Direct Current
DCL	Decision Logic
EMC	Electromagnetic Compatibility
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
GMR	Giant Magnetoresistive
HBM	Human Body Model
HF	High-Frequency
IC	Integrated Circuit
IEC	International Electrotechnical Commission
LED	Light Emitting Diode
LF	Low-Frequency
IGBT	Insulated-Gate Bipolar Transistor
JEDEC	Joint Electron Device Engineering Council
LPF	Low-Pass Filter
MM	Machine Model
OOK	On-Off Keying
PCB	Printed Circuit Board
PDS	Power Drive System
PWM	Pulse Width Modulation
RX	Receive
SCR	Silicon Control Rectifier
TDDB	Time-Dependent Dielectric Breakdown
TX	Transmit
UL	Underwriters Laboratory
VDE	Association for Electrical, Electronic and Information Tech.

1 Introduction

High currents and voltages that can be hazardous to human are present in variable-frequency drives. To protect the operators from these hazardous currents and voltages international system safety standards require isolation for the variable-frequency drives. Optocouplers have been the default isolation device for four decades. However, optocouplers have some intrinsic problems, such as degradation of the LED and low CMTI. In the last 10 years CMOS digital isolators have emerged, and they are challenging the optocouplers. The development of CMOS digital isolators has been rapid. However, there are concerns regarding the new technology. During the last 10 years many of the concerns have been solved, such as surge voltage rating being less than 10kV preventing the use as a reinforced isolator. But designers are still having concern about the long-term reliability, the EMC characteristics, and the price of the new technology.

Different isolation methods (optoelectric, capacitive, inductive and magnetoresistive) are presented in Section 2. The pros and cons of each method are discussed and a summary is presented. In addition, a summary of the current state of CMOS digital isolator technology and a roadmap for the next few years is presented. Also, the key characteristics concerning the isolation devices are discussed in more detail. Section 3 presents how some of the key characteristics of the isolation devices are defined and measured in the component-level standards. And, as the emerge of CMOS digital isolators has been so rapid, the standards have not been able to keep up, but the IEC standard for non-opto isolators is currently in a draft mode. Section 4 presents how the isolation is used in variable-frequency drive applications, and what are the safety and EMC requirements set by the international system level standards. The cost of implementing the required isolation functions is a major factor, and therefore the cost of implementing these functions with CMOS digital isolators versus a comparison technology is discussed. Typically, CMOS digital isolators need less components with them than optocouplers that is a factor decreasing BOM costs. With less components, assembling costs are also decreased. In addition, the possible PCB area saving also decreases the total function costs.

Measurements are made to attain insight about the EMC characteristics of the modern CMOS digital isolators. The measurements measure the immunity to different EM phenomena. Also, a partial discharge test is made with a goal to gain knowledge about the differences between manufacturers. Although the partial discharge test is used in determining the reliability and lifetime of the isolators, this is not the goal of a partial discharge test in this thesis. The main goal for all of the tests is to compare CMOS digital isolators between different manufacturers. In addition, it is interesting to learn the levels that cause interference with different EM phenomena. The tests are designed with a goal to expose the digital isolators to similar EM conditions that they face in variable-frequency drives, in a way that the EM phenomenon affecting the device is controlled.

2 Technology review

Galvanic isolation is needed to protect systems and end users from potentially hazardous voltages. The currents at which harm or even death can occur are far lower than most people think. These thresholds are demonstrated in Figure 1. Galvanic isolation is also used for breaking ground loops to reduce data transmission errors. Ground loops are physical loops resulting from multiple ground paths between circuits. Noise is induced to ground loops, and since grounds have low impedance the noise currents can be large. This can lead to data corruption. An example of the ground loop interference in data transmission path is shown in Figure 2. The ground loop can be broken by removing the ground connection through the cable using galvanic isolation. This prevents noise currents from flowing between Device#1 and Device#2. [1]

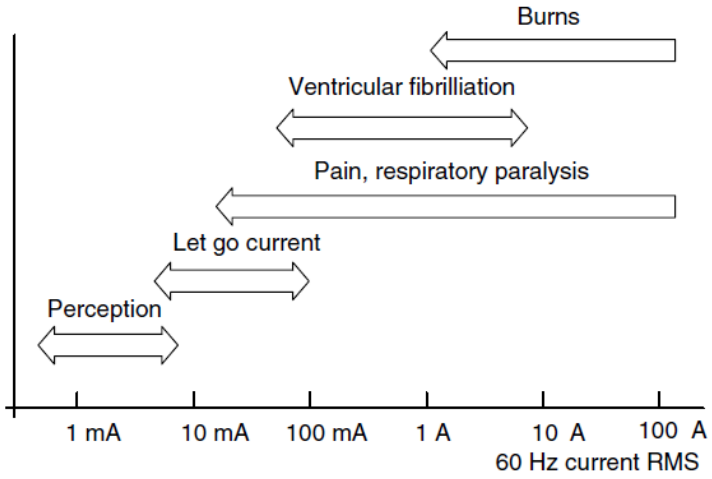

Figure 1: Electric shock thresholds. [29]

Industrial applications must be reliable in harsh environments, where they are susceptible to strong magnetic fields, surges, fast transients, and high noise floors. Such environments set challenges for the isolation. [2] Galvanic isolation can be achieved in multiple ways. For example, data can be transmitted through the isolation barrier by light, inductive coupling or capacitive coupling. Optocouplers have been the default isolation device over the last four decades [2]. However, in the last 10 years, digital isolators have emerged, and they are challenging the optocouplers.

Characteristics of the isolation devices that are relevant to the system design include isolation performance, timing parameters, CMTI, power consumption and package. Data sheets of the devices have parameters related to these characteristics. Parameters describing the isolation performance include maximum transient isolation voltage (V_{IOTM}), isolation withstand voltage (V_{ISO}), maximum repetitive peak voltage (V_{IORM}), working voltage (V_{IOWM}) and maximum surge isolation voltage (V_{IOSM}). Parameters about the timing performance include data rate, propagation delay and propagation delay skew. Parameters of the package include creepage, clearance

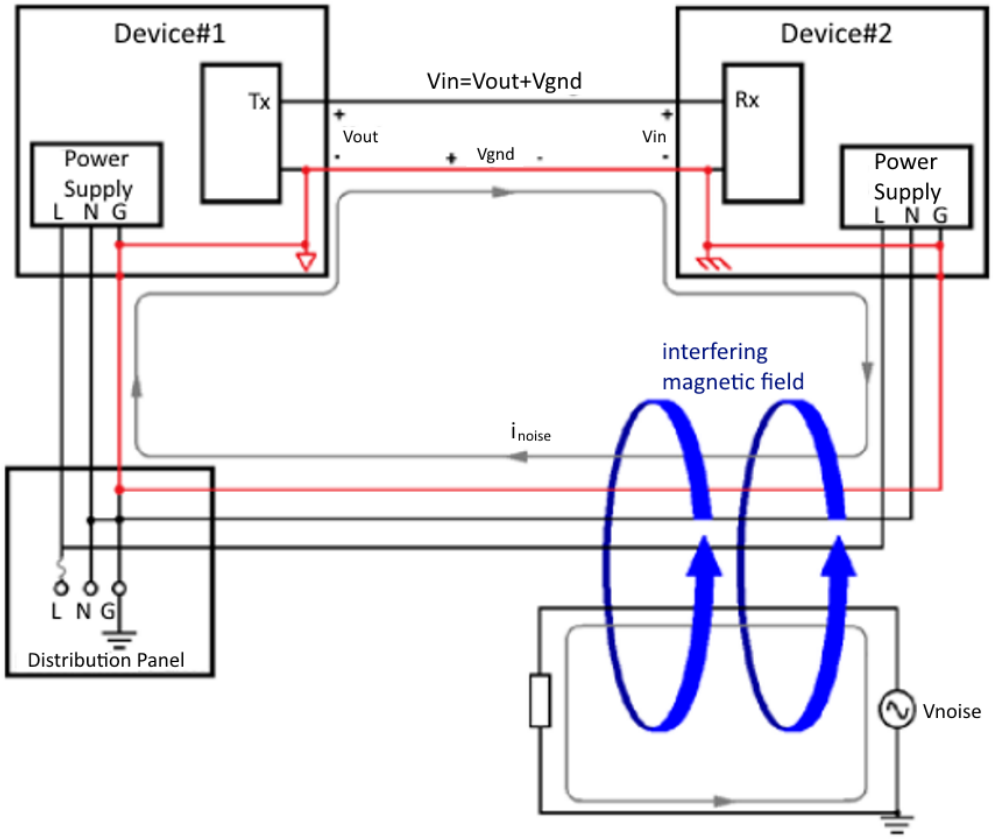

Figure 2: Ground loop interference in a data transmission path. [1]

and Comparative Tracking Index (CTI), and they are mandated by system level standards. [3]

In this section, we present a technology review of digital isolators. We present different isolation technologies, a summary on the current state of the digital isolator technology and a roadmap of what is to come. A comparison between digital isolators using different isolation technologies and optocouplers is made to demonstrate the pros and cons of various technologies.

2.1 Optocouplers

Galvanic isolation in optocouplers is achieved by transmitting the signal optically through the isolation barrier. Optocouplers have a LED that emits light through an optically transparent insulating film or dielectric. The light is then detected by a photo detector, and converted back from light into electrical signal. [2] Usually the optical wavelength is between red to infrared range [4]. The isolating barrier is constructed from a mold compound between the LED and the photo detector. The barrier can be enhanced with an additional isolation layer that is typically polymer based. [5] Optocouplers have a bandwidth ranging from DC to MHz band [4].

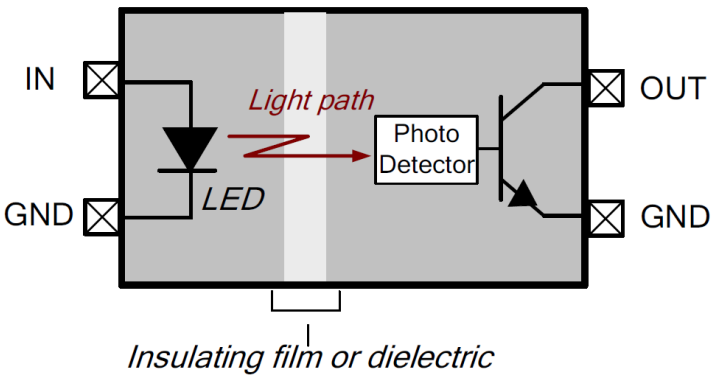

Figure 3: Basic operation of an optocoupler. [2]

The benefits of the transmission method in optocouplers are that the light is inherently immune to external electric or magnetic fields, and it allows for transfer of steady-state information. The disadvantages of optocouplers include speed limitations, power dissipation, low CMTI, and the degradation of the LED.

The photo detector in optocouplers can be, for example, a phototransistor or a photodiode. Phototransistors are inherently slower than photodiodes because of their intrinsic capacitances. For this reason, photodiodes are used in faster optocouplers. Photodiodes are extremely fast, the response time of PIN diodes is in the subnanosecond range. Therefore, signaling rate is limited by delays in the LED and in the biasing circuitry, and not by the photodiode. Fast digital optocouplers include integrated LED drivers and output amplifiers that are optimized for speed. [6, 7]

Parasitic capacitances inherent in optocouplers are limiting the signaling rates [5]. It can be overcome by increasing the intensity of light transmitted. This is done by increasing the LED current at the cost of increased power consumption. [5, 8] Another way to increase the signaling rates is to reduce the light transmission losses by making a thinner isolation barrier. However, this reduces the isolation capabilities. And to retain them, additional layer of material must be composed which increases costs. [8] The signaling rates of optocouplers can reach 50 Mbps, but higher speed optocouplers are many times more expensive than standard low cost optocouplers [6, 8]. For example, Digikey list price for 50 Mbps optocoupler is approximately 3.12 USD, and for commonly used optocoupler (Toshiba TLP719) Digikey list price is approximately 0.69 USD.

The parasitic capacitances also provide a coupling mechanism for transients, and therefore weaken the CMTI performance of optocouplers [5]. Another factor weakening the CMTI is that optocouplers have single-ended architecture [9]. The CMTI performance of optocouplers can be enhanced by using low-cost Faraday shield which decouples the optocoupler input side from the output side. Also, the package is designed so that the input-to-output capacitance is minimized. [10]

Reliability of isolation is an important factor to designers. Manufacturing inconsistency results in uncertainty about designing with optocouplers. Manufacturers of optocouplers have taken effort in addressing manufacturing issues that cause

manufacturing inconsistency. For example, a method to protect against field effect is to protect the phototransistor's PN junctions with a transparent ion screen. Field effect causes changes to the characteristics of optocouplers. It causes slow change over several days in the electrical parameters when voltage is applied. Changes in the electrical parameters of the phototransistor are caused due to the release of charge carriers. High temperature and voltage expose optocoupler to this phenomenon. Using this protection method, the changes in electrical parameters by the electrical field are limited to extremely low values or do not occur at all. [11]

The current transfer ratio (CTR) is one of the key characteristics for optocouplers. CTR measures the ratio of the current used to drive the LED and the resulting output current. [6, 12] The CTR of optocouplers varies between units, operating conditions and time. To guarantee that the optocoupler will continue operational at elevated temperature for device's expected lifetime, the worst CTR has to be assumed in design. Assumption of the worst CTR includes design margin that leads to increased power consumption and slower operating speeds as trade-offs. [13] The light emission characteristics of the GaAs LEDs are dependent on the temperature and device age. The LED degrades over time which can reduce its emission of light by 20% or more. [5, 6, 9, 12, 14] A decrease of 10% in CTR at ambient temperature 80℃ and $I_{\mathrm{F}} = 16mA$ takes between 5 and 15 years depending on the LED type and quality. CTR decrease of over 20% takes between 20 and 30 years. [14] The degradation is accelerated by elevated temperature and LED current [5, 6, 9, 12, 14]. The aging of the LED decreases the timing characteristics of the optocoupler. That is, propagation and rise/fall times are affected, which forces the designer to compensate them together with the temperature dependency, complicating designs and increasing BOM costs. [5, 9] If the CTR degradation is higher than the designer expected the optocoupler might not function properly. Adding a design margin on the worst case CTR introduces additional costs. A compromise with design margins and cost must be made. This causes that some optocouplers might fail due the LED degradation before the expected lifetime of the industrial products that is between 10 to 30 years.

2.2 Digital isolators - CMOS

Digital isolators are based on CMOS-technology. CMOS manufacturing processes have been used for a long time, and they have proved to be reliable. CMOS-technology provides digital isolators several advantages compared to optocouplers. Major advantage is that device operating parameters have only slight variations across voltage and temperature. [15] For example, propagation delay of Texas Instrument ISO7842 changes from 9.9ns to 10.2ns at 5.0V supply voltage when ambient temperature changes from 20 ℃ to 120 ℃. The propagation delay in ambient temperature of 20 ℃ changes from 9.9ns to 12.1ns when supply voltage changes from 5.0V to 2.5V. [16] However, in real applications the supply voltage is usually within 10% from the nominal value and therefore the parameter changes are also withing smaller range. Also, standard CMOS structure provides them with significant advantages in terms of power and speed [5]. The signaling rates of digital isolators can reach 150Mbps, which is three times the rate of the fastest optocouplers.

Digital isolators also have short propagation delays, and low channel to channel and device to device skews. [17] Digital isolators have propagation delays in range of 10 to 20 ns. High-end optocouplers can achieve propagation delays of 20ns, but typical cheap optocouplers have propagation delays of 800ns. The channel to channel skew is 3ns for digital isolators, and device to device skew is 5ns. High-end optocouplers can achieve skews of 16ns, but for typical cheap optocouplers the skews are not defined in the data sheets. System design is also made easier because designers no longer need to take changes in timing parameters due to optocoupler's aging into account [15]. Because digital isolators are compatible with standard CMOS processes it is relatively easy to integrate additional functions to simplify system design and to reduce costs [13]. Another advantage of digital isolators is that each CMOS digital isolator channel occupies little die area, which allows adding more channels on the device. However, crosstalk across the channels, and the creepage and clearance requirements for safe isolation set limits on the channel density and package size. Nevertheless, multiple channels can be added in single device without the cost increasing linearly. As a result, the cost per channel can be decreased significantly by adding more channels within the single device. This is not the case with optocouplers as their complexity directly increases with higher channel count, and so does the cost. [2] Also, digital isolators that are package- and pin-compatible to optocouplers have been developed to make it easier to replace optocouplers in old designs [15].

The supply voltage of digital isolators normally ranges from 3V to 5.5V, but larger range may be supported. For example, Texas Instruments ISO78XX device family can work with supplies down to 2.25V [16]. Digital isolators have a single-ended design and are intended only for isolating single-ended digital signal lines. Devices that have additional functionality integrated along with the isolator are called isolated functions. They may require higher supply voltage to drive the additional functions. [3] A concern with digital isolators is the output state on loss of the input signal. Usually, digital isolators have fail-safe functionality. Fail-safe refers to a determined output state under loss of the input. [6]

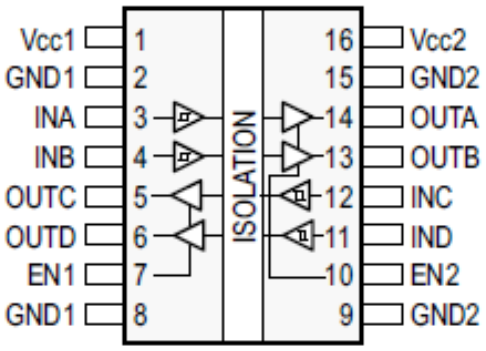

Figure 4: Digital isolator in 16-pin package. [3]

Digital isolators are manufactured using foundry CMOS processes and are limited to materials commonly used in those foundries. Nonstandard materials would complicate production, and result in poor manufacturability and higher costs. The

insulation materials commonly used includes polymers such as polyimide (PI), and silicon dioxide (SiO_2). Both of them have been used for years and polyimide is used in many optocouplers. [8, 13] Polyimide has excellent ESD performance. During ESD events, it absorbs some of the charge to form stable radicals that interrupt the avalanche process and bleeds away some of the charge. Without this ESD tolerant characteristic, the dielectric material may go into avalanche once the ESD level exceeds the dielectric strength, even if the ESD energy is low. [18] Thickness of the silicon dioxide layer is limited because of the inherent stress of the film. This limits the isolation capability achievable with silicon dioxide. Polyimide has lower stress and therefore the thickness can be increased as needed. [19] Compared to optocouplers, the insulation layers are very thin in digital isolators. Therefore, the insulation layers can be subjected to very high electrical field strength in which the aging mechanism is yet to be understood and proven. [20] This raises concerns for the reliability of the digital isolators over time. To support the claims for lifetime predictions of decades at a working voltage, manufacturers of digital isolators have performed accelerated lifetests. Other concerns regarding digital isolators are their ability to withstand overvoltage surges, their immunity to common-mode voltage transients, and immunity to external magnetic and electric field disruptions [13]. In addition, because digital isolators employ CMOS technology, they can be vulnerable to latch-up or ESD damage during system-level ESD, or other overvoltage conditions [21].

Components manufactured employing CMOS process have inherent parasitic PNP and NPN transistors configured as silicon control rectifiers (SCR). When this parasitic SCR is triggered by current injection or overvoltage, a condition known as latch-up occurs. In latch-up, a low resistance appears from V_{DD} to ground, and the low impedance path remains even after the trigger is no longer present. The low impedance path results in a subsequent large current to be drawn through the device. This excessive current may cause damage to the device due to electrical overstress. The damage caused by latch-up can range from complete destruction of the device to parametric degradation. Latent failures could affect the operation later in a system's lifetime. The latch-up is detected by a sustained increase in I_{SUPPLY} after the applicable stress is removed. Usually, latch-up is caused by an overvoltage condition that is beyond the component's absolute maximum ratings. In the system, the source of an overvoltage is not always clear. One of the de facto standard measures recommended in all applications to decrease possibility of a latch-up is adding a bypass capacitor between V_{DD} and ground. The capacitor should be placed as close to the device as possible. If latch-up is noticed during the system level tests, the source of an overvoltage in the system can be recognized. Then, a set of precise actions can be made to the final system design to decrease the possibility of a latch-up condition. Typically, a power cycle is required to eliminate the low impedance path resulted from latch-up. [21, 22] A power cycle means turning the supply voltage of the device off and then on again.

2.2.1 Capacitive digital isolator

Capacitive digital isolators employ capacitance for both isolation and data transmission across the isolation barrier. The galvanic isolation barrier is made of dielectric material between the capacitor plates. And the data is transmitted across the isolation barrier though capacitive coupling and changing electric field. [23] The electrical properties are determined by the plate size, distance between the plates, and the dielectric material [6]. Capacitive coupling has higher dependence on the distance between the plates than inductive coupling on the distance between the coils of the transformer. Therefore, capacitive digital isolators must use thinner isolation layer than inductive digital isolators. [6] For this reason, capacitive isolators employ silicon dioxide in the isolation layer instead of polyimide, because the dielectric breakdown strength of silicon dioxide (1000V/µm) is higher than of polyimide (400V/µm) [18, 24].

The benefits of capacitive digital isolators include immunity to magnetic fields. It enables operation in environments with strong magnetic fields. [6] Also, they use low currents for creating the coupling electric field. This becomes increasingly important with high data rates as the current consumption increases moderately with the data rate. [19] The disadvantage is that capacitors are single-ended, there is no differential signal and the noise and the signal share the same transmission path. However, capacitors can be used in differential pairs to compensate this. [6, 19] The signal frequencies must be well above the expected noise frequency to create low impedance path to the signal and high impedance to the noise [6].

External electric field immunity is a concern for capacitive digital isolators. External fields are seen as common-mode locally by the isolator. The capacitive isolators employ differential isolation by using differential pair capacitors, and the receiver has high selectivity. This architecture rejects interference from a variety of external fields and provides very high CMTI and robust operation, even in electrically noisy environments. [24]

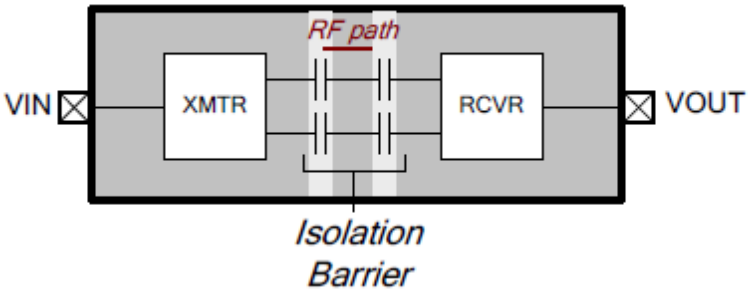

Figure 5: Basic operation of a capacitive digital isolator. [2]

There are two different architectures for the TX and RX circuits that are used to couple the signal into one side of the isolation, and to convert the signal on the other side of the isolation into digital levels. These architectures are: Edge-Based

Communication and On-Off Keying (OOK). In the Edge-Based Communication, a single isolated data channel splits into two data channels, a high-frequency channel with a bandwidth from 100kbps up to 150Mbps, and a low-frequency channel covering the range from 100kbps down to DC. HF-channel is also referred to as an AC-channel, and LF-channel is referred to as a DC-channel. Because both of these channels use differential signaling technique to provide high noise immunity, a total of four isolating capacitors are needed for a single isolated data channel. HF-channel splits the single-ended input signal into a differential signal via the inverter gate at the input. The high-frequency signal can pass the capacitive isolation layer, and the signal is then differentiated into small and narrow transients by the following capacitor-resistor network. The transients are then converted into rail-to-rail differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose outputs feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceed a certain time limit, as happens in case of a low-frequency signal, the DCL switches the output-multiplexer from the high-frequency to the low-frequency channel. Low frequency signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator to create a sufficiently high frequency, that is capable of passing the capacitive isolation barrier. A low-pass filter (LPF) is used to remove the high-frequency carrier before passing the signal on to the output multiplexer. The conceptual block diagram of Edge-Based Architecture is shown in Figure 6. [3, 25]

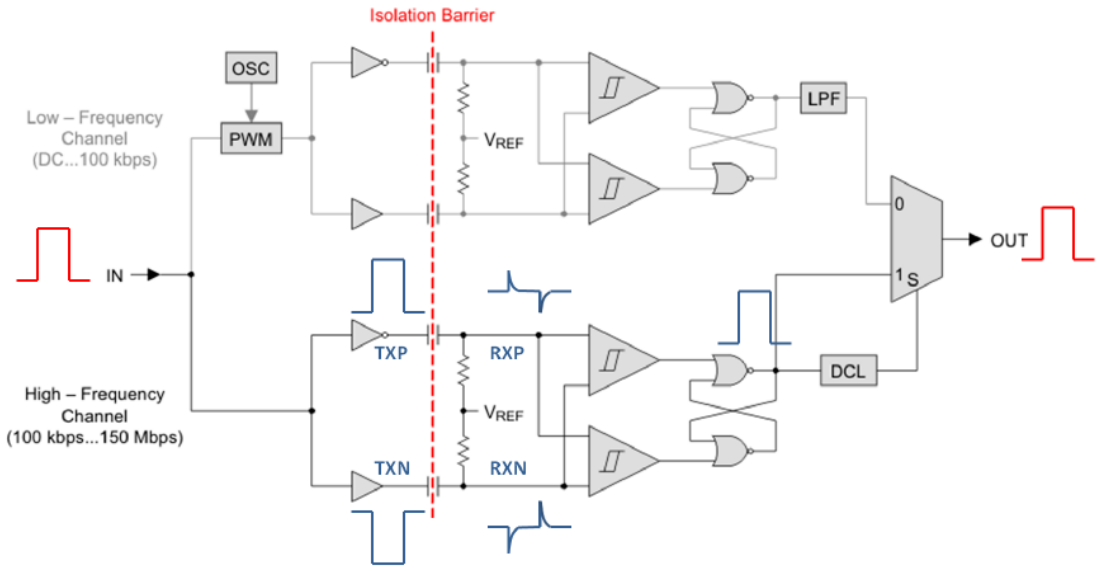

Figure 6: Conceptual block diagram of Edge-Based Architecture. [3]

In the On-Off Keying architecture, the incoming bits are modulated with an internal spread spectrum oscillator clock to generate OOK signaling, where one of the logical input signal levels is represented by transmission of a carrier frequency, and the other signal level by no transmission. This modulated high-frequency signal

couples through the capacitive isolation barrier, and the signal appears on the receive side in attenuated form. On the receive side, a pre-amplifier is used to gain up the incoming signal, and an envelope detector is used as a demodulator to regenerate the digital signal received. Also, CMTI is improved by using the TX and RX signal conditioning circuits. The conceptual block diagram of the OOK architecture is shown in Figure 7. Also, an example of the signal modulation can be seen in Figure 8. [3]

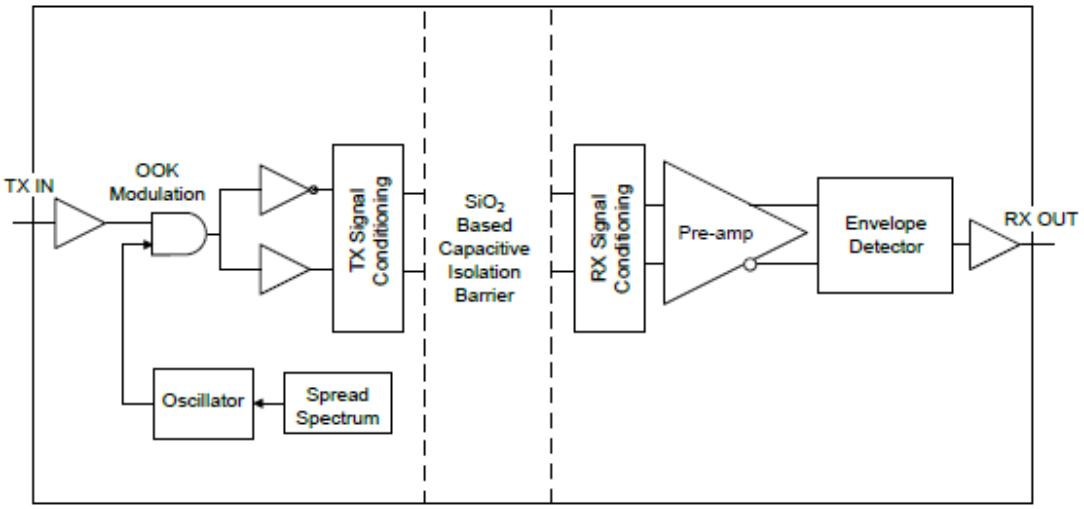

Figure 7: Conceptual block diagram of On-Off Keying (OOK) Architecture. [3]

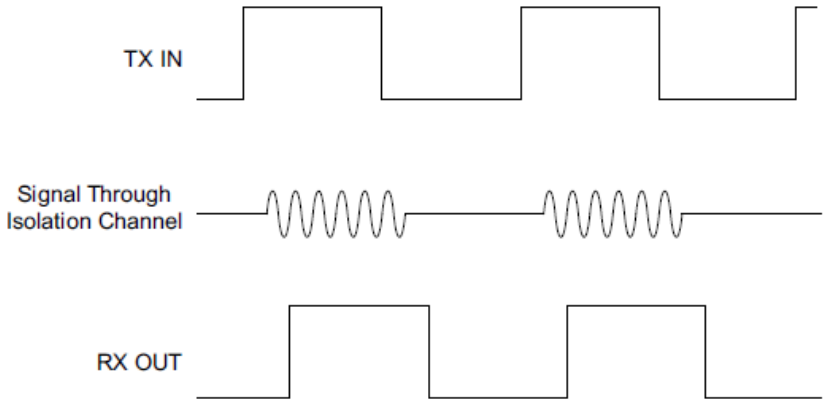

Figure 8: Example of the modulation in OOK architecture. [3]

2.2.2 Inductive digital isolator

Inductive digital isolators employ transformer based isolation method for galvanic isolation. The data is transmitted across the isolation barrier through inductive coupling and changing magnetic field between the two coils of the transformer. [6, 23]

The isolation layer is comprised of polyimide or silicon dioxide [5]. Transmission speed is inherently fast in inductive coupling. Inductive coupling is also differential, and inductive digital isolators have low parasitic capacitances across the isolation barrier. Therefore, it provides excellent CMTI. [5, 13, 26]

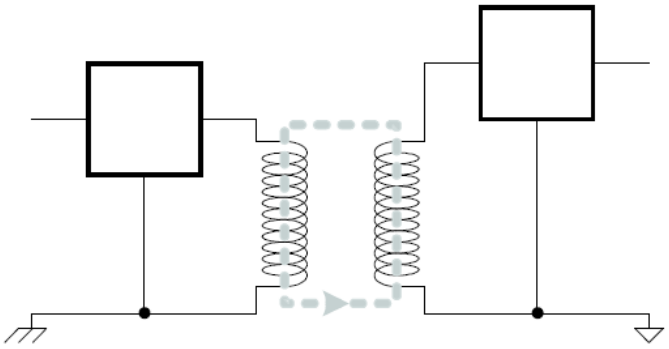

Figure 9: Basic operation of a inductive digital isolator. [6]

Immunity to external magnetic field is a concern for inductive digital isolators. Inductive digital isolators employ air core for the transformers. And because there is no magnetic component present, a problem with magnetic saturation of the core does not exist. Therefore, the immunity to DC magnetic fields is high. The AC magnetic field immunity level is set by the condition in which the induced error voltage in the receiving coil is high enough to cause errors in output or reset the decoder. Coupling of the voltage by external AC magnetic fields is decreased by the small geometry of the receiving coil. The PCB design also plays major role in the AC magnetic field immunity as the loops formed by traces in the PCB form a coupling mechanism for the error voltages. The PCB design is usually the determinative factor. Another concern with inductive digital isolators is the level of electromagnetic radiation emitted from the device, which is decreased by the small geometry of the coils. [27]

Inductive digital isolators use two different architectures for encoding and decoding data. These architectures are: Single Ended Pulse Encoding and On-Off Keying. In Single Ended Pulse Encoding, the rising and falling edges of the signal are encoded as double or single pulses that drive a transformer. These pulses are decoded back into rising/falling edges on the secondary side. Refresh circuits update the DC level regularly. The Single Ended Pulse Encoding architecture is presented in Figure 10. [19]

On-Off Keying (OOK) architecture used in inductive digital isolators is similar to the OOK architecture used in capacitive digital isolators. A high frequency carrier is used to transmit data across the isolation barrier. The OOK architecture used in inductive digital isolators is presented in Figure 11.

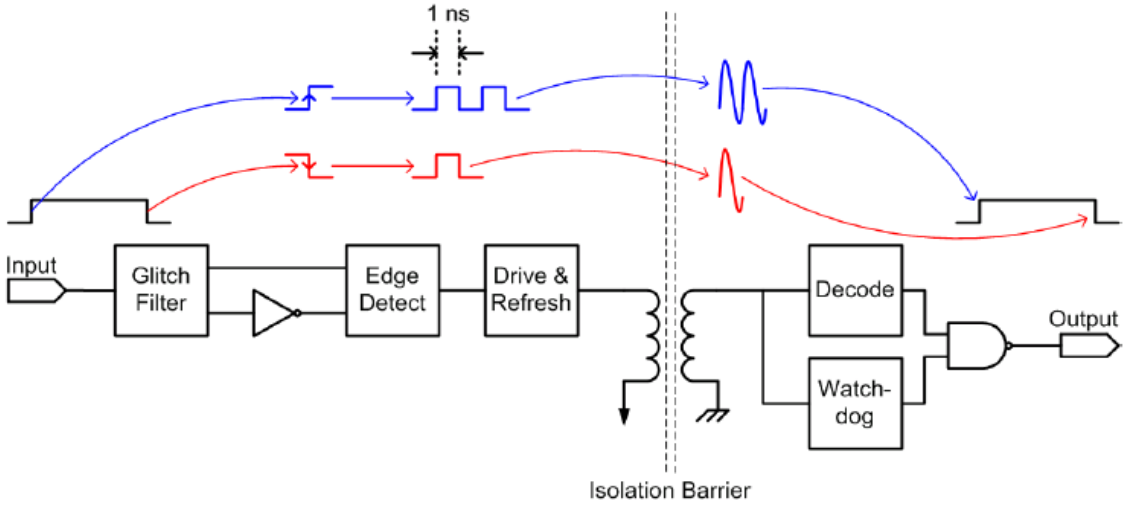

Figure 10: Single Ended Pulse Encoding architecture. [19]

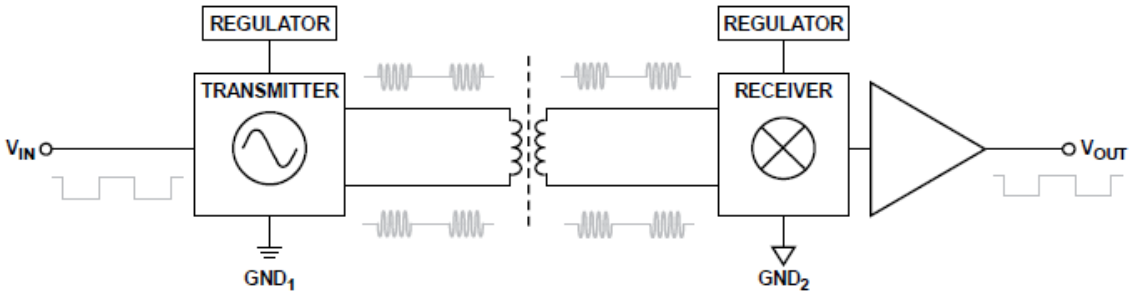

Figure 11: On-Off Keying architecture used in inductive digital isolators. [28]

2.2.3 Magnetoresistive digital isolator

Magnetoresistive digital isolators transfer the signal using a transformer on primary side and a resistor network on the secondary side. The resistors are made of a GMR (giant magneto-resistive) material [6]. The resistance changes when a magnetic field is applied. The circuitry senses the change of resistance and conditions it for output. Both, NVE and Avago, manufacture isolators employing this technology. [6] Magnetoresistive digital isolators are susceptible to induced noise from extraneous external magnetic fields [29].

Magnetoresistive digital isolators use Single Ended Pulse Encoding architecture for encoding and decoding data. The architecture is similar to the one used in inductive digital isolators. The only difference is that the secondary coil is replaced by a GMR network. The architecture detects the edge transition of the input signal and converts these to narrow current pulses that drive the primary coil. [30]

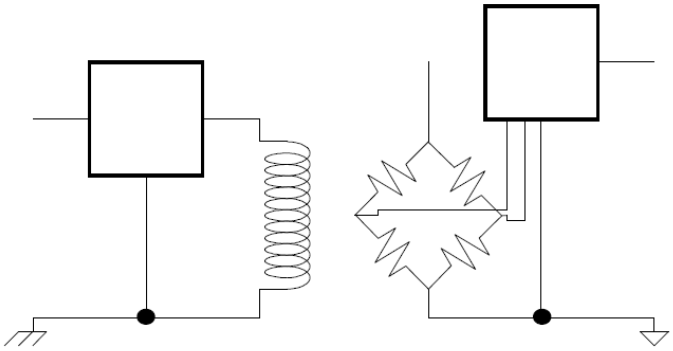

Figure 12: Basic operation of an magnetoresistive digital isolator. [6]

2.2.4 Current state of the technology and future roadmap

The current top-end isolation products and some of their key characteristics are discussed in Section 2.4. The section demonstrates the current state of different technologies. Currently, the highest isolation voltage achievable with digital isolators is $6kV$. This is achieved by NVE's digital isolator that is based on magnetoresistive technology. Texas Instruments has achieved an isolation rating of $5.7kV$ using a capacitive technology. The isolators employing inductive technology have achieved an isolation rating of $5kV$. [31, 32, 33, 34]

Capacitive digital isolator's have been able to achieve a working voltage of $1.5kV$. Working voltage is the voltage that can be applied across the isolation barrier throughout the lifetime of the isolator. The working voltage achieved with GMR technology is $1kV$. Inductive digital isolators are currently limited to working voltage of $600V$. [31, 32, 33, 34] Working voltage limits are derived from time-dependent dielectric breakdown (TDDB). It is an important failure mode of digital isolators. And, it is caused by the impurities and imperfections in the dielectric due to manufacturing and eventually leads in the failure of the dielectric. The effect is accelerated by increasing the electric field across the dielectric and increased temperature. [25] Capacitive digital isolators use silicon dioxide as their insulating material, GMR digital isolators use a unique ceramic/polymer composite, and inductive digital isolators use polyimide [31, 32, 33, 34]. Silicon dioxide has less impurities than polyimide and ceramic/polymer composite and therefore it is more resistant to TDDB and can withstand higher voltage across the barrier over the lifetime of the product [6]. Polyimide used in inductive digital isolators has better surge withstand capabilities than silicon dioxide [36, 40]. Also, the thickness of polyimide insulation layer can be higher than silicon dioxide layer, because of the inherent stresses [19].

Capacitive digital isolators have had a problem with surge withstand ability because they use silicon dioxide as their insulation barrier material. The surge withstand capability was low because the barrier thickness is limited due to inherent stresses in silicon dioxide. [19] However, the new generation of capacitive digital isolators is employing two isolation barriers in series which has increased the surge withstand capabilities on par with inductive and GMR digital isolators. The surge

withstand voltage for all technologies is currently at $12.8kV$. [31, 32, 33, 34]

The current consumption with lower signal rates is similar between all of the digital isolator technologies. The current consumption per channel for digital isolators at data rate of $10Mbps$ is approximately $2.5mA$. Capacitive digital isolators have been superior in terms of current consumption at higher data rates, but the new generation of inductive digital isolators has reached similar level. The change is due to the different architecture in sending the data across the isolation barrier. Inductive digital isolators can achieve dynamic current consumption comparable to capacitive technology by using On-Off Keying architecture. OOK has higher quiescent current consumption than the single ended pulse encoding architecture used in earlier generation products. The total current consumption for inductive digital isolators turns in favor for the OOK architecture at data rates above $10Mbps$. Magnetoresistive digital isolators have very high dynamic current consumption. The current consumption per channel for each technology achieved at data rate of $100Mbps$ is approximately $5.5mA$ for capacitive and inductive digital isolators, and $20mA$ for magnetoresistive digital isolators. [31, 32, 33, 34]

The propagation delay, channel to channel and part to part skews are similar across all the digital isolator technologies. Propagation delays are in the range of 7.5 to 16ns, channel to channel skews in the range of 1 to 3ns, and part to part skew in the range of 3 to 6ns. Capacitive digital isolators have currently achieved the best CMTI. The CMTI achieved by capacitive digital isolators is $100kV/\mu s$. Inductive digital isolators have achieved CMTI of $75kV/\mu s$. CMTI is one of the main weaknesses of the GMR digital isolators, they have achieved only a CMTI of $30kV/\mu s$, which is the same achieved by the high-end optocouplers. [31, 32, 33, 34]

Data rates of digital isolators are between 100 and $150Mbps$. [31, 32, 33, 34] An indication of the performance that can be attained with digital isolator is that NVE has prototype devices with signal rates of 300Mbps and a switching time less than one nanosecond. The device speed is expected to increase as ICs scale down and become faster, as the limiting factor is currently not the coupling structure but the silicon electronics. [35]

Manufacturers of digital isolators aim to improve the surge withstand capability further. Inductive digital isolators have lower working voltages than other technologies, but the gap is expected to be closed in the future. Different architectures to transmit and receive data across the isolation layer are also being developed. Each architecture has its pros and cons, for example one might have lower propagation delays but it comes at a cost of increased current consumption. Manufacturers aim to bring digital isolators with higher isolation voltage ratings and higher channel counts. Manufacturers are also interested in enhancing the noise immunity and decreasing the radiated emissions of the digital isolators. Enhanced noise immunity increases the margin for the system to remain operational under the harsh industrial environment. The radiated emissions from the digital isolators could cause distraction to the surrounding control electronics, if the emission level was high enough. Therefore, being able to reduce the emissions further increases the margin for system to operate properly. The emissions are a result of coupling the signal electrically across the isolation barrier in CMOS digital isolators. Optocouplers use light to couple the

signal across the isolation barries, and therefore, the emission is a charasteristic of CMOS digital isolators.

2.2.5 Forecast on the direction of the market

Digital isolators are manufactured using standard CMOS processes. These are mature and cost-effective processes. [24] Therefore, the price of digital isolators is not expected to become down by the development of the manufacturing process. A possible decrease in the prices could become from increasing volumes, as more and more designers are starting to use digital isolators to fulfill their isolation needs. This would allow the non-recurring development costs to be spread over more units.

Another factor that could lead to downward pressure on the price of digital isolators is the ever increasing competition in the market. New companies have joined the isolation component market along the old companies with the emerge of the digital isolators. Also, when in a longer term digital isolator technologies mature and the products become bulky, in other words the products between manufacturers will be highly similar, the manufacturers lose their pricing power that they were having by differentiating their products and owning patents. This is closer to perfect competition, and the price of the digital isolators faces downward pressure from this effect. This effect becomes more powerful if the technology develops slowly, and it reaches its full power if the technology is fully matured and the patents on it have been expired. Currently and in foreseeable future, the technology is developing rapidly and new patents are issued. Therefore, the full effect of technology maturation is not expected to happens in next decade or two.

2.3 Key characteristics

2.3.1 Working voltage and isolation voltage rating

Two ratings characterising the isolation capabilities of the isolator are working voltage and isolation voltage. Working Voltage (V_{IOWM}) quantifies the ability of an isolator to handle continuous DC or AC voltage across the isolation barrier over its lifetime [36, 37]. Isolation Voltage quantifies the ability of an isolator to handle an overvoltage condition for very short periods of time. Overvoltage conditions are caused by unintentional disturbances in the system. The overvoltage can be several times the line voltage and the isolator should be able to handle the overvoltage without damage. [36, 37] This sets a challenge for the manufacturers as the isolation devices are expected to have a lifetime of 10 to 30 years in industrial applications.

It is important to not interpret the isolation voltage as a working voltage [38]. Both of these ratings are defined in the component level standards. The test methods for specifying these voltage ratings for the isolators are presented in Sections 3.1 and 3.2.

2.3.2 Surge voltage rating

Surge levels are critical in defining the quality of isolation. An isolator must pass 10kV(peak) surge voltage testing to be able to achieve a reinforced insulation rating to the VDE 0884-10. The surge voltage rating of a digital isolator defines survivability after a repetitive series of short duration high voltage pulses. A 1.2/50 µs surge pulse is used in the test. The pulse waveform is presented in Figure 18. The test pulse is injected for a minimum of 5 times for both polarities, and the time between successive impulses is less than one minute. [39] The ability to pass a surge voltage test is primarily determined by the insulation thickness and the quality of the insulating material. The applied electric field tends to concentrate at defect points within the insulator, therefore lower defect densities generally lead to higher breakdown ratings. Also, thicker materials are more resistant to breakdown since the field strength is inversely proportional to the distance between the insulation. [36, 40]

Optocouplers usually pass the 10 kV surge testing because the insulation is very thick (typically 400 μm), which reduces the impact of insulation quality on the breakdown characteristics. Inductive digital-isolators use a high quality 20 μm to 32 μm polyimide layer deposited in a clean room environment. Since this material has a much lower defect level than the injection molded epoxies used in optocouplers, a much thinner layer can still meet the 10 kV requirement. Capacitive digital-isolators also use a high quality insulating layer, made from silicon dioxide (SiO_2) deposited during wafer fabrication. Silicon dioxide has a high dielectric strength but typically cannot be deposited in very thick layers without creating mechanical stress within the film. Thicker insulation layer also reduces the capacitance, which weakens the coupling efficiency across the barrier. Therefore, capacitive isolators have had troubles with passing the 10kV surge test, and have not been able to be certified by VDE as reinforced insulation. [36, 40] However, the new generation of capacitive digital isolators has been able to enhance the surge withstand capability by using two capacitive isolation barriers in series. Currently, the capacitive digital isolators are on par with other technologies in their surge withstand capability.

2.3.3 Common-mode transient immunity

Common-Mode Transient Immunity (CMTI) is one of the key characteristics for isolating devices such as digital isolators and optocouplers. High-slew-rate (high-frequency) transients can cause data corruption across the isolation barrier. Local parasitic paths on the isolator or circuit board can couple across the isolation barrier and provide a path for these fast transients possibly corrupting the output signal. [23] Common-mode transients are one of the leading causes of data corruption in isolation applications [24]. The CMTI is a measure of how well an isolator will reject these common-mode transients across the barrier without the data communication being disrupted by the transients. CMTI is usually measured in units of $kV/\mu s$. [8]

CMTI is measured in three different ways. Two of them are measured under static DC input/output condition. They are CMRL and CMRH. CMRL is used to denote CMR measured when output logic is low, and CMRH for output logic high. These measurements may be inadequate, because they correspond to the same

condition when the end application is in an idle, standby mode. However, it is critical to understand the CMR performance when the system is active with the isolator's input and output signals changing momentarily. The CMR performance when the inputs and outputs are switching is denoted by a dynamic CMR specification. [10]

CMTI measurement setup is shown in Figure 13. The dynamic CMR setup is similar except that an oscillator is connected to provide the switching input signal.

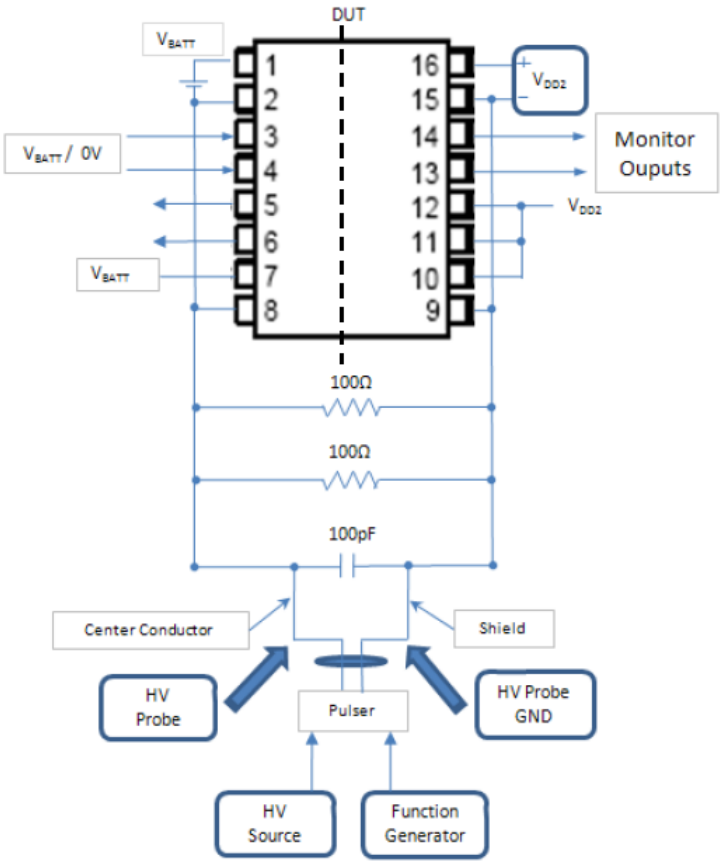

Figure 13: Typical CMTI Setup. [23]

2.3.4 Electrostatic discharge (ESD)

Electrostatic discharge (ESD) is the transfer of charge between two objects at different potentials and is caused by contact or an induced electric field [41]. ESD causes high-voltage transients across the isolation. Protection against ESD is conventionally achieved by using high-voltage diodes, but using them across the isolation barrier would violate the galvanic safety isolation requirements, and therefore is not allowed. [20] In addition, board-level ESD protection devices on one side of the isolation barrier cannot be employed, because major portion of the energy of an across the barrier strike appears as a common mode for the ESD protection device [41]. Therefore

the insulation material and construction of the device must withstand high ESD transients without insulation degradation [20].

The ESD robustness is measured in two levels: component-level and system-level [21]. Component-level ESD robustness is assessed by JEDEC standard models such as human body model (HBM), charged device model (CDM) and machine model (MM). System-level ESD performance test is defined in the IEC 61000-4-2 standard. [41] Component-level ESD test is the most useful in determining a device's robustness to handling by humans and automated assembly equipment prior and during assembly into a system. It is less useful in determining the robustness within a system subjected to system-level ESD events. [21] There are two reasons for this: [21]

- System- and component-level ESD testing have different objectives. The component-level tests are designed to address conditions typically endured during component handling and assembly. Whereas, the system-level tests are designed to address conditions typically endured during system operation.
- Board/module/system design has strong influence on the specific conditions the component is subjected to. The system design can impose a more severe voltage transient onto a component than is imposed on the system at the test point.

2.3.5 Max data rate and current consumption

The maximum data rate is limited mainly by the intrinsic parasitic capacitances in the optocouplers, and by the CMOS technology in digital isolators. The coupling technology is not the limiting factor. However, the data rate can have a significant impact on the current consumption. The coupling technology and the architecture used have significant impact on the current consumption characteristics. The increase in current consumption with increased data rate is characterised by a dynamic current consumption.

The current consumption of the isolator is dependent on the internal construction. Inductive isolators have always one channel per input, and increasing the channel count of the device leads to proportional increase in the current consumption. A capacitive digital isolator using an edge-based architecture splits the input into two separate channels, DC-channel and HF-channel. Therefore, the channel count in capacitive digital isolators with edge-based architecture is higher than the channel count in inductive digital isolators with same channel configurations. More channels in similar configurations show up as increased DC current consumption. However, this difference mitigates with increasing channels in the isolator. The reason for this is that a capacitive digital isolator using edge-based architecture only needs one DC-channel for each side of the transmission. This single DC-channel per one transmission side is then multiplexed across all AC-channels in the same direction. [25]

DC currents occur when the systems are idling. However, in most cases, the digital isolators are not idling but transferring data. Capacitive digital isolators need

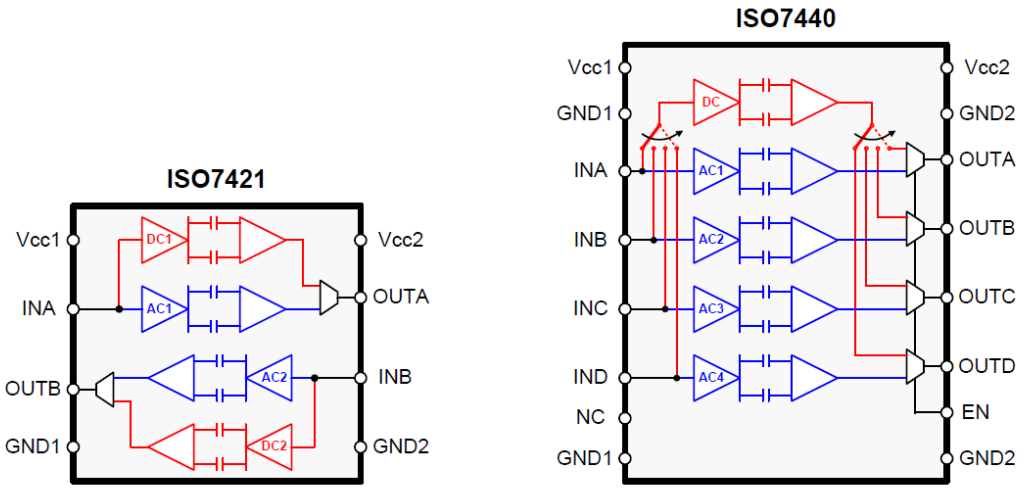

Figure 14: Channel construction in dual- and quad-channel capacitive digital isolators (Edge-based architecture). [25]

only very low currents for transmitting the data capacitively across the isolation layer, and this makes their current consumption very good at higher data rates. Inductive isolators use fast pulses in transmitting the data so the average current is not very high. The dynamic current consumption of capacitive digital isolators used to be significantly lower than of inductive digital isolators. However, the new generation of inductive digital isolators employing OOK architecture have achieved comparable dynamic power consumption to capacitive digital isolators. The enhance in dynamic current consumption has come at a cost of increased quiescent current consumption, that is still at a comparable level to capacitive digital isolators. The current consumption for the current generation inductive and capacitive digital isolators at data rate of 10Mbps is approximately 3mA per channel, and at data rate of 100Mbps approximately 7mA per channel. The graphs shown in Figures 15 and 16 demonstrate the effects of channel configuration at low signal rates and the difference in coupling technology with higher signal rates. The channel construction of these devices is shown in Figure 14. [25]

The current consumption of digital isolators and optocouplers is so low that it is not a determinant factor in variable-frequency drives. The power consumption is negligible to affect the efficiency coefficient of the drive, and the heat generation is also negligible. [42]

2.3.6 Max propagation delay and propagation delay skew

Important charasteristic of isolators is the max propagation delay. It measures the time it takes a signal to pass through the isolation barrier. The propagation delay skew is also important characteristic. [5] It defines the difference between the min and max propagation delays for any given group of isolators operating under the same conditions [24].

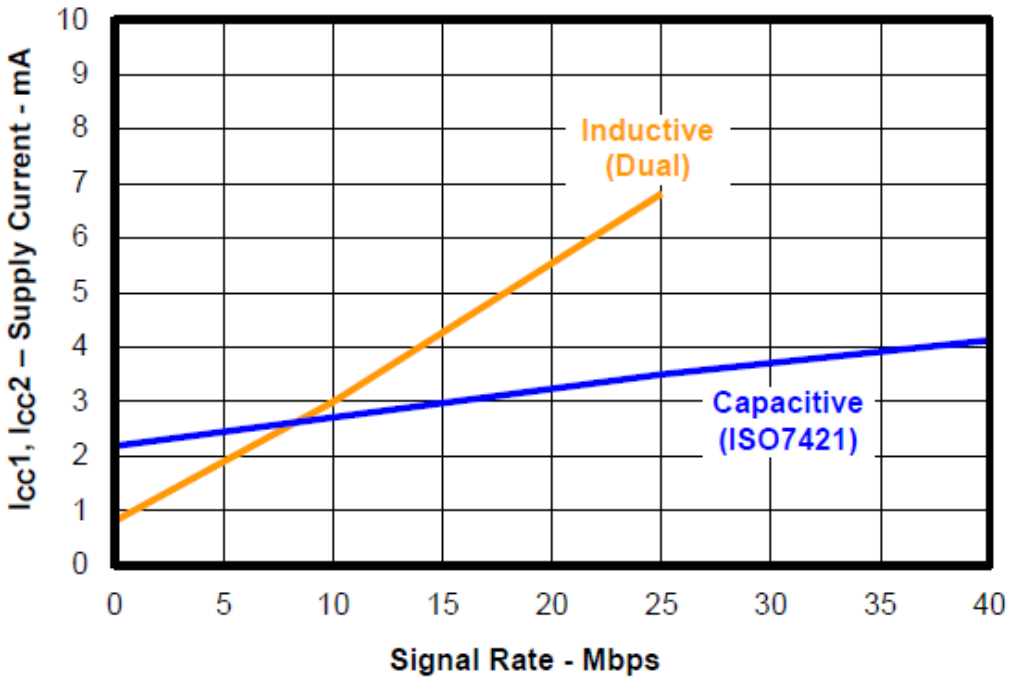

Figure 15: Current consumption versus signal rates of dual digital isolators. [25]

Digital isolator's have smaller channel to channel and device to device propagation delay skew than optocouplers. Typical channel to channel skew for digital isolators is approximately 3ns, and device to device skew is approximately 5ns. For high-end optocoupler the skew is approximately 16ns, and for typical low cost optocoupler the skew is not specified in the datasheets. Also, the propagation delay in digital isolators is not affected as much by temperature and aging as it is in optocouplers. The propagation delay of digital isolators stay within approximately 5% of its value at ambient temperature of 25℃ over the temperature range of -60 to 120 ℃ [16]. The propagation delay of optocouplers is stable across temperatures -40 to 35 ℃, but then begins to increase drastically and can increase over 15% of its value at room temperature when temperature is increased to 75℃. [24] The temperature and aging effects in optocouplers enforces the designer to add margins in the timing characteristics of the isolator. Because these values are not listed in the data sheets, the designer must decide how much margin is enough for the component to function for the lifetime of the product. However, there are some models that help take the temperature and aging effects into account, the needed margin to be on the safe side needs to be significant in any matter. These models include, for example, Lindquist's relative CTR degradation model and a model developed by J. Ben Hadj. Slama et. al. [43] Digital isolators match better to their datasheet values across the whole operating temperature range, and lower margins on timing characteristics can be used in design. Smaller propagation delay skew provides the designer possibility to use lower margins in timing considerations. More predictable timing also provides

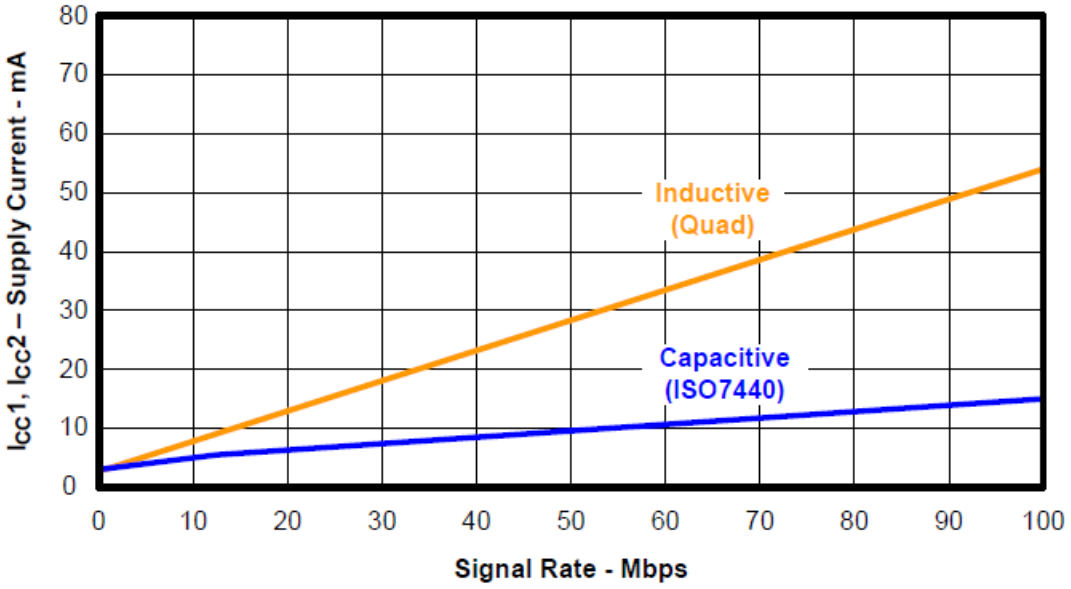

Figure 16: Current consumption versus signal rates of quad digital isolators. [25]

both performance and safety. [5, 24]

2.3.7 Reliability

Isolation device's isolation capabilities are determined mainly by the dielectric that makes up the isolation barrier. All dielectrics exhibit aging. And at some point in time, the voltage-withstand capabilities no longer match the specifications. Aging is caused primarily by dielectric degradation from thermal and/or electric energy fields. Aging for particular dielectric is determined by the inherent material and manufacturing properties, such as impurities and defects. Aging is non-reversible process. At the point of dielectric fatigue or failure, avalanche current flows through the dielectric causing permanent damage to the dielectric. All isolation device manufacturers provide an isolation lifetime estimate. Currently, the isolation lifetime estimates for CMOS digital isolators range from 20 to 50 years. It implies that at the end of this time period, the component's dielectric properties can no longer be guaranteed. And, at the end of the period, the devices are no longer guaranteed to function as isolators. The failure mode for all isolators is a resistive short between the previously isolated sides. The failure mechanism is independent of the coupling technique and applies to all isolators. It is a fundamental dielectric property. [24] This failure is also referred to as time-dependent dielectric breakdown (TDDB) [25].

The lifetime expectations for the equipment industry range from 10 to 30 years. The lifetime expectancy of an isolator is determined by the time-dependent dielectric breakdown intrinsic to all dielectrics. [25] However, optocouplers make an exception. The lifetime of optocouplers is more often limited by the degradation of the LED and not by a breakdown in the isolation material, especially when used at high

temperatures. [8] There are multiple models for determining the lifetime expectancy of the dielectric. These models include E-model, 1/E model, a combination of the two and other lesser-known models. [24] The TDDB E-model is the most widely accepted model for dielectric breakdown [25].

The TDDB can also be determined practically by applying a stress voltage across the isolator, while maintaining the ambient temperature at 150 °C. A timer is started at the start of the test, and it stops when the current through the isolator exceeds $1mA$, indicating a dielectric breakdown. The practical test is presented in Figure 17. The time-to-failure from the measurement is plotted against the theoretical E-model curve for each test voltage. The practical TDDB tests made by Texas Instruments have matched the predictions of the E-model. [25]

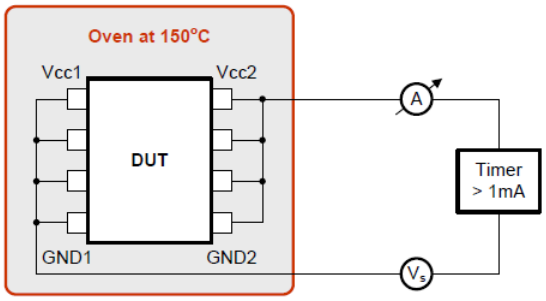

Figure 5. TDDB test methodology.

Figure 17: The setup for practical measurement of TDDB. [25]

2.4 Comparison summary

This section summarizes the comparison between different technologies employed in digital isolators. A set of digital isolators with the most relevant characteristics are presented in Table 1. The working voltage V_{IOWM}, which is the voltage the isolation carrier can withstand throughout its lifetime is approximately $1kV$ for all of the technologies, excepts for the inductive technology, which currently has a maximum working voltage of $600V_{\text{RMS}}$. The top-end device in terms of working voltage is Texas Instrument's ISO7842DW having a working voltage of $1.5kV_{\text{RMS}}$.

All of the isolation technologies are capable of withstanding surges over $10kV_{\text{PK}}$, which is a widely used gold standard for reinforced isolation. All of the isolation technologies have some products that have passed the surge voltage test with surge voltage of $12.8kV_{\text{PK}}$. Because the isolation barrier thickness is substantially higher in optocouplers than it is in digital isolators, optocouplers do not have problems passing the surge test. All isolation technologies have a 60s isolation withstand capability of over $5kV$. NVE has been able to achieve the highest isolation voltage rating at $6kV$, with Texas Instrument as second at $5.7kV$.

Capacitive and inductive digital isolators are able to achieve high CMTI values. A capacitive digital isolator, Texas Instrument's ISO7842DW has a CMTI of $\pm 100kV/\mu s$, which is the top-end value currently. Analog Devices has achieved a

Table 1: Comparison summary of digital isolators.

Type	Tech	V_{IOWM} V_{RMS}	V_{surge}* kV_{PK}	V_{ISO} kV_{RMS}	t_{prop} ns (max)	CMTI $kV/\mu s$	Current per ch** mA	D.rate Mbps (max)	Skew*** ns (max)
TI ISO7842DW	Cap OOK	1.5k	12.8	5.7	16	± 100 (min)	2.1/6.9	100	2.5/4.5
Silabs Si8642ET	Cap OOK	848	10	5	13	± 60 (min)	2/5.5	150	2.5/4.5
Maxim MAX14936C	Cap OOK	848	10	5	7.5	± 25 (typ)	3.2/9	150	0.9/3
AD Adum241E	Ind OOK	600	12.8	5	13	± 75 (min)	2.9/5.5	150	3/6.1
NVE IL716VE	GMR Edge	1k	12.8	6	15	± 30 (min)	3.2/21.2	100	3/6
Toshiba TLP719(F)	Opto	806	20	5	800	± 10 (min)	16	1	-
High-end	Opto	1k	20	5	22	± 30 (min)	16	50	16

*V_{surge} is the test voltage used in surge test. Surge rating for reinforced isolators is the test voltage divided by 1.6 , and the rating for basic isolators is the test voltage divided by 1.3.
**a/b, where a is the typical current consumption at data rate of 10Mbps, and b is the typical current consumption at data rate of 100Mbps.
***a/b, where a is the maximum channel-to-channel skew time, and b is the maximum part-to-part skew time.

CMTI of $\pm 75 kV/\mu s$ with their inductive digital isolator Adum241E. The GMR technology has only been able to reach CMTI of $\pm 30 kV/\mu s$ with their magnetoresistive digital isolator IL716VE, which is at the same level the top-end optocouplers can achieve. However, CMTI of a typical optocoupler is only at approximately $\pm 10 kV/\mu s$. The coupling method of the isolator is not the only thing affecting the CMTI as can be seen in that Maxim Integrated has a CMTI of $\pm 25 kV/\mu s (typical)$ with their capacitive digital isolator MAX14936C versus the $\pm 100 kV/\mu s$ of Texas Instrument's. However, the higher CMTI of the digital isolators has come at the expense of increased propagation delay.

The propagation delays of the digital isolators are very low. The propagation delays of the high-end optocouplers are at the same range, but the propagation delay of a typical optocoupler is multiple times higher. Digital isolator's have a benefit that their channel to channel and part to part skews are very low at approximately

$3ns$ (ch-ch) and $5ns$ (part-part). The optocoupler's cannot match digital isolators in skew performance. The high-end optocouplers have a skew of 16ns, and for a typical optocoupler it can be even higher and in many times it is not specified. When the maximum propagation delay of the optocoupler is $800ns$ and the skew is not specified, the designer has to add a high design margin for the skew if he is using multiple isolating devices and/or channels.

Digital isolators can achieve data rates up to $150Mbps$, NVE and Texas Instruments specify data rates up to $100Mbps$. The maximum data rates of digital isolators exceed the maximum data rate of optocouplers by a wide margin. The fastest optocouplers have data rates up to $50Mbps$. The current consumption of digital isolators at a data rate of $10Mbps$ is approximately $2.5mA$ for all of the digital isolator technologies. The current consumption at a data rate of $100Mbps$ is also very close between inductive and capacitive digital isolators at approximately $7mA$. The new generation of inductive digital isolators employs an OOK architecture for transmitting and receiving the data, versus the edge based communication used in earlier generation devices. The OOK architecture has provided inductive isolators very good dynanic current consumption rating and their current consumption has become on par with the current consumption of capacitive digital isolators even at very high data rates. However, this progress has not yet affected the GMR technology devices. The magnetoresistive digital isolator has a current consumption of approximately $3mA$ at data rate of $10Mbps$, but the current consumption increases to $21mA$ at a data rate of $100Mbps$. Optocouplers draw current mainly to light up the LED, this current is usually approximately $16mA$.

3 Isolation standards

Electrical insulation is a function of safety, and therefore isolation components are subject to regulatory requirements and approvals that can be country and industry specific [10]. Safety standard can be separated into three broad categories: system level standards, support standards, and component certification standards [44]. The system level safety standard for variable-frequency drives is IEC 61800-5-1, and the requirements it sets for the isolation components are presented in Section 4.2. The system level safety standard does not specifically address isolators, but it is, nonetheless, relevant to isolators because it specifies requirements for the isolation components, such as transient voltage withstand, and the minimum creepage and clearance distances [44]. This section presents some of the characteristics specified in the standards of different categories.

Safety standards specify different levels of insulation. Functional isolation is used to allow a circuit to operate properly. It does not necessarily provide protection from shock. Sufficient shock protection is provided by insulation that is referred to as basic insulation or reinforced insulation in the IEC standards. [36] The IEC 60664 insulation coordination safety standard defines following levels of insulation: [38]

1. Functional Insulation: insulation necessary for correct operation of the equipment between parts of different potential.

2. Basic Insulation: insulation needed to provide basic protection against electrical shock between a part and hazardous voltage and an earthed ground. The basic insulation is considered to be shorted under a single fault condition and therefore is not failsafe.

3. Supplementary Insulation: independent insulation applied in addition to basic insulation in order to ensure protection against electrical shock in the event of failure of basic insulation.

4. Double Insulation: insulation comprising both basic insulation and supplementary insulation.

5. Reinforced Insulation: a single insulation system which provides a degree of protection against electric shock equivalent to double insulation. It provides two levels of protection, making it failsafe.

In order to provide uniform specification and testing of isolators and electrical systems employing isolation national and international standards have been developed over time. Number of international standards related to electrical safety are published by the International Electrotechnical Commission (IEC). In addition, regional specifications are published by the Underwriters Laboratory (UL) in the US, and Verband der Elektrotechnik (VDE) in Germany. Testing and certification to these standards are provided by several entities. Both invidual components and end systems can achieve safety certifications, and certification requirements can vary in different regions of the world even if they reference the same base safety standards.

However, standards bodies have been working to harmonize the international and regional documents to simplify the certification process. But because the standards are complex and there are many of them, the harmonization takes time. During this period components have to meet specification of multiple standards to support worldwide sale of the end equipment. [36, 45] The harmonization of the standards could therefore provide efficiency and cost savings in the future.

Each agency might handle various parameters differently, which might complicate the harmonization. For example, UL 1577 documents the creepage and clearance achieved and verifies survival to the specified withstand voltage, but there is no specific requirement on creepage or clearance as long as the components pass the test. However, for example, the system level safety standard IEC 60950 for information technology equipment mandates specific creepage and clearance requirements based on the working voltage. These requirements must be met regardless of the test results. Also, some of the standards are written specifically for optocouplers. A standard addressing digital isolators that use inductive or capacitive coupling was released by VDE in 2006, the standard is VDE 0884-10. [36]

Safety standards specify several physical and electrical characteristics of the isolator. In order to withstand specific voltage stresses, the insulating properties of the component, as well as the physical dimensions of the packaging and insulation barrier are specified. Voltage levels may be specified as a peak voltage or in RMS terms. [36] Next, some of the most important characteristics specified in the standards are presented.

3.1 Maximum repetitive peak voltage and working voltage

Maximum repetitive voltage (V_{IORM}) and Working Voltage (V_{IOWM}) both quantify the ability of an isolator to handle continuous DC or AC voltage across the isolation barrier over its lifetime [36, 37]. Both values are defined in IEC 60747-5-5 and VDE 0884-10. Maximum repetitive voltage is defined as a peak voltage that the isolator can withstand, whereas working voltage is defined as maximum RMS, or equivalent DC voltage, that the isolator can withstand over a specified long term. [37]

Both of these values are specified by the manufacturer of the isolator based on their own testing. Standards VDE 0884-10 Ed 1.0 and IEC 60747-5-5 use partial discharge test that looks for localized discharges inside the insulation to determine V_{IORM} and V_{IOWM}. This partial discharge test is performed along with the test for V_{IOTM} using Method A test during certification and Method B1 in production. [37]

Additional requirement on V_{IORM} and V_{IOWM} is included in Ed 2.0 of the VDE 0884-10. In the Ed 2.0 manufacturers of a reinforced isolators must provide accelerated-stress test data to the certifying agencies to prove that the isolator can handle 1.2 times V_{IORM} / V_{IOWM} for more than 37.5 years. An accelerated-stress test is performed at both high temperature (150 °C) as well as room temperature (25 °C). During the stress tests, the isolator is subjected to varying levels of high voltage, that is much higher than the expected working voltage. The time it takes to breakdown are recorded, and the voltage vs. time curve is extrapolated for lifetime prediction at the expected working voltage. The relation between time-to-failure and stress

voltage is exponential for the isolators that use silicon-dioxide (SiO_2) as the insulation material. This means that the log of expected time to failure reduces linearly with the applied voltage stress. The standard requires that these isolators use this relation to curve-fit the test data. [37]

The accelerated stress tests mandated by the VDE 0844-10 Ed 2.0 give more confidence in the long-term reliability of the isolator for continuously applied high voltage compared to the partial discharge test mandated by IEC 60747-5-5 and VDE 0884-10 Ed 1.0, since there is no established relationship between long-term withstand capability and partial discharge for digital isolators. [37]

3.2 Maximum transient isolation voltage and withstand voltage

Maximum transient isolation voltage and Withstand Voltage, also known as Isolation Voltage, both quantify the ability of an isolator to handle an overvoltage condition for very short periods of time. Overvoltage conditions are caused by unintentional disturbances in the system. The overvoltage can be several times the line voltage and the isolator should be able to handle the overvoltage without damage. [36, 37] It is important to not interpret the withstand voltage as a working voltage [38].

Maximum transient voltage (V_{IOTM}) is defined by standards IEC 60747-5-5 and VDE 0884-10 as the peak transient voltage that the isolator can handle without breaking down. The test is performed during certification by stressing the isolator at V_{IOTM} for 60 seconds, and performing a partial discharge test at 1.6 times maximum repetitive voltage V_{IORM} for 10 seconds. This test is called Method A testing. Other test method called Method B1 is used in the production manufacturing process, where every device is stressed at V_{IOTM} for one second, and a partial discharge test at 1.875 V_{IORM} is performed for one second. The V_{IOTM} can be used to determine compliance to system-level standards. [37]

Withstand voltage (V_{ISO}) is defined in UL 1577 as the RMS value of voltage that the isolator can handle without breakdown for 60 seconds. During certification it is tested by applying a sinusoidal stress of V_{ISO} for one minute. In production, it is tested by stressing every device for 1.2 V_{ISO} for one second. [37]

3.3 Maximum surge isolation voltage

Maximum Surge Isolation Voltage (V_{IOSM}) quantifies the ability of an isolator to withstand a series of short duration high voltage pulses. These surge voltages are caused by direct or indirect lightning strikes, faults and short circuit events. To achieve a reinforced insulation rating an isolator must pass $10kV$ surge voltage testing. A reinforced insulation rating is required when humans are being protected from potentially lethal shock. Standards IEC 60747-5-5 and VDE 0884-10 specify that an isolator claiming to have a certain V_{IOSM} must pass the surge test at peak voltage 1.3 times V_{IOSM} for basic isolation, and 1.6 times V_{IOSM} for reinforced isolation. [36, 37]

The value for surge isolation voltage achieved in the tests is also used to determine compliance to system-level-standards that require a certain level of surge capability

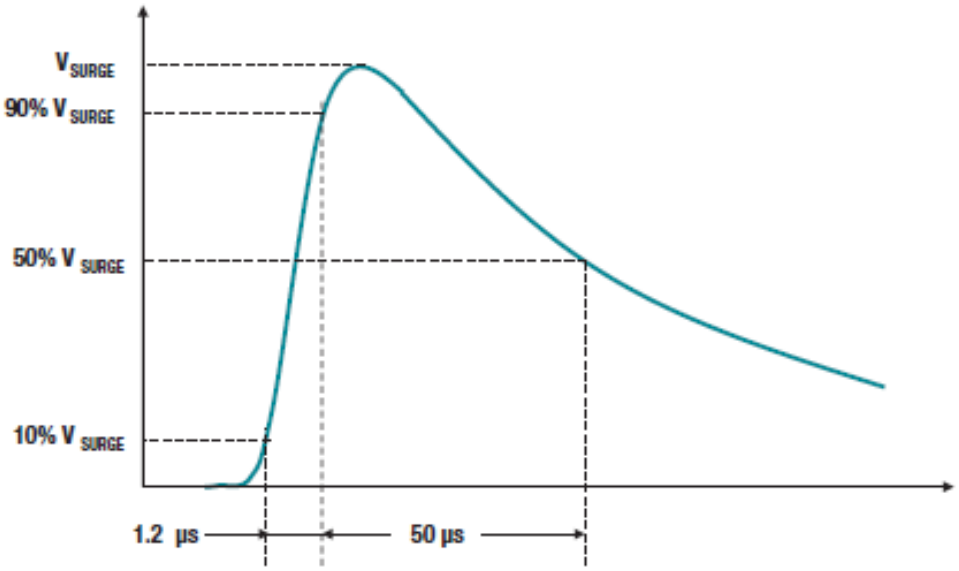

Figure 18: Surge impulse. [37]

for a given system voltage. A widely used standard for reinforced isolation is passing a surge test at levels greater than $10kV$. However, system level standards may allow for lower values of surge capability for systems with lower line voltages. [37]

3.4 Physical and environmental effects

The physical distance across the isolation barrier is determined primarily by the desired voltage rating. But, the characteristics of the environment also have an effect. The isolation distance is described by two dimensions, creepage and clearance, as illustrated in Figure 19. Creepage is the shortest distance along a solid surface across the isolation barrier, and clearance is the shortest line-of-sight path through air across the barrier. [36] The clearance must be high enough to prevent the peak values of impulse voltage and temporary overvoltage from causing the air between the pins to ionize and arc. The breakdown through the air is a fast phenomenon, and the requirements on clearance depends on peak voltages that could occur in the system. [46]

Two of the characteristics, in addition to the desired voltage rating, affecting the required creepage dimension are the mold compound or material used in the package, and the level of contamination in the environment. The mold compound or material of the package is important, because when high voltage is applied across the isolator, electric discharges on or close to the surface of the package can cause localized deterioration in the mold compound or material, resulting in a partially conductive paths across the isolator. This is called tracking, and it is characterized by the Comparative Tracking Index (CTI). Standard IEC 60664-1 classifies materials into four groups according to their CTI values, these groups are shown in Table 2. The CTI for a given material is the voltage that causes tracking with a specific

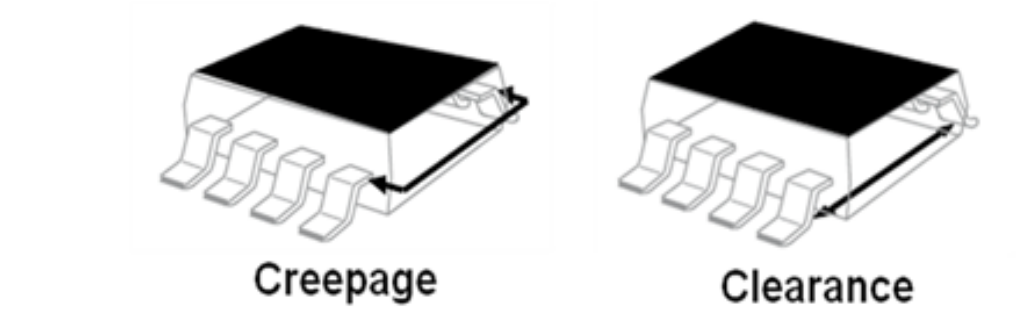

Figure 19: Creepage and clearance. [36]

quantity of an electrolyte on the surface. Higher CTI values indicate that a material has more resistance to tracking, and therefore lower creepage can be allowed. [36, 37]

Table 2: Material groups by CTI classified in standard IEC 60664-1. [37].

Material group I	$600V <$ CTI
Material group II	$400V <$ CTI $< 600V$
Material group IIIa	$175V <$ CTI $< 400V$
Material group IIIb	$100V <$ CTI $< 175V$

The other characteristic affecting the required creepage, the level of contamination in the environment is referred to as Pollution Degree. Environments are classified into four groups based on the amount of dry pollutants and condensation present. [36] The groups are: [10, 38]

1. Nonconductive pollution only, and pollution has no significant impact. Examples of these environments are: air conditioned office environment, and clean labs.

2. Only occasional, temporary conductivity due to condensation. Examples of these environments are: home environments.

3. Frequent conductive pollution due to condensation. Examples of these environments are: industrial warehouses, factory floors, and construction sites.

4. Persistent conductive pollution due to dust, rain or snow. Examples of these environments are: outside atmosphere.

Higher levels of contamination and condensation result in higher creepage and clearance requirements. Standards have tables that are used to determine the required creepage once the voltage ratings, CTI, and pollution degree are known. [36, 46]

3.5 Standard evolution

The emergence of digital isolators has been so rapid that the standards governing them are lacking behind. IEC is working on harmonizing standards, and they are currently working on a capacitive and magnetic isolator specific specification IEC 60747-17. However this standard is currently in draft mode. Meanwhile, the standards IEC 60747-5-5 and VDE 0884-10 are used to certify digital isolators. The standard IEC 60747-5-5 is specified for optocouplers. The VDE standard is for magnetic/capacitive isolators but it is a national standard. [44]

Currently, the most demanding standard for magnetic/capacitive digital isolators is the VDE 0884-10. The latest edition of the standard VDE 0884-10 Ed. 2 released in 2014 added new lifetime and reliability tests on top of the specifications in optocoupler standard IEC 60747-5-5 and earlier edition of the standard. The added reliability tests are based upon the time-dependent dielectric breakdown that is the primary breakdown mechanism for digital isolators and is intrinsic property of all dielectrics. The new edition is important, because current optocoupler standards have no clear definition of lifetime. Also, the working voltage is currently measured using only partial discharge test.

The future of the digital isolator standards is the standard IEC 60747-17 Ed. 1. It will be the first international standard for magnetic and capacitive isolators. It will make digital isolators easier to compare as the devices will be certified according to one standard that is specifically made for the inductive and capacitive digital isolators. The IEC standard is based upon the VDE 0884-10 Ed. 2. The standard IEC 60747-17 Ed. 1 was rejected in 2011, but it was accepted as a new work item proposal again in 2014 and it is currently in draft status. The approval cycle is 3 years, therefore the approval of the standard is possible earliest in 2017.

4 Applicability in variable-frequency drives

Variable-frequency drives are widely used in motor drive systems. Electric motors can be found in many places in industrial applications. They are used in applications such as blowers, compressors, conveyor belts, cooling and recirculating pumps, cranes, factory robotics, fans, elevators, hoists, mixers, paper mills, and printing presses. There are over 300 million industrial electric motors in use worldwide, and the number is growing steadily year after year. [46]

Isolating users and sensitive electronics from hazardous voltages is essential in variable-frequency drives, where high voltages and currents are present [5]. It is enforced by safety regulations [19]. Isolation can be split into two groups. One group is safety isolation that protects users from harmful voltages. And the other is functional isolation, that focuses on protecting the equipment and components. Isolation components are used in many parts of variable-frequency drives, and it is vital to select the components carefully for both safety reasons and to optimize performance, reliability, and cost. [5]

Isolation has its drawbacks. It introduces delays in transferring data across the isolation barrier and adds costs. Therefore, it is important to select correct components to minimize these factors. [5, 19] This section presents how isolation is used in variable-frequency drives, and what are the requirements for the isolation in these applications. The costs of implementing isolation functions with different components are compared to give insight on the cost efficiency of each solution.

4.1 Variable-frequency drives and isolation

Variable-frequency drives, also known as adjustable-speed drives or AC motor drives are smart motor-control systems. Sophisticated power electronics is used in these drives to control the speed, torque and angular position of a motor versus running the motor at a fixed speed and using mechanical elements to control these parameters. Variable-frequency drives are widely used in motor drive applications, and they vastly increase the efficiency and control of motor drive systems. [46]

Electric motor drive systems deliver output power in the range of a few watts to thousands of kilowatts. They operate on AC line voltages in the range of hundreds to thousands of volts. Because, of these high voltages and power involved, the designers must take measures to ensure the safety of humans involved in motor drive system operation. [46]

Variable-frequency drive utilizes usually three phase input power that comes from the grid or mains supply. This input voltage goes to a rectifier stage of power diodes, where the input AC voltage is converted into DC power rails (DC+ and DC-). High-voltage DC link capacitors, in between the rectifier and inverter stages, have two functions. They provide filtering to the rectifier and switching currents to the inverter stage. A three-phase inverter consists of an IGBT module, or a bank of IGBTs. [46]

Galvanic isolation is used in multiple functions in typical variable-frequency drives. An example of a typical variable-frequency drive is presented in Figure 20. Isolated

gate drivers are used to provide the required drive voltage to turn the IGBT on and off. Typically, a gate-emitter voltage of 15V is used to turn the IGBT on, and -8V to turn it off. [46] A dead time is required between the switching signals for the high and low side IGBTs to prevent a short circuit. This dead time is a function of the delays in the turn on/off of the power switches and the uncertainty in the delay introduced by the isolation circuits. An extended dead time introduces further nonlinearity into the power inverter transfer function that will generate unwanted current harmonics and potentially reduce the drive efficiency. Therefore, it is important that the method of sending data across the isolation barrier between the power circuits and control circuitry does not introduce timing uncertainty in the switching and is immune to noise. [8] Galvanic isolation is also used in isolated current and voltage-sense elements that provide current and voltage feedback to the closed-loop control system. Feedback is also provided by an encoder module, it provides feedback about the position and speed of the motor shaft. [46]

The variable-frequency drive provides a three-phase output that is connected to the electric motor. The electric motor is controlled by changing the amplitude and frequency of the three-phase output from the drive. The voltage and current waveforms at the motor drive output are provided using a control module that contains a microprocessor or field-programmable gate array (FPGA). The control module provides the right sequence of pulse-width modulated (PWM) controls to the IGBT gate drivers at the right frequency to generate the desired output. The output waveforms control the speed and torque output from the electric motor. The variable-frequency drive is a closed-loop system, and the control module receives feedback from the voltage and current-sense circuits, as well as possible feedback from the encoder about the angular position and speed of the motor. The control module has an interface connecting it with the rest of the control network, such as human-machine interface. The interface uses standard communication interfaces such as RS-485, CAN or Industrial Ethernet. [46]

Parts of the control module are accessible to human. Accessible parts include, for example, the connectors of the communication interface and the input port of the encoder interface. To protect the users, sufficient safety isolation is required between the exposed parts and the high-voltage circuit. High-voltage circuits are the circuitry connected to the DC buses and the incoming supply lines. The required isolation can be achieved through isolated gate drivers and isolated voltage and current-sense amplifiers. Additional isolation can be added between the control module and communication interface. [46]

An alternative isolation scheme is presented in Figure 21. In this scheme, the control module is not earth-referenced, but it is biased to the DC bus. Additional digital isolation is used to provide safety isolation between this control module that is connected to high-voltage and a second control or communications module that is earth-referenced. The parts or interfaces accessible to humans are behind the second control module. This architecture requires isolation for both the gate drivers and the isolated current and voltage-sense module for functional purposes. The isolation allows the control module that is connected to the DC- to communicate with the IGBTs and sense elements. [46]

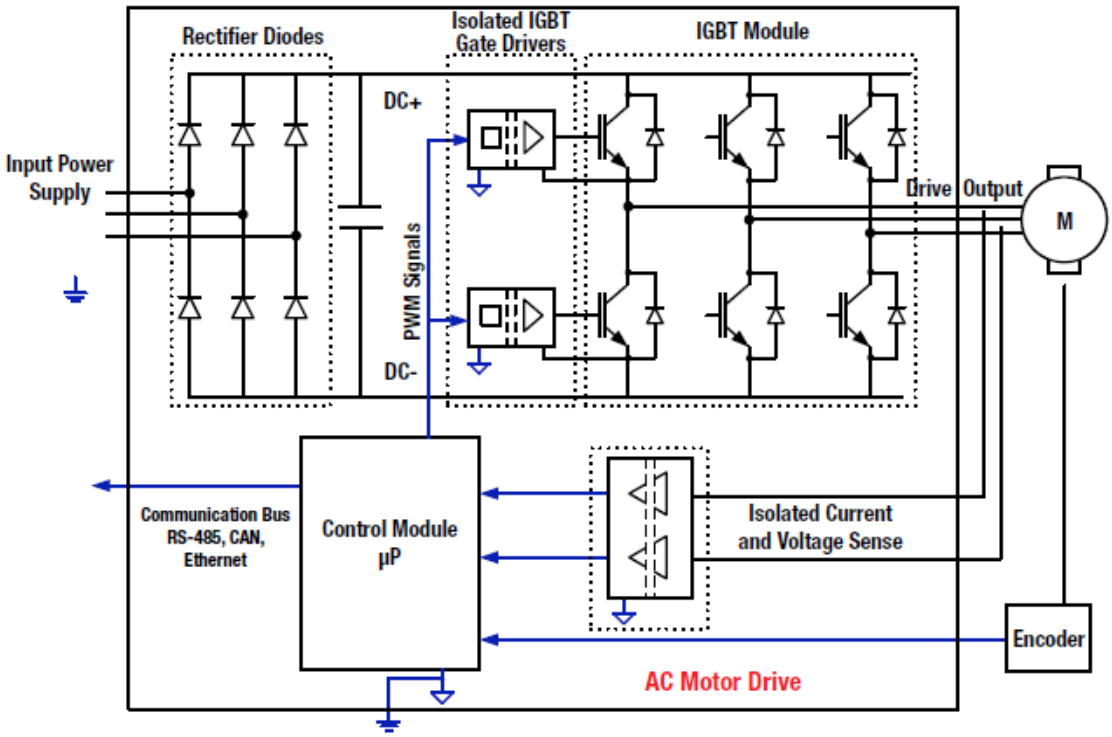

Figure 20: A simplified block diagram of typical AC motor drive. [46]

4.2 Isolation requirements

The system level safety standard for variable-frequency drives is IEC 61800-5-1 [37]. It covers electrical, thermal and energy safety. As part of the electrical safety, the standard defines the requirements for ensuring adequate insulation between circuits connected to voltages higher than $50V$ and any drive system parts or connectors that may be accessible to humans. [46]

Systems and end equipment standards mandate certain minimum values for the isolator's isolation parameters depending on the system line voltage, and based on whether basic or reinforced isolation is required [37]. The system line voltage is the RMS voltage between a phase of the input or grip supply and earth [46].

IEC 61800-5-1 classifies equipment into four categories based on how it is connected to the supply mains. The categories are: [46]

- Category I: Applies to equipment connected to a circuit where measures are taken to reduce surges and transient overvoltage.
- Category II: Applies to portable tools and plug-connected equipment not permanently connected to the mains.
- Category III: Applies to equipment connected permanently to supply mains downstream of the distribution board.

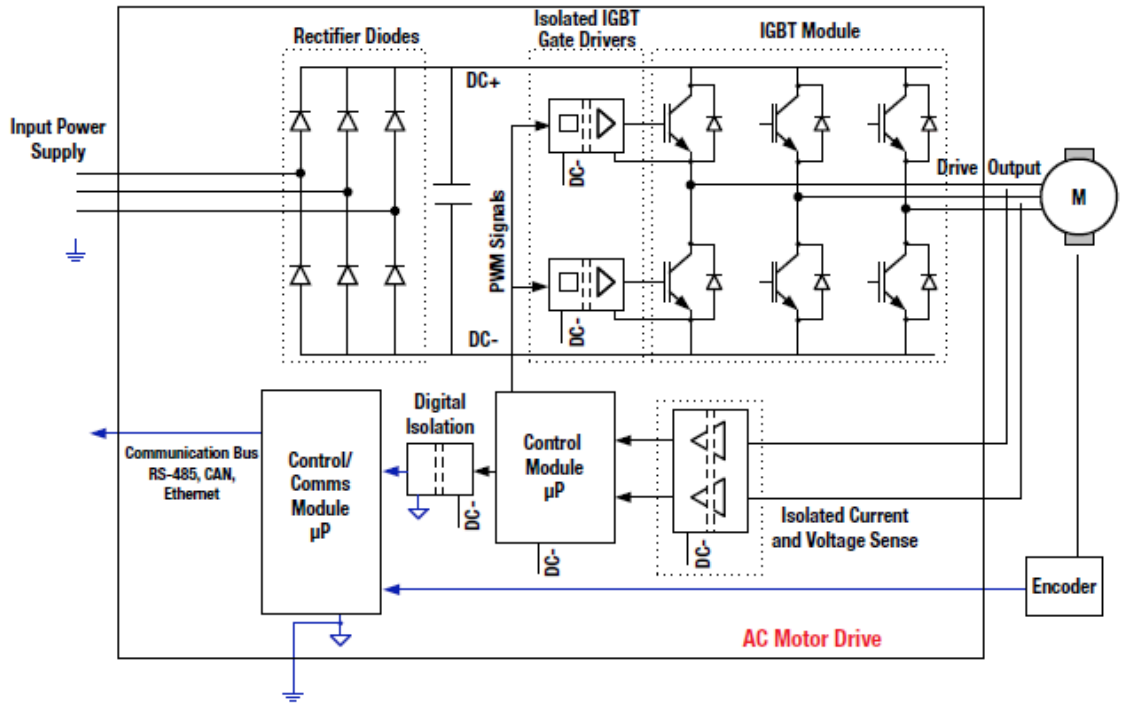

Figure 21: A simplified block diagram of typical AC motor drive with alternative isolation scheme. [46]

– Category IV: Applies to equipment permanently connected at the origin of the installation upstream of the main distribution board.

Equipment in a higher category is more likely to be subjected under higher voltage disturbances. Therefore, higher requirement on temporary overvoltage and impulse or surge voltage is needed. Most industrial motor drives belong to Category III. [46]

Sufficient safety isolation, alias protective separation in IEC 61800-5-1, is required between circuitry connected to high voltage and any parts or connectors accessible to humans. This protective isolation can be achieved by having two basic isolators in series, also known as double isolation, or by using one reinforced isolator. The motor drive in Figure 20 needs to have reinforced insulation in both the isolated gate drivers and isolated voltage and current-feedback circuits. If additional basic isolators are added in the path of signals that are connected to external interfaces or connectors, basis isolation is sufficient. In the motor drive shown in Figure 21, the digital isolator between the control modules needs to be a reinforced isolator. In this isolation scheme, the isolated gate drivers and isolated feedback circuits are DC bus-referenced and have high voltage on both sides of the isolation, and they do not need to have a protective isolation. For these, the isolation is functional. [46]

The requirement for temporary overvoltage and impulse or surge voltage for each isolator is determined by the system voltage using a table from IEC 61800-5-1. Interpolation is not allowed, and the next higher system voltage is used. The table in the standard lists the requirement for basic isolation. For reinforced isolation, the

value of temporary overvoltage requirement is doubled. And, for surge voltage, the next-higher impulse voltage is used. Also, to determine the required clearances for reinforced isolation, a temporary overvoltage of 1.6 times the basic requirement and the next-higher impulse voltage are used. [46]

The required clearances for the isolators are determined using a table from IEC 61800-5-1. The table lists required clearances for a given temporary overvoltage and surge or impulse voltage. The table shows values for altitudes of up to 2000m. Higher altitudes require increase in the clearance by a certain factor to account for the fact that air breaks down more easily at higher altitudes. This correction factor for higher altitudes is defined in a table in IEC 61800-5-1. [46]

The required creepage is determined using a table from IEC 61800-5-1. The creepage is determined based upon the RMS value of the working voltage. The table lists the required creepage for basic isolation, the creepage requirement is doubled for reinforced isolation. Also, the pollution degree and CTI of the isolator affect the required creepage, and their effect reflected in the table. [46]

The required creepage and clearance can be reduced by conformal coating or potting. They are used to reduce the pollution degree under the coating, and to block the path for arcing between pins. However, these methods add costs, need additional inspection steps to check the quality of the coating, and have limitations on the maximum voltage levels supported. Usually, choosing an isolator with a higher CTI and higher values of creepage and clearance is the cheaper and more reliable option. In a case where the required creepage is lower than the clearance requirements, creepage needs to be increased to meet the clearance. This is required because the creepage path along the package surface is also a path along which air breakdown can occur. [46]

The isolator must be able to sustain both peak and RMS values of the working voltage it is suspected to throughout the equipment's lifetime. Generally, isolators with working voltage matching the input phase to phase voltage covers most cases. But, the requirement is dependent upon the architecture of the drive. Despite, adding a margin provides a buffer that increases design robustness and reliability, but also cost. [46]

4.3 EMC requirements

EMC defines the ability of an equipment or a system to function satisfactorily in its electromagnetic environment without introducing intolerable electromagnetic disturbances to anything in that environment. Therefore, EMC can be divided into two subdivisions presented in Figure 22. [47] Electromagnetic emission of disturbances into the electromagnetic environment must be maintained below a level that would cause an unacceptable degradation of the performance of equipment operating in that environment. Also, all equipment operating in the electromagnetic environment must have sufficient immunity from all disturbances at the levels at which they exist in the environment. The needed limits to achieve EMC for emission and immunity cannot be set independently of each other. If emissions are controlled effectively, less restrictive immunity demands have to be placed on equipment. And,

similarly, if equipment is highly immune, there is less need for stringent limits on the emission of disturbances. The compatibility levels set in the EMC standards co-ordinate the limits adopted for emission and immunity. [48]

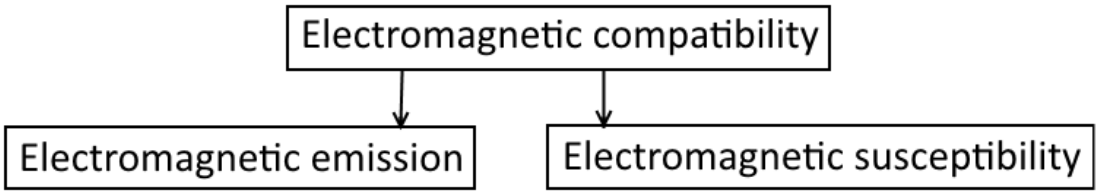

Figure 22: Subdivision of EMC. [47]

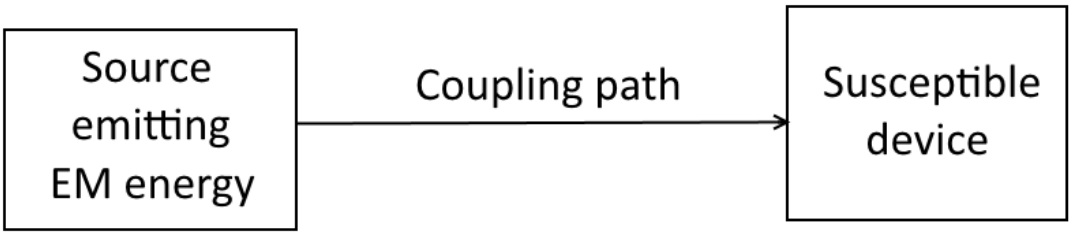

Figure 23: EMI couples from the source to the device through a coupling path. [47]

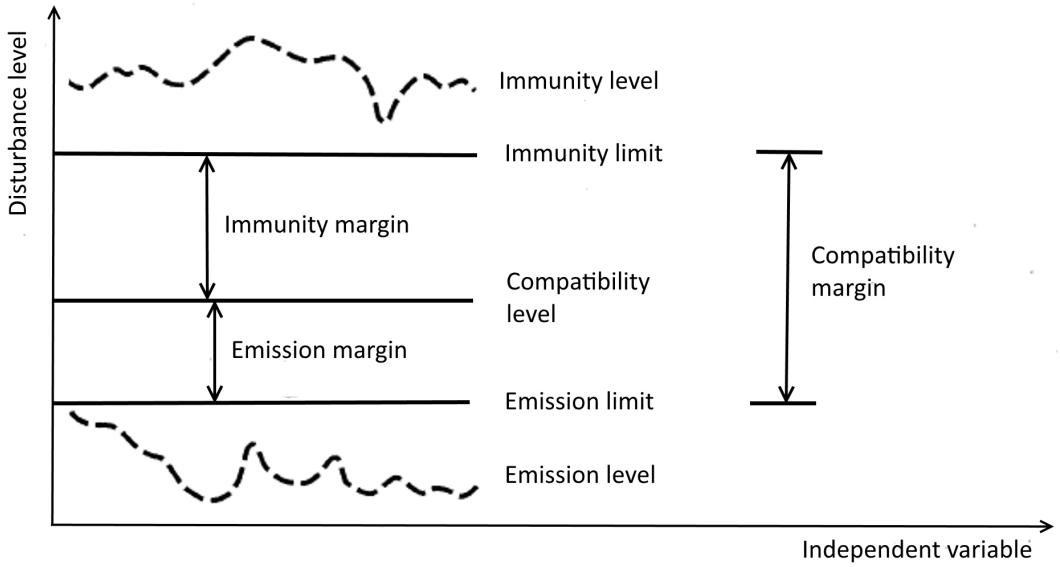

Figure 24: Emission/immunity limits and compatibility level. [47]

EMC requirements for power drive systems are defined in IEC 61800-3. The standard is an EMC product standard, and it takes precedence over all aspects of

the generic standards and no additional EMC tests are required or necessary. The generic EMC standard is IEC 61000 and it is used as an indispensable reference in the IEC 61800-3 product standard. For example, the test methods for different EMC phenomena have been defined in the IEC 61000-4. However, if modifications or additional requirements and information or specific test methods are needed for practical implementation and application of the tests, then they are given in the product level standard IEC 61800-3. The limits provided in the standard are given for conditions which do not consider the cumulative effects of different phenomena. [49]

Immunity requirements are given according to the environment classification. Immunity and emissions requirements are divided into two groups: low-frequency and high-frequency. Low-frequency emission requirements are given according to the nature of the supply network. High-frequency emission requirements are given according to four categories of intended use, which cover both environment and bringing into operation. [49] The environments and four categories of intended use are presented below. [49]

First environment

First environment includes domestic premises, it also includes establishments directly connected without intermediate transformers to a low-voltage power supply network which supplies buildings used for domestic purposes. Examples of first environment include: apartments, commercial premises, houses or offices in a residential building.

Second environment

Second environment includes all establishments other than those directly connected to a low-voltage power supply network which supplies buildings used for domestic purposes. Examples of second environment include: industrial areas and technical areas of any building fed from a dedicated transformer.

PDS category C1

PDS of rated voltage less than $1000V$, intended for use in the first environment.

PDS category C2

PDS of rated voltage less than $1000V$, which is neither a plug in device nor a movable device and, when used in the first environment, is intended to be installed and commissioned only by a professional.

PDS category C3

PDS of rated voltage less than $1000V$, intended for use in the second environment and not intended for the use in first environment.

PDS category C4

PDS of rated voltage equal to or above $1000V$, or rated current equal to or above $400A$, or intended for use in complex systems in the second environment.

In addition, the standard IEC 61800-3 classifies the effects of a given disturbance into three performance criteria: A, B and C. A-class criteria requires that no noticeable changes occur in the operating characteristics. For B-class criteria, noticeable changes in the operating changes can occur, but they must be self-recoverable. And for C-class criteria, changes in operating characteristics occur, that are not self-recoverable and a system shutdown is required. Also, possible triggering of protective devices results in a C-class criterion. The compliance for the low-frequency disturbance immunity requirements may be demonstrated using either testing or simulation. High-frequency disturbance immunity is verified by performing a type-test on a representative unit. The manufacturer or supplier ensures the EMC performance of the product is maintained in production by using quality control methods. Minimum immunity requirements are detailed in the standard. Table 3 presents minimum high-frequency disturbance immunity requirements for the use in the second environment. The table contains reference to the test method standard, and test result level and performance criterion requirements. [49]

The measurements for the emissions shall be made in the operating mode producing the largest emission in the frequency band, while being consistent with the normal application. The compliance for the low-frequency emission limits can be verified by simulation or test. It is sufficient to perform the conformance tests on one appliance only. Conformance of the PDS of categories C1, C2 and C3 shall be verified by performing a type test on a representative model. The manufacturer or supplier ensures that the EMC performance of the product is maintained by employing a quality system. Some of the emission limits might not be possible to achieve in some applications for PDSs of category C4. These applications are for large ratings or to meet specific technical requirements. In these applications of category C4 equipment, the user and the manufacturer shall agree on an EMC plan to meet the EMC requirements of the intended application. In this situation, the user defines the EMC characteristics of the environment including the whole installation and the neighborhood. The manufacturer provides information on typical emission levels of the PDS which is to be installed. [49]

4.4 Cost

A determining factor in choosing a component for isolation is the price of implementing the desired function. In this section, a cost comparison is presented for a few selected isolation functions. The comparison for particular function is between digital isolator implementation and a comparison technology implementation, such as optocoupler. The results are presented as a ratio of digital isolator implementation cost to the comparison technology implementation cost. In addition, a brief cost analysis about the possibility to use higher channel count digital isolators than necessary in some designs to boost the overall volumes is made. Also, a possibility to use one extra-wide

body digital isolator instead of two wide-body digital isolators is discussed.

The function cost comparison results are presented in Table 4. Digital isolators can be a very cost effective method to implement an isolation function if the volumes of digital isolators are high enough. Currently, the required volume for digital isolators to be competitive to optocouplers is high, near the mass production volumes. And they can be cheaper than optocouplers if the volumes are at a mass production level, which is the level used for calculating the optocoupler impelentation price. In other words, if digital isolator volumes were as high as current optocoupler volumes they would be cheaper. This produces an incentive to start using digital isolators as the default device to fulfill the isolation needs, providing higher volumes for them, and possibly reaching the critical volume where digital isolators would become a cheaper alternative.

The amount of components and PCB area required for the fieldbus serial communication function are significantly less in the digital isolator implementation than the optocoupler equivalent. The amount of components and PCB area required decreases almost 50% in the digital isolator implementation versus the optocoupler implementation. However, the indirect costs from increased component count and PCB area are approximately 10 to 20% of the functions total costs. And, the direct component costs are the main driver in the total function costs for the fieldbus serial communication function. The price of optocouplers is highly dependent on the speed. Optocouplers used in the optocoupler implementation are two ACPL-W454-560E and one TLP785F. The price of TLP785F in Digikey for orders above 3000 units is 0.12 USD, and the price for ACPL-W454-560E is 1.45. The ACPL-W454-560E has a turn on/turn off time of 200ns, and the TLP785F has a turn on/turn off time of 3000ns. The speed can limit the serial communication protocol used, and therefore faster and more expensive optocouplers might have to be used depending on the required speed. The required speed is the determinant factor in choosing if CMOS digital isolator or optocoupler is more cost effective.

In IGBT gate-drive isolation function, the amount of components and the required PCB area is similar between optocoupler and digital isolator implementations. The indirect costs are approximately 10 to 20% of the total function costs. Therefore, the cost difference is a result from the difference of direct component costs. The IGBT gate-drive function uses three optocouplers with similar characteristics and price to the optocoupler ACPL-W454-560E that is used in the fieldbus serial communication function.

In the PSL2-link, the amount of components decreases over 80% in the digital isolator implementation versus the transformer implementation. However, the change in required PCB area is not significant, because most of the components in the transformer implementation are chip resistors in a small 0402 package. Indirect assembly costs are approximately 20% of the total function costs for the transformer implementation, but only 5% for the digital isolator implementation. The indirect cost from PCB area is less than 5% of total function costs for both implementations. The direct component costs are the main driver for the total function cost.

The effect of volume to unit price can be divided in two volume categories: volume by individual customers and volume of the market. The general effects of increasing

volumes is that the unit price is decreasing to match the variable costs at which it remains constant. The decreasing unit costs are a result of being able to divide fixed costs to more units. This effect is driven by both increasing market volume and by increasing demand by individual customers. For example, increasing market volume results in NRE costs to be divided across more units, and increasing volume by individual customers results in delivery costs to be spread across more units. Figure 25 presents the unit price vs. the volume of individual companies. The shift presented in the Figure 25 is a result from increased market volume. After increased market volume, individual companies are able to benefit from lower prices without having to increase their own volumes. The effects of decreasing volume are opposite, and if digital isolators begin to take market share from optocouplers, the unit price of optocouplers could increase. However, a rapid decrease in optocoupler volumes is not expected in the next few years, and estimating further is not but an educated guess in a field developing so rapidly. Because, both digital isolators and optocouplers are manufactured using mature processes (CMOS and GaAs), the decrease in costs driven by development of manufacturing technologies is not likely to be a determinant factor in the price development of digital isolators or optocouplers. A forecast on the development of the market is in Section 2.2.5.

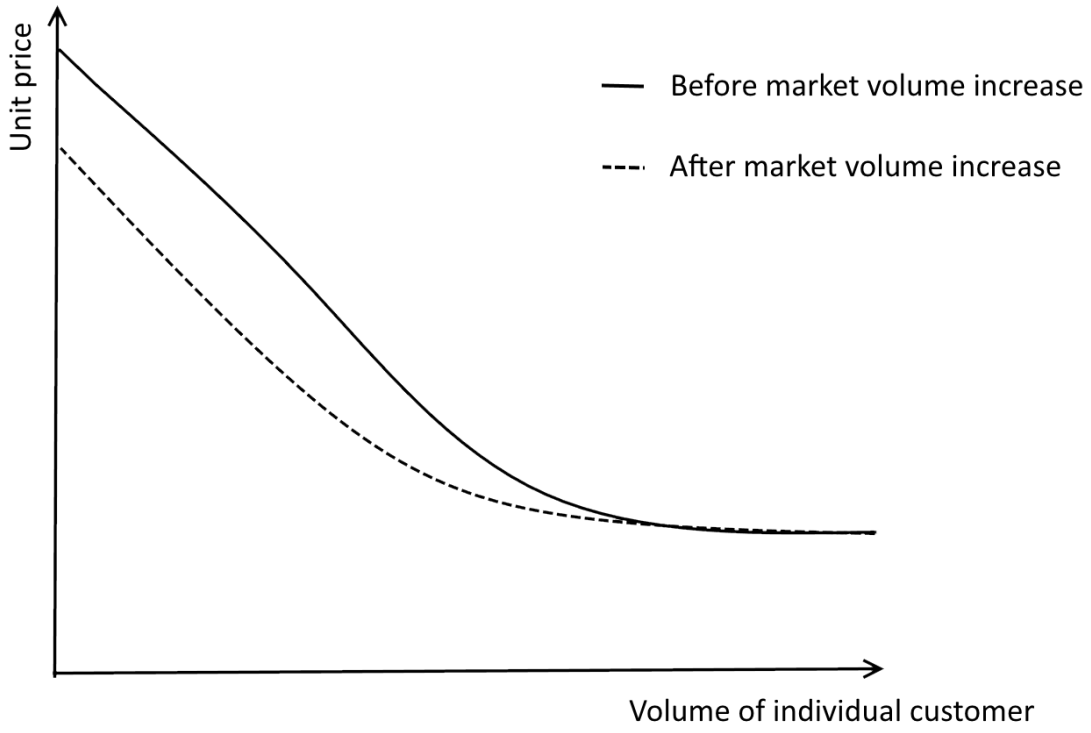

Figure 25: Unit price vs. volume of individual customers.

It is possible to use a digital isolator with more channels than is needed in the design to increase the overall volumes for the isolator to gain improvement in volume pricing. However, there is an additional cost for the extra channel. The decision is made with a goal to minimize the total cost. This depends on the cost of the

extra channel, and how much the increased volume can decrease the unit price. With current pricing, it is possible that the total cost can be decreased by increasing the volumes by employing digital isolators with extra channel in some designs. However, having more than one idle channel is not beneficial at any point because the cost of two or more extra channels is higher than what can be saved with increased volume pricing. Other than that there is no simple rule for the designer to make the best decision, and in order to accomplish the best result collaboration between designers and sourcing is needed. Another factor with being able to have multiple channels integrated easily within single device is that the price of a digital isolator is a base price plus a cost per channel. And, if a design can use a single device with more channels the base price is divided between more channels and a cost benefit can be obtained.

There are designs where two digital isolators in wide-body SOIC-16 package are used in series. Sometimes they could be replaced with one digital isolator in extra-wide body SOIC-16 package. This could potentially provide cost savings. However, at current pricing this is not the case. With a potential for cost saving and constantly changing prices, this option should be reviewed occasionally.

Table 3: Minimum high-frequency immunity requirements for second environment in IEC 61800-3.

Port	Phenomenon	Test method	Level	Acceptance criterion
Enclosure port	ESD	IEC 61000-4-2	4kV CD	B
	Radio-frequency electromagnetic field, amplitude modulated	IEC 61000-4-3 see also 5.3.4	80MHz to 1000MHz 10V/m 80% AM (1kHz)	A
Power ports	Fast transient-burst	IEC 61000-4-4	2kV/5kHz	B
	Surge 1.2/50µs, 8/20µs	IEC 61000-4-5	2kV	B
	Conducted radio-frequency common mode	IEC 6100-4-6 see also 5.3.4	0.15MHz to 80MHz 10V 80% AM (1kHz)	A
Power interfaces	Fast transient-burst	IEC 61000-4-4	2kV/5kHz Capacitive clamp	B
Signal interfaces	Fast transient-burst	IEC 61000-4-4	1kV/5kHz Capacitive clamp	B
	Conducted radio-frequency common mode	IEC 61000-4-6 see also 5.3.4	0.15MHz to 80MHz 10V 80% AM (1kHz)	A
Ports for process measurement control lines	Fast transient-burst	IEC 61000-4-4	2kV/5kHz Capacitive clamp	B
	Surge 1.2/50µs, 8/20µs	IEC 61000-4-5	1kV	B
	Conducted radio-frequency common mode	IEC 61000-4-6 see aösp 5.3.4	0.15MHz to 80MHz 10V 80% AM (1kHz)	A

CD: contact discharge, AM: amplitude modulation

Table 4: Cost comparison of digi isolator implementation vs. comparison technology implementation.

Function	Ch. conf.	Comparison technology	Cost ratio			
			Low volume	Moderate volume	High volume	Mass volume
Fieldbus serial com.	2 + 1	Opto	1.25	1.13	1.04	0.83
IGBT gate-drive	1 + 1 & 1 + 0	Opto	1.32	1.22	1.12	0.89
PSL2-link	1 + 1	Transformer	0.80	0.73	0.67	0.52

- Cost ratio is the ratio of digital isolator impelentation cost to the comparison technology implementation cost.
- The volumes in the table are digital isolator implementation volumes. Comparison technology implementation costs are fixed, and calculated only with one volume. The opto implementation costs are mass volume prices, and the transformer volume is unknown.
- Costs include direct component cost, and indirect costs from PCB area and assembly.

5 Measurements

Digital isolators play a major role in variable-frequency drives in ensuring continued, reliable performance of the systems. The systems are susceptible to extremely harsh conditions, and have to be able to withstand stresses like lightning strikes, high electrostatic discharges, and electromagnetically coupled, high-energy transients from neighboring high-power systems [41]. Electromagnetic interference (EMI) is defined as any electromagnetic disturbance that interrupts, obstructs or otherwise degrades or limits the effective performance of the system. Sources of EMI are plentiful in industrial environment, and they have different disturbance characteristics. A subset of different EMI categories is presented in Table 5. Traditional ways to minimize the effects of EMI to the system include proper PCB layout and grounding and limited trace lengths. [50]

Table 5: Subset of EMI categories. [50].

EMI Type	Description	Example Sources
Radiated	Radio frequency (RF) energy transmitted through air that penetrates the system, inducing noise.	Electric motors, handheld communication devices, power line spikes, improper PCB layout.
Conducted	RF energy that travels along a conductive path, coupling into a system.	Noise on power supply, power line or other system cabling noise.
Electrically Fast Transients	Fast perturbations, mostly associated with AC power lines, that couple into a system.	Transformer-less power supplies, local lightning strike, power line surges.
Electrostatic Discharge (ESD)	Static electricity accumulated on a conductive surface that abruptly discharges to ground, generating EMI and possibly damaging circuitry.	Human touch without proper ESD protection, improper system grounding.

Because industrial equipment is subjected under harsh environments that are electrically noisy, assessing the performance of the digital isolators during such stresses is critical in choosing the right isolator for the application. The standards were used as a baseline for the EMC tests, but some alterations may have been made to make the tests correspond better to the environment where the variable-frequency drives are used. This section demonstrates the test PCB, test equipment, and test methods. The tests can be repeated with the help of this section.

Test equipment:

- Oscilloscope Tektronix DPO4034B
- Signal Generator Aim and Thurlby Thandar Instruments TG1000
- ESD-simulator Schaffner NSG438
- Aim and Thurlby Thandar Instruments EX354RT
- EMC-simulator Teseq NSG 3040
- Forward voltage measuring instrument Schuster elektronik DM 659
- RF-chamber LaplaCell 300/2 Model B02
- Laplace Instruments RF 2000 Synthesiser
- Laplace Instruments RF 1100 RF Power Amplifier
- Laplace Instruments EMC Test Integration System RF-switch
- Soken Partial Discharge Tester DAC-PD-7

5.1 Measurement PCB

Performance of the isolators in the EMC tests can be enhanced artificially, by using costly or impractical board level implementations. Some of these methods are: [41]

- Adding large and expensive high-voltage capacitors across the isolation barrier.
- Complex PCB plane design intended to increase capacitance between both sides of the isolation barrier.
- Using different custom PCBs, each optimized for one of the tests.

Such methods should not be employed when evaluating the performance of a digital isolator. However, they can be utilized in the final system design. The reason is that, the methods mentioned, either block or divert the actual stress from reaching the isolators. These methods are designed to protect the isolator from the stresses, and the true performance of the isolator is not shown. Therefore, EMC results might look good, but the inherent weakness of the isolator is masked. [41]

A good EMC test PCB has following qualities: [41]

- Employ simple PCB design practices that are already in common use.
- Have basic components and blocks seen in most common digital isolator systems.
- Not be architected to make a device pass a standard test, but to identify its inherent capability.

– Not be changed from one test to another unless the standard requires it.

Saana Lindvall used a 2-layer PCB for making similar EMC tests in her master's thesis. Her PCB also had buffered channel for making some operational tests for the digital isolators. Saana chose a 2-layer PCB for lower costs. [42] The PCBs in variable-frequency drives are 4- or 6-layer PCBs. Digital isolators are commonly used in control boards, and generally these PCBs have 6-layers. For this reason, a new test PCB was designed that has 6-layers. PCB with 4- or 6-layers can achieve better EMC characteristics than 2-layer design. Another reason for designing new test PCB was that the buffered channel was not needed. And to mitigate its possible effects on the PCB's EMC characteristics, this buffered channel was not added in the new PCB.

The test PCB measurements are 112mm x 65.5mm. It is presented in Figures 26 and 27. The schematic and layout of the test PCB can be found in the Appendixes A and B.

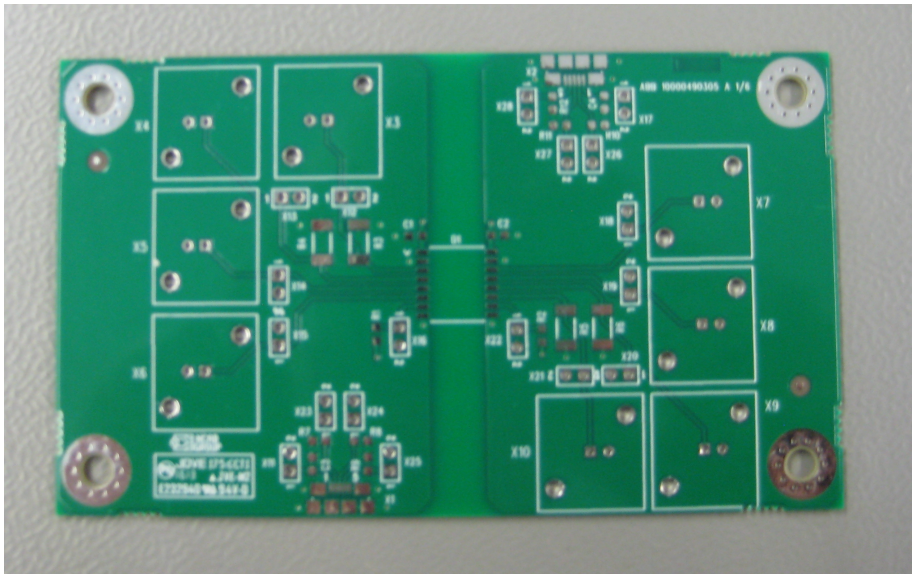

Figure 26: The test PCB.

5.2 ESD immunity test - indirect ESD

The test was performed using an ESD-simulator that complies to the standard IEC 61000-4-2. The ESD charge can subject the digital isolator to very high common-mode surges through radiation. The purpose of this test is to learn about the digital isolators ability to withstand common-mode EMI caused by ESD.

The test setup can be seen in Figures 28 and 29. A polycarbonate sheet with thickness of $1.5mm$ was placed beneath the metal sheet. These sheet were placed on top of a cardboard. The metal sheet was grounded to the metallic table forming the reference ground with a series of resistors totaling approximately $1M\Omega$. The ESD charge was injected in the metal sheet. The metal sheet's distance from the test

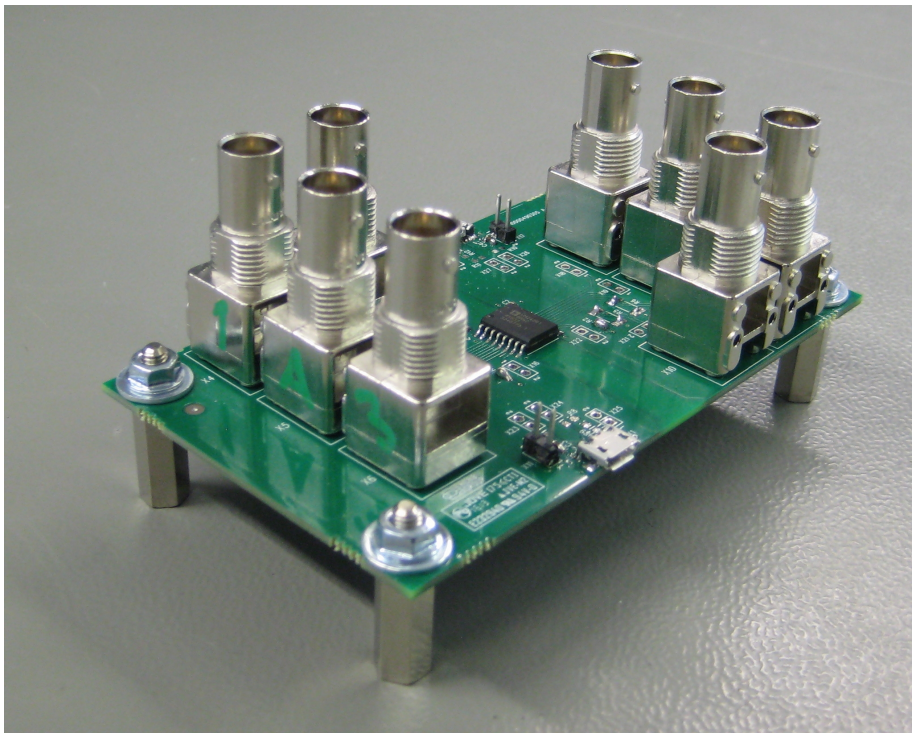

Figure 27: Assembled test PCB.

PCB was approximately $12cm$. The test PCB distance from the ground level was approximately $9cm$. Also, both sides of the PCB were grounded to the metallic test table forming the reference ground.

ESD charge was injected to the metal sheet 50 times at a frequency of $0.5Hz$. The test was repeated at different voltages until a level where no error occurred was found. An error is a condition where the output signal is different from the input signal in a way that the outputs logical level could be sampled incorrectly. Error conditions include locking of the signal, inverting of the signal, and spikes in the signal. The tests were made with both polarities. Also, the test was repeated without the input signal. During the test, the output signal was monitored, and the ratio of errors to ESD injections was recorded for each test voltage.

The output signal was monitored with an oscilloscope. The trigger level was set just above the signal level to get the signal on oscilloscope's display when the ESD shock was injected. The output waveform was a bit different between digital isolators, and some had noticeable ringing due to the mismatches. Ringing due to the mismatches was a result of the fact that the signal was looped through all channels of the digital isolator. The problem of ringing is mitigated significantly in real applications where the signal is not looped through multiple channels. Some digital isolators employed a schottky diode at the input, cutting the spikes resulting from the ringing. However, the signal was distorted for all of the digital isolators due to the mismatching. Because of ringing the oscilloscope triggering level had to be set above the normal signal level, and if the ESD impulse did not cause the voltage to raise at this point, the oscilloscope might have not triggered. When the trigger was

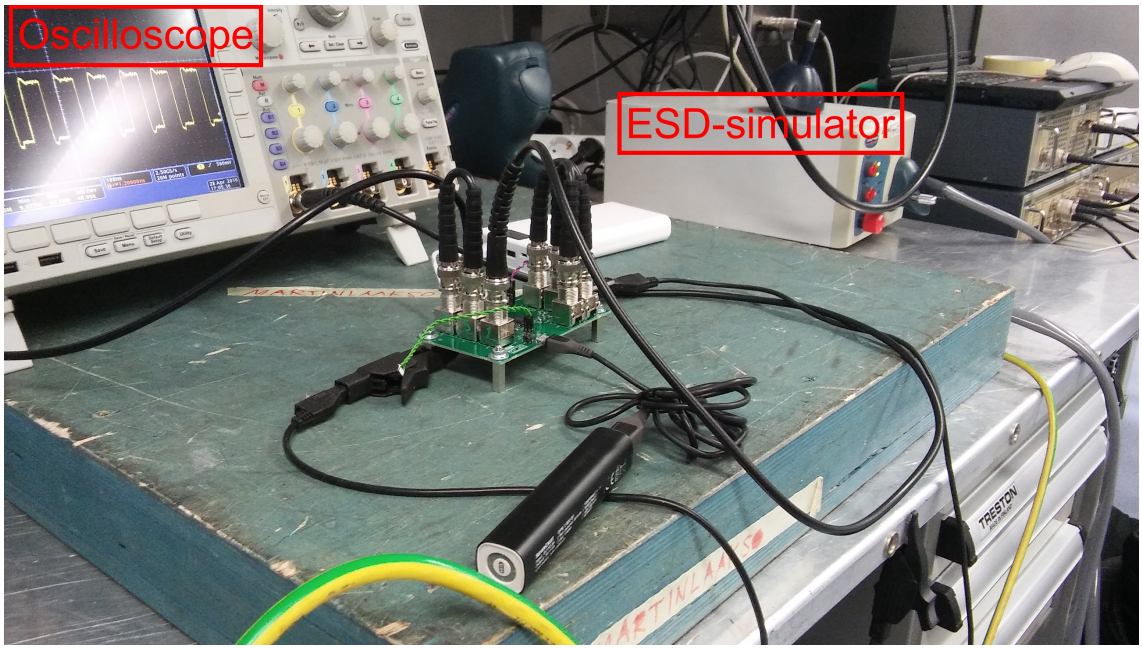

Figure 28: The setup for indirect ESD test beneath the cardboard.

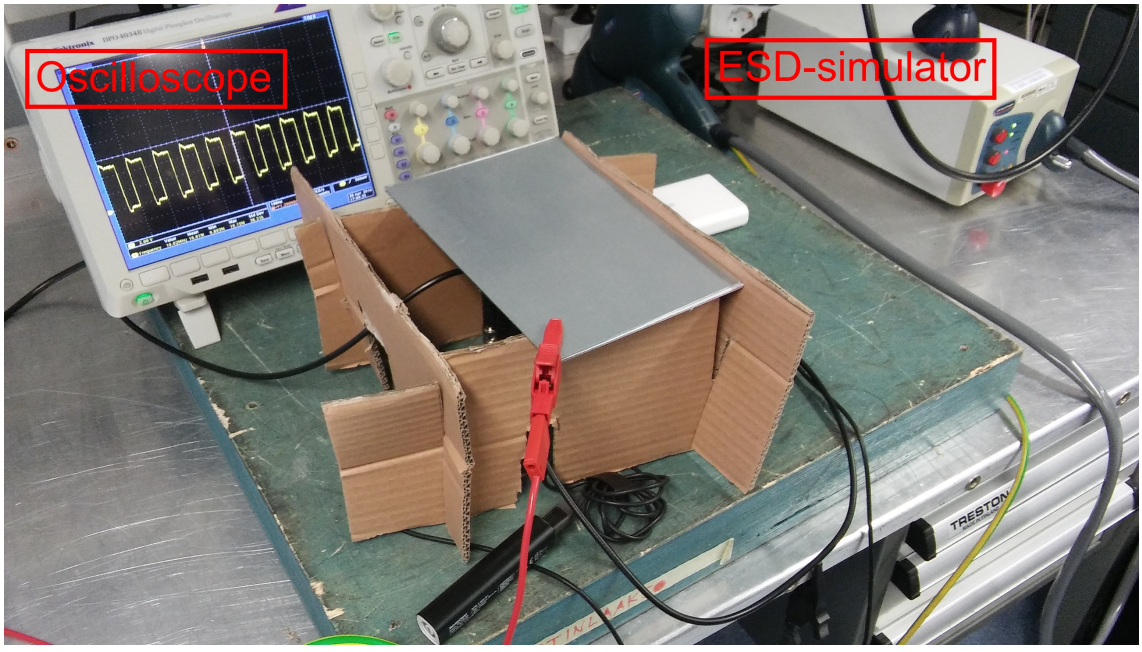

Figure 29: The setup for indirect ESD test with the cardboard.

dropped by a bit some errors were observed at a ESD injection levels that had not been triggered before. Therefore, the trigger level and different waveforms between digital isolators provide quite a remarkable source of uncertainty. In addition, if the trigger level is too close the oscilloscope might trigger multiple times in a row and some errors might not be observed. For these reasons, the results with the 20Mbps input signal are only indicative with an error margin of approximately $3kV$. However,

this problem with mismatching, ringing and trigger level does not exist when the input signal is low at a data rate of 0Mbps. Therefore, the results with 0Mbps data rate provide the most reliable comparison between the manufacturers. However, it was perceived by adjusting the trigger level of the oscilloscope that the input signal rate did not have an effect to the withstand capabilities of the digital isolators, and therefore, the results with datarate of 0Mbsp provide correct view also in situations where data in being transmitted through the device.

The ESD withstand levels with data rates 20Mbps and 0Mbps are presented in Tables 6 and 7. The digital isolators from given manufacturer were from the same batch. Nevertheless, the ESD withstand had variance between the units of the same type. The differences in ESD withstand for given type were limited to approximately $1kV$. The differences between batches could further increase the spread between the highest and the lowest withstand levels. The polarity of an ESD injection did have some effect. The withstand voltage could differ for $1kV$ depending on the polarity. However, whether the withstand was better with positive or negative polarity changed from unit to unit. Therefore, the effect of ESD polarization is limited. The withstand level for the both polarizations were positively correlated.

Digital isolators from different manufacturers had different characteristics in the way how their output behaved to the ESD injections. Digital isolators from Maxim had their output locked to high and low, and also sharp spikes occurred. The ringing resulting from mismatching was noticeable especially on Maxim. The ringing, spike and a lockout with a signal rate of 20Mbps are illustrated in Figure 30. Digital isolators from Maxim locked to high when ESD was injected at a ESD injection level of $\pm 2kV$. Most of the time, the output was locked to high beyond the time axis of the oscilloscope, and in few cases for approximately $200ns$. The locout condition with input signal rate of $0Mbps$ and input signal low is presented in Figure 31.

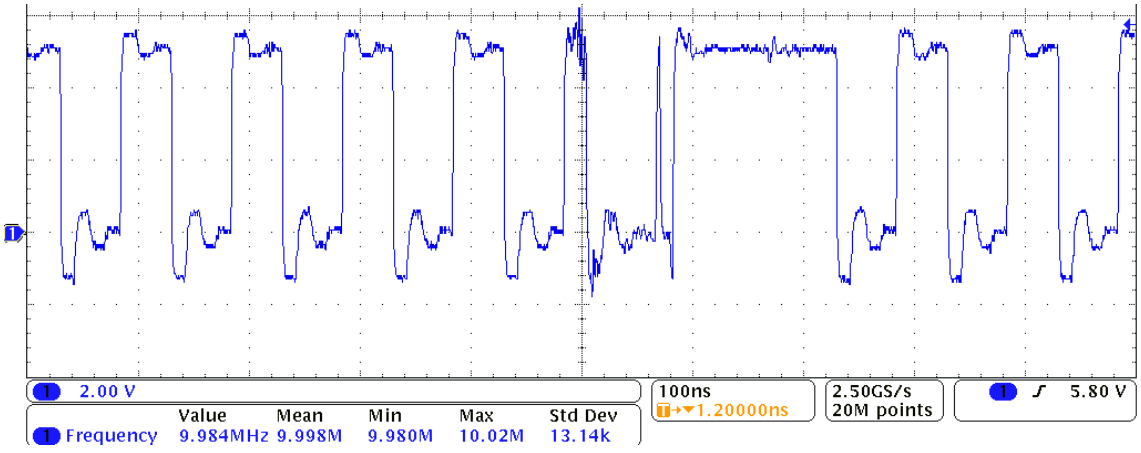

Figure 30: Typical error condition for Maxim at a data rate of $20Mbps$.

Typical error condition for digital isolators from Texas Instruments with a data rate of $20Mbps$ was locking to high. Some sharp drops occurred as well. These are presented in Figure 32. Notice the difference in the waveform between Texas Instruments and Maxim. The ringing noticeable in Maxim made it hard to set the

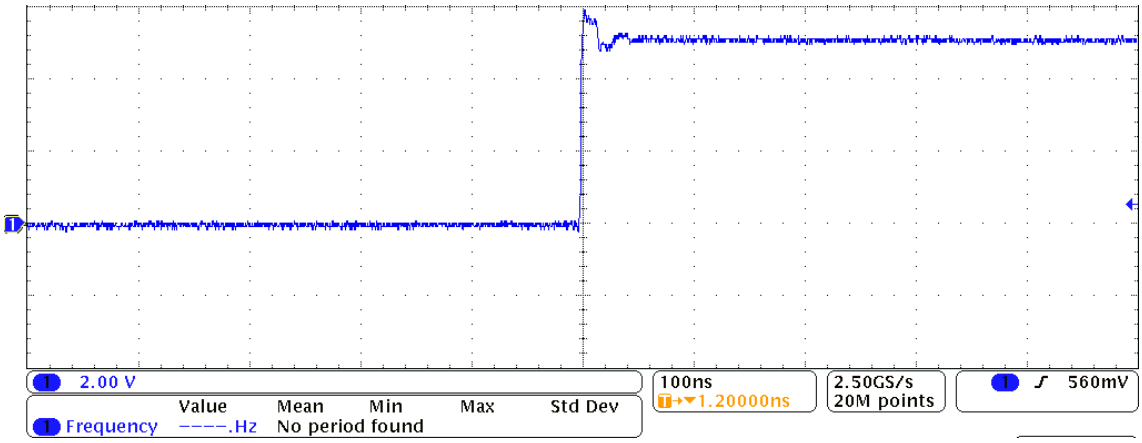

Figure 31: Typical error condition for Maxim at a data rate of $0Mbps$, input low.

trigger level for an oscilloscope. The digital isolators from Texas Instruments might have a diode that starts to conduct and prevents the voltage rise. With data rate of $0Mbps$, and input low, the typical error condition for Texas Instruments were sharp spikes at 5V, most of the time only individual spike occurred. Sometimes the output locked to high for a period of one bit, or multiple sharp spikes occurred in a row. The most typical error condition is presented in Figure 33.

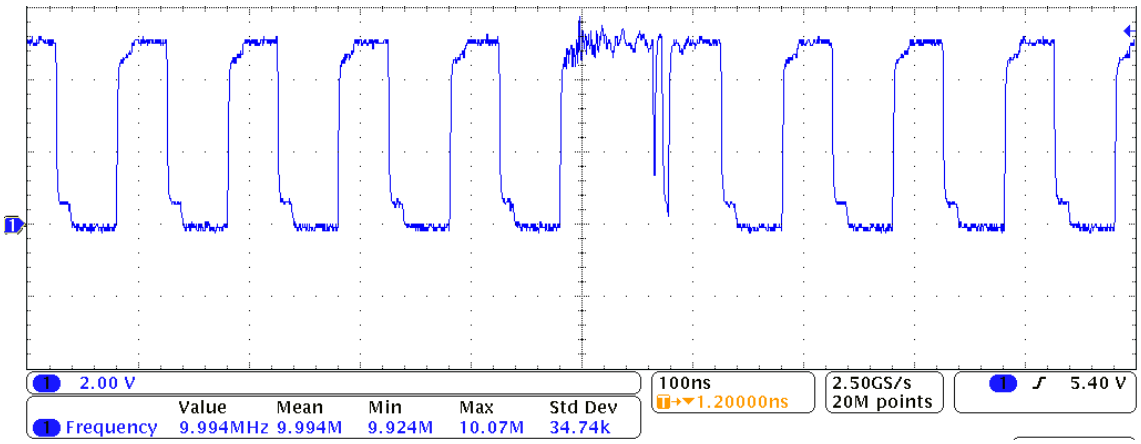

Figure 32: Typical error condition for Texas Instrument at a data rate of $20Mbps$.

The waveform of the digital isolators from Silicon Labs had a similar peak, caused by ringing due to mismatching as digital isolators from Maxim, therefore higher trigger level had to be used for the oscilloscope and some errors might not be observed. The typical error condition in Silicon labs with data rate of $20Mbps$ were spikes, occurring individually or few in a row. A group of spikes is presented in Figure 34. The same error condition occurred with a data rate of 0Mbps and input low. The number of spikes being 1 or 2. The error condition is presented in Figure 35.

The waveform of the digital isolators from Analog Devices was similar to Texas Instruments. If the ESD injection caused an extra voltage at a phase where the waveform had just raised high and was lower than it should be, the oscilloscope might

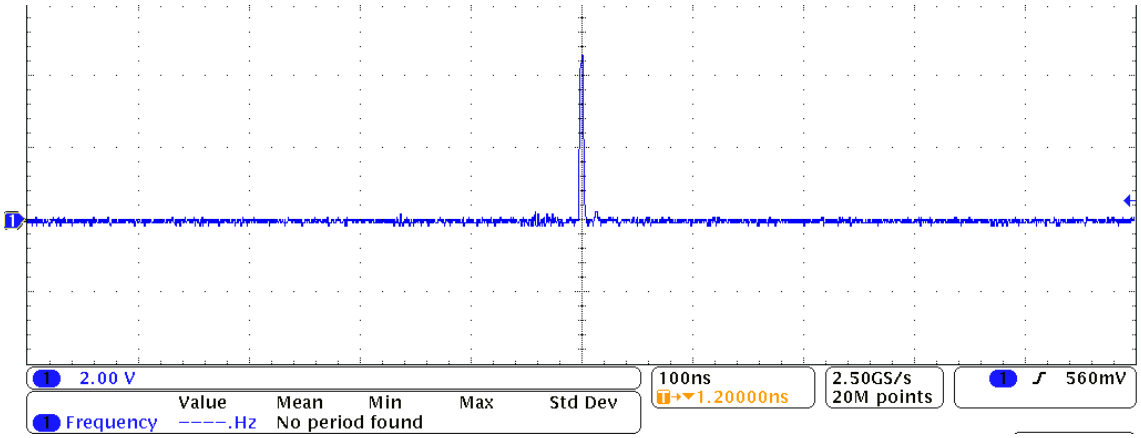

Figure 33: Typical error condition for Texas Instrument at a data rate of $0Mbps$, input low.

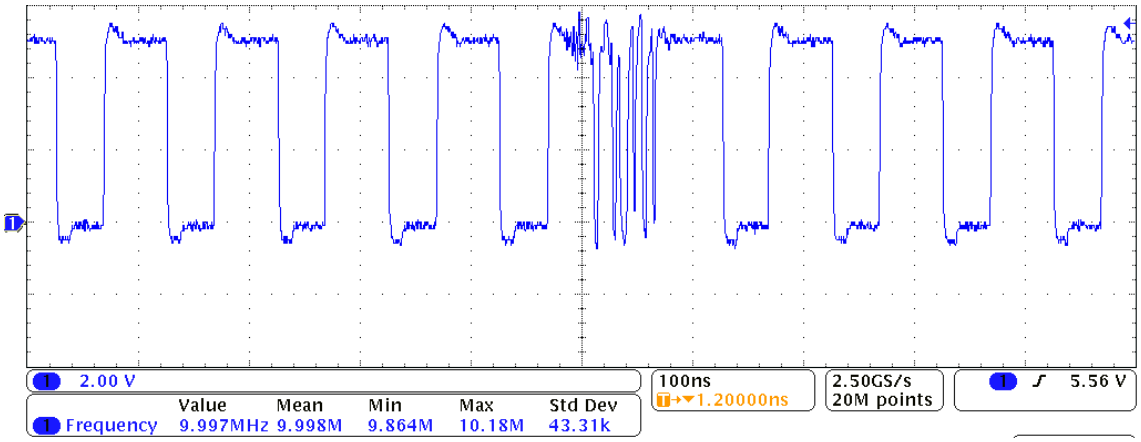

Figure 34: Typical error condition for Silicon Labs at a data rate of $20Mbps$.

have not triggered and the possible errors not observed. The typical error condition for Analog Devices with data rate of $20Mbps$ were sharp spikes and locking of a bit for a while. This is presented in Figure 36. The typical error condition with a data rate of $0Mbps$, and input low were sharp individual spikes at a voltage level of 2V or 4V. This is presented in Figure 37.

Digital isolators from Silicon Laboratories had the highest withstand voltages with data rates of $20Mbps$ and $0Mbps$. The withstand voltages for Silicon Laboratories was $2kV$ higher than the digital isolators from other manufacturers. The digital isolators from other manufacturers had poor ESD withstand capabilities compared to digital isolators from Silicon Laboratories.

The test setup was not corresponding to the standard IEC 61000-4-2, which is the test method for testing the ESD withstand capability in the product standard for variable-frequency drives, IEC 61800-3. However, the test setup used in this thesis corresponds well to the conditions where the digital isolators are being stressed in variable-frequency drive applications. The product standard IEC 61800-3 set a condition of allowing temporary disturbed communication, but no error reports

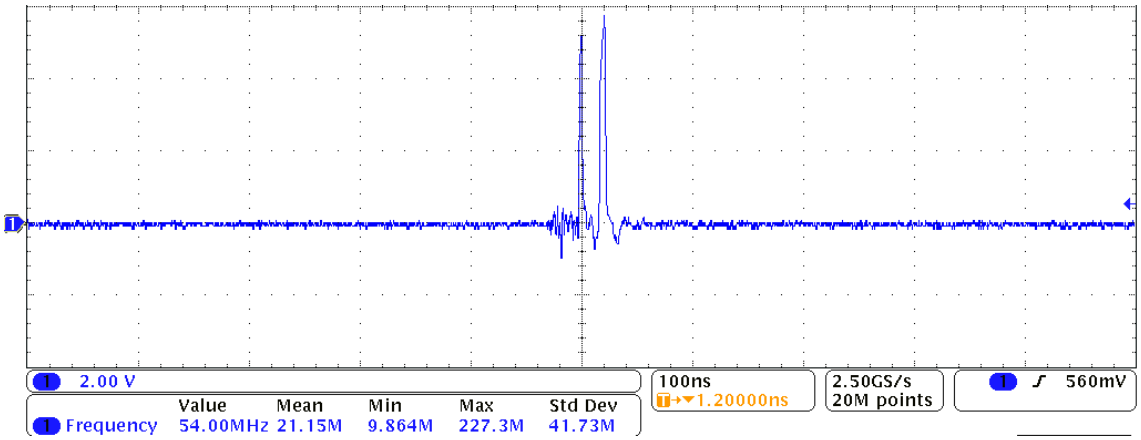

Figure 35: Typical error condition for Silicon Labs at a data rate of $0Mbps$, input low.

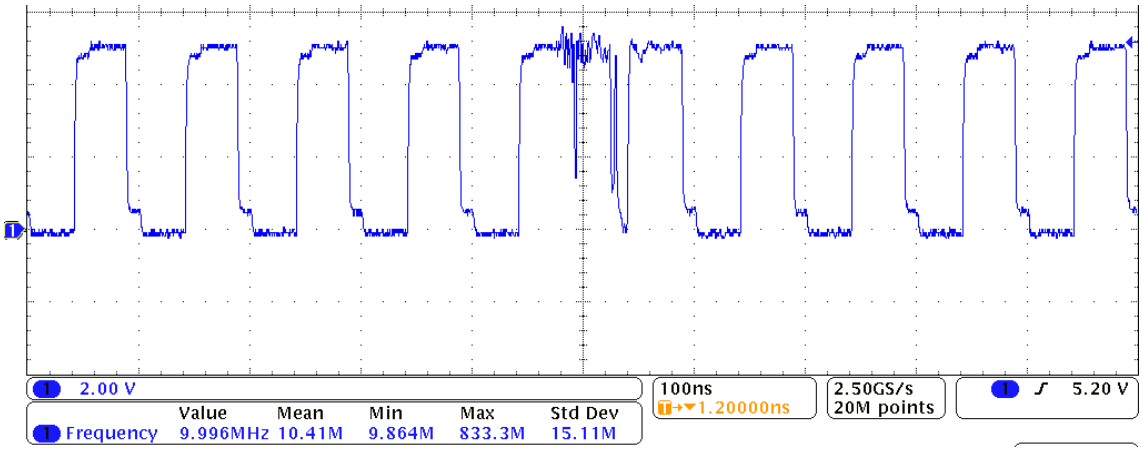

Figure 36: Typical error condition for Analog Devices at a data rate of $20Mbps$.

that could cause shut down at a ESD injection level of $4kV$. The test in this thesis does not provide the information whether the disturbance could cause a shut down at these levels. The most important result is that Silicon Laboratories performed significantly better than the peers in the indirect ESD test. However, additional tests are recommended before using digital isolators in variable-frequency drives.

5.3 Electrical fast transient/burst immunity test

The measurements of electrical fast transient/burst immunity were made mostly according to the standard IEC 61000-4-4. The test voltage was up to $3kV$ with steps of $250V$, or until the isolators were interfered. A transient burst consisted of 75 voltage pulses with injection frequency of $5kHz$. These transient bursts were injected to GND2 of the test PCB at a frequency of $1Hz$ for 50 times for each test voltage level and polarity. Also, the test was repeated without the input signal. The GND1 of the test PCB was grounded to the reference ground. And, the distance of the PCB from the conductive plane was approximately $7cm$. The test setup is

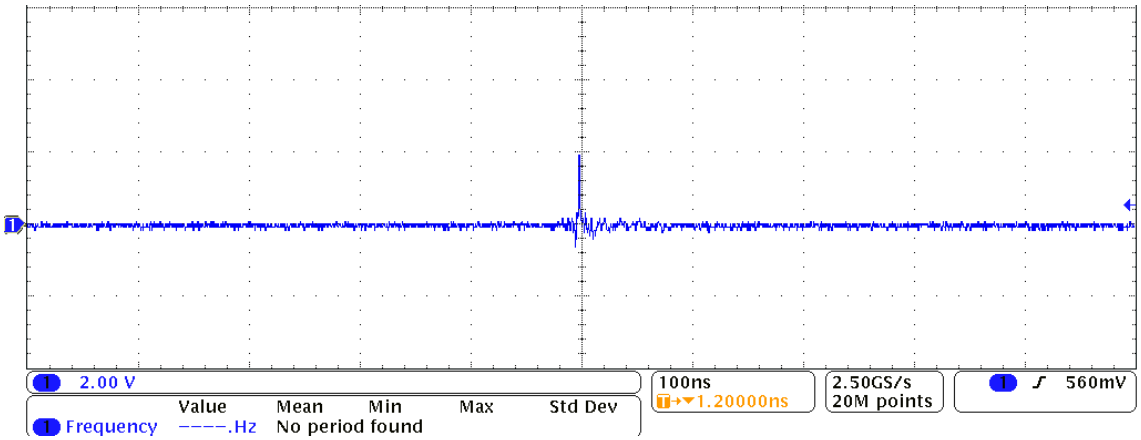

Figure 37: Typical error condition for Analog Devices at a data rate of $0Mbps$, input low.

Table 6: ESD withstand levels from the measurement with data rate of 20Mbps.

Voltage (kV)	Manufacturer			
	Maxim	Silabs	TI	AD
± 1				
± 2				
± 3				
± 4				
± 5				

- ESD withstand level is the highest ESD injection voltage at which no errors were observed. If the voltage is different for the opposite polarities, the smaller absolute value is the ESD withstand voltage.

shown in Figure 38.

The burst withstand levels are presented in Table 8. The digital isolators from given manufacturer were from the same batch. Nevertheless, the burst withstand had variance between the units of the same type. The differences in burst withstand for given type were limited to approximately $250V$. The differences between batches could further increase the spread between the highest and the lowest withstand levels. The polarity of a burst injection did have some effect. The withstand voltage could differ for $250V$ depending on the polarity.

Typical error condition for Silabs, TI and AD were sharp voltage spikes. These spikes occurred for Maxim as well, but Maxim was also susceptible to locking. These typical error conditions are presented in Figures 39 and 40. Digital isolators from Analog had the highest surge withstand capabilities. They achieved a burst withstand level of $1kV$. They are inductive digital isolators with small transformers which probably enhanced the robustness to common-mode burst voltages. However,

Table 7: ESD withstand levels from the measurement with data rate of 0Mbps, input is low.

Voltage (kV)	Manufacturer			
	Maxim	Silabs	TI	AD
± 1				
± 2				
± 3				
± 4				
± 5				

- ESD withstand level is the highest ESD injection voltage at which no errors were observed. If the voltage is different for the opposite polarities, the smaller absolute value is the ESD withstand voltage.

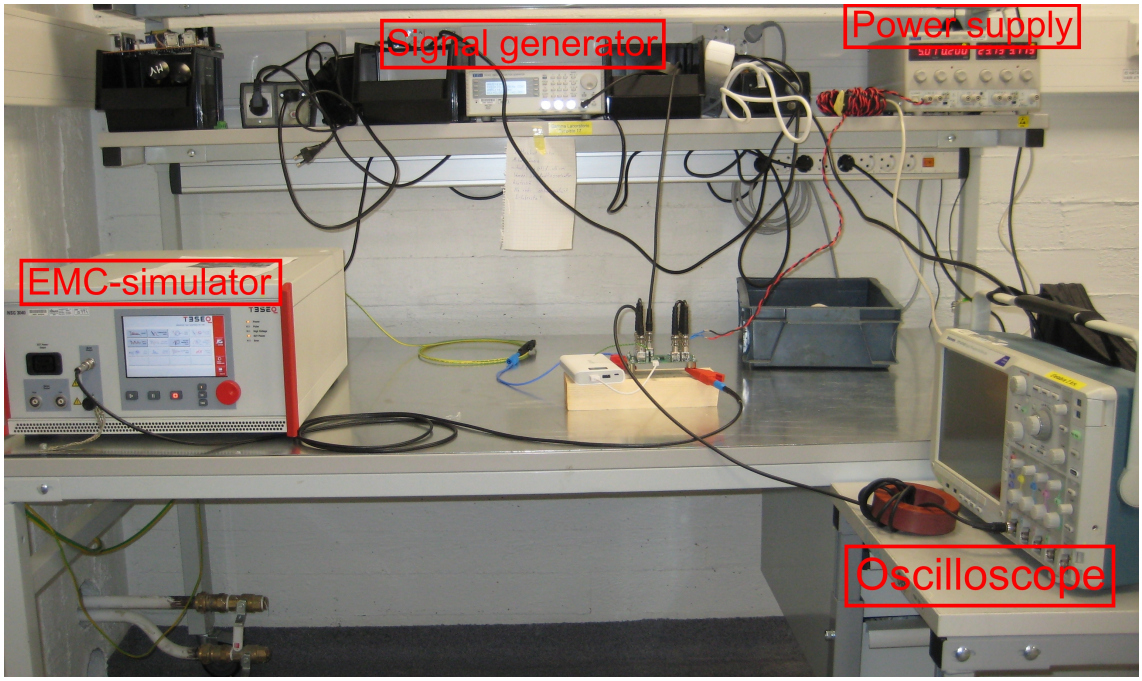

Figure 38: The setup for the burst test.

capacitive digital isolators from TI and Silabs were close with burst withstand level of 750V. Capacitive digital isolators from Maxim performed poorly in the burst withstand test. They were not able to pass the test at a burst voltage level of 250V. This demonstates that there are important factors other than the coupling method affecting the EMC withstand capabilities.

Table 8: Burst withstand levels from the measurement.

Voltage (V)	Manufacturer			
	Maxim*	Silabs	TI	AD
±250				
±500				
±750				
±1000				

*Did not pass the test at voltage level of 250V.
- Burst withstand level is the highest surge injection voltage at which no errors were observed. If the voltage is different for the opposite polarities, the smaller absolute value is the burst withstand voltage.

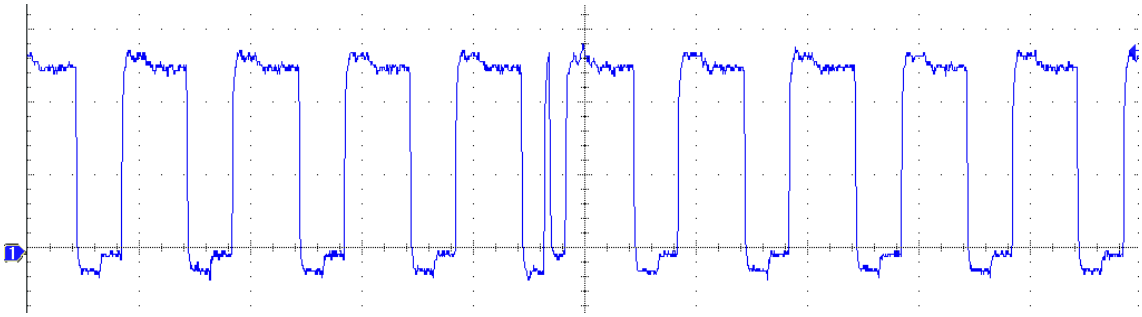

Figure 39: Typical error condition for Silabs, TI and AD.

5.4 Surge immunity test

The measurements of surge immunity were made mostly according to the standard IEC 61000-4-5. A total of 10 surge voltage pulses were injected with intervals of 10 seconds between the ground levels of the test PCB. First five of the pulses were positive polarity and the other five were negative polarity. Neither side of the test PCB was grounded. The measurements were made without the input signal as it was

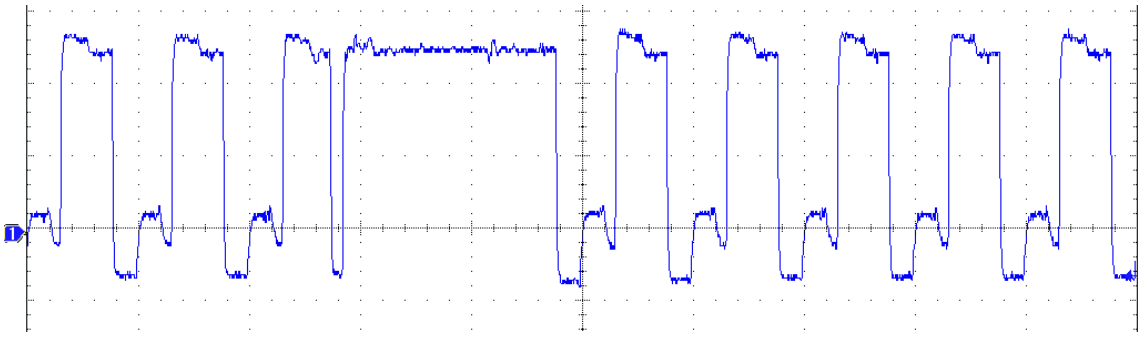

Figure 40: Typical error condition for Maxim.

observed that the oscilloscope did not trigger consistently to the surge injections and therefore the results would have been unreliable. The test voltage was up to 4250V with steps of 250V, or until the isolator was interfered. The test setup was similar to the one used in electrical fast transient/burst immunity test, and it is shown in Figure 41.

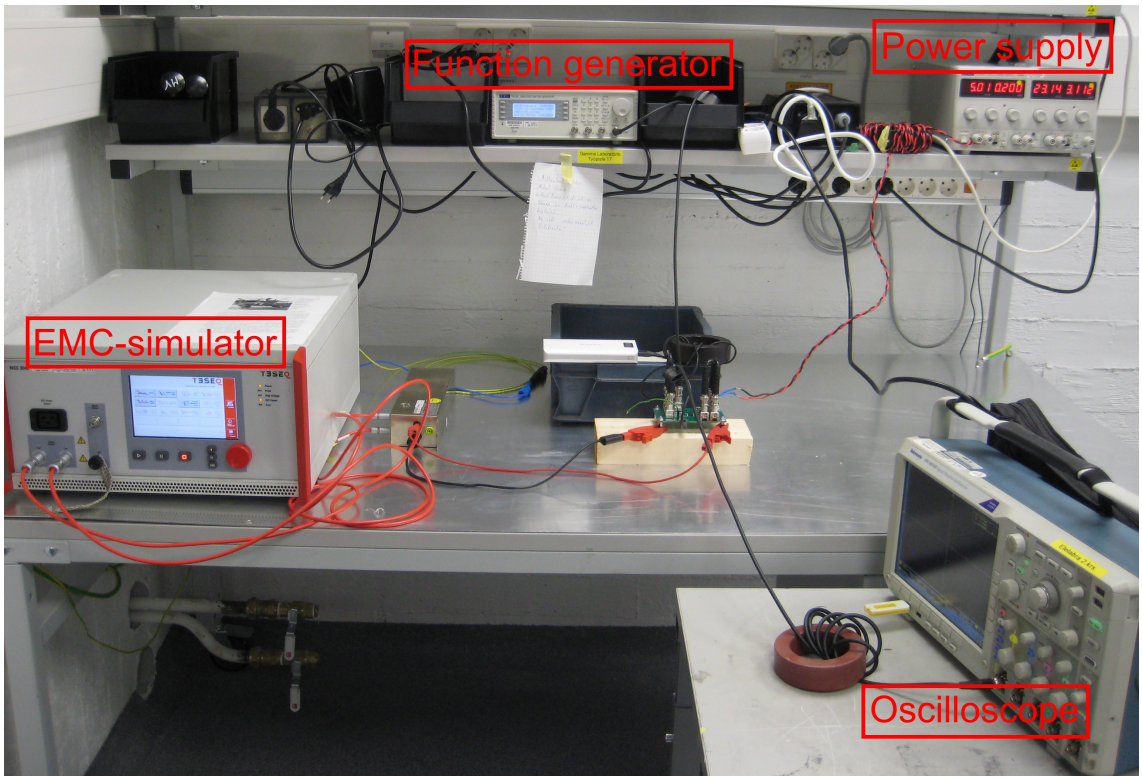

Figure 41: The setup for the surge test.

The surge withstand levels are presented in Table 9. The digital isolators from given manufacturer were from the same batch. Nevertheless, the surge withstand had variance between the units of the same type. The differences in surge withstand were almost 3000V between the lowest Maxim unit and the best Maxim unit. Analog had a difference of 1250V between its best and worst performing units. The differences between batches could further increase the spread between the highest and the lowest withstand levels. Silicon laboratories and TI passed the test at its highest voltage apart from one unit from Silicon laboratories that failed the test at 4250V. Therefore, it is impossible to say if such a high differences in performances occur for Silicon laboratories and TI. Also, the number of units of given component type is too small to make proper conclusions. The polarity of an surge injection had an effect. The withstand voltage could differ for 500 to 1500V depending on the polarity. Generally, the withstand for negative polarity surges was significantly better. Typical error conditions were voltage spikes. In addition, locking of output occurred in Maxim.

Table 9: Surge withstand levels from the measurement.

Voltage (V)	Manufacturer			
	Maxim	Silabs	TI	AD
±1250				
±1500				
±1750				
±2000				
±2250				
±2500				
±2750				
±3000				
±3250				
±3500				
±3750				
±4000				
±4250				

- Surge withstand level is the highest surge injection voltage at which no errors were observed. If the voltage is different for the opposite polarities, the smaller absolute value is the burst withstand voltage.

5.5 Magnetic field immunity test

The ability of the digital isolators to withstand magnetic fields was tested by exposing the isolators to a magnetic field that is typical in variable-frequency drives. The measurement was repeated with three different directions of magnetic field to see how it affects the results. In position A, the magnetic field was in right angle with the PCB-plane. Position A is presented in Figure 42. In position B, the magnetic field was pointing along the isolation barrier of the PCB, and the PCB had its longer side pointing towards the current loop. Position B is presented in Figure 43. In position C, the magnetic field was pointing across the isolation layer of the PCB, and the PCB had its shorter side pointing towards the current loop. The GND1 side that was connected to the signal generator and oscilloscope was pointing upwards in position C. Position C is similar to position B, but the PCB is rotated 90° from position B so that its shorted edge is facing the loop.

The current loop used in creating the magnetic field had two windings. A current pulse of up to 1200A was injected through the loop. The pulse duration was 300µs, with a rise and fall time of 100µs. The test was made with input signal low and high. The diameter of the current loop was approximately 18.5cm. The setup is presented in Figure 44. None of the digital isolators were interfered in the test. The inductance of the loop was limiting the maximum test current. The current was not increased above 1200A to avoid damage in the test equipment. Nevertheless, the ability of all

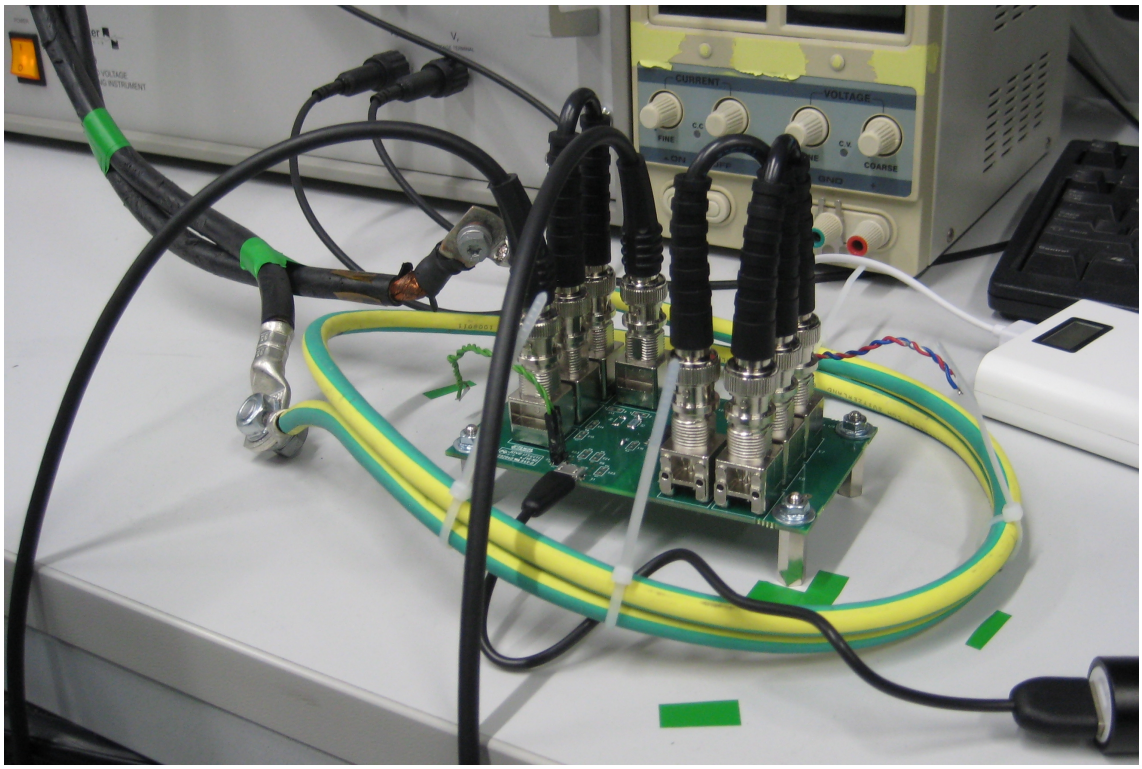

Figure 42: The position A in magnetic field immunity test.

digital isolators to pass the test with a current pulse of 1200A is a promising result.

5.6 RF field immunity test

The ability of digital isolators to withstand RF-fields was measured applying standard IEC 61000-4-3. The measurements were made in the Laplacell 300/2 Model B02 chamber. The measurement was repeated in two directions of the PCB, because the chamber did not have a rotating antenna. The PCB placement and directions are presented in Figures 45 and 46.

The interference signal was modulated using 1kHz amplitude modulation with depth of 80%. Each measurement frequency was sampled for a period of 2 seconds. The frequency range for the test was 30MHz to 1GHz, with 5% frequency increment step. The test was made with and without input signal. The test was repeated at different field strength levels until a level where no errors occurred in any position, or with or without the input signal was found. The maximum field strength used was $20V/m$, and it was decreased with steps of $5V/m$.

The field strength within the chamber could be different from the set value depending on the frequency and placement of the device. Therefore, the absolute levels used in the test are only comparable with each other. However, if the test result is lower than what is required in the application, further research is recommended. The system level standard for variable-frequency drives IEC 61800-3 sets a minimum RF-field withstand level of 10V/m for systems operating in second environment. At

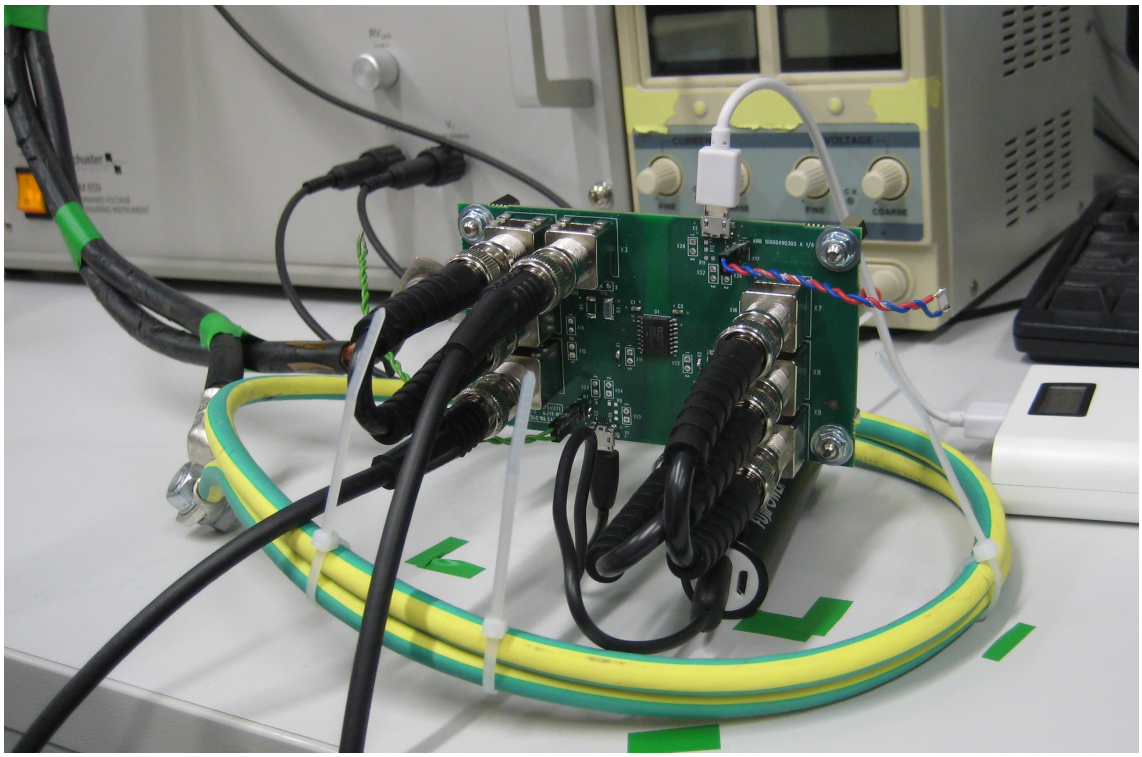

Figure 43: The position B in magnetic field immunity test. In position C the PCB was rotated 90°, with its shorter side facing the table.

this level, the communication should be undisturbed. In addition, it was found that some interferences occurred at only a narrow frequency band, that could be less than then 5% frequency increment step used. Therefore, some interferences at those frequencies could have not been observed. In further testing, the frequency increment step should be less than 2%.

The RF-field withstand levels are presented in in Table 10. Digital isolators from Silicon Laboratories were not disturbed at the highest field strength level used in the measurements ($20V/m$). Digital isolators from Analog Devices had a RF-field withstand level of $15V/m$. Digital isolators from Analog Devices performed better in sideway position than in upwards position. The interference frequency band was wider in upward position and the coupling of interference was stronger. The interference frequencies for Analog Device were in the range of 700 to 750 MHz.

Digital isolators from Texas Instruments had a RF-field withstand level of $5V/m$. The position did not have a noticeable effect on the coupling of interference. The interference occurred at frequency ranges: 180-240MHz, 480-790MHz and 880-900MHz. Digital isolators from Maxim did not pass the withstand test at the lowest test voltage ($5V/m$). The interference occurred at frequency ranges: 170-280MHz, 480MHz and 520-900MHz.

The digital isolators from Maxim, Texas Instrument and Silicon Laboratories were capacitive digital isolators. Digital isolator from Analog Devices was inductive digital isolator. Capacitive digital isolators had a RF-field withstand level ranging from over

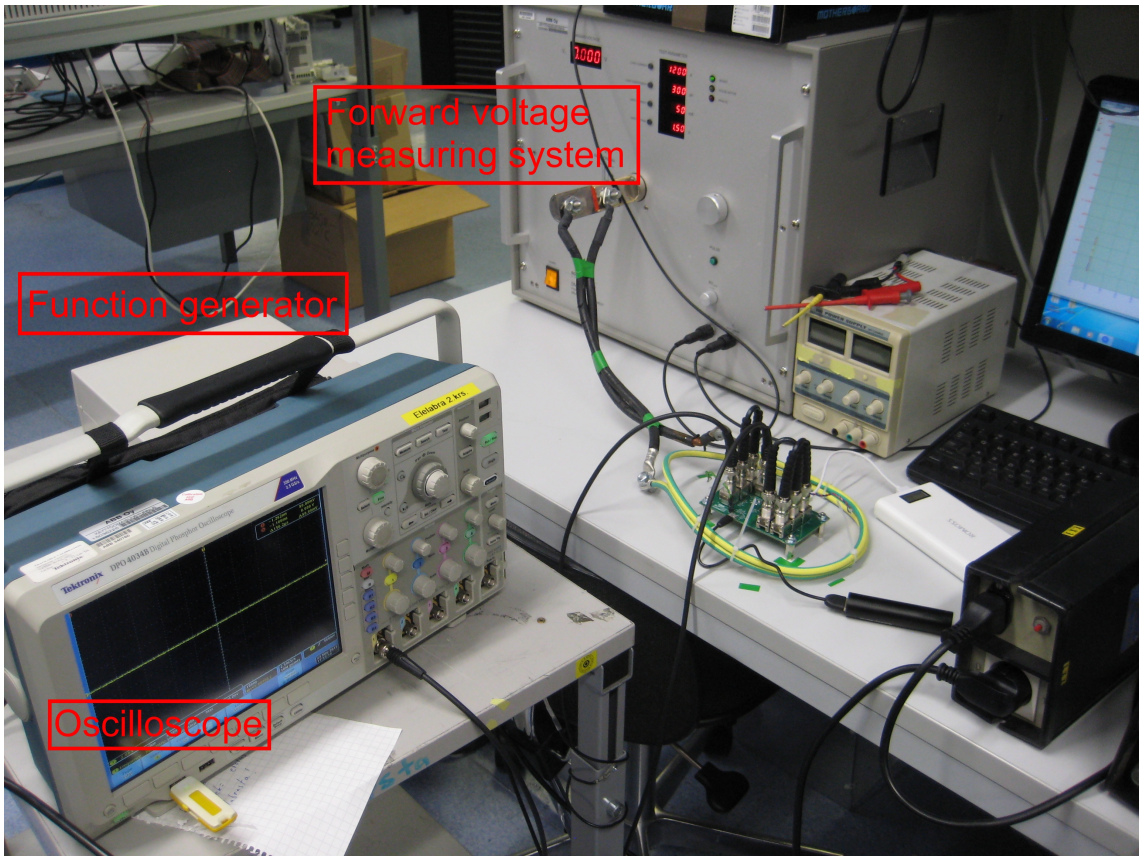

Figure 44: The setup for the magnetic field immunity test.

Table 10: RF-field withstand levels from the measurement.

Field strength (V/m)	Manufacturer			
	Maxim*	Silabs	TI	AD
5				
10				
15				
20				

- RF-field withstand level is the level at which no errors were observed.
* Did not pass the test at field strength of $5V/m$

$20V/m$ to below $5V/m$. Inductive digital isolator selected in the test from Analog Devices achieved a RF-withstand level of $15V/m$. The difference in RF-withstand performance within capacitive digital isolators presents that the coupling technology is not the sole factor in determining the withstand capabilities to RF-fields. Another interesting observation is that the interference frequencies were much wider for the

Figure 45: PCB placement in the chamber at sideway position.

Figure 46: PCB placement in the chamber at upward position.

capacitive digital isolators. Inductive digital isolators had only a small band of frequencies where interference occurred.

5.7 Partial discharge test

Voids can be created to the insulation material or package of the device during manufacturing process. These voids can experience higher electric fields under stress. This results in a transfer of charge across the void. The repeated transfer of charge can make the void larger and eventually cause the insulation to fail. A partial discharge test detects these voids, and devices containing too many of them can be rejected. Partial discharge is measured in pico-Coulombs, and standards set a threshold of $5nC$. [51, 52] Partial discharge test is made by the manufacturer for all the devices using production test method presented in Sections 3.1 and 3.2.

A purpose to conduct a partial discharge test in this thesis is to determine a partial discharge inception and extinction voltages for digital isolators of different manufacturers. The measurements were made with SOKEN Partial Discharge Tester DAC-PD-7. The device can output a voltage of $3kV_{\mathrm{RMS}}$. The test voltage was set to the maximum value of $3kV_{\mathrm{RMS}}$ incrementing from 0V at a rate of $50V/s$. The threshold for partial discharge inception and extinction was set to $10pC$. The rate of the test pulse was $50Hz$. The device was calibrated with auto calibration for each test device, the calibration level was set to $100pC$ for all the devices. The test setup can be seen in Figure 47.

No partial discharges occurred during the tests. The maximum output voltage of SOKEN Partial Discharge Tester DAC-PD-7 was too low to cause a partial discharge in any of the devices. However, an interesting observation was made when the test was made with the bar in upwards position. In upward position both the high-voltage and COM were in touch with the sheet. At this position partial discharges were detected at a voltage of approximately $2kV_{\mathrm{RMS}}$. The discharge did not occur when the bar was sideways in a way that the high-voltage was upwards few centimeters from the sheet as in Figure 47. Therefore, it was concluded that the partial discharge observed happened on the sheet and not in the isolator. This is an interesting result, it indicates that the pollution accumulating over time on the PCB or on the package of the isolator could provide a path where the partial discharge could happen at significantly lower voltage than what the isolator could handle. This effect is called tracking, it is presented in Section 3.4.

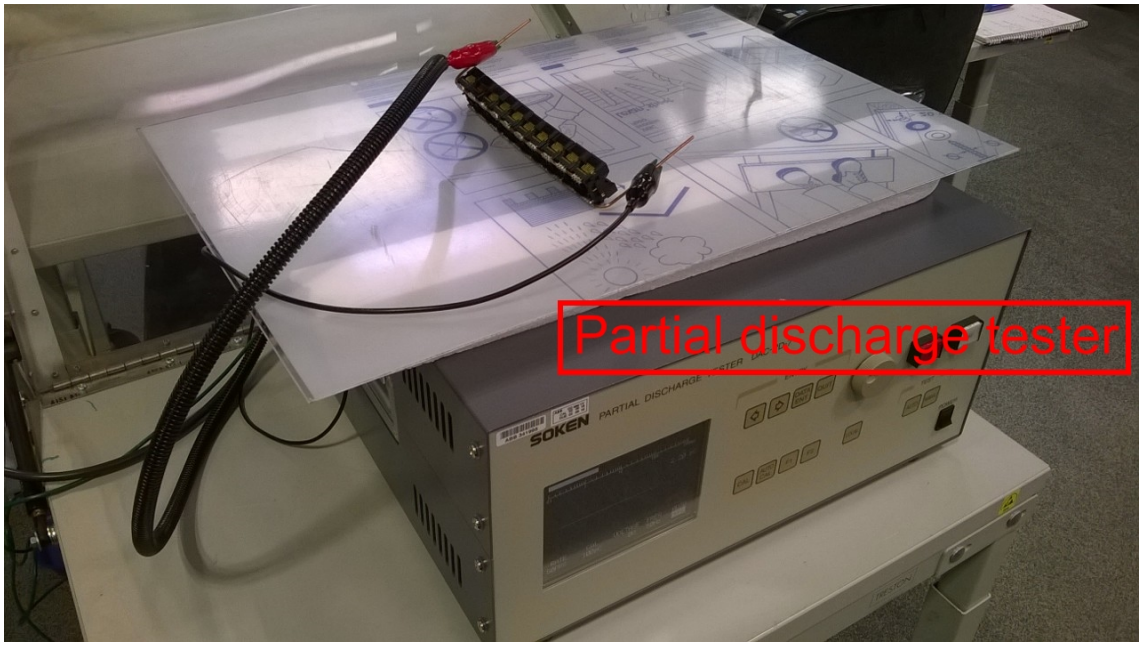

Figure 47: The setup of the partial discharge test.

6 Conclusions

CMOS digital isolator employ three different coupling methods to transmit the data across the isolation barrier. This divides the CMOS digital isolators to inductive, capacitive and GMR digital isolators. All of the coupling technologies have achieved an isolation voltage of 5kV or above. Currently, the working voltage of inductive digital isolators is limited to 600V, but the next generation inductive digital isolators are expected to have a working voltage of 1000V being on par with capacitive and GMR digital isolators. All coupling methods are able to achieve a surge voltage rating of 10kV, and therefore can fulfill the requirements for reinforced isolation.

Currently, digital isolators are tested using a VDE standard VDE 0884-10, or an international standard IEC 60747-5-5. The VDE standard is a standard for magnetic and capacitive isolators, but the IEC 60747-5-5 is a standard for optocouplers. Nevertheless, the optocoupler standard is being used to test and verify CMOS digital isolators. However, an international standard covering the magnetic and capacitive isolators is currently in draft mode, and it is expected to be released within the next few years. The new standard is based on the VDE standard VDE 0884-10 and it contains methods to assess the lifetime of CMOS digital isolators.

The direct per channel cost of digital isolator is currently significantly below the per channels price of optocouplers with turn on/turn off time in range of 200ns. Digital isolators have a per channel cost approximately 30% below the channel cost of optocouplers of this speed. However, the channel cost of slower optocouplers with turn on/turn off time of range in 3000ns is approximately four times cheaper than the channel cost of digital isolators. Therefore, if the slower speed is sufficient, optocouplers are probably the most cost effective alternative, but with higher speeds digital isolators begin to be more cost effective. When taking indirect costs from the assembly and PCB area required into account, the digital isolators are a competitive solution in many isolation functions. If the volumes of digital isolators are equal to the optocoupler volumes, digital isolator implementations can be approximately 10 to 20% cheaper than optocoupler implementations. The cost benefit is even higher in favor to digital isolators versus a transformer implementation. The cost benefit of digital isolators versus transformers for PSL-2 link function can be 20% to 50% depending on the digital isolator volumes.

The price of digital isolators is not expected to change much in the next three years. The competition is tight, and the isolators are manufactured using mature standard CMOS processes. Therefore, cost decrease from enhanced manufacturing methods is limited. Possible increase in the market volumes could decrease the needed volume by individual customers to gain the volume discount prices for the isolators. This would allow the customers to use digital isolators cost effectively when higher speed is required, and optocouplers when a turn on/turn off time of approximately 3000ns is sufficient.

There are concerns regarding CMOS digital isolators EMC characteristics. In this thesis, measurements were made to gain insight about the modern family CMOS digital isolator's EMC characteristics. The tests measured the immunity to different EM phenomena. In addition, a partial discharge test was made with a goal to find

differences between manufacturers and a limit where the partial discharge occurs.

There was high difference in the EMC performance between different manufacturers. Digital isolators from Silicon Laboratories were in the top group of manufacturers in all of the tests. Their performance was especially good in the indirect ESD immunity test when compared to other manufacturers. Analog Device was the only inductive digital isolator. It had the highest burst withstand level. This is most likely a result from the coupling method. Inductive digital isolators use miniature transformers that have intrinsic high CMTI. Capacitive digital isolators use differential pair capacitors, but there could be a small mismatch in the timing between the differential paths that could explain why the performance of capacitive digital isolators was slightly behind the performance of inductive digital isolators in the burst immunity test. Analog Devices performed well in the RF-field immunity test having withstand level of 15V/m.

Texas Instruments had the highest surge withstand level. It passed the test at the highest test voltage of $\pm 4250V$. Texas Instrument was in lower group of results in the indirect ESD immunity test, and in the RF-field immunity test. In general the performance in the indirect ESD immunity test was weak for all except Silicon Laboratories who had a withstand level of $\pm 4kV$. The performance of Maxim's digital isolator was is the lower group in all of the immunity tests. Maxim did not pass the tests at the lowest test voltages in burst immunity, and RF-field immunity tests. All of the tests were performed on three units of particular type. The units were from the same batch. The difference between test units was limited to one test level step for each test. An exception was the surge immunity test. The surge withstand level difference of Maxim between lowest and highest was almost 3000V. The difference between lowest and highest levels for Analog Devices was 1250V. The reliability of the results could be enhanced by increasing the unit count for each type, this would be beneficial especially in the surge immunity test where high difference in performance between units of the same time were observed. Also, units from different manufacturing batches could be tested to gain more reliable results of the performance of each manufacturer and component type.

The test expose the digital isolators to similar conditions they could face in a variable-frequency drive application. Although the tests differed from the standard tests, the minimum EMC requirements for EM immunity given in the system level standard IEC 61800-3 can be used to assess the tests performed with caution. For example, the standard sets a minimum withstand level to RF-field immunity to 10V/m at which no error in the communication can occur. Two of the manufacturers, Maxim and Texas Instruments, did not pass this limit. However, the results are only directional because the tests were not standard tests. Another test with low withstand levels was the indirect ESD test. The standard set a limit for contact discharge of 4kV, at which errors in the communication are allowed but the device must be self-recoverable. The communication was interfered at levels of 1kV for Maxim and Analog Devices, however the devices were self-recoverable. The EMC tests performed indicate that digital isolators can be used in the variable-frequency drives, but designers are recommended to make proper tests to the designs to prove the immunity characteristics to different EM phenomena. In addition, the

reliability of digital isolators in the long term is a concern for the designers as the lifetime expectation of variable-frequency drives is 10 to 30 years. However, the new international standard for the magnetic and capacitive isolators that is currently in draft mode sets methods to assess the long term reliability and lifetime of the isolators. A standard method could assure designers about the lifetime predictions of decades provided by the digital isolator manufacturers.

The primary goal for the measurements in the thesis was to compare EMC characteristics of CMOS digital isolators between different manufacturers. The measurements presented that there were big differences in the EMC characteristics between the manufacturers. In addition the goal for the thesis was to present how the current CMOS digital isolators compare to optocouplers, and whether CMOS digital isolators can be a cost effective alternative to optocouplers. Also the goal was to present requirements for the isolation and how it is employed in variable-frequency drives. The thesis met these goals succesfully.

The results for the EMC measurements provide comparison between the EMC capabilities of the modern CMOS digital isolators. The measurements were not standard tests. Therefore, the absolute values cannot be compared directly to the limits set in system level standard IEC 61800-3. Further study to assess the margin to the minimum withstand requirements set in IEC 61800-3 would be the next step. The measurements should be made according to the standard to the variable-frequency drive unit. In addition, a study of the EMC charasteristics with more units from different batches would be valuable to provide more reliable results and statistics.

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A Test PCB layout

The test PCB has 6 layers. The top layer of the PCB and the component placement is presented in Figure A1.

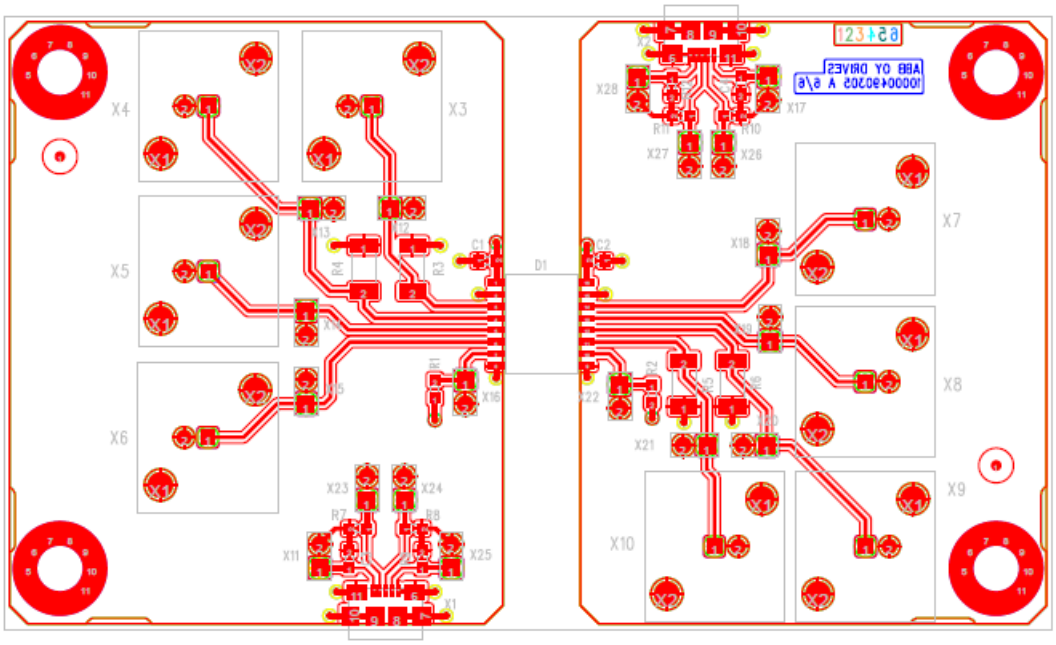

Figure A1: Layout of the test PCB.

B Test PCB schematic