CMOS integrated Circuits for RF-powered Wireless Temperature Sensor

Shailesh Singh Chouhan

Aalto University

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CMOS Integrated Circuits for RF-powered Wireless Temperature Sensor

Shailesh Singh Chouhan

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Abstract

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Abstract

This dissertation presents original research contributions in the form of twelve scientific publications that represent advances related to RF-to-DC converters, reference circuits (voltage, current and frequency) and temperature sensors. The primary focus of this research was to design efficient and low power CMOS-based circuit components, which are useful in various blocks of an RF-powered wireless sensor node.

The RF-to-DC converter or rectifier converts RF energy into DC energy, which is utilized by the sensor node. In the implementation of a CMOS-based RF-to-DC converter, the threshold voltage of MOS transistors mainly affects the conversion efficiency. Hence, for the first part of this research, different threshold voltage compensation schemes were developed for the rectifiers. These schemes were divided into two parts; first, the use of the MOSFET body terminal biasing technique and second, the use of an auxiliary circuit to obtain threshold voltage compensation. In addition to these schemes, the use of an alternate signaling scheme for voltage multiplier configuration of differential input RF-harvesters has also been investigated.

A known absolute value of voltage or current is the most useful for an integrated circuit. Thus, the circuit which generates the absolute value of voltage or current is cited as the voltage or current reference circuit respectively. Hence, in the second part of the research, simple, low power and moderately accurate, voltage and current reference circuits were developed for the power management unit of the sensor node. Besides voltage and current reference circuits, a frequency reference circuit was also designed. The use of the frequency reference circuit is in the digital processing and timing functions of the sensor node.

In the final part of the research, temperature sensing was selected as an application for the sensor node. Here, voltage and current based sensor cores were developed to sense the temperature. A smart temperature sensor was designed by using the voltage cores to obtain temperature information in terms of the duty-cycle. Similarly, the temperature equivalent current was converted into the frequency to obtain a temperature equivalent output signal.

All these implementations were done by using two integrated circuits which were fabricated during the year 2013-14.

Keywords CMOS circuit , RF-to-DC converters, voltage reference circuit, current reference circuit, frequency reference circuit, temperature sensors

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Preface

This dissertation is based on the work done at the Electronic Circuit Design Laboratory of Aalto University. This work is accomplished in the project, which is funded by the AUTOVOLT of the Academy of Finland and EFFINANO of the Aalto University, Finland. I have been supported financially by the Erasmus Mundus External Cooperation Window India4EU project (Lot 13c) scholarship, to which I express my sincere gratitude. I sincerely appreciate the financial support provided by the scholarship received from the Nokia Foundation during my research.

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Many thanks to my colleagues at the Department of Micro- and Nanosciences, with whom I have worked on projects. I appreciate the patience shown by them during my weird technical discussions and making the lab a great place to work for me. Especially, I would like to thank Mr. Jakub Gronicz, Mr. Jarno Salomaa, Mr. Mika Pulkkinen and Mr. Tuomas Haapala. I am also thankful to Mr. Ali Vahdati, Mr. Matthew Turnqvist, Mr. Karthik

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And finally, last but certainly not least, I wish to thank my beloved wife Barkha for her affection, absolute love and precious support. She is my teacher who taught me how to be a fighter in the toughest period of the life. If it wasn't for her continuous love and support, I wouldn't even imagine achieving my goals in doctoral studies. She is the chosen one whom made my difficult times bearable and my good times more special. I am very fortunate to have her as my soulmate.

Espoo, November 13, 2015
Shailesh Singh Chouhan

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I Chouhan S.S. and Halonen K. The design and implementation of DTMOS biased all PMOS rectifier for RF energy harvesting. *Proceedings of the 12th IEEE International New Circuits and Systems Conference (NEWCAS), Trois-Rivieres, QC Canada*, pp. 444–447, Jun. 2014.

II Chouhan S.S. and Halonen K.. The DTMOS based UHF RF to DC conversion. *Proceedings of the 20th IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Abu Dhabi, UAE*, pp.629–632, Dec. 2013.

III Chouhan S.S. and Halonen K. Internal Vth cancellation scheme for RF to DC rectifiers used in RF energy harvesting. *Proceedings of the 21st IEEE International Conference on Electronics, Circuits, and Systems (ICECS), Marseille, France*, pp.235–238, Dec. 2014.

IV Chouhan S.S. and Halonen K. Threshold voltage compensation scheme for RF-to-DC converter used in RFID applications. *Electronics Letters*, vol.51, no.12, pp.892-894, Jun. 2015.

V Chouhan S.S. and Halonen K. A novel cascading scheme to improve the performance of voltage multiplier circuits. *Analog Integrated Circuits and Signal Processing, Springer*, vol.84, no.3, pp.373-381, Sep. 2015.

VI Chouhan S.S. and Halonen K. Design and implementation of all MOS micro-power voltage reference circuit. *Analog Integrated Circuits and Signal Processing, Springer*, vol.80, no.3, pp.399–406, Sep. 2014.

VII Chouhan S.S. and Halonen K. Design and implementation of a micro-power CMOS voltage reference circuit based on thermal compensation of Vgs. *Microelectronics Journal, Elsevier*, vol.46, no.1, pp.36–42, Jan. 2015.

VIII Chouhan S.S. and Halonen K. A 0.67μW, 177 ppm/$^{\circ}$C all MOS current reference circuit in 0.18μm CMOS technology. *Submitted to IEEE transaction on circuits and systems-II: Express Briefs*, .

IX Chouhan S.S. and Halonen K. A micro power temperature compensated frequency generating circuit. *Proceedings of 22nd European conference on circuit theory and design (ECCTD),Trondheim, Norway, Aug.24–26*, pp.1-4, Aug. 2015.

X Chouhan S.S. and Halonen K. Design and implementation of micro-power temperature to duty cycle converter using differential temperature sensing. *Microelectronics Journal, Elsevier*, vol.46, no.6, pp.482–489, Jun. 2015.

XI Chouhan S.S. and Halonen K. Nano-ampere PTAT current source with temperature inaccuracy $< \pm 1^{\circ}$C. *Electronics Letters*, vol.51, no.1, pp.60–61, Jan. 2015.

XII Chouhan S.S. and Halonen K. A low power temperature to frequency converter for the on-chip temperature measurement. *IEEE Sensors Journal*, vol.15, no.8, pp.4234-4240, Aug. 2015.

Author's Contribution

Publication I: "The design and implementation of DTMOS biased all PMOS rectifier for RF energy harvesting"

The author performed all circuit analysis, was responsible for the reported chip, performed all measurements, wrote the manuscript of the paper and presented the paper.

Publication II: "The DTMOS based UHF RF to DC conversion"

The author performed all circuit analysis and simulations, wrote the manuscript of the paper and presented the paper.

Publication III: "Internal Vth cancellation scheme for RF to DC rectifiers used in RF energy harvesting"

The author performed all circuit analysis, was responsible for the reported chip, performed all measurements, wrote the manuscript of the paper and presented the paper.

Publication IV: "Threshold voltage compensation scheme for RF-to-DC converter used in RFID applications"

The author performed all circuit analysis, was responsible for the reported chip, performed all measurements and wrote the manuscript of the paper.

Publication V: "A novel cascading scheme to improve the performance of voltage multiplier circuits"

The author performed all circuit analysis, was responsible for the reported chip, performed all measurements and wrote the manuscript of the paper.

Publication VI: "Design and implementation of all MOS micro-power voltage reference circuit"

The author performed all circuit analysis, was responsible for the reported chip, performed all measurements and wrote the manuscript of the paper.

Publication VII: "Design and implementation of a micro-power CMOS voltage reference circuit based on thermal compensation of Vgs"

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Publication X: "Design and implementation of micro-power temperature to duty cycle converter using differential temperature sensing"

The author performed all circuit analysis, was responsible for the reported chip, performed all measurements and wrote the manuscript of the paper.

Publication XI: "Nano-ampere PTAT current source with temperature inaccuracy $< \pm 1^{\circ}C$"

The author performed all circuit analysis, was responsible for the reported chip, performed all measurements and wrote the manuscript of the paper.

Publication XII: "A low power temperature to frequency converter for the on-chip temperature measurement"

The author performed all circuit analysis, was responsible for the reported chip, performed all measurements and wrote the manuscript of the paper.

List of Abbreviations

ADC	Analog to Digital Converter
BJT	Bipolar Junction Transistor
BTMOS	Body Tied to Source Metal Oxide Semiconductor
BVR	Bandgap Voltage Reference
CMOS	Complementary Metal Oxide Semiconductor
CTAT	Complementary To Absolute Temperature
DAC	Digital to Analog Converter
DTMOS	Dynamic Threshold Metal Oxide Semiconductor
EVC	External Vth Cancellation
EIRP	Effective Isotropic Radiated Power
FCC	Federal Communication Commission
FBB	Forward Body Bias
FOM	Figure Of Merit
FSNL	Full Scale Non Linearity
IoT	Internet-of-Things
IVC	Internal Vth Cancellation
KVL	Kirchoff Voltage Law
LR	Line Regulation
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-type Metal Oxide Semiconductor

PCE	Power Conversion Efficiency
PMOS	P-type Metal Oxide Semiconductor
PSRR	Power Supply Rejection Ratio
PTAT	Proportional to Absolute Temperature
QoS	Quality of Service
RBM	Resistor Less Beta Multiplier
RF	Radio Frequency
RFID	Radio Frequency Identification
SBB	Swapped Body Bias
SOI	Silicon-On-Insulator
SVC	Self Vth Cancellation
TC	Temperature Coefficient
VCE	Voltage Conversion Efficiency
VNA	Voltage Network Analyzer
VM	Voltage Multiplier
WSN	Wireless Sensor Network

List of Symbols

A_M	Area of MOSFET
A_E	Junction area of BJT
A_v	Voltage gain of matching network
C_{OX}	Oxide capacitance of MOSFET
C_{out}	Load capacitance per stage
C_{fly}	Fly capacitance
C_{pad}	Equivalent capacitance of pad
C_{rect}	Equivalent capacitance of rectifier
ΔV_{ripple}	Peak-to-peak ripple voltage
ΔX	Difference of maximum and minimum value of reference signal
f_{RF}	Frequency of RF signal
I_c	Collector current of BJT
I_s	Reverse saturation current of BJT
I_d	Drain current of MOSFET
I_{d0}	Saturation current of MOSFET
I_{load}	Load current
I_{supply}	Supply current
J_E	Current density of BJT
K	Boltzmann constant
L	Length of MOSFET
L_d	Diffusion length
L_{sc}	Residual inductance
LR_{nom}	Nominal line regulation
n	Number of fingers
N	Number of stages
P_{out}	Output power
P_{in}	Input RF power
P_{loss}	Power loss in each branch

P_{source}	Source power
q	Electronic charge
Q_c	Quality factor of capacitor
R_{ON}	ON-resistance of MOSFET
R_{in}	Input resistance of the rectifier
R_L	Load resistance
R_{pad}	Equivalent resistance of pad
R_{rect}	Equivalent resistance of rectifier
R_{ant}	Equivalent resistance of antenna
R_{sc}	Residual resistance
S_{11}	Single-ended reflection coefficient
S_{dd11}	Mixed mode differential-to-differential reflection coefficient
S_{cd11}	Differential-to-common mode reflection coefficient
S	Aspect ratio of transistor
t_d	Delay
TC	Temperature coefficient
T	Temperature
T_0	Ambient temperature
V_{BE}	Base-emitter voltage of BJT
V_{in}	Input voltage
V_{out}	Output voltage
V_{sg}	Source-gate voltage of MOSFET
V_{sd}	Source-drain voltage of MOSFET
V_{th}	Threshold voltage of MOSFET
V_{thp}	Threshold voltage of pMOSFET
V_{thn}	Threshold voltage of nMOSFET
$V_{out_{ideal}}$	Ideal value of the rectified DC voltage
V_{DC}	DC voltage
V_m	Peak amplitude of RF voltage signal
V_{thp0}	Zero bias threshold voltage of pMOSFET
V_{SB}	Source-body voltage
V_{supply}	Supply voltage
W	Width of MOSFET
X_{nom}	Nominal value of reference signal
X_{max}	Maximum value of reference signal
X_{min}	Minimum value of reference signal
Z_{fly}	Fly impedance
Z_{source}	Source impedance

Z_{in}	Input impedance
α_μ	Temperature independent constant for mobility
α_T	Thermal slope of threshold voltage
β_n	Transconductance parameter of nMOSFET
β_p	Transconductance parameter of pMOSFET
Γ	Reflection coefficient
γ	Body effect coefficient
η	Subthreshold slope
η_{ehu}	Efficiency of energy harvesting unit
$\eta_{antenna}$	Efficiency of antenna
η_{match}	Efficiency of matching network
η_{rect}	Efficiency of the rectifier
μ	Mobility parameter of MOSFET
ϕ_F	Fermi potential
χ	Voltage loss
ω_{srfc}	Self resonating frequency

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1. Introduction

1.1 Motivation

The Internet-of-Things (IoT) is becoming an essential part of daily life to bring about the implementation of the smart and proactive standards both at work and at home [1]. The Wireless Sensor Network (WSN) is one of the key building blocks of IoT [2], being a group of spatially located, specialized transducers with a communication infrastructure. These transducers commonly known as wireless sensor nodes, are used to monitor and record various physical, chemical and biological parameters at diverse locations [3]. The performance of the whole WSN is largely dependent on the performance of the individual wireless sensor nodes [4]. And these nodes are greatly affected by the strict power budget for sensing, computation and transmission of data [5].

Traditionally, the battery has been used as a power source for these sensor nodes [6–10], but due to their limited capacity the challenge lies with nodes becoming inoperable once the battery is drained. The maintenance of these batteries becomes costly as they require continuous monitoring and direct human involvement for management and battery replacement. It becomes impractical and unworkable when hundreds of sensor nodes are spread out widely over a large geographical expanse [11].

The limits associated with battery-operated sensor nodes has drawn interest towards the development of energy autonomous sensor nodes. Thus, to achieve energy autonomy in them an extra energy transducer is added to the board. As a result, it will be able to harvest energy from the surrounding environment or by using dedicated energy sources. The ambient energy sources present are mainly solar [12], heat [13], wind [14], water [15], inertial [16] and Radio Frequency (RF) waves [17] to self-

support the sensor node for an unlimited lifetime.

The strength of many of these sources is limited only by the environmental situation except for RF energy. The usage of RF energy is a promising option for energy harvesting due to the omnipresence of RF signals [18]. The concept of transmitting energy wirelessly was first proposed by Nikola Tesla in the year 1893 [19]. Since then, it has excited researchers and several experimental studies have been conducted to demonstrate the possibility of RF- energy harvesting [20].

In general practice, the maximum RF power level from the source has been restricted within Federal Communication Commission (FCC) exposure limits [21]. Therefore, with lower power density levels the conversion efficiency of RF energy transducers will be affected [22]. Hence, it will result in lower values of available power for sensor nodes to function.

This dissertation focused on developing new architectures for RF-energy transducers which can operate effectively with a lower input RF power level. In addition, low power Complementary Metal Oxide Semiconductor (CMOS) components or circuits, used in the sensor node were also developed,.

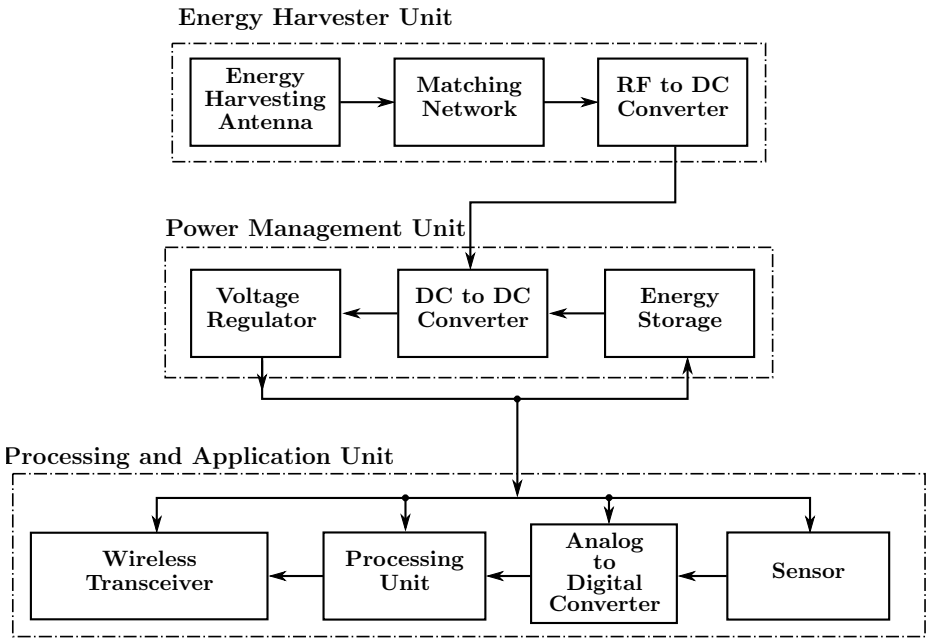


Figure 1.1. Block diagram of RF-powered wireless sensor node or system.

1.2 Research objectives

A typical block diagram of the RF-powered sensor node/system [23–25] is shown in Fig.1.1. The theoretical and the experimental work presented in the dissertation concentrates on three building blocks which are given in Fig.1.1. The specific contributions made in this dissertation for the development of a wireless sensor node are listed as follows:

1. **RF-to-DC converters for Energy Harvesting Unit**

   (a) Designed with body biasing techniques

   (b) Designed with threshold voltage compensation techniques

2. **Reference circuits for Power Management Unit**

   (a) Voltage reference circuit

   (b) Current reference circuit

   (c) Frequency reference circuit

3. **Processing and Application Unit**

   (a) Voltage-based temperature sensor

   (b) Current-based temperature sensor

These blocks and their design objectives differ widely from each other. However, all of the work focuses on the unified topic of making sensor nodes smaller and more efficient. The ultimate objective of the dissertation is to provide new implementations for RF energy harvesters and simple low-power CMOS components.

1.3 Content and thesis organization

The dissertation consists of two parts, the first providing an introductory background and the second being the compilation of the scientific publications [**I**]-[**XII**] by the author. The introductory part is comprised of five

chapters, which describe the design implementations and other relevant theories related to the original scientific contributions.

Chapter 2 provides an overview of the RF energy harvesting and highlights the key considerations and design challenges of the RF energy harvesters.

Chapter 3 is concerned with the temperature-independent reference circuits. The chapter opens with a discussion of the requirement and the performance parameters of the reference circuits It is then followed by a detailed investigation of the proposed voltage, current, and frequency reference circuits.

Chapter 4 incorporates the details related to realization of a low power temperature sensor. Two approaches have been adopted for temperature sensing namely, voltage and current based temperature sensing. The summary of these implementations and the experimental results are contained within this chapter.

The introductory part is concluded in Chapter 5 with a brief summary of the preceding chapters. In addition, the chapter also takes into account the primary outcomes of the dissertation and suggests directions for future work.

The second part of the dissertation consists of scientific publications [I]-[XII]. They are listed at pp. vii-viii and the author's contribution to each one is mentioned on pp. ix-xi. The publications explain the original contributions of this dissertation in greater detail.

1.4 Main scientific contributions

The most important scientific contributions to the research community to be found in Publications [**I**]-[**XII**] are summarized as follows :

1. Different threshold compensation methods are suggested for RF-to-DC conversion [**I**]-[**V**].

2. Two different simple temperature compensation circuits are proposed which, when combined with the Resistor Less Beta Multiplier (RBM) circuit, generate the reference voltages [**VI**]-[**VII**].

3. A simple circuit arrangement is proposed to improve the temperature coefficient of the conventional RBM current reference circuit [**VIII**].

4. The utility of the principle of the reversal of the temperature behavior with the supply voltage is demonstrated by the measurement for generating the reference frequency [**XI**].

5. Architectures for temperature sensors are proposed which generate a Proportional to Absolute Temperature (PTAT) and Complementary To Absolute Temperature (CTAT) temperature equivalent signal. These sensors are capable of operating at ultra low power and can sense temperature with moderate inaccuracy [**X**]-[**XII**].

2. Radio Frequency Energy Harvesting

2.1 Overview

Radio frequency (RF) energy transfer and harvesting techniques have recently become alternative methods for powering the next generation of electronic devices because they offer the possibility of transferring energy wirelessly. A rectifier (or RF-to-DC converter) is an important component present between the received RF signal and the system. It converts the RF energy to the DC energy and the system uses the rectified DC to perform various functions. A typical block diagram of an RF energy harvesting node/system is shown in Fig. 1.1.

This topology is widely used in wireless sensor networks [23–27], Radio Frequency Identification (RFID) [28–30] and implementation designed for biomedical instrumentation [31–33].

The power flow in the node (Fig. 1.1) is from the energy-harvesting unit to the processing unit. Thus, the energy-harvesting unit should deliver high performance to maintain high Quality of Service (QoS) from the node.

2.2 Performance affecting design parameters

The performance of an energy-harvesting unit depends on the conversion efficiencies of the RF-to-DC converter. Therefore, it is necessary to keep account of the performance affecting parameters to avoid the degradation of the power conversion chain. In this section, various parameters have been discussed, which inherently affects the performance of any rectifier. These discussions include all necessary design guidelines for improving the performance of the RF-to-DC converter.

2.2.1 CMOS implementation

In the CMOS technology, a diode-connected Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is generally used as a diode [34]. Thus, both N-type Metal Oxide Semiconductor (NMOS) and P-type Metal Oxide Semiconductor (PMOS) transistors are useful as a rectifying element in an RF-to-DC converter design. It is well known that a CMOS implementation is done in four general forms: (i) n-well, (ii) p-well, (iii) twin-well and (iv) triple-well [35]. In a modern CMOS implementation, either twin-well or triple-well implementations are the preferred choices [36].

In a CMOS process with a twin-well implementation, an NMOS transistor resides directly in the substrate as shown in Fig. 2.1. Hence, the NMOS transistor will introduce high substrate noise compared with the PMOS transistor, which is sitting inside a well. For this reason, a diode-connected PMOS transistor is the preferred choice for implementing the rectifier. Though an NMOS transistor has some inherent performance advantages over a PMOS transistor; the electron mobility is approximately twice that of hole mobility hence an n-channel device will have one-half the ON-resistance (or impedance) of an equivalent p-channel device with the same geometry under the same operating conditions. Therefore, it makes an NMOS transistor faster than a PMOS transistor [37].

Referring to Fig. 2.1 it can be noticed that the PMOS transistor has more parasitic Bipolar Junction Transistor (BJT)s in comparison to the NMOS transistor in a twin-well implementation. Generally, the lateral BJTs ($\mathrm{NPN}_{\mathrm{lateral}}$ and $\mathrm{PNP}_{\mathrm{lateral}}$) do not introduce any undesirable parasitic effects rather, they contribute to the input current and their contributions depend on the body biasing arrangement [38]. However, the presence of vertical BJTs ($\mathrm{PNP}_{\mathrm{vertical}}$) are the main problem during the working of a rectifier. This is because it lead towards an increase in the leakage current due to the periodic forward biasing of the base emitter junctions.

To estimate the loss that occurs in the current because of $\mathrm{PNP}_{\mathrm{vertical}}$ the following guideline is suggested.

Consider a diode-connected PMOS transistor shown in Fig. 2.2 where V_{in} is the input RF signal applied at the source terminal, and V_{out} is the rectified DC output voltage obtained at the drain terminal. It can be seen in Fig. 2.2 that the body terminal is tied to the source terminal; hence the loss in drain current (I_d) will be caused due to $\mathrm{PNP}^{\mathrm{B}}_{\mathrm{vertical}}$. Thus, the

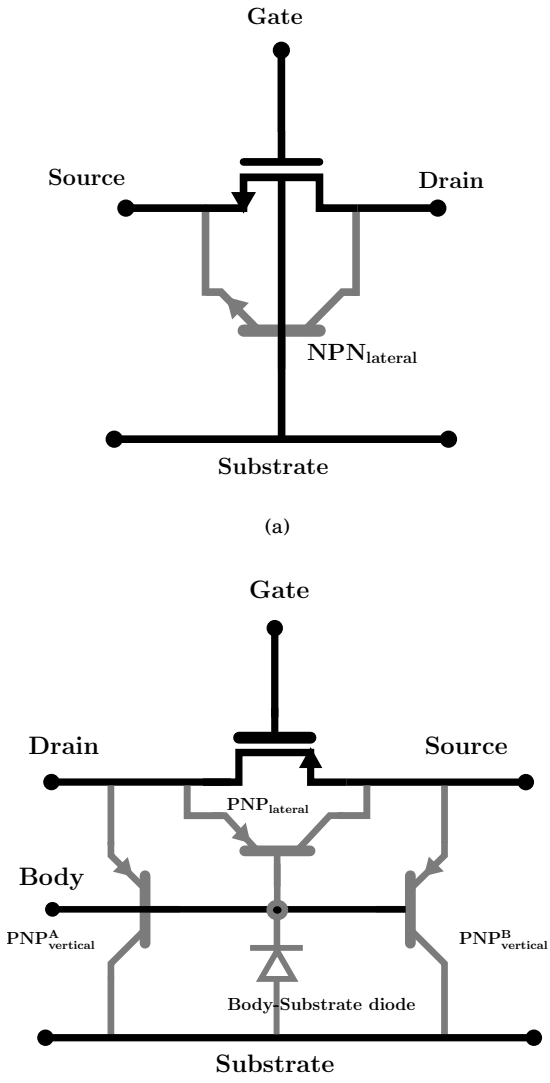


Figure 2.1. (a) NMOS and (b) PMOS transistors with parasitics BJTs in twin well process implementation.

collector current (I_c) flowing through it is given by [39]:

$$I_c = I_S \cdot \exp\left(\frac{V_{BE}}{V_T}\right) = I_S \cdot \exp\left(\frac{V_{in} - V_{out}}{V_T}\right) \tag{2.1}$$

where I_S is the reverse saturation current in the range of 10^{-15} amperes to 10^{-12} amperes, V_{BE} is the base-emitter voltage and V_T is the thermal voltage which is $\approxeq$ 26 mV at 300 °K.

Similarly, the drain current (I_d) [35],[40] flowing through the diode-

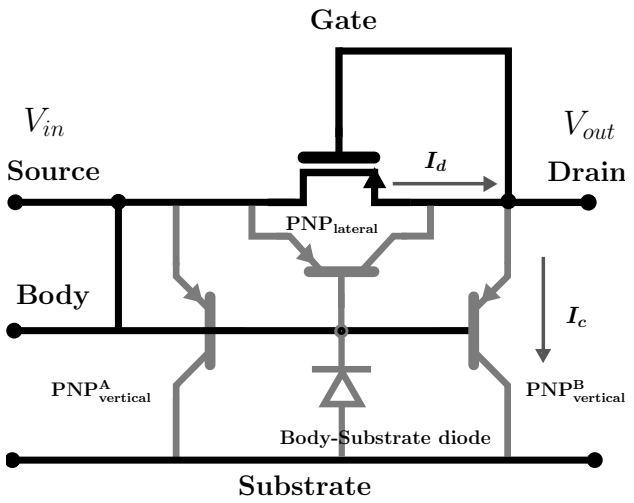


Figure 2.2. Diode-connected PMOS transistor with parasitic BJTs.

connected PMOS transistor is:

$$I_d = I_{d0} \cdot \exp\left(\frac{V_{sg}}{\eta V_T}\right) = I_{d0} \cdot \exp\left(\frac{V_{in} - V_{out}}{\eta V_T}\right) \tag{2.2}$$

where I_{d0} is the saturation current, V_{sg} is the source-gate voltage and η is the subthreshold slope. Dividing (2.2) with (2.1) will result in:

$$\frac{I_d}{I_c} = \frac{I_{d0}}{I_S} \tag{2.3}$$

It can be noticed that equation (2.3) provides a dependency between circuit controlled currents (I_d, I_c) and device dependent currents (I_{d0}, I_s). Hence, to reduce the loss in drain current (I_d), the ratio (2.3) should be maximized.

In the literature I_S and I_{d0} [35], [40] are defined as:

$$I_S = A_E \cdot J_S \tag{2.4}$$

and

$$I_{d0} = A_M \cdot 2\eta\mu_p C_{OX} V_T^2 \exp\left(\frac{V_{thp}}{\eta V_T}\right) = A_M \cdot I_M \tag{2.5}$$

where A_E is the junction area, J_E is the current density, μ_p is the mobility, C_{OX} is the oxide capacitance value, V_{thp} is the threshold voltage, and A_M is the area of the MOSFET.

By substituting (2.4), (2.5) in (2.3), the ratio between drain current (I_d) and collector current (I_c) will be expressed in terms of the geometry and process parameters of the transistor.

$$\frac{I_d}{I_c} = \underbrace{\frac{I_M}{J_S}}_{Process} \cdot \underbrace{\frac{A_M}{A_E}}_{Geometry} \tag{2.6}$$

Hence, to maximize (2.6) a transistor layout will be an important design parameter for a designer.

Considering a PMOS transistor with a aspect ratio of $n \cdot W/L$ where n is the number of fingers, W and L is the width and length of the basic cell. The junction area (A_E) and the MOSFET area (A_M) can be easily

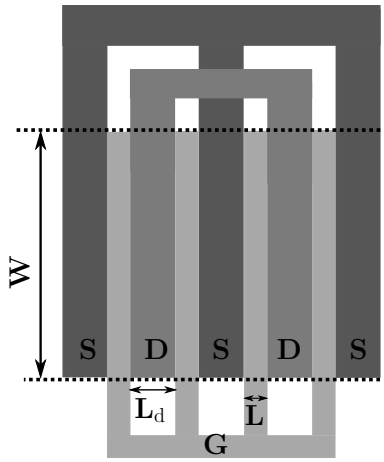


Figure 2.3. Example of a layout with number of fingers (n) equal to 4.

calculated from a layout shown in Fig. 2.3 as:

$$A_E = n \cdot W \cdot L_d \tag{2.7}$$
$$A_M = n \cdot \frac{W}{L}$$

By substituting (2.7) in (2.6) will result in:

$$\frac{I_d}{I_c} = \frac{I_M}{J_S} \cdot \frac{1}{L \cdot L_d} \tag{2.8}$$

It can be concluded from equation (2.8) that a selection of smaller gate and diffusion lengths will reduce leakage due to parasitic vertical BJT.

2.2.2 Transistor sizing and operating frequency

It has been shown in equation (2.8) that the dimension of the transistor is an important factor to improve its performance. This performance is generally measured in terms of the conversion efficiency. Typically, in a rectifier circuit a MOSFET is either used as a switch or implemented in diode-connected configuration. In these implementations the ON-resistance R_{ON} of MOSFET is an important design parameter. The R_{ON} of a PMOS

transistor is given by:

$$R_{ON} = \frac{1}{\mu_p C_{OX} \left(\frac{W}{L}\right) (V_{sg} - |V_{thp}|)} \tag{2.9}$$

where V_{sg} is the source-gate voltage.
It can be observed in (2.9) that the aspect ratio (W/L) is the primary design parameter. The increasing aspect ratio will lead to reduced ON-resistance and thus, will produce a larger saturation current. However, it will also increase the reverse current and parasitic capacitances. A higher reverse current will cause a reduction in the conversion efficiency of the rectifier [34]; while the presence of a large parasitic capacitance will proportionately result in lower bandwidth [41].

To further explain the impact of transistor sizes, the transient simulations have been performed on a diode-connected PMOS transistor (Fig. 2.2). These results are obtained by using the RF signal of peak amplitude 0.5 V with different RFID frequencies (f_{RF}) for a resistive-capacitive load of value 30 kΩ || 5 pF. The simulations are performed using a standard 0.18 μm CMOS technology by using the Spectre simulator in the Cadence environment. The performance of the rectifier is evaluated in terms of Voltage Conversion Efficiency (VCE) and Power Conversion Efficiency (PCE).

The VCE parameter is defined as:

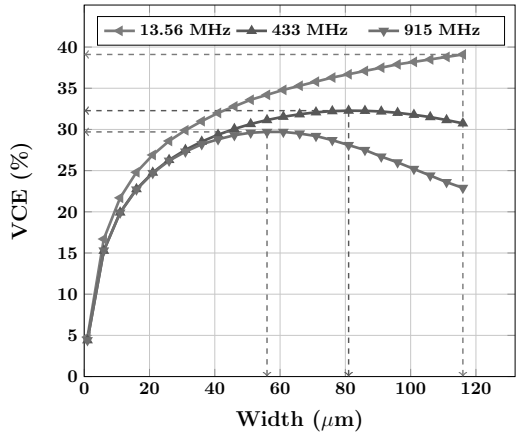
$$VCE(\%) = 100 \cdot \left(\frac{V_{out}}{V_{out_{ideal}}}\right) \tag{2.10}$$

where V_{out} is the rectified output DC voltage and $V_{out_{ideal}}$ is its ideal value.
The PCE parameter is given by:

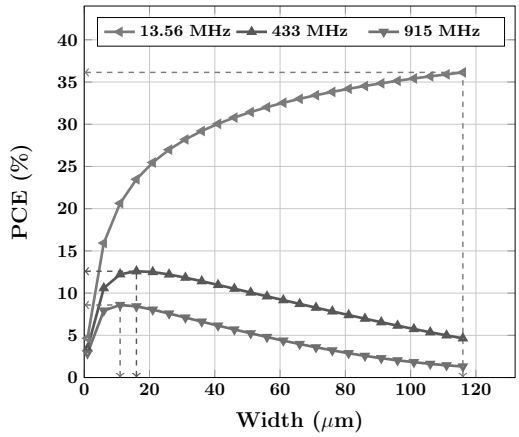
$$PCE(\%) = 100 \cdot \left(\frac{P_{out}}{P_{in}}\right) = 100 \cdot \left(\frac{R_{in}}{R_L}\right) \cdot \left(\frac{V_{out}}{V_{in}}\right)^2 \tag{2.11}$$

where P_{out} is the output power across resistive load and P_{in} is the input RF power to the rectifier, R_{in} is the input resistance value of the rectifier, R_L is the load resistance value and V_{in} is the peak input RF voltage amplitude.
The values of VCE (%) and PCE (%) parameters obtained after the transient simulations are shown in Fig. 2.4.
The following conclusions can be drawn from Fig. 2.4:

1. The curves exhibit dependence over the transistor width. At low input RF frequency (13.56 MHz) the variation follows higher degree polynomial. But, with an increase in input RF frequency the functional dependency converges towards a parabolic nature.



(a)



(b)

Figure 2.4. Simulation results of (a) VCE and (b) PCE with varying transistor width at different input RF frequencies for minimum length transistor.

2. It is possible to comment that for lower input RF frequency (<13.56 MHz) values, the power conversion efficiency will approach towards the ideal value of 40.6%.

3. The conversion efficiencies have been reduced with an increase in input signal frequency and transistor size. This phenomenon is due to an increase in reverse current and higher parasitic capacitances.

4. One of the most important observations is the presence of the maxima of VCE and PCE curves at different values of transistor width. This behavior will introduce a trade-off for the designer between the selection of either maximum PCE or maximum VCE in a rectifier implementation.

2.2.3 Sizing of load, fly capacitors and number of stages

In practice, a single-stage rectifier is insufficient to produce an output voltage ($\geq 2V_{th}$) value required to drive any typical CMOS circuit arrangement from a received small signal amplitude ($\lessapprox V_{th}$).

Hence, to obtain a higher voltage level a cascade arrangement is made by using a series of rectifiers. This stacked configuration, which is often known as the Voltage Multiplier (VM) circuit, is shown in Fig. 2.5.

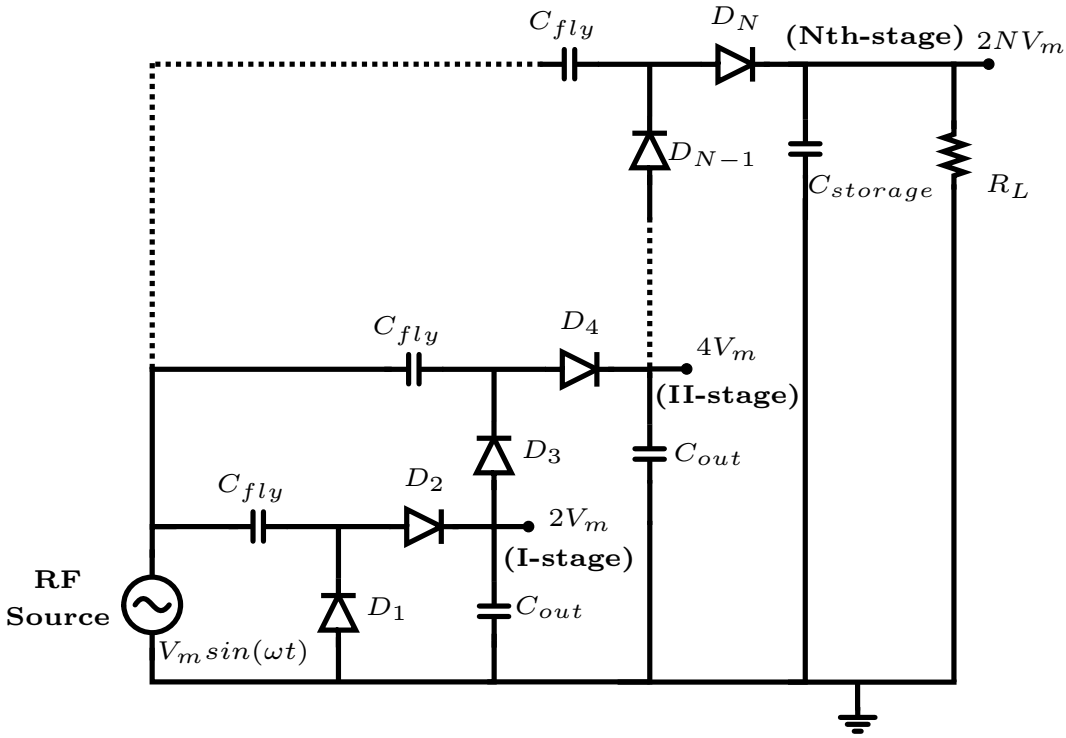


Figure 2.5. Voltage multiplier circuit.

It can be seen that, the arrangement is powered up by using an RF source of peak amplitude value V_m. Each stage of the voltage multiplier is a voltage doubler. Thus, the first stage (I-stage) is generating the output DC voltage equal to twice the peak RF amplitude value ($2V_m$). This progression will continue theoretically with the increase in the number of stages (N); thus, the maximum output DC voltage value of $2NV_m$ will be obtained after the Nth stage. Generally, diodes ($D_1..D_N$) in this architecture are implemented by using the Schottky diode [42], [43–46], or a diode-connected MOSFET [47–52]

It can be observed in Fig. 2.5 that the schematic is constituted by the three circuit components: (i) the load capacitor per stage (C_{out}), (ii) the fly capacitor (C_{fly}), and (iii) the diode (D). The criteria for the sizing of the diode was discussed in the previous subsection. The following subsections present the design considerations for load capacitor per stage (C_{out}), fly capacitor C_{fly} and the number of stages (N) used in the VM circuit implementation.

2.2.3.1 The value of load capacitor / stage

The value of the load capacitance per stage (C_{out}) is a function of the permissible peak-to-peak ripple voltage (ΔV_{ripple}) amplitude, which is given as [53]:

$$\Delta V_{ripple} = \frac{I_{load}}{C_{out}\ f_{RF}} \tag{2.12}$$

where I_{load} is the target load current and f_{RF} is the received RF frequency. It can be seen in (2.12) that the increase in C_{out} will result in less ripple voltage from the load current droop.

2.2.3.2 The value of fly capacitor

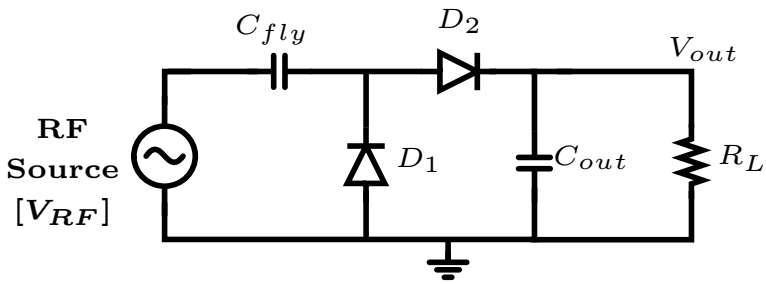


Figure 2.6. Single-stage rectifier.

A schematic of the single-stage rectifier is shown in Fig. 2.6, which is a half-wave voltage doubler (I-stage, Fig. 2.5). In the figure, $D1$ and $D2$ are the diode-connected MOSFET, C_{fly} and C_{out} are the fly and output capacitors respectively, R_L is the resistive load and an RF source $V_{RF} = V_m\ sin(\omega t)$ is used.

It should be noted that the analysis has been done by considering ideal components in the schematics. When the negative half cycle of the RF sinusoidal input waveform will appear, the diode D_1 will become forward biased. Thus, the fly capacitor C_{fly} will enter into charging phase. As a result a DC voltage V_{DC} will appear across it (Fig. 2.7(a)). Ideally, this

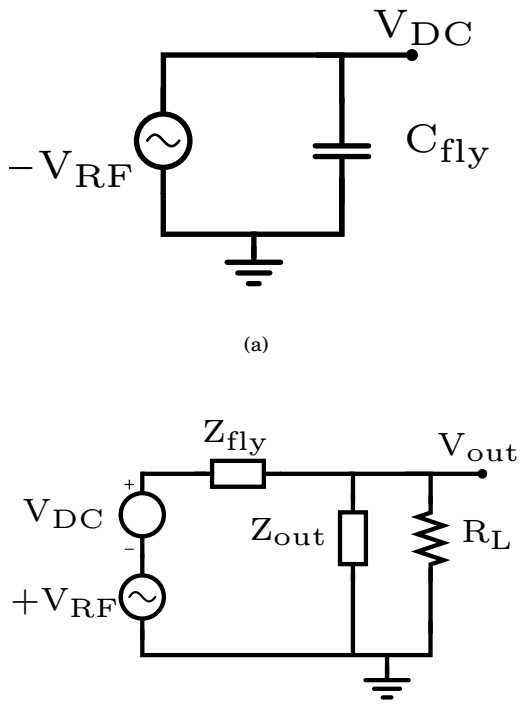


Figure 2.7. (a) Charging phase and (b) Discharging phase of single-stage rectifier.

value is equal to the peak value of the input RF signal V_m. Since there is no path for capacitor C_{fly} to discharge into, it remains fully charged.

During the positive half cycle, the diode D_1 is reverse biased blocking the discharging of C_{fly}. The voltage V_{DC} which was developed across C_{fly} will appear in series with the voltage supply and hence provide a DC shift to the input RF signal. Meanwhile, the diode D_2 will become forward biased and start charging up the capacitor C_{out}. As a result, a voltage V_{out} will appear across the capacitor C_{out} which will ideally equal to twice the peak voltage value (V_m) of the input signal. The equivalent circuit for this phase is shown in Fig. 2.7(b).

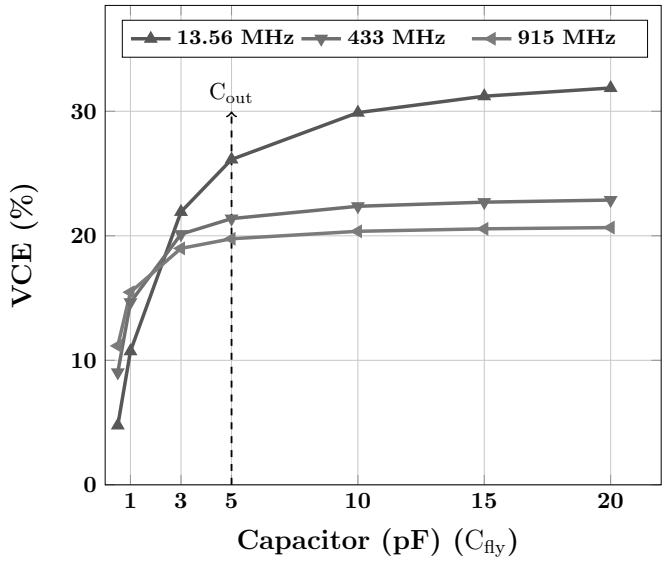
Referring to Fig. 2.7(b), consider a voltage source of value ($V_{RF} + V_{DC}$) with a source impedance of value Z_{fly} connected to the load impedance of value $Z_{out}||R_L$.

According to classical power transfer theorem:

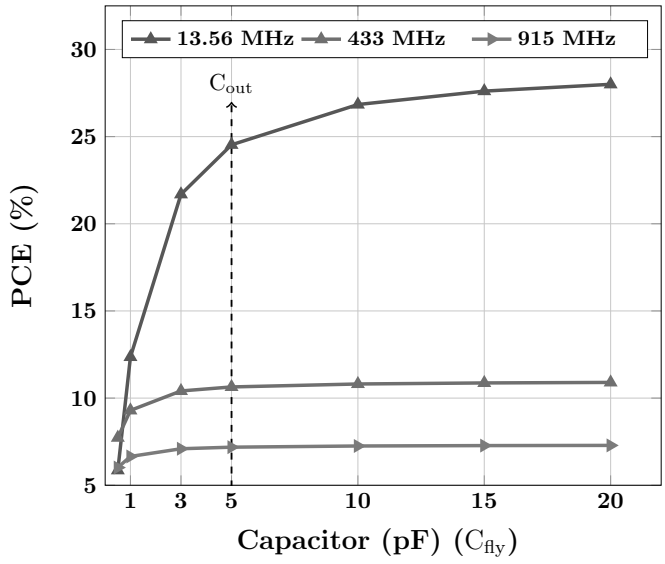
$$Z_{fly} = Z_{out}||R_L \implies C_{fly} = \frac{1}{\omega R_L} + C_{out} \tag{2.13}$$

It can be observed from 2.13 that the $C_{fly} > C_{out}$. Similarly, higher load resistor values (*i.e.* $R_L \to \infty$) will result in $C_{fly} = C_{out}$. Hence, increasing C_{out} will result in a large C_{fly} and thus, unnecessarily increases both circuit size and input capacitance.

Fig. 2.8 shows the transient simulation results of maximum VCE and maximum PCE approaches for a single-stage of the VM circuit (Fig. 2.6).



(a)



(b)

Figure 2.8. Simulation results of (a) VCE and (b) PCE with varying coupling capacitor size at different input RF frequencies.

The size of a diode-connected MOSFETs (D_1 and D_2) is selected by using the performance plots shown in Fig. 2.4. The load capacitor (C_{out}) value is selected as 5 pF and the current requirement has been emulated in terms of a load resistor (R_L) of value 30 KΩ. The RF signal of peak amplitude 0.5 V is used in transient simulations. Simulation results verify equation (2.13) that the fly capacitor C_{fly} should be equal to or greater than the load capacitor per stage C_{out} to achieve high conversion efficiency.

2.2.3.3 Number of stages

Theoretically with any increase in the number of stages (N), the V_{out} to V_{in} ratio will also increase (Fig. 2.5). In practical implementations, however an increase in the number of stages, increases the losses and hence the output DC voltage V_{out} decreases.

Fig. 2.9 shows the comparison between the ideal output DC voltage with the simulated output DC voltage obtained from the voltage multiplier with an increasing number of stages (N). The simulation environment parameters used to obtain the results are listed in Table. 2.1. It can

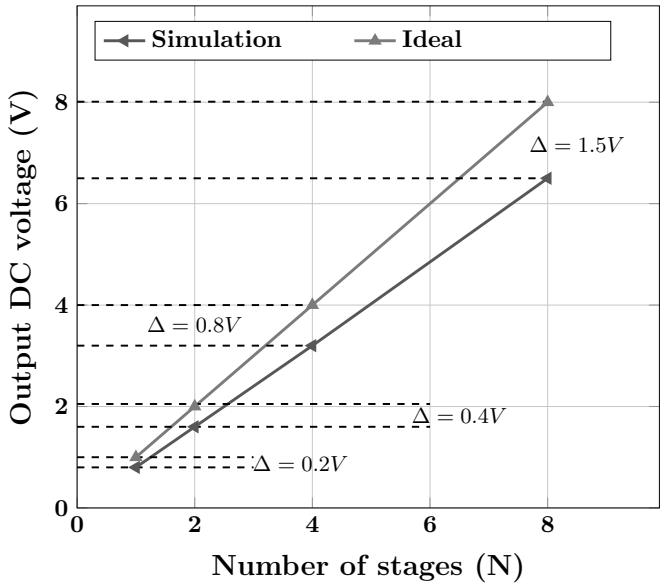


Figure 2.9. Simulated output DC voltage with increasing number of stages (N).

be observed from Fig. 2.9 that with an increase in the number of stages, the losses in the voltage multiplier increase correspondingly. Referring to Fig. 2.9 a empirical formula to estimate the output DC voltage can be written as:

$$V_{estimate} = 2NV_m - \chi * N \tag{2.14}$$

Table 2.1. Simulation environment used to evaluate voltage multiplier.

S.No.	**Parameter**	**Value**
1	Architecture	Fig. 2.5
2	Peak RF amplitude	500 mV
3	RF frequency	433 MHz
4	Number of Stages	1,2,4,8
5	Simulation Type	Harmonic Balance with 20 Harmonics
6	Transistor	PMOS
7	Size	4*10 μm/0.18 μm
8	Fly capacitor C_{fly} size	5 pF
9	Capacitor/output stage C_{out} size	5 pF
10	Load	Capacitive only

where N is the number of stages, V_m is the peak input RF amplitude and χ is the voltage loss (0.2 V) in a single-stage.

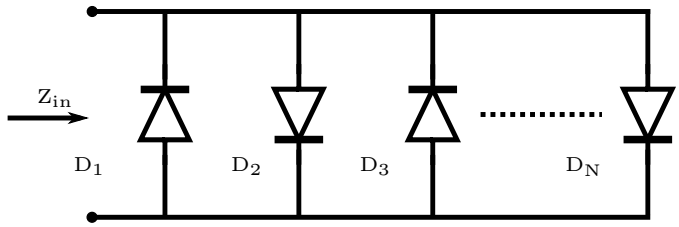


Figure 2.10. AC equivalent schematic of N-stage voltage multiplier circuit.

When a voltage multiplier is employed with a resistive load, then its performance becomes affected by both the number of stages (N) and the resistive load value (R_L). To understand this phenomenon, consider the AC equivalent circuit of the voltage multiplier of Fig. 2.5 as drawn in Fig. 2.10.

In practice, the input power (P_{in}) is the sum of the output power (P_{out}) and the power lost in each branch (P_{loss}). In this case (Fig. 2.5), only half of the diodes ($\frac{N}{2}$) will act during the conversion. Therefore:

$$P_{in} = P_{out} + \frac{N}{2} \cdot P_{loss} \tag{2.15}$$

where P_{in} is given by:

$$P_{in} = \frac{V_m^2}{2R_{in}} \tag{2.16}$$

and R_{in} is the input resistance of the voltage multiplier. By using (2.16) in (2.15) will result in:

$$R_{in} = \frac{V_m^2}{2\left(P_{out} + \frac{N}{2}P_{loss}\right)} \tag{2.17}$$

Considering that the diodes are lossless, then $P_{out} = P_{in}$ and V_{out} will be equal to $2NV_m$ hence:

$$\frac{V_m^2}{2R_{in}} = \frac{V_{out}^2}{R_{out}} \implies R_{in} = \frac{R_L}{2N^2} \tag{2.18}$$

The equation (2.18) shows that with an increase in the number of stages (N), the input resistance (R_{in}) of the rectifier will decrease for a given value of load resistance (R_L). The simulated values of R_{in} with N are shown in Fig. 2.11. The simulation environment parameters used are listed in Table. 2.1 with the exception of the load condition. Here a resistive load of value 10 KΩ was selected to perform these simulations.

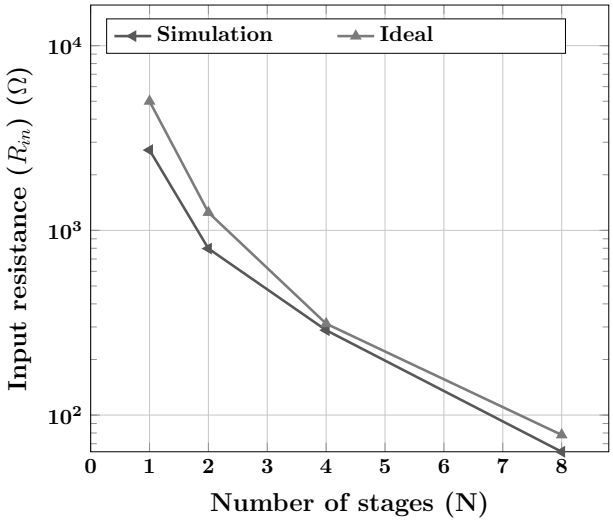


Figure 2.11. Variation of input resistance with increasing number of stages (N).

It can be verified from Fig. 2.11 that the simulated values of R_{in} follows equation (2.18). Thus, it can be concluded that the trend in the reduction of the input resistance with the number of stages will increase the input power (2.16), which will inherently decrease the power conversion efficiency (2.11). The simulation-based result obtained for the power conversion efficiency by using a resistive load of 10 KΩ is shown in Fig. 2.12 which verifies this conclusion.

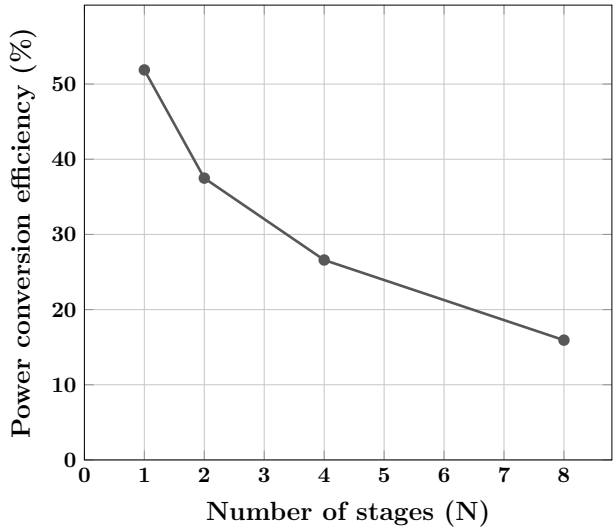


Figure 2.12. Variation of power conversion efficiency with increasing number of stages (N).

2.2.4 Matching network

Ideally, the matching network (Fig.1.1.) is a lossless network placed between the RF source (antenna) and the load (rectifier). The purpose of a matching network is to provide a narrow-band impedance and voltage transformation between the two ports. It is one of the contributing factors to the overall efficiency of an energy harvesting unit as shown in equation (2.19):

$$\eta_{ehu} = \eta_{antenna} \cdot \eta_{match} \cdot \eta_{rect} \tag{2.19}$$

where $\eta_{antenna}$ is the efficiency of the antenna, η_{match} is the efficiency of the matching network, and η_{rect} is the efficiency of the rectifier. In practice, the signal strength of a received RF signal is small, therefore along with the power-matching, a voltage gain-boosting is also mandatory for the matching network [45], [54], [55].

Fig. 2.13 shows a simplified schematic of an OFF-chip power-matching and gain-boosting network used in this work. The component models for the capacitor and inductor are selected from [56] and [57] respectively. The I/O pad and the rectifier are modeled as parallel RC circuits ($R_{pad}||C_{pad}$) and ($R_{rect}||C_{rect}$) respectively. In the following analysis, for simplicity, it has been considered that the series elements contribute in source impedance (Z_{source}) while parallel elements form the input impedance (Z_{in}). Thus, in the schematic the source impedance (Z_s) is

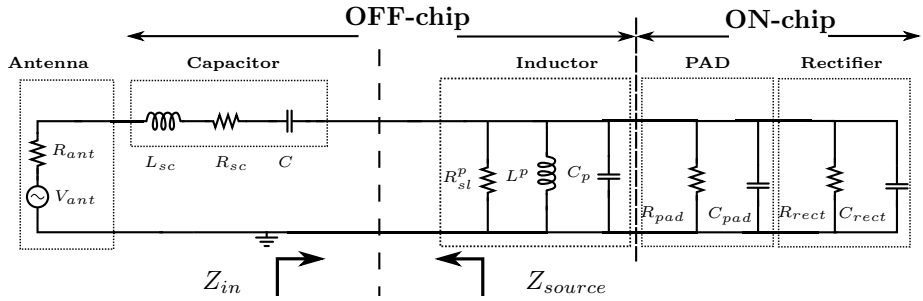


Figure 2.13. Matching network.

given by:

$$Z_s = (R_{ant} + R_{sc}) + j\left(\omega L_{sc} - \frac{1}{\omega C}\right) \tag{2.20}$$

where R_{ant} is the antenna resistance, L_{sc} and R_{sc} are the residual inductance and the resistance in the lead wires and electrodes, and C is an actual capacitor. Rewriting (2.20) as:

$$Y_s = \frac{1}{(R_{ant} + R_{sc})}\left(\frac{1 - jQ_c\left(\left[\frac{\omega}{\omega_{srfc}}\right]^2 - 1\right)}{1 + Q_c^2\left[\frac{\omega}{\omega_{srfc}}\right]^2}\right) \tag{2.21}$$

where, ω_{srfc} is the self-resonating frequency of capacitor (C) with parasitic inductance L_{sc} [58] and [59], Q_c is the quality factor of capacitor C, and it is defined as $\frac{1}{\omega C(R_{ant}+R_{sc})}$.

Similarly, input admittance (Y_{in}) is given by:

$$Y_{in} = \frac{1}{R_{eq}} + j\left(\omega C_{eq} - \frac{1}{\omega L_p}\right) \tag{2.22}$$

In (2.22), R_{eq} and C_{eq} are the total equivalent shunt resistance and capacitance respectively, given as follows:

$$\begin{aligned} R_{eq} &= R_{sl}^{p} || R_{pad} || R_{rect} \\ C_{eq} &= C_p + C_{pad} + C_{rect} \end{aligned} \tag{2.23}$$

Solving (2.22) will result in:

$$Y_{in} = \frac{1}{R_{eq}} + j\left(\frac{\left[\frac{\omega}{\omega_{srfl}}\right]^2 - 1}{\omega L_p}\right) \tag{2.24}$$

where ω_{srfl} is the self-resonating frequency of an inductor (L_p) with a shunt capacitance (C_{eq}).

It is known from fundamental theory on matching networks that to transfer maximum power the following condition holds:

$$Y_{in} = Y_s^* \tag{2.25}$$

Hence, by comparing the real parts it will result in:

$$\frac{R_{eq}}{R_{ant} + R_{sc}} = 1 + \left(1 - \left[\frac{\omega}{\omega_{srfc}}\right]^2\right) Q_c^2 \tag{2.26}$$

Assuming $\omega_{srfc} >> \omega$, than (2.26) is simplified to:

$$\frac{R_{eq}}{R_{ant} + R_{sc}} = 1 + Q_c^2 \tag{2.27}$$

Similarly, by comparing the imaginary parts will result in:

$$\frac{\psi_c}{\omega L_p} = \frac{\psi_l}{\omega C (R_{ant} + R_{sc})^2} \cdot \left(\frac{1}{1 + (\psi_l Q_c)^2}\right) \tag{2.28}$$

where

$$\psi_c = \left(1 - \left[\frac{\omega}{\omega_{srfc}}\right]^2\right)$$
$$\psi_l = \left(\left[\frac{\omega}{\omega_{srfl}}\right]^2 - 1\right)$$

Typically $\psi_l Q_c >>1$ hence (2.28) can be written as:

$$\omega^2 = \omega_{LC}^2 \cdot \psi_l \cdot \psi_c \tag{2.29}$$

where

$$\omega_{LC} = \frac{1}{\sqrt{L_p C}}$$

Assuming that $\omega_{srfc},\ \omega_{srfl} >> \omega$ then (2.29) is simplified to:

$$\omega = \omega_{LC} \tag{2.30}$$

The power distribution equivalent circuit of Fig. 2.13 is shown in Fig. 2.14.

Thus, the power conversion efficiency η will be:

$$\eta(\%) = 100 \cdot \frac{P_{rect}}{P_{in}} = 100 \cdot \left(\frac{R_{ant}}{R_{rect}}\right) \left(\frac{R_{eq}}{R_{ant} + R_{sc} + R_{eq}}\right)^2 \tag{2.31}$$

where P_{in} is the power obtained from the RF source and P_{rect} is the power delivered to the rectifier. It is evident from (2.31) that the equivalent resistance R_{eq} (2.21) influences the power efficiency of the system. As a result, the efficiency is always less than 100%.

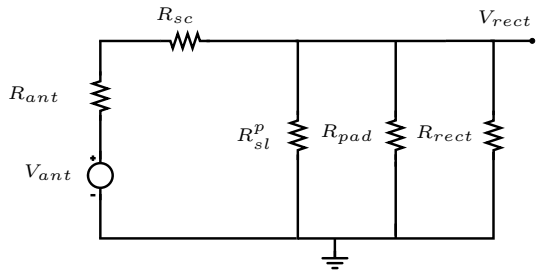


Figure 2.14. Power distribution network.

It has been pointed out earlier that a voltage gain is also demanded from the matching network. Therefore consider a matching network with a voltage gain of A_v: the voltage appearing across the rectifier will be $V_{rect} = A_v V_{ant}$. Thus, the power delivered to the matching network will become:

$$P_L = \frac{V_{rect}^2}{R_{sc} + R_{eq}} = \frac{(A_v V_{ant})^2}{R_{sc} + R_{eq}} \tag{2.32}$$

It is well known that if the matching is ideal, then the maximum power delivered is given by:

$$P_{eq}^{max} = \frac{V_{ant}^2}{4R_{ant}} \tag{2.33}$$

By equating (2.32) and (2.33) it is obtained that:

$$A_v = \frac{1}{2}\sqrt{\left(\frac{R_{sc} + R_{eq}}{R_{ant}}\right)} \tag{2.34}$$

The conclusions from the above analyses are as follows:

1. The self-resonant frequency of the discrete components must be greater than the matching frequency.

2. The voltage gain boosting is proportional to the quality factor of the discrete components from (2.27) and (2.34).

3. The I/O pads also affect the power conversion and gain boosting ability of the matching network.

4. Estimation of the parasitic resistances is necessary before designing the rectifier to make R_{rect} dominant on parasitic resistances (2.21).

2.2.5 Figure of merits

The performance evaluation of the rectifier is done by using the following figure of merits.

2.2.5.1 Voltage conversion efficiency

The RF-to-DC converter (or rectifier) is an AC/DC converter and the level of output DC voltage will determine the capability to drive the load such as a transmitter or a receiver. The voltage conversion efficiency (VCE) is measured to determine the level of output DC voltage for a given peak RF amplitude. The VCE is defined as:

$$VCE(\%) = 100 \cdot \frac{V_{dc}}{V_{dc\ ideal}} = \frac{V_{dc}}{A_v \cdot 2N \cdot V_{in}} \tag{2.35}$$

where V_{dc} is the output DC voltage from the rectifier, $V_{dc_{ideal}}$ is the ideal DC voltage from the rectifier, N is the number of stages of the voltage multiplier, V_{in} is the peak signal amplitude of the input RF signal and A_v is the voltage gain of the gain-boosting matching network.

2.2.5.2 Power Conversion Efficiency

The power conversion efficiency (PCE) is the ratio of the DC output power (P_{dc}) to the power delivered to the rectifier (P_{in}) given as follows:

$$PCE(\%) = 100 \cdot \frac{P_{dc}}{P_{in}} = 100 \cdot \left(\frac{V_{DC}^2}{R_L}\right) \cdot \left(\frac{1}{P_{source}(1 - |\Gamma|^2)}\right) \tag{2.36}$$

where V_{DC} is the rectified output DC voltage across the load resistor (R_L), P_{in} is the actual power delivered to the rectifier, which is calculated in terms of P_{source} and Γ. In (2.36) P_{source} is the power available from the RF generator and $|\Gamma|$ is the reflection coefficient which is defined as,

$$|\Gamma|^2 = \begin{cases} |S_{11}|^2 & \text{for a single input rectifier} \\ |S_{dd11}|^2 + |S_{cd11}|^2 & \text{for a differential input rectifier} \end{cases} \tag{2.37}$$

Here S_{11} is the single-ended reflection coefficient with S_{dd11} and S_{cd11} being the mixed mode differential-to-differential and differential-to-common mode reflection coefficients respectively, which are measured by using the Voltage Network Analyzer (VNA).

2.3 Proposed RF-to-DC converters

In RF energy harvesting applications the industrial, scientific and medical (ISM) bands at 433 MHz and 902- 928 MHz are most conveniently

used due to lower path loss with respect to the higher RF bands. Additionally, in this frequency range, a high 4W Effective Isotropic Radiated Power (EIRP) is sanctioned by the regulatory bodies [60–62] thus, allowing long node distance from the power transmitting module.

It is well known from the standard Friis free-space propagation equation [63] that the power available to the antenna is inversely proportional to d^2 where d is the link distance. Thus, the input power delivered to the RF energy harvesting module will be low in order to maximize the link length. As a result the micro-watt (μW) power budget is estimated for remote RF-powered devices.

The minimum incident power level that is required by a rectifier is a function of the threshold voltage of rectifying devices, *i.e.* diodes and transistors. In the published literature, two methods have been adopted to decrease the threshold voltage. In the first method, devices like a Schottky diode [64], Zero-V_{th} diode [65] or Native transistors [51] are used. It is well mentioned in the literature that these devices require additional fabrication steps. Hence, they do not provide cost-effective mass production. As a solution to this issue, a circuit-based method is a preferred choice. In this method, rectifiers are implemented by using standard CMOS transistors. Later, additional circuit arrangements are used to reduce the threshold voltage of these transistors [66], [67], [68].

In this research, three approaches are proposed to improve the performance of the rectifier. The aim of these methods is to reduce the threshold voltage influence in the rectifier. In the first method, the involvement of the body terminal in designing the rectifier is proposed. While in the second method, the performance improvement of the rectifier was demonstrated by the use of the auxiliary circuits. The proposed third approach was targeted to the designing of voltage multiplier circuits. In this method, a signaling scheme has been proposed to improve the conversion performance of the voltage multiplier circuits.

A brief discussion of the proposed three methods follows here after.

2.3.1 Design based on controlling body voltage

The essential feature for achieving high rectification efficiency in a rectifier is the low threshold voltage (Vth). One obvious solution would be is the use of a Zero-V_{th} [52] MOSFET. Unfortunately, however it suffers from reverse conduction loss. In addition, it will require an additional fabrication cost, which is not cost effective for mass production. In this work,

the aim has been rather to develop the circuit-based methods, which are capable of altering the threshold voltage of the switching transistors of the rectifiers.

In literature, the dependency of the threshold voltage (V_{thn}) with the source-body voltage (V_{SB}) is given in (2.38) for the NMOS transistor [35].

$$V_{thn} = V_{thn0} + \gamma \cdot \sqrt{2 \cdot \phi_F + V_{SB}} - \sqrt{2 \cdot \phi_F} \tag{2.38}$$

where, V_{thn0} is the zero-bias threshold voltage, γ is the body-effect coefficient, ϕ_F is the flat-band voltage and V_{SB} is the source-body voltage.

It can be noticed from equation (2.38) that the body-source voltage V_{SB} is the only circuit-based parameter. In order to understand the effect of the body-source voltage, the DC simulations were performed on the circuit arrangement shown in Fig. 2.15. The characterization of the transistor was done by varying the body-source voltage V_{SB} in the range of -1.8 V to 1.8 V. In these simulations, the gate-source voltage V_{GS} and the drain-source voltage V_{DS} were fixed at 900 mV and 1.8 V respectively. The aspect ratio of the NMOS transistor used for the simulation was 20 μm/0.18 μm. The simulated characterization plots for the threshold voltage, the

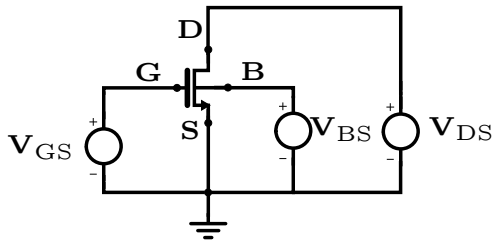
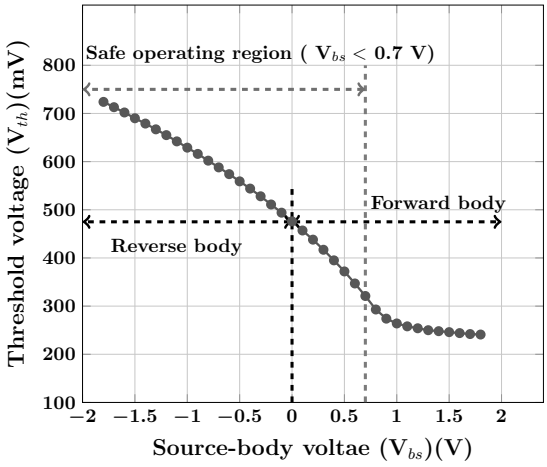
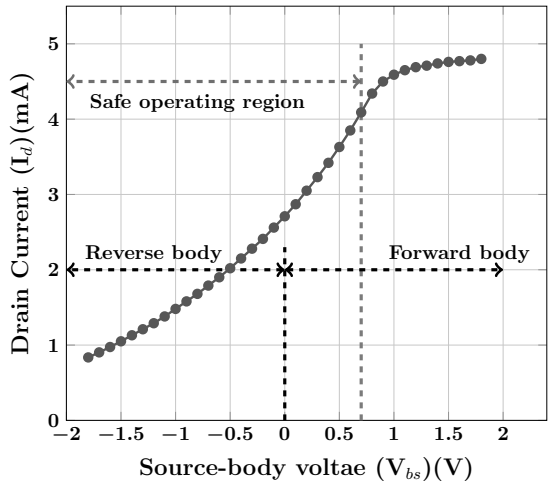


Figure 2.15. Circuit setup used for NMOS transistor characterization.

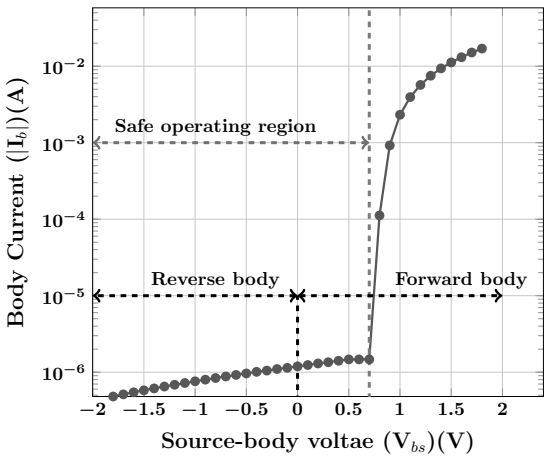
drain and the body currents are shown in Fig. 2.16(a), Fig. 2.16(b) and Fig. 2.16(c) respectively. The plots are divided into two regions depending on the source-body voltage. The region between 1.8 V $\leq V_{SB} <$ 0 V is termed as the 'Reverse body', while the region between 0 V $< V_{SB} \leq$ 1.8 V is termed as the 'Forward body' as shown in Fig.2.16. The V_{SB} = 0 V corresponds to the zero-body biased condition where the threshold voltage of the transistor is equal to V_{thn0} (2.38). Conventionally, $V_{SB} = 0$ V, *i.e.* the body terminal tied to the source terminal is preferred during CMOS-based rectifier circuit implementations [69]. This arrangement enables the threshold voltage value of the switching transistors to be set at V_{thn0}. It is observed from the simulation plots that by increasing the source-body



(a)



(b)



(c)

Figure 2.16. NMOS transistor characterization plots obtained by varying source-body voltage.

voltage the threshold voltage decreases. This variation is approximately $\pm$50% from V_{thn0}, thus it verified the dependence of the threshold voltage (V_{thn0}) on the source-body voltage (V_{SB}) as mentioned in equation (2.38).

This phenomenon, nevertheless, does not progress well for a higher value of V_{SB}. It can be seen in Fig. 2.16 that for the values of $V_{SB} \geq$ 0.7 V, two phenomena occur. First, the variation in the threshold voltage becomes independent of the source-body voltage (Fig. 2.16(a)) and second, the magnitude of the body-current becomes comparable to or greater than the drain current (Fig. 2.16(c) and Fig. 2.16(b)).

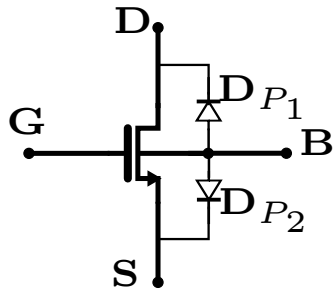


Figure 2.17. NMOS transistor with parasitic diodes.

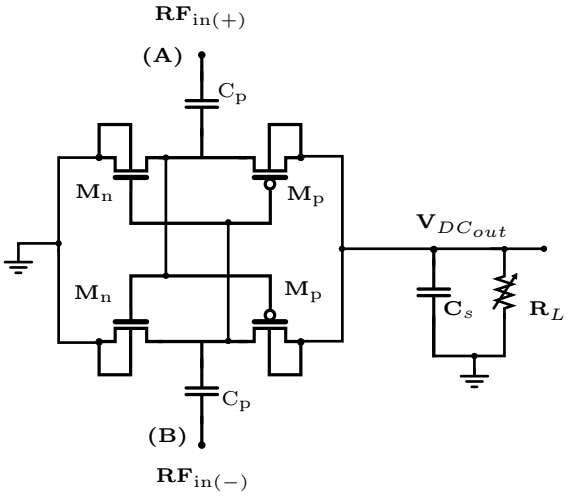
To understand this phenomenon, consider Fig. 2.17 where D_{p1} and D_{p2} are the parasitic diodes associated with the NMOS transistor. The contributions of these parasitic diodes can be estimated depending upon the source-body voltage value. When V_{SB} = 0 V, only the diode D_{p1} and when $V_{SB} <$ 0.7 V and $\neq$ 0 V both the diodes D_{p1} and D_{p2} are in reverse biased configuration. But when $V_{SB} >$ 0.7 V the diodes have become forward biased and as a result higher body current values started flowing. Therefore, the usage of V_{SB} lower than 0.7 V has been recommended in the literature [70].

In this research, the ability of the body-source voltage to reduce the threshold voltage has been exploited in the designing of the rectifier circuit. These methods are categorized as static and dynamic control of the body-source voltage.

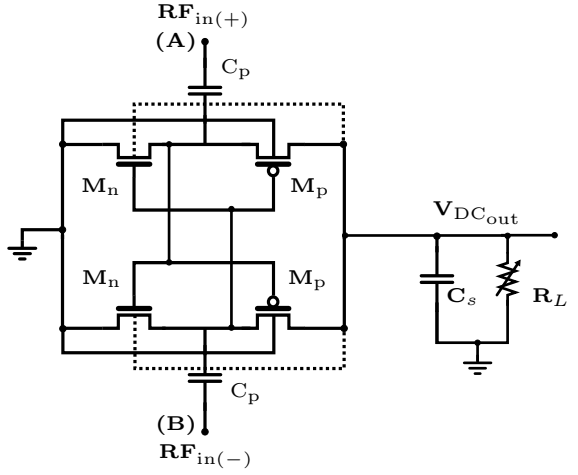
2.3.1.1 Static control of body-source voltage

In this method, a static DC control voltage is applied to the body terminal to pull down the threshold voltage of the MOSFET. This method is widely used in subthreshold-based digital circuit design. Since, the use of body biasing methods in the subthreshold region ensures fast switching with an effectively turning OFF of the devices during an ideal state. One

such method is the Swapped Body Bias (SBB) scheme [71]. This mechanism is also known as Forward Body Bias (FBB). This simple scheme was implemented in the classical high efficiency differential rectifier [72] to obtain static body voltage values. The circuit arrangements for single-stage rectifiers are shown in Fig. 2.18. It can be seen in Fig. 2.18(b) that to implement an SBB arrangement, the body terminal of the NMOS transistor is connected to the source terminal of the PMOS transistor, and vice versa is done for the PMOS transistor.



(a)



(b)

Figure 2.18. (a) Conventional and (b) SBB-based differential rectifier.

The transient simulations were performed for the resistive load (R_L) of values 1 KΩ, 10 KΩ, 100 KΩ and 1 MΩ. The values of the fly capacitor C_p and the storage capacitance C_s were selected as 5 pF and 10 pF respectively. It should be noted that the aspect ratio of the transistors conventional rectifier were optimized for 10 KΩ and later the SBB mechanism was implemented.

Table 2.2. Performance summary and comparison of differential rectifiers.

Single-Stage Architecture									
	Conventional (conv)			**Proposed (sbb)**			**Δ=sbb-conv**		
R_{Load}	**Peak**	**P_{in}**	**Out**	**Peak**	**P_{in}**	**Out**	**Peak**	**Pin**	**Out**
KΩ	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dB)**	**DC (V)**
1	49.79	-3.588	0.47	54.11	-3.67	0.49	4.32	-0.08	0.02
10	68.52	-13.62	0.56	71.83	-15.67	0.44	3.31	-2.05	-0.12
100	55.93	-24.60	0.44	72.26	-27.68	0.35	16.33	-3.08	-0.09
1000	15.50	-30.31	0.38	53.58	-38.24	0.28	38.08	-7.93	-0.10
Three-Stage Architecture									
	Conventional (conv)			**Proposed (sbb)**			**Δ=sbb-conv**		
R_{Load}	**Peak**	**P_{in}**	**Out**	**Peak**	**P_{in}**	**Out**	**Peak**	**Pin**	**Out**
KΩ	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dB)**	**DC (V)**
1	15.02	0.25	0.4	15.18	1.01	0.44	0.16	0.76	0.04
10	62.80	-2.29	1.93	61.91	-4.41	1.50	-0.89	-2.12	-0.43
100	67.07	-15.16	1.43	68.52	-17.45	1.11	1.45	-2.29	-0.32
1000	33.92	-24.60	1.03	32.99	-23.96	1.15	-0.93	0.64	0.12

In this optimizations, the constraint was the maximization of the power conversion efficiency. Hence, the achieved voltage conversion efficiency or the output DC voltage from the proposed architecture is lesser than the conventional architecture (Refer to section.2.2.2). The resultant optimized aspect ratio for PMOS (M_p) and NMOS (M_n) is 20 μm/0.18 μm.
The detailed post-layout simulation results of the power conversion efficiency and the output DC voltage of single-stage and three-stage conven-

tional and proposed rectifiers are shown in Fig. 2.24, Fig. 2.25, Fig. 2.26 and Fig. 2.27 respectively for an input RF frequency of 433 MHz. The performance summary of the conventional and the proposed rectifier is listed in Table. 2.2

It can be observed from Table. 2.2 that the sensitivity of an SBB-based differential rectifier towards a low RF power level has been increased by ≈-2.5 dB. This phenomenon of the increased sensitivity towards low voltage amplitude levels is also reported in [71]. The power conversion efficiency of the proposed rectifier has been considerably increased in a single-stage configuration and is comparable with a conventional differential rectifier in three-stage configuration depending upon the load condition.

2.3.1.2 Dynamic control of body-source voltage

In [73], it was demonstrated experimentally for Silicon-On-Insulator (SOI) that the dynamic control of the threshold voltage is possible by tying the body terminal to the gate terminal, and this arrangement is referred as Dynamic Threshold Metal Oxide Semiconductor (DTMOS).

The DTMOS approach was used in publication [**I**] for designing a diode-connected PMOS transistor using a standard CMOS technology. Measured results show that the DTMOS-biased single-stage all-PMOS rectifier results in achieving 7 % higher power conversion efficiency in comparison with a conventional Body Tied to Source Metal Oxide Semiconductor (BTMOS) biasing-based CMOS rectifier by using a 25% lower RF input power level.

The applicability of the DTMOS arrangement was also considered in other standard architectures used in RF-to-DC conversion. To perform this study, the high performance Self Vth Cancellation (SVC) CMOS rectifier [74] was selected in publication [**II**]. The post layout simulation results show that the settling time of a DTMOS-biased SVC rectifier, consistently decreases by 50% for various input RF signal amplitudes compared to the BTMOS-biased SVC rectifier. It was observed that both PCE and VCE performance was improved by a factor of two at the trigger voltage (0.5 V) [74] in the DTMOS-biased SVC rectifier as compared to the BTMOS-biased SVC rectifier.

In addition, the DTMOS arrangement was also implemented in a classical high efficiency differential rectifier [72]. The circuit arrangement is shown in Fig. 2.19. It can be seen from the figure that the body termi-

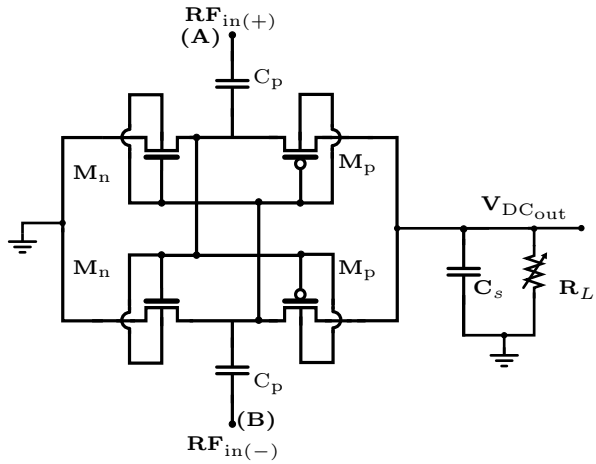
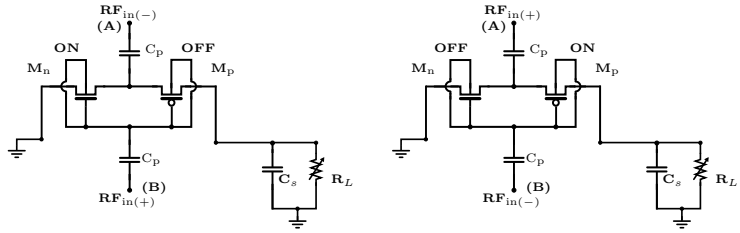


Figure 2.19. DTMOS-biased differential rectifier.



(a) (b)

Figure 2.20. (a) Charging and (b) Discharging phase of DTMOS-biased differential rectifier.

nal of the transistors are connected to the gate terminal thus forming the classical DTMOS biasing. When a negative ($RF_{in(-)}$) and a positive half ($RF_{in(+)}$) appear at nodes (A) and (B) respectively, the rectifier enters into charging phase (Fig. 2.20(a)). During this phase, NMOS (M_n) enters into conduction mode while PMOS M_p enters into non-conduction mode of operation. Since the rectifier is DTMOS-biased hence the presence of $RF_{in(+)}$ at the common gate terminals (node (B)) generates forward body biasing for M_n and reverse body biasing for M_p therefore there will, ideally, be no leakage towards the load (R_L) via M_p. Similarly, when the rectifier enters into discharging mode (Fig. 2.20(b)), the body biasing condition reverses for M_n and M_p ensuring that leakages via M_n will be absent. Thus, the presence of dynamic body biasing results in an improvement in the sensitivity of the rectifier towards a low input RF power level, with a considerable increase in the power conversion efficiency.

In the design, the aspect ratio of transistors (M_p and M_n) were determined by performing optimization with a constraint of high power efficiency. This optimized value is 10 μm/0.18 μm. For the optimization, the fly capacitor (C_p) and storage capacitor (C_s) were fixed as 5 pF and 10 pF respectively. It can be noticed that the optimized aspect ratio is reduced by a factor of two as compared to the aspect ratio of the conventional differential rectifier (20 μm/0.18 μm).

Table 2.3. Performance summary and comparison of differential rectifiers.

Single-Stage Architecture									
	Conventional (conv)			**Proposed (dtmos)**			**Δ=dtmos-conv**		
R_{Load}	**Peak**	**P_{in}**	**Out**	**Peak**	**P_{in}**	**Out**	**Peak**	**Pin**	**Out**
KΩ	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dB)**	**DC (V)**
1	49.79	-3.588	0.4726	46.17	-5.042	0.385	-3.62	-1.45	-0.09
10	68.52	-13.62	0.5605	73.25	-15.87	0.4364	4.73	-2.25	-0.12
100	55.93	-24.6	0.4405	69.97	-27.4	0.3568	14.04	-2.80	-0.08
1000	15.5	-30.31	0.3796	33.86	-35.76	0.2995	18.36	-5.45	-0.08
Three-Stage Architecture									
	Conventional (conv)			**Proposed (dtmos)**			**Δ=dtmos-conv**		
R_{Load}	**Peak**	**P_{in}**	**Out**	**Peak**	**P_{in}**	**Out**	**Peak**	**Pin**	**Out**
KΩ	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dB)**	**DC (V)**
1	15.02	0.2527	0.4035	20.08	2.063	0.5744	5.06	1.81	0.17
10	62.8	-2.288	1.929	64.15	-4.801	1.46	1.35	-2.51	-0.47
100	67.07	-15.16	1.431	52	-16.38	1.095	-15.07	-1.22	-0.34
1000	33.92	-24.6	1.029	14.85	-22	0.9683	-19.07	2.60	-0.06

The post-layout transient simulations were done for the resistive load R_L of the values 1 KΩ, 10 KΩ, 100 KΩ and 1 MΩ. The performance summary and comparison of the proposed rectifier with the conventional rectifier for single and three-stage architecture is listed in Table. 2.3. The detailed post-layout simulation results of the power conversion efficiency and the output DC voltage of single-stage and three-stage conventional and proposed rectifiers are shown in Fig. 2.24, Fig. 2.25, Fig. 2.26 and

Fig. 2.27 respectively for an RF frequency of 433 MHz. It can be observed in Table. 2.3 that the DTMOS biasing exhibits considerable improvement in the power conversion efficiency (<+4 %) and with the lower input RF power level (<-2 dB) in single-stage architecture as compared to a conventional rectifier for the resistive load values $\geq$ 10 KΩ In the three-stage configuration, the performance of the proposed rectifier is comparable with the conventional rectifier for heavy-load conditions (1 KΩ and 10 KΩ). On the contrary, power conversion efficiency has been reduced by 15 % in a three-stage configuration for light-load conditions (R_L=100 KΩ, 1 MΩ). This reduction in efficiency is due to the generation of a high DC voltage level at the electrical source terminal of a transistor and consequently the effective source-body voltage increases. The PCE value will worsen with any further increase in the resistance value, as it will result in a parallel increase in the body-source voltage. Consequently, the transistors will cross a safe operating region (as shown in Fig.2.16) and the conversion performance will be drastically reduced. However, this performance behavior of DTMOS biasing demonstrates that it is far more suitable for heavy-load conditions which is one of the essential requirement in RF energy harvesting based designs.

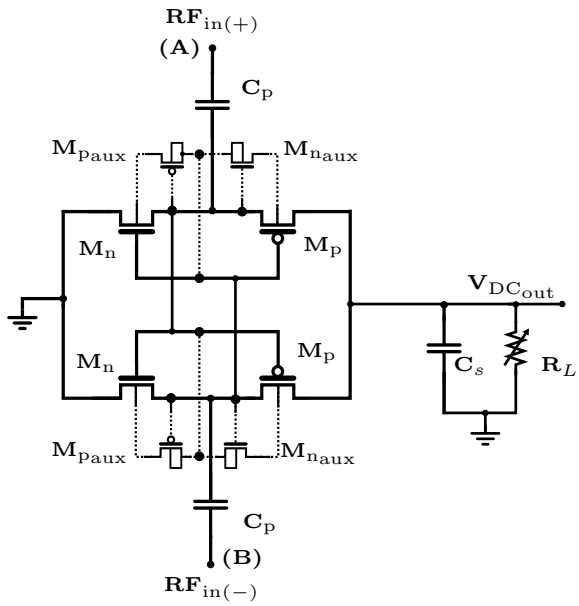


Figure 2.21. Modified DTMOS-biased differential rectifier.

An alternate architecture for providing DTMOS biasing to the transistors is proposed in Fig. 2.21. Here biasing to the body terminal of the main

transistors (M_n and M_p) have been provided by using auxiliary transistors M_{paux} and M_{naux} respectively.

Consider, only transistor M_n (Fig. 2.22) for analysis due to the alternate and similar operation behavior of M_n and M_p transistors. In the figure, V_{dN} and V_{gN} are the differential drain and gate voltages of M_n and the auxiliary PMOS transistor $M_{p_{aux}}$.

When a negative ($RF_{in(-)}$) and a positive half ($RF_{in(+)}$) appear at nodes (A) and (B) respectively (Fig. 2.21), transistor $M_{p_{aux}}$ will be switched-ON and hence, by applying Kirchoff Voltage Law (KVL) the body voltage V_{bN} of M_n will become:

$$V_{bN} = V_{gN} - V_{gbN} \tag{2.39}$$

where V_{gbN1} is the voltage between the source terminal and the drain terminal of $M_{p_{aux}}$.

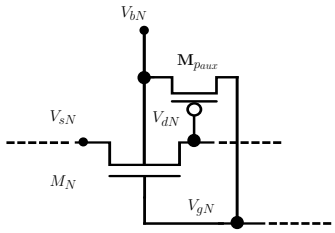


Figure 2.22. Body connection for NMOS transistor.

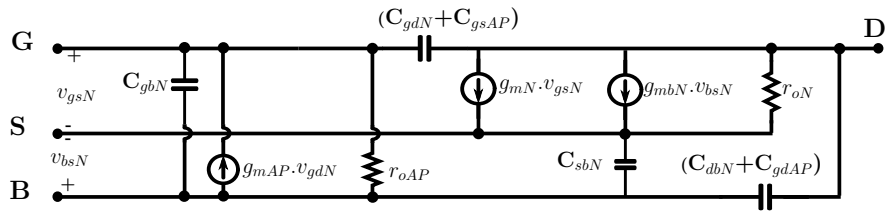


Figure 2.23. Small signal model equivalent of M_n and $M_{p_{aux}}$ transistors.

This auxiliary transistor acts as an additional rectifier which extracts a DC voltage value for the body terminals of the main transistors from the differential RF signal (node (A) and node (B)). The load capacitor to this rectifier is composed of body parasitic capacitances. To explain this phenomenon, a small signal model equivalent circuit of Fig. 2.22 is shown in Fig. 2.23. Here, the source, gate, drain and body terminals of M_n are denoted by nodes S, G, D and B. The parasitic capacitances associated with M_n (C_{gbN}, C_{gdN}, C_{dbN} and C_{sbN}) and with $M_{p_{aux}}$(C_{gsAP} and C_{gdAP}) are considered.

The drain and the gate voltages have an influence on the body voltage through ($C_{dbN} + C_{gdAP}$) and C_{gbN}. In the design, the minimum sized aspect ratio of 0.22 μm/0.18 μm was selected for the auxiliary transistors to minimize the parasitic capacitances introduced by them when compared to those of the primary transistors. Thus, it can be approximated that ($C_{dbN} + C_{gdAP}$) $\approx C_{dbN}$. Through simulations, it has been found that the

Table 2.4. Performance summary and comparison of differential rectifiers.

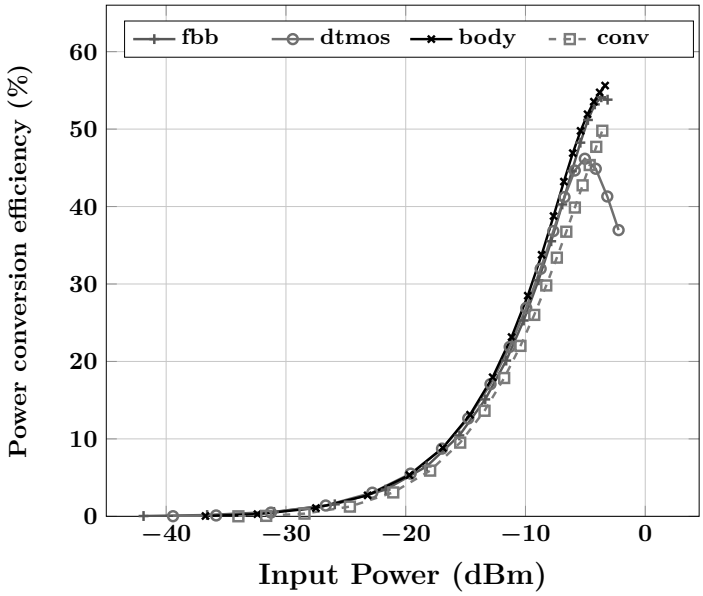
Single-Stage Architecture									
	Conventional (conv)			**Proposed (body)**			**Δ=body-conv**		
R_{Load}	**Peak**	**P_{in}**	**Out**	**Peak**	**P_{in}**	**Out**	**Peak**	**Pin**	**Out**
KΩ	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dB)**	**DC (V)**
1	49.79	-3.60	0.47	55.62	-3.351	0.52	5.83	0.24	0.04
10	68.52	-13.62	0.56	69.52	-16.73	0.39	1.00	-3.11	-0.18
100	55.93	-24.6	0.44	61.11	-27.12	0.35	5.18	-2.52	-0.10
1000	15.5	-30.31	0.38	25.98	-35.26	0.28	10.48	-4.95	-0.10
Three-Stage Architecture									
	Conventional (conv)			**Proposed (body)**			**Δ=body-conv**		
R_{Load}	**Peak**	**P_{in}**	**Out**	**Peak**	**P_{in}**	**Out**	**Peak**	**Pin**	**Out**
KΩ	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dBm)**	**DC (V)**	**PCE (%)**	**(dB)**	**DC (V)**
1	15.02	0.25	0.41	24.5	1.474	0.60	9.48	1.22	0.19
10	62.8	-2.30	1.93	67.22	-5.582	1.37	4.42	-3.29	-0.56
100	67.07	-15.16	1.4	73.37	-17.78	1.11	1.106	-2.62	-0.33
1000	33.92	-24.6	1.03	69.14	-30.43	0.80	0.7916	-5.83	-0.24

charging and discharging of the body terminal voltage follows the drain terminal voltage, which indicates that the influence of C_{dbN} on V_{bN} dominates compared to that of C_{gbN1}. It therefore acts as a load capacitor to the auxiliary transistor-based rectifier.

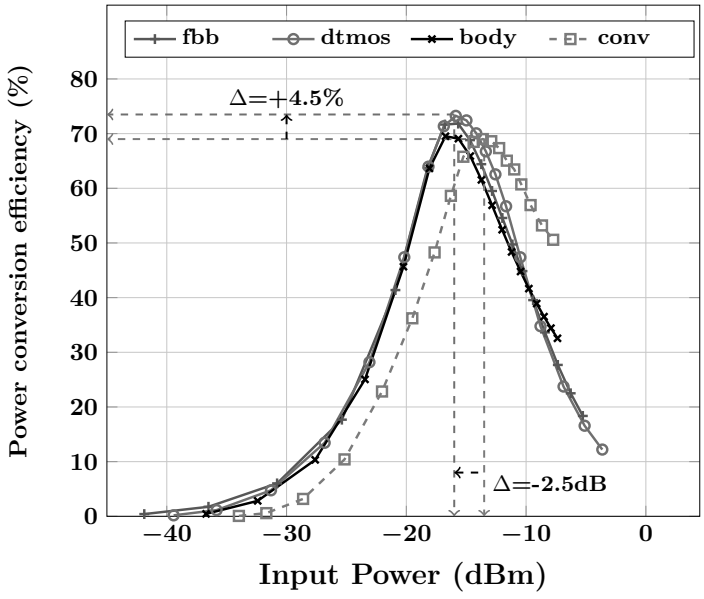
The optimized aspect ratio of the transistors (M_p and M_n) are 20 μm/0.18 μm, which was obtained by using maximum power conversion efficiency as a constraint. The optimization was done with the fixed values of the fly capacitor (C_p) and the storage capacitor (C_s) as 5 pF and 10 pF respectively. As mentioned earlier, the aspect ratio of the auxiliary transistor are 0.22 μm/0.18 μm. The post-layout transient simulations were done for the resistive load (R_L) of the values 1 KΩ,10 KΩ, 100 KΩ and 1 MΩ.

The performance summary and comparison of the proposed rectifier with the conventional rectifier for single and three-stage architectures are collected in Table. 2.4.

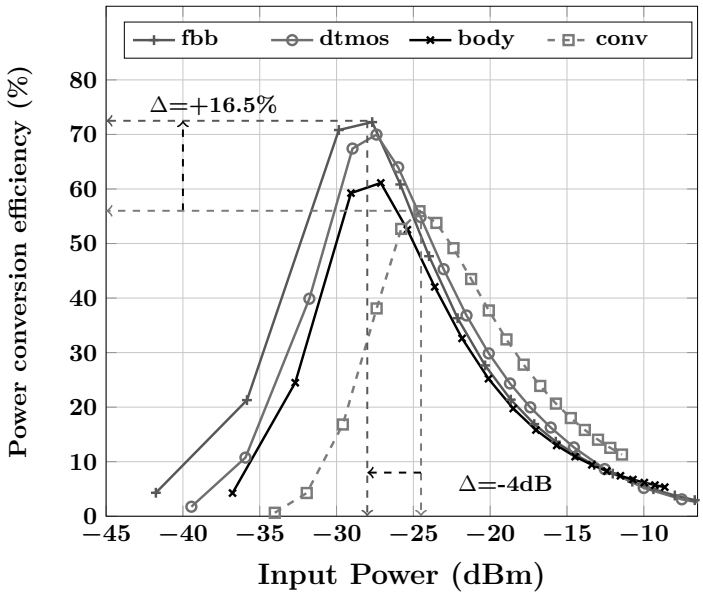
It can be observed from Table. 2.4 that in a single-stage configuration with increasing load ($R_{load} \geq$10KΩ) the PCE and the input RF power sensitivity are both increasing. On the contrary, in three-stage configuration the PCE is comparable but there is a considerable improvement in input RF power sensitivity. The detailed post-layout simulation results of the power conversion efficiency and the output DC voltage of single-stage and three-stage conventional and proposed rectifiers are shown in Fig. 2.24, Fig. 2.25, Fig. 2.26 and Fig. 2.27 respectively for an RF frequency of 433 MHz.



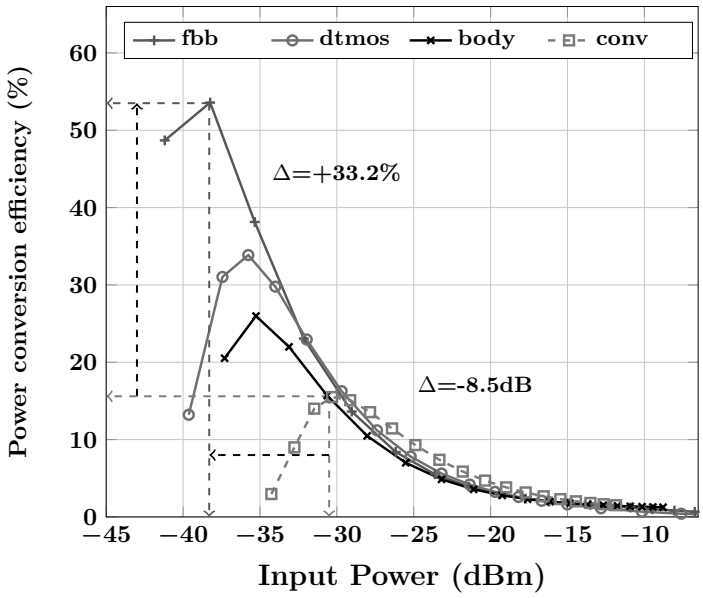
(a) R_L=1 KΩ



(b) R_L=10 KΩ

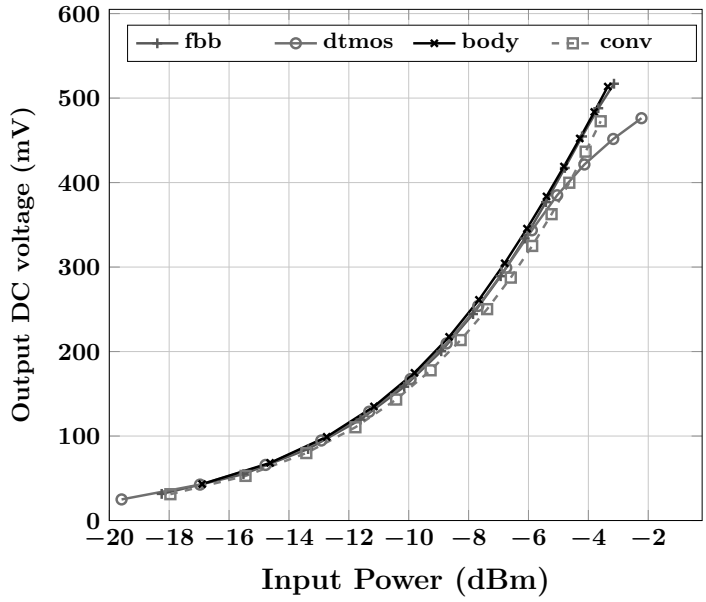


(c) R_L=100 KΩ

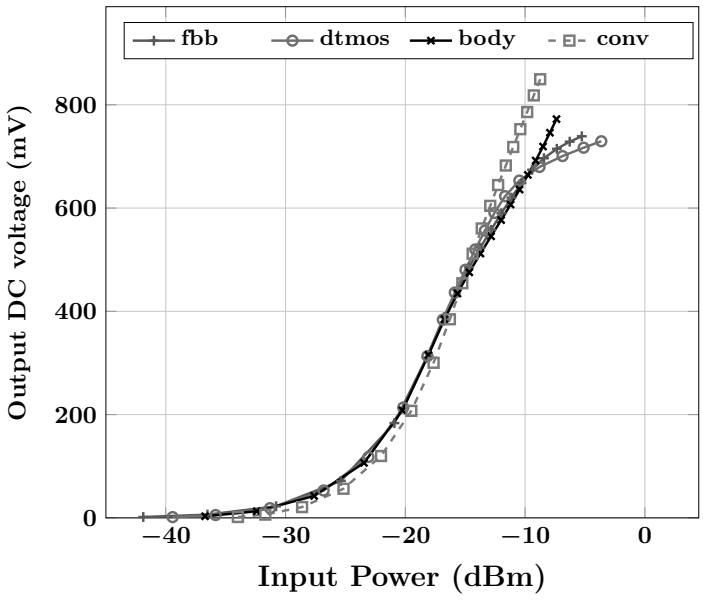


(d) R_L=1 MΩ

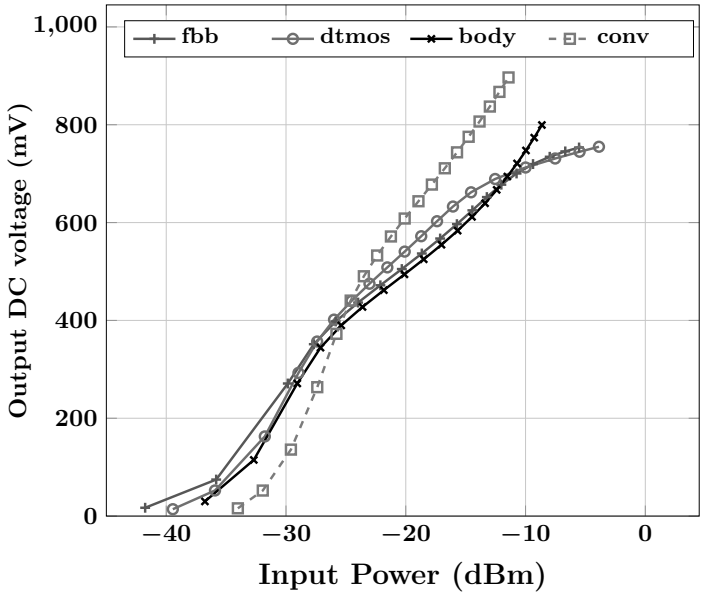
Figure 2.24. Power conversion efficiency at different resistive loads for single-stage differential rectifier.



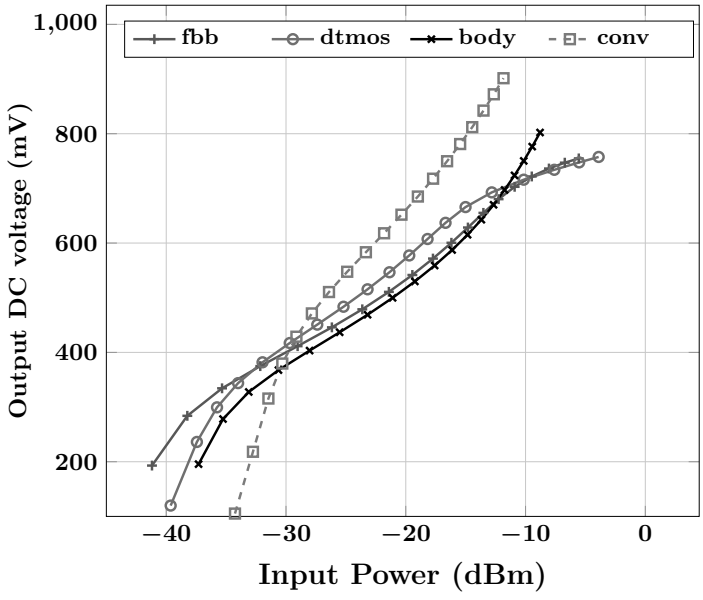
(a) R_L=1 KΩ



(b) R_L=10 KΩ

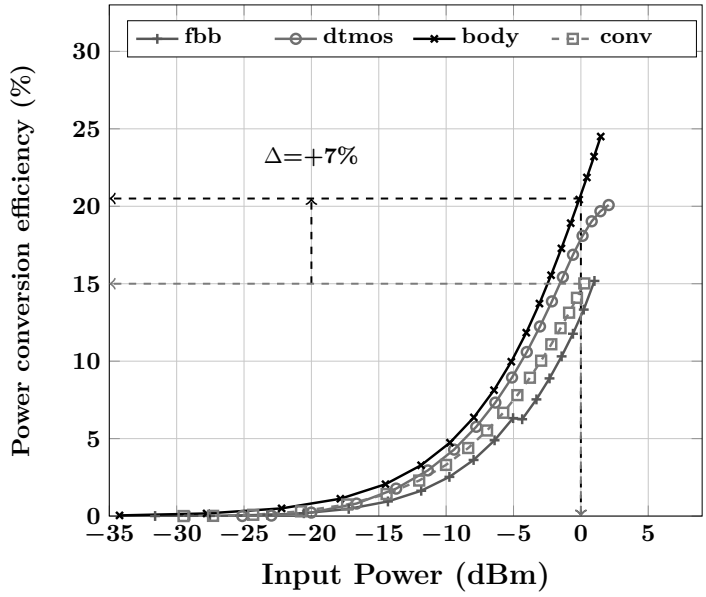


(c) R_L=100 KΩ

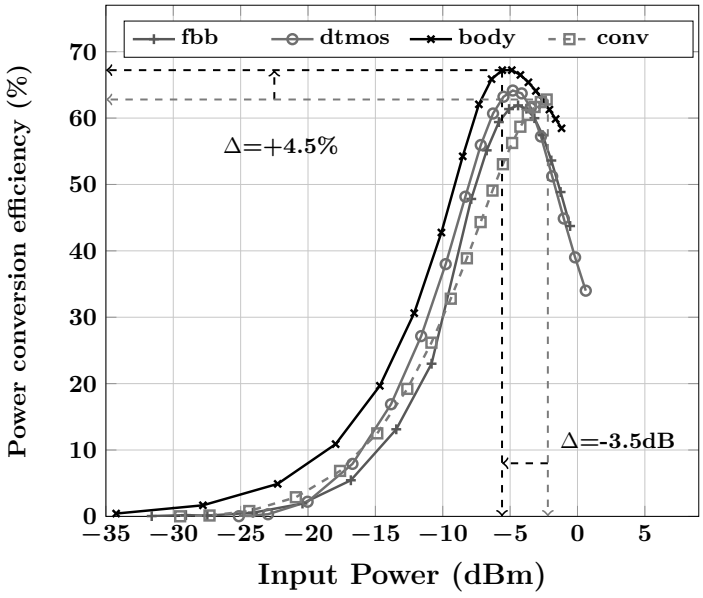


(d) R_L=1 MΩ

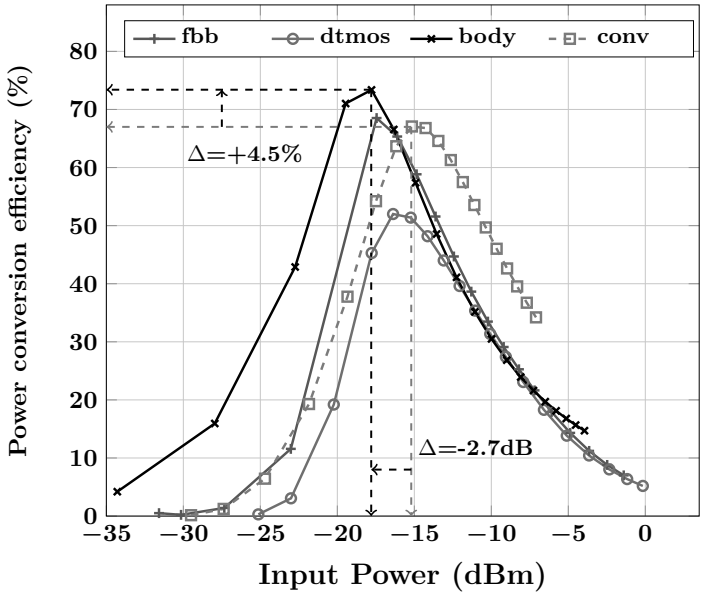
Figure 2.25. Output DC voltage at different resistive loads for single-stage differential rectifier.



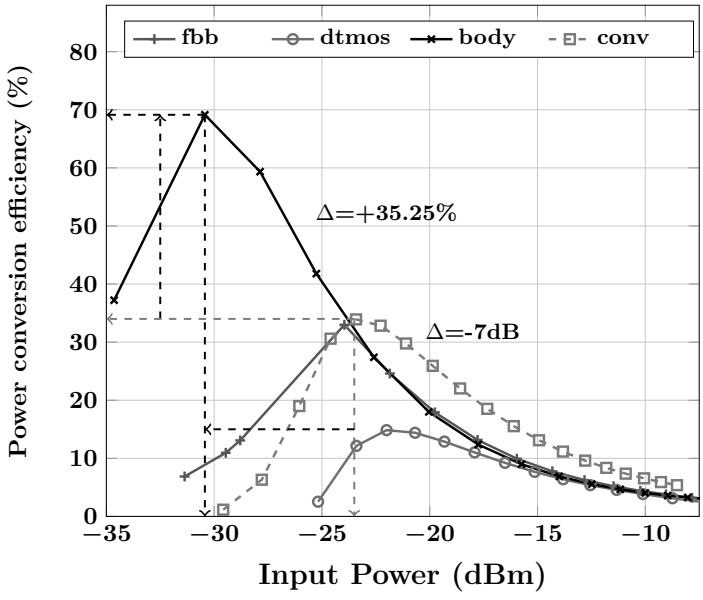
(a) R_L=1 KΩ



(b) R_L=10 KΩ

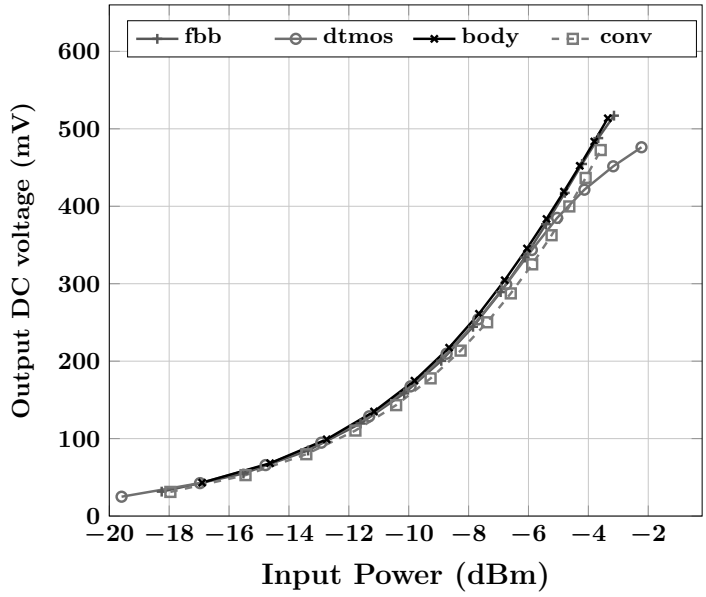


(c) R_L=100 KΩ

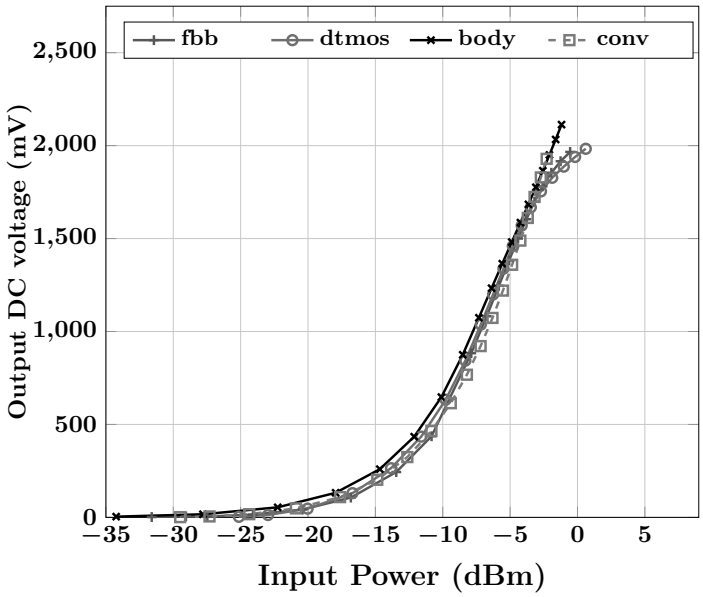


(d) R_L=1 MΩ

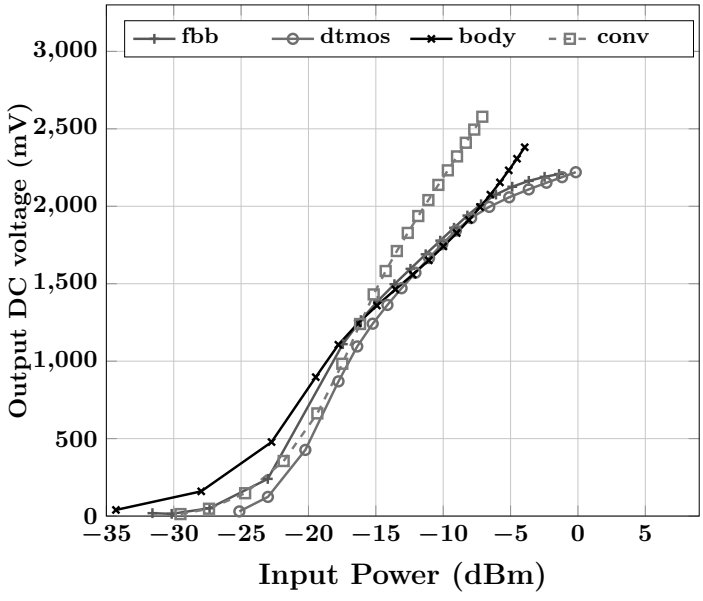
Figure 2.26. Power conversion efficiency at different resistive loads for three-stage differential rectifier.



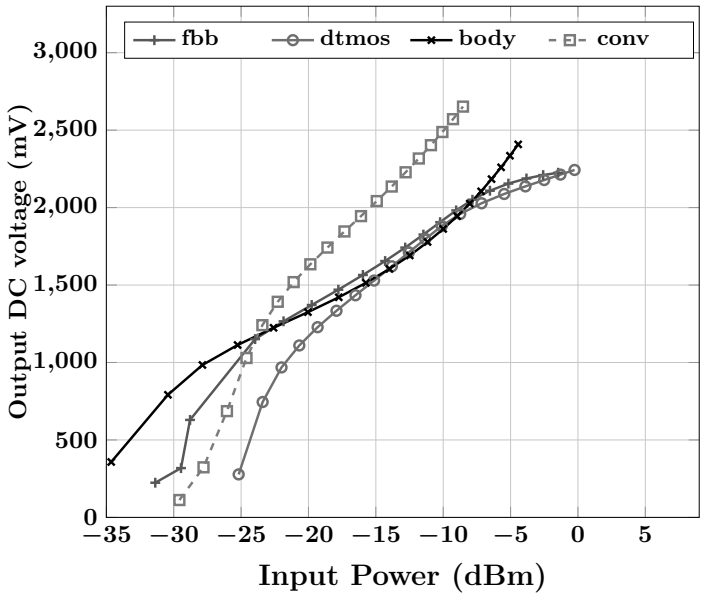
(a) R_L=1 KΩ



(b) R_L=10 KΩ



(c) R_L=100 KΩ



(d) R_L=1 MΩ

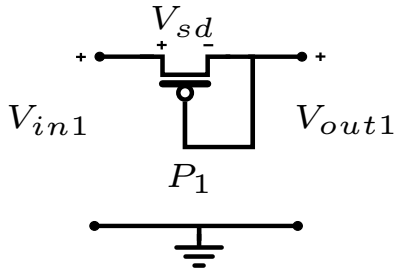
Figure 2.27. Output DC voltage at different resistive loads for three-stage differential rectifier.

2.3.2 Designs with additional circuits

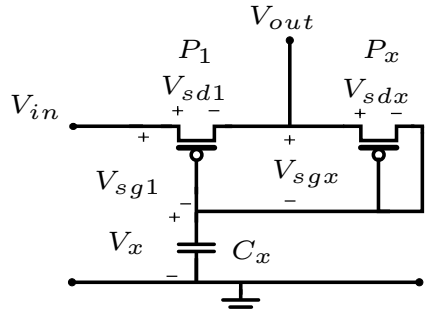
2.3.2.1 Circuit arrangement-I

The threshold voltage compensation of the transistors used in rectifiers can be achieved by applying a DC voltage between the gate and drain terminals or at the gate terminals [17]. If this voltage is obtained from an external source, then it is commonly known as the External Vth Cancellation (EVC) scheme [74], [75]. Similarly, if the compensation voltage is generated by using additional CMOS components and regulated DC voltage as a source, then it is referred to as the Internal Vth Cancellation (IVC) scheme [68], [76].

Fig. 2.28(b) shows the implementation of the proposed voltage cancellation scheme [**III**] in the PMOS transistor (P1) by using an additional PMOS transistor (P_x) and capacitor (C_{AUX}). In this implementation, the body-terminal of the transistors was tied to the source terminal to avoid body effect over threshold voltage.

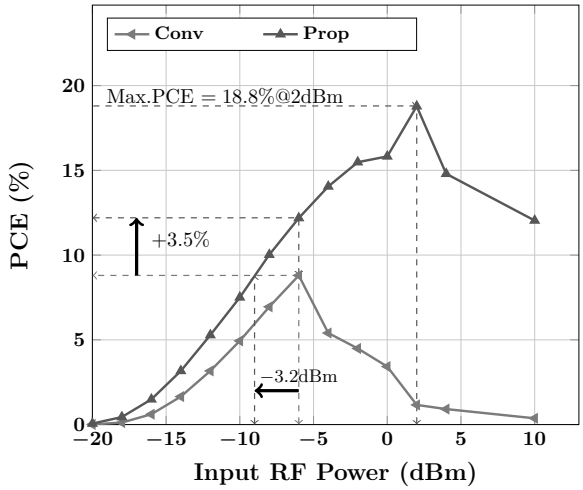


(a)

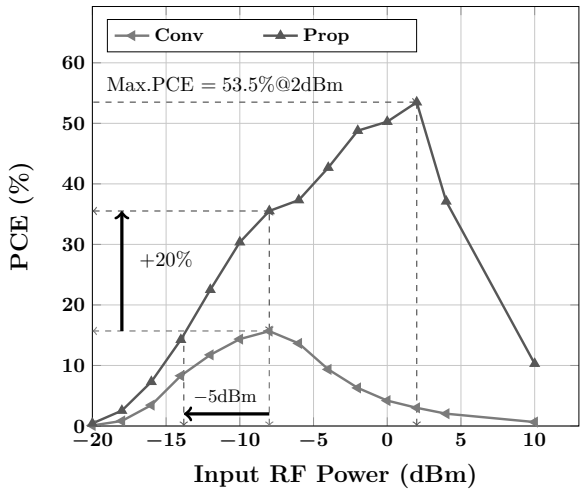


(b)

Figure 2.28. (a) Conventional diode-connected transistor and (b) after implementation of the proposed scheme.



(a) $Z_L = 1K\Omega||10pF$



(b) $Z_L = 10K\Omega||10pF$

Figure 2.29. Measured power conversion efficiency of the conventional and proposed rectifiers for different load impedances.

It was shown in publication [**III**] that, theoretically, the P_x reduces the effect of the threshold voltage of the P_1 effect in the rectified output DC voltage as follows:

$$V_{out} = \frac{1}{2}(V_{in} + V_{thp1} - V_{thpx} + V_{AUX}) \tag{2.40}$$

where V_{in} is the peak input RF signal amplitude, V_{thp} and V_{thpx} are the threshold voltages of P_1 and P_x respectively, and V_{AUX} is the voltage across capacitor C_{AUX}. In-depth implementation details of the proposed architecture are available in [77].

The measured results for the conventional CMOS rectifier (Conv) and after implementing the proposed scheme in the PMOS transistor (Prop) is shown in Fig. 2.29
The following observations can be seen in the measured results:

- After implementing the proposed scheme in a conventional rectifier the conversion performance has improved.

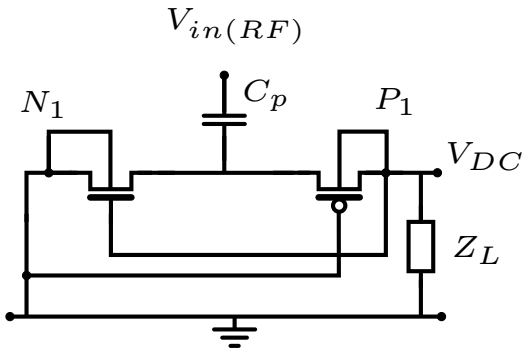
- The maximum power conversion efficiency obtained from the proposed rectifier is 53.5% at 2 dBm RF power level.

- The proposed architecture required 5 dB lower input RF power to achieve power conversion efficiency equal to the conventional rectifier.

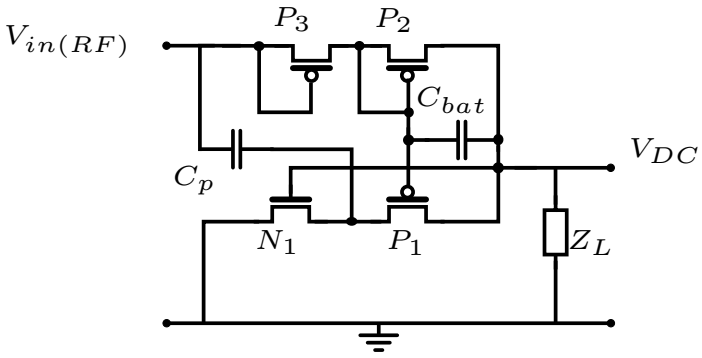
2.3.2.2 Circuit Arrangement -II

It has been mentioned earlier that the threshold voltage compensation is obtained either by using the EVC scheme or from the IVC scheme. In these schemes, the RF signal is not directly involved, *i.e.* the DC bias voltage is obtained either externally (EVC) or internally (IVC).
The work presented in [74], [78] proposed the method to involve received RF signals for threshold voltage compensation in a rectifier. In [74], a secondary rectifier network was used to compensate the threshold voltage of the primary rectifier network. Similarly, [78] employs diode-connected transistors with a gate-to-drain bootstrapping capacitor to overcome the threshold voltage loss. The charging and discharging of these bootstrapping capacitors depends on the received RF signal amplitude.

In publication [**IV**], a scheme was proposed to obtain the bias voltage required to compensate the V_{th} by collectively using the received RF signal and the rectified DC output voltage (Fig. 2.30(b)). It can be observed in Fig. 2.30(b), that the threshold compensation circuit was designed only for the PMOS transistor P1. The biasing arrangement for the NMOS transistor N1 was selected directly from [79] (Fig. 2.30(a)). Also, in this implementation, the body-terminal of the transistors was tied to the source terminal to avoid body effect over threshold voltage. To evaluate the performance of the proposed scheme, the SVC CMOS rectifier optimized for 433 MHz was also implemented ON-chip for the purpose of comparison. The measured power conversion efficiency for the SVC and the proposed



(a)



(b)

Figure 2.30. (a) Self Vth Cancellation based CMOS rectifier and (b) after implementation of the proposed scheme in PMOS transistor (P1).

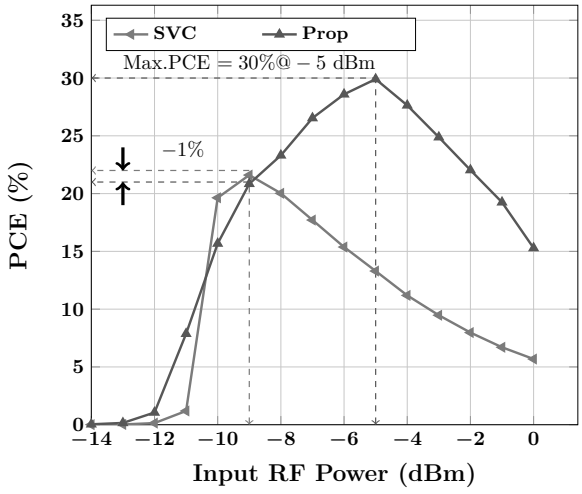
rectifier is shown in Fig. 2.31.

The following are of the observations from the measured results:

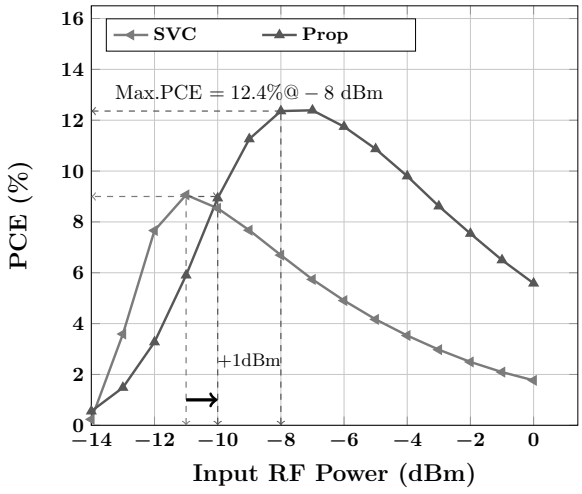
- The measured PCE values of the proposed architecture is comparable with the SVC architecture for same RF input power level.

- With an increase in resistive load the proposed architecture requires a 1 dBm higher RF input power level to equalize the PCE level with the SVC architecture.

- The area under the PCE curve of the proposed architecture is wider than the PCE curve obtained from the SVC architecture. Thus, the higher power conversion efficiency is available for a wide range of in-



(a) $Z_L = 10K\Omega||10pF$



(b) $Z_L = 30K\Omega||10pF$

Figure 2.31. Measured power conversion efficiency of self Vth cancellation scheme based CMOS rectifier (SVC) and the proposed CMOS rectifier (Prop) for different load impedances.

put RF power levels.

2.3.3 Design using signaling scheme for voltage multiplier

In general practice, a DC voltage level attended by a single-stage rectifier is not sufficiently high (< $3V_{th}$). Thus, to obtain a higher DC voltage level, multistage rectifier implementation has been adopted [80]. This arrangement is known as the voltage multiplier VM circuit in the literature. This circuit is a cascade arrangement designed from a series of rectifiers to obtain a high DC output voltage. In this classical approach, the DC voltage which becomes generated in the present stage contributes to the next stage. This phenomenon happens at every stage resulting in a higher DC output voltage than previously reported works in [17], [66], [81], [82].

In this work, the VM used to implement the proposed signaling scheme was selected from [72]. This voltage multiplier arrangement is shown in Fig. 2.32.

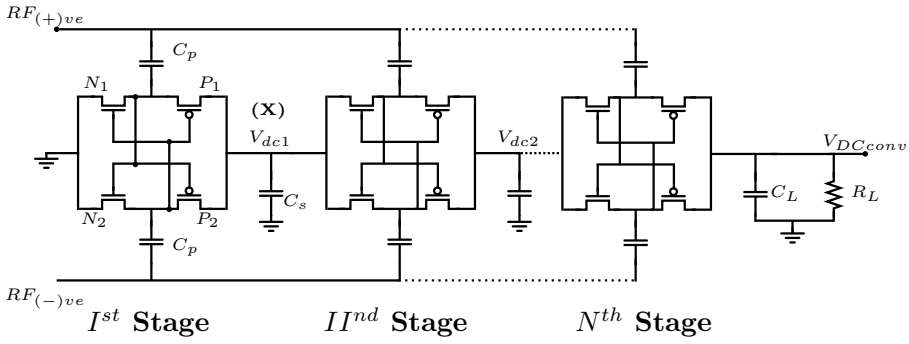


Figure 2.32. Differential drive rectifier based voltage multiplier arrangement.

It can be seen in Fig. 2.32 that the first stage is cascaded to the next stage and this pattern is followed with the increase in the number of stages. It was shown in publication [**V**] that a generalized first order expression for the output DC voltage for this VM circuit is given by:

$$V_{DCconv} = \underbrace{2N \cdot V_p}_{a} - \underbrace{N \cdot (V_{dn} + V_{dp})}_{b} \tag{2.41}$$

where N is the number of stages, V_p is the peak RF input amplitude, V_{dn} and V_{dp} are the voltage loss across the NMOS and PMOS transistors.

Eq. 2.41 is constituted of two parts; part (a) is an ideal output DC voltage, while part (b) indicates the dominant cause for the voltage loss. A straightforward conclusion that can be drawn from (2.41) is that with an increase in the number of stages (N), the loss will increase correspond-

ingly, and as a result, the net output DC voltage will reduce.

One of the possible solutions to this issue is shown in (2.42).

$$V_{DCconv} = 2N \cdot V_p - N \cdot (V_{dn} + V_{dp}) + V_{aux} \tag{2.42}$$

Here V_{aux} is the auxiliary voltage source that can be obtained through either external [74], or internal [68] circuit arrangement. Thus, the loss in output DC voltage will be compensated.

In this work, a simple signaling scheme shown in Fig. 2.33 was proposed to form the voltage multiplier arrangement. This scheme utilizes the input RF signal to generate the auxiliary voltage V_{aux} which is required to overcome the loss. The first order approximate output DC voltage from the proposed VM architecture [**V**] is given by:

$$V_{DCprop} = (4N + 2) \cdot V_p - N \cdot (V_{dn} + V_{dp}) \tag{2.43}$$

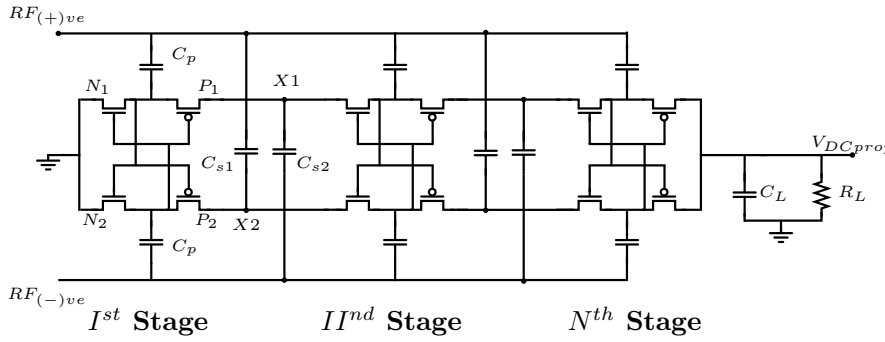


Figure 2.33. Differential drive rectifier-based voltage multiplier arrangement with proposed signaling scheme.

In Fig. 2.34, the plots that correspond to equations (2.41) and (2.42) are marked as C_{ideal} and P_{ideal} respectively. These plots have been made for the peak input voltage V_p =0.5 V, with the voltage loss of (V_{dn}, V_{dp}) =0.3 V. It should be noted that this voltage loss across the transistors has been estimated from the transient simulations.

Similarly, the simulated values of the output DC voltages obtained from the various number of stages of the proposed and the conventional voltage multipliers are shown as P_{sim} and C_{sim} respectively for the capacitive load of 5 pF only. These transient simulations were done in the Cadence environment using the Spectre simulator for an RF input signal amplitude of 0.5 V at 433 MHz. It can be observed in Fig. 2.34 that the simulated behavior trend of the voltage multipliers is in agreement with the ideal

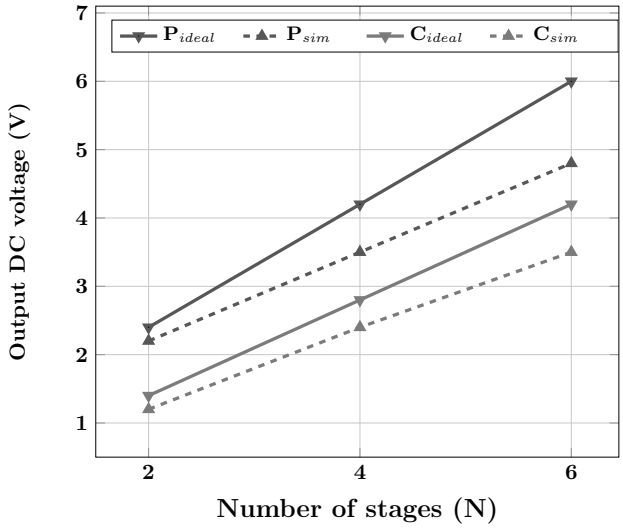


Figure 2.34. Ideal and simulated plots of conventional (C_{ideal} and C_{sim}) and the proposed (P_{ideal} and P_{sim}) voltage multiplier circuits.

equations (Eq. 2.41 and Eq. 2.42).

The measured results of these voltage multiplier were published in publication [**V**]. The performance of the VM circuits was evaluated in terms of the power conversion efficiency and the output DC voltage by using resistive load values of 30 KΩ, 100 KΩ,and 1 MΩ respectively. The measured results show that the proposed VM scheme has a better power conversion efficiency than the conventional VM scheme depending on load conditions and input RF power levels.

2.4 Summary

Different architectures for rectifier designing were presented in this chapter. A detailed theoretical analysis supported with simulations is presented. These observations are useful in the development of new rectifier circuits. The circuits which were proposed in this work are divided into three categories as, (i) use of the body terminal of the transistor, (ii) use of the additional circuits and (iii) use of the novel signaling scheme. The performance comparison of the proposed RF-to-DC converters with the state-of-the-art rectifiers is listed in Table. 2.5.

The simplicity in the implementation and the measured performance shown in various publications make the proposed rectifiers suitable in RF energy harvesting for various applications.

Table 2.5. Performance comparison with state-of-the-art RF to DC converters.

Literature	Tech.	No. of Stages	Peak PCE (%)	at Power level (dBm)	Load	Remark
[72]	180 nm	1	67.5	-12.5	10 KΩ	With RF options
[83]	130 nm	2	60	-17	-	Voltage regulator as a load
[17]	250 nm	36	60	-8	5.6 MΩ	-
[**III**]	180 nm	1	54.7	1	10 KΩ	-
[76]	350 nm	1	42	-3.5	-	-
[81]	65 nm	5	31.8	18	2 KΩ	-
[84]	90 nm	5	31.5	-15	330 KΩ	-
[27]	-	5	30	-10	50 KΩ	discrete components
[**IV**]	180 nm	1	30	-5	10 KΩ	-
[79]	180 nm	1	29	-10	10 KΩ	-
[85]	180 nm	24	26.5	-11	473 KΩ	Zero Vth MOSFET
[**I**]	180 nm	1	23	-10	10 KΩ	-
[86]	130 nm	12	22.6	-16.8	1 MΩ	-
[**I**]	180 nm	1	16	-8	10 KΩ	**Conv. CMOS rectifier**
[**V**]	180 nm	3	13.5	-1	30 KΩ	-
[75]	130 nm	6	11	-6	16 KΩ	Calculated Load
[66]	90 nm	17	11	-15	1 MΩ	-
[54]	180 nm	4	5.14	-14.1	5 MΩ	With Native Device
[82]	130 nm	16	10	-10	Output Current=10μA	-

3. Reference Circuits

3.1 Introduction

In addition to traditional digital circuits, the CMOS technology is extensively used in analog and mixed-mode implementations. The performance of these circuits largely depends on a special class of circuits known as reference circuits. The reference circuit provides an electrical quantity that exhibits well-defined dependence on supply, process and temperature [87]. These electrical quantities are mainly voltage [88], [89], current [90], [91] and frequency [92], [93]. In general, the voltage or current reference circuits are essential components in data converters and are used for biasing purposes, while the frequency reference is used for clock driven circuits. [94].

This chapter starts with a discussion of the performance measuring parameters used for reference circuits, followed by the error sources in typical reference circuit design; finally, the chapter concludes with a brief summary of the research work in this specific area.

3.2 Performance measurement parameters

In general practice, the performance of various circuit blocks is a function of the reference circuits performance. Hence, a number of metrics are used to quantify the quality of the output signal provided by the reference circuits. In this section, some brief details of a few of these metrics are discussed in more details.

3.2.1 Line regulation

The Line Regulation (LR) at nominal or room temperature (LR_{nom}) for a reference signal (X) is defined as:

$$LR_{nom}\left(\frac{\%}{V}\right) = 100.\frac{\Delta X_{nom}}{X_{nom}\cdot\Delta V_{supply}} \tag{3.1}$$

where X_{nom} can be the value of a voltage, current or frequency reference signal at nominal (nom) temperature, ΔX_{nom} is the difference between the maximum and minimum values of the reference signal within the supply voltage (V_{supply}) variation in the range of $\left[V_{supply(min)}, V_{supply(max)}\right]$.

3.2.2 Temperature coefficient

The Temperature Coefficient (TC), or temperature sensitivity, defines the reference signal change over a given range of operating temperatures $[T_{min},\ T_{max}]$. The parameter TC at the supply voltage (V_{supply}) is given by:

$$TC|_{V_{supply}}\left(\frac{ppm}{^{\circ}C}\right) = \frac{1}{X_{nom}}\frac{(X_{max}-X_{min})}{(T_{max}-T_{min})}\cdot 10^{6} \tag{3.2}$$

where X_{nom} is the value of the reference signal at nominal temperature (T_{nom}), X_{max} and X_{min} respectively represents the maximum and minimum values of the reference signal. These values have been achieved by the reference signal over the selected temperature range for a given supply voltage (V_{supply}).

3.2.3 Power supply rejection ratio

The Power Supply Rejection Ratio (PSRR) is the ability of the reference generating circuit to reject the noise and other spurious signals at a particular frequency on the power rail and thus provide a stable reference signal. The definition of the PSRR (dB) for a voltage reference circuit is:

$$PSRR(f)|_{T_{nom}} = 20\ log\ \left(\frac{V_{ref,AC}(f)}{V_{supply,AC}(f)}\right) \tag{3.3}$$

where $V_{supply,AC}(f)$ is the ripple voltage signal present in the DC supply voltage V_{supply}. Similarly, $V_{ref,AC}(f)$ is the variation that appeared in the reference voltage $V_{ref,nom}$ value at the nominal temperature due to the presence of $V_{supply,AC}(f)$, Likewise, in the literature, the PSRR parameter value for the current reference circuits is presented as [95–97]:

$$PSRR|_{T_{nom}} = \begin{cases} 20\cdot log_{10}\left(\frac{i_{ref}\cdot R}{V_{supply}}\right) & \text{in dB, where } R\text{=}1\Omega \\ 20\cdot log_{10}\left(\frac{\Delta i_{ref}}{\Delta V_{supply}}\cdot\frac{V_{supply}}{I_{ref}}\right) & \text{in dB, at DC point } (f=0) \end{cases} \tag{3.4}$$

3.2.4 Power dissipation

The power dissipation (P) is defined as:

$$P = V_{supply} \cdot I_{supply} \tag{3.5}$$

where V_{supply} is the supply voltage and I_{supply} is the quiescent current. The power dissipation of the reference circuit should be the target for a low value for two primary reasons; first, longer battery life and second, low temperature density of the hot-spots, for the selected temperature range.

3.2.5 Output noise

The output noise is a frequency-dependent parameter and is only used for the voltage and current reference circuits. The noise characteristics of the reference signal from 0.1 Hz up-to 20 Hz is known as flicker noise and it is useful in low frequency applications such as voltage regulators for instance. The noise from 20 Hz to 20 KHz is known as thermal noise. This noise is considered in designing an Analog to Digital Converter (ADC) and Digital to Analog Converter (DAC) [98–100].

3.2.6 Phase noise and Jitter

Phase noise is measured for a clock signal to evaluate its quality. This parameter examines the spectrum of the clock signal. Jitter is another factor that characterizes the clock signal and represents a fluctuation in the timing of the signal that arises due to the phase noise [101]. Due to the jitter, the zero-crossing time of a periodic signal will vary slightly from the ideal time instance since the clock signal is not strictly periodic due to the noise [102–104].

The common methods used to increase the performance of the reference circuits are listed in Table. 3.1

Table 3.1. Methods to improve performance parameters of reference circuits.

Parameter	Target	Methods to improve	Cons
LR	Decrease	Use cascode arrangement	Increase in supply headroom
		Use Pre-regulator	Require additional Circuit
TC	Decrease	Increase power budget	Not suitable for power aware circuits
		Use thermal compensation	Require additional circuit
		Reduce current mismatch	Require additional circuit
		Use transistors of same size	-
PSRR	Increase	Use cascode arrangement	Decrease in supply headroom
		Use Pre-regulator	Require additional circuit
		Use RC filter with supply line (pole at low frequency)	Require large capacitor
Output Noise	Decrease	Find and optimize noise contributing transistors	-
		Increase power budget	Not suitable for power aware circuits
Phase noise & Jitter	Decrease	Increase Q value	Trading with gain
		Reduce flicker noise (1/f) by use of good biasing circuit	-
		Maximize SNR	Increase in power dissipation
		Find and optimize noise-contributing transistors	-
		Suppress power supply noise	Require large capacitor
		Prefer to use all MOSFET implementations	Not possible always
		Select large sized transistors	Increase in the layout area

3.3 Proposed voltage, current and frequency reference circuits

Voltage, current and frequency reference circuits are needed as basic building blocks for any power management unit. The voltage reference circuit is used in the voltage regulator and in ADC circuits, while the purpose of the current reference circuit is primarily in biasing circuits, in addition, the frequency reference circuit is used in timing and control modules [94].

In this part of the research work, two voltage circuits, one current circuit and one frequency reference circuit were designed. In terms of the working principle, the voltage reference and current reference circuits are able to generate the temperature compensation of the PTAT current to obtain the reference voltage and the reference current values. The PTAT current used in the circuits is obtained from the classical resistorless current reference circuit suggested by Oguey and Aebischer [105]. The proposed reference circuits are all MOSFET-based designs, which operate with lesser power, require a small implementation area, and generate moderately accurate reference quantities.

The brief summary of the reference circuits that were developed for the power management unit (Fig. 1.1) are given in the following sections.

3.3.1 Voltage reference circuit

The Bandgap Voltage Reference (BVR) circuits are comprehensively used to generate an ON-chip reference voltage because of their stable performance against supply voltage and temperature variations [106]. In general, BJT-based implementations are used to obtain a reference voltage equal to the bandgap voltage of the semiconductor [107]. The reference voltage in these circuits is realized by summing the scaled base-emitter (V_{BE}) and PTAT voltages. Here, to perform the scaling function, resistors are a preferred choice due to their ease of implementation [108–113]. In modern CMOS technologies, parasitic BJTs are used in BVR implementations. As a result, the benefits of these circuits come with two limitations: first, the V_{BE} voltage is process dependent and second, a BJT implementation requires a comparatively large silicon area. Thus, any extra effort to reduce the process variation problem will result in an additional silicon area.

A CMOS-based implementation is viewed as an alternate choice to address these issues. Various principles are used to design a CMOS-based voltage reference circuit, for instance the threshold voltage subtraction

[114], the weighted difference of the gate-source voltages [115] or the mutual compensation of the mobility and the threshold voltage [116].

The proposed voltage reference circuits in the publications [**VI**] and [**VII**] are all MOSFET architectures with low power consumption and low temperature coefficients. The proposed circuits are simple in implementation. Hence, they are suitable for use locally during system implementation. The proposed voltage reference circuits are shown in Fig. 3.1 and Fig. 3.2 respectively.

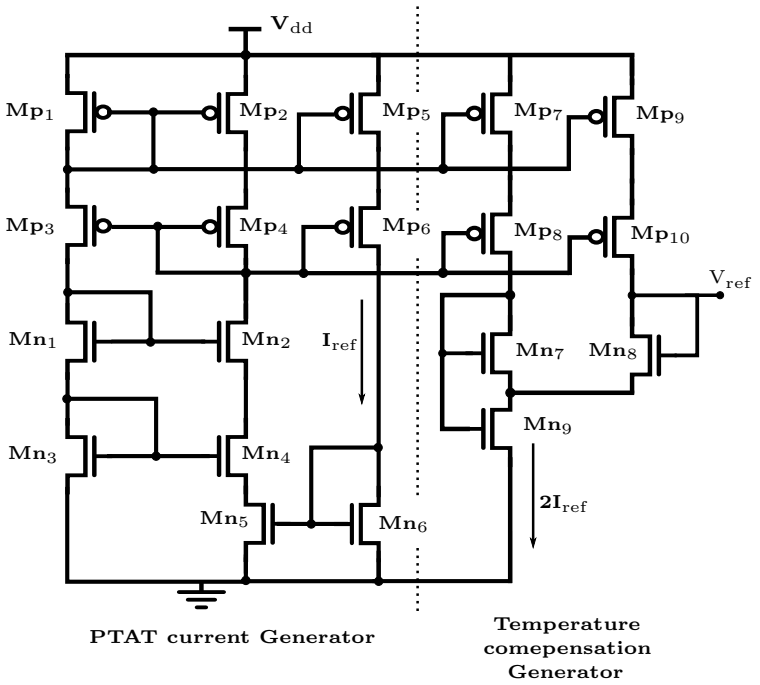


Figure 3.1. Schematic of voltage reference circuit I [**VI**].

It can be noticed in the schematics that the reference circuits have a similar PTAT current generator, which is the classical resistorless beta multiplier circuit reported in [105]. This architecture [105] fulfills the demand for a simple implementation with very a low power current reference circuit. Basically, [105] is the modification of the work published in [117] which is commonly known as the beta multiplier circuit in the literature. The beta multiplier circuit (Fig. 3.3(a)) meets the requirement of a simple implementation. However, the presence of a resistor in the design is a major drawback in case of target current values in the range of nanoampere or pico-ampere. Thus, to solve this issue in [105] the resistor was

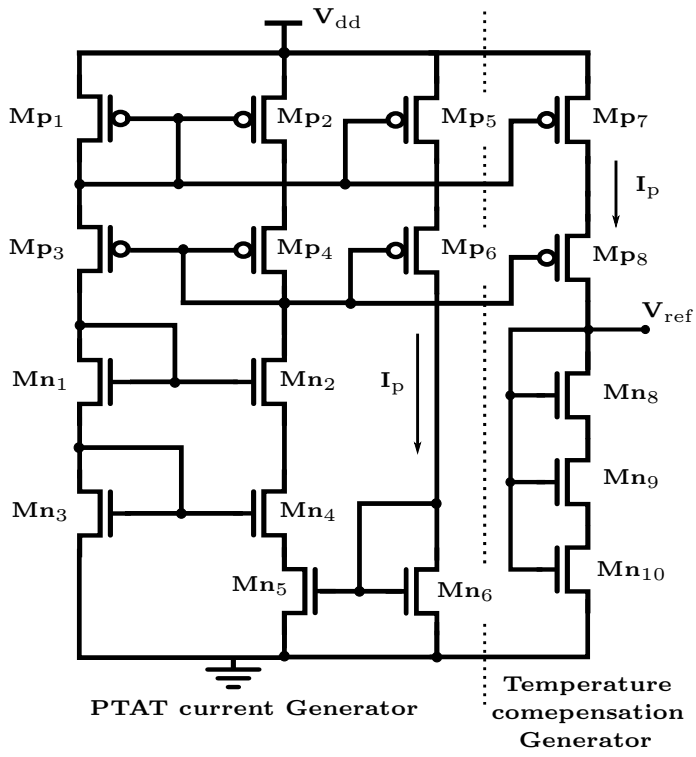


Figure 3.2. Schematic of voltage reference circuit II [**VII**].

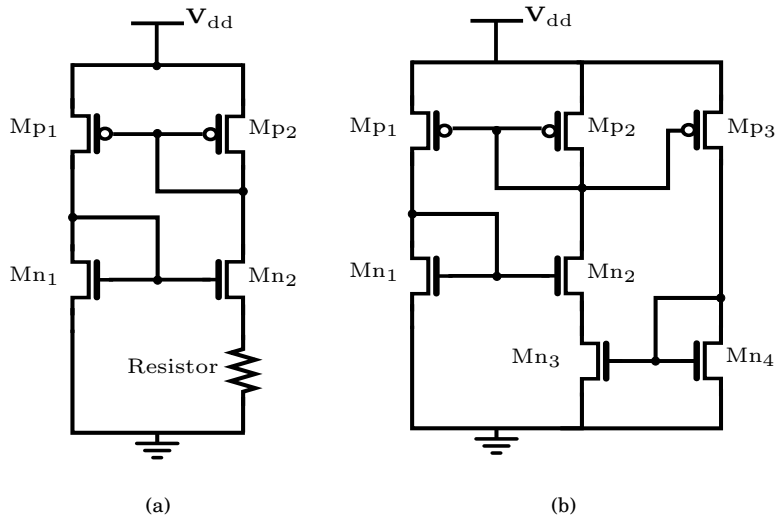


Figure 3.3. Schematics of (a) classical beta multiplier circuit and its (b) resistor-less implementation.

eliminated by using the MOSFET as shown in Fig. 3.3(b).

3.3.1.1 PTAT current generator

In the proposed voltage reference circuits, [105] is used to generate the PTAT current as shown in Fig. 3.1 and Fig. 3.2 respectively. The cascode-based implementation is preferred in the design, since poor PSRR is one of the shortcomings of [105]. The aspect ratio of the transistors (Mp_1 to Mp_8 and Mn_1 to Mn_4) was determined by following the design rules available in the literature [35] for a beta multiplier circuit. In the circuits (Fig. 3.1 and Fig. 3.2), the NMOS transistor Mn_5 is the MOSFET-based resistor hence it operates in a deep triode region. The gate-source voltage required by the transistor Mn_5 is provided by using the transistor Mn_6. It can be seen either in Fig. 3.1 or Fig. 3.2 that the NMOS transistor Mn_6 is in diode-connected configuration hence it operates in the saturation region.

Thus, the drain currents flowing through Mn_5 and Mn_6 can be given by:

$$I_{Mn_5} = \mu C_{OX} S_5 \left(V_{gs5} - V_{thn}\right) V_{ds5} \tag{3.6}$$

and

$$I_{Mn_6} = \frac{\mu C_{OX} S_6}{2} \left(V_{gs6} - V_{thn}\right)^2 \tag{3.7}$$

where μ is the mobility factor, C_{OX} is the gate-oxide capacitance of the MOSFET, $V_{gs}5$ and $V_{gs}6$ are the gate-source voltage of the transistors Mn_5 and Mn_6 respectively, S_5 and S_6 are the aspect ratios (width/length) of Mn_5 and Mn_6 respectively and V_{thn} is the threshold voltage of the NMOS transistor.

In the PTAT current generator circuit, an equal value of the current (I_p) was selected for each branch. Therefore, by equating (3.6) and (3.7) will result in:

$$S_5 \, V_{ds5} = \frac{S_6}{2} (V_{gs6} - V_{thn}) \tag{3.8}$$

In order to keep Mn_5 in the deep triode region, it is necessary that $V_{ds5} <<< 2 \left(V_{gs6} - V_{thn}\right)$ [35]. Hence, for manual calculations assume that:

$$V_{ds5} = \frac{|V_{gs6} - V_{thn}|}{3} \tag{3.9}$$

By substituting (3.9) in (3.8) will provide an empirical relationship between the aspect ratio of Mn_5 and Mn_6 as follows:

$$S_5 = 1.5 \, S_6 \tag{3.10}$$

The relationship shown in (3.10) is useful for a designer to obtain an initial guess of the aspect ratio for the transistors Mn_5 and Mn_6. It can be

seen in Fig. 3.4 that these transistors forms a closed-loop for the voltage-to-current conversion and vice-versa. For this reason, the random selection of the aspect ratio of these transistors will not initiate the loop and thus, it will result in extensive simulations to determine the aspect ratios.

The simulation-based illustration fixing the aspect ratio of the transistors as listed in Table. 3.2. The aspect ratio of the transistors Mn_5 and Mn_6 is selected using (3.10) and the aspect ratio of the remaining transistors are calculated using [35]. The width W_x of the transistor Mn_5 is selected as a degree of freedom.

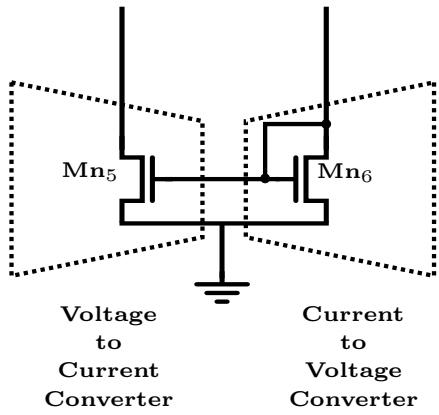


Figure 3.4. Voltage-current conversion loop formed by transistors Mn_5 and Mn_6.

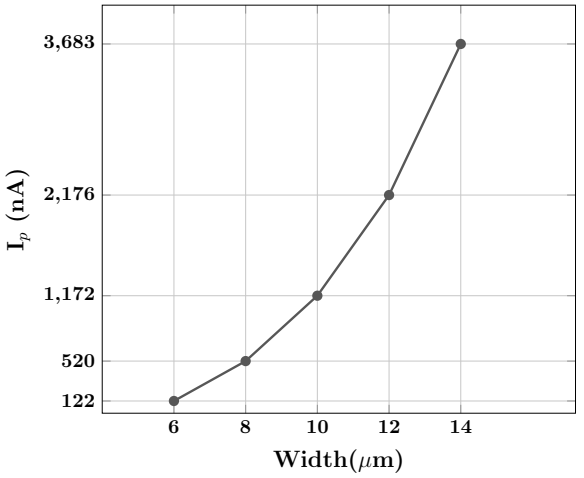
It can be observed in Table. 3.2 that the length for the transistors Mn_5 and Mn_6 is selected large. This selection will increase the current matching and reduce the harmonic distortion [118] between Mn_5 and Mn_6. It also will increase the ON-resistance (2.9) of Mn_5 and make it suitable for the nano-ampere current range.

Table 3.2. Transistors aspect ratios used in simulations.

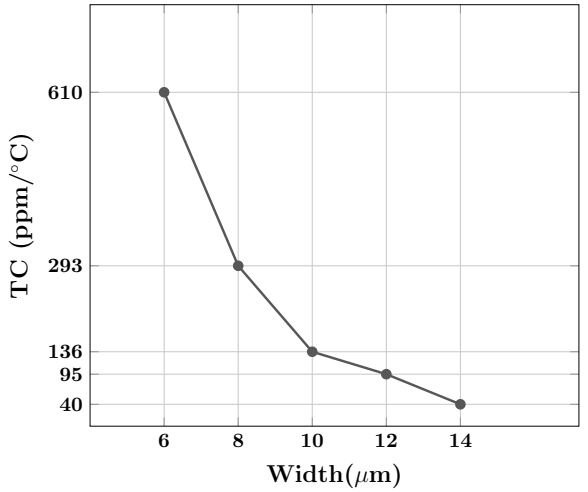
	Width	**Length**
Mp_1 to Mp_8	30μm	1μm
Mn_1 to Mp_3	10μm	1μm
Mn_4	40μm	1μm
Mn_5	W$_x$ μm	20 μm
Mn_6	2 μm	10 μm

The simulation results of the reference current and the temperature coefficient with respect to the width (W$_x$) of the transistor Mn_5 are shown

in Fig. 3.5(a) and Fig. 3.5(b). The simulations are performed at a supply voltage of 1.5 V for the temperature ranges from -40°C to +85°C. The temperature coefficient (TC) is calculated using (3.2).



(a)



(b)

Figure 3.5. Variation in the values of (a) current (I_p) at room temperature and its (b) temperature coefficient with increasing width.

It can be noticed in Fig. 3.5(a) that equation (3.10) is effective in finding an initial value of the aspect ratio. These plots also show the presence of an inverse relationship between the temperature coefficient and the current. Thus, decreasing the current values will result in an increasing temperature coefficient. This phenomenon was also present in [105].

3.3.1.2 Operating principle of voltage reference circuits I, II

Consider a circuit designed using a current source (I_x) and a diode-connected NMOS transistor as shown in Fig. 3.6.

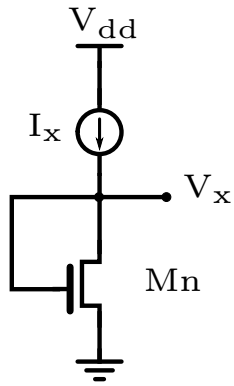


Figure 3.6. Simple diode-connected circuit.

The diode-connected NMOS transistor is operating in the saturation region. Hence, voltage V_x can be represented as:

$$V_x = V_{thn} + \underbrace{\sqrt{\frac{2L}{\mu C_{OX} W}}}_{M} \cdot \sqrt{I_x} \tag{3.11}$$

where W and L are the width and length of the transistor, and M represents the multiplying factor. In these implementations long length transistors are used hence the channel length modulation factor (λ) has been neglected during mathematical analysis. It is clear from (3.11) that the temperature behavior of V_x is a function of the temperature behavior of the threshold voltage V_{thn} and the current I_x flowing through the transistor. In this scenario, the temperature contribution of the mobility term (μ) is neglected. It is well defined in the literature that the threshold voltage decreases with the temperature [116]. Hence, the current I_x will become a dominant factor to control the temperature behavior of V_x. Thus, the resultant thermal behavior of V_x can be formulated as follows:

(i) If variation of I_x is independent of the temperature then V_x will have CTAT behavior with a voltage magnitude higher than the threshold voltage (3.12).

$$\underbrace{V_x(T)}_{CTAT} = \underbrace{V_{thn}(T)}_{CTAT} + constant \tag{3.12}$$

(ii) Similarly, if I_x exhibits CTAT behavior then it will result in CTAT

behavior in V_x.

$$\underbrace{V_x(T)}_{CTAT} = \underbrace{V_{thn}(T)}_{CTAT} + M \cdot \underbrace{I_x}_{CTAT} \tag{3.13}$$

It can be observed in (3.13) that the magnitude of the thermal gradient of V_x will be controlled by the multiplying term M. In the present case, the temperature variation due to the mobility term (μ) is neglected and therefore M is the temperature independent term.

(iii) Finally, if I_x is a PTAT current then the multiplying factor M will become the primary parameter which determines the PTAT or CTAT thermal behavior for V_x. Thus, for a given thermal slope of the PTAT current, V_x will have a positive thermal coefficient (PTAT) for higher values of M, while a negative thermal coefficient (CTAT) for lower values of M and, most importantly, V_x will become independent of the temperature for a certain value of M.

To validate the condition mentioned in (iii), the current I_x in Fig. 3.6 was obtained from the PTAT current generator shown in Fig 3.1. It should be noted that for these simulations the PTAT current generator was designed using the device parameters listed in Table. 3.2. The simulation-based results for a supply voltage (V_{dd}) =1.5 V in the temperature range of -40 °C to +85°C are shown in Fig. 3.7.

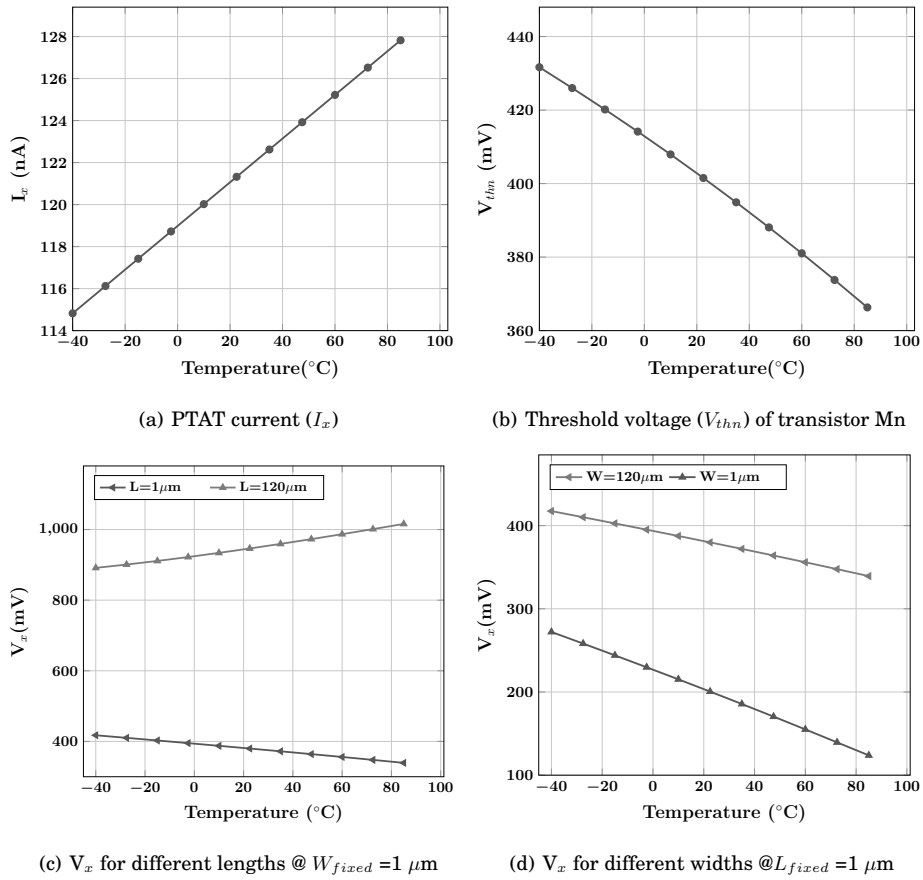
One of the important conclusions that can be drawn from Fig. 3.7(c) and Fig. 3.7(d) is that, in order to obtain the temperature independent behavior, a large size transistor (M_n) is required (Fig. 3.6), which is not favorable in terms of silicon area. Hence, as a solution to this issue, an alternate approach is required, which is shown in Fig. 3.8. Thus, by referring to Fig. 3.8 will result in:

$$V_x = \underbrace{V_{thn}}_{CTAT} + \underbrace{V_{PTAT} + \sqrt{\frac{2L}{\mu C_{OX} W}} \cdot \sqrt{I_x}}_{PTAT} \tag{3.14}$$

In this research, the primary target was to design a circuit that will generate V_{PTAT} voltage to obtain the temperature independent V_x. To achieve this aim two simple architectures were developed. The working operation of these architectures are briefly discussed as follows.

3.3.1.3 Architecture I

The conceptual schematic of architecture I of publication [**VI**] is shown in Fig. 3.9. In the circuit a composite transistor arrangement is formed by



(a) PTAT current (I_x)

(b) Threshold voltage (V_{thn}) of transistor Mn

(c) V_x for different lengths @ W_{fixed} =1 μm

(d) V_x for different widths @L_{fixed} =1 μm

Figure 3.7. Temperature dependent behavior of various circuit parameters.

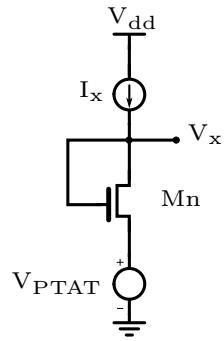


Figure 3.8. Alternate architecture to achieve temperature compensated voltage from a simple diode-connected circuit.

the NMOS transistors Mn_1 and Mn_2 to generate the PTAT voltage (V_{px}). This arrangement is a classical method of obtaining PTAT voltage [119]. In this circuit, the transistor Mn_1 is working in saturation and Mn_2 is in

the linear region and thus, the voltage V_{px} can be approximated as:

$$V_{px} = \frac{W\ I_x}{\mu\ C_{OX}\ L\ (V_x - V_{thn})} \tag{3.15}$$

where W and L are the width and the length of the transistor Mn_2. It can

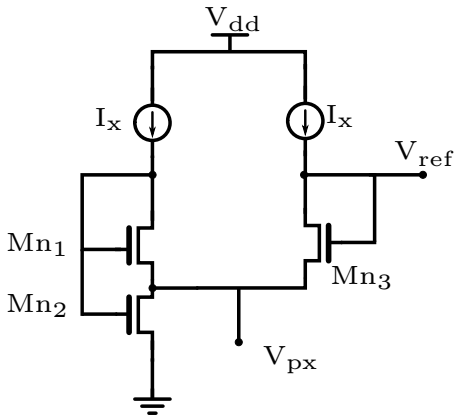


Figure 3.9. Conceptual schematic arrangement for voltage reference circuit I.

be observed in (3.15) that the temperature behavior of V_{px} is a function of I_x, V_{thn} and V_x. As mentioned earlier, I_x is the PTAT current source, V_{thn} and V_x decrease with the temperature. Hence, the use of these considerations in (3.15) will result in a positive thermal slope (PTAT) of the voltage V_{px}.

The PTAT voltage (V_{px}) obtained from the composite transistors is fed to the source terminal of the diode-connected NMOS transistor Mn_3 as shown in Fig. 3.9. As a result, the gate terminal voltage (V_{ref}) of Mn_3 will be compensated thermally (3.14).

Mathematically, it can be represented as in publication [**VI**]

$$V_{ref} = \underbrace{V_{thn}}_{CTAT} + \underbrace{\sqrt{\frac{2 \cdot I_x}{S_3 \cdot K_n}} + \sqrt{\frac{2 \cdot I_x}{K_n}} \cdot \left[2 \cdot \sqrt{\frac{S_2 + S_1}{S_2 \cdot S_1}} - \sqrt{\frac{1}{S_1}}\right]}_{PTAT(V_{px})} \tag{3.16}$$

where I_x is the reference current, V_{thn} is the threshold voltage, K_n is the transconductance parameter, S_1, S_2 and S_3 are the aspect ratio of transistors Mn_1, Mn_2 and Mn_3 respectively.

It can be noticed from equation (3.16) that the reference voltage V_{ref} is dependent on the aspect ratio of the transistors Mn_1, Mn_2 and Mn_3. Thus, for simplicity, the aspect ratio (W/L) of the transistors Mn_2, Mn_3 is selected as 1 μm/1 μm and the aspect ratio of Mn_1 was determined as 132 μm/1 μm. The simulation result of the voltage reference circuit (Fig. 3.1)

designed using these design parameters is shown in Fig. 3.10. It should be noted that the transistors sizes for the PTAT current (I_x) generator have been selected from Table. 3.2.

The simulations-based performance of this voltage reference circuit (Fig. 3.1) aimed at generating a reference voltage of 610 mV are available in [120].

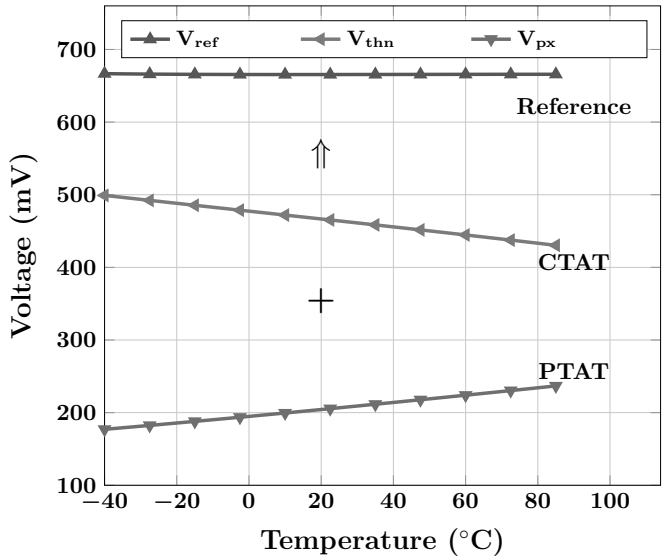


Figure 3.10. Simulation results for voltage reference circuit I.

3.3.1.4 Architecture II

Referring to the circuit arrangement of architecture I (Fig. 3.1), it can be observed that an additional current branch used for the transistor Mn_3 is contributing to increased power consumption of the circuit. As a solution to this issue, a simple circuit arrangement designed by stacking transistors with the diode-connected transistor to form a composite ladder structure was proposed in publication [**VII**]. The conceptual schematic arrangement for the proposed concept is shown in Fig. 3.11. In this architecture, the NMOS transistor Mn_1 is diode-connected and hence working in saturation while the remaining NMOS transistors (Mn_2...Mn_N) are in a linear region. It has been mentioned earlier that the diode-connected transistor will have a CTAT behavior while the transistors in the linear region will exhibit PTAT behavior. As a result the sum of these voltages will result in the temperature independent reference voltage (V_{ref}) as shown in (3.17):

$$V_{ref} = \underbrace{V_{ds1}}_{CTAT} + \underbrace{V_{ds2} + V_{ds3} + ... + V_{dsN}}_{PTAT} \tag{3.17}$$

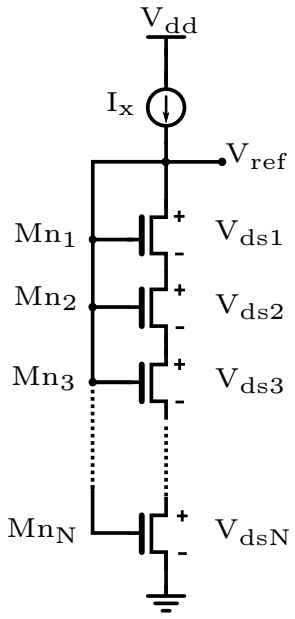


Figure 3.11. Conceptual schematic arrangement for voltage reference circuit II.

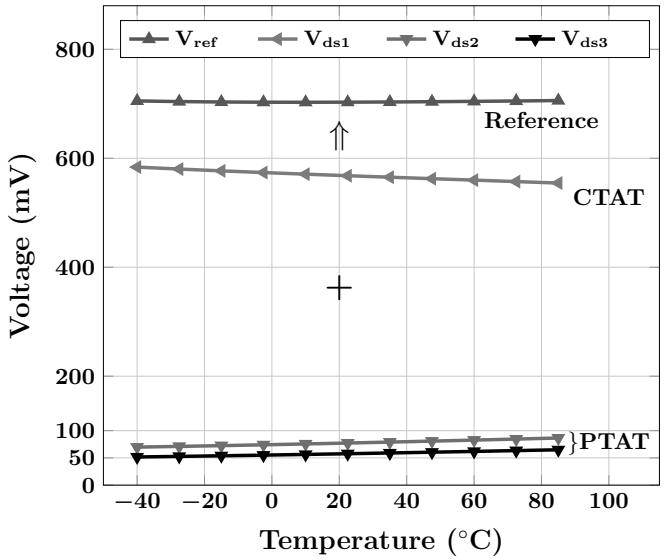


Figure 3.12. Simulation results for voltage reference II.

The simulation result of the voltage reference circuit (Fig. 3.2) is shown in Fig. 3.12. Here, a stack of three transistors (Mn_1,Mn_2 and Mn_3) was designed with the device dimension (W/L) of 1 μm/7 μm each and the aspect ratio of the transistors used in the PTAT current (I_x) generator implementation were selected from Table. 3.2. It can be observed in Fig.

3.12 that the sum of CTAT and PTAT voltages results in a temperature independent reference voltage.

The simulation-based analysis of this voltage reference circuit (Fig. 3.2) targeted at generating a reference voltage value of 595 mV is available in [121]. The performance summary of the proposed architectures publications **(VI, VII)** and comparison with state-of-the-art voltage reference circuits is listed in Table. 3.3. It can be observed in Table. 3.3 that the proposed architectures are capable of generating comparable temperature coefficients in the temperature range of -40°C to +85°C. Furthermore, the benefits include the smallest implementation area, a high PSRR and low noise density with low total power consumption (temperature compensation core and PTAT current generator).

Table 3.3. Performance comparison with state-of-the-art voltage reference circuits.

Ref.	**Tech.** (nm)	**Reference Voltage** (mV)	**Supply Voltage** (V)	**Operating Temp.** (°C)	**TC** (ppm/°C)	**Power Dissipation** (μW)	**PSRR** (dB)	**Line Sensitivity**	**Noise Density** ($\mu V/\sqrt{Hz}$)	**Area** (mm^2)
[122]	350	745	1.4 to 3	-20 to 80	7	0.3 (min)	-45 @100 Hz	20 ppm/V	-	0.055
[123]	500	487.6	1.2 to 3.2	-40 to 110	8.9	48 (min)	-58	2.4mV/V	-	0.1
[124]	500	337	0.96 (min)	10 to 100	9.9	73.8 (min)	-	290 ppm/V	-	0.3234
[125]	350	670	0.9 to 4		10	0.036(min)	-47 at 10Hz	0.27%/V	-	0.045
[126]	250	650	2.8	0 to 100	10.4	138.6	-53 at 100Hz	-	-	0.011
[127]	350	635	0.9 to 3.5	5 to 95	12.1	14.94 (min)	-47.6	3.5 mV/V	-	0.0590
[128]	180	620	1.2 to 3	-20 to 80	12.9	0.168 (min)	-68	-	6	-
[129]	350	905.5	1.85 to 3.3	0 to 100	14.8	214.5(max)	-61@100 Hz	-	-	0.01
[130]	180	767	1.2 to2	-40 to 120	15.9	43.2(min)	-	0.054mV/V	-	0.036
[VI]	180	543.65	1.25 to 2	-40 to 85	17.43	1.5 (max)	-62.24 @ 100Hz	1.642 mV/V	20.54	0.007
[VII]	180	536.02	1.25 to 2	-40 to 85	19.3	0.48 (max)	-55 at 10Hz	2.217 mV/V	12.28	0.0077
[131]	90	497.2	1 to 1.5	-40 to 80	28.3	331.92(min)	-	-	-	0.0337
[132]	500	765	2 to 5	0 to 100	39.2	16.48(min)	-	0.817%/V	-	0.014
[133]	130	781	1 to 2.3	0 to 100	48	8.1 (min)	-51.4	0.34%/V	-	0.053
[113]	350	847.5	1.1 to 3.3	-20 to 80	394	0.11	-	0.45%/V	-	0.21

3.3.2 Current reference circuit

The current reference circuit is an indispensable component of any mixed signal design used to provide stable biasing condition. Various design implementation methods for the current reference circuit are available in literature. These methods are broadly classified into two parts. First, are the designs based on the bandgap principle. In these implementations, a reference current is obtained either by converting bandgap voltage into current, or by using ON-chip resistors and BJTs for circuit designing [134–138].

Second are CMOS-based implementations. In these designs two concepts are most commonly utilized: the first approach is to obtain the reference current by combining the PTAT and the CTAT currents [90], [139]. While in the second approach, classical beta-multiplier architecture is used as a base circuit to obtain the reference current [117], [140].

In beta-multiplier-based designs, the resistor is a controlling parameter for the layout area, temperature coefficient, and reference current values. Later, this limitation was removed in [105] by replacing the resistor with MOSFET. Various current reference circuits based on [105] are available in the literature to obtain a nano-ampere current range [141], [142]. In [105] three shortcomings were reported namely, a low PSRR, a high temperature coefficient and a large spread.

The circuit arrangement of [105] is shown in Fig. 3.13. In this circuit, cascode configuration in a PMOS transistor is used to improve PSRR performance. The design implementation details of this architecture has been already discussed in section.3.3.1.1 above. It was also shown by using simulations that the temperature coefficient increases with a decrease in the reference current value (Fig. 3.5(b)). It has been observed during simulations that the high temperature coefficient is the result of unequal thermal slopes of the gate-source voltage (V_{gs3}) of the MOSFET resistor Mn_3 with its threshold voltage (V_{thn}). By applying KVL in the loop formed by the NMOS transistors Mn_3 and Mn_4 (Fig. 3.13):

$$V_{gs3} = V_{gs4} \tag{3.18}$$

Since Mn_4 is a diode-connected configuration and hence operating in the saturation region (3.18) can be therefore rewritten as:

$$V_{gs3} = V_{gs4} = V_{thn} + \sqrt{\frac{2 \cdot I_{ref}}{\mu C_{OX} S_4}} \tag{3.19}$$

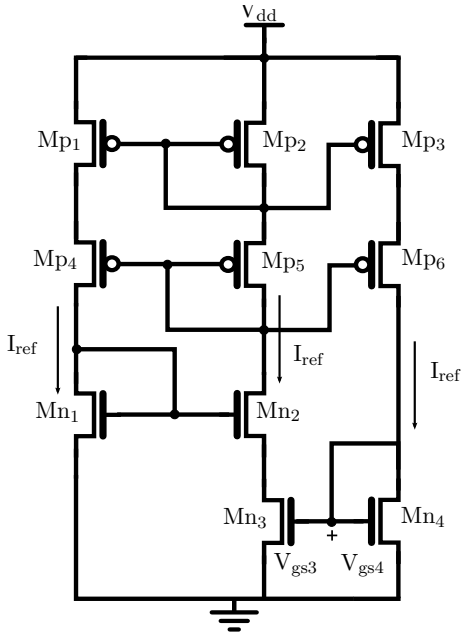


Figure 3.13. Conventional current reference circuit.

where S_4 is the aspect ratio of Mn_4. Differentiating (3.19) with respect to the temperature (T) and using [116] will result in:

$$\left[\frac{dV_{gs3}}{dT} - \frac{dV_{thn}}{dT}\right] = \frac{K_1\sqrt{(I_{ref})}}{2}\left(\frac{T}{T_0}\right)^{m/2}\left[\frac{1}{I_{ref}}\frac{dI_{ref}}{dT} + \frac{m}{T}\right] \tag{3.20}$$

where K_1 is given by

$$K_1 = \sqrt{\frac{2}{\mu(T_0)C_{OX}S_4}}$$

and rearranging (3.20)

$$TC|_{I_{ref}} = \frac{2}{K_1\sqrt{I_{ref}}}\left(\frac{T}{T_0}\right)^{-m/2}\left[\frac{dV_{gs3}}{dT} - \frac{dV_{thn}}{dT}\right] - \frac{m}{T} \tag{3.21}$$

It can be observed in (3.21) that the temperature coefficient (TC) of I_{ref} ($TC|_{I_{ref}}$) is a function of the thermal gradient of V_{gs3} and V_{thn}. Here, V_{gs3} is the circuit based parameter hence, if

$$\frac{dV_{gs3}}{dT} = \frac{dV_{thn}}{dT} \tag{3.22}$$

then, by substituting (3.22) in (3.21) will reduce TC of I_{ref} to:

$$TC|_{I_{ref}} = -\frac{m}{T} \tag{3.23}$$

The value of m lies between 1 to 2 and T is in °K hence, numerically TC of I_{ref} will become small.

The simulated variation of V_{gs3} and V_{thn} with respect to temperature are shown in Fig. 3.14. These simulations were performed for the reference current value of 80 nA at a supply voltage of 1.25 V. It can be observed from Fig. 3.14 that the thermal slopes of V_{gs3} and V_{thn} are not equal. They are reducing at the rates of $\approx$ 0.196 mV/°C and $\approx$ 0.522 mV/°C respectively.

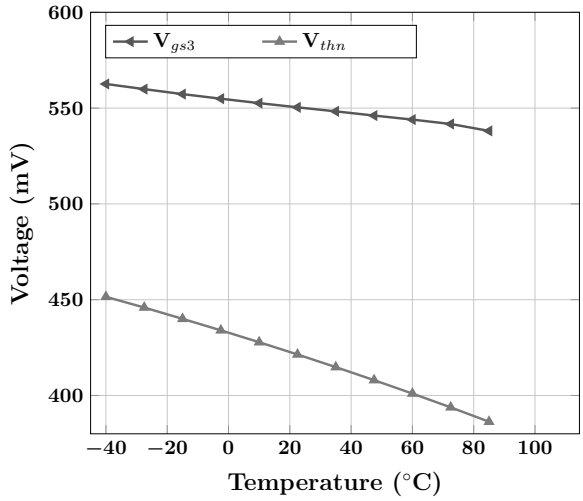


Figure 3.14. Simulated temperature behavior of V_{gs3} and V_{thn}.

This issue of the high temperature coefficient of [105] due to thermal slope inequality was addressed and solved in this part of the research. As a solution, a simple extension circuit is proposed. This circuit is designed by using the NMOS transistors Mn_5 to Mn_7 as shown in Fig. 3.15.

By applying KVL in the loop formed by the NMOS transistors Mn_3, Mn_4 and Mn_7 and differentiating with respect to the temperature (T), the following is obtained:

$$\frac{dV_{gs3}}{dT} = \frac{dV_{gs4}}{dT} + \frac{dV_{ds7}}{dT} \tag{3.24}$$

Referring to the theory explained in section.3.3.1.4 for a composite transistor array, it is known that the drain-source voltage of the array transistors has the PTAT behavior (Fig. 3.12) and its slope is a function of the aspect ratio of the transistor. Hence, to adjust the thermal slope of V_{gs3}, the aspect ratio of the transistors used in the composite array is an important design parameter.

The simulation results obtained by changing the width of the composite transistor are shown in Fig. 3.16. In these simulations, it has been considered that the channel length of the transistors is 1 μm. The purpose

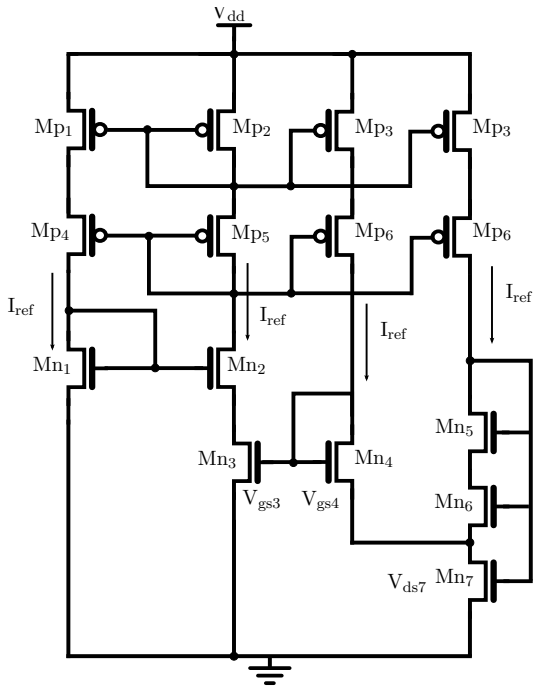


Figure 3.15. Schematic of the proposed current reference circuit.

of this simulation was to determine the width of the transistors used in the composite array for which the thermal slope of V_{gs3} achieves the "Target thermal slope" of $\approx$ 0.522 mV/°C. It can be observed from Fig. 3.16 that the thermal slope of V_{gs3} increases rapidly for lower values of width ($\leq$7μm). On the contrary, for the higher values of width (>7μm)) the increase in thermal slope has become sluggish as it approaches near the "Target thermal slope" value. The value of the thermal slope that was used in the implementation for V_{gs3} is $\approx$ 0.424 mV/ °C.

A brief summary of simulations-based comparison of the proposed current reference circuit with [105] is given in Table. 3.4. A more detailed simulation-based comparison is available in [143].

The measured performance summary of publication [**VIII**] and the comparison with state-of-the-art current reference circuits is listed in Table. 3.5. It can be seen in the table that the proposed current reference circuit is capable of generating a current value less than 100 nA with a comparable temperature coefficient in the temperature range of -40 °C to 85 °C. The proposed architecture uses the smallest area of all the state-of-the-art current reference circuits. The total power consumption of this architecture is 0.67 μW at a supply voltage of 1.5 V. This power consumption

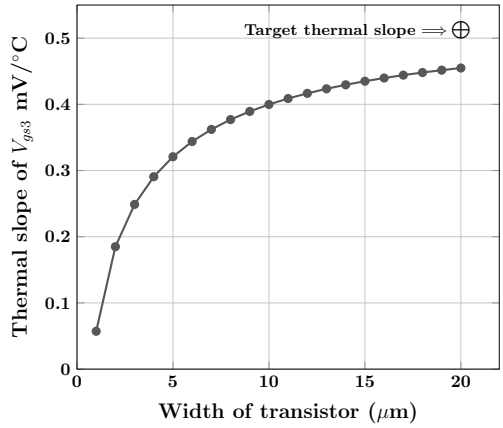


Figure 3.16. Variation of thermal slope of V_{gs3} with respect to width of composite array transistors.

Table 3.4. Simulation-based performance comparison.

Parameter	**Proposed** [143]	**Conventional** [105]	**Remark**
Reference Current	80 nA		-
Temperature	-60 to 85 °C		-
Supply Voltage (V)	1.25 to 2		-
TC (ppm/°C)	39.8	545.1	92 % ↓
Power Dissipation (nW) (max)	624.8	468.59	25 % ↑

can further be reduced by changing the amount of current flowing into the mirroring branches. The only shortcoming of the circuit is poor line sensitivity which is 7.5 %/V. This has appeared due to the high supply sensitivity of the voltage V_{ds7} (Fig. 3.15). One of the solutions for overcoming this limitation is the use of a voltage regulator circuit. This solution will come with an additional power dissipation and a large implementation area.

Table 3.5. Performance comparison of proposed current reference circuit with state-of-the art current reference circuits.

Ref.	Tech (μm)	Supply Voltage (V)	Operating Temp. (°C)	Reference Current (nA)	TC (ppm/°C)	Line Regulation (%/V)	Power Dissipation (μW)	Area (mm^2)	Remark
[144]	0.35	>1.5	0 to 80	9.14	44	0.569	0.109 @ 3V	0.035	Measurement
[90]	0.35	1.3 to 3	-20 to 80	9.95	1190	0.46	0.088 @ 1.3V	0.12	Measurement
[122]	0.35	1.4 to 3	-20 to 80	36	2200	0.002	0.3 @ 1.5V	0.06	Measurement
[145]	0.25	1.2 to 3.6	-40 to 150	50	263.1†	±0.32	-	0.018	Measurement
[146]	0.35	5	0 to 80	50	128	15%/100 mV	57 @ 5V	0.005824	Measurement
[VIII]	0.18	1.25 to 1.8	-40 to 85	92.3	176.91	7.5	0.67 @1.5V	0.0013	Measurement
[142]	0.35	1.8 to 3	-20 to 100	92.7	288	0.0150 %†	0.811@ 2.5	-	Simulation
[147]	0.35	1.8 to 3	-20 to 100	94.9	523	0.178†	0.586 @1.8 V	0.055	Simulation
[148]	0.35	1.8 to 3	0 to 80	96	520	0.2	1 @ 1.8V	0.015	Measurement
[141]	0.25	1.5 to 3	-20 to 100	97.7	±334†	-	1 @ 1.5V		Simulation
[105]	2	≥1.2	-40 to 80	1 to 100	1100	10	0.07 @ 2.3V	0.06	Measurement
[149]	0.18	>1.2	-40 to 120	500	119	0.6910	1.98 @ 1.2V	-	Simulation
[150]	3	>3.5V	0 to 80	774	375	0.013	10 @ 5V	0.2	Measurement
[151]	0.18	>0.7	-25 to 75	940	29	2.6	5.32 @ 0.7V	0.002	Simulation
[152]	0.18	>1	-40 to 120	1000	231	0.6530	2 @ 1V	0.00785	Simulation

† Calculated from the statistics shown in the article

3.3.3 Frequency reference circuit

High precision clock generation is an important requirement for a majority of digital circuits. Conventionally, a quartz crystal oscillator is used for reference clock generation, but ON-chip integration with a CMOS system is not feasible [153]. An LC oscillator is used as a substitute due to its phase noise performance but the implementation of an inductor requires a large chip area [154], [155], [156]; however the recent scaling trend of sensor node restricts the use of an LC oscillator [157]. Therefore, to meet lower power consumption, small size and high frequency stability for the timing reference, the RC-based [158], [159] or ring oscillator [160] [161] based implementation is a recommended solution. In practice, RC-based oscillators have higher sensitivity towards process and temperature variations. Therefore, additional circuits are required to compensate these variations [162] [163].

Generally, a ring oscillator based implementation is selected due to its scalability for integration [164]. Like other architectures, a ring oscillator also exhibits high sensitivity towards process, temperature and power supply [165], [166].

The aim of the proposed work was to implement the principle of the phenomenon of the reversal of temperature dependence in order to obtain a temperature independent frequency from a ring oscillator circuit. Apart from this principle, various temperature compensation methods for ring oscillator are already proposed in the literature, for example, the use of the PTAT current [167], CTAT current [168] and reference circuit [161],[169].

3.3.3.1 Principle of reversal of temperature dependence

The successful implementation of any temperature insensitive circuit depends upon the thermal properties of the constituting electronic devices. In a MOSFET-based circuit implementation, the thermal properties of the threshold voltage V_{th}(T) and the carrier mobility in the channel region μ(T) are of great importance. The simplified model describing the temperature dependency of these parameters are as follows [170]:

$$V_{th}(T) = V_{th}(T_0) - \beta_{th}(T - T_0) \tag{3.25}$$

$$\mu(T) = \mu_0(T_0) \left(\frac{T}{T_0}\right)^{-\beta_\mu} \tag{3.26}$$

where β_{th} and β_μ are the thermal sensitivity of the threshold voltage (V_{th}) and the mobility (μ) of the MOSFET. According to these formulas, both

the threshold voltage and the mobility decreases with increasing temperature.
Considering the drain current model proposed in [171], [172] for MOSFET in a sub-micron process

$$I_{ds} = \frac{\mu\, C_{OX}\, W}{2\, L}\,(V_{gs} - V_{th})^{\alpha} \begin{cases} \alpha = 1 \text{ for short channel device} \\ \alpha = 2 \text{ for long channel device} \end{cases} \tag{3.27}$$

where α represents the velocity saturation index. Substituting (3.25) and (3.26) in (3.27) yields

$$I_{ds} = \mu_0(T_0)\left(\frac{T}{T_0}\right)^{-\beta_\mu}[(V_{gs} - V_{th}(T_0) + \beta_{th}(T - T_0)]^{\alpha} \tag{3.28}$$

and differentiating (3.28) with respect to temperature (T) will result in:

$$\begin{aligned}\frac{dI_{ds}}{dT} &= \mu_0(T_0)\left(\frac{T}{T_0}\right)^{-\beta_\mu - 1}\left(\frac{-\beta_\mu}{T_0}\right)[(V_{gs} - V_{th}(T_0) + \beta_{th}(T - T_0)]^{\alpha} + \\ &\quad \mu_0(T_0)\left(\frac{T}{T_0}\right)^{-\beta_\mu}\alpha\beta_{th}\,[(V_{gs} - V_{th}(T_0) + \beta_{th}(T - T_0)]^{(\alpha-1)}\end{aligned} \tag{3.29}$$

The value of the voltage V_{gs} at the nominal temperature (T_0) for which the thermal sensitivity of the drain current I_{ds} will equal to zero is shown in (3.30).

$$V_{gs}|_{T_0} = V_{th}(T_0) + \frac{\alpha\beta_{th}T_0}{\beta_\mu} \tag{3.30}$$

In order to validate equation (3.30), the transfer characteristics ($\sqrt{I_{ds}}$ v/s V_{gs}) of the NMOS transistor at different temperatures are shown in Fig. 3.18. These characteristic plots are obtained using the circuit setup shown in Fig. 3.17 for a transistor of size W/L = 0.5 μm/ 0.18 μm.

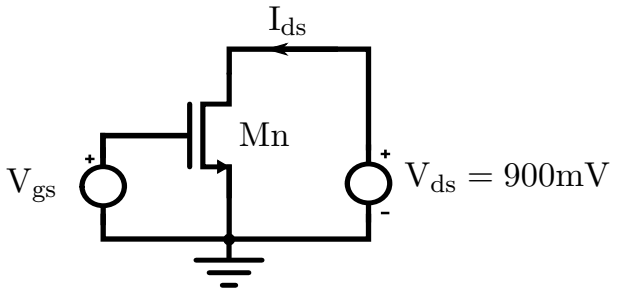


Figure 3.17. Circuit setup to plot transfer characteristics of NMOS transistor.

It can be observed in Fig. 3.18 that for lower values of V_{gs}, the temperature dependency of the plots exhibit CTAT behavior: for a low value of V_{gs} the current sensitivity towards threshold voltage increases. Basically, at

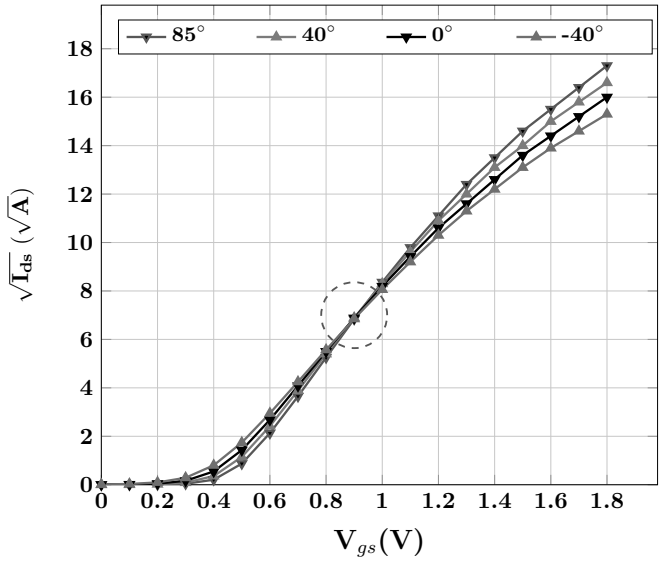


Figure 3.18. Transfer characteristics of NMOS transistor at different temperatures.

high temperature the small value of the threshold voltage increases the current sensitivity, but on the other hand lower mobility values will decreases its value. Thus, for a certain value of V_{gs} these effects will cancel each other and hence the current I_{ds} will become independent of the temperature. The value at which this phenomenon occurs is highlighted in Fig. 3.18. The temperature dependency of the characteristic plots become PTAT with an increase in V_{gs} voltage. This is due to the fact that in the higher voltage range ($V_{gs} >> V_{th}$), the threshold voltage has a small effect in comparison to the mobility over the drain current (I_{ds}).

Fig. 3.18, verifies the principle that was explained in [173]. According to this principle, the temperature dependent performance of a circuit degrades with a reduction in the supply voltage. Eventually, this phenomenon reverses into a performance improvement for a certain lower supply voltage value [173].

Based on the above analysis, the temperature and supply voltage dependency has been investigated in a three-stage ring oscillator. The simulation results are shown in Fig. 3.19. The inverters used to design the ring oscillator are selected from a standard library of the design kit. The transient simulations were performed for the supply voltage ranging from 0.6 V to 1.8 V in steps of 0.1 V. For each selected supply voltage the frequency was calculated in the temperature range of -40°C to 85°C. The percentage change in frequency with the supply voltages are shown in Fig. 3.20. It can be noticed from the simulation results that for the supply voltage

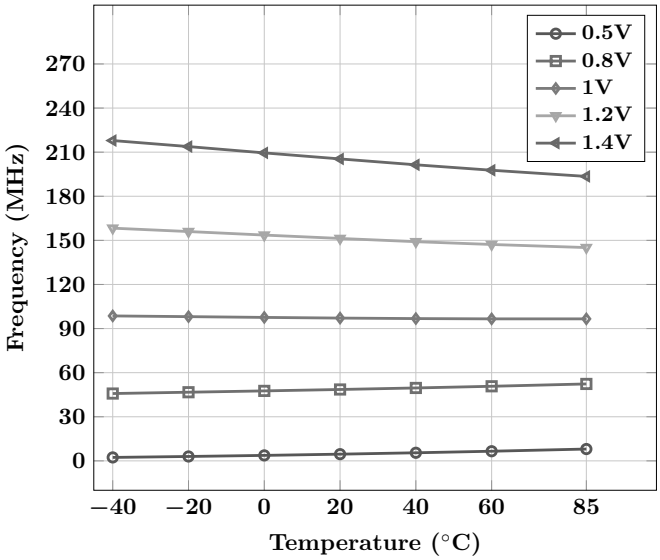


Figure 3.19. Variation of oscillation frequency with temperature for selected supply voltage values.

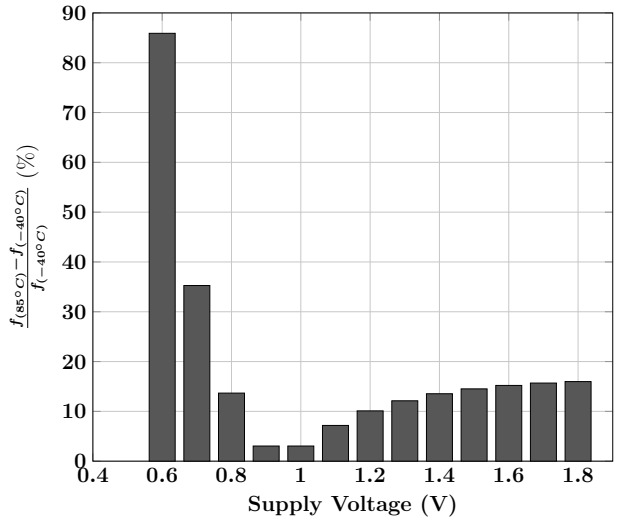


Figure 3.20. Percentage change in frequency with supply voltage.

ranging from 0.8 V to 1.1 V, the percentage change in frequency is minimum. Hence, referring to the theory explained above these voltage values can be referred to as the bias points where the principle of the reversal of the temperature dependence is functional.

Thus, apart from the conventional methods available in the literature, this simple method was used to obtain the temperature compensation in publication [**IX**]. The system model of publication [**IX**] consists of two

parts, the bias circuit and the oscillator. The bias circuit is a self-biasing V_{th} reference current source [174] to provide a biasing current to the ring oscillator based core.

In general, the delay of an inverter is given as [175]:

$$t_d \, \alpha \, \frac{C_L \, V_{dd}}{I_d} \tag{3.31}$$

where C_L is the load capacitance, V_{dd} is the supply voltage and I_d is the drain current. Using equation (3.28) in (3.31) and differentiating with respect to temperature (T), the temperature sensitivity of the delay (t_d) can therefore be represented as follows:

$$\frac{\partial t_d}{\partial T} \, \alpha \, \frac{1}{\left(\frac{T}{T_0}\right)^{\beta_\mu} (V_{dd} - V_{th})^{\alpha}} \left[\left(\frac{\beta_{th}}{(V_{dd} - V_{th})} \right)_{\textbf{(a)}} - \left(\frac{\beta_\mu}{T_0} \right)_{\textbf{(b)}} \right] \tag{3.32}$$

where β_μ is the temperature independent constant for the mobility term μ, β_{th} is the slope of the threshold voltage V_{th}, T and T_0 are the ambient and nominal temperature respectively and V_{dd} is the supply voltage. It can be observed in (3.32) that the temperature behavior of the delay t_d is a function of the term (**a**) and the term (**b**). Thus, three operation modes depending on the relative values of the terms (**a**) and (**b**) can be noticed, which are as follows:

1. When the term (**a**) $<$ (**b**) the delay t_d will exhibit CTAT behavior

2. When the term (**a**) $>$ (**b**) the delay t_d will exhibit PTAT behavior

3. When (**a**)=(**b**) the delay t_d will be independent of the temperature

The above stated three phenomena can be easily noted in Fig. 3.19 and Fig. 3.20. The performance summary and the comparison of the proposed frequency reference with the state-of-the-art frequency reference circuits are listed in Table. 3.6. The proposed architecture generates a reference frequency of 355 KHz with the temperature coefficient of 121.90 ppm/°C with a small implementation area. The figure of merit of the proposed architecture is high compared to the majority of the state-of-the art circuits. This measured result proves the effectiveness of supply voltage as an important degree of freedom in the designing of frequency reference circuits. However, an adaptation of the voltage regulation circuit will increase the area and the power dissipation.

Table 3.6. Performance comparison of proposed frequency reference with state-of-the-art frequency reference circuits.

Ref.	**Tech. (nm)**	**Supply Voltage** (V)	**Operating Temp.** (°C)	**Reference frequency (KHz)** (f_{ref})	**TC (ppm/°C)**	**Power dissipation** (μ**W**)(P)	**Frequency Variation**	**Area** (mm^2)	**FOM (dB)** $10 \cdot \log(f_{ref}/P)$	**Arch.**
[176]	180	1.5 to 3.63	-40 to 85	32.768	$\pm 0.024^{\dagger}$	1.5(min)	$\pm$3ppm	1.375	104	MEMS
[177]	180	1.8	-40 to 85	27	$\pm 0.032^{\dagger}$	3.6	$\pm$4ppm	1.14	99	MEMS
[178]	130	-	20 to 70	100	14	1	0.126% †	-	110	RO
[179]	60	1.6 to 3.2	-20 to 100	32.768	32.4	4.48	0.388% †	0.048	99	RXO.
[180]	180	0.8 to 1.8	-40 to 120	6.66	56	0.9	0.896% †	0.09	99	RXO.
[181]	90	0.6	-25 to 125	200	$\pm 33.33^{\dagger}$	48	$\pm$0.5%	0.04	97	RO
[182]	90	0.725 to 0.9	-40 to 90	100	$\pm 76.92^{\dagger}$	0.28	$\pm$1%	0.12	116	RXO.
[183]	65	1.2	-22 to 85	100	$\pm 113^{\dagger}$	40.8	$\pm$1.1%	0.11	94	RXO.
[184]	180	1 to 1.8	-40 to 100	32.55	120	0.472	1.68% †	0.105	109	RXO.
[**IX**]	180	1	-40 to 85	355	121.90	2.3	1.53%	0.0638	112	RO
[185]	90	1.5 to 5.5	-40 to 125	50	$\pm 133^{\dagger}$	1.28	$\pm$2.2%	0.03	106	RXO.
[163]	130	1	-40 to 80	1200	-296	5.8	$\pm$1.8 %	0.016	114	RC
[186]	BiCMOS	2 to 3	-40 to 150	100	$736^{\dagger}$	4.5	14%	0.1	104	RXO.
[187]	350	$>$1	0 to 80	80	842	1.14	6.73% †	0.24	109	RC
[188]	350	1.25	-25 to 80	200	1000	1001	10.5% †	0.032	84	RO

† Calculated from the statistics shown in the article. RO=Ring Oscillator, RXO= Relaxation Oscillator

3.4 Summary

This chapter presented the research work done in the field of reference circuit design, including the designing of voltage, current and frequency reference circuits. The chapter started with a description of performance evaluation parameters required for any reference circuits. Basic design strategies were also listed to obtain high-performance reference circuits as these circuits have become a key factor in the design of modern systems.

The detailed design implementations of two different voltage reference circuits publications [**VI**], [**VII**] were discussed. When compared to the conventional voltage reference architectures available in the literature, these structures offer simplicity in integration with a smaller silicon area. As a result, they can be easily deployed wherever voltage reference circuits are demanded. Other benefits included are low power consumption, a comparable temperature coefficient, a higher PSRR and lower line sensitivity when compared to state-of-the-art voltage reference circuits.

The detailed designed implementations of two different temperature compensation circuits were discussed. The current reference circuit publication [**VIII**] proposed in this work is based on the classical resistorless beta multiplier. Here, a simple extension circuit was proposed, which when used with a classical structure will result in a 68% lower temperature coefficient. The proposed current reference circuit generates a nanoampere reference current, with a comparable power dissipation, moderately high line regulation and the lowest silicon area when compared to state-of-the-art current reference circuits which are available in literature.

Lastly, a classical principle of the reversal of the temperature behavior was implemented to obtain the reference frequency. The aim of this research has been to demonstrate the utility of the supply voltage as an important design parameter for obtaining temperature compensation in the oscillator circuits. The measured results show that the proposed architecture publication [**IX**] is capable of generating the reference frequency with a variation less than 2% over the commercial temperature range and maintaining a comparable Figure Of Merit (FOM) compared to other architecture available in the literature. However, the implementation of this principle in the oscillator requires for an exclusive voltage regulation circuit, which can be considered as a key limiting factor.

4. Temperature Sensors

4.1 Overview

Temperature measurement is well known from the era of Galileo. The classification of the temperature measuring instruments and sensors by the measuring range is well documented in the literature [189], [190]. Every year, various smart electronic devices with smaller sizes and higher performance are entering the global marketplace [191]. Various challenges must be faced due to these tighter ON-chip integration requirements [192] [193]. One of which is a high power density profile which increases with the decrease in size, and with the increase in performance [194–196]. Hence, to restrict performance deviation due to power density an ON-chip thermal management module is required. A substantial amount of research in the development of ON-chip temperature sensors is on going. Temperature sensors are broadly classified into two categories; first, BJT-based and second, MOSFET-based.

The BJT-based temperature sensors are the preferred choice since they measure temperature accurately within $\pm 0.2^{\circ}$C over the military temperature range (-55°C to 125 °C) [197] [198]. In a BJT-based implementation, the dependence of the base-emitter (V_{be}) voltage over temperature is used for sensing temperature. Conceptually, three diode-connected PNP transistors are used to generate ΔV_{be} and V_{be}. The ΔV_{be} is amplified and combined with V_{be} to provide an input and reference to an ADC. The output of the ADC is the ratio between these two parameters [198].

However, BJT-based temperature sensors require a higher supply voltage and area, which cannot be scaled with the process technologies [199]. Therefore, the temperature sensing trend is focusing more towards designing MOSFET based temperature sensors. Like BJT, MOSFET-based

temperature sensors are also capable of sensing temperature with an accuracy of $\pm 0.2^{\circ}$C [200]. Several MOSFET-based ON-chip temperature sensing mechanisms have been reported in the literature. These schemes are broadly classified under three circuits-based implementation strategies: first, the temperature is sensed in terms of the PTAT/ CTAT voltage [201–203] or current [204],[205]; the second method is time-domain temperature sensing which generate a temperature-dependent delay [206–208]; using the third method, temperature is expressed in terms of the frequencies [209], [210].

4.2 Proposed temperature sensing methods

In this research work, all MOSFET-based temperature sensors are proposed. These sensors generate temperature equivalent Proportional to Absolute Temperature (PTAT) voltage, Complementary To Absolute Temperature (CTAT) voltage and PTAT current signals respectively. A brief summary of these temperature sensors is discussed as follows.

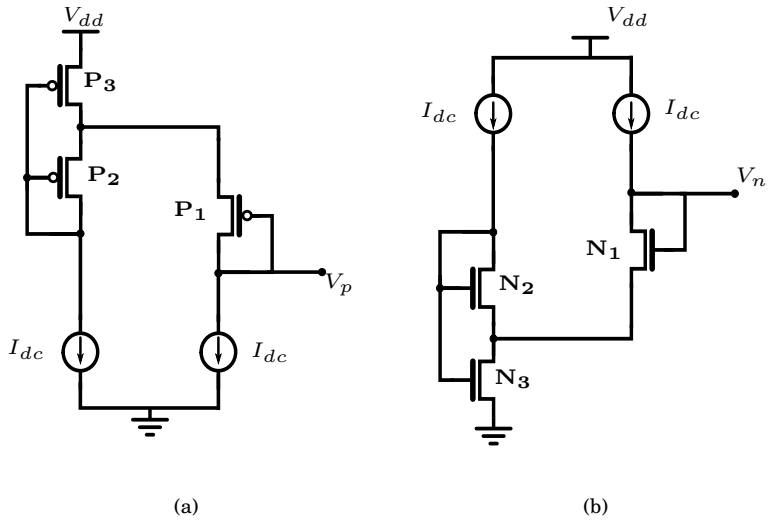
4.2.1 Voltage-based temperature sensor

In this work, two MOSFET temperature sensor cores were designed which generate the PTAT and CTAT voltage equivalent of temperature [201]. These sensors use the temperature-dependent behavior of the MOSFET threshold voltage [170]. The circuit arrangement of these sensors is the same as the circuit proposed to generate the reference voltage as shown in Fig. 3.9. The primary difference lies in the biasing conditions and the aspect ratio of the transistors to be used as the sensor core. The designs were made complementary to each other to obtain CTAT and PTAT voltage signals as shown in Fig. 4.1(a) and Fig. 4.1(b) respectively. In Fig. 4.1, $N1$ ($P1$) to $N3$ ($P3$) are NMOS (PMOS) transistors and I_{dc} represents the DC current. In the circuits transistors $N1$ ($P1$) and $N2$ ($P2$) operate in the saturation region while $N3$ ($P3$) is in the linear region of operation.

Considering a CTAT voltage generator (Fig. 4.1(b))) and apply KVL in a loop formed by $N1$ to $N3$. The voltage V_n can be expressed as:

$$V_n = V_{ds1} + V_{sd2} + V_{gs3} \tag{4.1}$$

where V_{ds1}, V_{sd2} are the drain-source voltage of the transistors N_1, N_2 respectively, while V_{gs3} is the gate-source voltage of the transistor N_3. The transistor N_3 is in the linear region hence the current flowing through it



(a) (b)

Figure 4.1. Circuit arrangements to generate PTAT and CTAT voltages.

will be given by:

$$2I_{dc} = \beta_n S_{N3}\left[(V_{gs3} - V_{thn})V_{ds3} - \frac{V_{ds3}^2}{2}\right] \tag{4.2}$$

where β_n is the transconductance parameter, V_{gs3} is the gate-source voltage, V_{ds3} is the drain-source voltage, V_{thn} is the threshold voltage and S_{N3} is the aspect ratio of the transistor $N3$ respectively. Similarly, by applying KVL in the loop formed by the transistors $N2$ and $N3$:

$$V_{gs3} = V_{ds2} + V_{ds3} \tag{4.3}$$

Since the transistors $N1$ and $N2$ are working in the saturation region therefore:

$$V_{ds1} = V_{thn} + \sqrt{\frac{2I_{dc}}{S_{N1}\beta_n}} \tag{4.4}$$

$$V_{ds2} = V_{thn} + \sqrt{\frac{2I_{dc}}{S_{N2}\beta_n}} \tag{4.5}$$

where S_{N1} and S_{N2} are the aspect ratio of the transistors N_1 and N_2 respectively. Using equations (4.2) to (4.5) in (4.1) will result in the following:

$$V_n = \underbrace{V_{thn}}_{(\mathbf{a})} + \underbrace{\left[\sqrt{\frac{1}{S_{N1}}} + \sqrt{\frac{S_{N3}+2S_{N2}}{S_{N3}S_{N2}}} - \sqrt{\frac{1}{S_{N2}}}\right]}_{(\mathbf{b})}\underbrace{\sqrt{\frac{2I_{dc}}{\beta_n}}}_{(\mathbf{c})} \tag{4.6}$$

Similarly, the expression for V_p can be derived as:

$$V_p = \underbrace{V_{dd}}_{(\mathbf{b1})} - \underbrace{V_{thp}}_{(\mathbf{a})} - \underbrace{\left[\sqrt{\frac{1}{S_{P1}}} + \sqrt{\frac{S_{P3}+2S_{P2}}{S_{P3}S_{P2}}} - \sqrt{\frac{1}{S_{P2}}}\right]}_{(\mathbf{b})}\underbrace{\sqrt{\frac{2I_{dc}}{\beta_p}}}_{(\mathbf{c})} \tag{4.7}$$

where S_{P1} to S_{P3} are the aspect ratios of the transistors P_1 to P_3, β_p is the transconductance parameter of the PMOS transistor and V_{dd} is the supply voltage.
Referring to equations (4.6) and (4.7), the following observations can be made:

1. The temperature equivalent voltages (V_n and V_p) are a function of the terms (a) and (c) only as the terms (b) and (b1) are constant.

2. It is well known that the threshold voltage V_{thn} decreases linearly with the increase in temperature [170]. Hence the aspect ratio of the transistors [term (b)] along with the amount and the temperature behavior of the DC-current [terms (c)] will control the thermal behavior of the temperature equivalent voltages V_n and V_p.

3. The presence of the supply voltage V_{dd} in (4.7) makes the PTAT sensor supply dependent. Hence, it will impose a limitation during the system level implementation.

To verify point (2) the DC simulation has been performed using an arbitrary simulation environment listed in Table.4.1. The performance of the sensors are presented in terms of the temperature coefficient (TC) and Full Scale Non Linearity (FSNL) [211]. The details of the bias circuit used in the simulations to obtain I_{dc} are available in publication [**X**].

Table 4.1. Simulation environment for proposed temperature sensors.

S.No.	Parameter	Value
1	Aspect ratio of S_{N2}, S_{N3}, S_{P2} and S_{P3}	W/L = 0.5 μm/0.18 μm
2	Aspect ratio of S_{N1} and S_{P1}	W/L = 10 μm/0.18 μm
3	Supply voltage V_{dd}	1.8 V
4	DC current I_{dc}	$10nA$ to $1\mu A$
5	Temperature (T)	-40°C to 85 °C

The simulated values of the temperature coefficients are shown in Fig. 4.2 for the PTAT and CTAT based voltage sensors. It can be seen in the figure that the temperature coefficients are decreasing with the increase in I_{dc}. The explanations of this behavior by using (4.6) and (4.7) are as follows:

1. For the lower values of I_{dc}, the term (a) will be greater than the terms (b) and (c) combined together. This is why the thermal behavior of V_{th} will dominant over the thermal behavior of I_{dc}.

2. With the increase in I_{dc}, terms (a), (b) and (c) all together will start contributing to the thermal behavior of the sensor output voltage.

3. Later, with the increase in I_{dc}, it is necessary to take the mobility factor μ into account as it will contribute to the thermal behavior of the sensor output by counter balancing the thermal effect generated by the threshold voltage V_{th}. It can be easily estimated in Fig. 4.2 that for a certain value of I_{dc} ($> 1\mu$A) the temperature coefficient |TC| will become minimal and hence, the sensors will converge in the voltage reference circuits (Fig. 3.1).

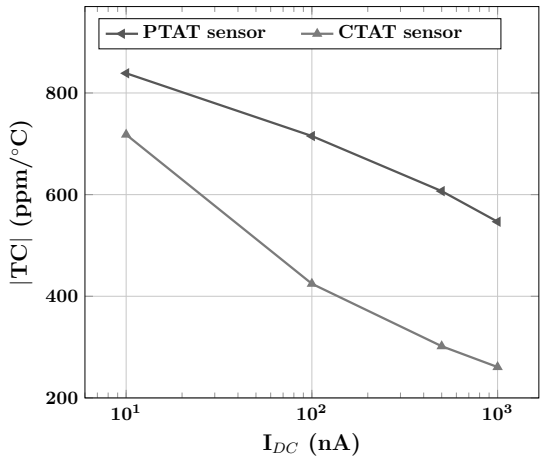
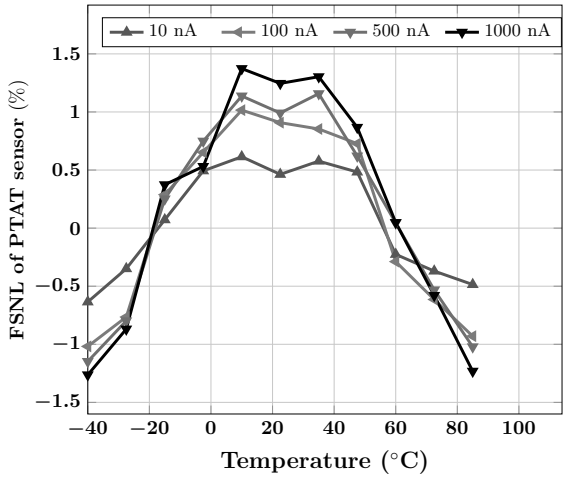


Figure 4.2. Variation of temperature coefficients with DC current.

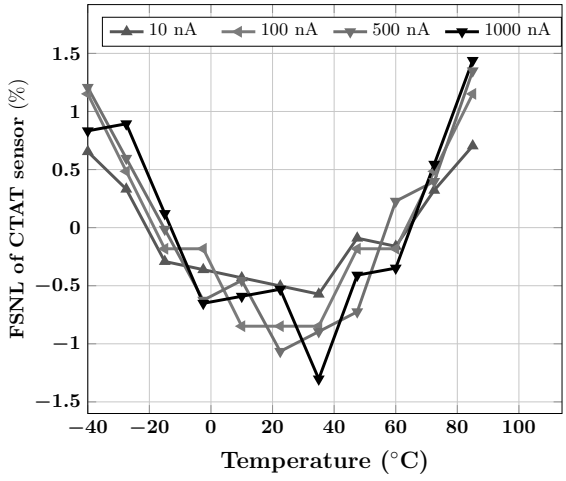
The variation of full scale non linearity (FSNL) (%) with the temperature of the PTAT and CTAT voltage generator is shown in Fig. 4.3(a) and Fig. 4.3(b) respectively. The FSNL parameter is the measure of linearity in terms of percentage over a full scale value from the straight line plotted over the data points. It should be noted that this straight line is a best fit straight line so that the data points will lie closer to it. The FSNL is calculated by using:

$$FSNL(\%) = \frac{\Delta X}{X_{FS}} \cdot 100\% \tag{4.8}$$

where ΔX is the deviation of data X from the best fit straight line and X_{FS} is the full scale value.



(a)



(b)

Figure 4.3. Variation of full-scale non linearity (%) with temperature (°C) of (a) PTAT and (b) CTAT sensors

By using PTAT and CTAT voltage generators, a simple smart temperature sensor publication [**X**] was designed. The aim of the work published in [**X**] was to describe that, if the thermal coefficient of temperature equivalent voltage signal is increased, then temperature information can be extracted using a simple readout circuitry. In order to increase thermal sensitivity, the output from the CTAT sensor was subtracted from the PTAT sensor output. As a result, a PTAT voltage with higher thermal sensitivity was obtained. The temperature information from this PTAT voltage was extracted in terms of the duty-cycle by using a simple pulse width modulator.

4.2.2 Current-based temperature sensor

The current-based temperature sensor is a PTAT current reference. The schematic of this sensor is the same as the current reference circuit published in [**VIII**]. The difference is in the aspect ratio of the transistors and operating supply voltage. It was found using simulations that, for a lower supply voltage, the proposed extension circuit [**VIII**] adds a positive temperature coefficient to the current. This particular behavior became the basis for the use of the current reference circuit [**VIII**] as a PTAT current generator.

The circuit diagram of the PTAT current generator is shown in Fig. 4.4.

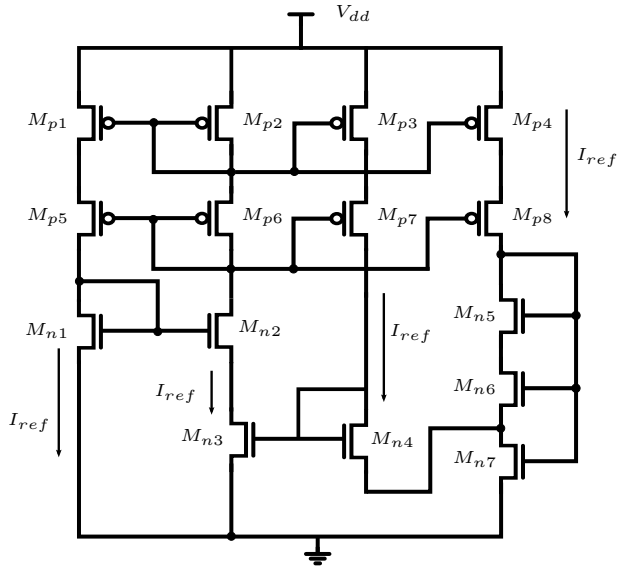


Figure 4.4. Schematic of PTAT current generator circuit.

It has been explained earlier in section.3.3.2, that the NMOS transistor M_{n3} is working as an active resistor. Thus, the current (I_{ref}) flowing through it will be:

$$I_{ref} = \beta_n S_3 \, (V_{gs3} - V_{thn}) V_{ds3} \tag{4.9}$$

where S_3 is the aspect ratio (W/L) of the NMOS transistor M_{n3}. The gate-source voltage (V_{gs3}) which is required to keep M_{n3} in the deep triode region can be written as:

$$V_{gs3} = V_{gs4} + V_{ds7} \tag{4.10}$$

It can be noticed from Fig. 4.4 that M_{n4} is operating in the saturation

region similarly, by referring to publication **[VII]** it is possible to express V_{gs3} as follows:

$$V_{gs3} = \underbrace{V_{thn}}_{(a)} + \underbrace{\left(\sqrt{\frac{2I_{ref}}{\beta_n S_4}}\right) + \left(\sqrt{\frac{2I_{ref}}{\beta_n S}}\right)}_{(b)} \tag{4.11}$$

where S_4 is the aspect ratio of M_{n4} and S is the equivalent aspect ratios of NMOS M_{n3} to M_{n7}. Equation (4.11) is a combination of terms (a) and (b). It is known from [170] that the threshold voltage will decreases with the temperature. If I_{ref} is the PTAT current then with a proper aspect ratio it is possible to thermally compensate V_{thn}. This will result in a thermally compensated V_{gs3}. The simulated plot of V_{gs3} at different temperatures is shown in Fig. 4.5. Here it can be observed that the variation of V_{gs3} with

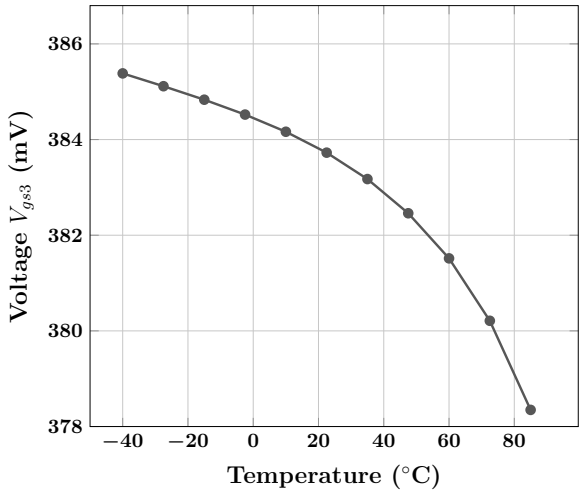


Figure 4.5. Temperature independent behavior of voltage V_{gs3}.

temperature is approximately 64 μV/°C. Thus, it can be considered that the V_{gs} exhibits temperature independent behavior. The transistors M_{n1} and M_{n2} in Fig. 4.4 are operating in the subthreshold; hence the voltage V_{ds3} is given by:

$$V_{ds3} = \eta \frac{KT}{q} \ln\left(\frac{S_2}{S_1}\right) \tag{4.12}$$

where η is the subthreshold slope, K is Boltzmann's constant, T is the absolute temperature, q is the electronic charge, S_1 and S_2 are the aspect ratio of the transistors M_{n1} and M_{n2} respectively.

By substituting, (4.11) and (4.12) in (4.9) will result in:

$$I_{ref} = \underbrace{\frac{\eta K S_3 \mu(T_0)}{q} \ln\left(\frac{S2}{S1}\right)\left(\frac{T}{T_0}\right)^{(1-m)}}_{(c)} \cdot \underbrace{(V_{gs3} - V_{thn})}_{(d)} \tag{4.13}$$

In (4.13), the term (c) will be constant for small values of the parameter 'm'. Hence, the thermal behavior of I_{ref} will be controlled mainly by the term (d). The simulated temperature behavior of the term (d) is shown in Fig. 4.6. It can be concluded easily by using Fig. 4.7 that the difference is progressing linearly with the temperature. As a result, it will introduce the PTAT behavior in I_{ref} as shown in Fig. 4.8.

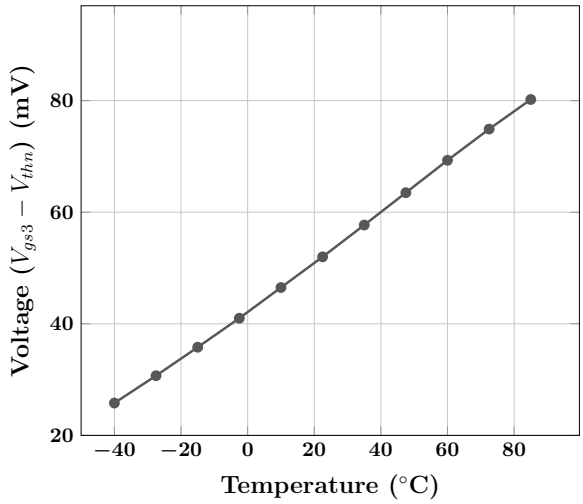


Figure 4.6. Simulated temperature behavior of voltage (V_{gs3}-V_{thn}).

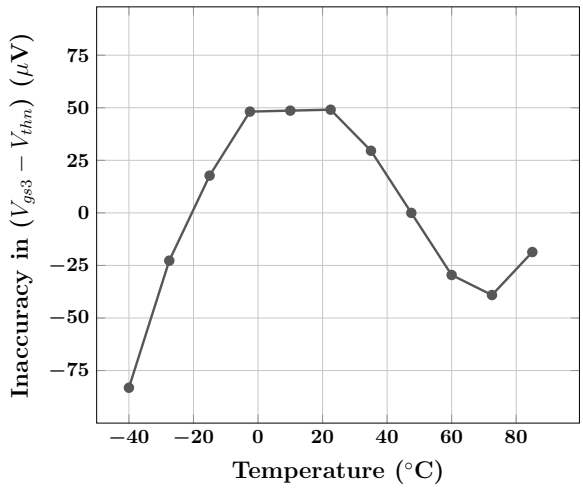


Figure 4.7. Linearity error in voltage (V_{gs3}-V_{thn}).

The simulated values of the temperature inaccuracy obtained from the PTAT current-based temperature sensor is shown in Fig. 4.9 over the given temperature range. It can be observed from Fig. 4.9 that the sensor is capable of measuring temperature with an inaccuracy of +0.6°C to

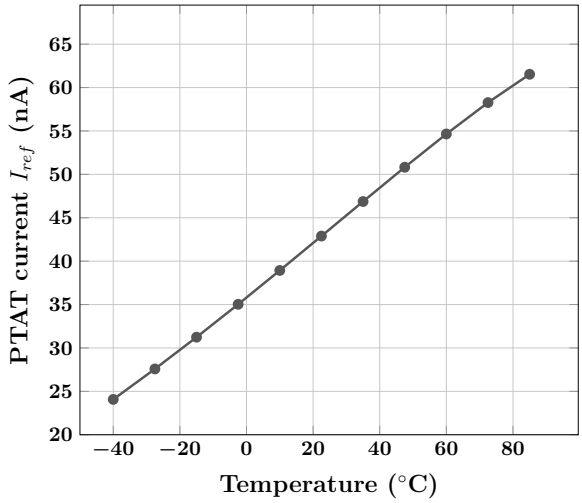


Figure 4.8. Simulated temperature behavior of PTAT current (I_{ref}).

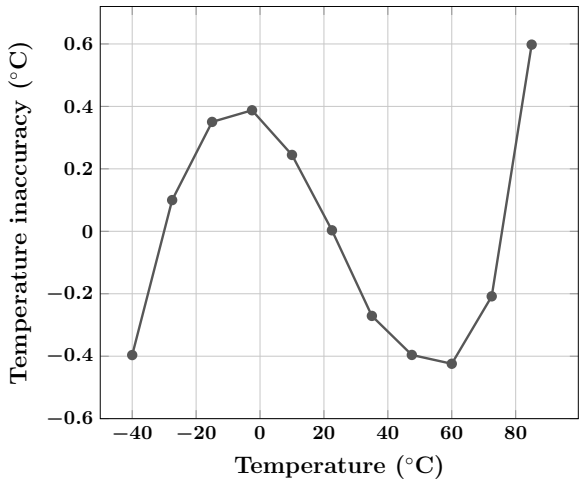


Figure 4.9. Simulated temperature inaccuracy (°C) of PTAT current (I_{ref}).

-0.4°C. The measured performance of this current-based temperature sensor or the PTAT current generator is available in publication [**XI**].
Later, this PTAT current was used to bias a source-coupled multi-vibrator in order to obtain the temperature in terms of the frequency. The measured results were published in [**XII**].

Table 4.2. Performance comparison of proposed temperature sensors with state-of-the-art temperature sensing circuits.

Ref.	Tech. (nm)	Supply Voltage (V)	Power Consumption (μW)	Operating Temp. (°C)	Temp. Accuracy (°C)	Calibration	Sensing type	Temp.in terms of
[200]	160	1.8	8.6	-55 to 125	±0.4	1-point	PTAT Voltage	Voltage Ratio
[212]	350	1.4	3.5	-40 to 125	-0.1 to 0.5	2-point	PTAT Voltage	Duty cycle
[213]	180	1.8	2.16	-40 to 85	-0.75 to 0.5	2-point	PTAT Voltage	Voltage
[214]	220/180 HP	2.5	175	0 to 100	-0.7 to 0.6	1-point	Delay line	Time
[215]	90	0.8 to 1.2	15.72 (max)	-40 to 125	-0.6 to 0.8	2-point	PTAT Voltage	Time
[XII]	180	0.9±10%	0.6 (max)	-40 to 85	-0.83 to 0.75	1-point	PTAT Current	Frequency
[216]	90	0.45 to 1.5	48 (max)	-55 to 105	±1	1-point	PTAT Voltage	Voltage
[XI]	180	0.85±10%	0.068 (max)	-40 to 85	±1	1-point	PTAT Current	Current
[217]	65	0.4	0.28	0 to 100	-1.6 to 1	2-point	PTAT Current	Delay
[X]	180	1.8	7.2	-30 to 70	±1.3	1-point	PTAT+CTAT Voltage	Duty cycle
[218]	180	1.2	0.071	0 to 100	-1.4 to 1.5	2-point	PTAT Voltage	Frequency
[219]	350	2.2 to 3	27 (max)	10 to 80	-1.8 to 1	1-point	PTAT Voltage	Frequency
[220]	32	1.65	100	5 to 100	±1.95	2-point	PTAT Current	Duty cycle
[221]	130	1.2	673.9†	20 to 120	-2.4 to 2.16	1-point	DCO	Pulse width
[203]	500	>1	21	-40 to 100	±2.5	-	PTAT voltage	Voltage
[222]	65	1.2	400	-40 to 110	-2.8 to 2.9	1-point	Delay line	Frequency

† Calculated from the statistics shown in the article.

4.3 Summary

Simple architectures for temperature sensing were presented in this chapter. The temperature was sensed in terms of the voltage and current. The working principles of these temperature sensors were described using a theoretical framework supported with the simulations. The performance comparison of the proposed temperature sensor with state-of-the-art temperature sensors is listed in Table.4.2.

Specifically, the new benefits of these temperature sensors are their simplicity in implementation, low power consumption, commercial temperature sensing range of -40°C to +85°C and moderate temperature inaccuracy within $\pm$1.5°C with single point calibration. These benefits compare favorably with the majority of the state-of-the-art temperature sensors available in literature.

With these design specifications the proposed temperature sensors are suitable for monitoring the temperature of the computer peripheral, the processor and memory module, environmental control and data acquisition systems, thermal protection, industrial process control, power system monitors, telecommunications equipment and office machines to name but a few operational scenarios.

5. Conclusions

A new study was recently published by WinterGreenResearch® about the wireless sensor network market worldwide for the years 2014 to 2020. This study projects a significant growth in wireless sensor based semiconductor industries due to its implementations in the Internet of things. A variety of projects are running worldwide to accomplish smart life for mankind. The backbone of all these projects is the wireless sensor node as it can be easily installed in hard-to-reach locations and can operate without the use of any mains supply and/or ON-board battery.

Presently, the implementation trend of wireless sensor nodes is focused on the development of passive implementations. This is simply due the fact that it will minimize the size and implementation cost, and maximize the applications of sensor nodes. The selection of energy harvesting technique for a node is a function of the application for which the sensor node will be used. In general, solar, wind and vibration energy harvesting methods are suitable for outdoor applications. However, they can not be used for indoor applications such as building automation or bio-medical applications, for instance.

In these applications, RF energy harvesting is the present solution because of its omnipresence. Presently, the total number of wireless devices worldwide is 9 billion and it is a predicted that, by the year 2020, the total will touch 100 billion. However, the energy density of the available RF signal is restricted by the Federal laws. As a result, intensive research in the development of passive RF powered wireless node is going on by various researchers.

The aim of the thesis has been the development of new strategies for efficient RF-to-DC conversion and to develop new low power CMOS components useful in the different units of a typical wireless sensor node. A comprehensive treatment of the contributions to this thesis is given in the

scientific publications [**I**]-[**XII**]. *The thesis focuses on the design of the key sub-blocks used in the wireless sensor node. These blocks include RF-to-DC converters, low power precision voltage reference, current reference and frequency reference circuits and moderately accurate smart temperature sensors.*

First, a brief examination of the parameters affecting the performance for radio frequency power harvesters was presented. It will give the reader an insight into the issues that should be addressed during the design of RF-to-DC converters. The focal point of this research was to obtain threshold compensation in the rectifiers. Two strategies were proposed : (i) the use of body biasing and (ii) the use of additional circuits. The rectifiers that use the dynamic body and static body biasing techniques are available in publications [**I**], [**II**] and [**III**]. The threshold compensation was obtained by the use of additional circuits are available in [**IV**] and [**V**]. In these circuits generate threshold compensation by using a rectified DC voltage alone [**IV**] or by inclusion of the received RF signal [**V**].

Second, a simple architectures for voltage, current and frequency reference circuits was developed for the power management unit of a wireless sensor node. Publications [**VI**] and [**VII**] include two different all-MOSFET voltage reference architectures. These architectures provide moderately accurate voltage reference values of 17.43 ppm/°C and 19.3 ppm/°C in the temperature range of -40 °C to 85 °C. The simplicity in the design implementation of these architectures is the most important benefit that enables the use of the architecture locally.

Moreover, a current reference architecture is published in [**VIII**] which is a modification of a classical resistor less current reference circuit. The primary target of this work was to shrink the temperature coefficient barrier of this classical structure. The measured results show a reduction of 68% in the temperature coefficient of the classical structure. However, this improvement was achieved at a cost of 58% extra power and with high line regulation (7.5%V).

A frequency reference circuit published in [**IX**] utilizes the principle of the reversal of temperature dependence by using the supply voltage. In the literature, various methods are proposed by the researchers to obtain a temperature compensated clock signal. Among all these methods, use of this principle is easier to implement. However, this method demands a dedicated supply voltage regulator. This principle was established by using measurement, and measured results show a mean deviation of 1.53%

from the reference frequency value of 355 KHz.

An extensive performance comparison of the proposed reference architectures with state-of-the-art reference circuits present in literature are listed. In order to evaluate the reference circuits with the present implementation trends, the majority of the-state-of-the-art reference circuits published within the last five years have been selected.

Third, moderately accurate smart temperature sensor architectures were proposed. These are configured as voltage-based and current-based architectures based on their temperature sensing core. The voltage-based temperature sensor generates PTAT and CTAT respectively, while the current-based sensor provides a PTAT signal. These architectures with a simple interface circuit are published in [**X**], [**XI**] and [**XII**]. The voltage-based temperature sensor provides temperature information in terms of the duty cycle within temperature inaccuracy of $\pm 1.3°C$ [**X**], while the current-based temperature sensor achieves temperature accuracy in the range of $\pm 1°C$ [**XI**]. In addition, the current-based temperature core [**XI**] that has been used in the temperature-to-frequency converter [**XII**] can measure the temperature with an inaccuracy of -0.83°C to 0.75°C .

These temperature inaccuracies were obtained after single point calibration. The temperature sensing field is very innovative primarily due to the shrinking technology node. The research in the field of temperature sensors is versatile and various architectures are published every year to sense the temperature. In order to evaluate the proposed temperature circuits, the majority of the state-of-the-art temperature sensor circuits published within the last two years have been selected.

As a possible future work, the development of simplified and energy aware architectures which would include power management, an ultra low power sensor interface, sensors with minimum inaccuracy and new architectures to increase power conversion efficiency the rectifier could be implemented. This topic will receive more attention in the future with the ever growing demands for wireless sensor node applications.

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