Modular development platform for implantable wireless medical sensor devices

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ABSTRACT OF THE
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Implanting medical sensor devices under skin improves the quality of the acquired measurement results, and can greatly increase the comfort for the patient in prolonged measurement. Design of such complex devices and related systems benefits from using a dedicated development platform that represents the functionalities and associated challenges.

This work presents the design, implementation and verified performance of a modular platform that can be used in demonstration, development and testing of various functionalities of wireless medical sensor implants. The system is constructed using discrete components and consists of five interconnectable modules, each representing a specific function of the sensor implant system: biopotential measurement front-end module, wireless communication front-end module, clock and power management module, control logic module and external reader module. The implemented system has measurement front-end with an ENOB of 9 bits and configurable structure for the needs of various biopotentials. Wireless data transfer operates at 840-960 MHz with supported datarate up to 640 kbps. The system demonstrates dual carrier operation for separating the power and data transfers. Power can be harvested and clock extracted from 6.75 MHz or 865 MHz radio signals, both radio signals can be generated by the external reader. Control logic is provided with a high-end FPGA evaluation board. The completed platform can be used for developing and testing aspects for novel implanted devices, such as different radio communication schemes, radio antenna options, or controls and algorithms in digital logic.

Keywords: Sensor implant, Biopotential, RFID, Development platform

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Lääketieteellisten anturien asettaminen ihon alle parantaa biopotentiaalimittauksien tulosten laatua ja pitkäaikaisten mittauksien mukavuutta potilaalle. Näiden monimutkaisten laitteiden suunnittelua voidaan tehostaa käyttämällä apuna sovelluskohtaista kehitysalustaa.

Tässä työssä suunnitellaan ja toteutetaan modulaarinen, korkean suorituskyvyn kehitysalusta biopotentiaalia mittaavien langattomien anturi-implanttijärjestelmien eri toiminnallisuuksien esittelyyn, kehitykseen ja testaukseen. Diskreeteillä komponenteilla toteutettu järjestelmä koostuu viidestä moduulista: biopotentiaalien mittausmoduuli, langattoman tiedonvälityksen radiomoduuli, tehon ja kellosignaalin keräysmoduuli, ohjauslogiikkamoduuli, ja kehon ulkopuolinen lukijamoduuli.

Kehitysalusta on muokattavissa eri biopotentiaalien mittauksien tarpeisiin. Mittausetupään tehollinen bittimäärä on 9 bittiä. Langatonta tiedonsiirtoa tuetaan 840-960 MHz taajuuskaistalla 640 kbps siirtonopeuksiin asti. Järjestelmällä voidaan demonstroida kahden kantoaallon yhtäaikaista käyttämistä, jolloin tehon- ja tiedonsiirto voidaan tarvittaessa erottaa toisistaan. Tehoa voidaan kerätä ja kellosignaaleja muodostaa 6.75 MHz ja 865 MHz taajuuksisilta radiosignaaleilta, jotka molemmat voidaan luoda hallitusti lukijamoduulilla. Ohjauslogiikka on toteutettu käyttäen ohjelmoitavaa porttimatriisipiiriä.

Kehitysalustaa voidaan käyttää uusien implanttijärjestelmien suunnittelussa, esimerkiksi eri tiedonsiirtotapojen, antennirakenteiden, ohjauslogiikan ja digitaalisten algoritmien arvioinnissa.

Avainsanat: Anturi-implantti, Biopotentiaali, RFID, Kehitysalusta

Preface

The work presented in this thesis has been carried out in Aalto University's department of Micro- and Nanosciences, Electronic Circuit Design unit, as a part of the EEGBIDE-project.

I would like express my gratitude to my thesis supervisor, professor Jussi Ryynänen for the opportunity to work in this project and write this thesis in the Department of Micro and Nanosciences. Special thanks to my instructor D.Sc. Marko Kosunen for excellent guidance and epic weekly project meetings, where even my stupidest questions were answered composedly, and Z-transformation was be used to explain the universe.

I would like to thank all the people of the Aalto MNT department who helped me in the course of this work, especially Jani Hevosoja, for his great help in both hardware and software design, Olaitan Olabode, for her help in everything ADC-related, and Tero Tikka for advicing me on the use of the different simulation softwares and measurement equipment.

Finally I would like to thank my dear Emilia for her support, who kept me (somewhat) sane during this process!

Otaniemi, 16.9.2015

Antti J. E. Ontronen

Symbols and Abbreviations

Abbreviations

AC	Alternating current
ADS	(Keysight) Advanced Design System
CMRR	Common mode rejection ratio
DAC	Digital to analog converter
DC	Direct current
DFT	Discrete Fourier transformation
DNL	Differential nonlinearity
ECoG	Electrocorticogram
EEG	Electroencephalogram
EMG	Electromyogram
ENOB	Effective number of bits
EPC C1G2	Electronic product code, class 1 generation 2
FIFO	First-in-first-out
FMC	FPGA Mezzanine card
FPGA	Field-programmable gate array
GPIB	General purpose interface bus
GPIO	General purpose input/output
HF	High frequency
INL	Integral nonlinearity
LVDS	Low voltage differential signal
MCU	Microcontroller unit
MOSFET	Metal-oxide-semiconductor field-effect transistor
NAD	Noise and distortion
PC	Personal computer
PGA	Programmable gain amplifier

PL	Programmable logic
PPM	Power path manager
PS	Processor system
RFID	Radio frequency identification
RMS	Root-mean-square
SAR	Specific absorption rate
SFDR	Spurious-free dynamic range
SNDR	Signal-to-noise-and-distortion
SNR	Signal-to-noise ratio
SoC	System on chip
SPI	Serial peripheral interface
TCP/IP	Transmission control protocol / internet protocol
THD	Total harmonic distortion
UART	Universal asynchronous receiver/transmitter
UHF	Ultra high frequency
USB	Universal serial bus

Symbols

H_{count}	Amount of channels
R_{sample}	Sampling rate
s_i	Signal at frequencies i
$X(s_i)$	Spectral component of the signal at frequencies i

Contents

1 Introduction

Electroencephalogram (EEG) is the measurement of electrical potential fluctuation of the brain. [1] Conventionally EEG is recorded noninvasely using scalp electrodes, but long term monitoring of EEG using scalp electrodes is often uncomfortable for the patient, and the patients modify their behaviour while wearing the electrodes [2], which defeats the purpose of measuring the EEG in natural conditions. These problems would be solved if the measurement system was implanted under skin as a medical sensor implant. Designing such as an implant is no trivial matter, several parameters and dependencies need to taken into account. Therefore, a good development platform is required to make informed decisions in the design of such a device.

This work describes the implementation of a modular demonstration platform to be used in the development of a variety of medical implants. The main design goals were modularity and high performance, whereas small power consumption or form factor were of less concern. Modularity enables the various sub-parts of a medical implant system to be developed and optimized either separately or combined, allows the ease of changing the sub-parts of the system depending on the requirements and grants the ability to re-use the sub-parts in other similar projects. High performance helps the early development by allowing the developer to exceed the normal limitations in creating methods and algorithms in the proof-of-concept stage.

The implemented system comprises of five modules: (1) a variable channel count biopotential measuring analog front-end module with suitable filter and amplifier structures, (2) a single frequency radio communication transceiver front-end module supporting a popular RFID protocol EPC C1G2 [3], (3) a dual frequency clock and power extracting supply module, (4) a dual frequency RFID transmitter/transceiver module with embedded microcontroller and connectivity to PC, and (5) a high end FPGA development board Xilinx ZC706 [4] , that works as a controller for all implant functionality modules. All modules except the FPGA development board were designed and manufactured specifically for this project.

System is tested, the key characteristics are measured and all problem points are thoroughly analyzed. System control, measurements and calculation of performance metrics were performed using custom drivers, applications and scripts.

Chapter 2 introduces the relevant theory related to the operation and design of different sensor implants and previous works on comparable development systems. Chapter 3 describes the design solutions made in this implementation, and chapter 4 describes the measurement methodology followed in this work and analyzes the system performance based on real measurement data. Chapter 5 concludes the work.

2 Inductively powered implanted sensor devices

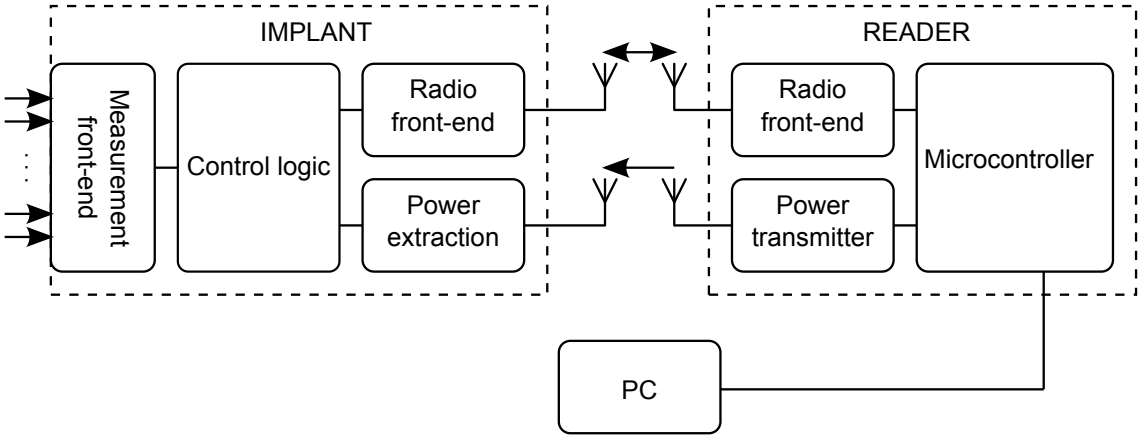


Figure 1: Block diagram of a medical implant sensor measurement system.

Inductively powered medical implants are biomedical electrical sensor devices that are powered from a external radio device by the means of inductive coupling. A commonly used system topology is presented in Figure 1. The implants discussed in this work are limited to very low distance operation transcutaneous devices.

Table 1: Characteristics of a selection of different biopotential signals. [5, p. 808]

Biopotential	**Electrode type**	**Amplitude range**	**Frequency range**
EEG	Surface/implanted	10 - 100 μV	0.5 - 100 Hz
ECoG	Implanted	50 - 500 μV	100 - 5000 Hz
EMG	Surface/implanted	50 - 5000 μV	2 - 500 Hz
ECG	Surface/implanted	100 - 2000 μV	100 - 1000 Hz

Medical implants can be used in instrumentation of different biopotential measurements. Electroencephalogram (EEG) is the measurement electrical potential fluctuations of the brain. Typical EEG signal bandwidth is from 0.5 Hz to 100 Hz, with amplitudes of 10-100 μV measured with on-scalp electrodes [6]. The amplitude increases up to 10 mV if the electrodes are placed under skin [7, p. 173]. Measuring and recording electrical potential directly from the surface of the brain is called electrocorticogram (ECoG). Electromyogram (EMG) is the instrumentation of muscle activity, usually measured from the body-surface. Electrocardiogram (ECG) is the measurement of biopotentials originating from heart activity. [7] The requirements for different biopotentials are diverse as can be seen from Table 1.

Previous works related to wireless implant prototypes for measuring EEG [8], ECoG [9] [10], EMG [11], ECG [12] and even multiple biopotentials [13] [14] [15], have displayed a variety of topologies and techniques for the common design goals of instrumentation front-ends, wireless data transmission, clock generation, power

extraction and the digital control logic. The following sections introduce and select the most suitable structures for the use of the development platform.

2.1 Biopotential measurement

The measurement front-end in Figure 1 is arguably the most critical part of a medical sensor implant, as it provides the core functionality of sensing the biopotential signal of interest. Biopotentials are generally very low amplitude signals, typically between 10 μV and 100 mV on a precise frequency range, so the measurement system for such signals must be sensitive and selective for only the desired signals. A general structure of a biopotential measurement front-end includes one reference electrode, an electrode per measured channel, pre-amplifiers, signal filtering, post-amplifier and an acquisition device such as an analog-to-digital converter (ADC). [5, p. 1185-1195] Multiple channel acquisition can be achieved by adding a channel selecting device to the structure before [15] or after [16] the filters.

There are several types of electrodes for biopotential measurements, including surface electrodes, needle electrodes and arrays of electrodes. The measured variable and the amplitude depends on the type, material and location of the electrodes. The input signal consists of (1) the desired biopotential on a known frequency range, (2) undesired biopotentials captured by the electrodes, (3) 50 Hz line interference captured by the measurement cables, (4) interference caused by the contact impedance of the electrodes on skin upon motion and (5) noise [5, p. 1185-1195]. The measured signal should be amplified as soon as possible before feeding it further on the front-end in order to separate the desired signal from the noise generated by the front-end itself. The noise from external sources, such as the line noise, can be minimized by using shielded cables and differential topologies in the amplifier stages, so that the external emissions are coupled to both of the differential lines and rejected. This common mode rejection ratio (CMRR) is one of the most important parameters of the pre-amplifier stage.

The amplified and filtered signal is digitized with an analog-to-digital converter. Successive approximation ADC digitizes the analog sample by comparing it to a incrementally changing reference value by following binary search algorithms. This type of ADC can be made very energy-efficient in medium to high resolution accuracy [17, p. 391], making it a popular choice in low power sensor technology [14], [9].

The accuracy of the ADC-based analog front-end is characterized by specific performance metrics, divided to static linearity and dynamic noise. Static linearity performance defines the deviation from ideal code transitions of the analog-to-digital converter without considering the time-domain effects. Dynamic noise performance describes the effect of time-domain non-idealities, such as generated harmonics and noise level.

Most important static performance characteristics are the differential nonlinearity and the integral nonlinearity. Differential nonlinearity (DNL) is the ratio of the measured deviation from the ideal average code bin width to the ideal average code bin width. Integral nonlinearity (INL) is the difference between the ideal and measured code transition level. The dynamic performance metrics can be derived

from the output frequency spectrum representation of a known signal input. Discrete Fourier transformation (DFT) is used to convert data sampled in time domain $x[n]$ to a representation $X[k]$ in frequency domain. If the time domain sampling is not coherent, a windowing function can be used to minimize the effect of spectral leakage. The magnitude of the DFT bins must corrected with the normalized noise power gain of the corresponding window in order to extract accurate metrics from the frequency domain presentation. [18]

Signal-to-noise ratio (SNR) is the ratio of the root-mean-square (RMS) of the fundamental frequency component amplitude s_{fund} to the RMS of the converter output noise and distortion (NAD) floor NAD_{floor} that excludes harmonic spectral components.

$$SNR = 20 * log_{10}\left(\frac{|s_{fund}|}{|\mathrm{NAD}_{floor}|}\right) \tag{1}$$

Total harmonic distortion (THD) is the ratio of the averaged spectral component amplitude of fundamental signal s_{fund} and the root of the sum of squared values of the averaged harmonic components s_{harm}, usually calculated to include second to tenth harmonics n.

$$THD = \frac{\sqrt{\left(\sum_{h=2}^{10} X_{ave}[s_{harm}]^2\right)}}{\sqrt{X_{ave}[s_{fund}]^2}} \tag{2}$$

Spurious-free dynamic range (SFDR) is the ratio of the spectral component amplitude of the fundamental input frequency $X(s_{fund})$ to the amplitude of the largest harmonic or spurious spectral component $X(s_{spurious})$.

$$SFDR = 20 * log_{10}\left(\frac{|X(s_{fund})|}{max(X(s_{spurious}))}\right) \tag{3}$$

Signal-to-noise-and-distortion (SINAD or SNDR) is defined as the ratio of $s_{fund.RMS}$ to the RMS of all noise and distortion $\mathrm{NAD}_{all.RMS}$ at the output, including random, harmonic and spurious noise sources.

$$SNDR = 20 * log_{10}\left(\frac{|s_{fund}|}{|\mathrm{NAD}_{all}|}\right) \tag{4}$$

Effective number of bits (ENOB) of a N bit ADC is the equivalent resolution of an ideal ADC corresponding to the measured SNDR. Equivalent value can also be approximated from INL. [18]

$$ENOB = \frac{SNDR - 1.76dB}{6.02dB} \tag{5}$$
$$\approx N - 1 - log_2(|INL|) \tag{6}$$

The combined set of the gain range, filtering characteristics, sampling rate, INL, DNL, SNR, THD, SFDR, SNDR, and ENOB, provides a comprehensive group of metrics to describe the accuracy and performance of the measurement front-end. Eventually this performance dictates the amount of meaningful measurement bits that the implant device should communicate forward to be stored and analysed.

2.2 Communication and data transfer

The biopotential measurements must be received or retrieved from the implant device, and the device must be controllable by some communication means. Wires puncturing the skin are an infection risk and can increase the noise of the measurement due to the high impedance levels and very low signal amplitudes, so wireless communication method is necessary to ensure patient safety and acquisition quality [19].

Radio front-end in Figure 1 handles the wireless communication. Many different wireless radio communication methods have been used in the previous works, with a variety of frequencies, modulations and encoding schemes [20], [12], [21] . Choosing a pre-existing radio protocol with predefined performance and commercially available front-ends should shorten the design cycle of the communication front-end of the system considerably at the expense of degrees of freedom in making changes to the communication. A ideal solution would be to find a existing off-the-self front-end component that both supports an existing protocol and could be used with custom protocols by operating only as modulator and demodulator over a range of frequencies, with suitable data transfer rate.

In the case of a medical sensor implant, the data transfer rate requirement is determined by the analog front-end bit count N, sampling rate R_{sample}, channel count H_{count} and any data packet structure bits, such as timestamps or error checking bits. With 32 channels of 12 bit accuracy at a sample rate of 200 samples per second on each channel, the absolute minimum data rate for EEG without packet structure is

$$\text{Datarate}_{min} = N * R_{sample} * H_{count} \tag{7}$$
$$= 12 \text{ bits} * 200 \text{ (samples)/s/channel} * 32 \text{ (channels)} \tag{8}$$
$$= 76.8 \text{ kbits/s} \tag{9}$$

Communication protocol for EPC C1G2 (electronic product code class 1 generation 2) is a suitable choice for implant communications [20] and supports continuous data rate up to 640 kbits/s [3], fulfilling our datarate requirement from (9). The protocol can be used with 865 MHz unlicensed ISM frequency, and a selection of off-the-self front-ends for both the reader and the implant side are available.

Table 2: Comparison of the available power densities from a selection of power sources for implantable devices. [22]

Power source	**Power density**
Batteries	0.09 μW/mm^2/year
Thermoelectric	0.6 μW/mm^2
Piezoelectric	$<$0.2 μW/mm^3
Electromagnetic	10-1000 μW/mm^2

2.3 Power transfer

Harvesting energy from a radio signal is a very efficient manner of powering the circuitry compared to batteries, piezoelectric harvester, thermoelectric harvester or glucose bio-fuel cells, as presented in Table 2 [22]. Regardless of the power source, the device requires antennas for wireless communication, so using the existing antenna for power transfer is a logical choice. Inductive link is a power transfer method based on the inductive coupling between two inductors in radio near-field, the operation is analogous with a loosely coupled transformer. [23] The challenge with using inductive coupling in power transfer to medical implants is the regulations limiting the allowed average radio power absorbed to a tissue mass, called specific absorption rate (SAR) regulations [24].

Recently the trend has been to combine the communication and power extraction in a inductively coupled radio link, which usually provides continuous power supply and efficient means of communication [22]. However, the requirements of the inductive data transfer and the power transfer are partially contradictory. Inductive data transfer benefits from high frequency and low quality factor, as a high datarate requires a wide bandwidth, whereas the inductive power transfer to implants requires a low frequency and a high quality factor [25], as the losses from tissue absorption are lower at frequencies under 10 MHz [24]. Common data modulation schemes used in inductive link communication, such as amplitude-shift-keying and phase-shift-keying, can interfere with the energy harvesting efficiency as they modulate the reflected power. Complex modulation may ease operation on single carrier and decrease the challenges associated with dual carrier, but increasing modulator elaboration hinders the requirement for minimal complexity on the implant. The mutually exclusive requirements can be separated and solved by using dual carriers, one for data transfer only and the other for power transfer only [26].

A suitable power transfer frequency choice with centimetre-size antennas is 6.78 MHz, that resides on the unlicensed ISM band [23], [17, p. 441]. It is worth noting that gigahertz range has also been proposed to be the optimal choice for powering transcutaneous implants [27], but this approach still allows less power available to the implant than the sub-10 MHz choice due to the SAR regulation limits [22], and is more beneficial only in single frequency applications with millimetre-size antennas.

2.4 Clock generation

In addition to power feed and communication, synchronization is required in the implant. Using on-chip oscillators as a clock source can commonly use a relatively significant amount of power, tens of microwatts [28] in the otherwise very low power system. A power efficient solution is to extract the clock from the carrier signal with a simple comparator architecture, also thus the clock is present whenever the implant is powered from or communicating through the inductive link. Comparator topologies have repeatedly achieved power consumption of under 2 μW [29], [30].

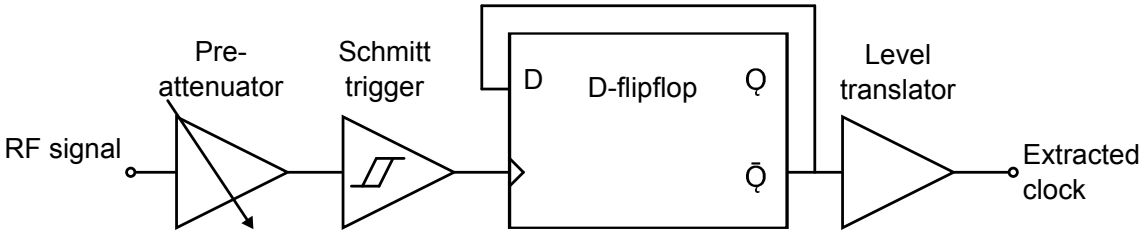


Figure 2: Block diagram of a generalized clock extraction from a radio circuit.

In Figure 1, this functionality can be included either in the radio front-end or the power extraction front-end. A general structure of a clock extractor presented in Figure 2 utilizes a preattenuator circuit to set the level for a Schmitt trigger that detects the edges of the signal, followed by a D-flip-flop to set the duty cycle of the clock signal to 50 % [19]. The clock can also be referenced to the modulated subcarrier coming from the external reader.

2.5 Control logic and algorithms

In order to use the limited power efficiently, the internal logic of the implant should be used to optimize its operations, presented by the control logic block in Figure 1. Most obvious way of reducing and optimizing the power consumption is to reduce the amount of data handled by the system, and three methods have been proposed for this: reduce the quality of the acquisition, use data compression algorithms on the raw signal, and transmit data discontinuously [2]. Quality of the acquisition is determined by the biopotential signal being measured, specifically by the sample rate and resolution it requires. Data compression and packaging algorithms with suitable package frame structure and acceptable level of data loss could be developed, and extended by utilizing efficient error detection to minimize the amount of data overhead needed for reliable transmissions. Discontinuous transmission could be implemented by feature detection, as in handling data only if some predetermined condition is fulfilled. For example, this condition could be related to epileptic seizure or a certain wavelength being active. Clearly, a flexible logic platform for developing such algorithms is needed.

2.6 Development platforms for implanted devices

One of the goals of this project is to offer a platform for developing digital logic for the use of a integrated circuit design. A high-end field-programmable gate array would provide the necessary performance for the development challenges with highest degree of freedom. An useful development environment provides a close imitation of the key characteristics of the system it is being used to develop while not being strictly restricted to the performance of the imitated system. It should to be able to surpass limitations, such as computational power, so that the developers are able to test a wide variety of scenarios and novel algorithms.

Previous works on creating development platforms and prototypes of wireless medical sensor devices with discrete components have commonly been embedded systems with small form-factor for wearability. Especially the WIMAGINE system [9], its derivative modular KDI system [31] and the EEGWISP system [8] are comparable prototypes to the system described in this project. The main contrast to the other works is that high-end FPGA components require considerable amount of power, cooling and board space [4], so the main design goals here were modularity and high performance, whereas small power consumption or form factor were of less concern.

FPGA-based development systems can be built around FPGA evaluation boards that are commercially available complete embedded systems on printed circuit boards with all of the necessary peripheral components to fully utilize the FPGA performance. Using these in development and prototyping of radio frequency identification (RFID) systems has yielded good results [32], [33]. As the inductively powered implanted device closely resembles a RFID sensor tag and will likely include the development or modification of a radio communication protocol, a similar approach will suite this modular development platform well.

Some FPGA evaluation boards provide access to high pin-count FPGA Mezzanine Card (FMC) connectors. Printed circuit boards with a suitable form factor of 69 millimeter width can be connected to these connectors as extension cards, allowing the FPGA to connect and control their functionalities. [34] Separating the implant functionalities from the FPGA functionalities allows the system to be highly modifiable and modular.

With the large evaluation board and extension cards the prototype system will not be wearable and certainly low power, but this is not a problem if we consider the demonstrated functionalities of the implant separately from the surrounding high performance structures of the development system.

3 Design of the development platform

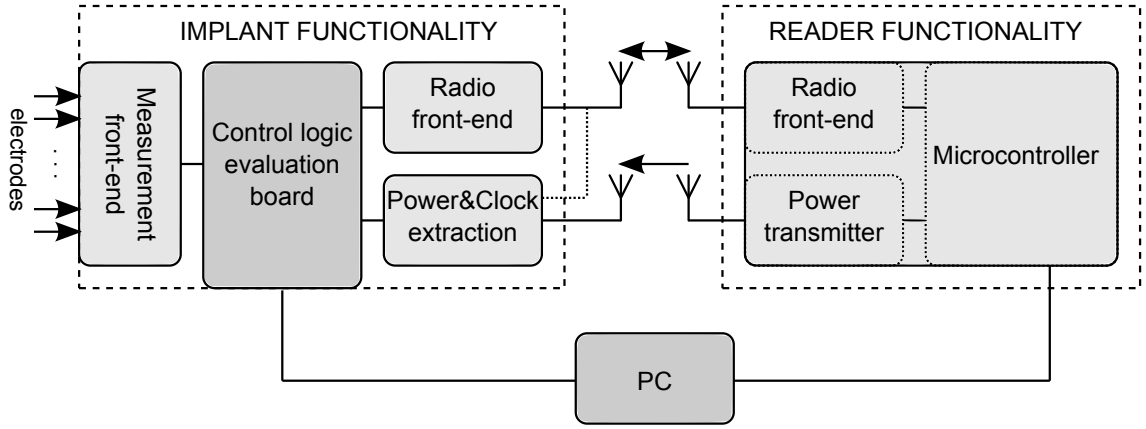


Figure 3: High level block diagram of the development system.

The proposed system design has three primary design goals. It (1) operates as a demonstration of the various functionalities of a wireless medical implant, (2) can be used as a development and measurement platform for testing and evaluation of important and novel aspects of the future integrated design, and (3) has a high performance level capable of imitating the operations of a wireless medical sensor devices for a range of biopotentials. In order to manage the complexity of the system and the design process, the different implant functionalities have been divided to separate interconnectable PCB modules as depicted in Figure 3. This approach has several benefits, as it enables one to measure and evaluate the different implant aspects separately and makes the prototype system design more manageable, as the system will be at least partly usable even with flaws in one or more functionalities.

3.1 Design methodology

The designed modules were kept as similar and interconnectable as possible, so communication protocols, connectors, form factors and components were carefully chosen to maximize the modularity. Circuit simulations with Eldo, Agilent ADS and Altium Designer were used to ascertain the correct operations in order to minimize the number of revisions needed in development, and to provide accurate simulation models for future users to test possible changes on the system. The simulation models were later revised according to the actual measured performance.

Serial peripheral interface bus (SPI) was chosen for communication to all components requiring digital control. SPI is a synchronous full-duplex single-master bus that commonly supports datarates of several megabits per second. Multiple slave devices can be added to a single bus, as the active slave is determined by dedicated chip select lines.

All of the digital signals between the modules are routed through voltage level translating bus-hold buffers, enabling the use of different logic voltage levels at

different sections and modules of the system. The bus-hold functionality intends to hold the most recent state of the driven line. The voltage thresholds and the hysteresis of the translators help in isolating the low amplitude and high frequency noise on the lines, and the buffers also provide additional protection against static discharge from the connectors. Fairchild FXLA10-series was chosen as it offers fast response times and low current requirements for the input, with additional automatic direction sensing. This enables using very low strength drivers at either side of the buffers, thus the other component choices are not limited by their line driver strength. Automatic direction sensing is incorporated by using a weak output driver that can be overdriven by an external driving source if the data direction changes. Due to the high series resistance of the weak output driver and the generally low overdrive current threshold of the direction sensing, pull-up or pull-down resistors should not be used at the driven side of these kind of buffers, as the conceivably high current from the pulling resistors can interfere with both the output voltage level and the direction sensing. [35]

Form factors of the different boards are designed to be partially compliant with the VITA 57 FMC standard [34]. All designed boards are 69 millimeters wide with FPGA Mezzanine connectors (FMC) connectors, whereas the length of the boards is defined by the area requirement of the application. Area minimization was not a priority, so excessive space was reserved between components to enable easier access to all components when measuring and modifying the system.

All modules use 6-layer printed circuit boards manufactured with FR4 dielectric with the same layer stack. The printed circuit boards were designed with Altium Designer. Transmission lines used in high frequency logic and radio signals are coplanar waveguides with ground, with impedance controlled routing trace width calculations done in Keysight Advanced Design System (ADS) electronics simulation software.

3.2 Biopotential measurement front-end

A development platform for measurement of multiple biopotentials and differing electrode types needs to be highly modifiable in terms of gain structure and filter passband. The objective was to create an analog front-end for accurate measuring of EEG, while also having high degrees of freedom so that the same structure could be modified to be used with other biopotentials. In order to achieve these goals, a differential four channel variable gain amplifier structure with a configurable filter followed by a high-speed analog-to-digital converter was designed. The resulting analog front-end structure is presented in Figure 4.

3.2.1 Biopotential amplifiers and gain settings

The amplitude range of biopotential measurement with different electrodes is approximately 10 μV to 100 mV. A signal this small needs to be amplified in order to be read in reference to a reasonably stable voltage level. If the reference voltage is 1.5 V, the total gain range needed is 150 to 150000.

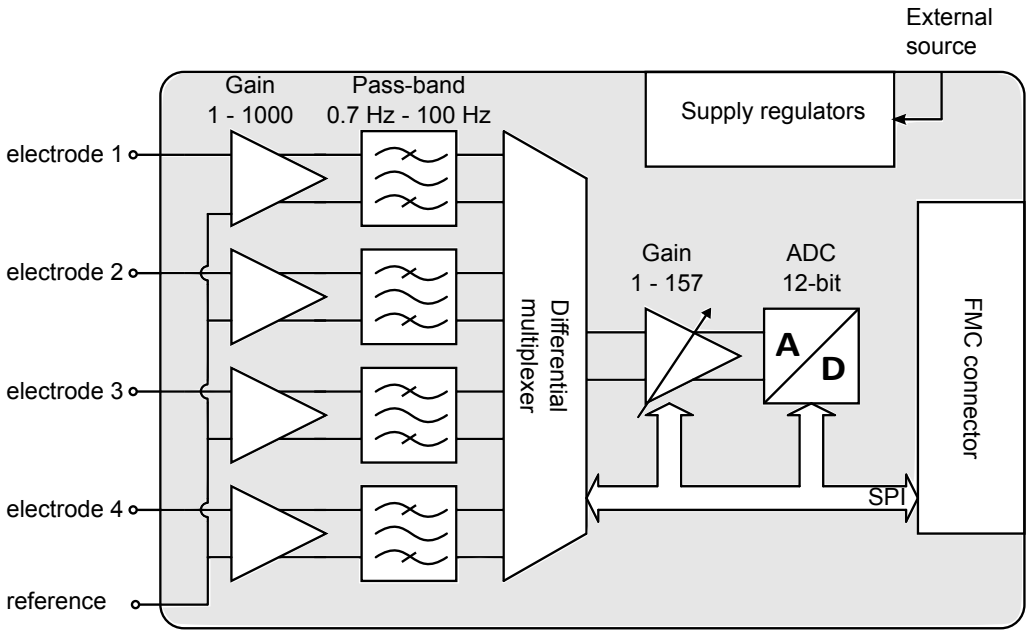


Figure 4: Structure of the implemented differential EEG-measuring analog front-end.

The first stage of the measurement front-end should be a pre-amplifier stage, presented as the leftmost amplifiers in Figure 4, to boost the desired signal above any ambient noise of the following structure. Pre-amplifier in EEG measurement needs to have input impedance of over 100 MΩ and a common mode rejection ratio (CMRR) of over 100dB [5]. Instrumentation amplifier INA333 from Texas Instruments has a typical input impedance of 100 GΩ, gain settable in the range of 1 to 1000 by an external resistor, and CMRR over 110 dB at gain values over 10. The rated input voltage noise of INA333 is 1 μV_{pp} in the frequency range of 0.1 to 10 Hz and 50 nV/Hz at frequencies higher than 10 Hz. [36]

As the chosen pre-amplifier has only a fraction of the required maximum gain, a programmable gain amplifier (PGA) MAX9939 from maxim integrated [37] is used to amplify the signal after the filter to the full dynamic range of the analog-to-digital converter. The PGA is located just before the ADC (Figure 4), it has a digitally programmable gain range of 1 to 157 and a possibility to adjust the internal input voltage offset. The PGA is followed by an anti-aliasing filter to decrease the aliasing of harmonics if a too high gain setting in PGA results in the signal clipping.

3.2.2 Filtering

After the signal has been amplified by the pre-amplifier, it needs to be filtered to include only the desired frequency components. In Figure 4 this stage is represented by the bandpass filters. Especially important is to reject the frequencies higher than half of the sampling frequency to minimize aliasing in analog-to-digital conversion. EEG signals related to neural activity have been measured to be in range of sub 0.1 Hz to well over 100Hz, but the clinically interesting portion of the EEG as in the portion that has been proven to include the most relevant EEG data is between 0.5

Hz to 100 Hz. [6] This is chosen to be the default bandpass for the filtering structure.

A high-pass filtering structure is needed in order to achieve the low cut-off frequency. Purpose of attenuating the low frequency components is to reject the common mode direct current (DC) component, distortion from breathing and any other low frequency alternating current (AC) noise not directly related to the wanted biopotential. A common way to remove the undesired DC component from the measured signal is to use capacitors as DC blockers to AC-couple the system. If the instrumentation amplifier is AC-coupled, a ground return path must be provided to the input pins or the bias currents of the instrumentation amplifier itself may slowly charge these capacitors until the common-mode voltage is exceeded [38, p. 5-2]. High CMRR of instrumentation amplifiers is based on the impedances of the input pins being well balanced, so additional components at the input of the amplifier would degrade the CMRR and introduce additional thermal noise.

Instead of relying on the poorly balanced additional components and introducing additive noise to the input of the instrumentation amplifier by AC coupling with the RC-network, the DC-component could be attenuated by servo filtering, where the unwanted frequency content is separated from the filter output and subtracted from the filter input through a feedback loop. With active filters this is accomplished by connecting a high-pass filter from the output to the non-inverting input of the first stage operational amplifiers of the low-pass filter. [39]

Low phase distortion is preferable in biopotential acquisition, so Bessel topology is recommended for the low-pass filter with 100 Hz cut-off [5]. Bessel filters are optimized for maximally flat time delay, so their transient response is very accurate. The trade-off is poor flatness of pass-band and low roll-of rate at the stop-band. In an effort to achieve lower noise feed-through from out-of-band sources and thus achieve a more accurate front-end, Butterworth filter topology was chosen instead of Bessel. Butterworth has maximally flat pass-band response and 20 dB/decade per order roll-off at the stop-band, while having only moderate ringing in transient response. The out-of-band roll-off can be increased by cascading several filter stages. Stages are arranged in the order of increasing quality factor to prevent the signal clipping in the middle stages of the filter. [40], [41, p. 331]

The wanted filter polynomials can be realized using second order active filter stages in multiple-feedback architecture. The architecture is insensitive to component variations, has good performance at high frequencies and is easy to convert to a differential structure in order to minimize coupling of distortion and noise to the signal. [40] The designed single ended cascade of filter stages was converted to a differential structure with the simple principles depicted in [41, p. 413].

The resulting complete filter structure is a 0.7 Hz - 100 Hz bandpass made from a differential 8th-order Butterworth low-pass filter and high-pass servo feedback negation. The complete analog front-end structure from pre-amplifier to the filter was simulated in the in-built circuit simulation tools of Altium Designer using precise components models provided by the respectful manufacturer of each active component. AC simulation was used to extract the frequency response of the complete front-end, and to change the ideal component values to more easily available standard values. Simulation results are presented in Figure 15.

3.2.3 Multiple channel acquisition

Biopotential measurement front-ends often need to measure several channels simultaneously, EEG for instance is commonly measured using 30 electrodes in so called 10-20 placing around patients head [7, p. 175]. The acquisition of multiple channels can be done either by reserving dedicated ADC for each channel or by using a single ADC with a channel selector, such as a differential multiplexer, as it is accomplished in Figure 4.

Important parameters in choosing a multiplexer are crosstalk between the channels, digital feed-through from the channel selection controls to the channels themselves, switching time when changing the channel and settling time after the change. On-resistance is not a critical concern, if both input and output are sufficiently buffered to minimize path losses.

Location of the multiplexer in the front-end structure depends on the filter characteristics. If a filter is placed after the multiplexer, the settling time of the filter defines the maximum sampling rate: if signals in two adjacent channels are in near maximum amplitude but in opposite polarity when the channel is changed, this maximum settling from the previous channel value must be taken in to consideration. If the multiplexer is placed after the filter, each channel requires a separate filter. Using parallel filters requires several times more components, board space and introduces channel variability from component value variance in the different channels. However, this structure lowers the effective settling time needed when switching channels, enabling faster sampling rate for the following ADC.

The switching frequency of the multiplexer determines the ADC sampling frequency. Sampling circuitry before the multiplexer would allow for simultaneous sampling and measurement of all channels. This would greatly increase the accuracy of the collected data, as all channel samples would be from the same time instance. For development purposes the sampling circuit should track-and-hold type, so that the sampling functionality can be disabled if required. Addition of any sampling or track-and-hold functionality before the multiplexer was omitted as a suitable off-the-self component with 3.3 V supply was not easily found.

Without a track-and-hold before the multiplexer, effective sampling method in multichannel acquisition is to attain one sample per time window of the multiplexed channel. To increase sampling rate the multiplexer switching time is increased accordingly. For a signal with highest frequency component of f_{max} the minimum multiplexing and sampling rate R_{sample} with H_{count} channels is

$$R_{sample} = 2 * H_{count} * f_{MAX} \tag{10}$$

where 2 is the sampling rate requirement from Nyquist theorem. For EEG f_{MAX} is 100 Hz, and with 32 channels the minimum required switching rate is

$$R_{EEG} = 2 * 32 * 100 \text{ Hz} \tag{11}$$

$$= 6.4 \text{ kHz}. \tag{12}$$

The multiplexer must be able to switch at least at the rate from (12). Analog Devices ADG709 differential multiplexer with four channels and a two bit control is used. As the final step in the front-end structure of Figure 4, the measurement acquisition is done with Texas Instrument AD7450, a differential 12-bit analog-to-digital converter that offers very high speed SPI interfacing to the control logic for minimal overhead in reading the ADC. The read values can be digitally processed in FPGA, structured to packets and transmitted forward with the wireless communication front-end.

3.3 Wireless communication front-end

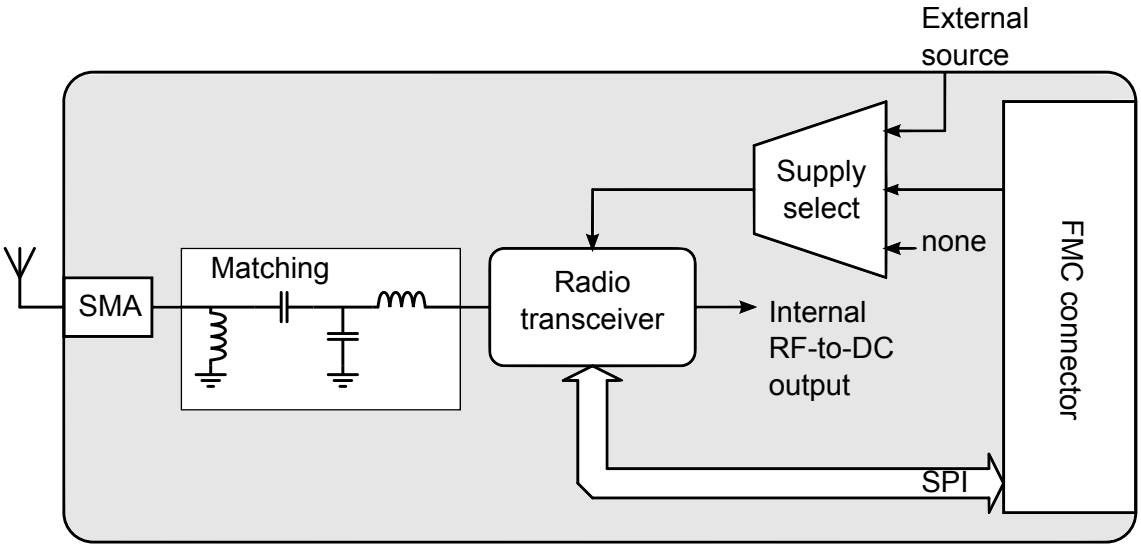


Figure 5: Structure of the implemented radio communication front-end module.

The structure of the wireless communication module of the implant is presented in Figure 5. The system uses a state-of-the-art RFID transponder front-end ams SL900A. The front-end supports EPC C1G2 protocol and a limited set of non-standard commands for faster reading of data through the radio link using a 8-byte first-in-first-out (FIFO) buffer. Communication to the control logic uses SPI and it can be programmed to generate interrupt requests for more time efficient operations. Connecting the SL900A to an external supply source enables the SPI communication and increases the radio sensitivity to -15 dBm. [42]

The implant radio front-end has three supply options. The first option is to use the regulated supplies of the FPGA board, and the second option uses the supply generated by the separate power module of the system (see Section 3.4). In the third option, the "none" option in Figure 5, no external source is connected and SL900A uses an internal RF-to-DC rectifier. The unregulated output of this rectifier can also be used to power other parts of the system. In default configuration the rectifier output is not used, as we design our own modifiable rectifier in a separate module.

If the communication and power extraction functionalities are to be operating at the same frequency, they should be close each other to imitate the implant operation.

The distances in the actual integrated circuit implementations of the medical implants and RFID systems are very short, so the data and power functions can be connected basically to the same point. This is important as the two operations affect each other and the overall impedance of the implant radio input. In a PCB the distances are relatively large, so if the single frequency operation is to be demonstrated in the modular design, a two-way power splitter can be used to connect the separate circuits to a single antenna. This is also a problem in dual carrier configuration, if the same antenna is used for both carriers [43].

In order to keep the design simpler and modular, a choice was made to separate the communication and power extraction to different modules. A specification of the frequency dependent behaviour of the input impedance of the SL900A was provided upon request, and this model was used in constructing a simulation model of the whole input structure of the communication module using S-parameter simulation in ADS simulation software. The simulation was used to match the SL900A input to a 50 Ω transmission line and a single SMA connector for antenna connection, using four component matching to maximize the available tuning topology options in case the matching needed to be adjusted later. A compromising solution to the distance problem between the different RF-circuits of the whole system would have been to connect and match the communication front-end in the middle of the transmission line leading to the power extractor, and having both RF input and RF output on the communication module. Unfortunately the simulations on ADS revealed the matching of such a structure to be very sensitive, especially when matching to dual carrier frequencies. Alternatively, power divider can be used to connect the communication module and the power and clock management module to the same antennas.

3.4 Power and clock management front-end

Power and clock management module (Figure 6) generates supply voltages for the other modules and a clock for the use of the digital logic. Extraction of power and clock from the dual radio signals is demonstrated using popular topologies used in integrated circuit implementations, but scaled to discrete component implementation. The module houses programmable supply voltage amplitudes, supply paths, clock dividers and clock paths for development purposes.

3.4.1 Power extraction and management

In order to extract power from radio signal to the use of supplying common electronic circuits, the alternating RF voltage needs to be rectified and regulated to stabile direct voltage. Creating a low power, high efficiency RF-to-DC rectifiers is challenging, as the non-linearities of diodes and rectifying transistors structures have an abrupt non-zero threshold level, under which no DC output is generated. A common way to minimize this threshold voltage is to use Schottky diodes with low turn-on voltage. [17, p. 478]

The voltage boosting charge pump structure in Figure 7, known as modified

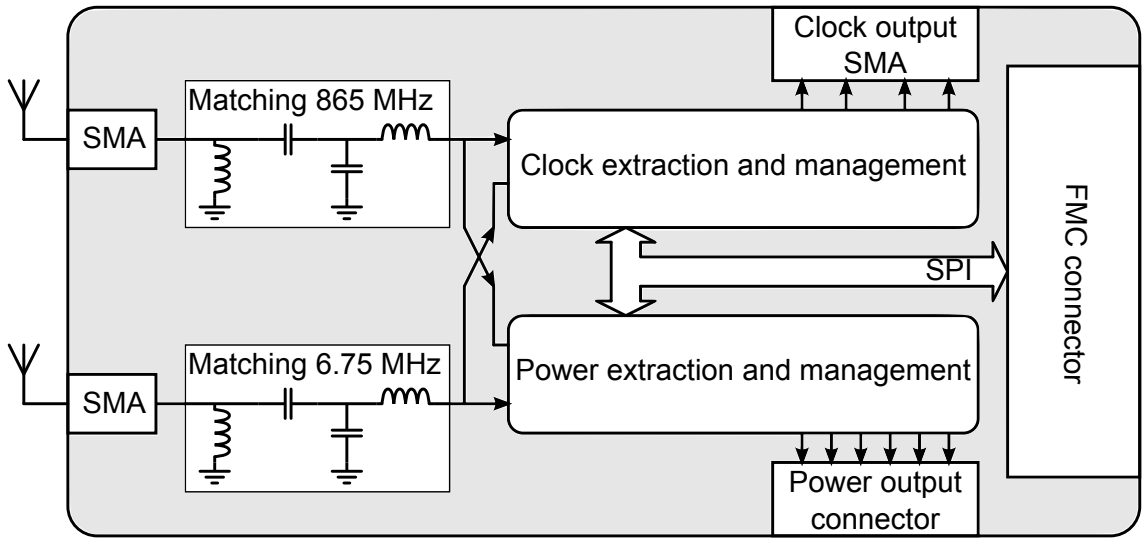


Figure 6: Structure of the implemented clock and power management front-end module.

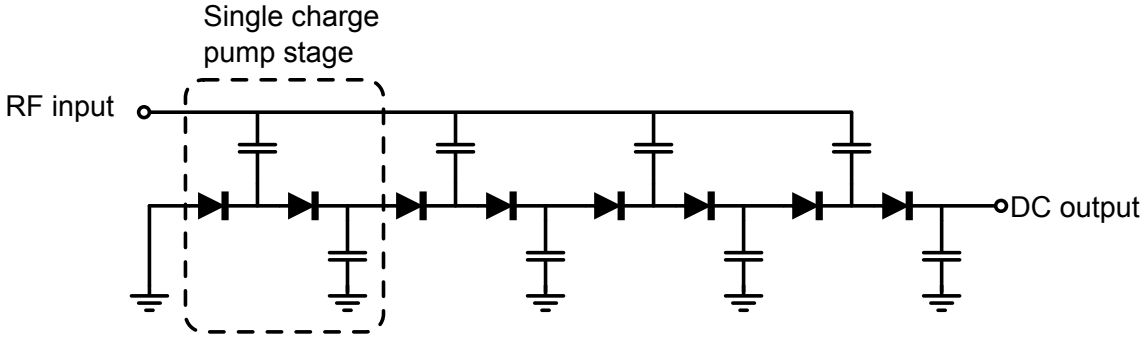


Figure 7: Chosen voltage boosting charge pump rectifier.

Dickson multiplier or modified Cockroft-Walton multiplier is a popular type of rectifier used with UHF medical implants [29] and RFID systems [44], [45]. Several voltage boosting rectifier cells can be cascaded to multiply the output to a level high enough to be regulated efficiently. The resulting multistage modified Dickson is straightforward to design and implement using discrete Schottky diodes and capacitors.

Two rectifiers , tuned to 865 MHz and 6.78 MHz respectively, are designed. The discrete component implementation is highly unlikely to give absolutely comparable results with IC integrated rectifiers, so the main function of the power extraction demonstration is to provide an interface to measure proportional metrics, such as the effect of different duty cycling or different modulation schemes to the available proportional power for the implant. For this the structure has reservations for connecting external measurement equipment to access the voltage and power after the rectifiers. The complete input structure was simulated in ADS simulation software using harmonic balance simulation. Linear simulations such as S-parameter extraction and AC analysis do not return accurate results with non-linear components, such as the diodes used in this design.

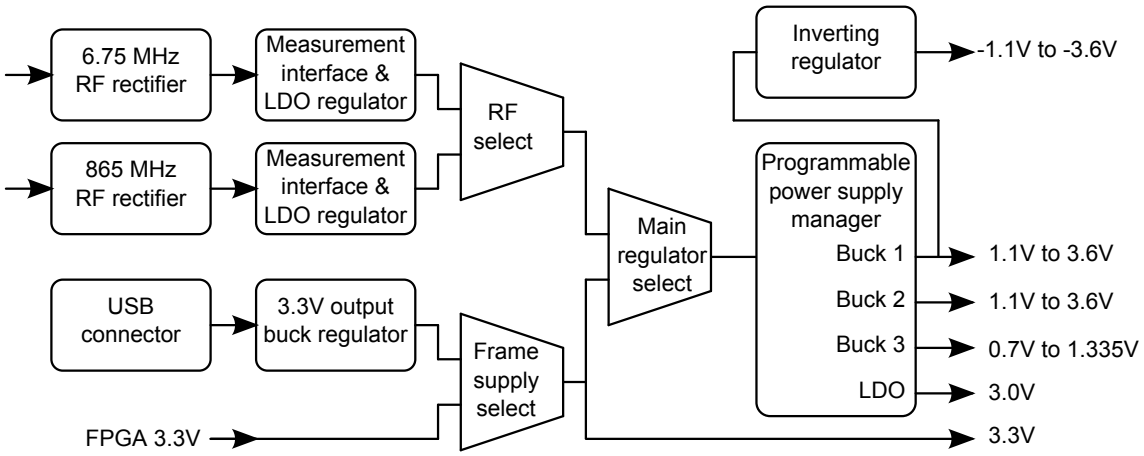


Figure 8: Structure of the implemented power extraction and management functionality.

The rectifiers are followed by a low drop-out regulators with high supply noise rejection ratio at high frequencies. Using voltage boosting switching regulators could have allowed the operation at lower input power levels, but the switching operation might have varied the impedance seen by the antenna as the switches open and close, effectively backscatter-modulating the signal and corrupting the radio communications.

Figure 8 presents the detailed block diagram of the implemented power management structure. For demonstration, parts of the system can be powered from the harvested energy, but for development purposes the system needs to be able to use a optional secondary source. The power extraction module has a power path manager structure (PPM) built with reverse current protected switches to choose from the supply sources. The development platform has programmability and modularity through frame structures surrounding the demonstrated implant operation functionalities. These frame structures, such as programmable regulators and inter-modular buffers, need to be constantly powered from a stable supply source. The power path manager structure provides options to supply them through an on-board regulated USB-connector or from the regulated supplies of the FPGA development board through the FMC connector.

The power module provides three programmable buck regulator outputs and one fixed LDO output through an programmable power manager TI LM10504. Programmable regulators enable the module to be used in the changing demands of the system, if new modules with varying supply needs are to be developed.

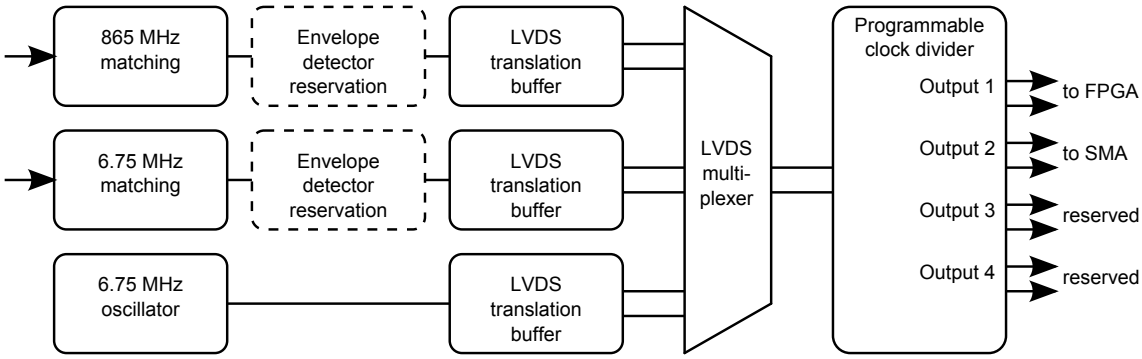


Figure 9: Structure of the implemented clock extraction and management functionality.

3.4.2 Clock extraction and distribution

The detailed clock management structure is presented in Figure 9. The clock extraction functionality in the designed system is achieved using a high speed sine-wave-to-LVDS buffer PL130-09. This component includes the aforementioned general clock extraction functionalities presented in section 2.4, with added integrated low voltage differential signal (LVDS) [46] output buffer. A well implemented LVDS clock distribution structure has benefits compared to single-ended solutions, mainly being less susceptible to noise and differences in ground potentials, as well as emitting less interference from the high speed clock edges. The clock recovery circuit is commonly followed by a phase-locked loop to minimize deviation in frequency and duty cycle [29], but this functionality was not incorporated in the demonstration platform.

The presented platform provides a way to extract the clock signal from either high or low frequency radio signals, in order to be able to evaluate the clock synchronization in both single and dual frequency scenarios. In a dual band application the clock should be generated from the lower carrier, as it is always available when the system is powered by the inductive link, holds constant level and form as no data is being modulated on this carrier, and requires less dividers to generate a low frequency clock signal. Clock from the higher frequency carrier could be used to develop and synchronize the radio and data transfer related operations. A reservation for a simple serial diode-based envelope tracker is provided for the option to change the clock extraction source from carriers to amplitude modulated subcarriers.

The clock distribution system in Figure 9 comprises of a differential multiplexer to select the clock source and a programmable divider to set the frequencies to wanted values. Clock can be sourced from either of the radio extractors, but the system has also an option to use a 6.75 MHz oscillator as a clock source in case the carriers are not available or stabile enough. Chosen multiplexer ICS854S057BI is a clock multiplexer, accepting the LVDS level inputs and repeating the signal in output LVDS driver with minimal delay and additive jitter. A normal differential multiplexer would have required a complex termination scheme for the multiplexed inputs, as a non-terminated lines might have operated as antennas, generating markable noise and crosstalk. Channel of the multiplexer is chosen by using a DIP-switch.

Table 3: Clock distribution division limits with AD9508 clock manager.

Clock source	On-board oscillator	HF carrier	UHF carrier
Nominal frequency	6.75 MHz	6.75 MHz	6.75 MHz
Min. frequency	6.59 kHz	6.59 kHz	844.73 kHz
Max. frequency	6.75 MHz	6.75 MHz	865 MHz

The output of the multiplexer is connected to a programmable 10-bit clock divider Analog Devices AD9508 [47]. The clock frequency can be divided by an integer in the range of 1 to 1024, the divider is set by SPI control. Table 3 presents the achievable clock output frequency options of the system, excluding the subcarrier options. 6.75 MHz is chosen as the nominal operation frequency of the system, as it can be easily generated from all clock sources. The AD9508 has four differential outputs that support a selection of both differential and single-ended signal level standards. One output is connected to SMA connectors for easy connection to measurement equipment, two are terminated and brought to the PCB edge for testing purposes, and one differential output is connected to the FMC connector to be used in development of control logic and algorithms.

3.5 Control logic

The development system requires a versatile, high performance control structure that has little restrictions for developing and testing different applications, control schemes and novel algorithms [2]. A field programmable gate array (FPGA) is a suitable platform for such prototyping and development [32]. Xilinx Zynq-7000 system-on-chip on a ZC706 development board (Figure 10) was chosen as the FPGA solution for this system [4]. The Zynq-7000 is divided two two sections; the programmable logic (PL) and the integrated hardware processor system (PS).

The programmable logic of the Zynq-7000 (bottom section of Figure 10) is a field-programmable gate array that can be used to generate a variety of different digital logic structures. To maximize modularity, all signals coming from and going to the other modules are routed through the PL. These signals can be connected through a output multiplexer to any of the possible output pins of the FMC connectors, as set by the VITA 57.1 standard [34]. The input and output logic levels and standards can be chosen from a variety of options, including both single-ended and differential options. If no other control logic is used in the PL side, all the signals are routed through extended multiplexing input/output interface of the Zynq-7000 to the processor system.

The processor system section of Zynq-7000 (top section of Figure 10) has embedded dual ARM Cortex A-9 microprocessor cores. PS has several common peripheral devices that the cores can use in communication and control of the system. Most relevant for this system are the two SPI controllers, two universal asynchronous receiver/transmitters (UART) controllers, general interrupt controller, and the general purpose input/output (GPIO) controller.

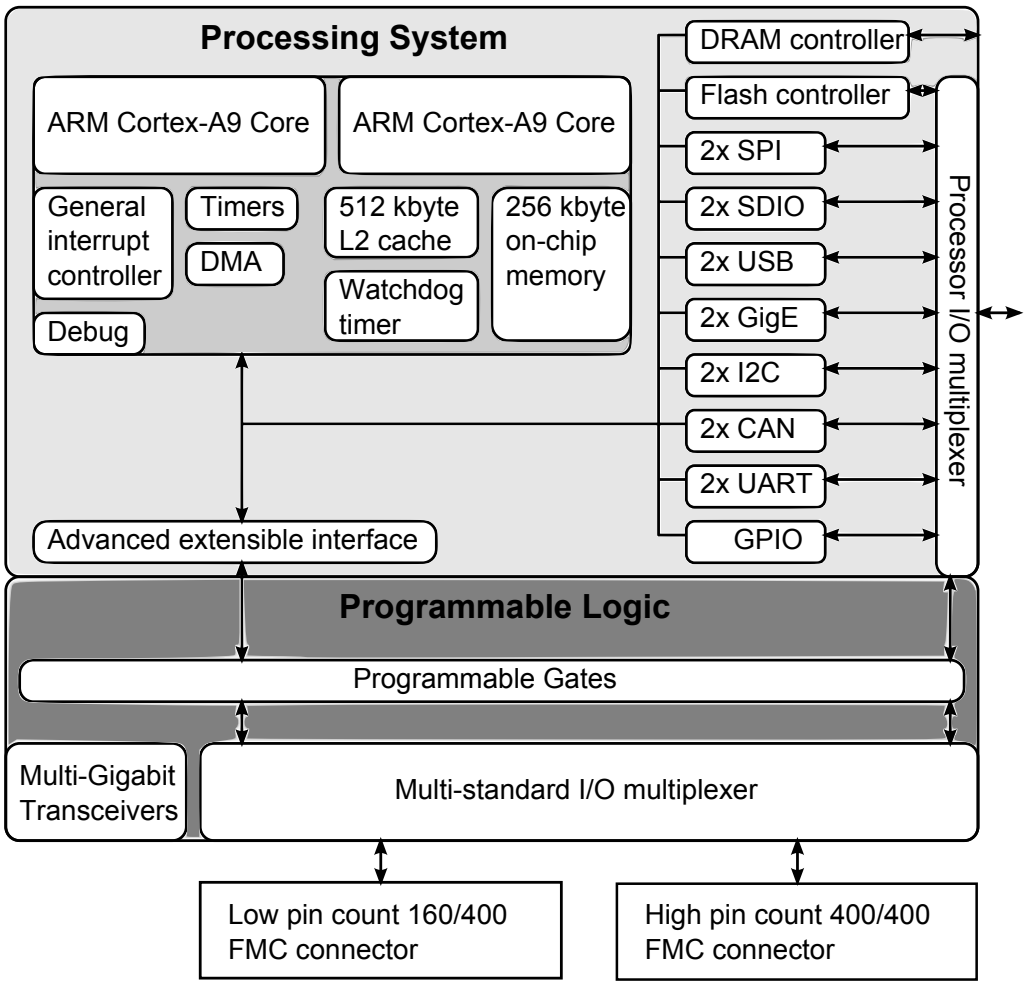


Figure 10: The main blocks of the Zynq-7000 system-on-chip on the ZC706 development board.

3.6 External reader device

The wireless implant in Figure 3 needs an external reader device to generate the power carrier, communicate with the sensor device, read and store the wirelessly transmitted biopotential measurement data and to transmit the data forward for further analysis or storage on PC. Objective is to create a extendible reader device that could be used also with a real integrated circuit implementation of the wireless sensor implant. Figure 11 presents the main functions of the implement reader device module.

3.6.1 High frequency carrier generation (6.75 MHz)

The 6.75 MHz high frequency (HF) carrier generation functionality of the bottom left of Figure 11 is realized with a class-E power amplifier presented in Figure 12. Basic class-E amplifier consists of a transistor switch supplied by a shunt-feed inductor L1, followed by a tuning bank of parallel capacitor C1 and a series C2 and L2. The tuning

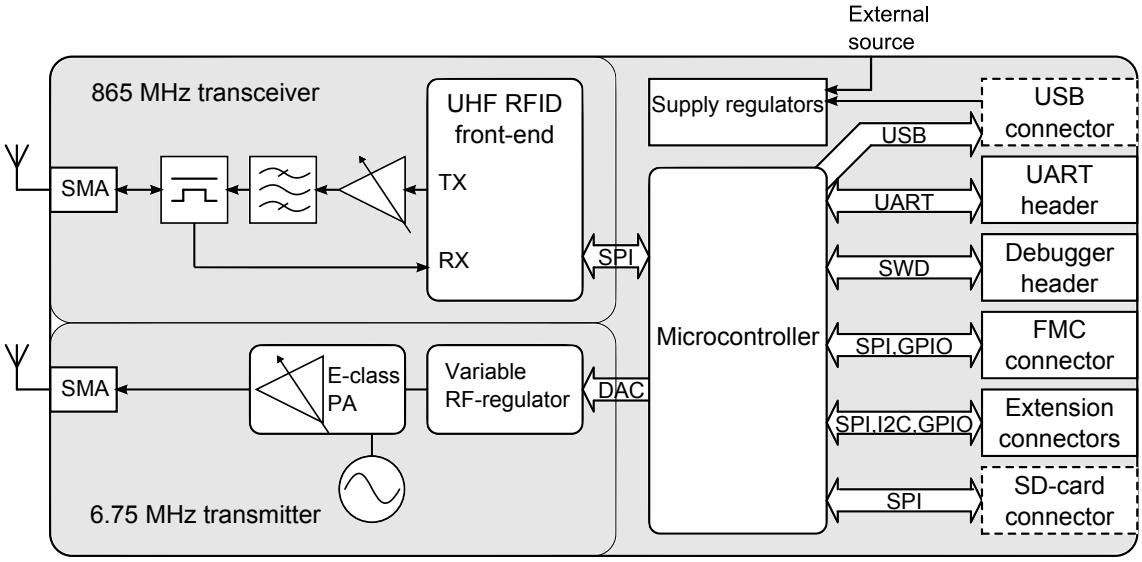


Figure 11: Structure of the implemented external reader device module.

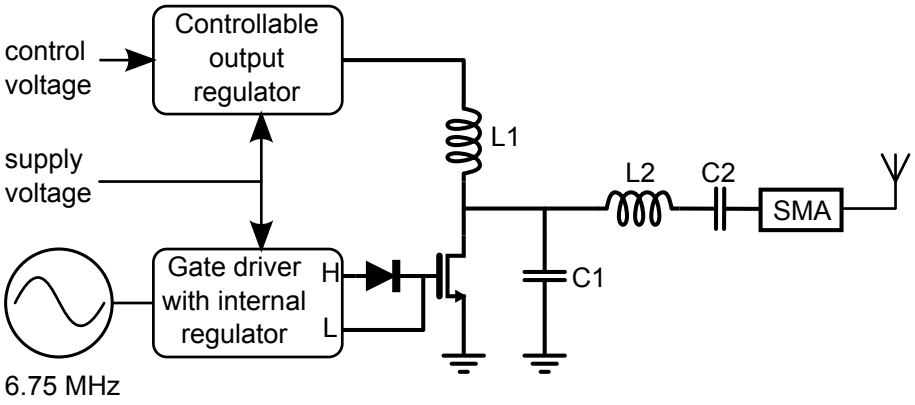


Figure 12: 6.75 MHz controllable carrier generation using E-class amplifier structure.

calculations of the E-class are not trivial, as the tuning bank is not in resonance at the output frequency [48]. The component values were calculated with the formulas from [48] in accordance to the practical design considerations given in [17, p. 445].

Design errors in the tuning and other structures of the amplifier are likely to lead to unideal switching and consequent high switching losses. A transistor with high current rating was chosen so that the initial errors would not lead to transistor breakdown. The chosen transistor was N-channel metal-oxide-semiconductor field-effect transistor MOSFET TI CSD16415Q5 [49]. Transistor gate driver UCC27611 from Texas Instruments was used to provide better switching accuracy and reduce the switching noise leakage to other parts of the system. The chosen gate driver has an internal regulator that supplies its two output drivers for sourcing (H in Figure 12) and sinking (L in Figure 12) current from the transistor gate, thus increasing the drive strength and speed. The gate driver and thus the intended output frequency of the whole class-E amplifier structure is set by a 6.75 MHz oscillator.

The output power of a class-E power amplifier can be controlled by changing the

DC voltage level fed to the shunt-feed choke of the amplifier structure, represented by L1 in Figure 12. A variable output regulator, with high power supply ripple rejection rating, was used to provide a stabile power output. The output voltage level is defined by the reference voltage input generated by either from an external voltage source or the DAC of the microcontroller through a level translating amplifier.

3.6.2 Ultra high frequency communication (865 MHz)

The design of the ultra high frequency (UHF) RFID communication system (top left of Figure 11) is based on the structures and principles provided in ams reference designs for AS3992 UHF Reader IC [50], that were also used successfully by Xia et al. in [51]. AS3992 was chosen as the communication front-end for the external reader module, as it offers a full support of the EPC C1G2 protocol in the frequency range of 840-960 MHz. The protocol handling can be modified extensively or totally bypassed, giving access the subcarrier data directly, so that the developers can easily create custom protocol using the AS3992 only as a modulator and demodulator. The UHF reader IC can be controlled through SPI and it provides an interrupt request pin to inform the microcontroller when attention is required.

The transmitter has an internal +20 dBm power amplifier output and a optional differential 0 dBm output. The internal amplifier has a very limited gain control range, so to provide more accurate control of the output an external power amplifier is used with the 0 dBm output [50]. Differential, variable gain power amplifier ADL5331 from Analog devices provides a linearly controllable range of -18 dBm to +15dBm at 900 MHz [52]. The gain is controlled with a single reference voltage with range of 0.1 V to 1.45 V, that can be generated using the internal 8-bit digital-to-analog converter (DAC) of the AS3992 followed by a level translating amplifier.

During reception the transmitter provides a constant carrier for the implant radio front-end to modulate using amplitude shift keying or phase shift keying, as required by the EPC C1G2 standard [3]. A directional coupler is used to separate the strong transmitting signal and the received weak backscattered signal [53, p. 320]. AS3992 has a direct conversion receiver to detect and demodulate the received data and an internal received signal strength indication measurement system that can be used to determine the backscattered power levels.

3.6.3 Microcontroller and PC connections

Freescale KL25Z microcontroller unit (MCU) is used to control the external reader operations. The main function of the embedded microcontroller in Figure 11 is to handle the RFID communication to the implant by controlling the radio front-end according to the commands coming from PC. The MCU also controls the output power levels of the two transmitters, storage of received measurement data and optional wired bypass communication with the implant.

KL25Z from Freexcale Kinetis L series is a low power microcontroller with 48 MHz ARM Cortex-M0+ core and high speed communication peripherals. The reader communicates with a personal computer (PC) using UART at a baudrate of 115200 bps. KL25Z has also a universal serial bus (USB) controller, so a micro-USB

connector can be used for PC communication and for an optional supply source. A FMC connector enables direct communication between the implant system and reader system.

Two extension connectors are provided for future expansion of the reader functionalities. A selection of peripheral controller connections from the MCU and supply options from the regulators are routed to these connectors. The extensions could include new radio front-ends for testing other frequency ranges and communication schemes, additional memories for enhancing the storage capabilities, or alternative PC connections, such as an ethernet peripheral controller.

3.7 Software

The development system in Figure 3 is to be controlled by a serial connection from PC through Matlab. The default communication hierarchy is analogous to automated measurement equipment, where the PC operates as the master by sending commands for the slave devices to perform. Matlab multi-paradigm numerical computing environment was used to create a application in the PC side utilizing object oriented programming. The same communication object classes were later utilized in interfacing with the laboratory measurement equipment used to characterize the developed system. Both the implant and the reader house capable microcontrollers, so more sophisticated means of control could be developed in the future.

3.7.1 Implant side control

The implant control software architecture presented in Figure 13 supports the incremental development of digital logic for control and analysis algorithms, as any and all incomplete digital logic can be fully handled in the processor instead. All signals to and from the modules are digitally routed to the programmable logic section of the Zynq-7000.

Control application for one core of the dual core Cortex A-9 processor was written in C programming language using the Vivado SDK environment. Application and drivers for controlling the different devices on the modules have been developed utilizing Xilinx standalone operating system, the general interrupt controller and the peripheral controller driver structures. The application is constructed so that making changes on the modular hardware requires minimal changes in software.

3.7.2 Reader side control

Reader control software (Figure 14) utilizes FreeRTOS real-time operating system ported to the KL25Z microcontroller. FreeRTOS has also been ported to Zynq-7000 SoC, it could be enabled in the implant side in the future. The reader application executes prioritized operations on the reader device according to commands received from a PC. Device drivers for the power carrier control, EPC communication front-end and PC communications are developed utilizing the nested vector interrupt controller and SPI, UART and GPIO peripheral controllers. The application utilizes time and power efficient low level peripheral drivers written by Jani Hevosoja [54].

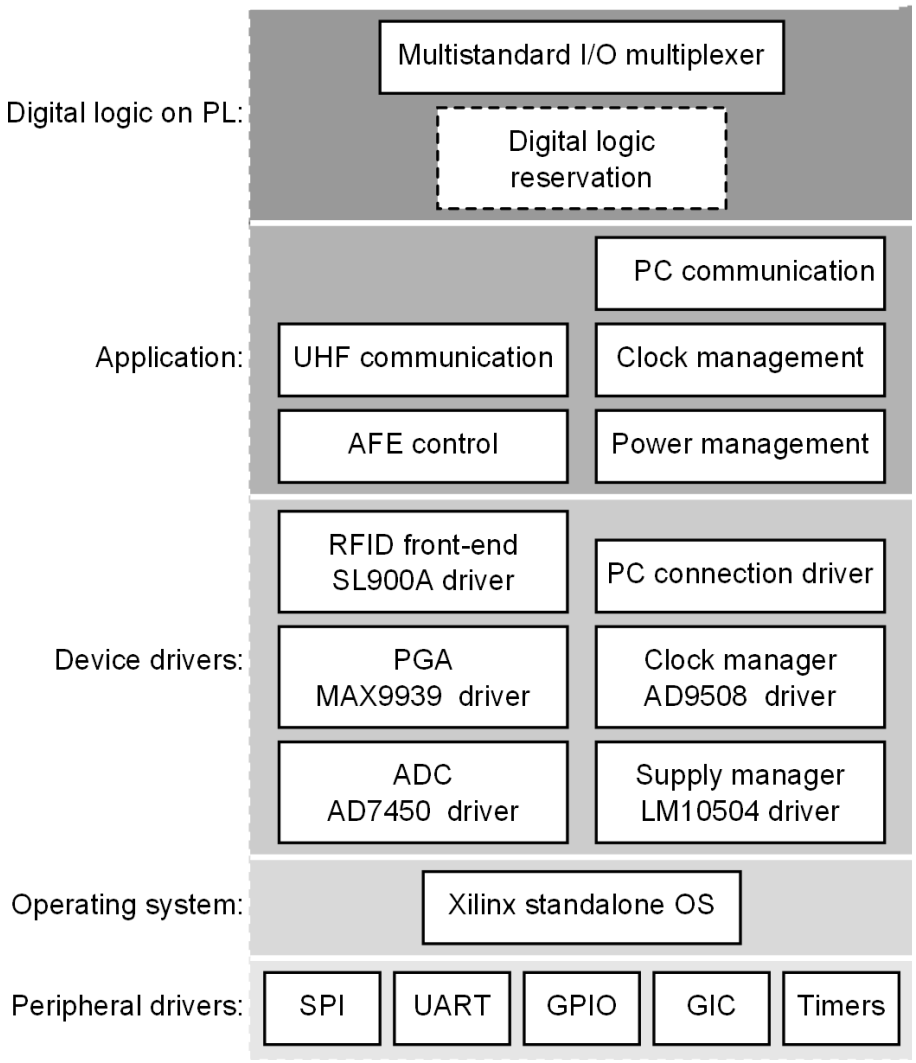


Figure 13: Structure of the implant development software.

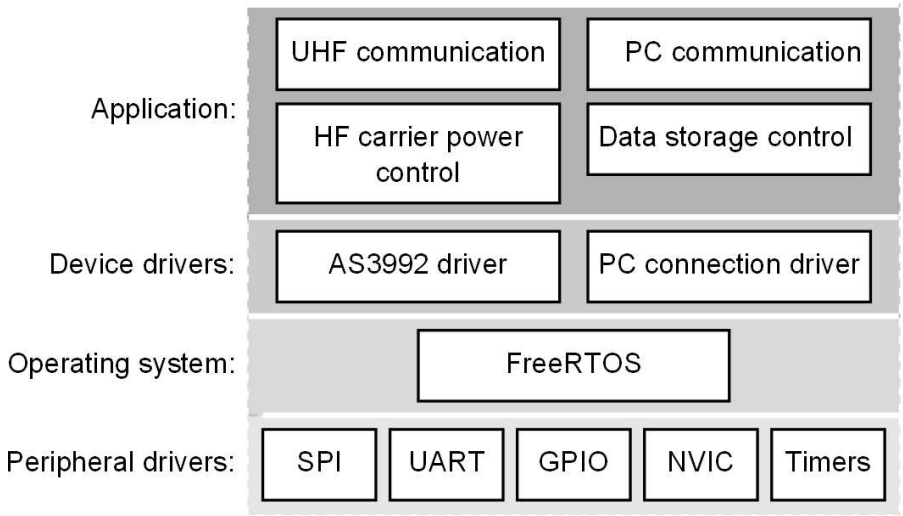


Figure 14: Structure of the reader development software.

4 Analysis of implemented design

This section presents the finished implementation, measurements of the key characteristics and design highlights. Measurement setups, methodologies and results are explained.

4.1 Measurement methodology

The measurement configuration planning started by determining the key parameters in the early design of the system. All printed circuit board layouts were designed with intention to provide ample space and measurement points for the characterization measurements. The actual measurements were divided to two phases. In the first phase all of the core functionalities were verified module by module, and accurate measurements were done only if the performance was as expected. This way the time and priority for handling the found performance inefficiencies could be divided in justified manner for the second phase, that included case studies of the most critical design aspects and found problems. Fixes were made only after the likely root cause of the problem was located and explained by case study. The used simulation models were updated to reflect the true performance, so that any future modifications could be evaluated in simulation.

First common verification steps for all boards were to inspect all the components for correct orientation and all significant supply lines for short or open faults. These verification tests were done by hand, checking the boards visually and with the help of Fluke 179 hand-held multimeter.

Correct operation of the control signals between the modules and the FPGA was verified. The lines were probed with Lecroy PP009 500 MHz probes connected to LeCroy Wavesurfer 424 oscilloscope. The waveform was checked visually for correct voltage levels, rise times and correct transmitted binary values. It became obvious that more test points should have been placed on both sides of the voltage buffers of the digital lines for easier probing of signals, and generally all the excess space on the boards should have been used to house additional through hole test points for measurement connections of different low speed lines. Lack of test points on some lines was compensated by manually soldering small connection wires to the appropriate component pins and printed circuit lines.

Rest of the measurements were dependent on the specific functionality of each respectable module. The critical measurements were automated to perform several accurate, repeatable multisample acquisitions with decreased time and effort required compared to operating the equipment manually [55]. Measurement equipment were interfaced to a PC through General Purpose Interface Bus (GPIB) or Transmission Control Protocol / Internet Protocol (TCP/IP), depending on the interface options available on equipment. The controlling structure of both the implant and the external reader was developed to be similar to a general remotely controlled instrumentation equipment (see section 3.7.1).

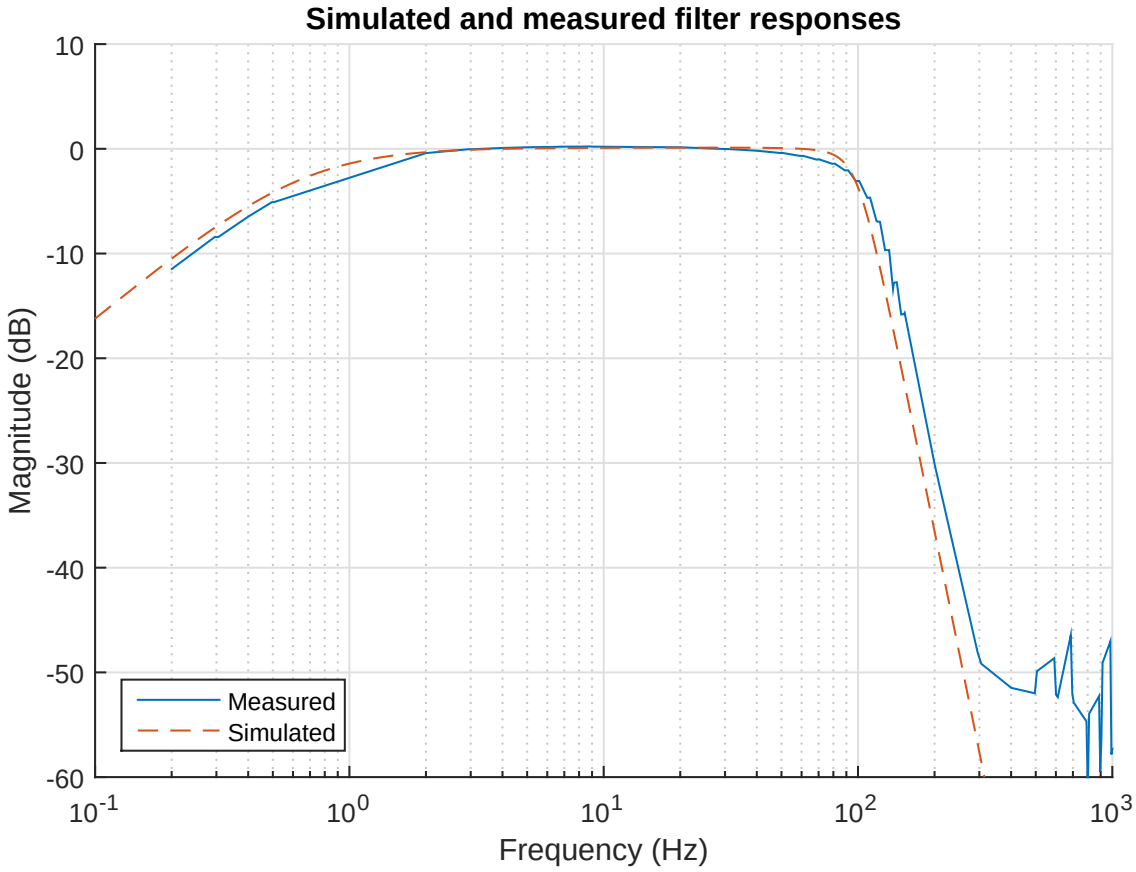


Figure 15: Simulated and measured frequency responses of the implemented passband filter.

4.2 Biopotential measurement front-end module

The performance of the analog front-end determines the suitability of the system for actual biopotential measurements. The module was characterized to verify the response of the filter and correct amplifier operation, and to measure the linearity, noise and harmonic operation of the complete analog front-end structure.

4.2.1 Filter response

Filter response measurements were performed by using Agilent 33220A 20MHz Function/Arbitrary Waveform Generator to feed a sine signal to the filter input at target frequencies. The differential input and output waveforms were measured using two channels of Lecroy WaveSurfer 424 200 MHz Oscilloscope. The system was powered from HP E3631A Triple Output DC power supply. Results were transferred to computer, where the response was calculated using discrete Fourier-transform.

The measured frequency response of the differential multiple-feedback eighth order Butterworth filter with servo feedback presented in Figure 15 shows that the implementation has succeeded with reasonable accuracy, and the simulation has been valid. Using the simulation to design the filter response enables shorter

design cycles when modifying the filters for the varying acquisition needs of different biopotentials. Modifications to filtering require resoldering components on the board, so the versatility has been acquired at the cost of time and effort to make the required changes. A filter structure with programmable passband setting would have been a better solution.

The designed system itself is not sensitive to the noise coupled from external sources, because to front-end layout follows the practices of minimized loop areas, differential design, and high CMRR. However, the long unshielded wires used to connect the measurement electrodes to the front-end can capture the 50 Hz line noise originating from power lines and other nearby electrical equipment, and practical EEG measurements have shown that the resulting noise component can be of higher amplitude than the actual biopotential signals, saturating the dynamic range in high gain settings. The problem is that the 50 Hz line noise resides inside many of the desired biopotential signal frequency bands (see Figure 20), so even implementing a high order notch filter with very narrow stopband region around 50 Hz results in losing some of desired signal information. The recommended solution for problems with line noise is to carry out measurements only in shielded environments or use shielded cables.

4.2.2 Analog-to-digital conversion characterization

The operation of the analog front-end was characterized to extract the static linearity and dynamic performance metrics of the implemented structure as a whole. The voltage gain setting of the analog front-end in these tests was approximately 80 dB. Multiple definitions and test methods for ADC characteristics exist, the metrics used in this work were defined in section 2.1. The static non-linearity was characterized using a histogram test [56], where a 15 Hz in-band sine wave was fed to the input of the analog front-end, and the amplitude was set so that the ADC input was slightly clipped. A significant amount of samples (over one million) was acquired with a sampling rate of 4500 samples per second, and the code density of the measured data was compared to a calculated ideal code density.

Figure 16 reveals that the front-end has poor integral linearity. The INL in Figure 16d is presented in best end-point fitting which typically gives an accurate value. The total INL error is approximately ± 5 LSB, corresponding to a ENOB of approximately 8.7 bits according to (6). The AD7450 ADC has a specified INL range of ± 2 LSB, so the amplification and filtering stages are likely responsible for most of the resulting non-linearities of the front-end. High rate of change in at the low and high end of the output codes may also indicate calculation errors, mainly on the correctness of the ideal spread calculation, gain error correction and DC-offset correction.

Dynamic frequency performance was characterized with DFT method descrided in the IEEE standard 1241-2010 [18]. Hann window was applied to the sampled time domain signal to reduce and manage the effects of spectral leakage [18], [56]. EEG measurement systems are sometimes tested with a 10 Hz square wave signal of 50μV amplitude [16], but the available Agilent 3320A signal generator can not output such a low amplitude. Attenuator of -40 dB was added to the signal generator output to

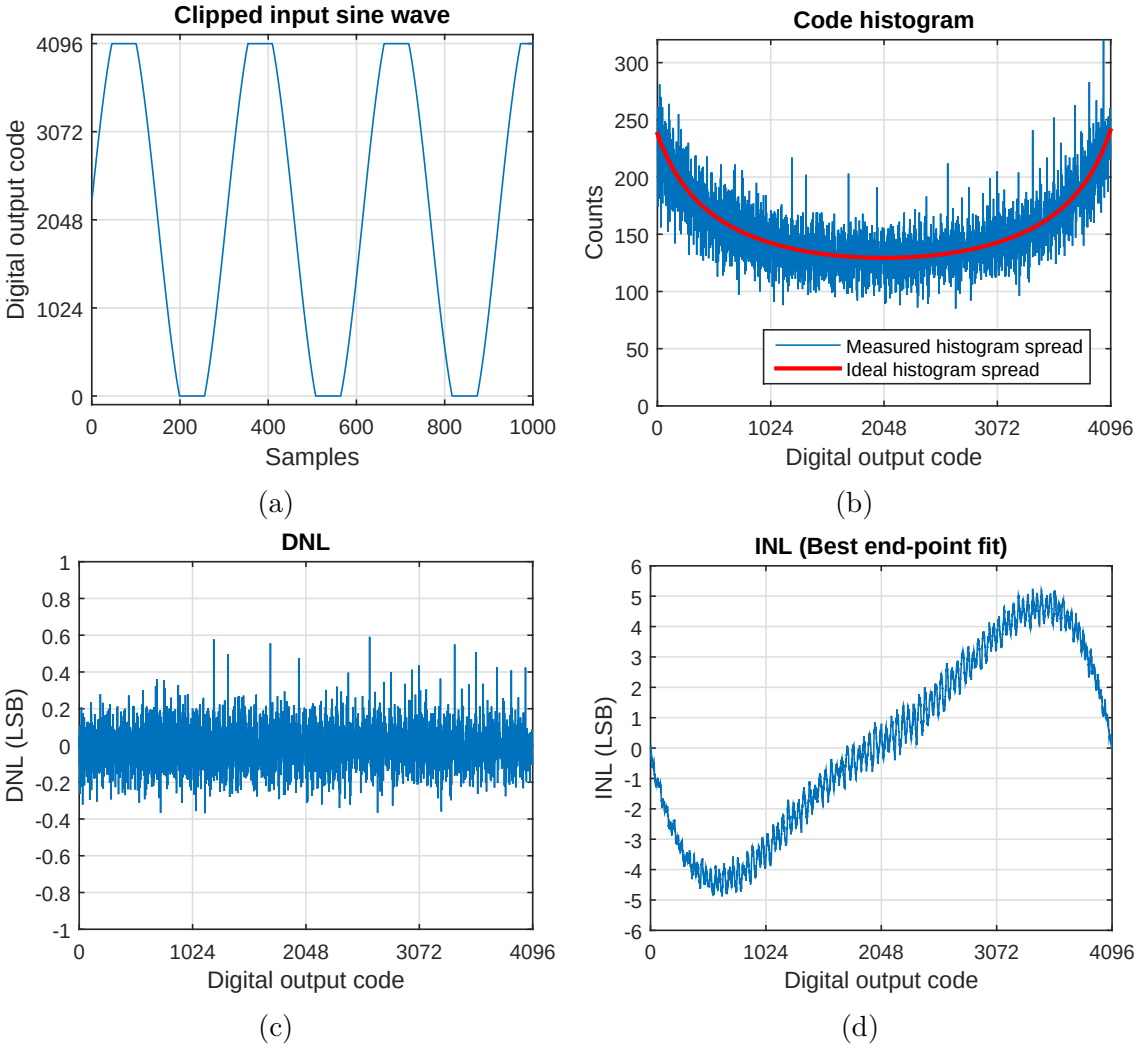


Figure 16: Histogram method to claculate the static nonlinearity metrics: a) 20 Hz clipped sine wave input, b) corresponding ideal spread and measured spread of digital codes, c) DNL and d) INL.

create a 15 Hz sine wave of peak-to-peak voltage of 1.32 mV, that corresponds to normal EMG, ECG or epilepsy peak level EEG. The measured dynamic characteristics are presented in Figure 17.

Figure 18 depicts the measured SNR and SNDR in relation to the amplitude of the fundamental 15 Hz input signal. THD can be approximated as the difference between SNDR and SNR. SNR raises steadily as the amplitude increases, until after 1.5 mV the dynamic range of the system is surpassed and the harmonics generated by the clipped signal corrupt the calculations. SNDR rises with the SNR until the high harmonics of the sine wave caused by the non-linearities of the system start to dominate the performance, causing SNDR to set to a level of 56 dBc. Corresponding effective number of bits is 9 bits according to (6). The ENOB calculated previously from INL was only 8.7, but the small difference is explained by inaccuracies in measurements and calculations.

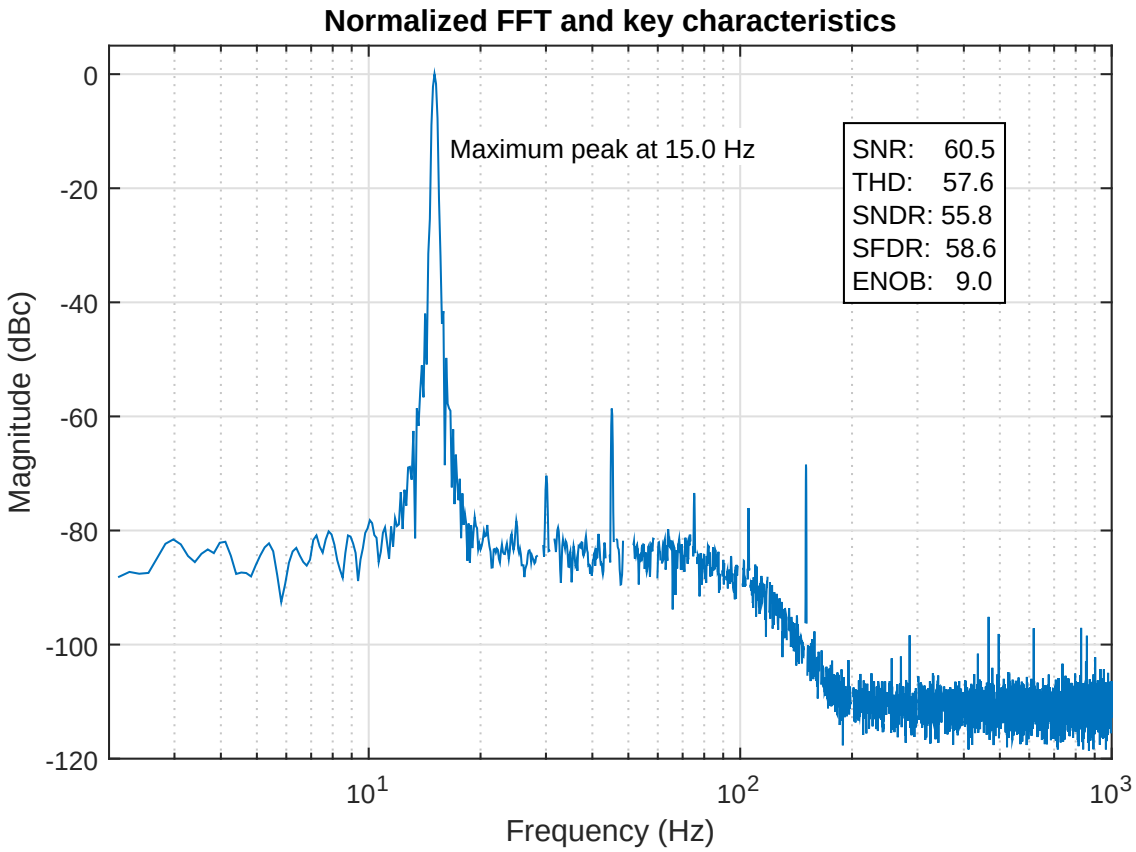


Figure 17: DFT with 1.32 mVpp 15 Hz sine wave and the key dynamic characteristics of the analog front end.

The channel count of the system can be modified by using the multiplexers to select input channels on each analog front-end board and by stacking more of these boards to the FMC-connectors. Up to four boards can be stacked to one connector, each assigned one of the four available chip select lines using a DIP-switch. With two FMC connectors available on the ZC706 FPGA development board, the channel count can be modified in increments of four between 0 and 32. The system was tested up to 16 channels, using a stack of four boards on one FMC connector. The maximum achievable sampling was not properly characterized, but the tests were performed using 4500 samples per second without any problems, so the system is capable measure most biopotential signals up to at least 2250 Hz.

4.2.3 Gain settings ranges

The gain of the instrumentation amplifier INA333 can be modified by choosing a suitable resistor value for the gain setting common resistor of the instrumentation amplifier. The overall gain accuracy of the instrumentation amplifier or the following single-ended to differential conversion structure was not characterized by measurement, as the accuracy is likely to be dominated by the accuracy of the gain setting resistor value [36].

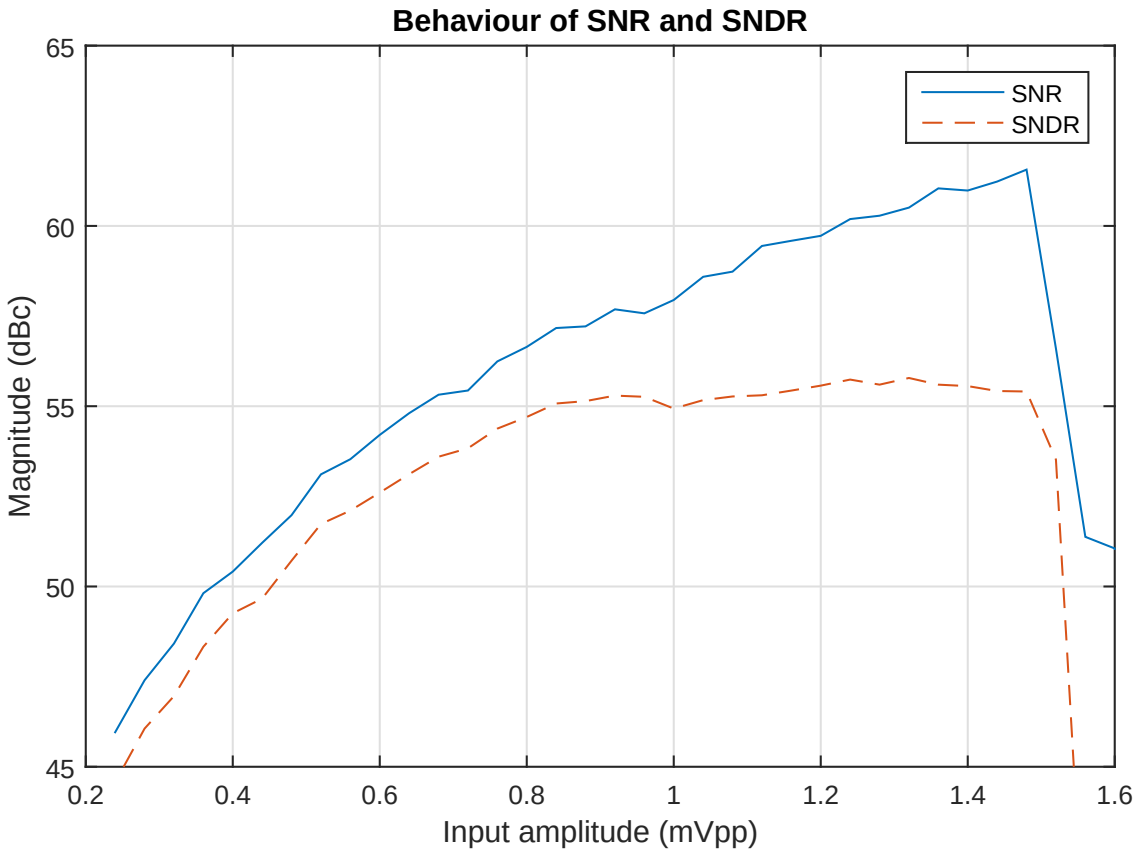


Figure 18: Behaviour of signal-to-noise ratio (SNR) and signal-to-noise-and-distortion ratio (SNDR) with increasing signal ampltiude.

If resistors with 1% accuracy are used and temperature drift is neglected, the approximated gain error at gain of 1000 is

$$\text{Gain error \% @ 1000 V/V} = \pm\frac{|Gain_{ideal} - Gain_{max.error}|}{Gain_{ideal}} * 100\% \tag{13}$$

$$= \pm\frac{|1000 - \left(1 + \frac{1000}{10\pm1\%}\right)|}{1000} * 100\% \tag{14}$$

$$= \pm 0.9901\% \tag{15}$$

Differential programmable gain amplifier MAX9939 operates as specified in the datasheet [37]. Full control of gain and input offset trimming in specified ranges is achieved with control through SPI. In order to minimize the effect of the internal input offset voltage of the PGA, a calibration procedure function was implemented to the processor system. The calibration algorithm sets the programmable gain amplifier to calibration mode, reads the resulting output value through ADC, calculates the effective input offset by dividing the measurement by the current gain of the amplifier, and finally adjusts the input offset trim of the PGA accordingly. This cycle is repeated until the offset is smaller than one offset step value of PGA.

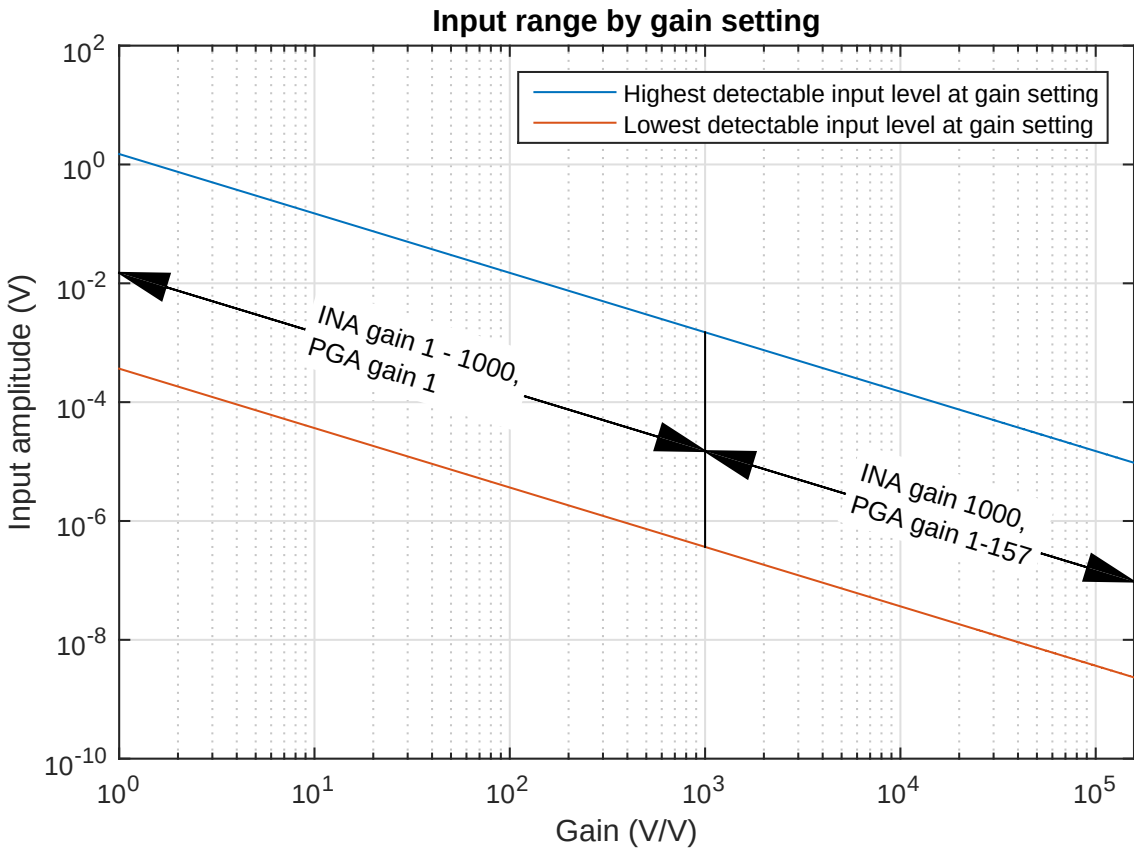


Figure 19: Input range options of the implemented biopotential measurement front-end.

The gain can be set from 1 to 157000 in order to accept a wide range of input amplitudes, as shown in Figure 19. As the frequency response of the filter can also be modified, the implemented analog front-end structure can be used to measure many different signals other than EEG, such as EMG or ECG. Figure 20 shows the tested input amplitude and sampling rate of the implemented analog front-end in reference to the requirements of different biopotentials.

Following the refined design practises of biopotential measurement front-ends discussed in section 2.1 have given a good overall result. Using off-the-self measurement front-ends that have integrated filters, multiplexers and analog-to-digital converters would have probably shortened the development time of the system and in many cases given more programmability in form of digitally tuned filtering. On the other hand, breaking the structure to smaller units has given a better demonstration of the different stages needed in the measurement front-end of the actual implantable device. The sources of the front-end non-linearity should be analysed in-depth in order to raise the ENOB in possible future revisions. The revisions should also be designed with an optional notch filter for demonstrating the biopotential acquisition in noisy environments.

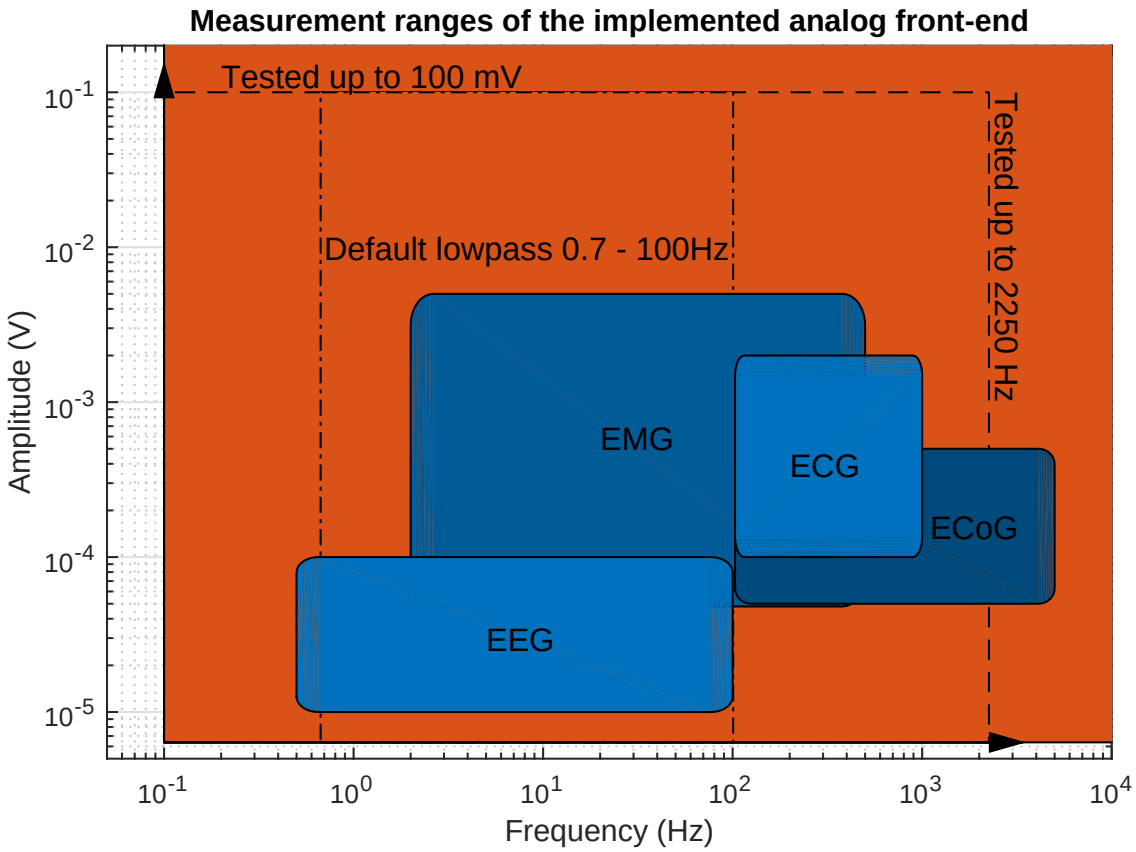


Figure 20: Acceptable input signal ranges of the implemented biopotential measurement front-end, the default filter setting, the tested range, and the requirements of different biopotentials.

4.3 Wireless communication front-end module

The radio communication front-end utilizes SL900A RFID front-end, that is a fully integrated system with minimal access to the internal operations. The only significant measurable metric of the communication module is the matching of the input, so that 50 Ω coaxial cables and antennas can be used and antenna development has accurate impedance data. The internal RF-to-DC rectifier output of the SL900A was not measured as its topology is not well known, its performance cannot be affected and it is not a primary power source to anything. Measurements were conducted by measuring the reflection coefficient of the antenna input with a calibrated Agilent 8722ES vector network analyzer set to -15 dBm power. Assuming that the losses on the short 50 Ω cable used to connect the equipment were negligent and the calibration was successful, the measurement accuracy is determined by the analyzer accuracy which is better than ±10 parts per million in frequency and ±0.6 dBm in level.

Figure 21 shows input impedance measurement initially and after the matching circuit was tuned. Initial measurement of the radio signal input of the wireless communication revealed the original tuning to be significantly different from simulation results. Reasons for the mismatch were determined to be the inaccurate simulation

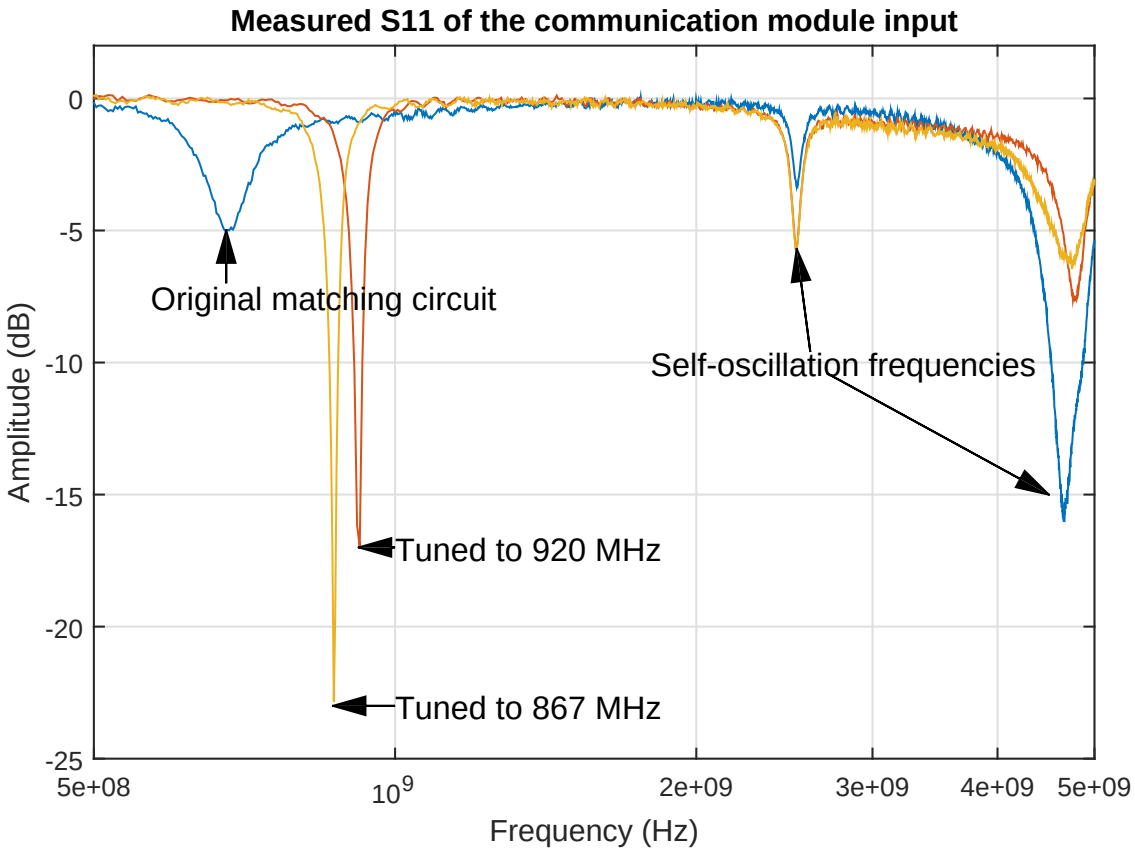


Figure 21: Input matching of the communication front-end module.

model used for the developing the matching circuit and inaccuracy in SL900A port impedance model received from manufacturer. Initial matching simulation model did not account for the narrowing of the transmission line at the connection to the SL900A RF-input pin. This piece of coplanar waveguide is considerably thinner than the rest of the actually matched transmission line, and was found to have significant impact to the impedance despite being only 2 millimeters long.

The SL900A input impedance was initially modeled after a dedicated application note [57]. The measurement results given at the application note were presented in unclear manner, in a low resolution graph without sufficient legends or explanations. The input impedance of passive RFID front ends is highly dependent on the input power level and input frequency, so providing accurate impedance models is critically important. The whole transmission line and matching circuit structure was remodeled to match the measurement results, and the resulting model was used to extract the effective input impedance of the SL900A. The input of the SL900A seen in this implementation was found out to have a larger resistive component than stated in the application notes. A possible reason is the decreased current consumption of the internal radio frequency energy harvesting rectifier of SL900A due to the chip being powered externally. The revised model was used to successfully create new matching circuits for 837 MHz, 867 MHz and 920 MHz frequencies.

SPI communication with SL900A has exceptionally long hold times compared to

the other components utilizing SPI in this system. The front-end supports SPI clock frequency up to 10 MHz, but requires 150 μs setup time between each packet of data sent through SPI. As the maximum datapacket to SL900A would be 2 command bytes followed by 8 payload bytes, the maximum effective datarate trough SPI is

$$\text{Datarate} = \frac{8 \text{ payload bytes}}{\text{setup time} + \text{transmit time}} \tag{16}$$

$$= \frac{64 \text{ bits}}{150\mu s + \frac{80}{10 \text{ MHz}}} \tag{17}$$

$$\approx 405 \text{ kbits/s}. \tag{18}$$

The resulting effective datarate is enough to handle the data generated by the 32 EEG channels that was calculated in (9). Excess datarate in SPI to the radio front end is beneficial in order to test different radio transmission schemes, such as retransmission in case of errors are detected in the payload.

Compared to the other functionalities of the whole system, this front-end intended to imitate the radio front-end of the implant has very little modification and programming possibilities. The chosen radio SL900A does not support creating fully custom RFID commands and protocols in the same extent as the reader front-end AS3992 does, only a few commands differing from the EPC C1G2 standard are available, predetermined by the manufacturer. As the operation of the comparable ASK modulator and demodulator is rather simple [53, p. 43-45], the design could have been separated to discrete parts in the same way that was done with the analog front-end. This would have provided considerably more development possibilities, such as easier development and testing of radio communication schemes, at the exchange of time and effort needed to design and match the related hardware and to develop some basic communication protocol base structure in digital logic.

Even though the complexity of the wireless communication module is very low compared to the other designed modules, the same principles of design precaution proved to be very useful. Especially the additional matching circuit component reservations made the tuning easier in the unexpected input impedance problem.

4.4 Clock and supply management module

The clock and power functionalities were verified and characterized. Power management metrics of interest are the threshold levels of the power extractor operation, control of the power path manager, and control of the programmable regulator. Meaningful clock metrics are the operation threshold levels of the clock extractor and the clock jitter.

4.4.1 Power extraction output levels

Testing the four-stage RF-to-DC rectifier started by making considerable modification to the system due to design errors. The 0402-packaged Schottky-type diodes were all the wrong way around due to a mistake in creating the component footprint,

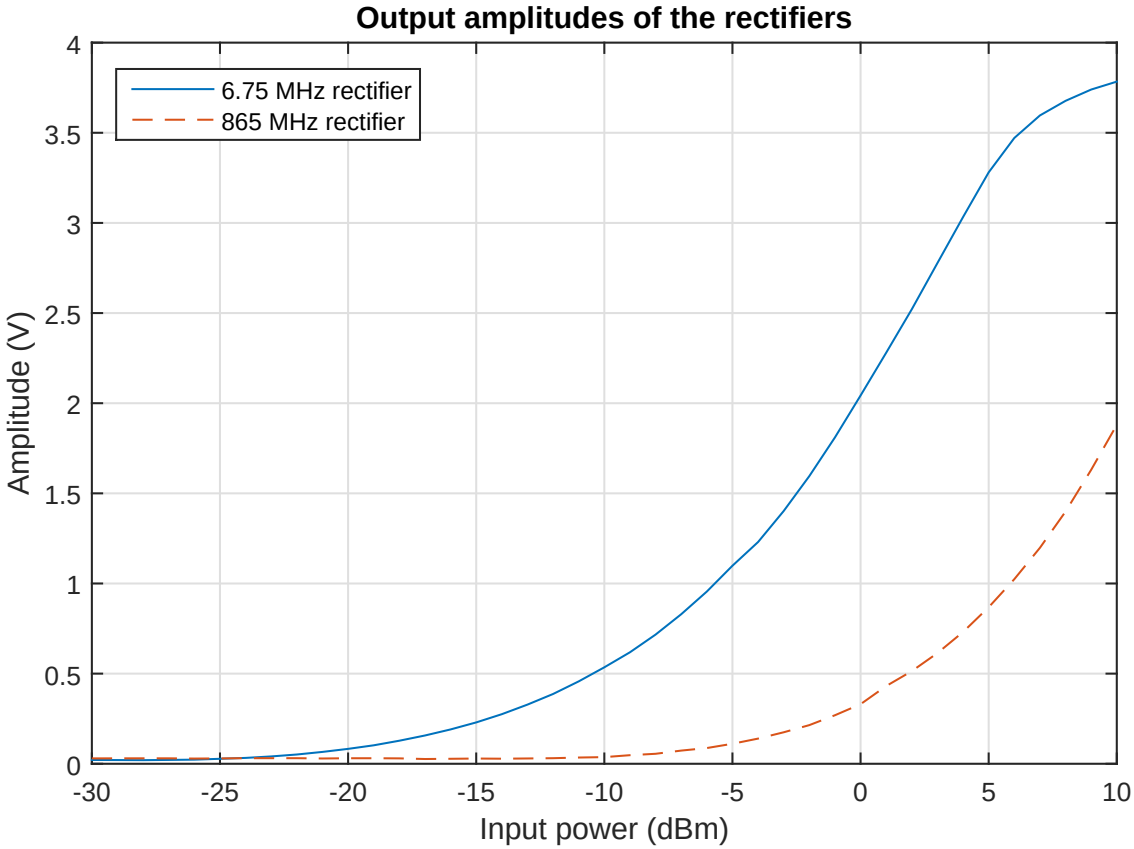


Figure 22: Measured output voltages of the RF-to-DC rectifiers, vertical accuracy±100mV and horizontal accuracy ±0.5 dBm

effectively inverting the rectifier output voltage and rendering the following regulators unusable, as they require a positive input voltage. As the potentially large amplitude of the voltage with negative polarity may harm the following circuitry, the rectifier output was disconnected and terminated with an equivalent 11 kΩ resistor as an imitation of the load.

Anritsu MG3710A vector signal generator was used to feed a signal of known power level to a matched rectifier input through a short 50 Ω coaxial cable, and the output of the rectifier was measured with Agilent infiniium 54855A 20 Gs/s oscilloscope and Agilent 1134A 7 GHz differential probe system. The measurement accuracy is determined by the level accuracy of the vector generator in the corresponding power range and the DC measurement accuracy of the oscilloscope, assuming the transmission losses are very small and the probe is well calibrated. The power efficiency of the rectifiers, as in the ratio of power available at the output in relation to the power fed to the input, was not measured, but measurement points are reserved for developers to measure and evaluate it in the future.

The 6.75 MHz rectifier output level measurement presented in Figure 22 shows that the rectifier operates with reasonable performance for a discrete component implementation. The output amplitude is negative due to the flipped diode orientation.

The initial input tuning of the 865 MHz rectifier was off by approximately 40

MHz due to simulation errors, so the matching circuit was revised with the help of harmonic balance simulation and straight forward impedance fitting in a Smith chart. The output level measurement is presented in Figure 22. The performance of the implemented 865 MHz rectifier is poor, possibly because the revised matching circuit may still not be properly optimized for the following nonlinear rectifier, or the malfunctioning 865 MHz clock extractor (see section 4.4.3) may be presenting a too low load impedance level.

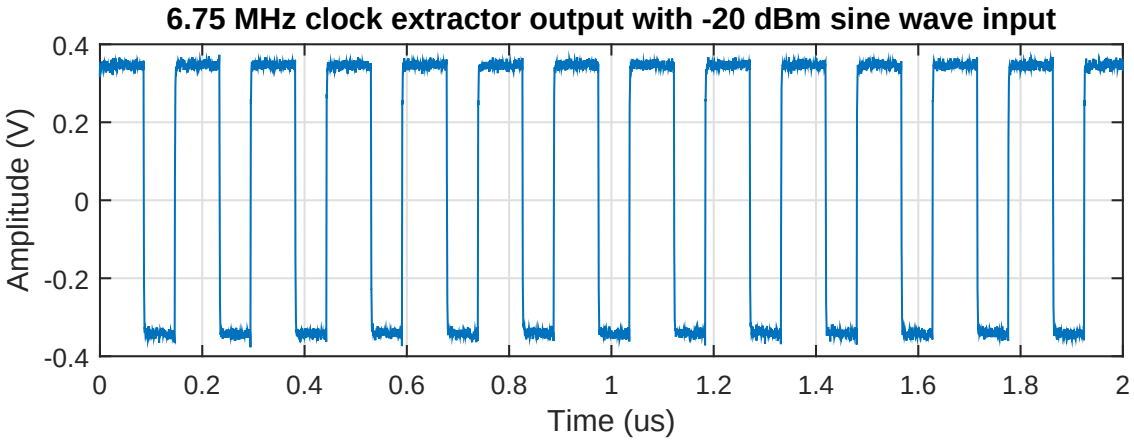
The power extractors designed in this system are only a proof of concept at best, the performance is very far from any state-of-the art. In order to be more beneficial as a independent development environment, the power extraction should have been accompanied by on-board measurement capability. Measuring the voltage and power output fluctuations would have allowed developers to test the effect of different communication schemes and duty cycling to the actual rectifier performance without using external measurement equipment. However, the system provides sufficient reservations for evaluating the power extractors using external measurement equipment, such as power and voltage meters.

4.4.2 Supply management and accuracy

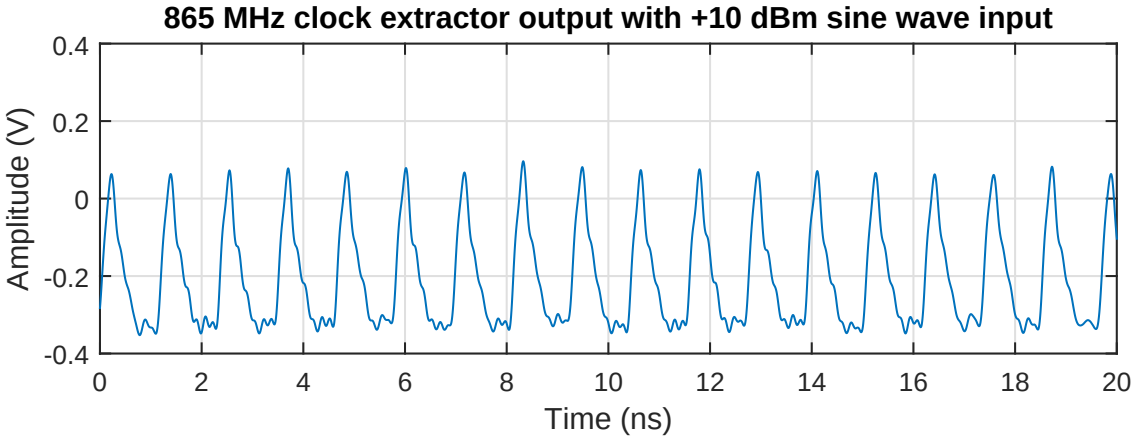
Table 4: Supply manager output capability

	Buck 1 +	**Buck 1 -**	**Buck 2**	**Buck 3**	**LDO**	**+3V3**
Max. voltage (V)	3.3	-3.3	3.6	1.335	3.0	3.3
Min. voltage (V)	3.3	-3.3	1.1	0.7	3.0	3.3
Accuracy (mV)	±50	±50	±50	±5	±90	±100
Max. current (mA)	1600	-60	1000	1000	250	2000

The output of the programmable supply regulator LM10504 was tested using Fluke 179 hand-held multimeter and LeCroy Wavesurfer 424 oscilloscope. Table 4 presents the digitally controllable range of the different supply outputs and the level accuracies provided by this module. Buck 1 output voltage can not be controlled, because the input voltage supplying for this regulator is too low for the regulator to operate properly. Unlike the other outputs of the LM10504, Buck 1 has a bypass MOSFET that connects input straight to output of the buck regulator when the input voltage is less than 3.5 V, but unfortunately the power supply path on the board is designed so that all of the different regulators are supplied from the common positive 3.3 V voltage. Same supply is used by all digital systems on the board, so increasing the input supply voltage amplitude might harm other systems on board. Output of the Buck 1 is not regulated on board, so the noise visible on the Buck 1 and inverted -Buck 1 supply lines is likely to be larger than the other supplies provided by the board. Systems that require the use of these supplies should house their own regulators.



(a)



(b)

Figure 23: Typical waveform from the outputs of the a) 6.75 MHz clock extractor and b) 865 MHz clock extractor.

Table 5: Clock extractor detection levels.

	6.75 MHz extractor	**865 MHz extractor**
Minimum detection level	-28dBm	+8dBm
Measurement accuracy	±0.5 dBm	

4.4.3 Clock extraction levels

Clock extraction operation was characterized by supplying a sine wave of known power level from Anritsu MG3710A vector signal generator through a short 50 Ω coaxial cable to the clock extractor input, thus the input power level corresponds to the input signal level coming from a matched antenna. The detection level in Table 5 is determined as the smallest input power needed for the extracted clock output to be generated. Measurement accuracy is determined by the level accuracy of the vector generator in the corresponding power range.

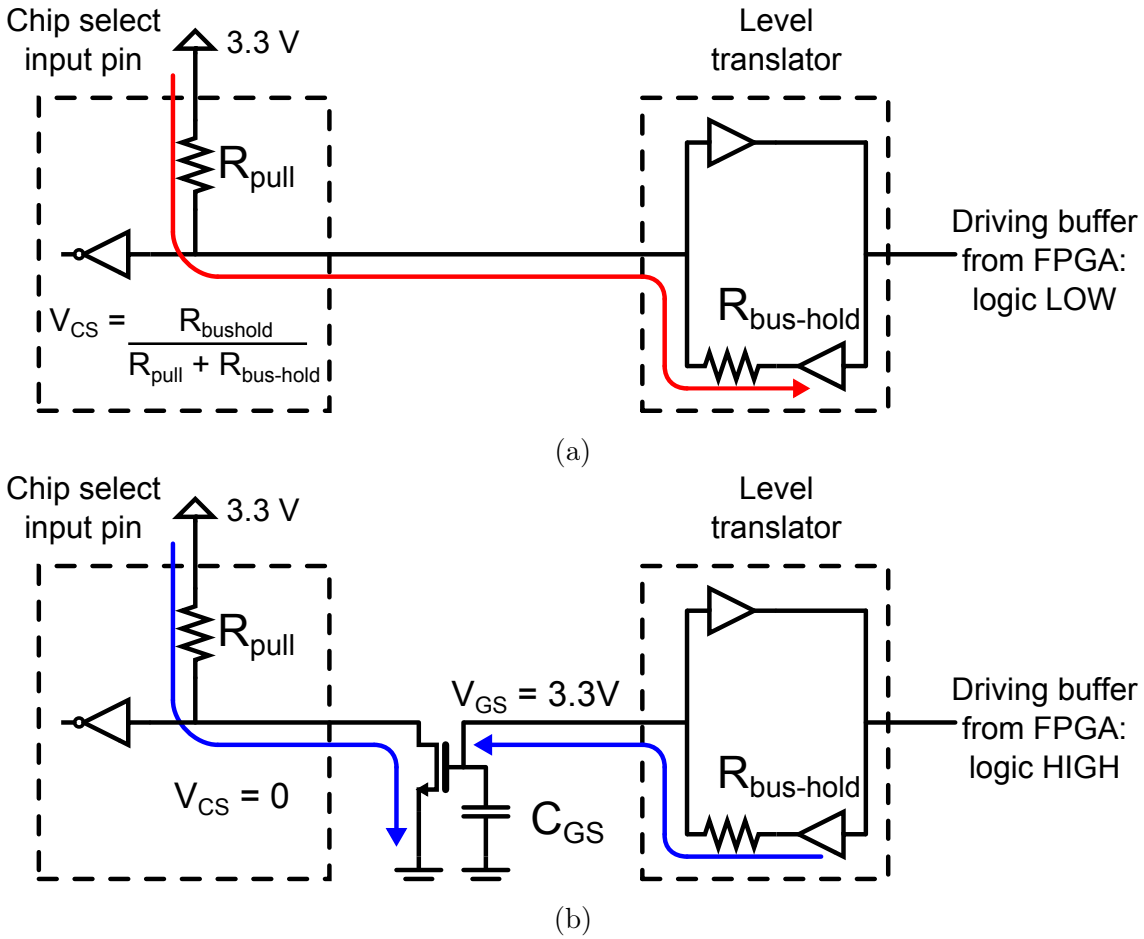


Figure 24: a) Using pull-up resistors with weak bus-hold circuits: the voltage divider formed by R_{pull} and $R_{bus\text{-}hold}$ causes problems if not $R_{pull} \gg R_{bus\text{-}hold}$. b) Revised circuit with added transistor to increase the driving capability.

The 6.75 MHz clock extractor works very well, as can be seen from the low minimum detection level in Table 5 and the waveform in Figure 23a. The ultra high frequency 865 MHz clock extraction using PL130-09 translation buffer does not operate as intended, the minimum detection level is unsuitable high and the resulting output waveform is severely distorted, as seen in Figure 23b. The buffer fails to generate LVDS level output [46] at such a high frequency, even though it was rated for operate up to 1 GHz. Manufacturer verified the performance gap of PL130-09 at high frequencies, and promised to revise the datasheets to reflect the actual performance. Currently the system does not provide any reasonable way to extract the clock from low power 865 MHz carrier, so the extractor should be totally redesigned.

4.4.4 Clock management and jitter

Initial connection tests with clock manager AD9508 failed, as the chip select line of the SPI bus was not pulled to low enough voltage to be recognized as logical

zero. Unlike the other control pins of AD9508, the chip select pin has an internal pull-up resistor R_{pull} [47]. The weak output driver of the voltage level translator FXLA104 that is driving the pin presents a too high of a effective series resistance $R_{bus\text{-}hold}$ to drive the pin under the low logic voltage threshold, as presented in Figure 24a. N-channel MOSFET with a negligibly small drain-source resistance was added between the voltage buffer and AD9508 to create a stronger output driver. Driving the gate of the transistor presents a load of considerably higher resistance for the FXLA104, allowing a correct operation of the voltage buffer, but as depicted in Figure 24b, the line logic operation is inverted and the large gate-source capacitance of the chosen transistor results in a large settling time.

Once the digital communication was fixed and the clock manager could be properly controlled, the outputs were configured to LVDS standard levels [46] and dividers set to suitable values for the output jitter measurements. Jitter metrics of the clock extraction structures were measured by feeding a sine wave from Anritsu MG3710A vector signal generator to the input of the extractor and measuring the cycle-to-cycle jitter spread with Agilent infiniium 54855A 20 Gs/s oscilloscope and Agilent 1134A 7 GHz differential probe system. Measurement accuracy is determined by the jitter measurement floor accuracy of the oscilloscope. 25 measurements of 10000 cycle-to-cycle jitter samples were acquired and averaged to get reliable jitter spread metrics of peak jitter and standard deviation [58]. The jitter from the signal source is not separated from the results, so the actual additive jitter of the measured clock management system itself is not properly analyzed here.

Table 6: Jitter of the different extracted clocks, measured at the output of the clock management module.

Jitter metric	**6.75MHz extracted clock**	**6.75 MHz oscillator clock**	**865MHz extracted clock**
Average peak value	328.7 ps	9.6 ps	16.6 ps
Average standard deviation	90.7 ps	3.1 ps	4.9 ps
Measurement accuracy	±70 fs RMS		

Jitter results are presented in Table 6. The 865 MHz clock was tested with unreasonably high input power level of +15 dBm in order to get a stabile edge for the jitter measurement, resulting in steeper edges in the input sine wave and low jitter, but the actual waveform as seen in Figure 23b is unlikely to be usable in digital logic.

All clock sources except the 865 MHz extractor provide a suitable LVDS level clock with a low amount of jitter, and as such should be suitable as a synchronization clocks for digital logic. Circuit simulation was not used as heavily in the design of the clock management structure as it was in all the other modules. A good simulation might have predicted the problems experienced in the 865 MHz clock extraction, assuming the component model provided by manufacturer was accurate.

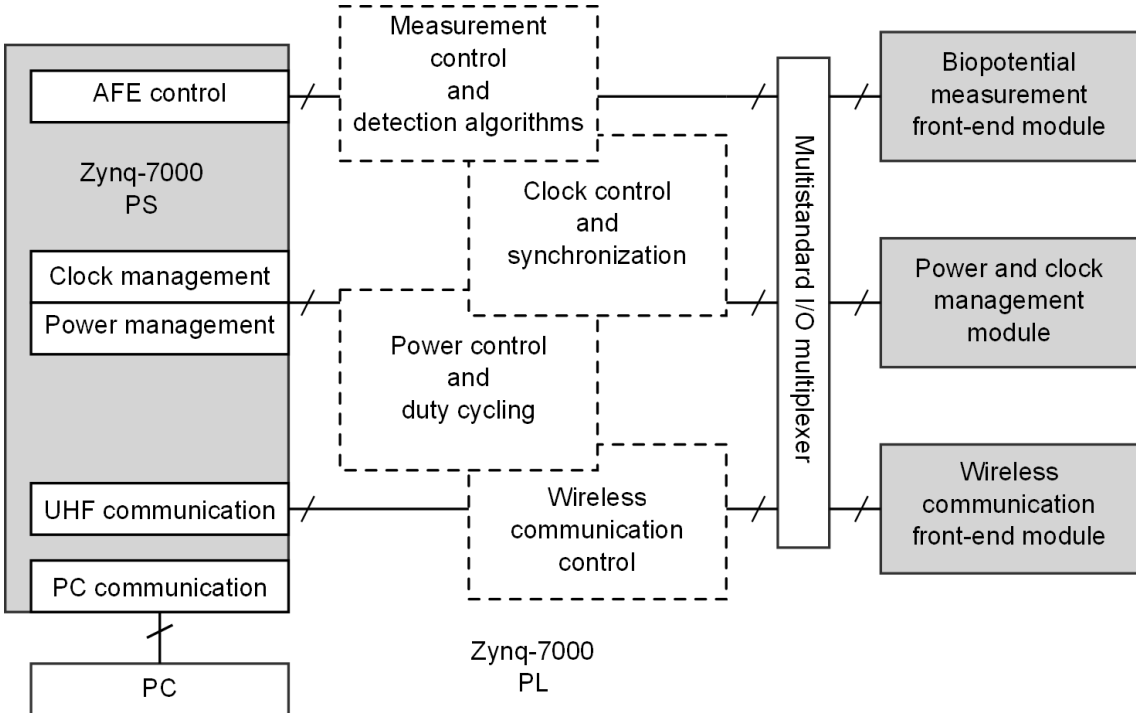


Figure 25: Structure of the implemented Vivado software. The dashed lines represent reservation for VHDL/Verilog implementations.

4.5 Control logic FPGA

Using a FPGA with an embedded hardware microcontroller turned out to be an efficient way of creating control structures for a development plaform. The Zynq-7000 SoC is used to control all of the modules representing the implant system. The system structure supports gradually implementing sections of the control logic in the FPGA PL section of the Zynq-7000, while the microprocessor PS section handles any unimplemented part. The used software supports VHDL and Verilog hardware description languages. As an example, simple logic inverters and multiplexers were written to the PL in both languages. Figure 25 shows a block diagram representation of the completed software structure, following the structure set in Figure 13. Easily modified structure supports different configurations with the modular system and enables the user to freely change extension boards between the two FMC connectors.

The processor system represented by the leftmost block in Figure 25 is programmed using C-language. New peripheral driver structures inheriting the default Xilinx peripheral driver structures were created to enable more control and modifiability to driver functionalities, such as custom interrupt capability from SPI master-in slave-out line. By default the application operates as a slave, waiting for executable commands coming from PC through UART. The relatively slow wired serial connection to PC is a bottleneck in testing the maximum performance of the system, and a viable pathway for noise to couple from the very noisy PC chassis and PC power source chopper. TCP/IP communication through ethernet connection would likely solve both the speed and noise issues.

4.6 External reader module

The external reader module is a separate system with an embedded microcontroller for controlling its functions, so unlike the other modules it does not necessarily need to be connected to the FPGA for operation. The main functionalities of the reader is the generation of radio frequency carrier signals, the power level control of the carriers and UHF communication using EPC C1G2. These functionalities are verified and characterized.

4.6.1 865 MHz RFID transceiver operation

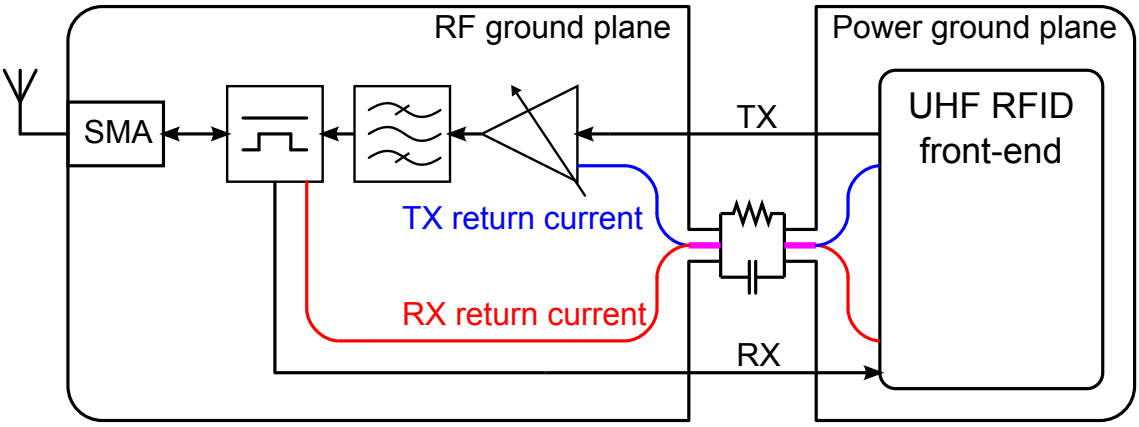


Figure 26: Ground layout problem points of the reader UHF transceiver front-end. The separation between receiving (RX) and the transmitting (TX) signals created with the directional coupler is diminished due to the paths of the return currents.

UHF communication of the reader module suffers from receiver sensitivity problems. Mistakes were made in the ground planning when setting the location of the star-point that separates the sensitive radio ground plane and the generally noisy supply ground plane. The reader component was left in the power ground plane, forcing the return currents of the transmitted and received signals through the same point, effectively diminishing the critical separation created with a directional coupler. The initial ground connection point was disconnected and bypassing capacitors added near both ground crossings in order to provide a safer path for the return currents, thus minimizing the disruptive coupling between the signals. The ground design error also causes some of the transmission lines to be referenced to a wrong ground plane, as the width and gap of the coplanar waveguide structure was not properly adjusted to the actual ground plane height.

The controllable output power range of the UHF was measured directly from the board output connector using spectrum analyser Rohde&Schwarz 20 kHz - 40 GHz FSER and short 50 Ω coaxial cable. The measurement error caused by the cable is assumed to be insignificant, so the overall measurement accuracy is defined by the level measuring accuracy of the spectrum analyzer, which is ± 1 dBm at frequencies lower than 1 GHz.

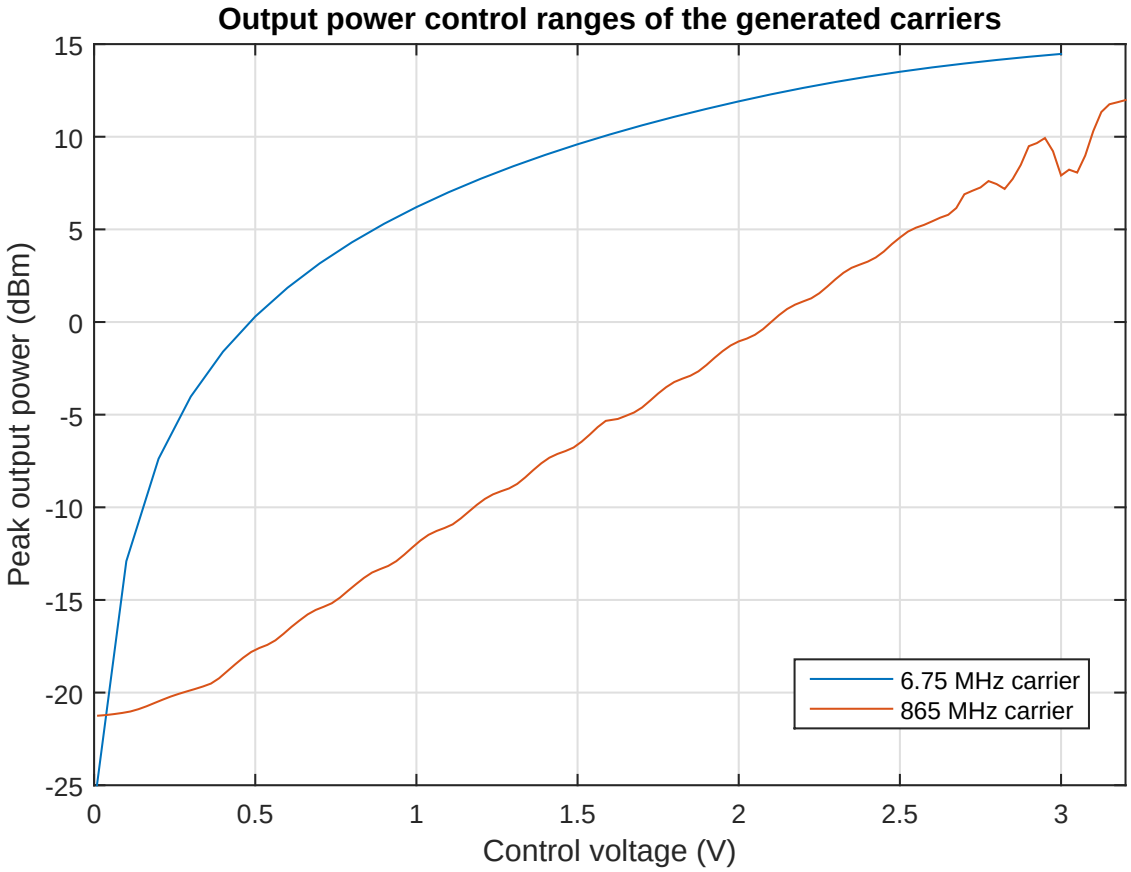


Figure 27: Output power ranges of the generated carriers, measurement accuracy ±1 dBm.

Usable amplification range of the transmitter structure with 865 MHz output frequency is measured to be -22 dB to +7dB, as presented in Figure 27. The output power level starts to behave erratically past power level of approximately +7 dBm, corresponding to voltage level of approximately 2.8.

The 865 MHz power amplifier output becomes unstable at levels above +7 dBm, as can be seen from the envelope of the signal in Figure 28 where the power amplifier is set to the maximum power of +14 dBm. The reason for this fluctuating behaviour is the insufficient transient current supply capability of the supply structure for power amplifier. The power amplifier is supplied from a low drop output regulator that is intended specifically for radio applications, but the supply has only a couple of small supply filtering capacitors. At high output power levels the momentary supply current required by the power output can be higher than what the regulator can provide, depleting the charge from the capacitors and forcing the power amplifier output level to vary. The frequency of the varying envelope is roughly 30 kHz and the amplitude variation is so high that the distortion can not be distinguished from the actual desired modulated signals. This results in corrupted data in both the transmitting and especially the receiving operations, so the usable maximum power level is limited to +7 dBm.

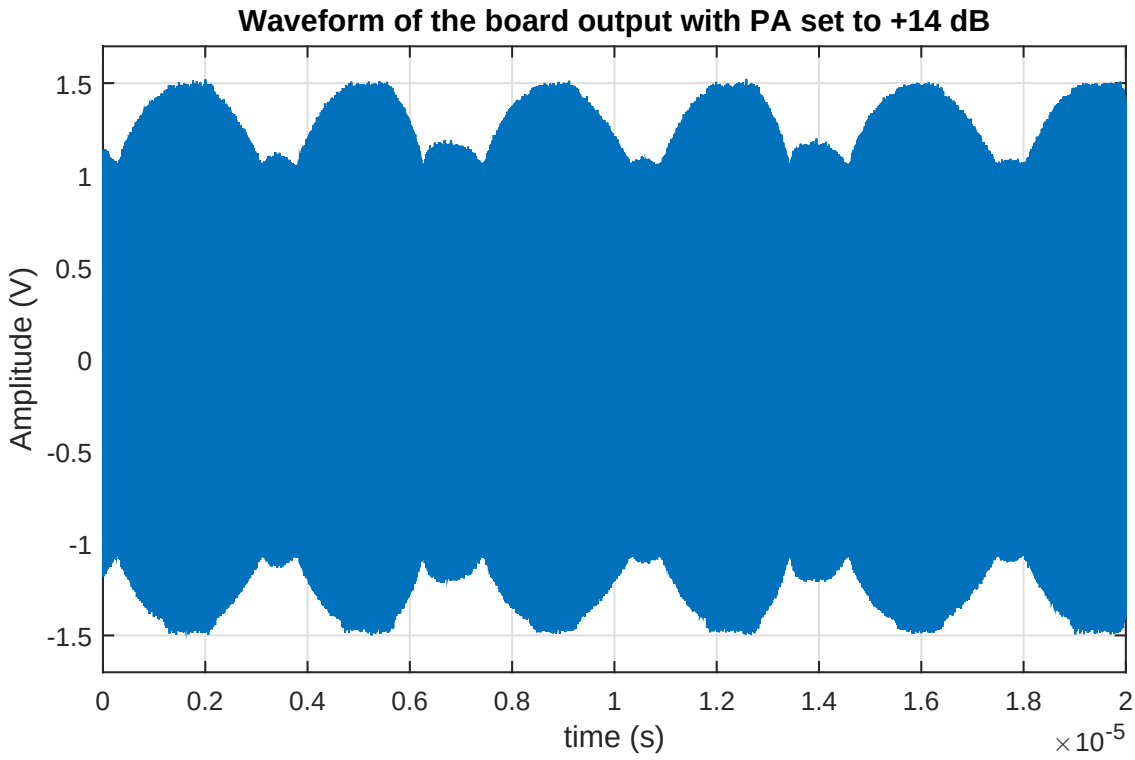


Figure 28: 865 MHz output waveform at the maximum output power setting.

Table 7 presents the capability of the wireless communication of the system. The reader radio is much more versatile and suitable to development purposes than the implant radio that has very limited functionalities and low speed in SPI communication. Despite the sensitivity problems on the receiver of the reader, the overall performance of the inductive radio link is satisfying.

The measurements have displayed again how important thoughtful ground planning, return current consideration and power supply dimensioning are for a radio front-end. The applied fixes to the encountered problems have been effective and the front-end successfully communicates using the EPC C1G2 protocol. If the sensitivity problems resurface, an alternative for re-manufacturing the whole reader module is to use one of the provided extension connectors from Figure 11 to attach a new dedicated radio front-end extension board, either a custom design or an off-the-self evaluation module.

4.6.2 6.75 MHz carrier generation

LF generation capability was measured using LeCroy waveSurfer 424 200 MHz oscilloscope to capture the waveform in time domain, and Rohde&Schwarz 20 kHz - 40 GHz FSER spectrum analyzer to capture the frequency domain signal content and power. Output voltage waveform of the custom designed class-E power amplifier confirms that the structure can generate a suitable sine-wave output with controllable output power.

Table 7: Key specifications and capability comparison of the implemented UHF communication front-ends.

Capability	**Reader radio**	**Implant radio**
EPC C1G2	Yes	Yes
Custom protocol support	Yes (direct mode)	No
Custom commands	Yes	Limited (ams determined only)
Maximum RF datarate	640 kb/s	640 kb/s
Maximum SPI clock frequency	2 MHz	10 MHz (3 V supply)
Maximum SPI datarate	1 Mb/s (8 bits per frame)	405 kb/s (64 bits per frame)
FIFO buffer depth	24 bytes	8 bytes

Initially the generated 6.75 MHz wave would not stay on continuously due to the limited driving capability of the chosen gate driver and the relatively high input capacitance of the chosen N-channel MOSFET transistor. The gate driver has an internal low-dropout regulator that supplies its output driver stage. The high dynamic current requirement of the capacitive load presented by the gate capacitance of the switching transistor drains the charge from the decoupling capacitors at a higher rate than regulator can recharge them, similarly to the problems encountered with the 865 MHz power amplifier. This effect can be seen in Figure 29: high strain on the driver causes its internal power supply voltage to drop gradually, until the internal low voltage lockout circuit triggers and disables the output switching. After approximately 7 microseconds the internal regulator has charged the output supply decoupling capacitor to a level above 3.9 Volts and the low voltage lockout circuit restarts the output switching. The gate driver has been specified to operate at least up to 1 MHz switching frequency when driving a 1 nF capacitive load, whereas the driver was now being used to drive a gate-source capacitance of 3.2 nF with switching frequency of 6.75 MHz. This problem was solved by changing the power amplifier transistor to a model IRLML6246, that reportedly has significantly lower gate-source capacitance of 650 pF.

After changing the switching transistor the output waveform stays on continuously. Optionally the problem might have been fixed by increasing the power and voltage level of the main supply, as the gate driver is currently being used only very near its minimum supply level. The spectrum of the generated continuous wave is displayed in Figure 30. The small side-lobes 21 kHz from the carrier are possibly generated by non-ideal switching characteristics or oversights in the measurement setup, but the causes should be analysed more if a spectrally pure sine signal is required.

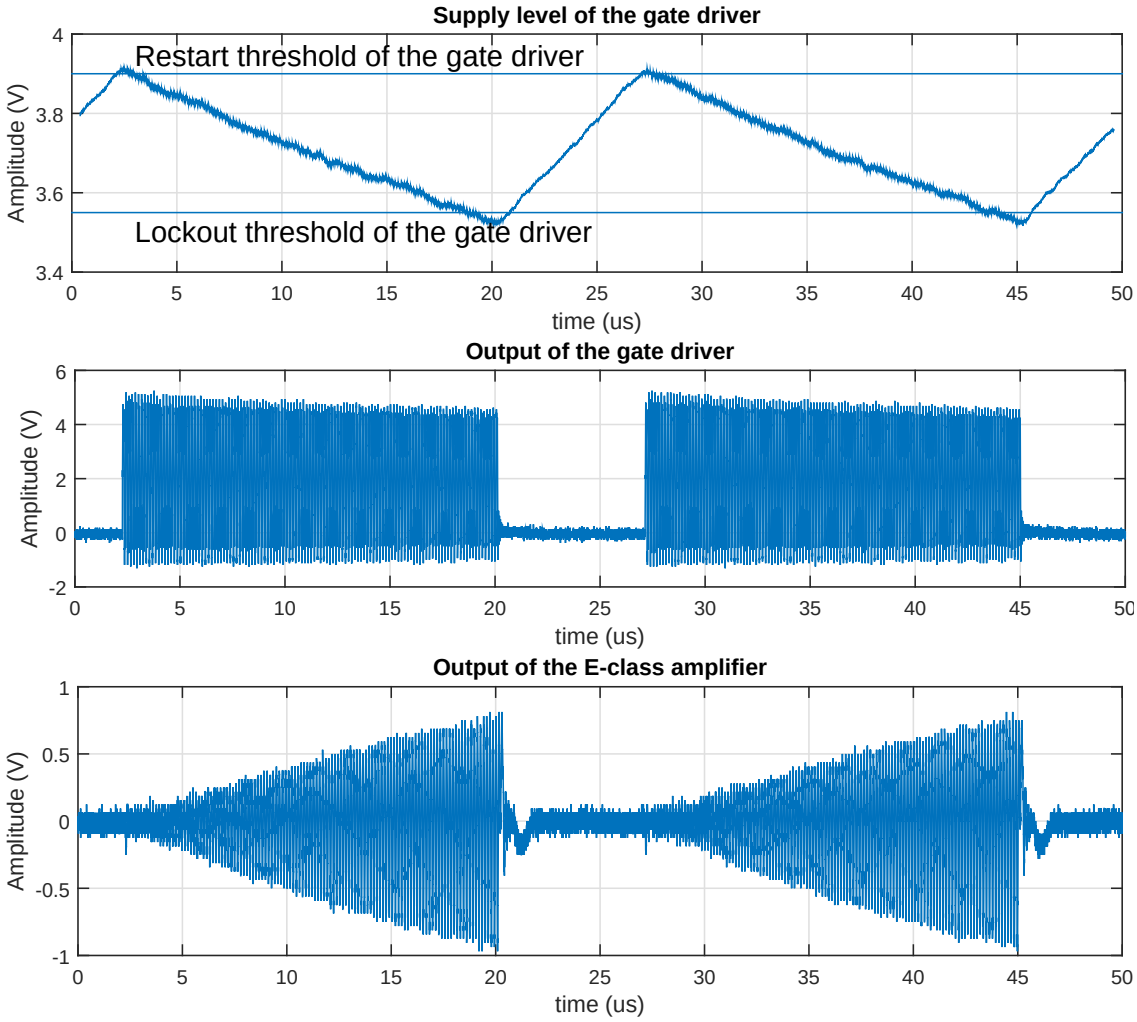


Figure 29: 6.75 MHz transmitter output waveforms before changing the transistor.

Figure 27 presents the controllable output power range of the 6.75 MHz E-class amplifier as function of the voltage used to control the variable output regulator of Figure 12. The curve of the output power level follows a logarithmic path as it should with a linear control voltage. Digital-to-analog converters of the microcontroller could be used to digitally control the output power in this range.

The precautions made in isolating the structure have worked well, as it does not seem to interfere with any of the other functionalities of the module. On the other hand, the precaution of oversizing the switching transistor was a mistake. Another shortcoming was that the structure can not be turned on and off digitally, a single control line to the enabling pin of the gate driver would have sufficed. In summary the implemented 6.75 MHz carrier generation functionality operates as intended after the aforementioned changes were made.

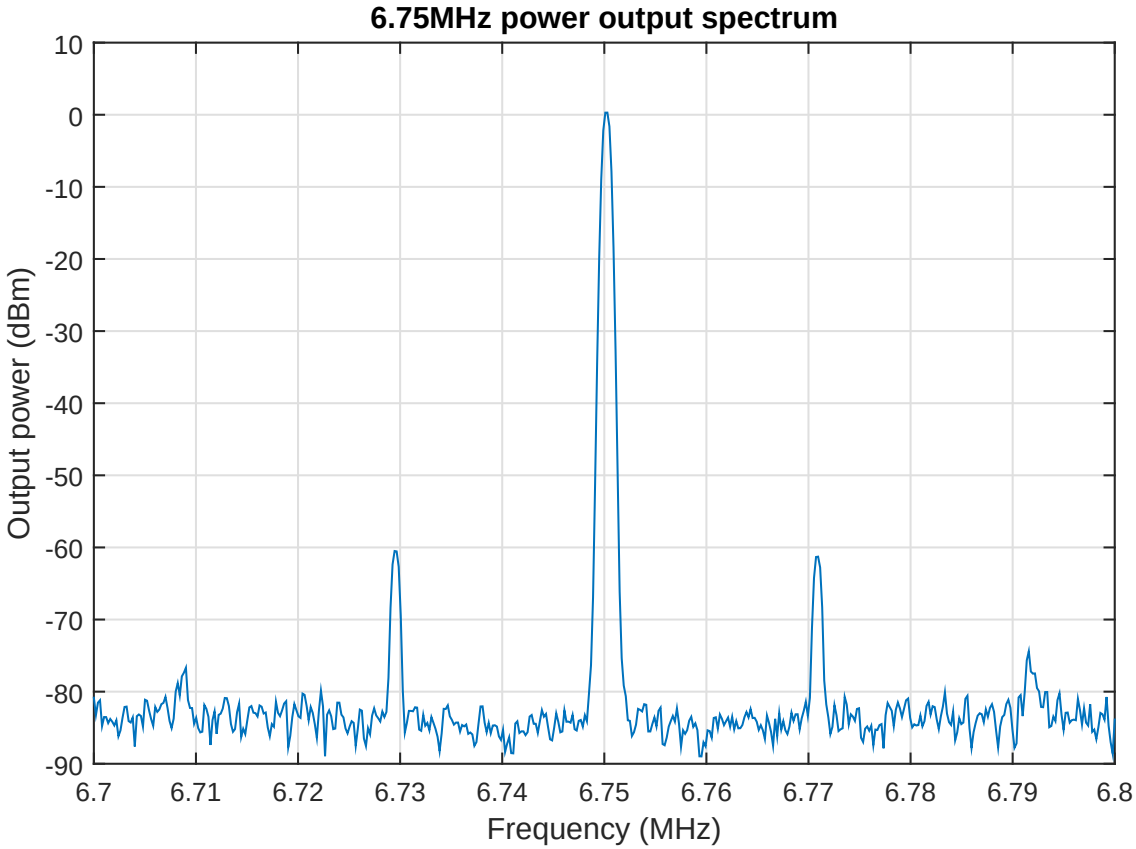


Figure 30: 6.75 MHz output power spectrum, measurement accuracy ±0.5 dBm.

4.7 Overall system performance

The platform presented in this work has been used successfully in the demonstration of the various functionalities of a wireless sensor implant. The only exception is the 865 MHz power and clock harvesting, that should be redesigned to reach a comparable performance to an inductively powered device. Figure 31a presents a single channel measurement result of measuring EEG with the system, Figure 31b presents one channel of EMG. Same timescale is used in both figures to display the difference in frequency content in the two biopotentials. The measurements were conducted in noisy office environment without any shielding, so digital filtering was used to attenuate the 50 Hz line noise. The ripple visible in the graph is mostly 50 Hz line noise captured by the long wires of the electrodes, and the resulting harmonic signals generated by the non-linearities of the measurement front-end.

The EEG in Figure 31b shows the effect of blinking eyes as spike artefacts typical to EEG [59]. The EMG in Figure 31b was acquired from the left arm using the same electrodes as with EEG, the effect of flexing muscles is visible as high frequency bursts. Although flexing the muscles has generated notable activity in the waveform, it should also be noted that the passband filtering was set to the default 0.7-100 Hz (see section 3.2.2), whereas the signal band of EMG is usually up to 500 Hz (see Table 1), so a large part of the desired signal content has likely been filtered out.

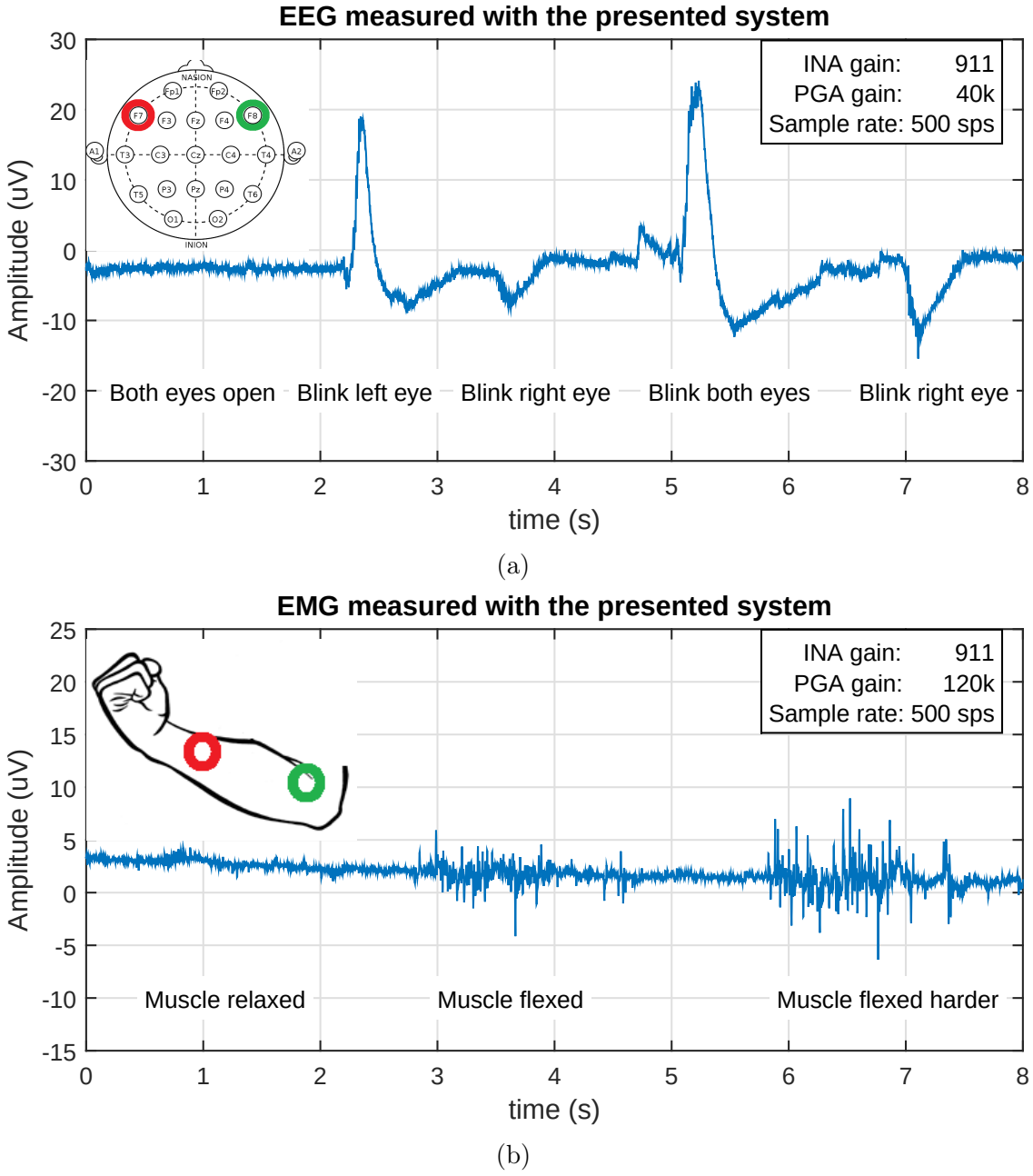


Figure 31: Biopotential signals captured with the system using on-skin electrodes, a) electroencephalogram (EEG) and b) electromyogram (EMG). Reference electrode location marked with green, measurement electrode location with red.

Table 8 displays a comparison of the implemented system to a collection of previous medical sensor development systems that utilize comparable structures and are constructed with discrete components. The main improvements in this work are the achieved high level of modularity, and the FPGA-based control module that allows the development of digital logic using hardware description languages. This work also has higher maximum achievable gain, 15.7 times the maximum

Table 8: Comparison to other published works on wireless medical sensor development platforms

	EEGWISP [8]	**WIMAGINE** [9]	**KDI** [31]	**This work**
Radio front-end				
Dual frequency	No	No	Yes	Yes
Data freq. (MHz)	902 - 928	13.56	400 or 2450	840 - 960
Power freq. (MHz)	902 - 928	13.56	13.56	6.78 or 865
Datarate (kbit/s)	0.65	400-450	800 or 2000	160 - 640
Measurement front-end				
Channels	1	64	32	32
Gain (V/V)	1 - 10000	1 - 1370	1 - 1370	1 - 157000
Bandwidth (Hz)	0.16 - 30	0.25 - 3000 programmable	0.25 - 3000 programmable	0.7 - 100 tunable
ADC resolution	10 bits	12 bits	12 bits	12 bits
ADC ENOB	-	10.7 bits	10.7 bits	9 bits
Biopotential capability	EEG	EEG, ECoG	EEG, ECoG	EEG, ECoG, EMG, ECG
Other				
Modularity	low	low	medium	high
Form factor	small,	small,	small,	very large

gain of EEGWISP [8], allowing the use of a range of electrode types with different sensitivities. The passband of the tunable filter can be set to virtually any value achievable with the eight order structure, but adjusting the passband by manually changing passive components is inconvenient compared to the programmable filters used in the WIMAGINE [9] and KDI [31]. The dual frequency operation has been previously demonstrated in the KDI platform, with higher datarates, but in this platform the user can choose to utilize either single or dual frequency operation. In summary, the added value of this work has been to add levels of freedom for the designers. Due to the size and power constraints presented by the high performance FPGA module used in this work, the system is not wearable, but in turn provides a capable platform for emulating and developing complex structures for the integrated circuit implementation of a medical sensor implant.

5 Conclusion

Proposed uses of medical implants include the long term monitoring of the electroencephalogram (EEG) of epilepsy patients. Compared to traditional on-skin electrodes and measurements, implanting the electrodes along with an implantable wireless measurement front-end under skin can greatly improve the convenience of extended monitoring for patients, raise the quality of the acquired data for researchers, and the create new application possibilities, such as novel human-machine interfaces, especially in brain-machine interfaces.

This thesis presents an implementation of a modular development platform for wireless medical sensor implant devices. The first objective was to study the existing medical implants in depth to extract the main requirements and related design challenges that the development platform needs to reflect as a demonstrator of the various functionalities. Second objective was to design and fabricate the development platform from discrete components in such a way that the resulting environment is accurate, effective and practical in terms of both implant development and future development of the system itself. Finally, the performance of the developed system was characterized by measurements to evaluate the capability and suitability for implant development.

An EEG-measuring implant consists of a biopotential measurement front-end, digital processing unit for data handling and control, power- and timing management unit and communication unit, and an external reader unit handles the required power and data transfer. The design presented here has been divided to interconnectable modules, enabling the performance of the whole system to be scaled and modified according to the needs of the developers of medical implants. The modules are implemented as FMC daughter boards around Xilinx ZC706 Zynq-7000, a high performance FPGA evaluation board. Highly complex controls and algorithms can be implemented using programmable logic or the two on-chip ARM9-microprocessors, thus the development of digital logic for an integrated circuit can be done gradually, as any unimplemented section can be fully controlled by the processor. This approach was found to be successful, as the resulting modular system is easy to test, develop and use.

An implanted wireless sensor device acquires data, such as neural signal data, through an analog measurement interface and transforms it to digital format. The presented measurement front-end module provides an interface for acquiring biopotentials with ENOB of 9 bits. The resulting structure was found to be very modifiable for the needs of many biopotentials in terms of gain range, sampling rate and channel count, but the overall accuracy is limited by non-linearity of the structure. Additionally, making changes to the filter passband in the current structure requires a large amount of component changes, so using programmable filters would have improved the system.

Implemented wireless communication front-end module is capable of datarates up to 640 kb/s using an existing RFID protocol EPC C1G2, and it demonstrates the implant side inductive link communication operation on 865 MHz carrier. The matching circuit was revised after the actual chip input impedance differed from the

claimed impedance. The implemented power and clock extraction module supports dual carrier operation and is tuned to perform at 6.75 MHz and 865 MHz. The 6.75 MHz extractions operate as intended, but the 865 MHz has severe problems due to unpredicted component malfunctions. All of these component-related problems could have been avoided by evaluating the performance of all critical components by tests and measurements before incorporating them in the system.

The dual radio frequency carriers are generated by external reader device module, that houses a Freescale KL25Z microcontroller, a versatile 865 MHz RFID transceiver and a custom designed 6.75 MHz transmitter. Both radio outputs have programmable output power in the range of approximately -20 dBm to +7 dBm, but the sensitivity problems of the higher frequency transceiver displayed how important thoughtful ground planning, return current consideration and power supply dimensioning are for a radio front-end.

The presented system provides programming and modification possibilities for testing different options and trade-offs related to the design of a wireless implant. The system has been used successfully used in the demonstration of the various functionalities of a wireless sensor implant, only exception is the 865 MHz power and clock harvesting, that should be redesigned to reach a comparable performance to an inductively powered device.

The resulting system can narrow the gap from simulation to finished device by providing a possibility to test uncertain aspects using real neural signal measurement data and real inductive radio link. However, the platform has limited integrated monitoring capacity, and would have benefited from extended capabilities such as monitoring the efficiency of wireless power transfer. The system is ready to be used for developing and testing aspects for novel implanted devices, such as different radio communication schemes, radio antenna options, or algorithms in digital logic, thus achieving the objectives set for this work.

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