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Title: High-yield of memory elements from carbon nanotube field-effect transistors with atomic layer deposited gate dielectric

Year: 2008

Version: Final published version

Please cite the original version:

Rinkiö, Marcus & Johansson, Andreas & Zavodchikova, Marina Y. & Toppari, J. Jussi & Nasibulin, Albert G. & Kauppinen, Esko I. & Törmä, Päivi. 2008. High-yield of memory elements from carbon nanotube field-effect transistors with atomic layer deposited gate dielectric. *New Journal of Physics*. Volume 10, Issue 10. 103019/1-16. ISSN 1367-2630 (printed). DOI: 10.1088/1367-2630/10/10/103019

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High-yield of memory elements from carbon nanotube field-effect transistors with atomic layer deposited gate dielectric

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High-yield of memory elements from carbon nanotube field-effect transistors with atomic layer deposited gate dielectric

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New Journal of Physics **10** (2008) 103019 (16pp)

Received 23 June 2008

Published 16 October 2008

Online at <http://www.njp.org/>

doi:10.1088/1367-2630/10/10/103019

Abstract. Carbon nanotube field-effect transistors (CNT FETs) have been proposed as possible building blocks for future nano-electronics. But a challenge with CNT FETs is that they appear to randomly display varying amounts of hysteresis in their transfer characteristics. The hysteresis is often attributed to charge trapping in the dielectric layer between the nanotube and the gate. We find that the memory effect can be controlled by carefully designing the gate dielectric in nm-thin layers. By using atomic layer depositions (ALD) of HfO₂ and TiO₂ in a triple-layer configuration, we achieve to our knowledge the first CNT FETs with consistent and narrowly distributed memory effects in their transfer characteristics. The study includes 94 CNT FET samples, providing a good basis for statistics on the hysteresis seen in five different CNT-gate configurations.

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1. Introduction

The quasi-one-dimensional, nearly perfect, crystalline structures of carbon nanotubes (CNTs) make them promising candidates [1]–[4] to extend the down-scaling of electronic components beyond the limitations of present Si-based technology. Featuring either semiconducting or metallic transport properties, they can in principle replace both active components as well as their interconnects. It was suggested that CNT-based devices could be mounted with an integration level of up to 10^{12} cm^{-2} [5], which is about four orders of magnitude higher density than in current technology. Field-effect transistors (FETs) have been made out of CNTs with impressive device parameters, e.g. subthreshold slopes close to $60 \text{ mV decade}^{-1}$ [6], and field-effect mobilities of up to $79\,000 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ [7]. But there are many challenges with incorporating CNTs into logic devices, such as being able to separate the semiconducting CNTs from the metallic ones, or to control their placement with nanometre accuracy. Another challenge with CNT FETs is that often they display some degree of hysteresis in their transfer characteristics. For a CNT FET this is an unwanted feature, rendering it unpredictable in its output, and it has motivated several studies to find ways to prevent or remove these tendencies [6], [8]–[11]. On the other hand, the presence of hysteresis opens up the possibility to utilize the device as a memory element instead. This has been pointed out by several studies [12]–[17], demonstrating CNT FETs with ON and OFF states which are well separated and addressable with positive or negative gate voltage pulses. However, the challenge is to be able to control the presence of hysteresis, which so far has been reported as a widely varying property among the studied CNT FETs [14, 16, 18]. In this paper, we use Hf-based atomic layer deposition (ALD)-grown gate dielectric to control hysteresis and achieve a 100% yield in memory effect, as well as study the origin of the hysteresis in our devices. This is to our knowledge the first report on CNT FETs featuring memory effects that are *consistent* from sample to sample.

Several different models, which all can explain hysteresis in the transfer characteristics of a CNT FET, have been suggested. First it was pointed out that, especially for CNT FETs with a gate insulator of SiO_2 , it may have the same origin as the hysteresis sometimes seen in

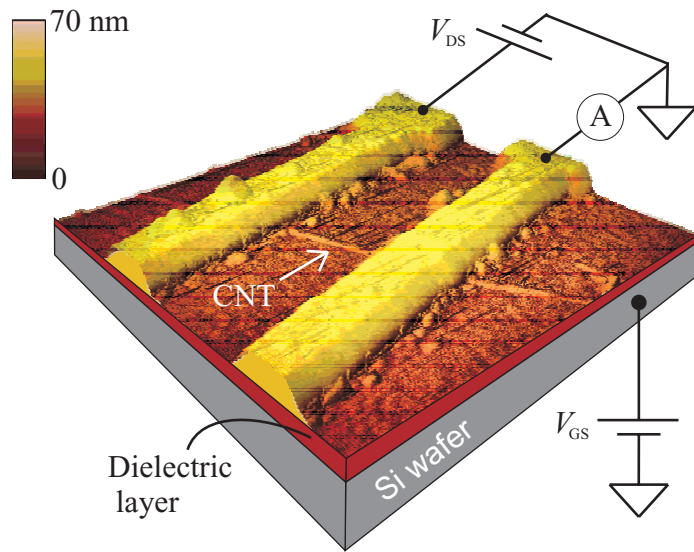


Figure 1. AFM image of a typical device, covering an area of $1\ \mu\text{m}^2$. The SWCNT is resting on a dielectric layer, and has source and drain electrodes of Pd deposited on top with a spacing of 260 nm. The measurement setup is schematically drawn with voltage applied to the Si wafer, acting as a backgate, and voltage applied between the drain and source electrodes while measuring the current response through the CNT.

conventional Si-MOSFETs [12, 13, 16]. There it is known that mobile ions or charges within the SiO_2 layer can relocate in response to the applied gate voltage, and as a result modify the local electric field sensed by the charge carriers in the conduction channel. But this is not the only proposed mechanism. It has also been suggested [12, 19, 20] that the charge traps may not be mobile, but located stationary in the near vicinity of the CNT. An applied gate voltage could then assist in filling or emptying the charge traps with charge carriers moving in the CNT, which in turn screens the applied electric field and causes hysteresis to appear in the gate voltage response. Yet another possibility is that surface chemistry plays an important role. For example water molecules adhered to the surface have been shown [8, 10] to give a large contribution to the hysteresis of some CNT FETs. A fourth model suggests that defects in the nanotube itself could provide charging centers, which can be filled or emptied in response to the gate modulation. A charging center in this case may be a carbon atom substituted with a different atom or molecule, which can donate or accept electrons from the conduction channel. All four models may contribute in varying degree to hysteresis in the transfer characteristics of a CNT FET. One way of controlling the memory response would be to tailor one mechanism to dominate the electrostatic charging around the CNT conduction channel.

2. Experiment

2.1. Sample preparation

This study includes in total 94 single-walled carbon nanotube (SWCNT) FETs with varying gate insulator, which by far exceeds the number of samples included in earlier studies of hysteresis in CNT FETs [8, 10, 12, 13, 15, 16, 19, 20]. An atomic force microscope (AFM) image of a

typical sample is shown in figure 1. The samples were built in a bottom-up approach, described in detail in [21], starting from a highly boron-doped Si wafer which acts as a backgate. While there are many possible device parameters to vary, we chose here to study the influence of two of them; the first is the composition of the dielectric material and the second is variation of the thickness of the same. The backgate was covered with an ALD layer of either Al_2O_3 (nominal thickness: 20 nm), HfO_2 (20 nm), or $\text{HfO}_2\text{--TiO}_2\text{--HfO}_2$ (40–0.5–3 or 40–0.5–1 nm). All ALD depositions were done at Beneq Oy. (Espoo, Finland), using a Beneq P400A ALD deposition tool. The idea motivating the triple-layer structure is to create, in a controlled way, charge traps in the close vicinity of the CNT FET [15]. The interface between two different ALD layers may serve that purpose, and thereby dominate the local electrostatic charging effects. We also prepared reference samples with gate insulator of the more commonly used thermally grown SiO_2 (300 nm). On top of the gate insulator a matrix of alignment markers was deposited, using e-beam lithography and metallization of Pd with an adhesion layer of Ti. CNTs were then deposited in two different ways, depending on their origin. Our primary source was commercial SWCNTs produced by NanoCyl S.A. (Sambreville, Belgium), bought in the form of black powder, which was suspended in dichloroethane by ultra-sonication for about 30 min. Typically 5–15 droplets of the nanotube suspension were then deposited onto the sample while it was spun at 1500 rpm. We also prepared, as a reference, 11 samples with SWCNTs from a hot wire generator reactor on to substrates with the $\text{HfO}_2\text{--TiO}_2\text{--HfO}_2$ (40–0.5–1 nm) triple-layer. The hot wire generator reactor is based on aerosol (floating catalyst) synthesis of CNTs. Iron particles and carbon monoxide were utilized as the catalyst and the carbon source, respectively [22]. Individual CNTs were filtered out from the bundled tubes in the gas phase as described in [23] and deposited onto the sample surface at room temperature using a thermophoretic precipitator [24]. In both methods CNTs were left at random places on the surface. Their locations were then mapped in relation to the matrix of alignment markers, using an AFM. The AFM images allowed us to select what appeared to be non-bundled and clean CNTs for the remaining fabrication steps, but some of the devices may also consist of a small bundle of semiconducting CNTs. Finally, electrodes of Pd were deposited onto the ends of the CNTs, with the help of e-beam lithography and subsequent metallization. The CNT diameters and FET channel lengths were then determined from AFM images of the devices, and can be found in appendix A.

2.2. Measurements

All measurements in this study were carried out at room temperature in an electrically shielded room, either under ambient conditions or in a chamber under dry nitrogen gas flow, which reduced the relative humidity to below 1% (below the resolution of our humidity sensor). Two-terminal measurements were performed, with the substrate acting as a backgate. Dc measurements were used with the applied voltage given by a home-built voltage distribution box, powered by batteries and computer controlled via a data acquisition card, while measuring the current response through the nanotube. I – V characteristics and conductance response to an applied backgate voltage were collected from all samples. A schematic of the measurement setup is drawn in figure 1. The samples with linear I – V characteristics and conductance not sensitive to an applied backgate voltage were considered to have metallic CNTs. The study includes in total 94 semiconducting SWCNTs, featuring a clear backgate dependence. These comprise about 82% of all the samples made, which is somewhat higher than the expected

67% for randomly picked CNT chiralities. Surprisingly, eight of the eleven devices made with SWCNTs from the hot wire generator reactor show clear metallic behavior. Of the three remaining semiconducting SWCNTs, one had a malfunctioning backgate, leaving only two CNT FETs of this kind added to the study. As will be seen in figure 3, these two CNT FETs do not deviate notably in performance compared to the other 25 devices with the same gate dielectric.

2.3. Contact resistance

An often problematic part of CNT sample processing is to achieve low contact resistance between electrode and nanotube [25]. As an upper limit measure of the contact resistances in our devices, we sampled the total two-terminal resistances of the metallic CNTs. These were found to be in the range of 14–160 k Ω , which is close to the theoretical minimum resistance for SWCNTs of $1/2G_0 = h/4e^2 \approx 6.45$ k Ω . Here G_0 is the quantum unit of conductance, e is the charge of the electron and h is Planck's constant.

3. Results

The focus of this study is on the appearance of hysteresis in the transfer characteristics of our CNT FETs in relation to the gate dielectric used. Seven of the 94 samples had the backgate covered with ALD of Al₂O₃ (nominal thickness: 20 nm), 14 with ALD of HfO₂ (20 nm), 11 with ALD of HfO₂–TiO₂–HfO₂ (40–0.5–3 nm), 27 with ALD of HfO₂–TiO₂–HfO₂ (40–0.5–1 nm), and the remaining 25 with thermally grown SiO₂ (300 nm). A typical example of a CNT FET exhibiting hysteresis is shown in figure 2(a), for a SWCNT resting on a backgate dielectric of 20 nm thick HfO₂ with 10 mV applied between the drain and source electrodes. Most SWCNT FETs displayed typical unipolar p-type behavior [26, 27], with strongly suppressed conductance at positive gate voltages and a transition into a highly conducting state at negative gate voltages. A few devices showed ambipolar dependence with a somewhat increased conductance at high positive backgate voltages, which has been attributed to semiconducting nanotubes with a small bandgap [28, 29]. From these data, estimates of field-effect mobility and subthreshold slope have been made, which are presented in appendix C. Upon scanning the backgate voltage back and forth, the threshold voltage attains in some, but not all, of the CNT FETs a higher value for the reverse sweep than for the forward sweep, resulting in a highly reproducible hysteresis loop with different conductance values at zero backgate voltage depending on the sweep direction. In figure 2(b), it is demonstrated how the current response of such a CNT FET can be switched between the two states by sending either a positive or negative voltage pulse to the backgate.

The working memory devices included in this study have so far been subjected to slow switching frequencies of up to 10 Hz. Some of the devices show charge stability with no change in ON or OFF state for several days, while others have a retention time of down to a few hours. Durability has been tested for a few of the CNT memories, with no significant change in ON/OFF states after switching 10⁴ times or more. We are currently studying these aspects, but would like to add they should not be compared to single device characteristics of state-of-the-art commercial memories before the gate configuration is changed from a backgate to a local gate for each CNT. That work is also in progress.

All mass-fabricated electronic devices have a natural variation of characteristic parameters, which is acceptable as long as the parameter distribution is narrow enough not to interfere

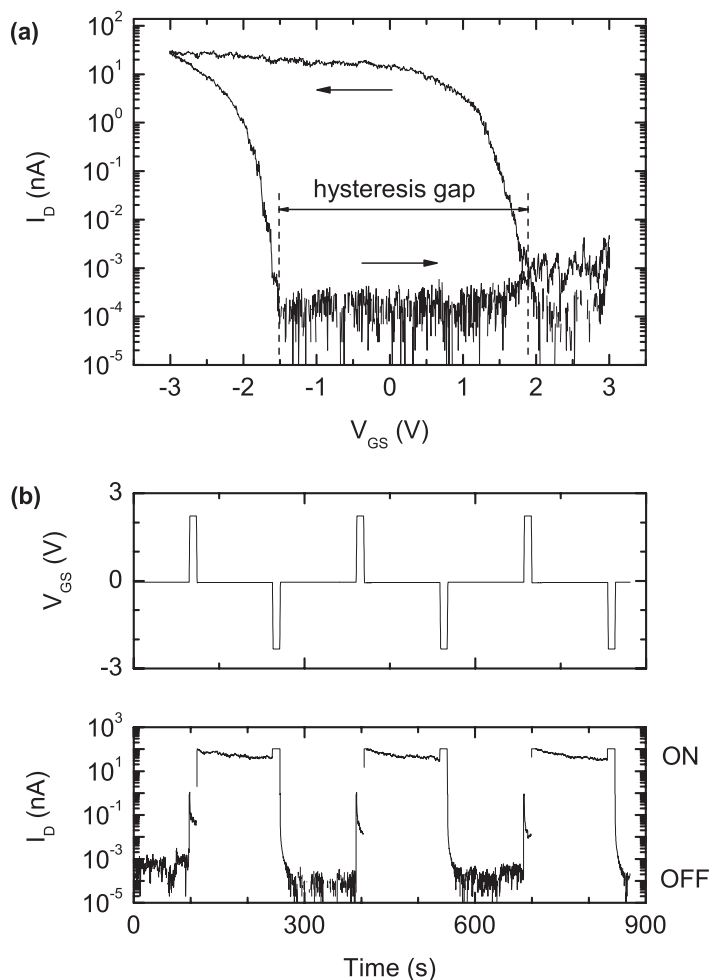


Figure 2. Memory effect for a typical SWCNT FET with a gate dielectric of HfO_2 . (a) Drain current versus backgate voltage at a constant drain–source voltage of 10 mV. The arrows mark the scan direction within the loop. The hysteresis gap is given by the difference in threshold voltage between the reverse and the forward scan direction. (b) Demonstration of its memory function. The upper panel displays the voltage applied to the backgate as a function of time. The lower panel shows how at a constant V_{DS} of 0.1 V, the current response through the CNT switches to an ON state or an OFF state in response to a positive or negative voltage pulse on the backgate, respectively.

with its intended function. The large number of devices in this study allows us to estimate the distribution of hysteresis response seen for differing gate dielectrics. We quantify the memory effect in each device in terms of the shift in threshold voltage, called the hysteresis gap (see figure 2(a)). This measure relates directly to the reconfiguration of charges trapped in the close vicinity of the SWCNT, and is sensitive to the gate voltage scan rate, the scan range, as well as the hold time at the turning points of the scanning interval before starting the next scan. While the scan rate was kept at 10 mV s^{-1} and the hold time at the turning points was close to 1 s throughout the study, the gate voltage scan range was altered between the samples

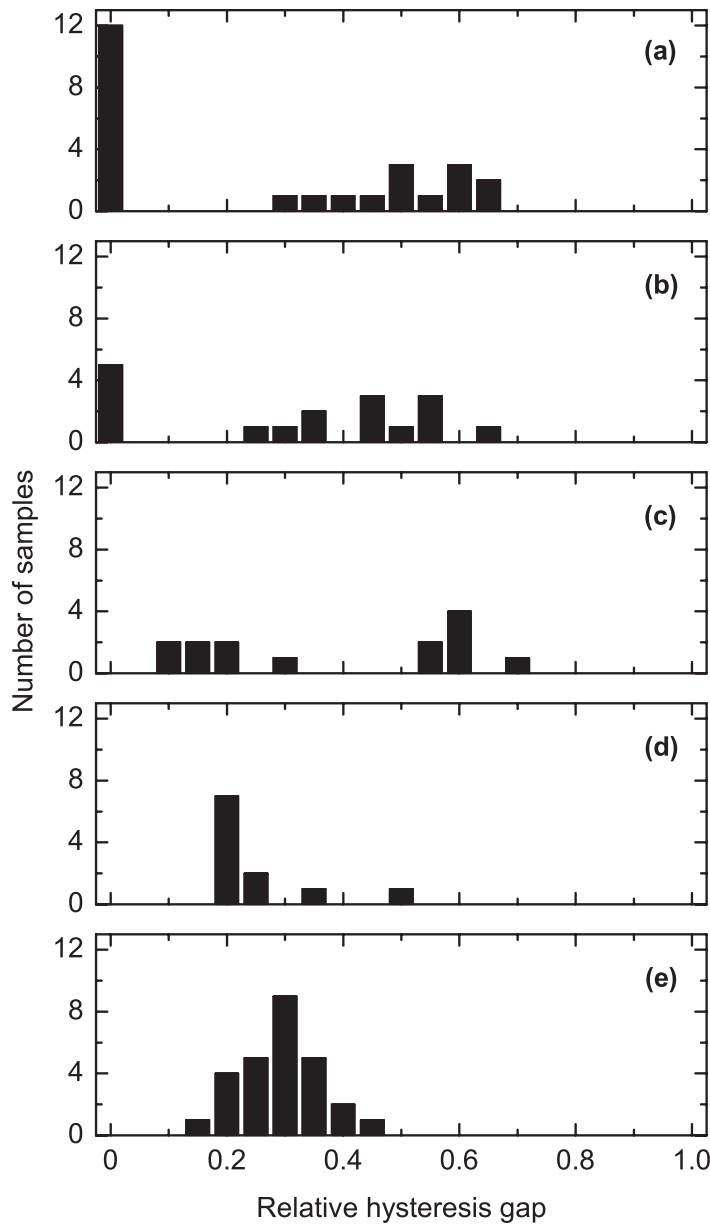


Figure 3. Statistics of the relative hysteresis gap from 94 devices with varying gate dielectric. Each column represents a 5% interval of the full scale. The gate dielectric is in (a) SiO₂ (300 nm), (b) Al₂O₃ (20 nm), (c) HfO₂ (20 nm), (d) HfO₂-TiO₂-HfO₂ (40–0.5–3 nm) and (e) HfO₂-TiO₂-HfO₂ (40–0.5–1 nm).

due to differing gate insulator thicknesses. The samples with 300 nm thick SiO₂ dielectric were measured with a gate voltage scan range of ± 10 V, while the ALD based samples with gate insulator thicknesses of 20–43.5 nm had gate voltage scan ranges of ± 2 –3 V. To allow comparison between these different cases, we calculated the relative hysteresis gap, where the hysteresis gap is normalized by the gate scan range. The measured threshold voltages together with ON and OFF conductance values for the CNT devices are presented in appendix B.

Our results are plotted in figure 3. Each column represents a 5% interval of the relative hysteresis gap along the x -axis. We show in figure 3(a) that from 25 SiO₂-based CNT FETs, 12

Table 1. Statistics taken from data in figure 3, with the lettering of gate dielectric in the first column according to that of the panels. The following columns display the total number of samples, the mean relative hysteresis gap, and its standard deviation.

Gate dielectric	Number of samples	Mean relative hysteresis gap	Standard deviation
a	25	0.27	0.27
b	17	0.32	0.24
c	14	0.38	0.22
d	11	0.26	0.09
e	27	0.29	0.06

devices do not exhibit hysteresis at all. The remaining 13 display a relative hysteresis gap almost evenly spread within the interval 30–65%. The results are in agreement with earlier reports [14, 16] on SiO₂-based SWCNT FETs, finding that only a fraction of the produced devices show hysteresis in their transfer characteristics. The picture is very similar in figure 3(b), where the SWCNT FETs have a gate dielectric of 20 nm thick ALD grown Al₂O₃. Five devices show no hysteresis, whereas 12 devices have their relative hysteresis gap within the interval 25–65%.

For the remaining three panels of figure 3, there is a distinct difference in that *all* the fabricated devices display a clear relative hysteresis gap. With memory devices in mind, this translates into a 100% fabrication yield. In figure 3(c), the gate dielectric is 20 nm thick ALD grown HfO₂. The 14 devices made have their relative hysteresis gaps spread from 10% up to 70% of the total gate scan range. While all CNT FETs in this set show a memory effect, the distribution of the relative hysteresis gaps is very wide, having a standard deviation of 22%. The following two panels of figure 3 show data from a specially designed three-layered ALD structure. It was made in order to study the hypothesis that the lower interface of the top most HfO₂ layer could play an important role in controlling the amount of charge traps available. The first deposited layer is a 40 nm thick buffer layer of HfO₂ with the purpose of providing a stable dielectric which can withstand the physical stress of sample processing. Next a 0.5 nm thick layer of TiO₂ was deposited with the intent of creating an interface to the top most layer. Finally another layer of HfO₂ was deposited, with a thickness of 3 nm in figure 3(d) and 1 nm in figure 3(e). While the total thicknesses of the ALD dielectrics in figures 3(d) and (e) are about twice the thickness in figure 3(c), the lower interface of the top HfO₂ layers are moved considerably closer to the CNT. The resulting relative hysteresis gap distributions show strongly decreased standard deviations of 0.09 and 0.06 for figures 3(d) and (e), respectively. More so, the latter panel with a top layer of only 1 nm thickness displays a distribution of relative hysteresis gap values that closely resembles the normal distribution. This indicates that the distribution is not likely to change noticeably if we were to add more samples to the study.

Our results are summarized in table 1, displaying the number of samples, the mean of the relative hysteresis gap, and its standard deviation for each type of gate dielectric according to the lettering in figure 3. Clearly, the triple layer with thinner upper HfO₂ layer is the better choice as gate insulator when preparing a memory storage device. More importantly, we show here that memory effects in a CNT FET can be controlled in ambient conditions, even without applying any kind of surface passivation layer onto the device. To test the influence of surface

chemistry (e.g. adhered H_2O molecules) on the memory effects seen for CNT FETs with the thinner triple-layer ALD dielectric, 12 of these samples were measured in a chamber with dry nitrogen gas flow, reducing the relative humidity to less than 1%. The samples were kept at these conditions from 30 min up to 18 h, while repeatedly measuring the transfer characteristics [30]. The relative hysteresis gap decreased somewhat during the first 30 min, on average 12% with a standard deviation of $\pm 8.6\%$, and was thereafter stable. The ON and OFF states remained almost unaffected. It is therefore reasonable to assume that while the water molecules adhered to the surface of the CNT and the dielectric somewhat affect the hysteresis, they play a minor role in the memory effects seen. In addition, the fact that changes in memory effects follow changes in gate dielectric, with relatively narrow distributions in two cases, discredit the model that defects in the SWCNTs are providing the charge traps responsible for the hysteresis. The reason for the differences seen between single layer dielectrics of SiO_2 , Al_2O_3 and HfO_2 is difficult to discern, but may be related to differing charge trap densities, or even types of charge traps. While we have not made direct measurements of the charge trap densities, this could possibly be done for charge traps close to the surface using either scanning probe microscopy or conductive AFM.

Turning our attention to the rapidly narrowing distribution in hysteresis gap when going from single layer HfO_2 to a triple-layered dielectric structure, the most significant difference in the surrounding of the CNT is the closely located interface between the HfO_2 and the TiO_2 layer. It is commonly known that the interface between two different materials may carry defects or charge traps. An alternative explanation could be that as the top-layer of HfO_2 becomes thinner, its surface becomes rougher and hosts an increasing number of defects, e.g. oxygen vacancies. The defects may act as charge traps and cause the increased hysteresis. But here we would like to point out two opposing observations. Firstly, surface defects are likely to interact with or be screened by adhered water molecules, which then would decrease the relative hysteresis gap in ambient conditions. We see the opposite trend, a slight decrease of the relative hysteresis gap in dry nitrogen flow. Secondly, our AFM measurements show no quantitative difference in surface roughness between the samples with different layer thicknesses. Here should be added though that the AFM is working close to its limit of resolution, measuring roughnesses of the order of 0.1 nm. From Si MOSFETs it is known that mobile charge traps within the gate dielectric cause retarded hysteresis [31]. Here we see the opposite, advanced hysteresis, which is the case for charging of stationary charge traps close to the CNT. While mobile charge traps also may be present within the dielectric, and could possibly be a minor contributor to memory effects seen in the single layer dielectrics, it is reasonable to assume on the basis of these data that moving the lower interface of the upper HfO_2 layer closer to the CNT provides a layer of stationary charge traps at a well-calibrated distance from the CNT. This is supported by the notion that a layer of stationary charge traps in the vicinity of the CNT will screen the action from mobile charge carriers, thus creating a well-defined device geometry with a narrow hysteresis gap distribution. We therefore conclude that the most probable dominating charge storage mechanism in the triple layer structure is due to stationary charge traps at the lower interface of the uppermost HfO_2 layer, which are filled and emptied by charge carriers from the CNT in response to application of a negative or a positive gate voltage.

Here, we would like to end with a short discussion of the response time of the memory devices. As was mentioned earlier in the measurements section, the shortest write and erase pulses that were used for switching the CNT memories in this study had a duration of 0.1 s. From earlier studies by others we have found working frequencies for CNT FET memories of at most 100 Hz [12, 13, 32]. This is a number that needs to be improved to be able to compete

with, e.g. commercial flash memories, which currently have write and erase times approaching $100\ \mu\text{s}$ [33] and readout performed in tens of nanoseconds [34]. It has been shown that the CNT FET itself can have a working frequency of tens of GHz [35], making the readout competitive. Hence, the limiting factor is the response time for write and erase operations. Here the charge trapping mechanism is of fundamental importance. Naturally, mobile ions or charges within the dielectric layer as well as molecules adhered to the surface have, due to their size, a slower response time compared to stationary charge traps, where electrons are responsible for the charge redistribution. Thus, stationary charge traps should provide the more competitive charge storage mechanism. We are currently investigating these aspects.

4. Summary

We have investigated 94 SWCNT FETs with different gate insulators, giving us unprecedented statistics on the presence of hysteresis in their transfer characteristics. We find that by using a gate dielectric composed by consecutive ALD layers of HfO_2 , TiO_2 , and then HfO_2 again, all SWCNT FETs display hysteresis with a narrow distribution of their relative hysteresis gaps, which narrows down further when the upper most layer is changed from 3 nm to 1 nm. The study shows that these SWCNT FETs can be fabricated and operated in ambient conditions without any surface passivation. This points toward having stationary charge traps beneath the upper layer that are dominating the electrostatic charging in the vicinity of the CNT such that the memory effect is insensitive to changes in the relative humidity. Such a layered gate dielectric is of particular interest for memory applications, providing to our knowledge the first proven route to 100% yield in single CNT-based memory elements. However, several challenges remain to be solved in order to make highly integrated CNT memory cells, such as positioning the CNTs with nm precision and providing each of them with a local, nanotube-specific gate.

Acknowledgments

We acknowledge valuable discussions with Professor H Häkkinen, and our research project collaborators: Professor M Ahlskog's and Professor K Rissanen's groups at University of Jyväskylä, as well as the companies Vaisala Oyj and Nokia Oyj. We thank Beneq Oy and Olli Jylhä for ALD processing and suggesting the materials used. This work was supported by the Finnish Funding Agency for Technology and Innovation (TEKES), project number 40309/05, and the Academy of Finland. MR acknowledges support from the Magnus Ehrnrooth Foundation and the Finnish Foundation for Technology Promotion (TES).

Appendix A. Nanotube diameters and FET channel lengths

The physical dimensions of each CNT FET was determined through AFM imaging. A pie chart of nanotube diameters used in this study is presented in figure A.1. Most of the nanotubes have diameters between 0.8 nm and 3 nm (all together 73 nanotubes, or 78%) and are interpreted as single-walled nanotubes. The rest of the tubes fall between 3 nm and 10 nm and are probably comprised of large diameter single-walled and/or multi-walled carbon nanotubes and nanotube bundles.

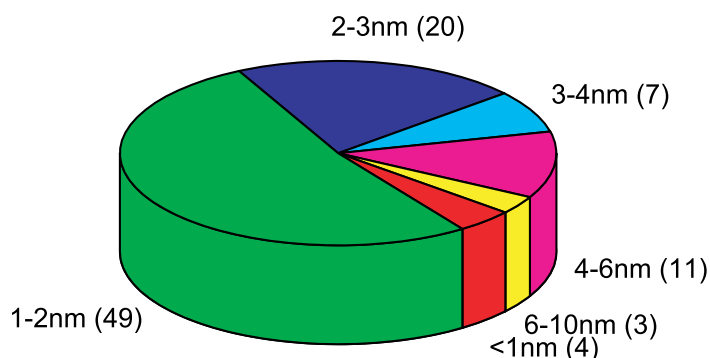


Figure A.1. Distribution of the conduction channel diameter for the CNT devices, with the interval displayed in nanometres followed by the number of CNTs within that range. The CNT diameter was determined from AFM images.

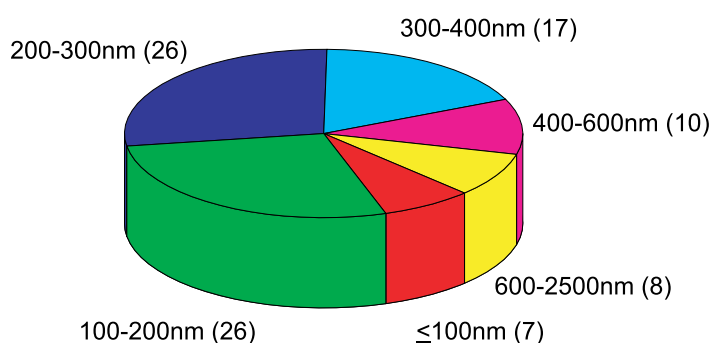


Figure A.2. Distribution of CNT lengths between the source and drain electrodes. The channel length interval is displayed followed by the number of devices in that range.

A pie chart of transistor channel lengths is presented in figure A.2. Most of the channel lengths fall in between 70 nm and 600 nm (all together 86 nanotubes, or 91%), leaving only eight devices in the range from 600 nm to 2.5 μm .

Appendix B. Threshold voltages and ON and OFF conductances

In this section, the threshold voltages from all samples in the study are presented, see figure B.1. The values are extracted from the drain current versus backgate voltage data taken at ambient conditions. When sweeping the backgate voltage in forward and reverse directions, different threshold voltages are seen for some of the samples, as explained in the measurements section and shown in figure 2(a). Both forward (blue) and reverse (red) sweep threshold voltage values are displayed, and divided into different panels according to the dielectric layer used. The last 12 samples in panel (a) and the last five samples in panel (b) show no shift in threshold voltage. The remaining samples have a shift in threshold voltage between forward and reverse scan directions, which depends on the scan rate, the scan range and the hold time when changing the scan direction. Therefore the scan rate was kept at 10 mV s^{-1} and the hold time at about 1 s throughout the study. Due to the significantly thicker (300 nm) dielectric of SiO_2 compared to

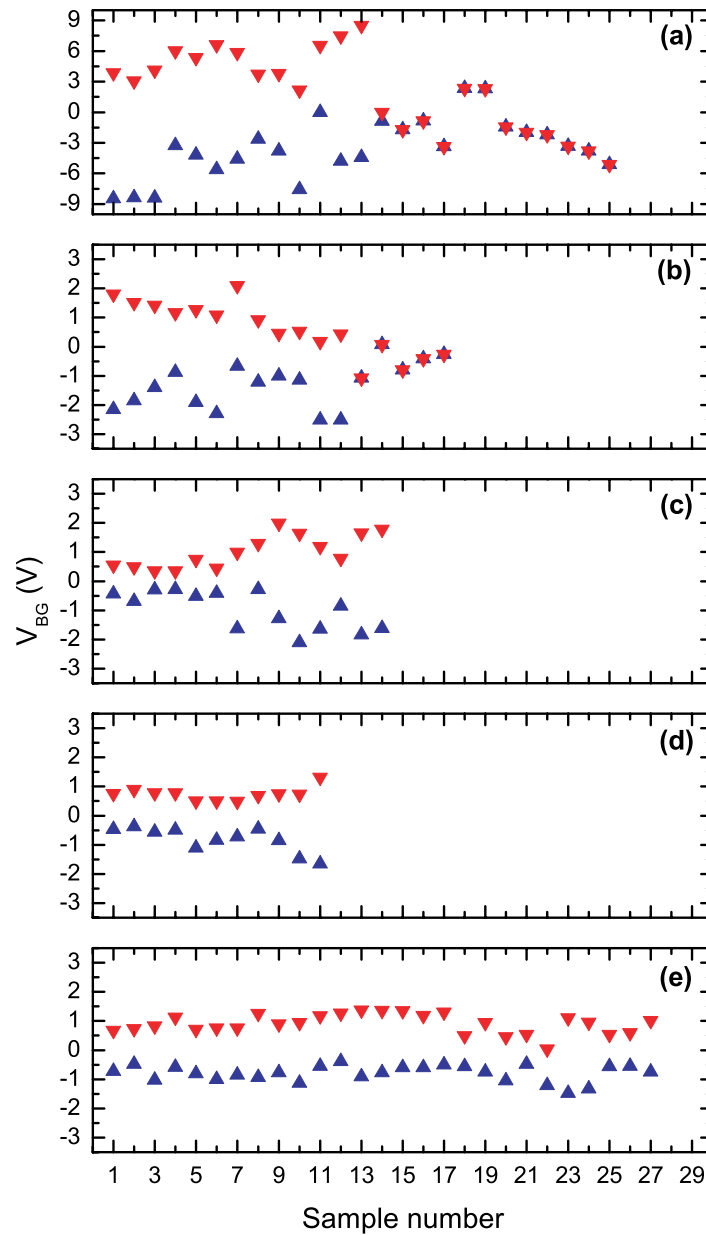


Figure B.1. Threshold voltages for forward (blue) and reverse (red) scan directions for all samples. The voltage scan range was in (a) ± 10 V and in the rest of the panels ± 2 –3 V. The gate dielectric is in (a) SiO_2 (300 nm), (b) Al_2O_3 (20 nm), (c) HfO_2 (20 nm), (d) HfO_2 – TiO_2 – HfO_2 (40–0.5–3 nm) and (e) HfO_2 – TiO_2 – HfO_2 (40–0.5–1 nm).

the other gate dielectrics (20–43.5 nm), a higher backgate voltage range was used to produce the electric field strength required for reaching the saturation plateau in the ON state. All the SiO_2 based CNT FETs in figure B.1(a) have a scan range of ± 10 V. All the samples in the remaining panels have a scan range of ± 3 V, except for a few exceptions. The exceptions are samples 11 in panel (c) and 17, 25 and 26 in panel (e), which have a scan range of ± 2.5 V and sample 12 in

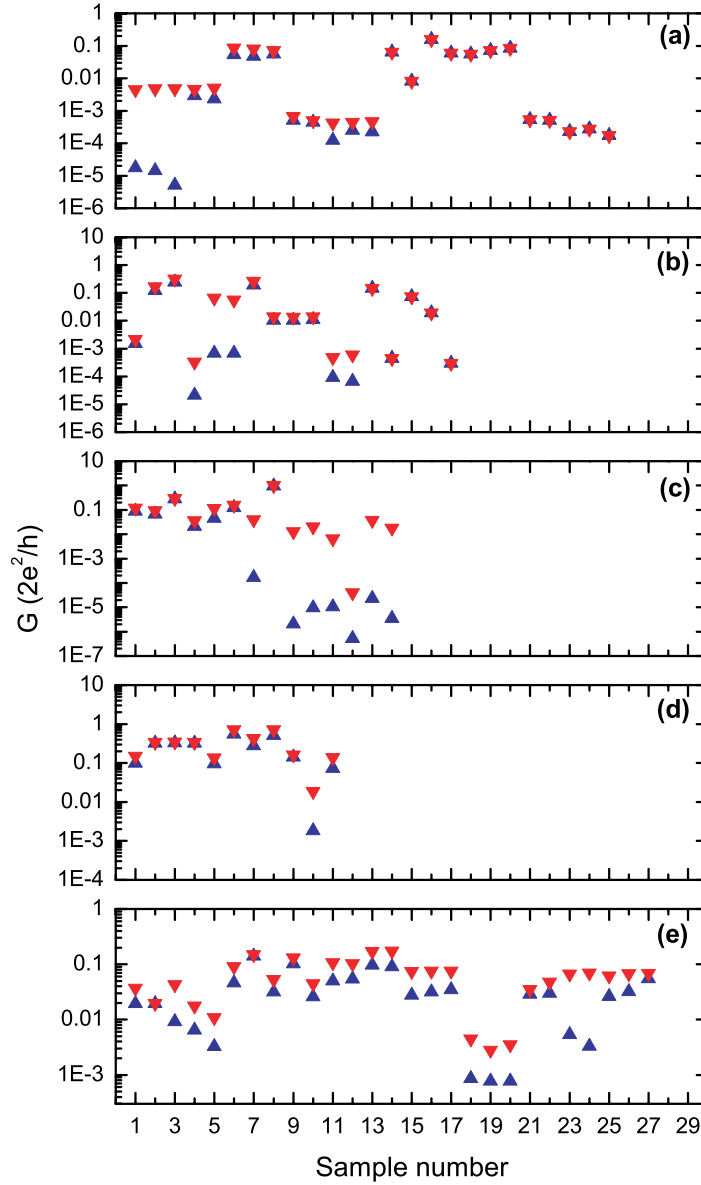


Figure B.2. ON (red) and OFF (blue) conductances for the CNT memories at zero gate voltage. The gate dielectric is in (a) SiO₂ (300 nm), (b) Al₂O₃ (20 nm), (c) HfO₂ (20 nm), (d) HfO₂–TiO₂–HfO₂ (40–0.5–3 nm) and (e) HfO₂–TiO₂–HfO₂ (40–0.5–1 nm).

panel (c) which has a scan range of ± 2 V. It has been shown that for CNT FETs with hysteresis, the threshold voltage value scales roughly linearly with the scan range for quite large voltage ranges [10, 18]. Therefore we calculate the hysteresis gap and normalize it with the scan range to include the samples with a differing scan range. The normalization also makes comparison of the hysteresis gap distribution between different samples sets easier, as seen in figure 3.

The corresponding ON and OFF conductance values for the memory devices are displayed in figure B.2. The ON and OFF values are taken at zero gate voltage, as appropriate for nonvolatile memory readout. The last 12 samples in panel (a) and the last five samples in

panel (b) have no shift in threshold voltage, and thus show the same conductance value for both forward and reverse scan directions. The best memory devices have an ON/OFF ratio of about four orders of magnitude, while some of the others have a value just above 1. We would like to point out that in these cases the ON and OFF states were clearly separated and reproducible in the data. The small ON/OFF ratios in some of the samples are caused by a ‘bad’ or highly conducting OFF state, which could be explained by these devices consisting of either a small band gap CNT or a bundle of several CNTs instead of a single tube. But for memory applications, a large ON/OFF ratio is of much smaller importance than having a narrowly distributed hysteresis gap. We therefore also valued these samples and included them in the study.

Appendix C. Mobility and subthreshold swing

For determining mobilities for our devices we first calculated the nanotube capacitances per unit length with respect to the backgate given by $C_{bg}/L \approx 2\pi\epsilon\epsilon_0/\ln(2h/r)$, where r and L are the nanotube radius and the length of the device, and h and ϵ_0 the thickness and the average dielectric constant of the dielectric [27]. For the SiO₂ samples the calculated capacitances were around $C_{bg}/L \sim 0.33 \text{ pF cm}^{-1}$ and for the Al₂O₃ samples $C_{bg}/L \sim 1.1 \text{ pF cm}^{-1}$. In the capacitance calculation, we used average dielectric constant values of 3.95 for thermally grown SiO₂ and 7.5 for the ALD grown Al₂O₃ gate dielectric. For the ALD grown HfO₂-based gate dielectrics we used an ϵ_0 value of 25 for all. The corresponding capacitances are $C_{bg}/L \sim 4.0 \text{ pF cm}^{-1}$ for the HfO₂ (20 nm) samples and for the HfO₂-TiO₂-HfO₂ (40–0.5–3 nm) and (40–0.5–1 nm) samples $C_{bg}/L \sim 3.2 \text{ pF cm}^{-1}$, and $C_{bg}/L \sim 3.7 \text{ pF cm}^{-1}$, respectively. As most of the calculated capacitances are close to the quantum capacitance of a carbon nanotube having a value in the order of $C_q/L = 4e^2/\pi\hbar v_F \sim 4 \text{ pF cm}^{-1}$, we need to take C_q into account. Here v_F is the Fermi velocity. The C_{bg} and the C_q add inversely, so that the total capacitance is $C = (1/C_{bg} + 1/C_q)^{-1}$ [36]. For devices having SiO₂ as a gate dielectric the contribution from the gate capacitance clearly dominates over the quantum capacitance.

For calculating the mobility of our devices we used the so-called ‘field-effect mobility’ μ_{fe} , which is often used to compare device properties. It is device specific and includes e.g. surface effects, contact resistances, etc. The field-effect mobility of a SWCNT FET can be calculated by [7]

$$\mu_{fe} = \frac{L^2}{C} \frac{\partial G}{\partial V_{bg}}, \quad \text{where } V_{bg} \text{ is the backgate voltage.} \quad (\text{C.1})$$

Purewal *et al* [37] reported electron mean free paths for semiconducting SWCNTs ranging from $\sim 250 \text{ nm}$ to $\sim 800 \text{ nm}$ at room temperature. The majority of our CNT devices have lengths that fall between 70 nm and 600 nm , and are thus in the ballistic limit where the field-effect mobility does not apply. We therefore calculated the mobility for our longest device of $2.5 \mu\text{m}$, which has HfO₂-TiO₂-HfO₂ (40–0.5–1 nm) as its gate dielectric. Using equation (C.1), we extracted a value of $200 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which corresponds well to previously reported mobilities for similar devices [12, 13, 27, 38, 39].

We also calculated the subthreshold swing S , which is given by $(d(\log G)/dV_{bg})^{-1}$. We found for our SWCNT FETs values as small as $100 \text{ mV decade}^{-1}$, e.g. from the data shown in figure 2(a). This is close to the theoretical limit of $60 \text{ mV decade}^{-1}$ [6].

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