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Title: Noise of a single electron transistor on a Si3N4 membrane

Year: 1999

Version: Final published version

Please cite the original version:

Hakonen, Pertti J. & Ikonen, J. M. & Parts, U. & Penttilä, J. S. & Roschier, L. R. & Paalanen, M. A.. 1999. Noise of a single electron transistor on a Si3N4 membrane. Journal of Applied Physics. Volume 86, Issue 5. 2684-2686. ISSN 0021-8979 (printed). DOI: 10.1063/1.371110.

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Citation: Journal of Applied Physics **86**, 2684 (1999); doi: 10.1063/1.371110
View online: http://dx.doi.org/10.1063/1.371110
View Table of Contents: http://scitation.aip.org/content/aip/journal/jap/86/5?ver=pdfcov
Published by the AIP Publishing

Noise of a single electron transistor on a Si_3N_4 membrane

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(Received 5 January 1999; accepted for publication 27 May 1999)

We have investigated the influence of electron-beam writing on the creation of charge trapping centers which cause $1/f$ noise in single electron transistors (SET). Two $Al/AlO_x/Al$ devices were compared: one where the SET is on a {100} silicon wafer covered by a 120-nm-thick layer of Si_3N_4, and another one in which the Si was etched away from below the nitride membrane before patterning the SET. The background charge noise was found to be $1\times10^{-3}e/\sqrt{\text{Hz}}$ at 10 Hz in both devices, independent of the substrate thickness. © *1999 American Institute of Physics.* [S0021-8979(99)02517-7]

INTRODUCTION

Single electron transistors (SET), as well as other devices based on tunneling of individual electrons, have been investigated vigorously during the past decade.[1,2] One of the major problems hampering practical applications of such devices has turned out to be the strong, ubiquitous $1/f$ noise which easily drives these devices out of their operating points unless compensative measures are taken. Therefore, this noise presents a fundamental problem on the operation and integration of single electron devices.

A lot of effort has been put into understanding the $1/f$ noise in single electron transistors. The present picture, based on several investigations,[3–12] indicates that the noise is caused by trapping centers of charge both in the vicinity of the island as well as in the tunnel barriers themselves. Sometimes conductance fluctuations in the tunnel barriers dominate,[8] while typically background charge fluctuations on the substrate are more important, as demonstrated in correlation measurements[9] and in detailed studies of trapping state dynamics.[10]

We have investigated how much of the $1/f$ noise in SETs can be attributed to the lithography phase, i.e., to the e-beam writing process that is known to cause damage in the substrate. Is the amount of damage large enough so that it causes a major fraction of charge trapping states and, thereby, most of the $1/f$ noise. To test this hypothesis we have considered two structures in which the amount of damage in the e-beam writing should differ radically: one where the SET is on a {100} silicon wafer covered by a 120-nm-thick layer of Si_3N_4, and another one in which the Si was etched away from below the nitride membrane before patterning the SET. By making the substrate thickness small it is possible to reduce the amount of backward scattering (secondary electrons) and, thereby, to minimize the damage in the e-beam writing process.

As there is evidence that the noise scales with SET size,[7,8] we chose to work with quite large island areas so that the sensitivity towards substrate defects would be large. We also chose to work with superconducting samples since the charge sensitivity is higher but the charge trapping should not be affected in any way.[13] Within our resolution, however, no contribution can be assigned to the e-beam writing process.

SAMPLE FABRICATION

The samples were manufactured using a 375-μm-thick Si substrate with both sides covered by 120-nm-thick Si_3N_4 layers. The silicon nitride was grown using low-pressure chemical vapor deposition which yielded membranes under considerable tensile stress. Hence, free-standing structures could be easily constructed.

First, a window of size $600\ \mu\text{m}\times600\ \mu\text{m}$ was etched to the back Si_3N_4 layer using reactive ion etching (RIE) with CHF_3. A 35 nm layer of chrome, patterned using PMMA resist and a $K_3Fe(CH)_6$-based etching solution, made up the mask in the RIE step. The final step, the etching through the Si substrate, was made with 20 mass % KOH solution at 70 °C.[14] The etching in KOH took 5 h and provided us with a free-standing $100\ \mu\text{m}\times100\ \mu\text{m}$ Si_3N_4 membrane. A two-layer resist, made of 250 nm of PMMA/MAA and 100 nm of PMMA, was then spun on top of the membrane in order to facilitate regular e-beam lithography. The last step was the only one in the fabrication of the unetched reference sample.

The SETs were made using a standard two-angle evaporation technique[15] with resistive Al evaporation. The geometric size of the junctions at the ends of a $140\times1200\ \text{nm}^2$ central island were $100\times100\ \text{nm}^2$. The total capacitance of the SETs was determined from the offset voltage $V_b=e/C$ of the IV curve at large bias. The etched sample (E) had a total capacitance of 1.2 fF while for the unetched sample (U) we obtained 1.8 fF. The gate capacitance C_g was determined from the periodicity of the modulation curves: $C_g(E)=10\ \text{aF}$ and $C_g(U)=92\ \text{aF}$. The sum of the tunneling resistances was 400 and 215 kΩ for samples E and U, respectively.

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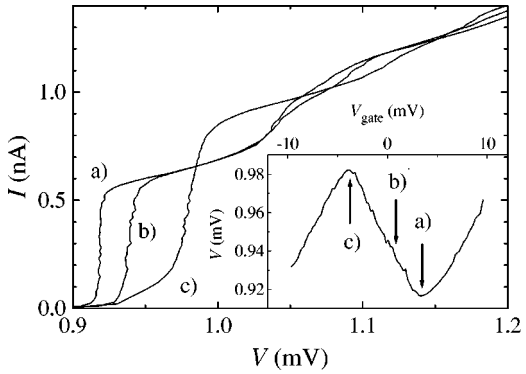

FIG. 1. *IV* curves measured on the SET on a Si_3N_4 membrane for three gate charges: (a) 0, (b) 0.2e, and (c) 0.5e. Temperature $T=150$ mK. The inset shows the gate modulation of the drain voltage using 0.38 nA bias current. Arrows denote the locations of the gate biasing points in the *IV* measurement.

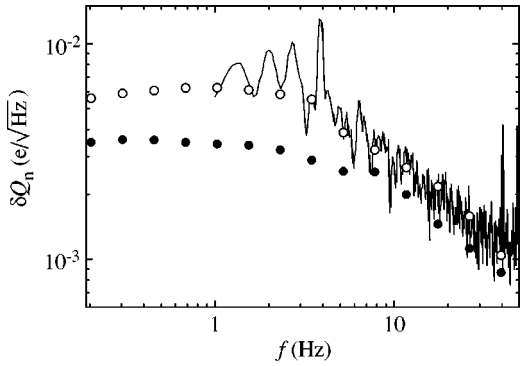

FIG. 2. Charge noise measured on an ''etched'' (○,●) and on an ''unetched'' (-) SET. The filled and open symbols refer to measurements at minimum and maximum gain, respectively. For the unetched sample, only data at maximum gain are shown.

NOISE MEASUREMENTS

Our experiments on noise covered the frequencies 0.2–50 Hz. The upper limit was set by the RC time constant of the sample and wiring setup. The lower end was limited by the temporal stability of the SET operating point. At 0.2 Hz, the duration of the record was about 5 min. The gain of the SET remained practically unchanged over this period of time and, thus, a feedback arrangement keeping the operating point stable was not considered necessary.[6] In fact, even longer measuring periods could have been possible but 0.2 Hz was definitely a safe cutoff.

The noise measurement on sample E was carried out using an SR830 lock-in amplifier (Stanford Research Systems, Sunnyvale, California). This device has a built-in numerical algorithm to calculate the magnitude of Gaussian noise. For all measuring frequencies the equivalent noise bandwidth $(1/8\tau)$ was taken to be less than 1/5 of the frequency. The measuring time (the averaging time of the samples) was proportional to the time constant τ of lock-in by a factor of 10–80. Owing to these conditions, a data record lasting for $50/f$ was employed in the measurement at each frequency f. Reference sample U was measured using a HP89410 spectrum analyzer.

We followed the procedure outlined by Starmark *et al.*[12] and measured the noise separately using the minimum and maximum gain of the SET. This ensured that the origin of the noise can be traced back to the SET itself. Using modulation techniques, we were also able to check that the major part of the noise in sample U came from background charge variations and not from $1/f$ resistance fluctuations.

RESULTS

We made our experiments in the superconducting state at 150 mK. The advantage of the superconducting state is that single electron effects can be seen more easily at high temperatures.[4,13] At this temperature, the operating point of the minimum gain is not too sharp, as seen from the inset in Fig. 1. In addition, when operating at high temperatures we avoid problems with self-heating which can be substantial in certain cases.[16] Since previous experiments have not shown any strong T dependence at the lowest temperatures,[5] experiments at $T=150$ mK were considered sufficient.

Figure 1 illustrates *IV* curves measured on sample E using current bias at three different gate charges; the gate biasing points are denoted by arrows on the modulation curve shown in the inset. The maximum modulation 70 μV is somewhat less than the value e/C obtained from the *IV* curve offset measurements in the normal state. Since the gain is almost constant over large variation in the gate charge, even large background charge fluctuations can be tolerated without the need of feedback in the noise measurements. When measuring at minimum gain, the operating point was checked right before and after the noise scan.

Our results on SET noise are displayed in Fig. 2. The general shape, showing saturation at the lowest frequencies and a corner to $\sim 1/f$ dependence around 1 Hz, agrees with former experiments (see, e.g., Refs. 10–12). The noise is large, two orders of magnitude larger than the reported value for the best, stacked construction,[8] which reflects the fact that the island size (and, consequently, the junction size) was chosen to be rather large. At 10 Hz, we obtain $3\times10^{-3}\,e/\sqrt{\text{Hz}}$ in the superconducting state while in the normal state the corresponding figure is $2\times10^{-3}\,e/\sqrt{\text{Hz}}$; after subtracting the noise at minimum gain we obtain $1\times10^{-3}\,e/\sqrt{\text{Hz}}$ in both cases.

The noise over 1–50 Hz was found to be the same for the etched and unetched samples. Below 1 Hz, however, there is a slight difference. The corner between constant noise and $1/f$ behavior takes place at lower frequencies for sample U than for sample E. The data have been omitted from the picture because the gain changed below 1 Hz due to the ac input filter of the HP89410 spectrum analyzer. The smaller amount of low-frequency noise in the etched sample was seen in the *IV* measurements as well: the curves measured over 2 min on sample E are much more stable than on sample U.

DISCUSSION

On the basis of this work, we are inclined to conclude that the quality of the original substrate is more important than the minimization of defects produced by the e-beam

writing procedure. In this sense, the recommendation of Ref. 8, viz. that the contact area between the SET and the substrate has to be minimized, sounds reasonable. It is possible of course that our Si_3N_4 membranes were not thin enough to reduce the damage caused by secondary electrons in the writing process or that etching by KOH induced potassium atoms into the substrate,[17] even though their mobility is rather limited.[18] On the other hand, large stress of the substrates might play a role and, therefore, it would be interesting to make similar experiments on nonstoichiometric Si_3N_4 membranes with less tensile stress.

One way to improve the results might be to etch the SET structure completely free as has been done with wires and films.[19] Of course, the present design with a loose gate is not suitable, but a separate back gate could well be used. An ensuing problem is that reactive ion etching does produce defects in the aluminum itself, which has been seen clearly as an increase in the superconducting transition temperature.

ACKNOWLEDGMENTS

The authors are obliged to Sami Franssila (State Research Center, Espoo) for the Si_3N_4 coatings. The authors wish to thank Mikko Kiviranta, Alexander Korotkov, Sami Lähteenmäki, Heikki Seppä, and Alexander Zorin for useful discussions. This work was financially supported by the Academy of Finland, by TEKES of Finland via the Nanotechnology program, and by the Human Capital and Mobility Program ULTI of the European Community.

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