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Enhanced performance in the deteriorated area of multicrystalline silicon wafers by internal gettering

Yacine Boulfrad, Antti Haarahiltunen, Hele Savin, Eivind J. Ovrelid and Lars Arnberg

ABSTRACT

The deteriorated area of the multicrystalline silicon (mc-Si) ingots grown by directional solidification, commonly known as the Red Zone, is usually removed before wafering. This area, characterized by poor minority carrier lifetime, is located on the sides, at the top, and the bottom of the mc-Si ingots. In this study, the effect of internal gettering by oxygen precipitates and structural defects has been investigated on the bottom zone of a mc-Si ingot. Nucleation and growth of oxygen precipitates as well as low temperature annealing were studied. Photoluminescence imaging, lifetime mapping, and interstitial iron measurements performed by μ-PCD reveal a considerable reduction of the bottom Red Zone. An improvement of lifetime from below 1 μs to about 20 μs and a reduction of interstitial iron concentration from 1.32×10^{13} at/cm^3 to 8.4×10^{10} at/cm^3 are demonstrated in this paper.

1 INTRODUCTION

Solar cells based on crystalline silicon wafers, including multicrystalline and single crystalline, are still dominating the photovoltaic market with approximately 85% [1] of the production of solar modules. Multicrystalline silicon (mc-Si) wafers are produced mainly from block cast ingots grown by unidirectional solidification method.

Despite the beneficial effect of the unidirectional solidification method in refining metal impurities due to their segregation to the melt during the solidification, mc-Si ingots contain several transition metal impurities; their distribution along mc-Si ingot is heterogeneous. High concentrations of Fe, Co, and Cu are usually found near the top of the ingot [2]. This is due to the segregation process from the solid to the melt during solidification and the back diffusion during the cooling of the ingot. This part of the ingot is normally also characterized by a higher dislocation density exceeding 10^5 cm^{-2} [3]. Consequently, the part close to the top of the ingot very often shows a poor minority carrier lifetime and is difficult to improve by external gettering because of the trapping of impurities by dislocations [4]. It is usually cut from the blocks before wafering by the solar cell manufacturers; moreover, it cannot be recycled unless SiC and Si_3N_4 are removed from the silicon scrap [5].

High transition metal concentrations have also been measured near the bottom of the ingot because of the solid state diffusion from the crucible. A similar tendency with high levels of Fe near the side edges of the ingot has been reported by Nærland *et al*. [6]. The bottom and the near edge parts of mc-Si ingot are cut-out recycled regions, where external gettering is not sufficient to improve the quality of the material to achieve acceptable solar cell efficiency. This is mainly due to oxygen

precipitates for the bottom part and metal precipitates for the near edge one. All these defects present in the edge, top, and the bottom of mc-Si ingots results in a zone of low minority carrier lifetime, often called as the ‘Red Zone’.

It is clear that a reduction of the Red Zone, that is, the cut-off material will improve the ingot mass yield by producing more wafers per brick. One way to reach this goal is the use of high purity crucibles and coatings [7]. In addition, the increase of the industrial size of mc-Si ingots from 240 kg to 450 kg has naturally increased the fraction of waferable material leading to the enhancement of the ingot mass yield.

Internal gettering, that is, gettering of metal impurities by internal gettering sites that are often related to oxygen precipitates, has been used successfully in the past in semiconductor industry. It has also proven to be an effective process to improve the performance of as-grown mc-Si material, although the idea is quite different [8, 9]. An overview of internal gettering in microelectronics and photovoltaics technologies is published elsewhere [10].

This paper focuses on the effect of internal gettering in as-grown mc-Si wafers sliced from the bottom Red Zone. The aim is to improve the ingot yield by increasing the waferable material from the bottom part of the ingot. In addition to conventional low temperature annealing (LTA), the effect of special oxygen precipitation anneal on internal gettering efficiency is studied.

2 EXPERIMENTAL

We used *p*-type 5 × 5 cm^2 1 Ωcm mc-Si wafers with thickness of 220 µm, cut from a 12 kg cylindrical mc-Si ingot with a diameter of 25 cm and a height of about 10 cm directionally solidified in a lab scale Bridgman furnace (Crystalox DS250). Seven neighbor horizontal wafers were taken from about 8 mm far from the crucible bottom, whereas four neighbor vertical wafers were cut perpendicular to the bottom crucible wall as illustrated in Figure 1.

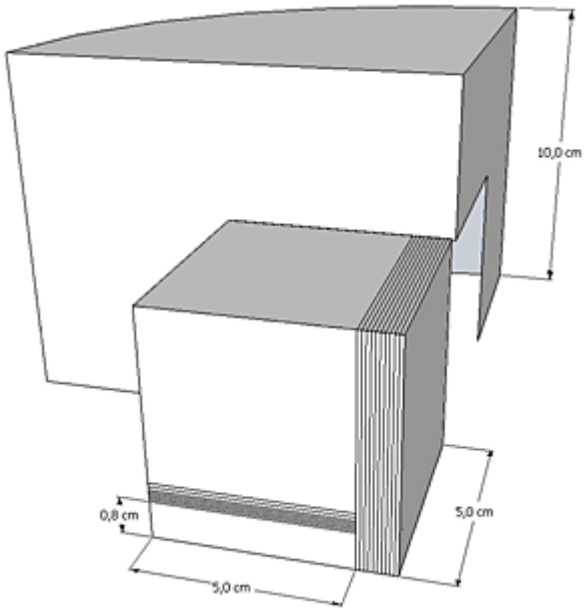

Figure 1. Illustration of the wafers' positions in the mc-Si ingot dedicated to the present investigation.

Wafering and saw damage removal were performed at Fraunhofer ISE institute. The wafers were subject to different annealing procedures in a tube furnace under argon atmosphere as shown in Table 1. Two wafers were kept as references. Uncalibrated photoluminescence images were taken on some wafers before and after the heat treatment.

Table 1. Summary of the experiments performed on the vertical and horizontal wafers; V and H denote vertical and horizontal wafers, respectively. AC refers to air cooling, LTA to low temperature annealing, and PDG to phosphorous gettering.

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Wafer/name	Pre-annealing	Thermal treatment	Cooling	PDG
V01/OP	1020°C (30 min)	650 °C (6 h) + 900 °C (2 h)	1 °C/min to 600 °C + AC	—
V02/LTA	—	550 °C (2 h)	AC	—
V03/HT + LTA	1020 °C (30 min)	550 °C (2 h)	AC	—
V04/PDG	—	—	—	Yes
V05/Ref		Reference		
H21	—	550 °C (4 h)	AC	—
H22	950 °C (1 h)	550 °C (2 h)	AC	—
H23	1020 °C (30 min)	550 °C (2 h)	AC	—
H24	1100 °C (20 min)	550 °C (2 h)	AC	—
H25	1020 °C (30 min)	550 °C (2 h)	AC	Yes
H26	—	—	—	Yes
H27		Reference		

For comparison, two wafers were gettered externally by means of phosphorous diffusion. Phosphorous was indiffused in a $POCl_3$ tube furnace at 830 °C for 30 min. The emitter layer was then removed in a CP5 solution (HNO3: Ch3COOH: HF, 10: 5: 2) for 90 s.

After thermal anneals, all wafers were cleaned in a Piranha solution (H_2SO_4: H_2O_2, 4:1) followed by a passivation with a layer of amorphous silicon a-Si:H on both sides by using plasma-enhanced chemical vapor deposition.

Lifetime measurements were carried out by means of the microwave-detected photoconductance decay μ-PCD by using a Semilab WT2000 (Budapest, Hungary).

Interstitial iron (Fe_i) was measured through μ-PCD by using Fe-B pair splitting technique where lifetime is measured before and after light soaking. The concentration of Fe_i was calculated by using the equation:

$$N_{Fe} = C_{\mu\text{-PCD}}\left(\frac{1}{\tau_{before}} - \frac{1}{\tau_{after}}\right)$$

where $C\mu\text{-PCD} = 3.4\times10^{13}$ μs/cm^3 was used.

Interstitial oxygen concentration (O_i) was measured by Fourier transform infrared spectroscopy, the absorption peak at 1107 cm^{-1} was used to quantify O_i according to ASTM F1188-93a standard [11].

A vertical cross-section 2 mm slice was dedicated to measure O_i along the ingot height. The slice was polished both sides prior to Fourier transform infrared spectroscopy measurements.

A set of samples, 1 × 1 cm^2 and approximately 2 mm thick was dedicated to measure Fe_i profile as a function of the distance from the ingot bottom. Seven horizontal neighbor samples were taken from the bottom and three similar ones from the center of the ingot.

3 RESULTS AND DISCUSSION

3.1 As-grown wafers

In as-grown wafers, interstitial iron and interstitial oxygen profiles along the ingot height shows an increase of both O_i and Fe_i towards the bottom accompanied with a decrease of the lifetime (Figure 2). As mentioned in the introduction, high concentration of Fe_i in the bottom and edges of the ingot is due mainly to diffusion from the crucible and coating during the crystallization of the material. O_i exists in higher concentrations than Fe_i because of the poor segregation of oxygen during the solidification of silicon (segregation coefficient close to 1). The increase of oxygen concentration towards the bottom is probably due to solid diffusion from the crucible coating. It has been shown that Fe_i is the dominant defect reducing the lifetime in the edge of mc-Si ingot [6]. According to Figure 2, a similar trend can be noticed in the bottom region.

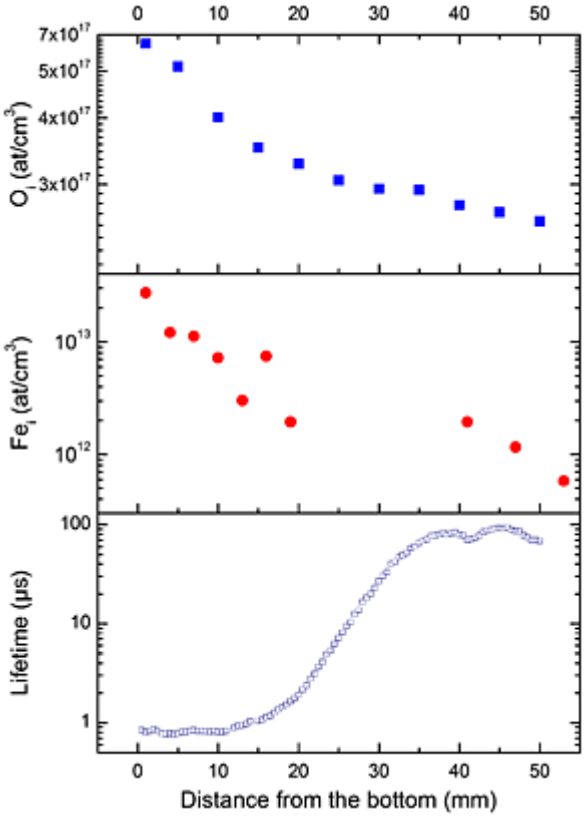

Figure 2. Average interstitial oxygen concentration (O_i), interstitial iron concentration (Fe_i), and lifetime along the half bottom part of the ingot.

The bottom Red Zone of mc-Si ingot is therefore characterized by relatively high concentration of metal impurities, particularly iron and dissolved oxygen, which is likely accompanied with relatively high density of oxygen precipitates. These factors make the bottom zone of mc-Si ingots a

good candidate for studying the effect of oxide precipitation on internal gettering efficiency. Moreover, the fact that this zone normally contains low dislocation density could be beneficial to final lifetime achieved by metal gettering.

3.2 Internal Gettering

3.2.1 Vertical wafers

Conventionally, the so-called high–low–high anneal is carried out to induce oxygen precipitates in silicon [12]. The first high-temperature anneal is performed to destroy the effect of the thermal history of the wafer. Following low-temperature anneal (typically at 500–650 °C) creates the oxygen nuclei. A final high temperature anneal is performed to grow the oxygen nuclei to larger precipitates.

In our experiments with vertical wafers, such three-step anneal, was performed for a vertical wafer (V01) taken from the bottom of the ingot, see Table 1 for details. The actual internal gettering process took place during slow cooling from 900 °C to 650 °C with a rate of 1 °C/min.

Figure 3 shows photoluminescence images of the wafer V01 before (3a) and after (3b) the heat treatments. The Red Zone can be seen clearly in the as-cut wafer (Figure 3a); it extends to about 2 cm from the bottom of the ingot. After the internal gettering process, the Red Zone has been clearly reduced (Figure 3b). This is likely due to the nucleation and precipitation of dissolved metal impurities around oxide precipitates and in grain boundaries.

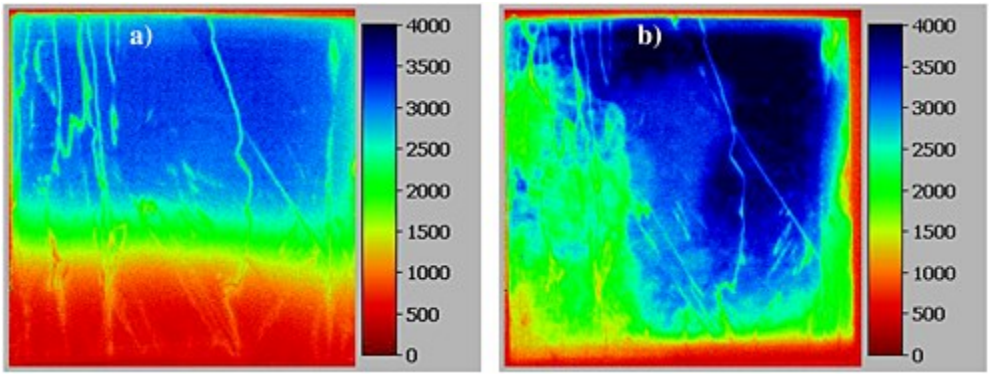

Figure 3. Photoluminescence images of the vertical wafer VA01 (a) before and (b) after the heat treatments illustrated in Table 1.

The next step is to compare the internal gettering efficiency in wafers with high–low–high treatment to slightly varying internal gettering treatments (V02 and V03), to phosphorous diffusion gettering (PDG) (V04), and to as-grown reference wafer (V05).

By comparing the iron profiles of wafers subjected to LTA and PDG treatments (Figure 4), it appears that the interstitial iron concentration is higher in the PDG wafer in almost all areas, except for a few millimeters from the bottom. Notice that this is not correlating with lifetime (Figure 5). In both cases (LTA and PDG wafers), the lifetime starts to decrease having similar shape around 15 mm towards the bottom, where oxygen approximately starts to increase (Figure 2). This indicates that after PDG and LTA, the lifetime is likely affected by oxygen-related defects close to bottom. Furthermore, it has been reported [13] that the injection of silicon self-interstitials during the PDG decreases the density of oxide precipitates and thus their recombination activity; this could

explain the higher lifetime measured in the bottom of the PDG wafer compared with the LTA one; another reason could be the higher interstitial iron remained in the LTA wafer in the 1 cm close to the bottom.

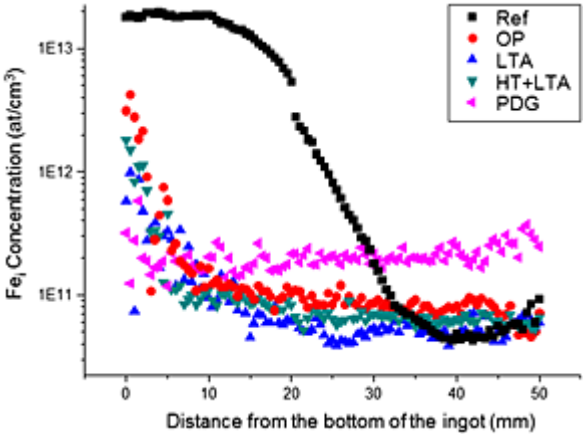

Figure 4. Average concentration of interstitial iron measured by Fe-B splitting technique of wafers VA01-05; Ref is the reference wafer (wafer VA05), OP refers to internal gettering in wafer with oxygen precipitation anneal (wafer VA01), LTA denotes low temperature annealing at 550 °C for 2 h (wafer VA02), HT + LTA refers to the high temperature pre-annealing at 1020 °C prior to LTA (wafer VA03), PDG is the phosphorous gettered wafer (VA04).

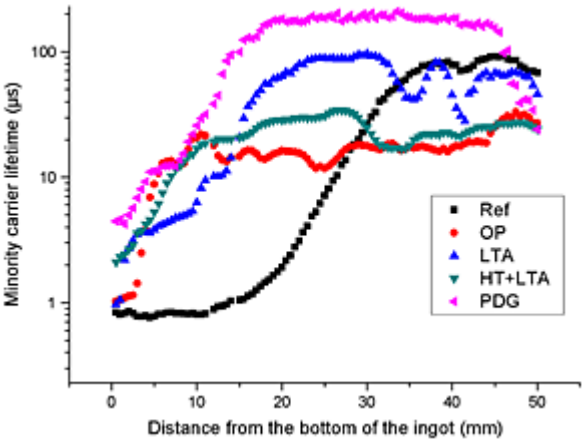

Figure 5. Vertical lifetime scans in the center of vertical wafers subject to different treatments. Labels are similar to those in Figure 4.

High temperature pre-anneal before LTA (labeled HT + LTA) dissolves too much iron close to the bottom (<5 mm), giving poor lifetime there. However, this process gives better lifetime than the LTA in the rest of the Red Zone (5–15mm); this is probably due to an enhanced precipitation of iron caused by high supersaturation after dissolving some iron related precipitates.

The results of linescans of lifetime are shown in Figure 5. The lifetime of the reference wafer varies from below 2 µs in the Red Zone to about 70 µs in the top of the wafer, that is, the center of the ingot. The LTA treatment can clearly improve lifetime in the Red Zone, but interestingly the wafers with OP and HT + LTA treatments can improve lifetime even more between 5 to 15 mm. The lifetime is comparable with the PDG wafer in this area where up to 20 µs was reached.

We can see that The LTA treatment improves lifetime in areas where lifetime is initially low, that is, where iron contamination level is high. Due to high iron concentration, there are already as-grown iron precipitates that act as gettering sites and thereby improve lifetime by reducing interstitial iron concentration in that area. The center part remains unaffected because the lifetime is not limited there by iron.

It is clear that these results indicate that (i) oxide precipitates can have a positive role as sinks for metal impurities but also are among the defects limiting lifetime in the bottom zone and (ii) high temperature pre-anneal enhances internal gettering of iron in the bottom Red Zone.

It is important to mention that the lifetime values in Figure 5 would not be representative of the actual lifetime of the horizontal wafers located at a given position because of the difference in grains orientation between vertical and horizontal wafers. Therefore, it is important to investigate the effect of pre-annealing on internal gettering of horizontal sister wafers taken from the bottom Red Zone of the ingot as shown in Table 1.

3.2.2 Horizontal wafers—the effect of high temperature pre-anneal

The effect of the pre-annealing temperature at (950, 1020, and 1100 °C) before low temperature annealing at 550 °C for 2 h was investigated on the wafers H22, H23, and H24, respectively. The resulted average lifetime and interstitial iron concentration are shown in Figure 6.

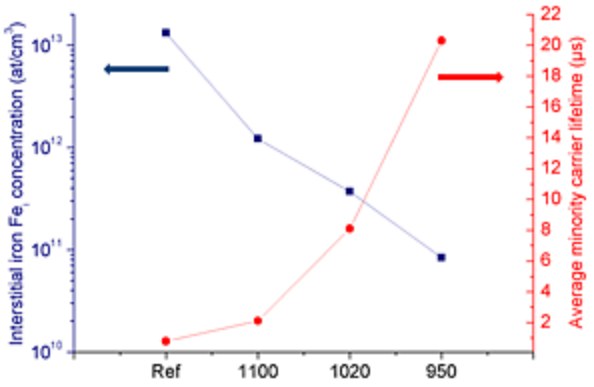

Figure 6. Average lifetime and interstitial iron concentration in wafers H22, H23, H24, and H27 as function of the pre-annealing temperature prior to a low temperature annealing at 550 °C for 2 h H27: as-cut reference wafer H22: pre-annealing at 950 °C for 1 h and LTA at 550 °C for 2 h H21: extended LTA at 550 °C 4 h.

The lifetime increases from below 1 µs in the as-grown wafer to 20.3 µs in the wafer H22 subjected to pre-annealing at 950 °C for 1 h prior to LTA with a reduction of interstitial iron from above 1.32×10^{13} at/cm^3 to 8.4×10^{10} at/cm^3. Lower lifetimes are obtained by increasing the pre-annealing temperature with a higher remaining iron concentration. The interstitial iron concentration increasing is apparently because of the dissolution of metal precipitates at high temperatures.

An extended low temperature annealing at 550 °C for 4 h was performed on the wafer H21, giving an average lifetime of 16.6 µs and an average concentration of interstitial iron of 1.02×10^{11} at/cm^3 was measured. This confirms previous observations with vertical wafers that in some cases the internal gettering of iron and 'background' lifetime can be enhanced by high temperature pre-annealing.

Figure 7 presents the photoluminescence images of the reference wafer (H27), the wafer subject to the extended annealing (H21) and the wafer (H22) pre-annealed at 950 °C for 1 h followed by LTA. The photoluminescence (PL) intensity is clearly enhanced in both H21 and H22 wafers. Importantly, the PL intensity of grain boundaries was higher than the background in the reference wafer and became lower after both internal gettering processes of H21 and H22; this confirms that metal impurities getter effectively to grain boundaries after internal gettering.

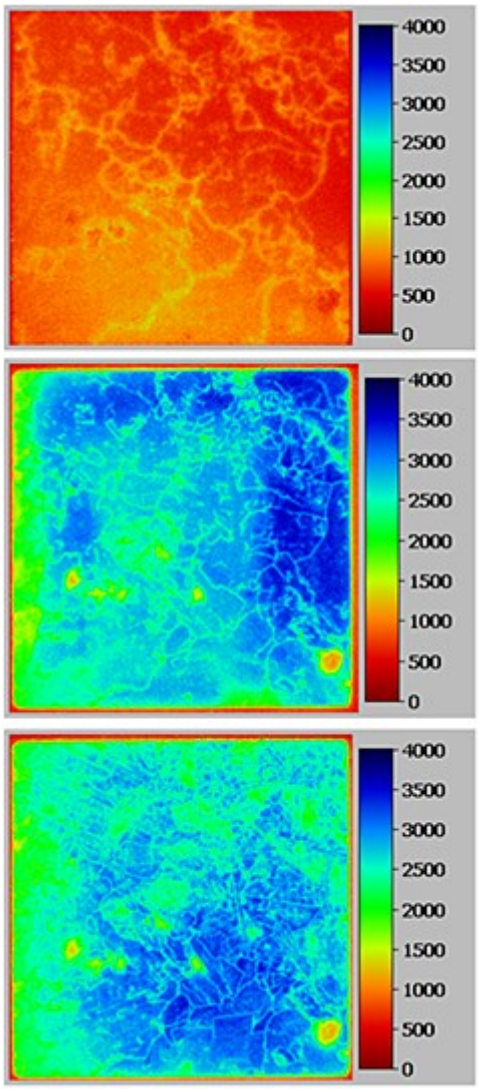

Figure 7. Photoluminescence images of the wafers H27 (top) H22 (middle) and H21 (bottom) such as: H27, as-cut reference wafer; H22, pre-annealing at 950 °C for 1 h and LTA at 550 °C for 2 h; and H21, extended LTA at 550 °C 4 h.

3.3 Internal gettering followed by external gettering

To investigate the overall effect of internal gettering to a standard solar cell process, two sister wafers (H25 and H26) were subject to PDG; H26 had an internal gettering process prior the phosphorous gettering unlike H25 as illustrated in Table 1.

As shown in Figure 8, there is a little enhancement of the lifetime and lesser reduction of interstitial iron on the wafer H26 (subject to LTA + PDG) compared with the wafer H25 (subject to PDG only). The poorer iron reduction is likely caused by the dissolution of unstable precipitates formed

by internal gettering. Moreover, the background lifetime improvement is much smaller after 1020 °C temperature preanneal step. An optimization of the phosphorous diffusion time and temperature as well as internal gettering annealing parameters is needed to enhance the improvement of the material because of combined effect of internal and external gettering. Moreover, the stability of precipitates formed by internal gettering is an important issue for further investigations.

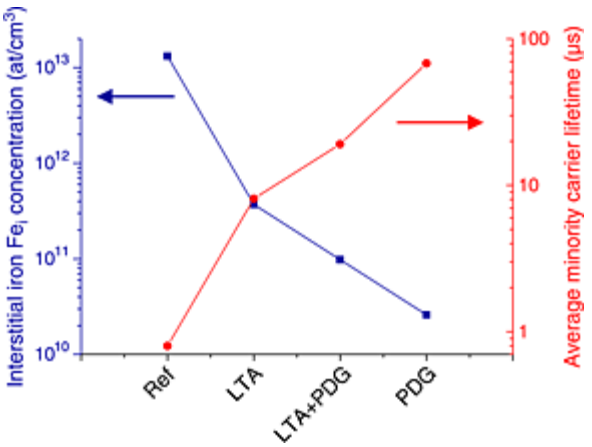

Figure 8. Average minority carrier lifetime and interstitial iron concentration on wafers H23, H25, H26, and H27 subject to different processes.

4 CONCLUSIONS

The main conclusions drawn from this work can be summarized as follows:

- Significant reduction of the bottom Red Zone of mc-Si ingot can be reached. Both internal gettering by nucleating oxide precipitates and by low temperature annealing showed considerable effect on the lifetime of the material from the mentioned area.
- Oxide precipitates could play both beneficial and detrimental roles on the performance of the material. On one hand, they could act as precipitation sites for dissolved metals and on the other hand, they affect the lifetime of the material especially in the bottom part of the ingot because of their high recombination activity.
- High temperature preanneal enhances internal gettering of iron in some part of the bottom Red Zone. The best improvement was reported for a pre-annealing at 950°C for 1 h followed by a low temperature annealing at 550°C for 2 h where the average lifetime has improved from below 1 µs to above 20 µs.
- The complete process mentioned in the last point takes about 6 h including heating, cooling, and idle times. However, the duration of the anneal is greatly reduced if this treatment is included in the cooling of the ingot.
- Phosphorous gettering does not enhance significantly the performance of a wafer internally gettered. The stability of precipitates formed by internal gettering at high temperature is crucial and need further investigations.

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