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Author(s): Feshchenko, A. V. & Koski, J. V. & Pekola, Jukka
Title: Experimental realization of a Coulomb blockade refrigerator
Year: 2014
Version: Final published version

Please cite the original version:

Feshchenko, A. V. & Koski, J. V. & Pekola, Jukka. 2014. Experimental realization of a Coulomb blockade refrigerator. *Physical Review B*. Volume 90, Issue 20. P. 201407/1-5. ISSN 1098-0121 (printed). DOI: 10.1103/physrevb.90.201407.

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Experimental realization of a Coulomb blockade refrigerator

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(Received 16 September 2014; revised manuscript received 15 October 2014; published 24 November 2014)

We present an experimental realization of a Coulomb blockade refrigerator (CBR) based on a single-electron transistor (SET). In the present structure, the SET island is interrupted by a superconducting inclusion to permit charge transport while preventing heat flow. At certain values of the bias and gate voltages, the current through the SET cools one of the junctions. The measurements follow the theoretical model down to ~ 80 mK, which was the base temperature of the current measurements. The observed cooling increases rapidly with decreasing temperature, in agreement with the theory, reaching about a 15 mK drop at the base temperature. The CBR appears as a promising electronic cooler at temperatures well below 100 mK.

DOI: [10.1103/PhysRevB.90.201407](https://doi.org/10.1103/PhysRevB.90.201407)

PACS number(s): 73.23.Hk, 73.40.Rw, 73.50.Lw, 07.20.Mc

Over the past several decades, there has been continuous growth of research dedicated to thermoelectrics in a variety of nanostructures (see Refs. [1–3] and references therein) and, in particular, to electronic microrefrigerators [4,5]. The first quantum dot refrigerator (QDR) for cryogenic temperatures was proposed by Edwards in 1993 [6,7]. In the QDR discrete energy levels of the dot are tuned to cool the electronic Fermi-Dirac distribution of a small reservoir. Soon afterwards, it was demonstrated in a different device [8] that the electrons can be cooled down below the phonon temperature of the lattice. These cooling effects have been observed in several different systems, such as a normal metal-insulator-superconductor (NIS) tunnel junction [8–10] and with improved performance in a related SINIS device with a double junction configuration [11,12]. Also, the exact realization of the above mentioned QDR was shown later in a two-dimensional (2D) electron gas [13]. All of these devices, which are able to cool down on-chip electronic systems to subkelvin temperatures, have potential scientific and commercial applications, especially when size, weight, and ease of operation become important. Examples of possible applications are microbolometers, discussed in Ref. [14]. Recently, several implemented coolers on a Si_3N_4 membrane [15] with a transition-edge sensor for high-resolution x-ray spectroscopy [16] have been demonstrated. These refrigerators work most of the time in the temperature range of 300–100 mK. They perform suboptimally at lower temperatures, due to several reasons, including excess quasiparticle population in a superconductor [17,18], leakage of the junctions [19], and a low electron-electron scattering rate [13].

In this Rapid Communication, we present an experimental realization of a type of cooler that has been recently proposed by some of the authors [20]. A Coulomb blockade refrigerator (CBR) is based on thermal transport through a fully normal single-electron transistor (SET) [21]. The relative temperature drop is expected to increase when the base temperature is lowered, which we verify here experimentally down to 80 mK. This feature makes the CBR suited for temperatures below 100 mK, and could be used in cascade coolers as the last

stage, for example, in combination with a superconducting refrigerator [22]. Here we want to emphasize the most important feature of the CBR. In contrast to the NIS cooler, the operating point can be optimized by the bias and the gate voltages at any given temperature. For example, at a base temperature of 20 mK, which is possible to achieve with standard dilution refrigerators, a temperature of ~ 5 mK can be reached by the CBR assuming no extra heat leaks.

Figure 1 shows the principle of the operation of the cooler. The SET has two NIN tunnel junctions with tunneling resistances $R_{T,k}$ each, formed between two normal metal (N) electrodes separated by a thin insulator (I) layer. We define the order of the junctions as $k = 1, 2$, where 1 is the “cold” junction and 2 is the “hot” junction. Our cooler is biased by voltage V transporting electrons through the SET, first to the island through the “hot” junction, then out of the island through the “cold” junction. When the SET island has n excess electrons, the electrostatic energy is $E = E_c(n - n_g)^2$, where $E_c = e^2/2C_\Sigma$ is the charging energy, and C_Σ is the total capacitance of the SET island. The electrostatic energy is controlled by tuning the gate position $n_g \equiv -C_g V_g/e$, where C_g and V_g are the gate capacitance and voltage, respectively. For simplicity, we define the two extreme gate values that will be used later: (i) gate closed ($n_g = 0$) and (ii) gate open position ($n_g = 0.5$).

In this experiment, we focus on the low-temperature regime, where the number of excess electrons on the island is restricted to $n = 0$ or 1. An electron that tunnels into the island through junction 2 changes n from 0 to 1 with an energy cost $\Delta E_2 = eV/2 + E_c(1 - 2n_g)$. Similarly, an electron that tunnels out of the island through junction 1 changes n from 1 to 0 for an energy cost $\Delta E_1 = eV/2 - E_c(1 - 2n_g)$. The tunneling electrons distribute the energy evenly to their respective heat baths formed by the junction electrodes with typically about 10^9 free electrons in each. The energy ΔE_2 is added to the heat bath of junction 2 at a temperature T_2 , heating that junction, while the energy ΔE_1 is removed from the junction 1 heat bath at a temperature T_1 , cooling that junction. At the optimum point of n_g and V , where $\Delta E_1 = 2k_B T_1$, the cooling power of the junction 1 is given by [20]

$$\dot{Q}_{\text{opt}} \simeq 0.31 \frac{(k_B T_1)^2}{e^2 R_{T,1}}. \quad (1)$$

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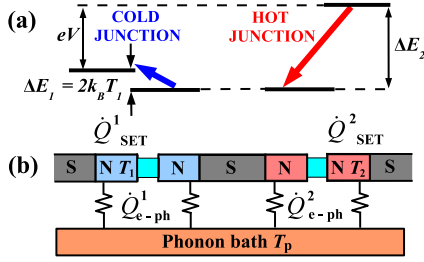


FIG. 1. (Color online) Principle of the operation of the cooler. (a) Schematic of the energy levels of the device at its operation point. (b) Thermal scheme of the structure.

Next we consider the conditions to observe a temperature drop in the CBR. As presented in Fig. 1(b), substrate phonons exchange heat with electrons via electron-phonon coupling $\dot{Q}_{e-ph}^k = \Sigma \Omega_k (T_k^5 - T_p^5)$, where Σ is a constant specific to the electrode material, Ω_k is the volume of that electrode, T_k is the temperature of the electrons, and T_p is the temperature of the phonon bath. Since \dot{Q}_{e-ph}^k is proportional to the electrode volume, the CBR junction electrodes need to be small, as well as thermally insulated to prevent heat leaks from outside and between each other, as indicated in Fig. 1(b) by the S parts. Finally one needs temperature probes to measure T_1 and T_2 . To realize the CBR, we make use of several different types of high-quality Al junctions, all contacting Cu, compatible with cofabrication of other metallic structures [15,16,22].

In the following, we describe the present realization of the proof-of-concept CBR that is shown in a scanning electron micrograph (SEM) in Figs. 2(a) and 2(b). The device is made by electron beam lithography and a three-angle shadow evaporation technique [23]. First, a 20 nm layer of Al forms

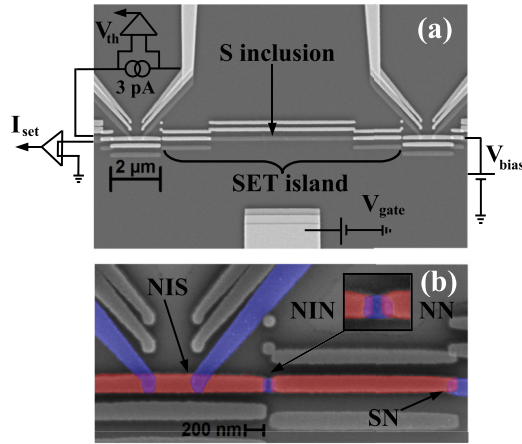


FIG. 2. (Color online) (a) SEM image of the device, shown together with a schematic of the experimental setup, where the SET island consists of two normal metal islands with a superconducting inclusion in between. (b) Closeup SEM image shows the left part of the SET that is connected to the cooled island through the Al “dot” (see text for more details). Zoom into the Al “dot” with NIN and clean NN contacts is shown in the inset. In the main panel, the NIS probes used to monitor the temperature of the cooled island are highlighted. All normal metal parts are colored red, while superconductors are shown in blue.

the superconducting inclusion, outer leads, fingers for the NIS temperature probes, and Al “dots” [see the inset in Fig. 2(b)]. Next, a 25 nm layer of Cu, evaporated at a different angle, creates normal metal parts that form clean contacts to the superconducting inclusion from one side and to Al “dots” on the other side. Short Cu intermediate leads that are connected to the outer leads are formed at this step as well. *In situ* thermal oxidation followed after the second metal evaporation to form a thin Al_2O_3 layer over Al to provide the insulator for tunnel junctions. In the last evaporation step, 25 nm thick Cu electrodes form tunnel junctions for the SET, for the NIS probes, and connections to the intermediate leads. Connections to the outer leads are assumed to be transparent junctions between two Cu layers, which are, however, slightly oxidized in between. Underneath all of the leads, except for the gate electrode, we use a ground plane made out of 50 nm of copper covered by 50 nm of AlO_x . Here, the ground plane serves the purpose of reducing the leakage current in the subgap region of the NIS thermometer [24,25], and suppresses voltage noise in general.

The SET junctions are made by the laterally proximized tunnel junction technique [26], where the small Al “dots” (100 nm × 100 nm) are in direct contact with a bigger volume of normal metal Cu that suppresses the superconductivity by the inverse proximity effect [27–29]. The inset in Fig. 2(b) shows the lateral junction with an Al “dot” (colored blue) that is connected on the left side by the NIN tunnel junction to the island to be cooled, and to the SET island through a clean NN contact on the right side. Two fully normal NIN tunnel junctions of the SET were made intentionally unequal by lithography. Junction 1 with low resistance increases the cooling power at the optimal bias point [see Eq. (1)], and at the same time junction 2 is more resistive, decreasing cotunneling, which will be described later in the text. The SET island splits into three parts, where the superconducting section of 5 μm length in the middle is surrounded by shorter normal metal islands that are 2 μm long each, as indicated in Fig. 2(a). We have chosen this particular length of the superconductor for two reasons. First, to avoid the inverse proximity effect, the length of the inclusion is much longer than the coherence length for Al that is typically around 200 nm at 100 mK. Thus the superconductor provides good thermal insulation [29] while maintaining an electrical connection through the SET. Second, to keep the total charging energy of the SET island in the range of our interest, around 1 K, it cannot be longer than a few μm .

Next, we present the measurement data that characterize the SET and the NIS temperature probes. We conduct our experiments in a ^3He - ^4He dilution refrigerator at a bath temperature T_{bath} . In Fig. 3(a), the measured current voltage characteristic (I - V) of the SET is shown as blue dots. The dots appear as vertical lines due to the gate voltage sweep recorded at each bias voltage point. The slope in the gate open position is constant around zero bias, demonstrating the absence of a superconducting gap, meaning that the SET junction electrodes are normal. The theoretical model used in the inset and in the main panel is based on the theory of sequential single-electron tunneling [21]. The fit to the I - V curve gives values $E_c = 78 \mu\text{eV}$ for the charging energy, and the tunneling resistances are $R_{T,1} = 103 \text{ k}\Omega$ and $R_{T,2} = 448 \text{ k}\Omega$.

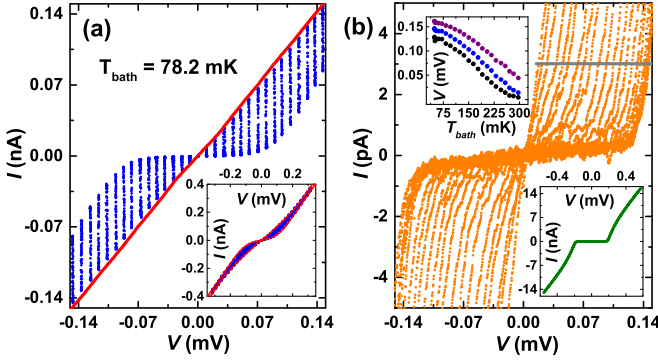


FIG. 3. (Color online) (a) Closeup of the measured I - V of the SET shown as blue dots. The solid red line is the fit for the gate open case. The inset shows the full I - V of the SET at ~ 207 mK (blue dots) together with a full theory fit (solid red line) for both gate open and gate closed positions, utilizing the same R_T and E_c as in the main panel. (b) I - V curves (orange dots) of one of the probing NIS junctions at various temperatures between 50 and 300 mK. The solid horizontal gray line indicates the 3 pA current bias of the NIS probe (see text for details). The lower inset shows the measured full I - V at a bath temperature of ~ 48 mK. The upper inset shows the voltage calibration obtained from the I - V curves in the main panel for bias currents of 1, 3, and 14 pA (shown as black, blue, and purple dots from bottom to top, respectively).

In Fig. 3(b), we characterize the NIS thermometer probe by measuring the temperature sweep of its I - V . The curves are well separated for different temperatures. The solid gray line in Fig. 3(b) indicates 3 pA, which we have chosen as a biasing current for the temperature probe. This value is in the temperature sensitive region, not influenced by the Andreev current leakage [30–32] that appears as a constant slope at low bias values in Fig. 3(b).

The experimental setup to test CBR performance is shown in Fig. 2(a). The voltage bias is applied to the right lead of the SET and at the same time the gate voltage is used to tune the electrostatic potential of the island. At each bias point, the gate voltage is swept over a few gate periods, at constant current bias for temperature probes. The observed cooling depends on the bath temperature as well as on the bias and gate voltages. We define the base temperature $T_{e,0}$ as the electronic temperature observed at the gate closed position, meaning zero current through the SET; here no cooling or heating takes place at the junctions. The temperature traces obtained by the NIS thermometer at different bath temperatures are presented in Fig. 4. The measured thermal voltages across the NIS probes and the outer leads are converted into temperature with a calibration [8,14,33,34] [see the upper inset in Fig. 3(b)] with respect to the bath temperature of the dilution refrigerator. The measurement data shown in the left column [Figs. 4(a)–4(c)] and in the right column [Figs. 4(d)–4(f)] were obtained at base temperatures of 111 and 83 mK, respectively. Both columns from top to bottom present the temperature traces of junction 1 [shown in Figs. 4(a) and 4(d)] and of junction 2 [shown in Figs. 4(b) and 4(e)], and the current through the SET [shown in Figs. 4(c) and 4(f)] during the gate voltage sweep. The cooling ΔT appears as a dip below $T_{e,0}$, indicated by the dashed lines, and the signal above the line indicates heating. The solid red

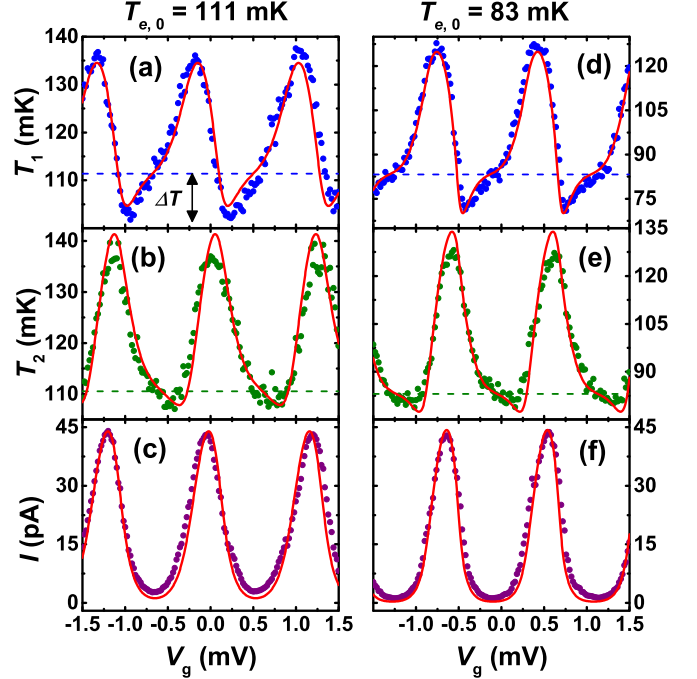


FIG. 4. (Color online) Top panels: Temperature T_1 over a few gate periods [shown as blue dots in (a) and (d)]. The solid red lines correspond to the theoretical prediction, where the voltage of the SET has a value of $45 \mu\text{eV}$. The base electronic temperatures $T_{e,0}$ are shown as blue dashed lines for data. The two middle panels, (b) and (e), show T_2 (green dots) together with the theory (solid red lines), and the base temperatures marked as dashed lines. The two lowest panels, (c) and (f), present the gate dependent current I through the SET, measured simultaneously as the temperatures T_1 and T_2 .

lines shown in all the panels present the theoretical model to be described. We measured similar temperature traces at various bath temperatures. At each bath temperature, the drop ΔT was averaged over repeated gate sweeps and the standard deviation was calculated. The result is shown in Fig. 5(a) for three different voltage bias values indicated by orange circles, blue squares, and red triangles. The error bars are $\pm 2\sigma$ confidence intervals estimated from the observed scatter.

Next, we describe the theoretical model presented by the lines in Figs. 4 and 5. The electron temperatures T_1 and T_2 are obtained as a solution to the steady state heat balance equation $\dot{Q}_{\text{SET}}^k + \dot{Q}_{e\text{-ph}}^k = 0$ for both junctions $k = 1, 2$, where \dot{Q}_{SET}^k is the heat flow through the junctions based on a sequential single-electron tunneling model and cotunneling [20]. We estimate that in the present structure at $T_{e,0} = 83$ mK the temperature drop is reduced by 11% due to cotunneling. We assume $T_p = T_{e,0}$ in the expression of electron-phonon coupling $\dot{Q}_{e\text{-ph}}^k$. The volume of the cooled island is approximately $\Omega \simeq 5 \times 10^{-21} \text{ m}^3$. We obtain a fit $\Sigma = 4 \times 10^9 \text{ W K}^{-5} \text{ m}^{-3}$ by assuming that at the gate open position the heat flow through the junctions is equal to Joule heating, $\dot{Q}_{\text{SET}}^k = IV/4$, distributed equally among the four electrodes of the SET.

The observed cooling increases rapidly, in agreement with the theory towards low temperatures, giving a maximum value of $\Delta T = 15 \pm 1.15 \text{ mK}$ for a bias voltage of $60 \mu\text{eV}$ at

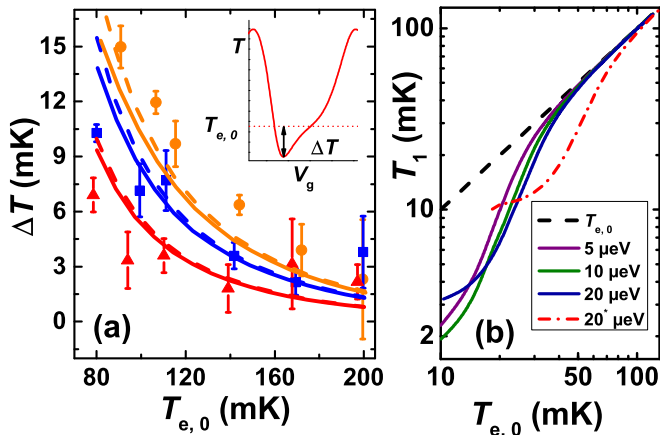


FIG. 5. (Color online) (a) Observed cooling ΔT (see the inset for definition) for three different voltage bias values over the temperature range from 200 down to 80 mK. The data sets obtained by averaging over all realizations within a $\pm 5 \mu\text{eV}$ range are shown for mean bias values of $60 \mu\text{eV}$ (orange circles), $40 \mu\text{eV}$ (blue squares), and $20 \mu\text{eV}$ (red triangles), from top to bottom. The error bars are calculated as a standard deviation for the data. The theoretical predictions of ΔT for the three voltage bias values (60 , 40 , and $20 \mu\text{eV}$) are shown as orange, blue, and red solid lines, respectively. The dashed lines show the theoretical prediction without cotunneling. (b) The theoretical predictions of T_1 for the three voltage bias values, as indicated in the legend, in the temperature range of 10–130 mK, are shown as solid lines. The dashed-dotted red line indicated as $20^* \mu\text{eV}$ is the same as in (a), where in the model we used values of $R_{T,k}$ obtained from the experiment. The solid purple, dark green, and dark blue lines (from top to bottom at $T_{e,0} > 20 \text{ mK}$) are predictions for a CBR with tunneling resistances ten times higher than those in the present measurements.

$T_{e,0} = 90 \text{ mK}$. The electronic temperature saturation at 80 mK can be explained by the NIS thermometer losing its sensitivity [see the upper inset in Fig. 3(b)]. Another contribution is the heating due to radiation from the hotter electromagnetic

environment [24,25,35]. These problems can be resolved in the future by improving filtering and thermometry. Increased resistance of the NIS junctions would reduce the magnitude of the Andreev current and the heat it produces, which is significant towards low temperatures [31]. Alternative thermometry can be used as well. For example, a proximity Josephson junction has a temperature dependent critical current [31,36,37] and essentially zero dissipation, and it could be adjusted to a specific temperature interval.

Finally, in Fig. 5(b) we show the theoretical prediction within the model above, including the effect of cotunneling, but with tunneling resistances that are ten times higher than in the present experiment. As a reference, we show the dashed-dotted red line ($20^* \mu\text{eV}$), which is identical to the one that is shown in Fig. 5(a) as a red curve, with $R_{T,k}$ values obtained from the experiment. To reach lower electronic temperatures in the present configuration, one can thus benefit from higher tunneling resistances of the junctions and lower bias voltages. The higher tunneling resistances thus would decrease the cooling power [see Eq. (1)], but on the other hand, cooling required to reach lower electronic temperatures is significantly smaller as well.

In conclusion, we have shown the experimental realization and demonstrated the proof-of-concept performance of a Coulomb blockade refrigerator. The present realization of the device measured down to 80 mK demonstrates about a 15% temperature drop which increases rapidly towards lower temperatures.

We acknowledge the availability of the facilities and technical support by Otaniemi research infrastructure for Micro and Nanotechnologies (OMN). We acknowledge financial support from the European Community FP7 Marie Curie Initial Training Networks Action (ITN) Q-NET 264034 and INFERNOS grant (Project No. 308850), and the Academy of Finland through its LTQ CoE grant (Project No. 250280) and Väisälä Foundation. We thank D. V. Averin and I. M. Khaymovich for useful discussions.

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