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High-*k* GaAs metal insulator semiconductor capacitors passivated by *ex-situ* plasma-enhanced atomic layer deposited AlN for Fermi-level unpinning

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This paper examines the utilization of plasma-enhanced atomic layer deposition grown AlN in the fabrication of a high-*k* insulator layer on GaAs. It is shown that high-*k* GaAs MIS capacitors with an unpinned Fermi level can be fabricated utilizing a thin *ex-situ* deposited AlN passivation layer. The illumination and temperature induced changes in the inversion side capacitance, and the maximum band bending of 1.2 eV indicates that the MIS capacitor reaches inversion. Removal of surface oxide is not required in contrast to many common *ex-situ* approaches. © *2012 American Institute of Physics*. [doi:10.1063/1.3687199]

As the scaling down of silicon metal-oxide-semiconductor field-effect transistors (MOSFET) progresses, the fundamental limitations of silicon integrated circuits (ICs) are approaching. Utilization of high-mobility III-V compound semiconductors in IC technology is one proposed method to continue to improve the performance. GaAs has six times higher electron mobility than silicon and is monolithically integrable to high hole-mobility germanium. However, at the moment, there is no insulator material for GaAs which would be even closely comparable to the Si/SiO_2 material combination. As a result, industrially feasible realization of GaAs MOSFETs has not yet been demonstrated.

The most important requirements for the insulator layer are thermal stability, high dielectric constant with sufficient band offsets, the formation of a high-quality interface with a low interface trap density, and an unpinned Fermi level. Fermi level pinning is commonly explained in the literature by formation of unpassivated dangling bonds which exist on the GaAs surface after formation of native oxide. Therefore, the most common approaches developed to overcome this problem consist of *in-situ* passivation or *in-situ* deposition of the insulator material. For instance, inversion has been demonstrated in MIS structures fabricated from *in-situ* deposited Ga_2O_3.[1,2] However, the drawback of this approach is that it requires a multichamber MBE technique which is unsuitable for high-volume manufacturing. Recently, the most discussed approach has been the utilization of crystalline or amorphous silicon interfacial control layers as an *in-situ* passivation layer.[3–6] One benefit of this approach is that it enables the integration of the high-*k* insulators on the passivation layer. In contrast to these *in-situ* approaches, it has also recently been discovered that it is not necessary to seal the GaAs surface in ultra-high vacuum conditions to unpin the Fermi level. For instance, GaAs/insulator interfaces with an unpinned Fermi level have been demonstrated

from *ex-situ* deposited Al_2O_3[7] and Si_3N_4[8] dielectrics. However, an insulator layer with interface trap densities of the order of 10^9- low 10^{10} cm^{-2} eV^{-1} has not yet been demonstrated. Therefore, there is still a constant search for new materials to fabricate even better GaAs/insulator interfaces to enhance the properties of already existing solutions.

Surface passivation of GaAs by plasma-enhanced atomic layer deposited AlN (PEALD AlN) has recently been demonstrated optically.[9] PEALD AlN is an interesting *ex-situ* candidate for passivation of GaAs surfaces for MIS structures as it possesses a similar surface self-cleaning effect as an *ex-situ* deposited ALD Al_2O_3 dielectric layer.[7] In addition to this, PEALD AlN is amorphous at the deposition temperature used in this study providing a suitable foundation for the fabrication of a high-*k* HfO_2 dielectric layer. Moreover, PEALD AlN may be suitable for passivation of future multigate devices due to conformal deposition. In contrast to a silicon interfacial control layer approach, AlN has a large band gap of 6 eV which ensures that no surface quantum well is formed from the passivation material as is the case with crystalline silicon.[4] In addition, the effect of AlN on the dynamics of the charge carriers should be smaller than that of amorphous silicon which has a band gap energy comparable to GaAs. Furthermore, the thermal expansion coefficient of AlN is also closer to the thermal expansion coefficient of GaAs than that of silicon is to GaAs.

In this letter, we show that PEALD AlN can be used as an *ex-situ* deposited passivation layer to fabricate high-*k* GaAs MIS capacitors. Capacitance-voltage (CV) and current-voltage (IV) measurement results imply that the Fermi level is unpinned. The illumination and temperature induced changes in the inversion side capacitance, and the maximum band bending of 1.2 eV indicates that the MIS capacitor reaches inversion.

GaAs MIS structures were fabricated on a 1 μm thick p-GaAs layer grown on p+ GaAs substrates by metalorganic

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vapor phase epitaxy. The doping concentration of $3 \times 10^{17}/cm^3$ of the p-GaAs layer was determined by a Hall measurement. The insulator layer of the MIS structure was comprised of a 2 nm thick PEALD AlN passivation layer deposited using the process described in Ref. 10 and a 35 nm thick HfO_2 layer. HfO_2 was grown by thermal ALD at 350 °C using $HfCl_4$ and water precursors. A combined capacitance of $0.32 \mu F/cm^2$ was determined from equivalent metal-insulator-metal structures for the insulator stack corresponding to an equivalent oxide thickness (EOT) of 10.7 nm for silicon dioxide. AlN passivated MIS components with smaller EOT were also fabricated but to show the Fermi level unpinning, we present the results of the component with a thick insulator layer to minimize the effects of leakage current. In addition to the AlN passivated sample, a 35 nm thick HfO_2 layer was grown directly on p-GaAs without the passivation layer for reference. Circular Au metal gates with surface area of 4.3 mm^2 were fabricated by thermal evaporation. After the evaporation, MIS structures were placed on a copper coin and the backside ohmic contact was formed using liquid indium-gallium. High frequency CV characterization of the MIS structures was carried out at the frequency of 100 kHz with the sweep rate of 100 mV/s unless otherwise mentioned. In some of the measurements, the microscope lamp was used as light source to enhance the generation of the minority carriers. In addition, a resistive heater was used in some of the measurements for the same purpose. All the measurement temperatures mentioned in this paper are heater temperatures. The measured admittance values were corrected with formulas obtained from equivalent circuit models.[11,12] In addition, IV measurements were performed to gather information about the leakage currents of the MIS components. In order to study the Fermi level unpinning a high-frequency CV curve was simulated with a procedure presented by Engel-Herbert *et al.*[12,13]

Fig. 1 shows the high frequency CV curves of unpassivated and AlN passivated GaAs MIS components measured at room temperature. Three main observations can be made. First, AlN passivation enables a larger capacitance change with a reduced stretch out. The stretch out depends on the density of the trap states within the band gap and the reduced stretch out implies that the AlN passivation enhances the interface quality. Second, light affects the behavior of the inversion side capacitance of the AlN passivated component, whereas it does not affect the operation of the unpassivated MIS component. Third, the inversion side capacitance of a CV curve of the AlN passivated component depends on the sweep rate even for very low sweep rates and under illumination. This implies that the lifetimes of the trap states and valence band states are very long and that the measured CV curves are not steady state curves. The resulting delayed response is expected to explain the increase of the measured capacitance under illumination in the bias range from 3 V to 4 V.

The effect of light in the CV curves of Fig. 1 originates from the deep depletion of the structure.[8,14] In deep depletion, the minority carrier system is not in thermal equilibrium due to slow thermal generation of minority carriers. This allows band bending to increase beyond values that can normally be reached in a system in equilibrium and results in a smaller inversion side capacitance. It has been shown that the time constant for the thermal generation is of the order of hundreds of seconds in GaAs at room temperature which makes the formation of inversion in the dark practically impossible.[14,15] When the MIS component is illuminated, radiative generation enhances the formation of minority carriers reducing the band bending closer to the steady state value and, thereby, causing the larger measured capacitance values for positive gate biases. However, radiative generation is not sufficient for the formation of a steady state curve as was concluded earlier. It is important to note that the larger variation in the measured capacitance or the reduced stretch out of the CV curve implies smaller trap density but does not directly indicate an unpinned Fermi level. The indication of an unpinned Fermi level, however, is obtained as the light obstructs the occurrence of deep depletion. Light can generate minority carriers and contribute to minority carrier population but does not significantly affect the trap states. The extent of deep depletion and the capacitance is, therefore, affected by light in inversion. Thus, the observation that light affects the capacitance of the passivated structure but not the unpassivated structure, therefore, shows that the passivated structure reaches inversion whereas the unpassivated does not. In addition, note that in reality, light generates minority carriers only outside the opaque 400-nm-thick Au gates from where the carriers diffuse to under the gate.

The inset of Fig. 1 shows the leakage current through the AlN passivated structure with EOT of 10.7 nm as a function of the applied voltage. The leakage DC current is less than 100 nA/cm^2 with typical bias voltages used in the CV measurements. In addition, the electric breakdown voltage of the AlN passivated component is larger than 10 V providing an electric breakdown field larger than 3 MV/cm for the insulator stack. This implies that the quality of the insulator layer of the MIS component is high. Steady state deep depletion has been reported as a possible mechanism enabling the capacitance of the MIS component with a pinned Fermi level to change with gate bias.[14] Typically, steady state deep depletion is caused by insufficient energy band offsets or tunneling through a thin insulator layer. Due to the high quality of the insulator, it is unlikely that the capacitance
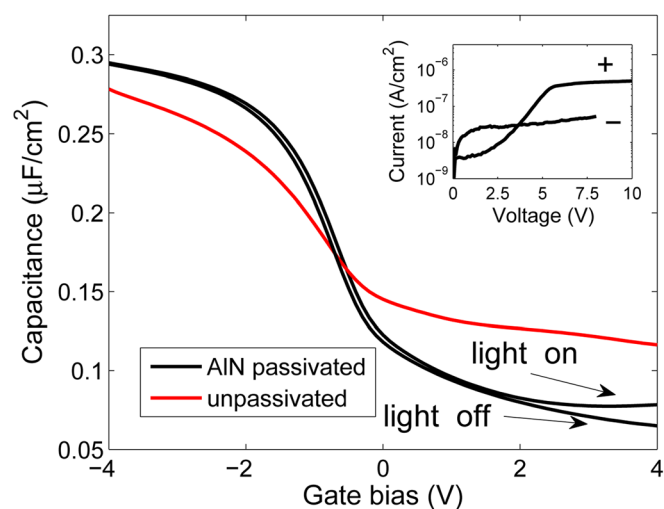

FIG. 1. (Color online) CV curves of the AlN passivated and the unpassivated GaAs MIS structures. The inset shows the leakage current of the AlN passivated component. Plus (+) and minus (−) signs denote the sign of the gate bias.

change with gate bias in AlN passivated component is affected by the increased leakage current. The leakage current in unpassivated sample is significantly larger (not shown). The increased leakage may originate from crystallinity of GaAs. It has been observed that HfO_2 layer, when deposited on crystalline substrate by ALD, can have polycrystalline crystal structure which degrades the electrical properties of HfO_2 layer.[16] As a result, the observed change in capacitance with voltage in unpassivated component may be affected by the increased leakage.

The unpinning of the Fermi level at the GaAs/AlN interface was also examined by estimating the band bending at the interface. A steady state CV curve was measured at the temperature of 75 °C with a sweep rate of 0.2 V/min. Fig. 2 shows the band bending—gate bias relationship obtained by comparing the measured and simulated CV curves which are presented in the inset. The maximum band bending of the AlN passivated component is between −0.1 eV and 1.2 eV in the gate bias range of −2 V–3 V. Inaccuracies in the doping concentration may create the difference between the estimated band bending of 1.2 eV and the simulated band bending of 1.4 eV. Note that the difference is within the error margin of our Hall measurement setup. This close agreement between the simulations and measurement along with the estimated band bending of 1.2 eV, however, gives further support for the conclusion that the AlN passivation enables the Fermi level unpinning in the interface.

Frequency dependent CV measurements were performed to AlN passivated MIS component to characterize the interface properties. It has been shown that frequency dependent CV curves of GaAs MIS structures should also be measured at higher temperatures to enable the slow midgap trap states to contribute to the frequency dependent CV measurements.[17] Fig. 3 displays the frequency dependent CV curves of AlN passivated sample measured at room temperature and at the temperature of 100 °C. At 100 °C, the capacitance saturates in the inversion side indicating that deep depletion is not occurring. This is caused by the increased temperature which increases the generation rate of the minority carriers

FIG. 3. (Color online) Multifrequency CV curves of the AlN passivated MIS structures measured (a) at room temperature and (b) at the temperature of 100 °C.

just like illumination. In contrast at room temperature, the capacitance does not saturate due to slow minority carrier generation. This temperature dependent behaviour gives further support for the Fermi level unpinning. Furthermore, frequency dispersion, measured at the gate bias of −3 V in the frequency range from 1 kHz to 100 kHz, increases from 2.4% to 4% when the MIS structure is heated. In addition, the flat band voltage shift of 0.1 V/decade at room temperature increases to 0.2 V/decade at the temperature of 100 °C. This is caused by the increased temperature which enables the slower interface traps closer to midgap also to contribute to frequency dependent CV curves.

To examine the interface trap distribution quantitatively, we have applied the Terman method to the band bending—gate bias relationship. Fig. 4 shows the interface trap distribution. The method results in an interface trap density minimum of the order of low 10^{11} $cm^{-2}eV^{-1}$. In addition, no interface traps are observed at the energy range of 0.4 eV–0.6 eV above the valence band. We expect that this is caused by long response time of the mid gap interface traps. This may make the interface traps at this energy range unable to respond to the gate bias sweep even when the MIS structure is heated. In contrast, the interface traps close to the valence band are expected to respond to the AC signal due to increased temperature. The basic assumption of the Terman method is that interface traps follow the gate bias
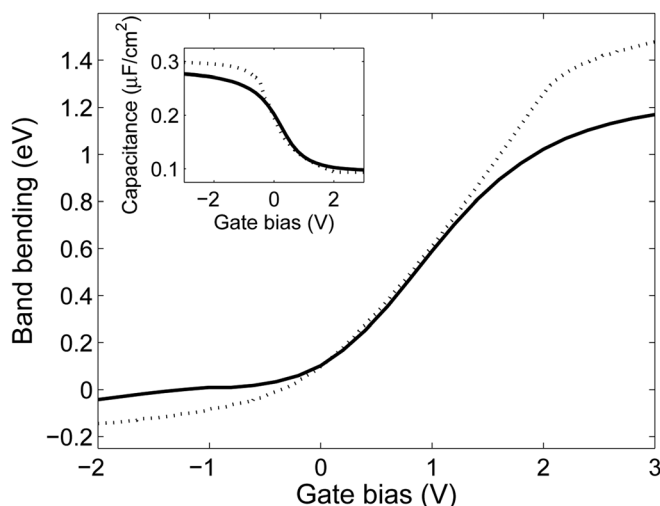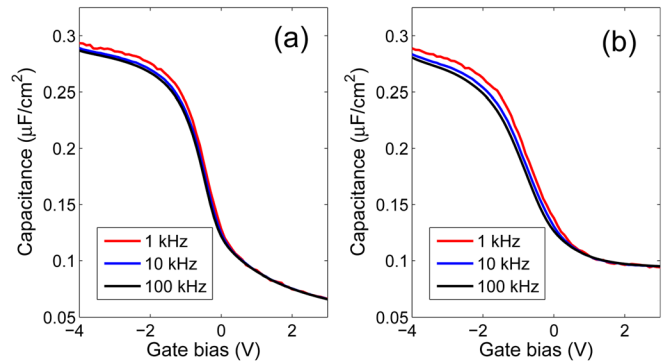

FIG. 2. Band bending—gate bias relationship in an AlN passivated GaAs MIS structure is obtained comparing the steady state CV curve and the simulated CV curve (shown in the inset) of the AlN passivated MIS structure.
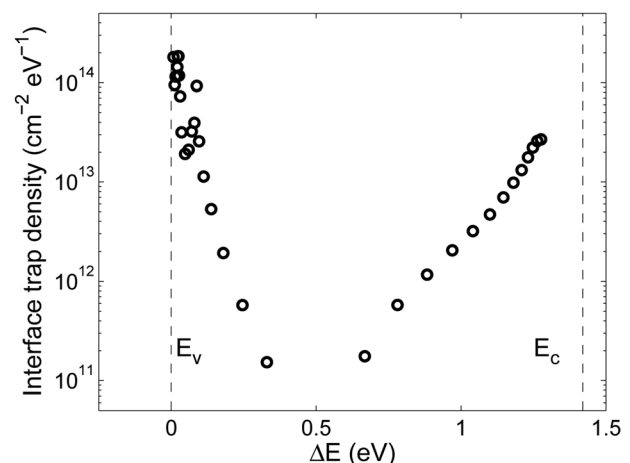

FIG. 4. Interface trap distribution obtained by Terman method.

but are unable to respond to AC signal due to high measurement frequency. As a result, the accuracy of this estimate is partly challenged and further studies are required to more reliably estimate the interface trap distribution.

In conclusion, it was shown that high-*k* GaAs MIS capacitors can be fabricated with an unpinned Fermi level utilizing a thin *ex-situ* deposited PEALD AlN passivation layer. The illumination and temperature induced changes in the inversion side capacitance, and the maximum band bending of 1.2 eV with a gate bias of 3 V indicates that the AlN passivated MIS capacitor reaches inversion. Hence, PEALD AlN is an interesting candidate for passivation of GaAs surfaces for fabrication of MOS structures.

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