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Reliability and Lifetime Assessment of Through-Silicon Vias Under Thermal Cycling

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ABSTRACT OF THE
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Through-silicon via (TSV) is one of the key technologies for three-dimensional (3D) integrated circuits (ICs). TSVs enable vertical electrical connections between components which greatly reduces interconnection lengths. Regardless of all the promise the technique has shown, there are still major obstacles surrounding reliability and the cost of fabrication of the TSV structure.

The first part of the thesis is a literature survey that focuses on different failure mechanisms of TSVs. In addition, different fabrication and design choices of TSVs are presented with the focus being on their effect on reliability. The experimental part of the thesis presents reliability and lifetime assessment of tapered partially copper-filled blind TSVs under thermal cycling. The reliability test was carried out with nine samples. Six of them had 420 vias and three of them had 1400 vias in a daisy chain structure. Finite element method (FEM) was used to predict the critical failure locations of the TSV structure. Lifetime was predicted by Weibull analysis. The cross-sections of the test samples were prepared by molding, mechanical grinding and polishing and analyzed by scanning electron microscope (SEM).

Electrical measurements showed almost constant resistance increase in the samples before failures were noticed. The first failed sample was noticed after 200 cycles and the last at 4000 cycles. Lifetime of TSVs under thermal cycling was proven to be acceptable with used failure criterion. According to Weibull analysis, about 10 % of the samples with 420 vias will break after 1000 cycles. Sample preparation for imaging was deemed sufficient although the grinding caused artifacts. The simulation results were compared with SEM micrographs. The images showed that the failures were located at the maximum stress areas, identified with FEM simulations, at the bottom of the via. From the SEM images, it was deduced that the defects initiated from the fabrication process and propagated due to maximum localized stress.

Keywords: Through-silicon via, reliability, Weibull analysis, finite element method

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Piin läpivienti -rakenteet ovat keskeisessä osassa kolmiulotteisten integroitujen piirien kehityksessä. Piin läpiviennit mahdollistavat komponenttien vertikaalin yhdistämisen toisiinsa, mikä lyhentää huomattavasti niiden välistä etäisyyttä. Kaikista hyvistä puolista huolimatta tekniikalla on vielä haasteita edessään. Niistä suurimmat liittyvät rakenteen luotettavuuteen ja valmistuskustannuksiin.

Diplomityön kirjallisessa osuudessa keskitytään piin läpivientien erilaisiin vauriomekanismeihin. Sen lisäksi tutkitaan valmistus- ja suunnitteluratkaisujen vaikutusta läpivientien luotettavuuteen. Kokeellisen osan tarkoituksena on osittain kuparitäytettyjen kaventuvien piin läpivientien luotettavuuden ja eliniän määrittäminen termisessä syklaustestissä. Luotettavuustestaus suoritettiin yhdeksällä näytteellä, joista kuudessa oli 420 läpivientiä ja kolmessa 1400 läpivientiä ketjurakenteessa. Elementtimallintamisen avulla määritettiin kriittiset vauriokohdat läpivientirakenteessa ja elinikä määritettiin Weibull-analyysillä. Näytteiden poikkileikkauksien valmistamiseen käytettiin muovaamista, mekaanista hiomista ja kiillotusta ja analysointi suoritettiin pyyhkäisyelektronimikroskoopilla.

Näytteiden resistanssi nousi tasaisesti ennen rikkoutumisten havaitsemista. Ensimmäinen rikkoutuminen huomattiin 200 syklin jälkeen ja viimeinen 4000 syklin kohdalla. Näytteiden luotettavuus osoittautui hyväksi käytetyillä kriteereillä. Weibull-analyysin mukaan 10 % 420 läpiviennin näytteistä rikkoutuu 1000 syklin jälkeen. Karkea arvio voidaan tehdä, että satunnainen läpivienti rikkoutuu 0,024 % todennäköisyydellä 1000 syklin jälkeen. Pyyhkäisyelektronimikroskoopin kuvien perusteella havaittiin, että näytteet rikkoutuivat maksimaalisen rasituksen alueella läpivientien alaosassa. Kuvien perusteella päädyttiin johtopäätökseen, että näytteiden rikkoutumisen aiheuttivat virheet, jotka ovat peräisin valmistusprosessista ja jotka etenivät rakenteessa termisen rasituksen vaikutuksesta.

Avainsanat: Piin läpivienti, luotettavuus, Weibull analyysi, elementtimallintaminen

Preface

The research for this thesis was conducted at the department of Electrical Engineering and Automation in the unit of Electronics Integration and Reliability at Aalto University.

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Symbols and abbreviations

Symbols

A	Area (m^2)
A_c	Constant depending on the wire geometry
α	Coefficient of thermal expansion
β	Shape parameter
c	Atomic concentration ($\frac{\mathrm{mol}}{\mathrm{m^3}}$)
γ	Field acceleration factor
D	Diffusivity ($\frac{\mathrm{m^2}}{\mathrm{s}}$)
E	Electric field ($\frac{N}{C}$)
E_a	Activation energy (J)
E_{BD}	Breakdown field ($\frac{\mathrm{N}}{\mathrm{C}}$)
E_y	Young's modulus (Pa)
e	Electron charge ($1{,}60217657 \times 10^{-19}$ C)
ε	Strain
F	Force (N)
h	Height of the via (m)
η	Scale parameter
I	Current (A)
i	adjusted rank of the failed sample
J	Total atomic flux ($\frac{\mathrm{mol}}{\mathrm{m^2 \cdot s}}$)
J_a	Atomic migration ($\frac{\mathrm{mol}}{\mathrm{m^2 \cdot s}}$)
J_e	Current-induced migration ($\frac{\mathrm{mol}}{\mathrm{m^2 \cdot s}}$)
J_s	Stress-induced migration ($\frac{\mathrm{mol}}{\mathrm{m^2 \cdot s}}$)
J_t	Temperature-induced migration ($\frac{\mathrm{mol}}{\mathrm{m^2 \cdot s}}$)
j	Current density ($\frac{\mathrm{A}}{\mathrm{m^2}}$)
k	Boltzmann constant ($1{,}3806488 \times 10^{-23}\ \frac{\mathrm{J}}{\mathrm{K}}$)
N	sum of failures and suspensions
ν	Poisson ratio
$Q^\star$	Heat of transport (eV)
ρ	Resistivity (Ω·m)
σ_m	Hydrostatic stress ($\frac{\mathrm{N}}{\mathrm{m^2}}$)
σ_x	Normal stress (Pa)
σ_{xy}	Shear stress (Pa)
R	Resistance (Ω)
R_r	Ramp rate

R_0	Reference ramp rate
r	Correlation coefficient
r^2	Coefficient of determination
r_r	Radius (m)
T	Temperature (K)
t	Failure time
t_{bd}	Time to breakdown (h)
t_0	Location parameter
V	Voltage (V)
Z	Effective charge
Ω	Atomic volume ($\frac{\mathrm{cm}^3}{\mathrm{mol}}$)

Abbreviations

AFM	Atomic force microscopy
ALD	Atomic layer deposition
BCB	Benzocyclobutene
BEOL	Back-end-of-line
BSE	Backscatter electron
C_4F_8	Octafluorocyclobutane
CCC	Critical correlation coefficient
CDF	Cumulative distribution function
CF_4	Tetrafluoromethane
CMP	Chemical-mechanical planarization
CTE	Coefficient of thermal expansion
CVD	Chemical vapor deposition
c-t	Capacitance-time
DRIE	Deep reactive-ion etching
EBSD	Electron backscatter diffraction
ELD	Electroless plating
FEA	Finite element analysis
FEM	Finite element method
FEOL	Front-end-of-line
FIB	Focused-ion beam
IC	Integrated circuit
JEDEC	Joint Electron Device Engineering Council
KOZ	Keep-out zone
low-κ	Low dielectric constant
MOS	Metal-oxide-semiconductor
MTTF	Mean time to failure
N_2	Nitrogen
NF_3	Nitrogen trifluoride
PDF	Powder Diffraction File
PDF	Probability density functions
PECVD	Plasma-enhanced chemical vapor deposition

PSI	Phase-shifting interferometry
RDL	Redistribution layer
SEM	Scanning electron microscopy
SF_6/O_2	Sulfur hexafluoride/oxygen
SiN	Silicon nitride
SiO_2	Silicon dioxide
TDDB	Time dependent dielectric breakdown
TEM	Transmission electron microscopy
TGV	Through-glass via
TaN	Tantalum nitride
TiN	Titanium nitride
TSV	Through-silicon via
VSI	vertical scanning interferometry
XRD	X-ray diffraction

1. Introduction

Moore's law states that transistor density in two-dimensional (2D) integrated circuits (ICs) doubles approximately every two years [1]. Nowadays, the law is becoming unsustainable. Modern electronic devices are in a constant demand of higher density integration, smaller size, superior performance and lower cost. For instance, MEMS solutions demand high density small size packaging. Traditional two-dimensional integration approaches have been shown to have serious limitations when it comes to fulfilling these demands. Since interconnects do not scale with transistors, long distances contribute to increased circuit delay and power consumption [2]. These factors have driven semiconductor industry to develop more advanced three-dimensional (3D) packaging technologies with shorter interconnections. 3D IC consists of two or more layers of active electronic components that are integrated both horizontally and vertically into a single circuit [3]. [4]

Different techniques that provide short interconnections between stacked chips have been developed in recent years. One of these methods is through-silicon via (TSV). A comparison among technologies of wire bonding, flip chip and through-silicon via is presented in Table 1. In recent years TSV technology has garnered a lot of interest because it is considered as a key enabling technology for three-dimensional integrated circuit stacking and thus a key factor for More-than-Moore technologies [5]. The concept More-Than-Moore implies combining multiple functionalities, that do not necessarily scale according to aforementioned Moore's law, into a device [6]. [7]

Through-silicon via is a structure through entire silicon substrate that enables vertical electrical connections between chips. The substrate material is most often silicon, but other materials, such as glass can also be used as a substrate material [8]. In this case the technique is called through-glass vias (TGV). TSV has numerous favorable electrical properties that are needed in three-dimensional integration including high density, high electrical performance, high signal speed, reduced resistance and capacitance delays and low power consumption. TSVs are filled with conductive material, most commonly with copper because of its high conductivity, good resistance against electromigration and stress migration and relatively easy fabrication methods. [9]

Reliability issues and the cost of manufacturing are the biggest obstacles with TSV technology. The fabrication process of TSV is slow and complicated due to its high aspect ratio structure. Thus, the yield is low. The large difference in thermal expansion mismatch between copper and silicon can cause reliability issues. Common defects in TSV structure are voids and cracks which will propagate at high temperatures with time. Also, the small features increase the effect of electromigration in the structure. [10]

Table 1: Comparison among technologies of wire bonding, flip chip and through-silicon via.

Wire bonding	Flip chip	Through-silicon via
Advantages	Advantages	Advantages
- Low cost - Long experience - Flexible and easy manufacturing - Reliability	- Low cost - Short interconnections	- Shortest interconnections - Allows high density stacking - High electrical performance
Disadvantages	Disadvantages	Disadvantages
- Low density - Long wiring length - Large pad area - Poor signal integrity at high frequencies	- Reliability issues e.g. CTE mismatches - Requires underfill - Large solder ball size and pitch inhibits high density stacking	- Reliability e.g. electromigration and CTE mismatches - Complex and high cost fabrication process

This master's thesis consists of a literature survey and an experimental research section. The structure of thesis is as follows: in section 2, the fabrication process steps of TSVs are presented. The effect of design choices on reliability of the via are discussed. Different via profiles of TSVs are also introduced. In section 3, resistance measurement of TSVs is discussed. In section 4, the main reliability issues of TSVs are introduced. Also, FEM simulations and Weibull analysis are discussed. Section 5 consists of sample preparation techniques and imaging options for failure analysis of TSVs. After the literature survey the purpose of the thesis is summarized in section 6. Section 7 presents the methodology used in order to achieve the goals of the research. The objective of the thesis is reliability and lifetime assessment of tapered partially copper-filled blind TSVs. The results of the experiments are presented and discussed in section 8. Finally, section 9 summarizes the results and concludes the thesis.

2. The fabrication of TSVs

In this section the fabrication processes of the TSVs are introduced. Via-first, via-middle and via-last approaches are also presented. The fabrication process of the TSV structure varies depending on the design. For instance, partially-filled (annular) and fully-filled TSVs have a different fabrication processes. Also, the structures, such as redistribution lines (RDL) and contact pads, which enable electrical measurement, add fabrication steps. Regardless of the design, there are similar main steps in all of the fabrication processes, namely, etching of the vias, deposition of insulation and barrier layers and filling of the vias.

The design choices have a major impact on the reliability of the structure. For instance, by changing current density and bath chemistry in the electroplating process, copper fillings with different properties can be fabricated.

2.1. The fabrication process steps

The fabrication process of TSVs starts with the etching of the silicon wafer. The etching is often done with deep reactive-ion etching (DRIE) using the BOSCH process. Sulfur hexafluoride/oxygen (SF_6/O_2) plasma etching is also used quite often in high aspect ratio structure applications, like in TSVs, because of its high etching rate of silicon [11]. After etching, the next step is most often the deposition of a silicon dioxide (SiO_2) insulation/dielectric layer which electrically isolates the TSV from the surrounding silicon substrate [7]. This is followed by the fabrication of diffusion/barrier layer which can be made from silicon nitride (Si_3N_4), titanium nitride (TiN) or tantalum nitride (TaN). The thickness of the insulation layer is about 1-2 µm whereas the thickness of the diffusion layer is in the range of 5-20 nm. Both of these layers can be deposited with the plasma-enhanced chemical vapor deposition (PECVD). Silicon dioxide layer can be also deposited with wet thermal oxidation process. Atomic layer deposition (ALD) can also be used to deposit diffusion/barrier layers. It produces highly conformal layers and it allows the deposition in the low temperatures [12]. The temperature during these steps is kept under 250 ^{o}C. [7]

After the fabrication of the insulation and the barrier layer, copper seed layer is sputtered on the structure. This is followed by filling of the vias. The most common technique for the copper via filling is an electroplating process. This technique does not require costly and complex vacuum systems and the processes are easily controlled and maintained [4]. After this, a chemical-mechanical planarization (CMP) can be used to remove overburden copper. If the overburden copper is not removed, thermo-mechanical load increases in the structure in high temperatures [13]. Figure 1 presents a simplified TSV structure. [7]

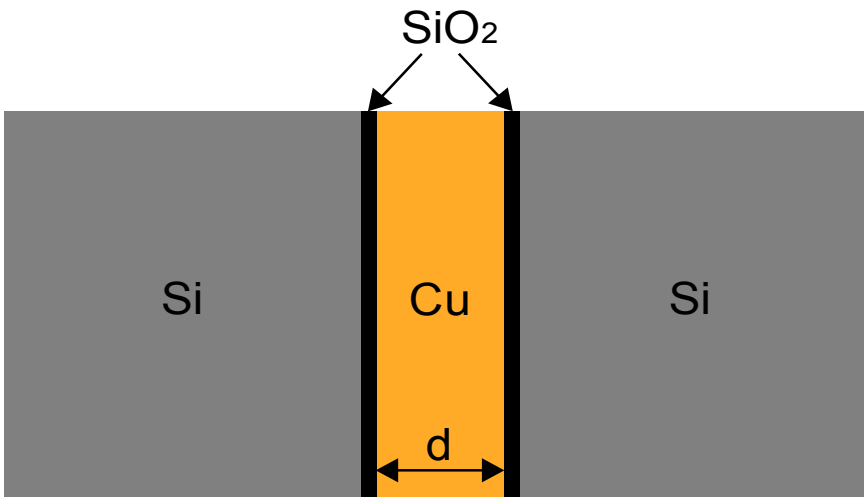

Figure 1: A simplified TSV structure. The symbol d denotes the diameter of the via.

TSVs are initially buried in the silicon substrate. These vias are called blind-vias. In order to get the via through the substrate, it needs to be exposed in a process called thinning, in which the substrate is grinded away. Therefore, TSV device wafers are thin and fragile. TSV device wafers are quite often bonded to carrier/handle wafers, to ensure mechanical durability during the three-dimensional integration. This bonding can be done with a direct bonding or with adhesive bonding. In the direct bonding, temperature may get really high causing high thermo-mechanical stresses in the structure. [2]

In order to get daisy chain structure, redistribution layers (RDLs) are often fabricated to TSV wafers. Redistribution layers can be fabricated from aluminum and copper. The aluminum is sputtered on the backside of the device wafer and then patterned. This is followed by etching of the vias so that the bottoms of the vias are in contact with the patterned aluminum. In order to get the electrical contact between backside aluminum and the copper filling of the vias, the isolation layer and the barrier layer have to be etched away before the copper seed layer deposition. Front-side copper redistribution layers and contact pads can be fabricated with through-resist electroplating. [14]

TSV performance can be enhanced if the height of the via is shortened. Deep TSVs degrade frequency response. This is because all of the parasitic elements, such as resistance, inductance and capacitance, scale up as the interconnection length increases. Electrical properties of TSVs can also be altered by changing the via diameter. TSV with large diameter results in small resistance and high capacitance whilst the TSV with small diameter results in high resistance and low capacitance. Therefore, either too large or too small via diameter is not an ideal choice when designing electrical performance of the TSV. [15]

2.1.1. Deep reactive-ion etching

Reactive-ion etching (RIE) is a dry etching technique which is frequently used to etch silicon substrates. It uses reactive plasma to remove materials and yields tapered sidewalls due to its isotropic etching process. However, the technique has a poor selectivity between silicon and the

masking material. Hence, the technique is typically used to etch only shallow features. When creating deep features, other techniques such as deep reactive-ion etching (DRIE), are used. [16]

Deep reactive-ion etching (DRIE) is used to create near vertical walls with a high aspect ratio. The aspect ratio in a geometric shape is the ratio between dimensions. For instance, if the diameter of via is 5 µm and the height is 50 µm, the aspect ratio is 1:10. The etching process is highly selective between silicon and masking material. For example, silicon dioxide (SiO_2) can be used as the hard mask during the etching process. [17]

The BOSCH DRIE process causes a sidewall surface roughness called scalloping. This is because of the cyclic etching and passivation in BOSCH process. The deposition of the passivation layer protects the sidewalls during subsequent etching process. A schematic illustration of the BOSCH process is presented in Figure 2. DRIE uses fluorine based chemistries, such as tetrafluoromethane (CF_4), nitrogen trifluoride (NF_3) and sulfur hexafluoride (SF_6) that etches silicon isotropically. Passivation layer is usually formed with oxygen (O_2) or octafluorocyclobutane (C_4F_8). Modifications in gas flow ratio change the etching profile [18]. For instance, lowering the ratio of the etching gas in relation to the passivating gas, decreases the tapering angle [18]. If the roughness is high, it is difficult to deposit conformal insulation and diffusion layers. This is an issue especially in TSVs with a high aspect ratio. [17]

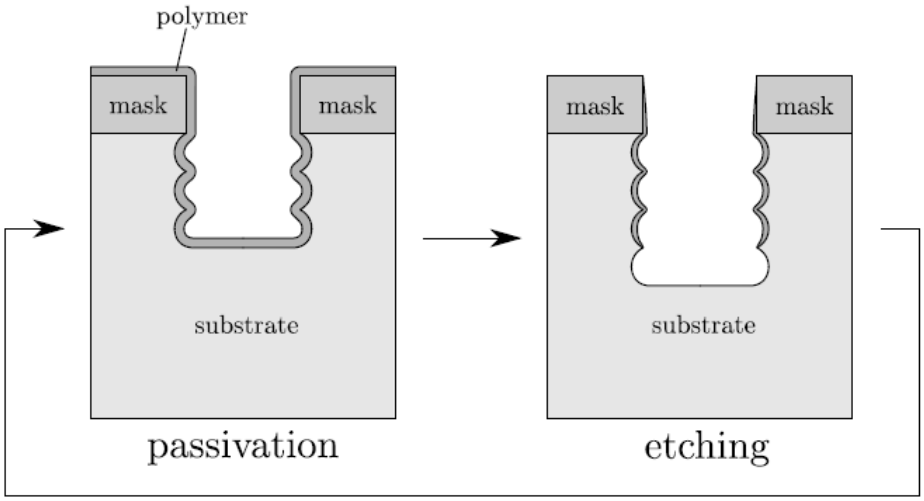

Figure 2: A schematic illustration of the BOSCH process. The process consists of cyclic passivation and etching steps. The passivation layer protects sidewalls during the etching cycle. [19]

Cryogenic etching process can also be used to fabricate TSV structures. The method uses SF_6/O_2 gas mixtures to etch silicon at low temperatures in the range from -100°C to -130°C. Etching does not occur below -140°C since the reactive gases start to freeze. The main advantages of cryogenic etching when compared with BOSCH DRIE are higher etching rate and no scalloping at the sidewalls. Different via profiles can be obtained with cryogenic etching by altering gas flow ratios. [20]

2.1.2. Fabrication of insulation and barrier layers

The fabrication of reliable insulation and diffusion layers is a challenging step in the TSV fabrication process. There are two main factors that cause difficulties: the high aspect ratio of the TSV and the sidewall scalloping. Thus, the fabrication of conformal layers inside the via, is difficult. If the quality of the insulation layer and barrier layer are substandard, this might result in electrical leakage or other reliability issues in the TSVs. [21]

The thickness of the diffusion layer is few nanometers. With such thin layer it is difficult to get a good coverage. Because of this some defects, for instance pinholes, may occur. Pinhole defects cause leakage currents between the TSV and the silicon substrate, thus increasing the capacitance of the TSV [2]. [17]

Lee et al. [22] reported that the deposition rate of the TiN diffusion barrier on the SiO_2 insulation layer has a bigger impact on the reliability than the thickness of the barrier. Slow deposition rate, for example 0.05 nm/s, creates a conformal deposition and thus better barrier performance than rapid deposition, for example 1.00 nm/s. Slow deposition rate leads to amorphous structure while rapid deposition leads to polycrystalline structure. Crystallinity increases with the deposition rate. Amorphous structure is preferred for a diffusion barrier because the diffusion of copper ions mainly takes place through grain boundary paths. When the thickness of the TiN barrier layer is increased above 20 nm, columnar grain structures were noted [22] to occur rather than random orientation structures. Columnar structure does not provide effective diffusion barrier because it provides rapid diffusion paths for copper. Thus, it is not useful to increase the thickness of the barrier layer above 20 nm. [22]

Tantalum nitride (TaN) is an attractive material for the diffusion layer, because of its amorphous structure provides good barrier properties to diffusion of copper. Tantalum nitride has a high melting point which results in a high activation energy for the diffusion process and it has good adhesion to copper seed layer. Titanium nitride (TiN) also has good adhesion to copper and is cheaper than tantalum. These factors make TiN more appealing barrier material. [17]

2.1.3. Seed layer deposition and filling of the vias

Critical requirements for the high aspect ratio via filling, is continuity, a good adhesion and uniformity of the seed layer. These properties provide an underlayer that is necessary for nucleation and growth of copper inside the via. If the aspect ratio of the TSVs is high, the electroplating process will be done slowly in order to avoid possible defects. [4]

Insufficient electroplating process cause defects in copper filling, such as cracks, voids and necking of the via. High current density electroplating process tends to leave voids at the center of the via. This happens because of the necking phenomenon which is due to higher copper ion concentration and current crowding at the top of the via than in the bottom of the via [23]. Defects can cause variations in resistance or even electrically open vias. They can also contain trapped electroplating chemicals which would present a reliability risk. Also, thermo-mechanical stresses cause the propagation of the aforementioned defects. Typical via filling defects are presented in Figure 3. [24]

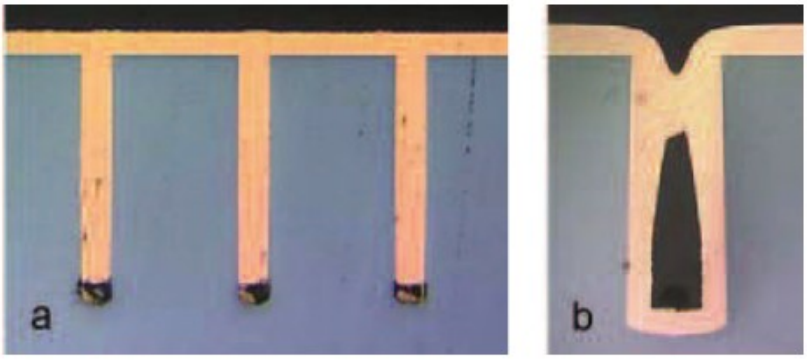

Figure 3: Via filling defects. (a) Voids at the bottom of the via due to poor wetting and (b) necking of the via. [24]

Although electroplating is the most commonly used via filling technique, it is not the only one. For instance, Santagata et al. [12] presented TSV filling by copper electroless plating (ELP). This method produces uniform fillings and in a shorter time than electroplating. This is because the plating process happens selectively on desired locations. This feature becomes even more important when the diameter of the via decreases. Furthermore, the method enables low cost and low temperature fabrication process. [12]

2.1.3.1. The effects of electrolyte composition during electroplating process

Improvements in bath chemistry composition and wettability are fields of interest for the electroplating of copper in TSV technology. The aim is to have fast and defect free filling of the vias with desired crystal structure. This would save time and thus money in fabrication. [25]

The level of impurity in copper fillings has a considerable impact on the microstructure and thermo-mechanical behavior of the TSVs. These impurities are caused by additives in electrolyte used in the electroplating process. It has been reported [26] that the high impurity copper films show three times larger tensile stress level than the low impurity copper films. These results indicate that the void free filling of the vias should not be the only consideration when adjusting the electrolyte composition. [26]

High level of impurities, such as chlorine, nitrogen, oxygen and carbon, cause fine grain size in copper even after the heating phase. This can be explained by a phenomenon called Zener pinning. The phenomenon means that the small particles prevent the motion of the grain boundaries by causing a pinning pressure which counteracts against the force pushing the boundaries. This means that the impurities distribute along the grain boundaries and inhibit the free growth of grains. Impurities also prevent free movement of dislocations, which limits the relaxation of stress causing high tensile stress in the structure. The stress can build up, for example, from fabrication processes or external thermal stresses. The lack of impurities in the grains enables freedom to grow and relax from thermal stresses thus increasing reliability. [26]

A typical electrolyte used in copper electroplating process consists of following components: copper ions, acidic electrolyte, halide ions, accelerator, suppressor and leveler. The most commonly used acidic electrolyte is sulfuric acid and it provides necessary conductivity to the

bath. Halide ions reduce anode polarization and accentuate the effect of some additives. Chloride is the most commonly used halide ion. Accelerator increases the copper deposition rate whilst suppressor decreases the deposition rate. Leveler prevents copper deposition at via aperture preventing a pinch off. The purpose of these additives is to accelerate deposition of copper at the bottom of the via and suppress deposition at the top of the via. This is needed in order to achieve void free filling. Desired electroplating process is presented in : Figure 4. [4]

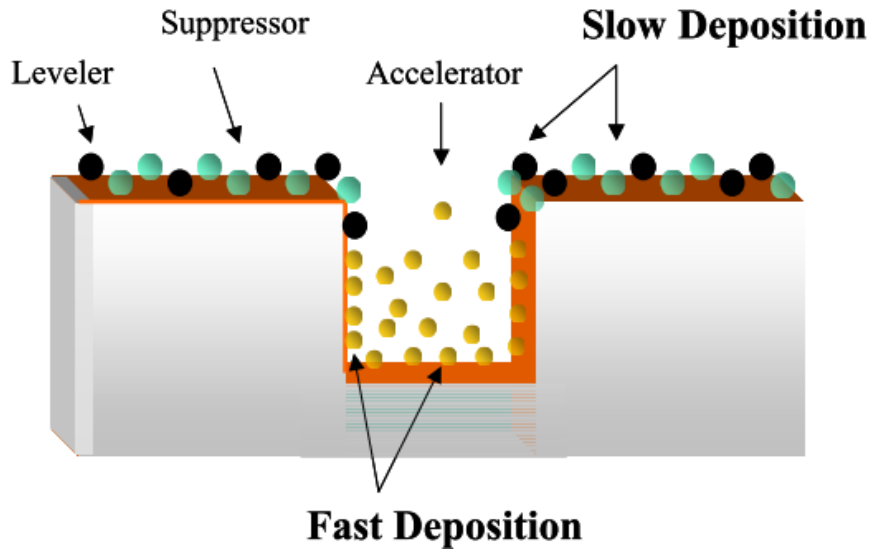

Figure 4: Typical electrolyte characteristics for void free electroplating process. [4]

2.1.4. Types of TSV profiles

There are four main types of TSV profiles, namely cylindrical, tapered, annular and coaxial TSVs. The profile depends on the etching process as well as the via filling process. Different via profiles are presented in Figure 5.

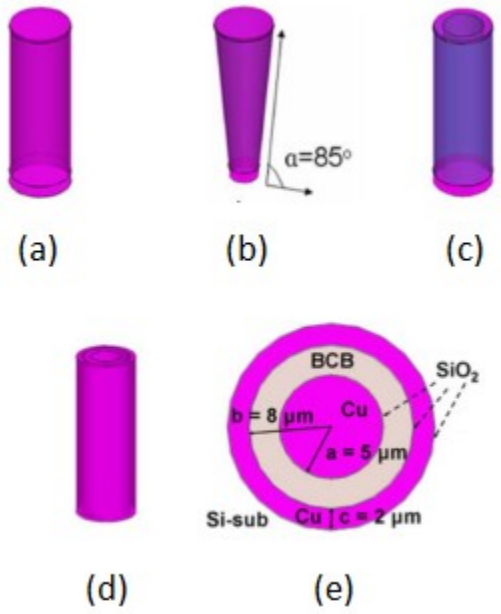

Figure 5: Different via profiles. (a) Cylindrical via, (b) tapered via, (c) annular via, (d) coaxial via and (e) top view of the coaxial via. (Modified from [15] and [27])

2.1.4.1. Cylindrical vias and tapered vias

Usually, sidewalls of the vias are slightly tapered because of the DRIE has an intrinsic isotropic etching process. If the walls are vertical and there is a poorly made seed layer at the bottom, it is quite possible that vias will close during the electroplating process leaving a void inside. However, a tapered wall can make it easier to fabricate conformal depositions. This is due to the fact that with tapered walls the step coverage is improved. For instance, the necking phenomenon is lesser in tapered vias than in cylindrical vias although the copper deposition rates are similar [23]. These features of tapered vias increase the yield and reduce the cost of fabrication [18]. The downside of the tapered walls is that the interconnection density is decreased due to the larger openings of the vias. However, in cylindrical vias the stress accumulation at the opening of the via is greater than in tapered vias [18]. Because of these factors, the walls are usually made with slight angles of about 85^{o} which is considered a good trade-off. [28]

Only a slight reduction from the 90^{o} angle causes a significant variation between the top and bottom surface areas. For example, if the taper angle is 87^{o} in TSV which has 4 µm top diameter and height of 30 µm, the bottom diameter is only 0.856 µm. This causes different electrical and mechanical properties in the top and bottom sections of the TSV. For example, current and thermal stresses will not distribute evenly, unlike in cylindrical vias, across the whole via. Thus, there are some critical failure points due to non-uniformity. [29]

Simulations [29] have proven that the tapering of the vias causes a greater peak and variation in the direct current values at the bottom region of the via compared to the top region of the via. On

the other hand, the temperature is uniformly distributed across the TSV. This is likely due to the good heat conductivity of copper. These results indicate that the tapering worsens the TSV's electromigration resistance. [29]

Different via profiles have different keep-out zones (KOZ). A keep-out zone is the area near the TSV that cannot be used due to TSV-induced thermal stresses and mounting constraints. The size of the zone is usually defined by a stress threshold. Devices are placed in areas that have smaller stress than the threshold value in order to guarantee that the devices are not exposed to unpredictable stresses. Tapered vias require much smaller KOZ at the bottom regions of the via when compared to cylindrical vias. This enables an opportunity to fit more devices in the stacked structure. Basically, the smaller diameter of the via the smaller KOZ. [29]

Tapering affects TSVs signal delay. It causes signal delays for both directions to be different. Bottom to top delay is reported to [29] be consistently larger than the top to bottom delay. This feature makes it difficult to use tapered vias in bi-directional buses where it is usually assumed that the delays are the same in both directions. In cylindrical vias there is the same delay to both directions due to its symmetric form. This allows them to be used on bi-directional buses with the same clock. [29]

2.1.4.2. Annular vias

Filling the vias partially, also known as annular vias, reduces the electroplating time and thus the fabrication cost. Electroplating process is the single most time consuming step in fabrication. Partially filled vias require about 50 % less time in electroplating than fully filled vias. Nevertheless, the electrical properties of the partially filled vias are satisfactory. Filling vias partially also has the effect on the thermo-mechanical properties. With free surface at center the stresses are lower and thus the reliability is improved. Nevertheless, the durability of the copper also worsens with the annular filling. [30]

2.1.4.3. Coaxial vias

Coaxial TSVs have a basic configuration of a central signal-carrying conductor surrounded by a concentric ground return. Coaxial TSV offers better signal integrity than any other TSV structure. This is because the electromagnetic fields carrying the signals exist only between inner conductor and outer shell. The structure provides inherent signal shielding and electromagnetic interference control. This structure also demands a small keep-out zone (KOZ) thus enabling enhanced TSV input/output density when compared to other TSV structures. The major disadvantage of the coaxial TSV is the challenging fabrication process. Out of all via profiles, coaxial vias are the rarest at the moment. [27] In Table 2 a summary of the properties of cylindrical, tapered and annular vias is presented.

Table 2: Summary of the properties of cylindrical, tapered and annular vias.

Cylindrical	Tapered	Annular
Advantages	Advantages	Advantages
- Signal delay same to both directions - Stresses and currents distributed evenly - Better electromigration resistance than in tapered vias	- Smaller reflection noise and signal loss than in cylindrical vias - Requires smaller KOZ at the bottom region - Improved step coverage, increases yield and thus reduces fabrication costs	- Decreases fabrication time and thus the cost is lower - Lower stresses than in cylindrical and tapered vias - Both cylindrical and tapered vias can also be fabricated as annular
Disadvantages	Disadvantages	Disadvantages
- Necking phenomenon causes voids inside the vias, problem especially in high aspect ratio structures - Stress accumulation greater at the opening of the via when compared to tapered vias	- Different signal delay to both directions - Worse electromigration resistance than in cylindrical vias - Currents and thermal stresses do not distribute evenly across the structure. Causes critical failure points.	- Electrical properties - Durability

2.2. Via-first, via-middle and via-last approaches

There are three different integration options for TSV technology depending on which point of the process flow the via is fabricated. The options are called via-first, via-middle and via-last. Via-first process means that the via is made right at the beginning of the fabrication process. After the via is made, front-end-of-line (FEOL) processes, for instance the formation of transistors, occurs. Lastly, the back-end-of-line (BEOL) processing is done. During the back-end-of-line processes, for example, interconnections are made to form desired electrical circuits. The temperature is kept relatively low during the back-end-of-line processes. [9]

There are certain advantages in via-first approach. For instance, it enables the usage of the high conformal deposition materials for isolation and filling of the vias. This would enable higher density of connections or high voltage operations for certain final product applications [31]. The downside of the via-first option is that the wafer undergoes the highest temperatures, for instance annealing takes place, during the front-end-of-line processes. The annealing step causes reliability issues in the TSV structure. For instance, diffusion of the filling material into silicon increases and the thermal stresses may cause cracking at the interfaces. [9]

Via-middle process means that the front-end-of-line processes are done before the fabrication of the vias. Thus, the vias are not affected by high temperature annealing processes. In the via-last process the vias are made at the very end of the process flow. The downside of the via-last process is that the alignment of the vias to the exact desired position is challenging. [9]

2.3. Non-copper TSV filling materials

At the moment, copper is by far the most common filling material. The filling process of the TSV is the most expensive of all fabrication processes. This is because of the excessively long time to fill the TSVs. This has inspired studies about different filling materials and methods to lower the cost of the fabrication without losing the electrical properties of the TSV. [12]

Some of the reported filling materials and techniques being assessed are vacuum assisted via filling with molten solder [32], printing technique to fill the vias with conductive paste [33] and filling the vias with carbon nanotubes [34]. In vacuum assisted via filling with molten solder, an etched wafer is dipped into a molten metal bath. After this, pressurized nitrogen (N_2) gas is applied which forces molten metal to fill the vias. This technique is quicker, and costs less than copper electroplating. [32]

The conductive paste has showed excellent filling characteristics. The upside of the paste is a low cost and a quick filling time. The downside is relatively high resistance and the contraction of the paste material during the cure cycle. [33]

TSV technology could make use of the unique characteristics that carbon nanotubes possess especially thermal, electrical and mechanical properties. For instance, carbon nanotubes can carry current densities in excess of 10^{10} A/cm^2 while conventional copper can carry up to 10^6 A/cm^2. The use of carbon nanotubes would also eliminate the problem of electromigration with copper interconnects. The filling process of TSV with carbon nanotubes can be done with chemical vapor deposition (CVD). [34]

Although, carbon nanotubes demonstrate electrical and thermal properties that are suitable for TSV filling material, they still have major drawbacks in fabrication cost and electrical performance. It has also been reported, that it is difficult to achieve carbon nanotube forest that has lower resistance than copper filled TSVs. [12]

Wang et al. [35] reported a novel approach to fabricate carbon nanotube fillings for the TSVs. This approach overcomes two major limitations of carbon nanotube interconnects, which are carbon nanotube forest density problem and high fabrication temperature. The density problem is caused by a porosity of more than 90 % in a typical aligned carbon nanotube forest. This causes

carbon nanotube forests to be inefficient in thermal and electrical transportation. The porosity is reduced by vapor densification process, which permits packing many more carbon nanotubes in the same footprint, to improve thermal and electrical properties. [35]

The reported fabrication process is illustrated in Figure 6. The electrical performance was measured and the results indicate that good ohmic contacts were established on both ends of carbon nanotubes. In their previous study Wang et al. measured carbon nanotube forest resistivity to be 33.8 mΩ·cm [36]. But when the nanotubes are densified the resistivity drops to 3.9 mΩ·cm, thermal transportation also improved. [35]

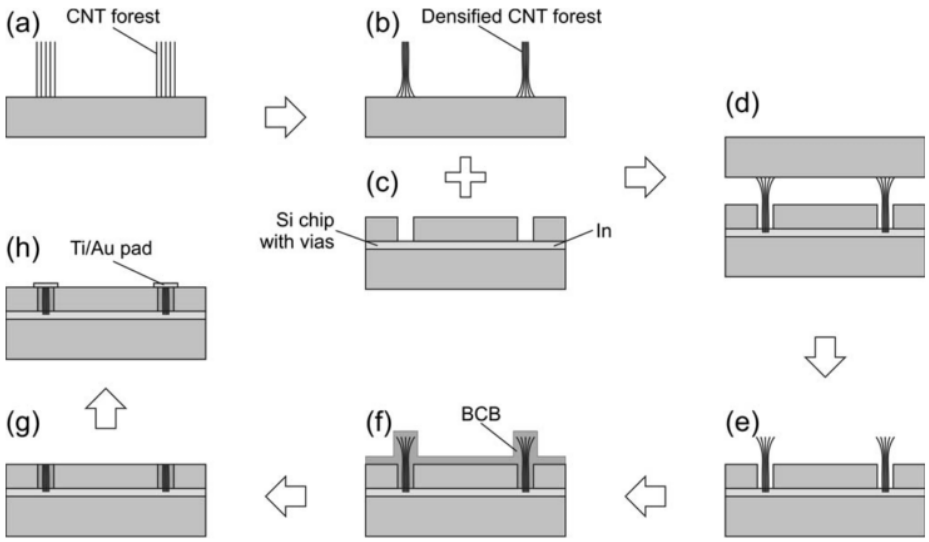

Figure 6: The fabrication process of carbon nanotube filled TSVs. (a) Carbon nanotube forests are grown by thermal CVD at high temperature (700 ^{o}C). (b) The forests are densified with a vapor densification process. (c) The target chip is prepared with indium (In) layer on the bottom of the vias. (d) The two chips are aligned and bonded at low temperature (200 ^{o}C). (e) The growth substrate is separated from carbon nanotube forests. (f) Benzocyclobutene (BCB) is spin coated in order to fill the gaps between sidewalls of the vias and the carbon nanotube forests. (g) The BCB supported structure is planarized. (h) Metallic pads are fabricated on the vias. [35]

Tungsten is one option for the conductive filling material of the TSV. The main advantages of tungsten are relatively low resistivity, very conformal to fill high aspect ratio structures, coefficient of thermal expansion matches better than one from silicon when compared to copper and it has good resistance to electromigration. On the other hand, tungsten needs an adhesion layer before deposition. The biggest disadvantage of using tungsten as the filling material is the high stress of the film that limits allowed deposition thickness. In order to get a good conformal filling, different approaches have been investigated. For instance, higher fabrication temperatures have been tried to lower the stress of the deposited tungsten film. Tungsten can be deposited with chemical vapor deposition (CVD). [31]

3. Resistance measurement

Electrical parameters of the TSV can be measured with both 2-point probe and 4-point probe. In the 2-point probe measurement, the resistance is measured by attaching two wires to the test sample. The problem is that the resistance of the wires and the contact resistance between the wires and the sample are also measured. Usually, the contact and the wire resistance are much smaller than the resistance of the sample. But, when measuring very small resistances the contact resistance may dominate and thus the resistance of the sample may be hard to define. [37]

The effects of the wire resistance and the contact resistance can be eliminated by using 4-point probe. Schematic four-point probe set-up is presented in Figure 7. In this method four wires are attached to the sample. A constant current is made to flow through the sample. This can be done using a current source or a power supply. An ammeter in series with the power supply can be used to obtain value of the current. If the sample is resisting the flow of electrical current, there will be a drop of potential as the current flows through the sample. This can be measured with voltmeter. There is high impedance at voltage port which minimizes the current flow through the voltmeter. Thus, the voltage drop is extremely low in the voltmeter circle. [37]

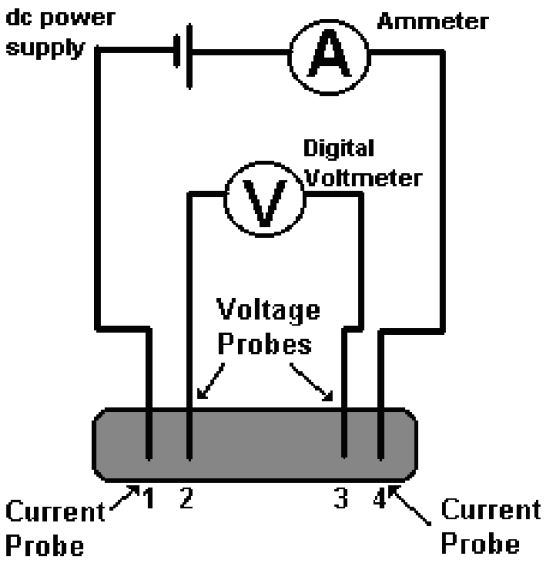

Figure 7: Schematic four-point probe set up. [38]

3.1. Resistance of the via

The total resistance R_{Total} of the via is a combination of the via wall resistance R_{Wall} and the metal contact resistance R_{Contact} between via and metallization

$$R_{\mathrm{Total}} = R_{\mathrm{Contact}} + R_{\mathrm{Wall}} \quad (1)$$

The total resistance can be measured and the via wall resistance is calculated as follows:

$$R_{\mathrm{Wall}} = \rho_{\mathrm{Cu}} \frac{L}{A_{\mathrm{Eff}}} \quad (2)$$

in which ρ_{Cu} is the copper resistivity, A_{Eff} is the effective area and L is the height of the via. When R_{Total} and R_{Wall} are known, the contact resistance can be easily calculated from Equation (1).The value of the sidewall resistance ranges from 22 % [37] to 40 % [31] of the total resistance of the via. Thus, the contact resistance is 60-78 % of the total resistance. The difference is because of the used materials and the shape of the via. [37]

Voids inside of the via only seem to slightly increase the resistance of the TSV. Let say that the void decreases the cross-sectional area of the single TSV by 2 %, which should lead to <1 % increase in the resistance of the daisy chain structure. In other words, the voids in TSVs have a negligible impact on the increase of the resistance. The major resistance increase is caused by propagation of cracks between interfaces thus effectively reducing the contact area. [39]

During reliability tests appropriate failure criterion definition of a single TSV is needed to quantify the reliable samples. Some uses the 10 % change in resistance as a criterion because electrical circuits are designed to work with a maximum RC delay change of 10 %. Basically, if the resistance increases more than 10 %, the sample is considered as failed. It has been suggested [10] that failure criterion for a TSV should be 1 Ω resistance increase because initial electrical resistance spread caused by fabrication makes 10 % failure criterion for a single TSV irrelevant. [40]

3.2. Kelvin structure

Kelvin structure has certain advantages compared to daisy chain structure, in which there are numerous TSVs in a chain. The Kelvin structure enables accurate TSV resistance monitoring and it ensures that change in resistance in the structure is due to TSV by itself and not of metallization of interconnect. It is good to notice that the via resistance is the key parameter, when evaluating the electrical performance of the TSV. The value of the resistance is affected by fabrication and design parameters such as the area of TSV opening, the barrier layer thickness and the seed layer type. The resistance of a single via is usually around 5-15 mΩ. [37]

The Kelvin structure is presented in Figure 8. The structure employs 4-point probe measurement as follows: the constant current is present between two contacts, for example contacts 1 and 3, and the voltage is measured between the other two contacts 2 and 4. [37]

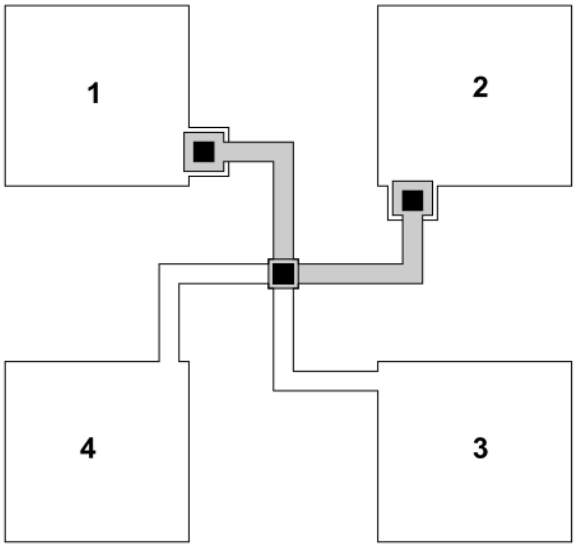

Figure 8: Kelvin structure to measure contact resistance. [41]

3.3. Daisy chain structure

Daisy chain structure is a sequence of numerous samples in series, for example TSVs. Several hundred samples can be examined without finding any defects caused by fabrication process or accelerated stress testing. Because of this, daisy chain structures are almost necessity in order to detect defects. With daisy chain structure, it is easy to increase the number of the samples. The drawback of daisy chain is that the weakest link of the structure is spotted first. If even one TSV fails, the whole daisy chain behaves as an open circuit. This might skew the conclusion of the durability of the test sample. Also, pinpointing the sample that has actually failed can be difficult. Naturally, this complicates failure analysis. [37]

The daisy chain structure for TSVs is presented in Figure 9. The daisy chain enables measurement of the total resistance of the structure that consists of numerous vias. In daisy chain structures the electrical resistance increases steadily during thermal cycling. This is because thermally induced damage leads to the formation and growth of defects. The total resistance can be used as an indicator of a rate of success of the manufacturing process. Also, the change in the resistance can be observed during reliability testing. In addition to the resistance of the vias, the total resistance also includes the resistance of copper and aluminum lines that connect the vias. [42]

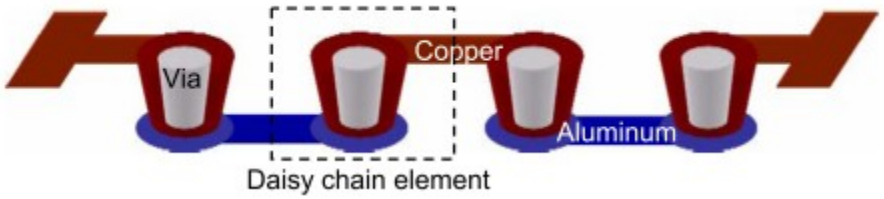

Figure 9: Schematic drawing of the TSV daisy chain structure. [42]

4. Reliability and simulations of TSV

Reliability is the ability of an item to maintain its intended functions without failure under predetermined conditions over a specific period of time [43]. The reliability studies of TSVs are mainly focused on four failure mechanisms: cracking and interfacial delamination caused by thermal stresses, electromigration, dielectrics reliability and copper diffusion from the vias into active silicon. [40]

In addition to common failure mechanisms of TSVs, finite element method (FEM) simulations and Weibull analysis are also discussed in this section.

4.1. Electromigration

Electromigration is a phenomenon in which metal atoms are gradually moved due to the electron momentum transfer. Electrons release metal atoms from the conductor when current is flowing through it. These atoms accumulate at the positive end of the conductor causing extrusions while the voids are formed at the negative end of the conductor. Voids increase resistance and might even cause open circuits while the extrusions might cause short circuits if the extrusion serves as a bridge between adjacent metals. The more prominent of these failure modes is the accumulation of voids. This is because of the small dimensions make it easier for voids to reach a critical size large enough to cause an electrical failure. Also, the presence of harder layers, for example metallic barrier layers, prevents the formation of extrusions. [44]

4.1.1. Driving forces for electromigration

Electromigration happens through diffusion under an electrical driving force. The driving force can be divided into two main factors: a direct force and an electric wind force. The schematic presentation of these forces is presented in Figure 10. The driving force equation is as follows:

$$F_{\mathrm{EM}} = F_{\mathrm{direct}} + F_{\mathrm{wind}} \tag{3}$$

The magnitude of the direct force is proportional to the applied electric field. Also, the direct force has the same direction as the electric field. The electron wind force means the scattering of the electrons at the places of imperfections of the lattice, such as dislocations, vacancies and grain boundaries. When the free electrons in metals shift through the material, they interact with the imperfections. This interaction causes scattering. Higher temperature causes more vibration of the atoms which leads to greater scattering of the electrons. The scattering causes a force proportional to the intensity of the electric field and in the opposite direction to the electric field. In metals the electron wind force is larger than the direct force. Thus, the atomic flux goes to the

opposite direction than the electric field. If the atomic flux in a certain region is greater than the atomic flux out of the same region, atoms accumulate and cause extrusions. The other way around, the voids are formed. [45]

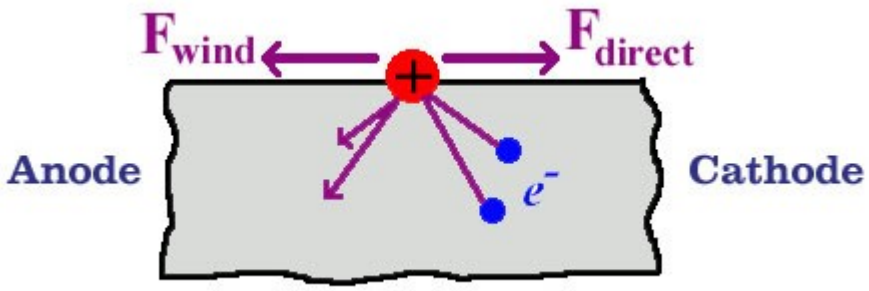

Figure 10: The driving force of the electromigration is the sum of the direct force and the electron wind force [46]

The most important factors affecting the speed of the electromigration process is the temperature and the current density. The higher these values are, the quicker the process is. Due to the demand of high aspect ratio structures local heating and current density increases. Thus, electromigration becomes a larger problem when the feature size decreases [44]. The value of the current density increases rapidly, for instance, in interconnects and voids, in which the cross-sectional area is reduced. This non-uniform distribution of current density across the conductor is a phenomenon called current crowding. It causes a local increase in the temperature called Joule heating. The rise in temperature in turn increases the electromigration which leads to the formation of voids and extrusions. The voids in turn increase the current crowding which leads to increased temperature and so forth. [45] The cycle is presented in Figure 11.

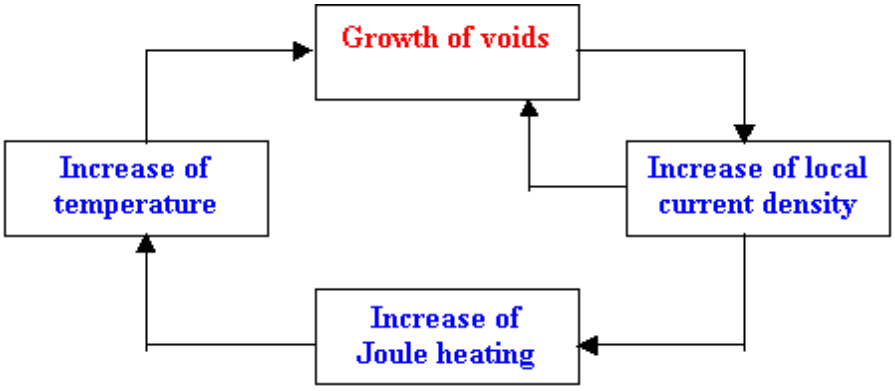

Figure 11: Thermal acceleration cycle during electromigration.

4.1.2. Electromigration in TSVs

Mean time to failure (MTTF) of a wire when taking electromigration into consideration can be calculated with the Equation (4), which is called the Black's equation:

$$\mathrm{MTTF} = A_c j^{-n} e^{(\frac{E_a}{kT})} \tag{4}$$

where A_c is a constant depending on the wire geometry and the metals microstructure, j is a current density, n is the current density exponent, E_a is a activation energy, k is the Boltzman's constant and the T is the conductor temperature. [47]

Electromigration in metal wires can be divided into four categories. These categories are as follows: current-induced migration caused by movement of electrons, stress-induced migration caused by thermo-mechanical stress gradient, temperature-induced migration caused by temperature gradient and atomic migration caused by atomic concentration gradient. A complete estimation of electromigration should consist of all of the driving forces. [48]

The atomic flux terms J_e, J_s, J_t and J_a that are caused by aforementioned current-induced migration, stress-induced migration, temperature-induced migration and atomic migration respectively, can be calculated with following equations:

$$J_e = \frac{Dc\vec{j}e\rho Z}{kT} \tag{5}$$

$$J_s = \frac{Dc\Omega}{kT} \cdot (\nabla(\sigma_m)) \tag{6}$$

$$J_t = \frac{DcQ^\star}{kT} \cdot \frac{\nabla(T)}{T} \tag{7}$$

$$J_a = -D\nabla c \tag{8}$$

The equation that consists of all driving forces of electromigration is as follows:

$$\frac{\partial c}{\partial t} + \nabla \cdot (-D\nabla c + \frac{Dc\vec{j}e\rho Z}{kT} + \frac{Dc\Omega}{kT} \cdot (\nabla(\sigma_m)) + \frac{DcQ^\star}{kT} \cdot \frac{\nabla(T)}{T}) = 0 \tag{9}$$

where c is atomic concentration, D is diffusivity, $\vec{j}$ is current density, e is electron charge, Z is effective charge, Ω is atomic volume, σ_m is hydrostatic stress, $Q^\star$ is heat of transport, ρ is resistivity, k is Boltzmans constant and T is temperature. [29]

Lu et al. [29] used in their study Equation (9) to simulate MTTF at different points of TSV. The results are presented in Table 3. The alphabets in Table 3 match the ones in Figure 12**.** Both tapered and cylindrical TSV were simulated. They found out, that tapering causes worse overall electromigration trends. They also found out, that the position that suffers the most from electromigration in cylindrical TSVs is the point J in Figure 12. That is the center point of the TSV and the bottom pad. In the tapered TSV, points I and K are the most vulnerable. The edges of the TSV and the bottom pad. The difference between the values can be explained by the different stress and direct current distributions at the bottom pad in the cylindrical and tapered TSV. Also, it can be noted from the results, that position D is the most vulnerable between the TSV and the top pad in both cases. [29]

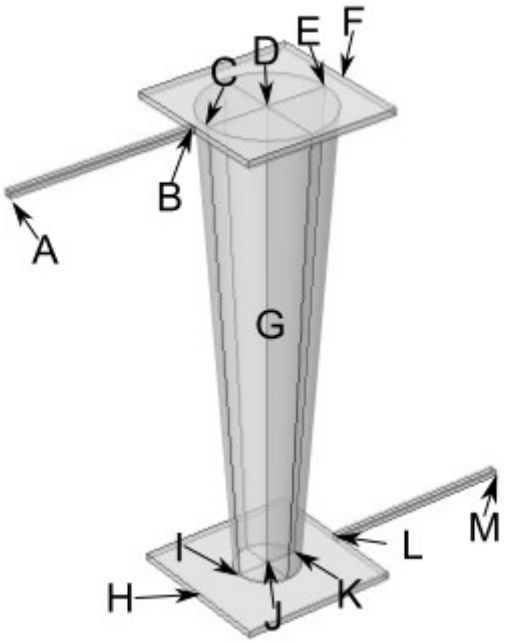

Figure 12: Points of interest in electromigration simulation. The values of the points are presented at the Table 3. [29]

Table 3: Mean Time to Failure (MTTF) for tapered and cylindrical TSV. The alphabets match the ones in the Figure 12. [29]

	Mean Time to Failure (10^8s)												
Position	A	B	C	D	E	F	G	H	I	J	K	L	M
Tapered	>10	0.45	0.05	0.04	0.08	0.3	0.4	1.4	0.03	0.05	0.03	2.0	>10
Cylindrical	>100	3.1	3.2	0.9	2.0	1.9	0.6	2.0	0.7	0.2	17.2	32.5	>100

It has been reported [49] that thermo-mechanical stress gradient is dominant factor to electromigration performance instead of current density in TSVs. During thermal cycling tests high localized stress points appear at the interconnection of the TSV and the contact pad. These stress points are expected to have negative impact on electromigration performance. Thus, reducing the thermal stresses will improve reliability. It was also reported that the geometrical dimensions and the metallization schemes of the TSV structure have a significant impact on electromigration performance. Dimensions affect the current densities in the structure while the metallization that do not cover vias fully worsens reliability. [49]

The amount of current crowding at the intersection of TSV and the landing pad depends on the relative ratio of the TSV diameter to the landing pad size. For example, if the diameter of the via is 5 µm, there will be less current crowding at the corners of the intersection if the thickness of the pad is 3 µm compared to the pad thickness of 1 µm. Thus, slightly thicker pad at the intersection reduces the effects of electromigration. [50]

Electromigration performance of the tapered and cylindrical TSV can be examined with the down-stream and up-stream configuration presented in Figure 13. The results from the experiment [40] indicate that the voiding happens in the metallization (M_{TOP} and M_{BOT}) at the interfaces. The formation of the void happens when copper atoms are driven off from the metallization by the electron flow. When the void at the interface grows larger than the conductive section of the via the resistance increases greatly. This forces the electrons to flow through the high resistive barrier layer. [40]

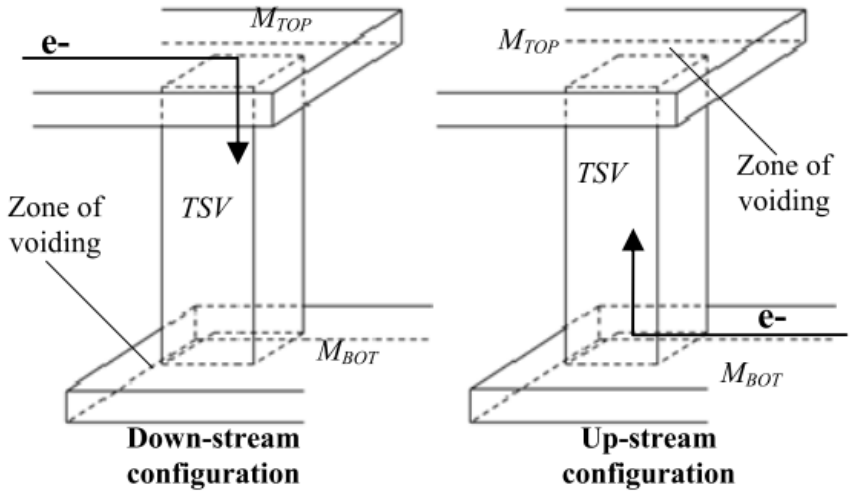

Figure 13: Down-stream configuration (on the left) and up-stream configuration (on the right) for the electromigration testing. [51]

Several studies [40] [49] [52] [51] have reported that TSVs are resistant to the electromigration induced voiding. The voids were exclusively found at the intersection of copper contact pad and the TSV.

4.2. The time dependent dielectric breakdown

A dielectric material is an electrical insulator that exhibits weak polarization when exposed to an externally applied electric field. In semiconductor industry, low dielectric constant (low-κ) dielectrics are materials with lower dielectric constant than that of silicon dioxide. These materials are used as insulators in multi-level copper damascene interconnects in order to reduce the resistance-capacitance delay (latency), crosstalk and dynamic power dissipation. [53]

The time dependent dielectric breakdown (TDDB) refers to a phenomenon, in which the loss of insulating properties of dielectric occurs, when it is subjected to voltage/current bias and temperature stress. The failure happens as a result of a long-time exposure to relatively low stresses. It usually turns out as an abrupt and irreversible increase in leakage current. TDDB is often used method to evaluate the integrity of copper/low- κ systems. [54]

4.2.1. Time dependent dielectric breakdown lifetime analysis

Time dependent dielectric breakdown lifetime analysis is done by obtaining dielectric failure times at different stress fields E. Then one of the several field acceleration models is used to estimate the failure time at operating field. This is done by extrapolating median failure time $t_{50\%}$ obtained at a higher field to a lower field. The one of the most commonly used field acceleration models is the E-model which can be expressed as follows:

$$t_{50\%} \propto e^{-\gamma E} \tag{10}$$

where $t_{50\%}$ is median failure time, E is the electric field and γ is called field acceleration factor, which is the key parameter when estimating the dielectric reliability. Basically, high field acceleration factor value means good dielectric reliability and thus long lifetime when extrapolated to operating condition [55]. As can be seen from Figure 14, high value of $t_{50\%}$ equals high γ. Likewise, low $t_{50\%}$ equals low γ. Thus, the structure has better TDDB reliability the higher the value of $t_{50\%}$ is. [56]

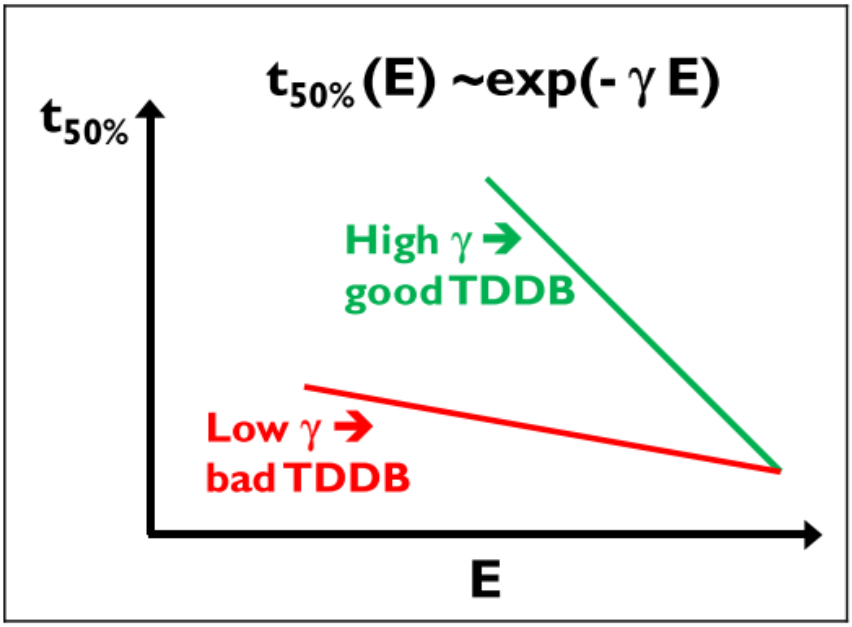

Figure 14: $t_{50\%}$ as a function of electric field, indicating impact of γ on reliability. [56]

4.2.2. Time dependent dielectric breakdown in TSVs

In TSVs dielectric breakdown happens when copper contamination occurs in silicon oxide insulation layer causing reliability issues. This copper contamination can be caused by atomic diffusion at high temperatures, for example during annealing processes, and by copper ion drift under biased thermal stress. The copper ion drift happens under the influence of electric field causing rapid drift of copper ions through silicon oxide layer during the operation of IC chips even at low temperatures in which the diffusion of copper is insignificant [57]. Seo et al. [58] proposed that the breakdown of insulation layer in their study is caused by thermal cracking followed by fast drift of copper ions through the cracks. Seo et al. [58] used biased thermal stress, temperature was at 250°C and electric field of 2 MV/cm was applied through the structure, which ionized copper atoms and then injected them into the cracks causing conductive paths. Figure 15 presents dielectric breakdown caused by copper ion drift under biased thermal stress. [58]

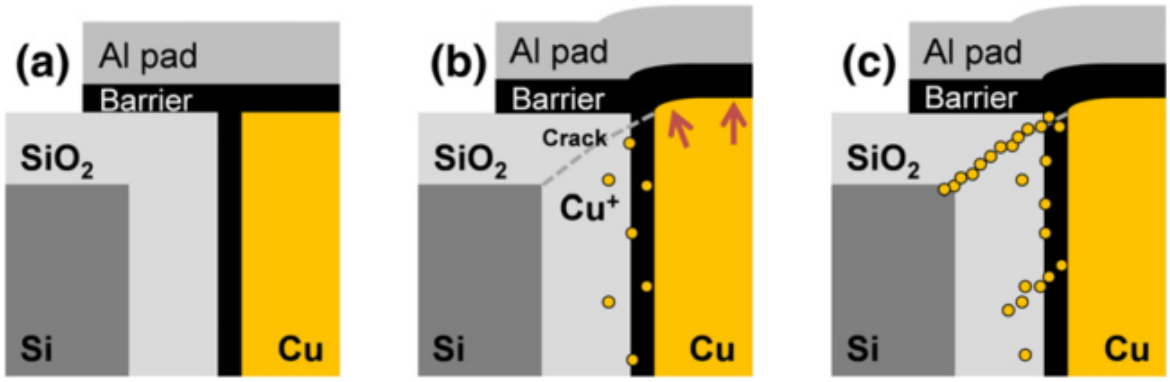

Figure 15: Failure of the insulation layer due to thermal cracking followed by copper ion drift. (a) TSV structure under no external stresses. (b) Generation of cracks due to thermal stresses. (c) Insulation layer breakdown by conductive copper path along the crack. [58]

It is extremely hard to use standard TDDB measurements in TSVs, because of non-uniformity in layer thicknesses caused by rough sidewalls of the vias. These factors cause significant variations in obtained failure times even if the stress fields are the same. Hence, such tests are impractical for TSV applications. [56]

A controlled I-V method has been proposed [59] to accurately determine TDDB field acceleration parameters. In practice, the method uses varying ramp rates R_r of I-V sweeps to obtain breakdown fields E_{bd}. The parameter γ can then be obtained from Figure 16

$$E_{\mathrm{bd}}(R_r) = E_{\mathrm{bd}}(R_0) + \frac{1}{\gamma}\ln\left(\frac{R_r}{R_0}\right), \tag{11}$$

where R_0 is a reference ramp rate. [56]

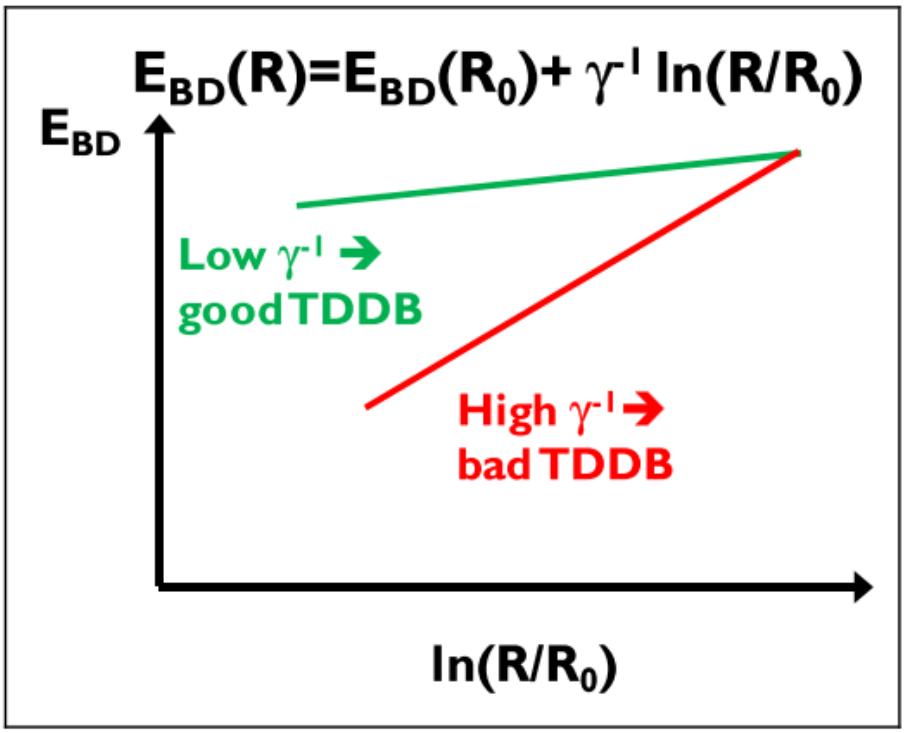

Figure 16: E_{bd} as a function of $\ln(R/R_0)$. Gives estimation of γ. [56]

4.3. Diffusion of copper in TSVs

Diffusion is a process in which the atoms move along the concentration gradients from high concentrations areas to low concentration areas [60]. In TSVs, the problem is the diffusion of copper into active silicon region. This contamination may cause electrical degradation in a device. The diffusion also creates voids in copper region. The barrier layer is deposited in the fabrication process to prevent the diffusion, but sometimes the layer is either poorly deposited or damaged and therefore unable to prevent the diffusion. [17]

A transient capacitance measurement, which is called capacitance-time (C-t) analysis, is suggested as an electrical evaluation method to measure the effects of copper contamination in the active silicon region. With this method one can electrically characterize the lifetime degradation of minority carriers caused by diffusion of copper into active silicon region. [61]

Lee et al. [61] examined the effect of sidewall scalloping and barrier layer thickness on diffusion reliability with capacitance-time analysis. TSVs were fabricated with different average sidewall roughnesses, 30 nm and 200 nm, and with different sputtered tantalum barrier layer thicknesses, 10 nm and 100 nm. Because of the sidewall roughness, the minimal barrier layer thicknesses in TSVs were approximately 3 nm and 30 nm when the sputtered layer thicknesses were 10 nm and 100 nm respectively at the surface. [61]

In order to get the copper to diffuse, the samples were annealed for different periods of time. It was found out that when annealed, the samples with 10 nm thick barrier layer did not prevent the diffusion of copper into silicon region in either 30 nm or 200 nm average sidewall roughness. On the other hand, the thickness of 100 nm was sufficient to prevent diffusion, even when the samples were annealed for 60 min at 300^{o}C. When they raised the annealing temperature to 400^{o}C, they started to see the degradation of the performance even in the thick barrier layer. This caused rapid copper diffusion into the silicon region. Therefore, the copper diffusion is a more serious issue, when there are multiple annealing processes in fabrication. All in all, capacitance-time analysis was found to be a very useful method to characterize electrically and quantitatively the influence of copper contamination on TSV reliability. [61]

Civale et al. [62] found out in their study that both 5 nm thick tantalum barrier layer and 10 nm thick titanium barrier layer proved to be reliable against diffusion even after thermal ageing at 420^{o}C. This was observed with capacitance measurements. However, it was discovered that 5 nm thick titanium layer was degraded during the thermal ageing. [62]

4.4. Thermal reliability

Thermal expansion is the general increase or decrease in volume of the material, when the temperature changes. Different materials have varying responses to temperature change. This characteristic of the material is expressed as its coefficient of the thermal expansion and it usually varies with the temperature. [63]

A thermal mismatch strain happens at the interface of the different materials. The magnitude of the strain between materials depends on the values of the coefficients of thermal expansion. This can be expressed as follows:

$$\varepsilon = (\alpha_a - \alpha_b)\Delta T \tag{12}$$

where ε is thermal mismatch strain, α_a and α_b are coefficients of thermal expansion of two different material and ΔT is the change in temperature. If $\alpha_a > \alpha_b$, the strain is tensile and If

$\alpha_a < \alpha_b$, the strain is compressive. Tensile strain pulls the surface from the body of the material while compressive strain pushes the surface into the body of the material. [63]

Thermal stress σ in the centre region of the substrate is given by

$$\sigma = (\frac{E_y}{1-\nu})\varepsilon \quad (13)$$

where ν is the poisson ratio, E_y is the Young's modulus and ε is thermal mismatch strain.

4.4.1. Thermal reliability of TSVs

TSVs are one of the key technologies for three-dimensional stacking. However, power dissipation must be carefully planned in three-dimensional stack because hot spots can easily occur. It has been reported [64] that the thermal hot spots can cause three times higher temperatures in three-dimensionally stacked IC structures with TSV interconnects when compared with two-dimensionally stacked IC structures. The reason for the higher temperature in three-dimensional structures lies in the increased power densities and proximity of the dies. These high temperatures have an influence on the reliability and electrical characteristics of the devices [65]. [64]

The differences in thermo-mechanical properties between copper and silicon can lead to substantial stresses at the interfaces of TSVs. In high temperatures, copper expands and contracts more than five times as much as silicon. Thermal expansion coefficient is 3.05 (ppm/^{o}C) for silicon and 17.7 (ppm/^{o}C) for copper. When the temperature is ramping up, axial expansion of copper causes high shear stresses to silicon and to silicon dioxide layer causing delamination at the interfaces. Simultaneously, the radial expansion of copper causes compressing stresses to silicon and to silicon dioxide. However, aforementioned compressive stress does not contribute to the driving force for delamination. [66]

During the heating phase (ΔT>0), which is presented in Figure 17, the interfacial delamination crack is only caused by an axial shear stress σ_y as mentioned earlier. However, during the cooling phase (ΔT<0), which is displayed in Figure 18, driving force for delamination is a combination of a radial tensile stress σ_x and axial shear stress σ_y. This is due to the peeling effect that the contraction of copper causes at the interface. Because of this, the stresses in the cooling phase are usually higher than in the heating phase. [67]

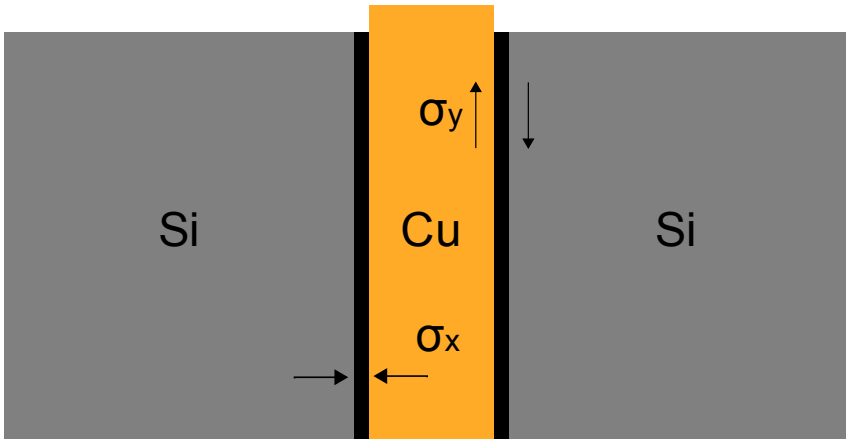

Figure 17: Stresses in the TSV structure during the heating phase.

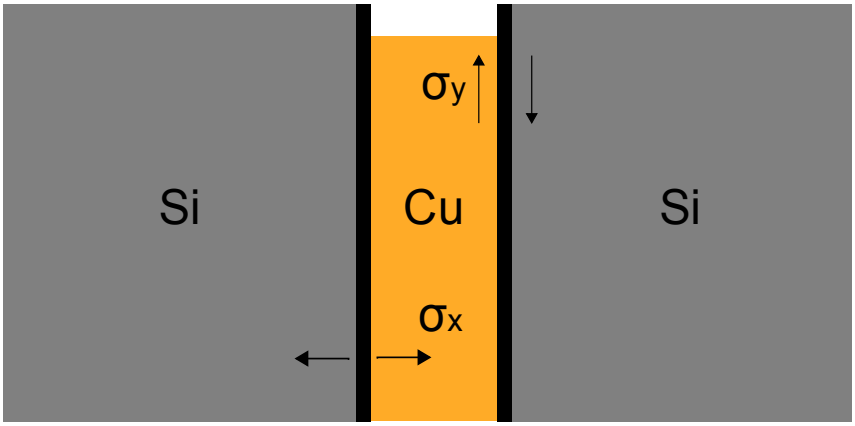

Figure 18: Stresses in the TSV structure during the cooling phase.

There are two critical failure points. Firstly, the failure may occur due to the shear stresses at the top and bottom edges of the via between the copper and dielectric layer interface. Cracking only happens between the copper and the dielectric layer. This is due to greater mismatch in thermal expansion coefficients between copper and dielectric layer than between the dielectric layer and silicon substrate [67]. Secondly, cracking of copper or silicon dioxide could happen at the midpoint of the TSV. This cracking may propagate due to thermal stresses and thus cause the failure of the entire structure. [66]

A larger via diameter results in a larger thermal stress in the structure because the volume of copper also increases when the diameter of via increases. Thermo-mechanical stresses can be reduced by partially filling the vias, thus increasing the reliability [14]. Stress in surrounding silicon substrate decreases with the distance from the via [68]. [69]

4.4.2. Thermal cycling tests for TSVs

Thermal cycling tests are usually run according to JEDEC JESD22-A104 standards. A thermal cycling test determines the ability of the test subject to withstand exposure to low and high temperatures, while maintaining its operational capabilities. Both thermal cycling and thermal shock tests accelerate temperature related fatigue failures depending on temperature ranges, the transfer time and the dwell time between the low and the high temperature. [70]

Thermal cycling tests may cause different types of damage in the TSVs structure, such as front metallization thickness reduction due to oxidation, voids inside of TSVs, cohesive cracking in silicon substrate, cracks at the bottom metallization-damascene silicon dioxide interface, cracks at the interfaces of the TSVs and the metallizations and cracks at the sidewall interfaces between TSV and dielectric layer [39]. Thermal cycling promotes the growth of the defects. This is due to high stress localization at the tip of the defect which causes plastic deformation. [66] Cohesive cracking in silicon and interfacial delamination between the copper and the dielectric layer are presented in Figure 19.

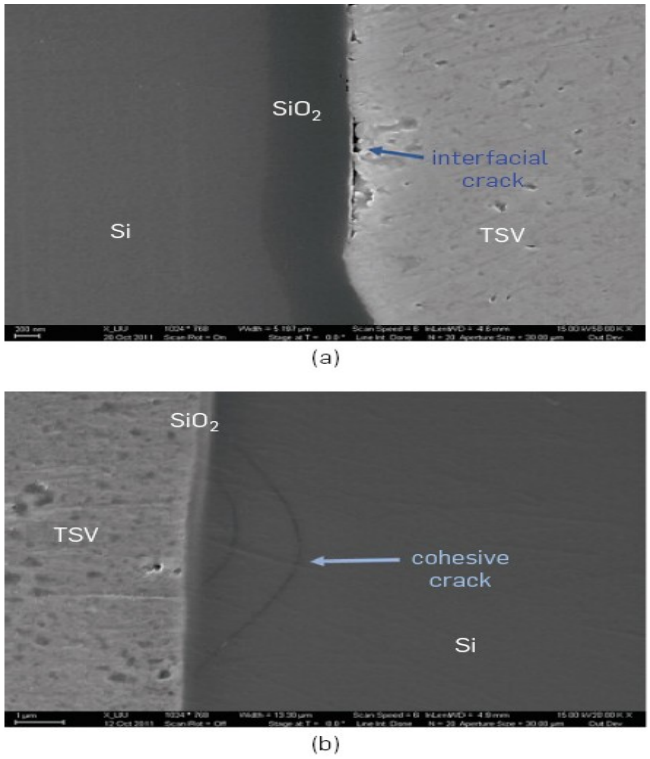

Figure 19: Crack growth due to thermal stresses. (a) Interfacial crack between dielectric layer and silicon substrate. (b) Cohesive crack in silicon substrate. [71]

Pre-existing defects at the sidewalls, mostly pinholes, act as nucleation point for crack propagation during thermal cycling. Cracks at the sidewalls cause two serious failures in TSV: diffusion of the copper into active silicon and current leakage through the active silicon. These cracks can also propagate along the interface between TSV and the top/bottom metallization as well as between the interface of the TSV and dielectric layer causing other kind of failures. The crack propagation after thermal cycling at the interface of the bottom metallization and TSV is presented in Figure 20. Cracks are formed at the edges of the via and then high stresses cause them to propagate inwards through the via filling. [39]

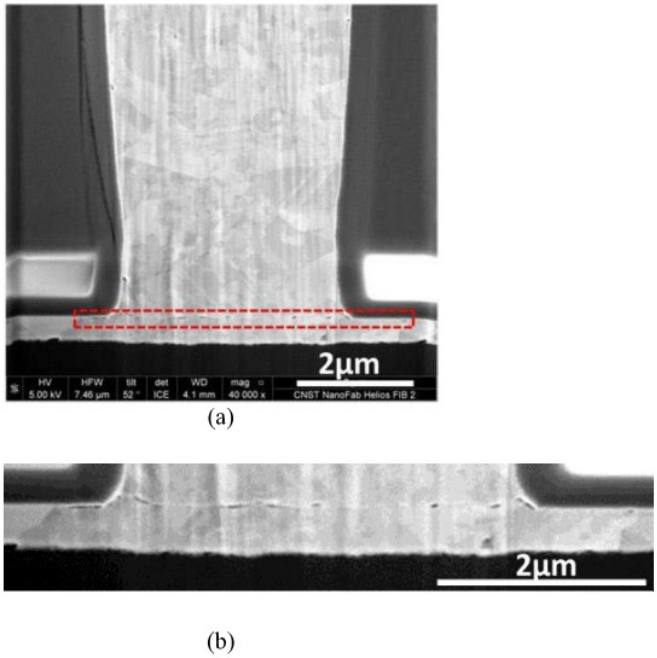

Figure 20: (a) Crack propagation after thermal cycling at the interface of the bottom metallization and copper filling. (b) Magnification of the crack. [39]

The cracks inside the copper are initiated from voids. Thermal residual stress can lead to the growth of these defects. However, it is usually hard to determine whether thermal cycling causes the formation of the voids or the voids originate from the fabrication process. On the other hand, it has also been reported [2] that the thermal strains alone are not high enough to cause failures in the copper region. However, when these strains are combined with fabrication imperfections, such as voids and cracks, failures in copper region might happen [2]. [39]

The front metallization thickness reduction due to oxidation can be studied by carrying out thermal cycling test in air. The front metallization thickness reduction has been observed to cause a noticeable increase in resistance. The reduction of the thickness is caused by the roughening and voiding of the surface due to its oxidation. The metallization can be passivated which can mitigate the oxidation. [39]

Frank et al. [40] reported that during thermal cycling test no sample was found to fail due to a crack initialized at a void during 500 cycles test between -65^{o}C and 150^{o}C. The examined structures had fully filled Kelvin TSVs in a silicon substrate and diameters of TSVs were 2-4 µm and the depth was 15 µm. It was also reported that thermal cycling and thermal storage did not build up any stresses at TSV interfaces that affected electromigration failure rate. It was deduced that thermal cycling durability is not a critical concern for mature high density via-last TSVs. It is concern only in the TSVs with initially imperfect structures. [10]

4.4.2. Annealing

When the temperature is below the recrystallization point, metal recovers completely from the thermal stresses if there is enough recovery time. This means that there will not be permanent changes in the microstructure of the material when the strain is removed. In higher temperatures, grain growth happens. The microstructure and the properties of the material change. The longer the material is exposed to the heat, the more the microstructure changes. The recrystallization point of copper is 250°C. [25]

High temperature tests are a field of interest in TSV reliability studies because annealing is a common fabrication step in semiconductor industry. Annealing is used to reduce internal stresses inside of metals and to stabilize the material against thermal stimuli. High temperatures cause copper to expand profusely without complete recovery at the lower temperatures. This causes plastic deformation in the copper. Copper is surrounded by silicon substrate in TSVs which causes copper to expand only vertically. This causes copper protrusions. These protrusions can cause mechanical failures, such as cracking or lifting in dielectric layers. [25]

The protrusion height strongly depends on the annealing temperature but it is not a linear function of temperature. This means that there are also other factors affecting the height of the protrusions than temperature. The protrusion height can be theoretically lowered by making the diameter of the via smaller. This would lower the amount of copper and thus decrease the thermal expansion force in high temperatures. Also, the relative surface area would increase, which would enhance the adhesion force between copper and silicon dioxide. Thus, the formation of copper extrusions decreases. The protrusion of copper and the delamination of sidewalls strongly depend on TSV dimensions. Theoretically this can be expressed with equations

$$\Delta h \propto (\alpha_{Cu} - \alpha_{Si}) \cdot \Delta T \cdot h \tag{14}$$

$$(\text{relative surface area}) = \frac{2}{r}, \tag{15}$$

where Δh is the height of extrusion, h is a depth of TSV and r_r is the radius of TSV. [69]

After the electroplating process, copper exhibits a high defect rate with many small grains. Also the orientation of the grains is random. This kind of structure causes protrusions because noticeable grain size increase takes place in high temperatures. In order to stabilize the structure and to prevent protrusions, additional annealing step during fabrication is needed. [25]

Annealing process before CMP stabilizes the copper in a low-stress condition in TSVs. Heryanto et al. reported [65] that as long as the temperature of the annealing is higher than the temperatures in the following processes, there should not be any protrusions. For example, if the sample is annealed at 400°C and the protrusions are removed with CMP process, there should not be any protrusion in re-annealing processes if the temperature is kept below 400°C. If the temperature is

400°C or more, protrusions will occur. Sometimes, diffusive creep causes small copper protrusions during the second anneal process. Diffusive creep occurs due to the different concentration gradients along the TSV. [65]

Heryanto et al. [72] carried out an experiment in which they observed the behavior of TSV structures in high temperatures. They kept the samples at different temperatures, ranging from 25°C to 450°C, for 30 minutes. They discovered that the protrusion height increases with the temperature. The increased dwell time also had an increasing effect on the height of the protrusion. Furthermore, the shape of the protrusion alters with the increase in the annealing temperature. At the highest temperature the height of the protrusion was measured to be 958 nm. The diameter of the TSV was 5 µm and the height was 50 µm at the beginning of the test. They also noticed that the protrusions come visible starting from 350°C and they may form either at the center or at the edge of the TSV. [72]

Even though, it is well documented that the height of the protrusions is dependent on the peak temperature, it is hard to predict the shape of the protrusions. The protrusion may have multiple peaks and they vary randomly from one TSV to another. Zhang et al. [73] came to a conclusion that the grain boundaries, which vary significantly between TSVs, are most likely the biggest factor affecting the shape of the protrusions. [73]

4.5. Finite element method

Finite element method (FEM) is a structural simulation technique widely used in different industrial applications. FEM was first used in applications in structural analysis and aeronautical engineering in the 1950s. In these fields the failure could be costly and even fatal. Since then FEM has become an industry standard for simulating the behavior of complex structures. FEM can be used to determine any points of weaknesses in a design before it is manufactured. Thus, it is an important part of the reliability analysis. After the critical points are identified, the designing efforts for reliability can be focused on known problem spots instead of whole structure. [74]

The finite element modeling is a numerical technique to analyze any shape or geometry, any material properties, any boundary conditions and any loading conditions. FEM is a dominant discretization technique in structural mechanics. The basic concept of the method is to reduce the number of degrees of freedom to a finite number. This gives components a simple geometry called finite elements. Each of these elements can be given the response in terms of a value of an unknown function or functions. These elements are connected to each other by nodes. The response of the whole structure can be approximated by assembling all of the elements. [75]

Finite element method simulation consists of four main steps: modeling the geometry of the desired structure, meshing the structure to numerous simple geometry components, defining different material sections from the structure and giving those correct material properties and finally specifying boundary, initial and load conditions. The finer the mesh the more accurate simulation results are obtained. On the other hand, the simulation time increases with more complex and defined structures. [76]

4.5.1. Finite element analysis of TSV structures

Finite element analysis (FEA) is often carried out in order to study the stress profile of the TSV structure during thermal testing. Simplified two-dimensional TSV models provide the information of maximum stress areas in the structure. Figure 21 (a) presents a simplified two-dimensional finite element mesh structure of TSV and Figure 21 (b) presents stress distribution along the simplified TSV structure during the heating phase. Simplified TSV models consist of copper and surrounding silicon regions. In addition, insulation layer can be added and via profiles can be altered in simulations in order to find out their impact on stresses in the structure. [65]

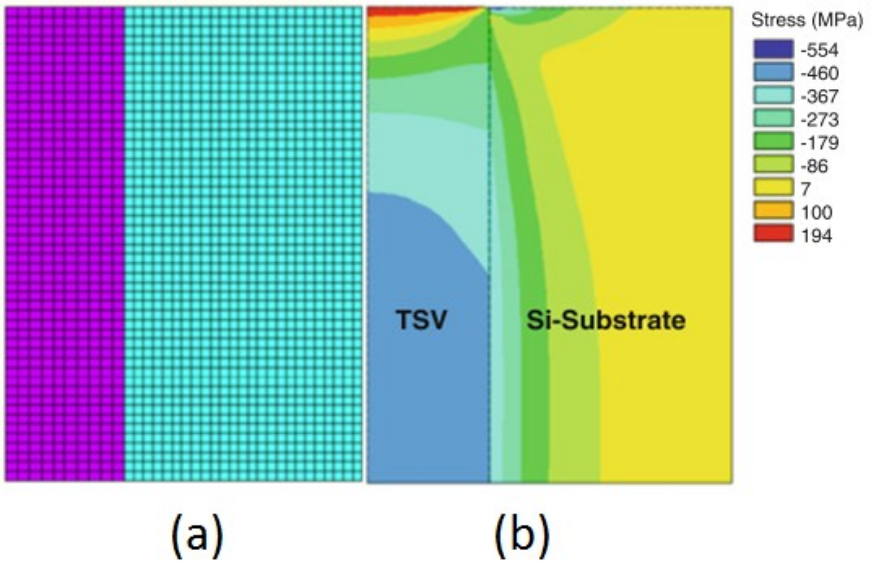

Figure 21: (a) Two-dimensional finite element mesh description of the TSV structure. (b) Stress distribution along the TSV during temperature ramp-up phase. [65]

In order to investigate thermal stress distribution in a TSV array, three dimensional finite element analysis models are used. For instance, keep-out zone design can be optimized by arranging TSV arrays according to information provided by three dimensional FEA models. Figure 22 presents normal stress σ_x distributions in TSV arrays. It can be seen that different array orientations have significant effect on keep-out zones that are highlighted by rectangles. In Figure 22 (b) keep-out zones are smaller than in Figure 22 (a), even though TSV density is the same in both cases. [68]

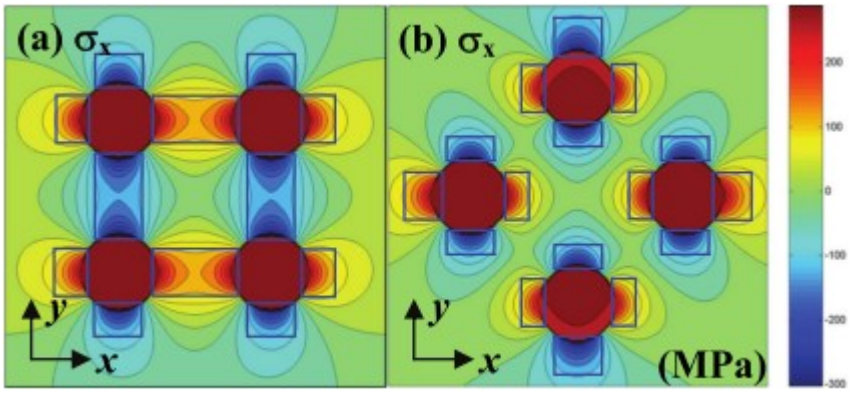

Figure 22: Keep-out zones in TSV arrays outlined by rectangles. [68]

Stress interactions between two TSVs can also be examined with three dimensional models. When two TSVs are aligned along the y-axis, the normal stress σ_x is intensified and shear stress σ_{xy} is suppressed in the space between two TSVs. This can be seen in Figure 23 (a) and in Figure 23 (b). However, when two TSVs are aligned in diagonal direction, normal stress is suppressed and shear stress is intensified in the space between two TSVs as shown in Figure 23 (c) and in Figure 23 (d). These results indicate that stress interactions are directionally dependent and they can be minimized if the TSV arrays are arranged accordingly. [68]

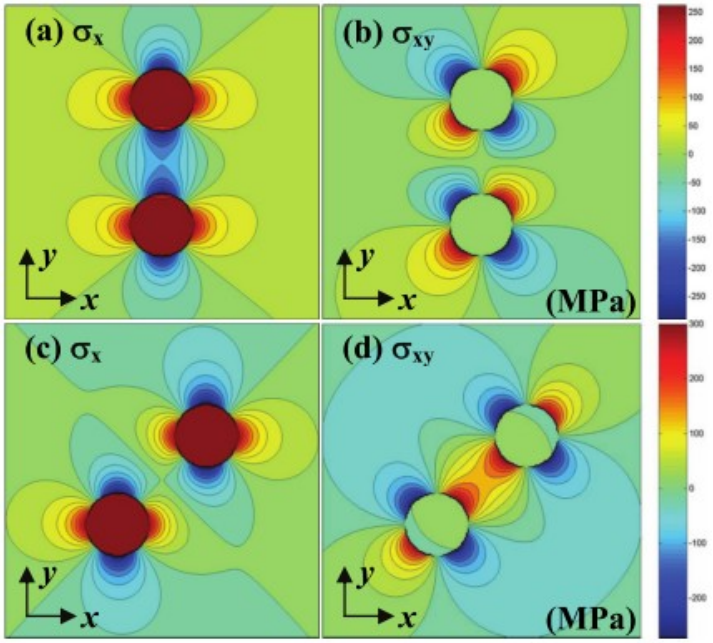

Figure 23: Thermal stress interaction between two TSVs. [64]

As well as thermal stress distributions, current density distributions in TSVs can be examined with finite element analysis models. These models provide the information of durability of the structure against electromigration. An example of current density distribution in cylindrical TSV is presented in Figure 24. [29]

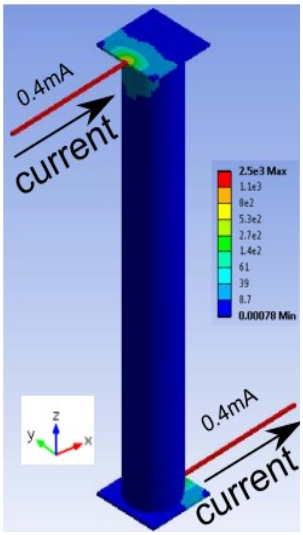

Figure 24: Current density (mA/µm^2) distribution in a cylindrical TSV. [29]

4.6 Weibull probability distribution

In this section, the Weibull probability density function and cumulative density function are discussed. Also, the function parameters and their estimations are discussed.

4.6.1. Background and benefits of the Weibull analysis in reliability assessments

The reliability is expressed in terms of probability, which can be described by a distribution. The one of the most often used distribution was published by Waloddi Weibull in 1939, which is nowadays called Weibull distribution [77]. The Weibull distribution is widely used in reliability engineering and lifetime analysis because of its versatility. Another advantage of Weibull analysis compared to the other methods is that the Weibull distribution fits a broad range of life data. [78]

In order to determine the reliability of the population of units, estimations are made based on examined samples. The exact reliability value of the population is not known since it would require analyzation of failure data of every single unit in the population which is rarely a realistic option. The Weibull analysis makes it possible to achieve engineering objectives with very small sample sizes. This is a clear advantage, when the cost of the samples is very high. Naturally, small sample sizes always cause uncertainties. To evaluate these uncertainties, confidence methods are used. If confidence bounds are employed, a range is obtained within which the reliability issues are likely to occur a certain percentage of the time. This range of values is called a confidence interval. For instance, if the confidence interval is 95 %, there is 5 % probability to observe a failure outside of the interval area. [78]

4.6.2. Weibull parameters and probability functions

The most often used distribution for life data analysis is the two-parameter Weibull distribution. The Weibull cumulative distribution function (CDF) provides the probability of failure up to the time *t* in percent:

$$F(t) = 1 - \mathrm{e}^{-(t/\eta)^{\beta}} \tag{16}$$

where t is failure time, η is characteristic life or scale parameter and β is slope or shape parameter. [78]

In addition to two-parameter Weibull distribution, there is also a three-parameter distribution. The third parameter is a starting point/location parameter which is denoted by t_0. In two-parameter Weibull distribution the value of t_0 is zero. Three-parameter distribution can be used to better fit the curved probability function to the data in analysis in which the time does not start from zero. For instance, failures might not happen early in the test, in which case the location parameter can be used to move the distribution function along the x-axis without affecting the shape of the distribution. Three-parameter Weibull cumulative distribution function is as follows:

$$F(t) = 1 - \mathrm{e}^{-((t-t_0)/\eta)^{\beta}} \tag{17}$$

where t is failure time and t_0 is starting point or origin of the distribution. [78]

There are certain criteria that should be met before using three-parameter Weibull: the Weibull plot should show curvature, there should be an explanation why the failures cannot occur before time t_0, a large sample size of minimum 20 failures should be available and correlation coefficient should be higher with three-parameter than with two-parameter Weibull distribution. [78]

The slope parameter indicates the kinds of failures: β < 1.0 means infant mortality failures, β = 1.0 means the failures are independent of age and are random and if β > 1.0 the failures are caused by wear. A change in the scale parameter η has the same effect on the distribution as a change of the time scale. When η is increased while keeping β constant, the probability density function stretches out along the x-axis and decreases in height in y-axis. This is because the area under the probability density function is always one. The value of the scale parameter indicates the moment at which 63,2 % of all subjects are failed. This is the case for all Weibull distributions regardless of the shape parameter β. [78]

4.6.3. Weibull parameter calculations and data plotting

The most popular approach to estimate the Y-axis plotting positions is a median rank. There are other plotting position methods but the median rank is considered as the most accurate. The first

step in order to plot the data is to give every sample an order number according to the failure time. The sample that breaks first is assigned as number one; the second is assigned as number two and so on. If more than one failure is detected at the same time, they are plotted at different median rank values on the Y-axis as a function of the failure time. [78]

Median rank regression uses a best-fit straight line through the plotted data to estimate Weibull parameters. The best-fit line is determined with the least squares method. Benard's Median Rank can be used to approximate the median rank values. It is sufficiently accurate for plotting and estimating the parameters. The equation is

$$\text{Benard's Median Rank} = \frac{i - 0.3}{N + 0.4} \tag{18}$$

where *i* is the adjusted rank of the failed sample and *N* is the sum of failures and suspensions. Failure times and median ranks are transformed as in Equation (19) and Equation (20):

$$Y = \ln(\text{Failure time}) \tag{19}$$

$$X = \ln\left(\ln\left(\frac{1}{1 - \text{Median Rank of } Y}\right)\right) \tag{20}$$

The method of least squares is used to estimate A and B from equation

$$Y = A + BX \tag{21}$$

The median rank regression estimates of the Weibull parameters are presented in Equation (22) and Equation (23).

$$\beta = \frac{1}{B} \tag{22}$$

$$\eta = e^{A} \tag{23}$$

B can be calculated from the equation

$$B = \frac{\sum_{i=1}^{n} x_i y_i - \frac{\sum_{i=1}^{n} x_i \sum_{i=1}^{n} y_i}{n}}{\sum_{i=1}^{n} x_i^2 - \frac{\left(\sum_{i=1}^{n} x_i\right)^2}{n}} \tag{24}$$

The correlation coefficient r measures linear relationship between two variables. The closer the value of r is to one the better the linear fit. The 90 % critical correlation coefficient (CCC) is used in Weibull analysis to measure the goodness of the fit. If the correlation coefficient is larger than CCC you have a good linear fit. Otherwise, you have a bad linear fit. The correlation coefficient squared is called the coefficient of determination r^2. This is considered to be a better option than correlation coefficient to measure goodness of a fit. The coefficient of determination is equal to the proportion of the variation in a data. For instance, if r^2 is 95 % it implies that 95 % of the variation in the data is explained by the fit of the data line. [78]

The correlation coefficient *r* can be calculated with the Equation (25) and the proportion of the variation in the data r^2 can be easily calculated from the result of the equation.

$$r = \frac{\sum_{i=1}^{n} x_i y_i - \frac{\sum_{i=1}^{n} x_i \sum_{i=1}^{n} y_i}{n}}{\sqrt{\left(\sum_{i=1}^{n} x_i^2 - \frac{\left(\sum_{i=1}^{n} x_i\right)^2}{n}\right)\left(\sum_{i=1}^{n} y_i^2 - \frac{\left(\sum_{i=1}^{n} y_i\right)^2}{n}\right)}} \tag{25}$$

5. Failure analysis of TSV

Stress characterization of the TSV usually has three main approaches. The first one is the FEA simulation which compares theoretical data and measured data using thermo-mechanical coupled analysis. The second approach is direct experiments, such as Raman microscopy and XRD, to make quantitative assessments of the stresses. These stresses can be, for instance, caused by temperature changes during thermal cycling tests. The last approach is to perform a microstructure analysis in order to verify failure point, mode and mechanism. This includes methods like EBSD, FIB and SEM. [79]

In this section common TSV sample preparation and imaging techniques are shortly introduced.

5.1. Electron microscopies and electron backscatter diffraction (EBSD)

5.1.1. Electron microscopies

Scanning electron microscope (SEM) produces images by scanning the specimen with a beam of electrons. The electrons that are produced by an electron gun collide with the specimen. These are called primary electrons. When the primary electrons collide with the sample, the penetration of the electrons is directly dependent on the energy of the electrons and inversely dependent on the atomic number of the atoms in the sample. The collision causes ionization of the atoms which leads to electron emission from the sample. The electrons that are ejected from the sample due to the collision are called secondary electrons. Detection and analyzation of ejected electrons is called secondary electron imaging. Some primary electrons scatter due to elastic collision with the sample. These are called backscatter electrons (BSE). BSE can be used to get the information about the distribution of the different materials in the specimen. The specimen has to be electrically conductive in order to be imaged with SEM. The non-conductive samples are coated before the imaging. [80]

Transmission electron microscopy (TEM) is method that uses a beam of electrons to transmit through the sample. The image is formed based upon the interactions of the transmission electrons and the specimen. The samples have to be very thin and the preparation is difficult. The TSV via structure can be analyzed at different depths with transmission electron microscope [40].

Cross-sectional images are crucial in order to inspect the quality of the fabrication of TSVs or the results of reliability testing. Focused ion beam (FIB) milling is the most used method to prepare cross-sections of the samples. After milling, it is possible to use scanning electron microscope (SEM) for imaging the cross-section. In addition, microstructure analysis can be made with electron backscatter diffraction (EBSD).

5.1.2. Electron backscatter diffraction

Copper annealing behavior can be studied with electron backscatter diffraction (EBSD) measurements. It is a scanning electron microscopy technique and it is based on the detection of the diffracted accelerated electrons. The diffraction is caused by crystal planes of the sample. The sample is placed in SEM chamber at a tilted angle, which increases the signal-to-noise ratio towards the phosphor screen. The diffracted electrons intersect with the phosphor screen and generate visible lines called Kikuchi bands. These patterns are effectively projections of the geometry of the crystal planes. This method enables obtaining grain sizes and crystallographic grain orientations from individual grains with high accuracy. EBSD images of annealed TSVs are presented in Figure 25. [81]

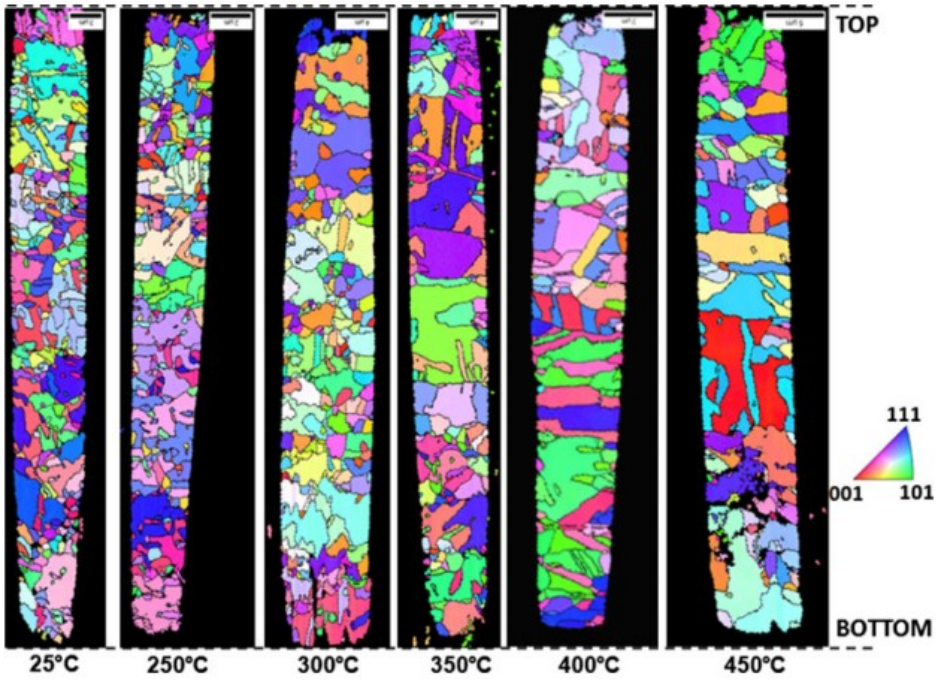

Figure 25: EBSD images of TSVs annealed at different temperatures. [65]

Sample preparation is a crucial part in EBSD. This is because the electrons diffract from the top 20 nm of the sample surface. If material near the surface is deformed, contaminated, or oxidized, then EBSD pattern formation may be suppressed. For instance, polishing has to be done carefully so that the crystal planes are not damaged. Any damage to the surface worsens the results or prevents them altogether. [82]

Due to the high tilt angle, surface topography causes shadowing. Because of this the surface has to be smooth and clean. ESDB samples are usually uncoated because the results come from the very top of the surface layer. This also can lead to charging problems with the samples. The polishing of the sample is usually made with mechanical polishing, chemical etching or ion beam milling. [82]

The most common polishing technique for the TSVs is FIB milling. Also, mechanical polishing has been used for the sample preparation in TSVs [25]. FIB milling is a very convenient technique because FIB-SEM systems can also equip EBSD. FIB smoothes the surface of the sample and

immediately after that the microstructure can be mapped with EBSD without breaking the vacuum. [72]

5.2. Stress measurement techniques

5.2.1. Raman spectroscopy

Raman spectroscopy is based on inelastic scattering of a monochromatic excitation light. Inelastic scattering means that the frequency of photons in the light changes after it interacts with the sample. The frequency of photons is shifted either up or down in comparison with the frequency of the excitation light. This is called the Raman Effect. The shift in frequency gives information about vibrational, rotational and other low frequency transitions in molecules. [83]

μ-Raman spectroscope is used in characterization of strains and stresses in TSVs after the heat treatment. It is a fast and non-destructive method that requires no sample preparation. The downside is that copper does not exhibit Raman signal so the measurements has to be carried out at the silicon substrate surface surrounding the TSV. Also, it is complicated to converse thermo-mechanical strains into Raman shifts. The measurement is done by focusing a laser beam on a silicon surface and scanning the point of interest. Thermo-mechanical strain in silicon causes a change in observed phonon frequency. From the scattered light, the characteristic Raman peaks are observed. These peaks are compared with the reference peak that is stress-free silicon. [13]

After TSV-induced stresses in surrounding silicon region are characterized, Raman stress map can be fabricated. An example of a Raman stress map of an isolated TSV is presented in Figure 26. Figure 26 illustrates a positive Raman shift in relation to stress-free silicon within 1-2 μm from the TSV, which indicates compressive stress. A transition to negative Raman shift is evident at greater distances, which indicates tensile stress. The largest measured compressive stress is around 90 MPa, whilst the largest tensile stress is around 30 MPa. [84]

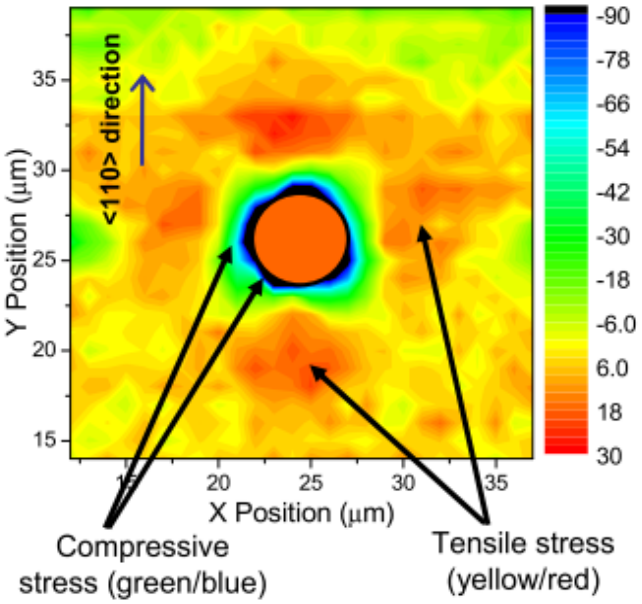

Figure 26: Two-dimensional Raman stress map of an isolated TSV. [84]

5.2.2. X-Ray diffraction

X-ray diffraction (XRD) can be used to measure stresses in the TSV structure. The technique is based on the analysis of the diffraction patterns caused by an interaction between X-rays and the atomic structure of the specimen. XRD measures the average stresses near the top of the TSV. [5] XRD yields averaged results that are inappropriate in the local assessment of stresses [79].

5.3. Surface inspection methods

Protrusions caused by annealing processes can be studied with a profilometer and an atomic force microscope (AFM). Both of these methods are capable of producing nanometer scale data. Heryanto et al. used 3D optical surface profilometer to conduct the measurements. It is a non-contact device that is used to measure wide range of surface heights. It employs two techniques: the phase-shifting interferometry (PSI) mode, which allows the measurement of smooth surfaces and small steps, and the vertical scanning interferometry (VSI) mode, which allows the measurement of rough surfaces. Both techniques use the same working principle: light that is reflected from a reference mirror interferes with light reflected from the sample to produce interference fringes. The fringe with the best contrast occurs at the best focus. Profilometers do not require sample preparations. Profilometer image of an annealed TSV array is presented in Figure 27. [65]

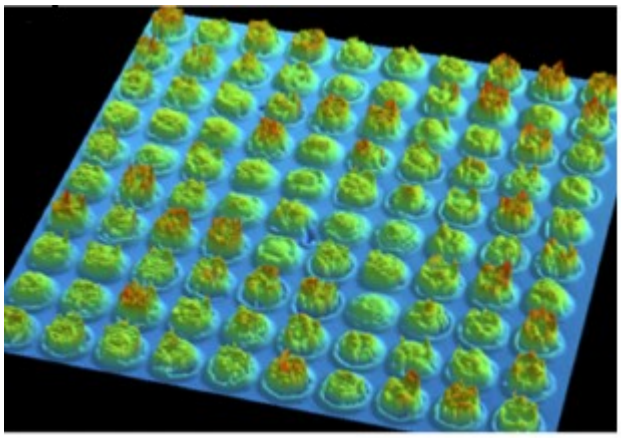

Figure 27: Three dimensional surface profilometer image of TSV array annealed at 400^{o}C. [65]

AFM is used to study the surface of the sample with high accuracy. The technique is based on the interactions between the scanning cantilever tip and the surface of the sample. When the tip is brought near the surface of the sample, the forces between the tip and the surface cause the deflection of the cantilever based on the topography of the sample. The deflection is measured using laser that reflects from the top surface of the cantilever into the array of photodiodes. Tip to surface distance is maintained by keeping constant force between them in order to avoid collision and thus damage to the sample or to the tip. [85]

In Figure 28 summary of different imaging and simulation methods used to study TSVs are presented.

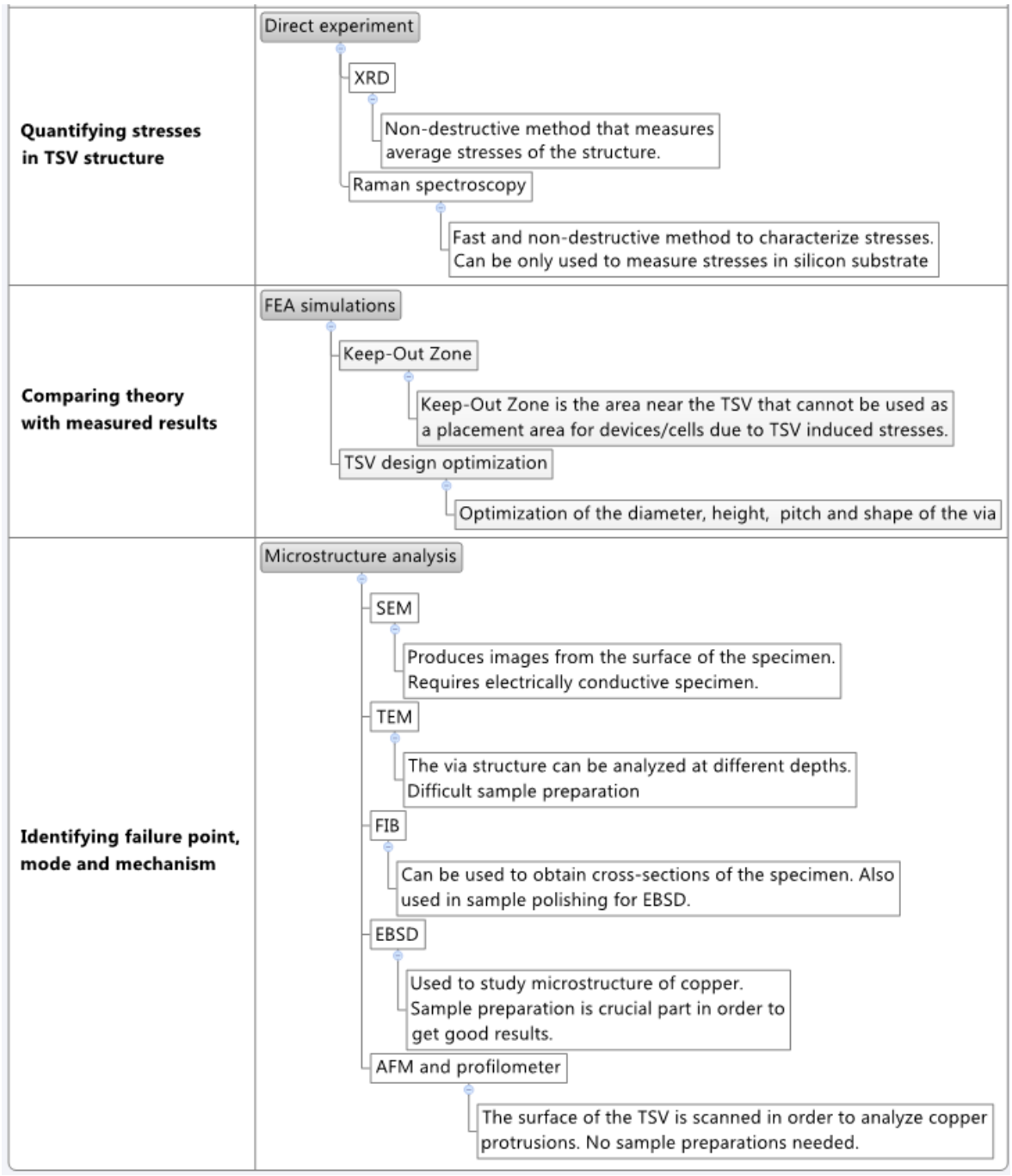

Figure 28: Summary of characteristics of different simulation and imaging methods used in examination of TSVs. (Modified from [79])

6. The purpose of the work

The purpose of this thesis is to carry out a literature survey and an experimental study concerning reliability of TSVs. The literature survey mainly focuses on different failure mechanisms of TSVs and how they can be examined and identified by different experiments and microstructural analysis methods. In addition, design and fabrication alternatives of TSVs are discussed and their impacts on reliability are presented. In the experimental section a lifetime assessment and failure analysis of tapered partially copper-filled blind TSVs is carried out. This is done by measuring the electrical performance of the TSVs during the temperature cycling test. The formation of open circuits is used as a failure criterion for the samples. There are not many lifetime assessments of any TSV profile reported in literature. Usually, the reliability tests are not carried out until failure. In this thesis Weibull reliability analysis is carried out in order to obtain the lifetime of TSVs and finite element analysis is performed to identify the critical failure locations of different TSV structures. The simulation results are compared with the imaging results and thus the origins of the failures can be determined.

7. Materials and methods

In this section the fabrication process of the examined wafer is introduced. Also, resistance measurement and thermal cycling test are presented.

7.1. Details of the fabrication and performed reliability tests of the test wafer

Test wafer was fabricated by VTT. The fabrication process of the test samples is presented in Figure 29. The fabrication process starts by growing 500 nm thick thermal oxide insulation layer on the device wafer (Figure 29(a)). This is followed by sputtering and patterning of 1000 nm thick aluminum (1 % silicon) metal layer on the backside of the device wafer to form RDLs (Figure 29(b)). After this the device wafer is bonded to the handle wafer with 10 µm thick SINR polymer adhesive (Figure 29(c)). The tapered vias are formed with SF_6/O_2 plasma etching in which F* radicals etch the material whilst O_2 creates a passivation film. The device wafer is reduced to 100 µm by back grinding and polishing (Figure 29(d)). This is followed by depositions of a 2500 nm thick PECVD oxide and a 500 nm thick PECVD silicon nitride layers which act as insulation layer and diffusion barrier respectively. After the deposition, the layers are etched so that the electrical contact to the backside aluminum RDLs is sustained. The next process step is sputtering of a 1000 nm thick copper seed layer (Figure 29(e)). After this a direct current electroplating is used to deposit a 10 µm thick copper layer to the via sidewalls (Figure 29(f)) which is followed by Chemical-Mechanical Planarization (CMP) process in order to remove overburden copper (Figure 29(g)). Front-side RDLs and contact pads are made with through-resist electroplating process and lastly the wafers are cleaned (Figure 29(j)). [14]

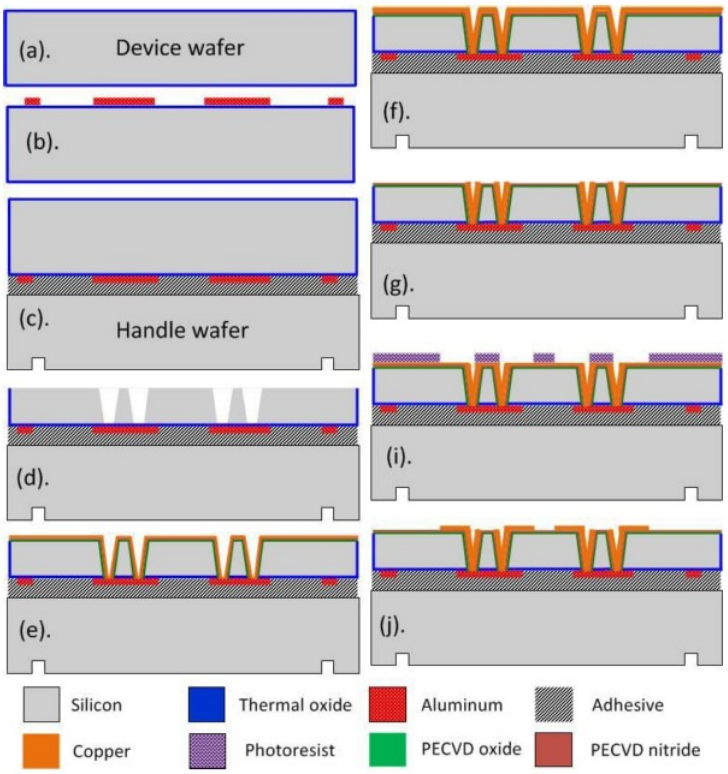

Figure 29: The fabrication process of the tapered copper-filled vias with redistribution lines. The structure consists of two silicon wafers; handle wafer and device wafer. The handle wafer provides mechanical support whilst TSVs and redistribution lines (RDLs) are fabricated into the device wafer. [14]

All of the examined chips were on a single wafer which was diced before thermal cycling test. Only a small portion of the chips were working correctly and their location a on the wafer were random. The examined chips have two different pitches: 90 µm and 300 µm. The pitch size has an effect on the number of the vias on a single chip which are 1400 and 420 respectively for a smaller and a larger pitch size. All of the vias have tapered sidewalls with 82-85^{o} profile angles and the vias are annular which means that they are not completely filled during the electroplating process. All of the vias had diameter of about 60 µm at the top of the via and diameter of about 30 µm at the bottom of the via and height of 100 µm. [14]

The wafer had undergone series of tests before it was received. The details of these tests are presented in Table 4. These tests, especially the temperature cycling, had to be accounted for when the reliability analysis was conducted.

Table 4: Details of the tests conducted with the wafer. [14]

No.	Reliability test	Standard	Test conditions
1.	Temperature cycling	JESD22-A104A-G	640 cycles, -40°C to +125°C
2.	High temp storage	JESD22-A103	100 hours, 200°C,
3.	Highly accelerated stress testing (HAST)	JESD22-A118	200 hours 85°C, 85%RH
4.	Current cycling	-	72 hours, DC, -100mA to 100mA, 3000 to 125000 cycles
5.	Current stressing	-	168 hours, DC, 150 mA

The wafer was diced with Loadpoint Dicing Saw AL-6. The chips had unique coordinates on the wafer which were used to identify each chip when the electrical measurements were performed. These coordinates are transferred into the chip numbers as in Table 5 in order to simplify the identification. Finally, the reliability testing was started with nine completely working chips. Six of those nine had 420 vias while only three had 1400 vias.

Table 5: The information about the samples at the start of the reliability testing.

The chip number	The number of TSVs/chip	The TSV pitch (µm)	Resistance (Ω)
1	420	300	72.0
2	420	300	68.5
3	420	300	68.2
4	420	300	72.6
5	420	300	72.4
6	420	300	73.7
7	1400	90	65.2
8	1400	90	119.2
9	1400	90	66.1

7.2. The resistance measurements

The electrical measurements were conducted at Aalto University School of Electrical Engineering. The main objective was to measure the resistance of the entire chip which consisted of seven identical TSV loops. Even though, the chips had Kelvin TSVs, they were not used in electrical measurements. Resistances of single loops were also measured in order to get the information of how resistance is distributed among them. Ideally, resistances would be the same in every loop, but in some loops the resistance was measured to be much higher than in any other loop. With this information the likely point of failure could be identified.

Electrical measurements were planned to be carried out with a constant real time resistance monitoring while the samples were in the thermal shock chamber. The plan was to make a connection with copper wires between the contact pads and the datalogger. The connections that were made successfully proved to be extremely fragile. During the thermal cycling, it would have been difficult to determine if the failures had been caused by the breakage in the TSVs or in the connection between the chip and the wires.

The idea of constant electrical measurements was aborted. It was decided that the test subjects would be planted in the thermal shock chamber without any real time monitoring and the electrical measurements would be made when the samples were taken out of the chamber. The problem with this approach was that the measurements were made in the room temperature which means that the information about the behavior of the samples was never obtained in the high and in the low temperatures. For instance, cracks might be present at the high or the low temperature but vanish at room temperature.

The first electrical measurements were done before and after the dicing. These resistance measurements yielded identical results and are presented in Table 5. The electrical resistance measurements were made with 2-point probe using two self-made copper tip probes which were manually pressed to desired contact pads on the sample in order to measure the resistance. The probes were attached to Agilent 34901A 20-Channel Armature Multiplexer, Figure 30, which was placed inside 34970A Data Acquisition/Data Logger Switch Unit. The data logger was attached to a computer which used Agilent BenchLink Data Logger 3 software to collect the measured data.

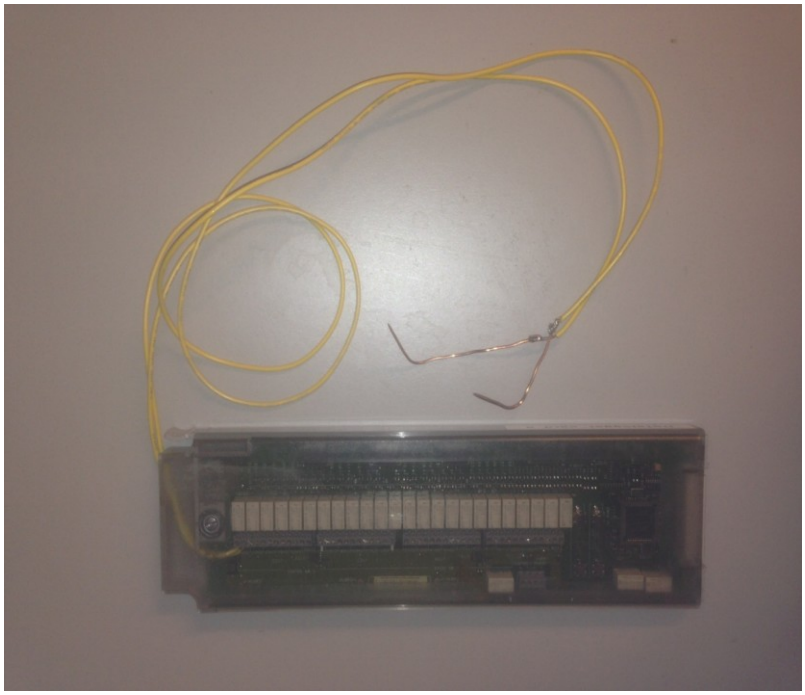

Figure 30: Self-made probes attached to Agilent 34901A 20-Channel Armature multiplexer.

7.3. The thermal cycling test

The samples were placed into the ESPEC TSA-71S thermal shock chamber in which the thermal cycling test was carried out. The machine consists of one chamber that circulates cold and hot air and it is presented in Figure 31. The temperature ranged from -40 ^{o}C to +125 ^{o}C with 30 minute cycle time. The dwell time at the low and the high temperatures were 15 minutes to ensure that the temperature was evenly distributed across the samples. The thermal cycle profile is presented in Figure 32. The test samples were taken out of the chamber in order to measure the resistances of the samples. The measurement results were gathered and possible failure times recorded and if a failure had happened, the sample was taken out of the thermal shock chamber and the point that failed was recorded.

Figure 31: ESPEC TSA-71S thermal shock chamber which was used to do thermal cycling test.

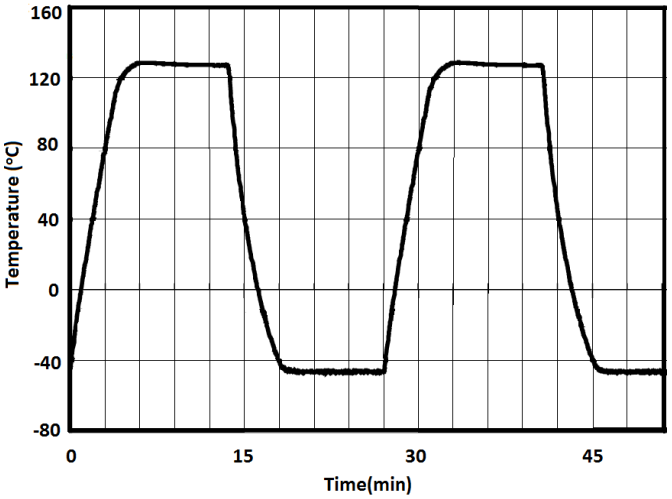

Figure 32: Thermal cycle profile for the test samples.

7.4. Imaging and sample preparation

The sample preparation started with molding the samples in mixture of Struers EpoFix Resin and Struers Epofix Hardener epoxy. This was followed by using Struers Epovac vacuum apparatus in order to eliminate possible bubbles in the epoxy. The hardening of the epoxy took one day. After the molding, the samples were mechanically grinded with Struers LaboPol-21 in order to achieve cross-sectional view of the vias and then polished with Struers RotoForce-4/RotoPol-22. The polishing was carried out with 9 µm and 1 µm polishing cloths which were used for 15 minutes. The samples were prepared for SEM imaging by coating them with chromium in Emitech K575X Sputter Coater in order to avoid charging of the non-conductive samples. After this, JEOL JSM-6330F field emission SEM was used to image the samples at Aalto University at Micronova. The images were taken with back-scattered electron (BSE) detector as well as with secondary electron detector. Working distance was set to 15 mm and the accelerating voltage was at 15 kV.

8. Results and discussion

Results from the electrical measurements, FEM simulations, Weibull analysis and sample imaging are presented in this section with discussions.

8.1. The electrical measurement results

The electrical measurements were planned to be made every 200 cycles at the beginning of reliability testing. The period was increased to 400 cycles between measurements after 1000 cycles due to minimal changes in the resistances. Samples were taken out of the thermal shock chamber during the running of the program which means that the samples were not completely settled to the room temperature when the resistances were measured. For instance, some failures were noticed when the measurements were made right after the samples were taken out of the chamber. When the measurements were repeated after a short while, the previously noticed failures were not present anymore. With this information an assessment can be made that the samples underwent a recovery of some degree in which the cracks closed under room temperature conditions. The samples in which this was observed were considered as failed samples.

The measurements were repeated at least three times, most often five times, in order to minimize the human error. If some of the measurements differed greatly from other results, they were disregarded as human errors. The other results were used to calculate the arithmetic mean of the measurements.

Other sources of errors other than the human error were also identified during the measurements. The most notable ones were the error caused by the probes and the erosion of the contact pads. The probe resistance was measured at the beginning of every time that the electrical measurements were made. The probes had the small resistance of 0.2 ± 0.05 mΩ which was added to the calculated arithmetic mean.

The sharpened tips of the copper probes caused unexpected and serious damage to the contact pads which proved to be a serious source of error during electrical measurements. The damage to the contact pads was noticeable even after the very first measurement session. What made things even worse was the fact that the measurements were repeated several times in every session. During the very last electrical measurements it was difficult to get any results with the probes. The damaged contact pads most definitely had an effect on the measured resistances, although, the exact amount is difficult to determine. What is worse, the damage might cause the conclusion that one or more TSVs on the chip have failed even though only the contact pads have broken down. When assumed failure was encountered, the exact point of failure was carefully observed in order to be certain that the failure was in the TSV structure and not in the contact pads.

When a failure was noticed, the exact failure point was determined. At first the resistance of the every loop was measured in order to find open circuits. When the failed loop was found the exact point was determined by measuring the resistance between two TSVs by gently pushing the probes against the via openings. This was continued until the open circuit was found. A drawback for this plan was that the pressure from the probes could seal the crack so that the loop seemed to be working correctly when measured later. Nevertheless, if the chip was not working completely in the first measurement, it was considered as a failed sample.

The total resistance at the start of thermal cycling was 65-75 Ω to all but one sample which had the resistance of 120 Ω. Arithmetic means of measured resistances are presented in appendix A. The total resistance of the samples with 420 TSVs was increasing noticeably slower than the samples with 1400 TSVs as can be seen in Figure 33. This was an expected result because the samples with more TSVs have a greater risk of formation and propagation of voids and cracks thus increasing the total resistance.

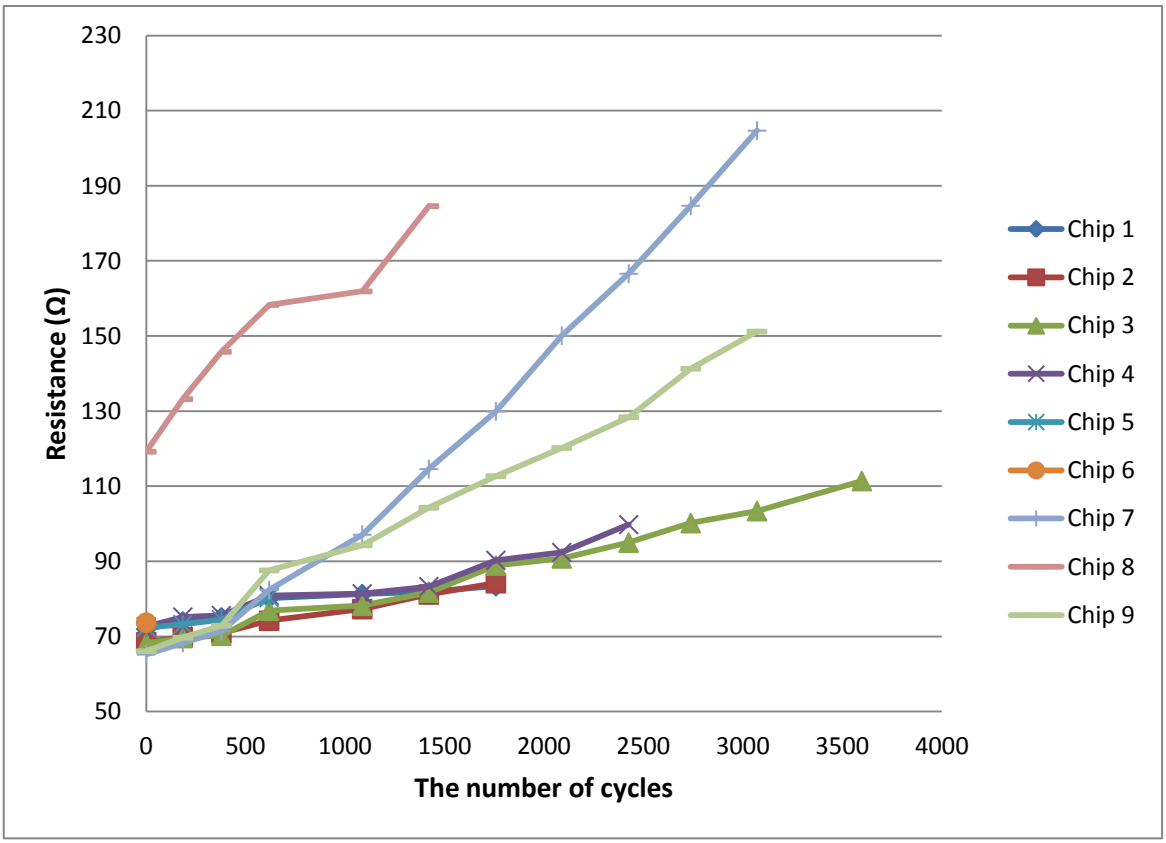

Figure 33: The increase of the resistance as a function of temperature cycles in all tested samples.

The increase of resistance was also less constant in samples with more vias. The samples with 420 vias had almost constant resistance increase, Figure 34, whilst the samples with more vias had rapid increases in resistances, Figure 35. This phenomenon can also be explained with increased likelihood of formation of cracks. What was a little surprising was that the samples with more TSVs seemed to be more durable even if the resistance was increasing more rapidly. The failures were detected later in relation to samples with lower amount of vias. This is most likely due to small sample size which skewed the results.

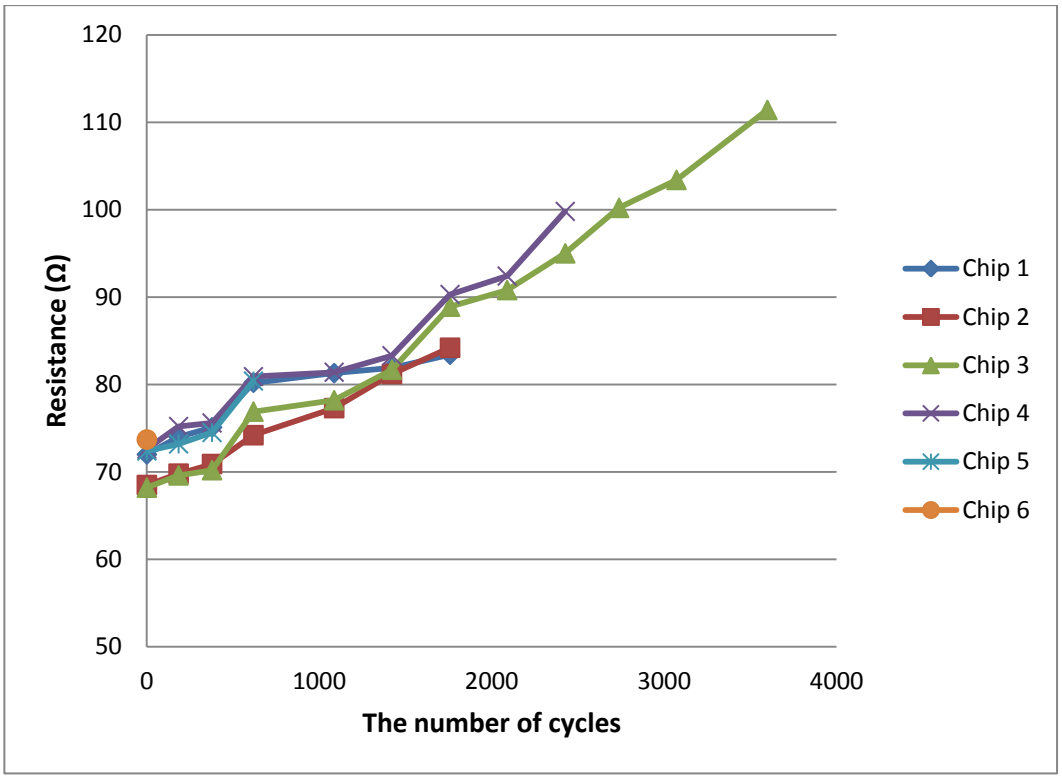

Figure 34: The increase of the resistance as a function of temperature cycles in samples with 420 vias.

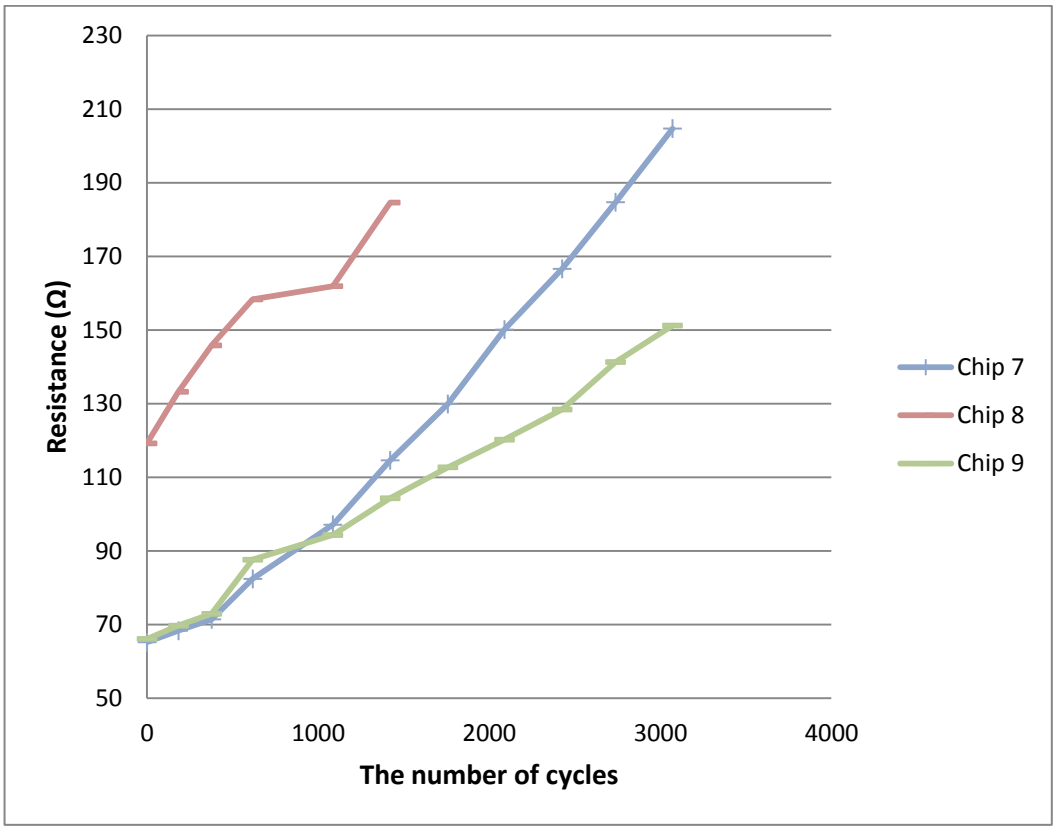

Figure 35: The increase of the resistance as a function of temperature cycles in samples with 1400 vias.

In addition to total resistance measurement, the resistances of single loops were also measured. In these measurements, the rapid increases of the resistances just before the failure were tried to be identified to a single loop. This information could be used in predicting the exact failure point. The resistance of a single loop was about 10 Ω at the beginning of the testing. The resistance increase was almost constant to all but one sample. This would indicate that the deterioration, such as crack formation and propagation, happens in many vias simultaneously. But when the resistance increased rapidly in one sample (chip number 8), the crack has most likely propagated to a level where the failure is imminent. Later, the failure was pinpointed to the exact loop that had the rapid resistance increase.

8.2. Finite element method

In this thesis FEM simulations are used to examine stresses in copper, silicon dioxide and silicon regions in TSVs. Stresses vary with the changes in via profile, diameter, pitch and height.

8.2.1. Finite element simulations

Finite element analysis (FEA) analyses were carried out in order to identify the critical failure points in TSV structure. When modeling thermal stresses in a TSV, some assumptions are usually made. For instance, the barrier layer is much thinner than the dielectric layer, so its effect is negligible [67].

Table 6: Used material properties in simulations. [5]

Material	Silicon	Copper	Silicon oxide
Young's Modulus (GPa)	162	115.5	71.7
Poisson Ratio	0.28	0.343	0.16
CTE (ppm/^{o}C)	3.05	17.7	0.51

Failure analyses were performed on tapered, cylindrical and annular via profiles. In every analyses, the via is filled with copper (leftmost section) and there is a silicon oxide insulation layer between the copper and the silicon substrate (rightmost section). Used material properties are presented in Table 6. Temperature variation range is from -45 ^{o}C to 125 ^{o}C for all the analyses and the stresses are expressed in terms of von Mises stress in GPa. Basically, if the von Mises stress is larger than the yield strength of the material, it starts to yield. The tapering angle is set to 85^{o}. The analyses results are presented in Figure 36, Figure 37 and Figure 38.

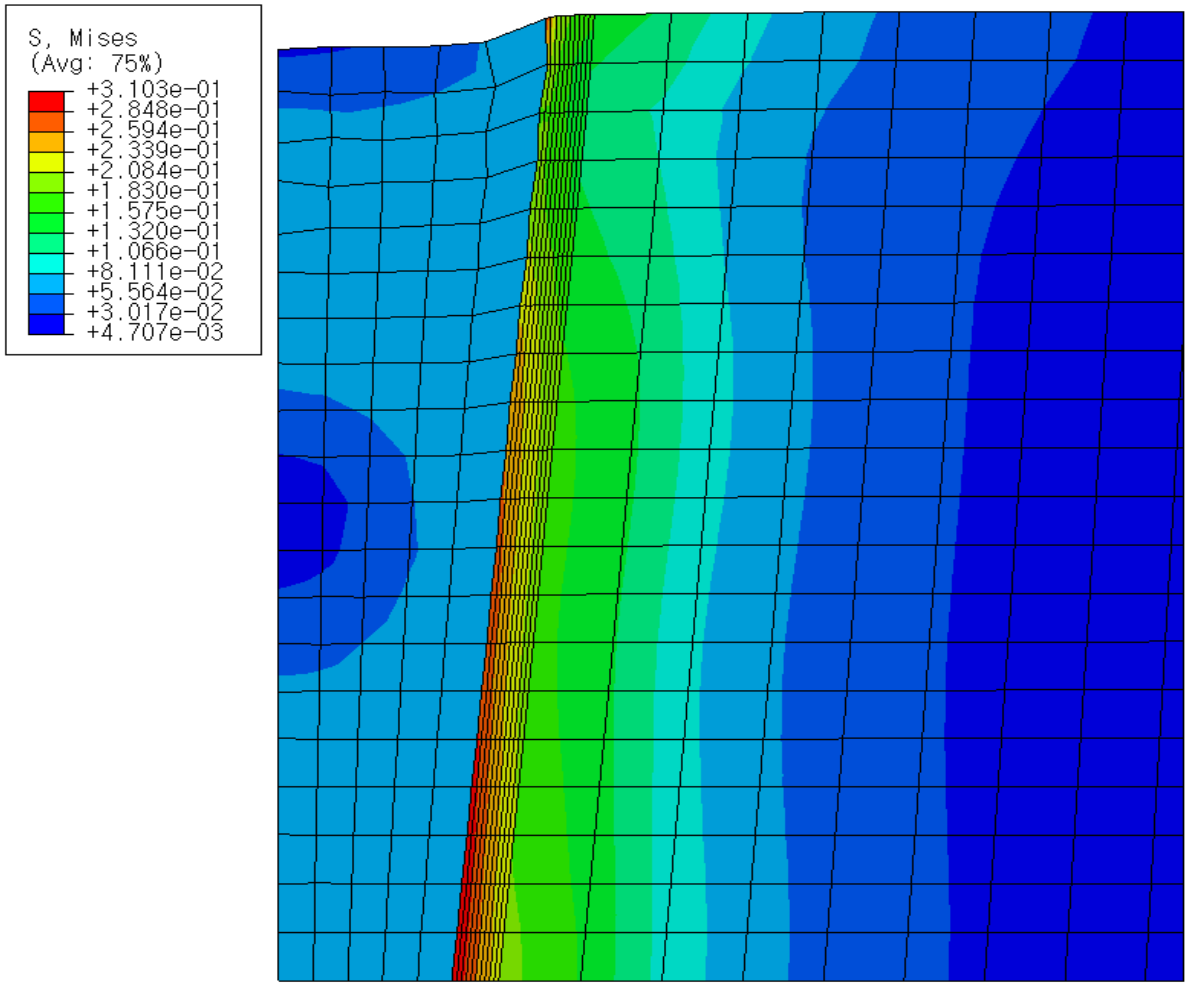

Figure 36: Compression phase in a tapered via. Deformation magnified 20 times.

As can be seen in Figure 36 the maximum von Mises stress is located in tapered structure at the bottom of the via at the interface of the copper and the insulation layer. These results would indicate that this is the most likely failure point for the structure. The results are in line with the study reported by Selvanayagam et al. [66] concerning stress analyses of copper filled TSVs. The amount of stress diminishes the further the location is from the aforementioned interface which would indicate that via diameter and pitch are the most important factors that determines the magnitude of stress in the silicon substrate between the vias. There is another critical failure point at the interface at the opening of the via. Nevertheless, von Mises stress at this point is considerably lower than at the interface at the bottom of the via.

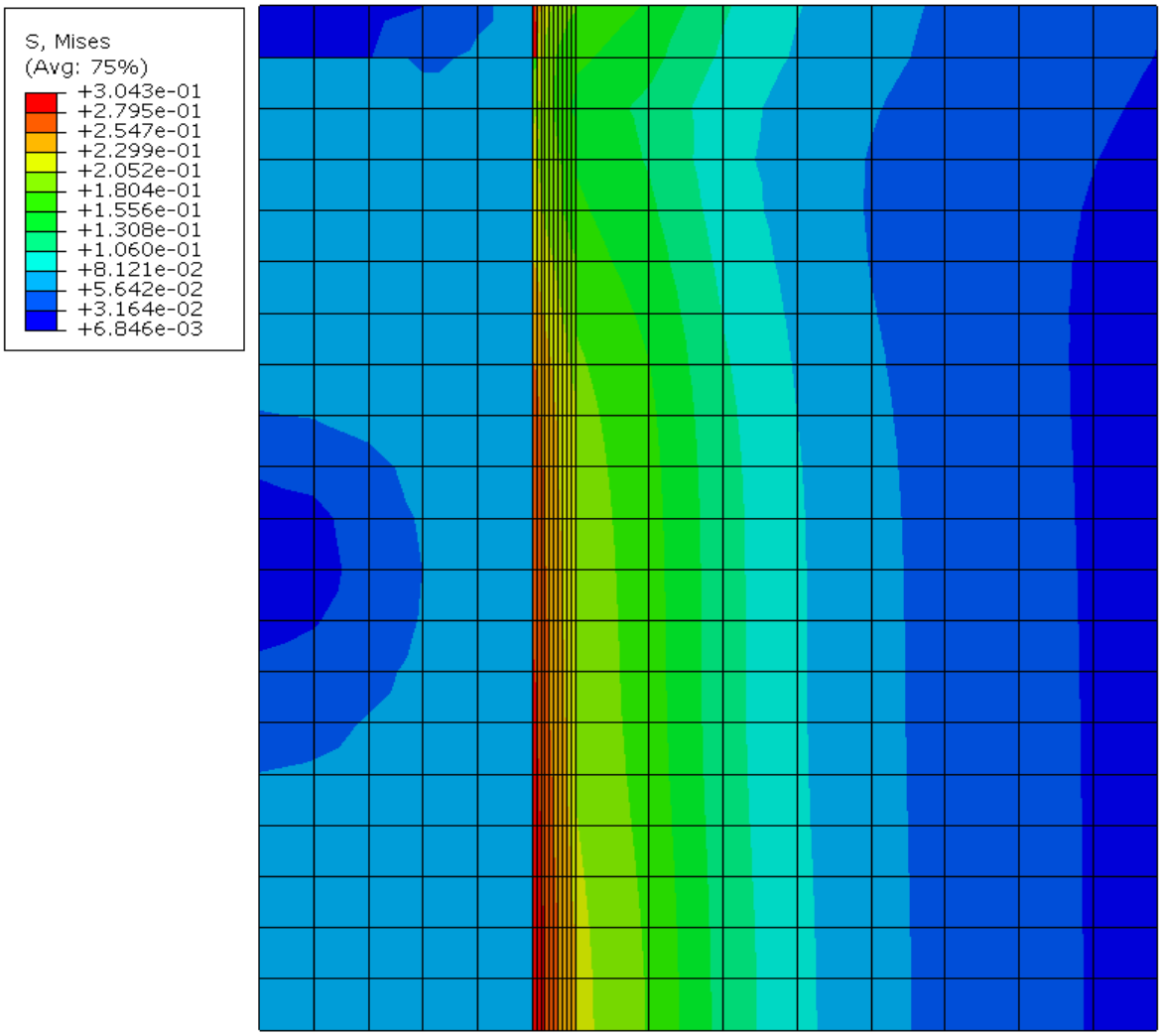

Figure 37: Expansion phase in cylindrical via.

Figure 37 presents a simulation of a cylindrical via. The results are very similar with the analysis of a tapered via. The maximum von Mises stress is located yet again at the bottom at the interface of the copper and the insulation layer. However, the major difference is that the stress at the opening of the cylindrical via is larger than in tapered vias. The result is the same as mentioned in the study by Shenglin et al. [18] concerning the properties of tapered TSVs.

Figure 38 presents a simulation of an annular tapered via. As can be seen, the critical failure point is at the same location as previously. However, the stresses are much lower in silicon oxide and silicon substrate regions which is due to lesser amount of copper filling as has been mentioned by Dixit et al. [30] in their study of annular vias. It is good to notice that there is not any critical failure point at the top of the via unlike in previous simulations in Figure 36 and in Figure 37. Also, unlike in previous simulations, the copper endures more stress in annular vias but it is smaller than the yield strength of copper which is 70 MPa [86]. These results indicate that tapered annular vias are the most reliable ones when exposed to thermal stresses and in every simulation, yield strength of copper is significantly larger than the maximum von Mises stress.

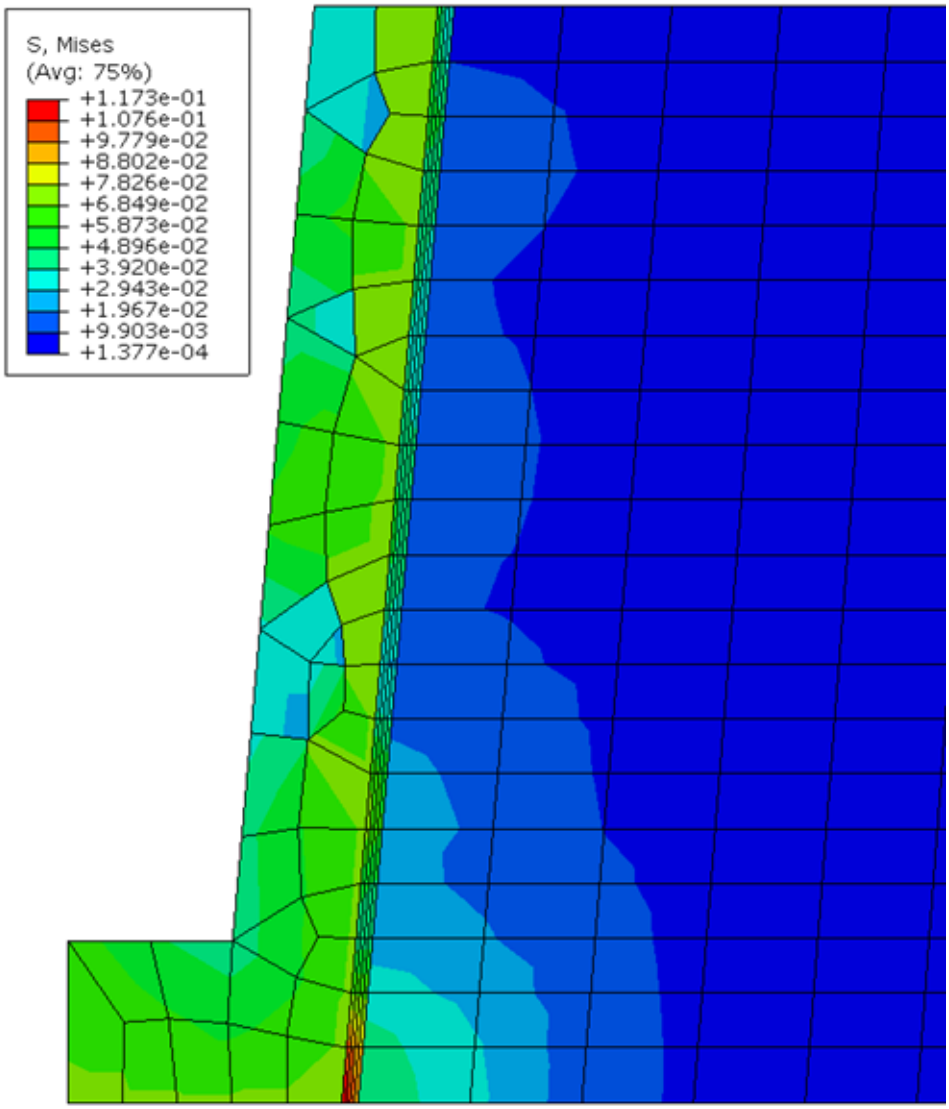

Figure 38: Annular tapered via during the compression phase.

8.3. Weibull reliability analysis

The tested samples had a different number of vias, 420 and 1400, and thus they also had different reliability. Figure 39 presents Weibull probability plot of the samples with 420 vias. As can be seen, the failure data points do not fit the straight line. Because of this, t_0 = 650 was added to each data point in order to improve the goodness of the fit. The results are shown in Figure 40.

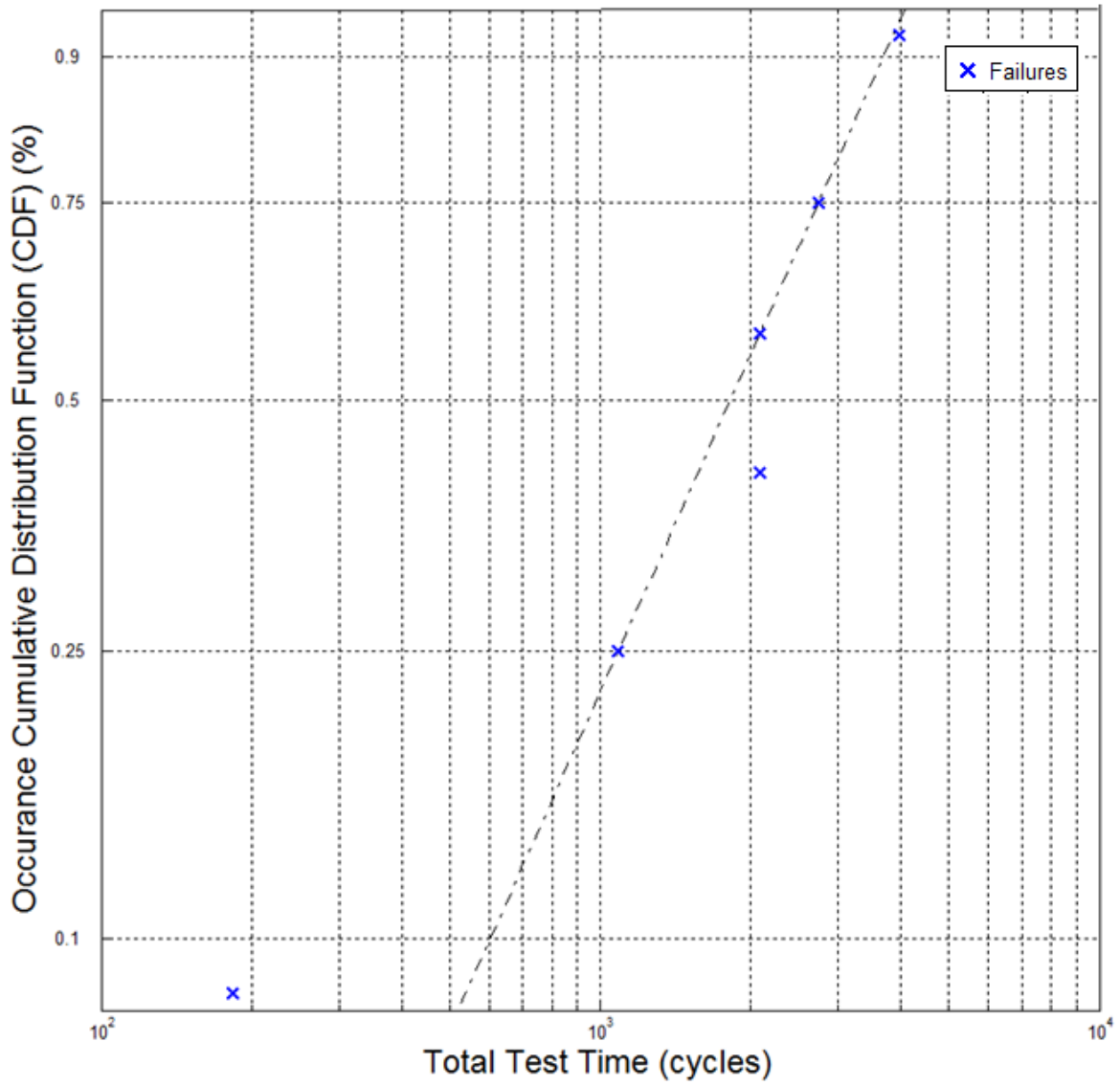

Figure 39: Weibull probability plot of the samples with 420 vias.

When using three-parameter Weibull, there are four criteria points that should be met. These criteria points were discussed earlier in section 4.6.2.. Firstly, as can be seen the Weibull plot shows some curvature in Figure 39. Secondly, t_0 = 650 was chosen to be location parameter because the samples had underwent a series of reliability tests, most importantly thermal cycling test of about 640 cycles as presented in Table 4, before they were given to me. Thirdly, correlation coefficient increases in three-parameter Weibull when compared to two-parameter Weibull as presented in Table 7. One criterion was not met when three-parameter Weibull was chosen. The sample size was smaller than recommended 20 being only six. Nevertheless, three-parameter Weibull improved the goodness of the fit considerably and thus it was chosen for the Weibull analysis.

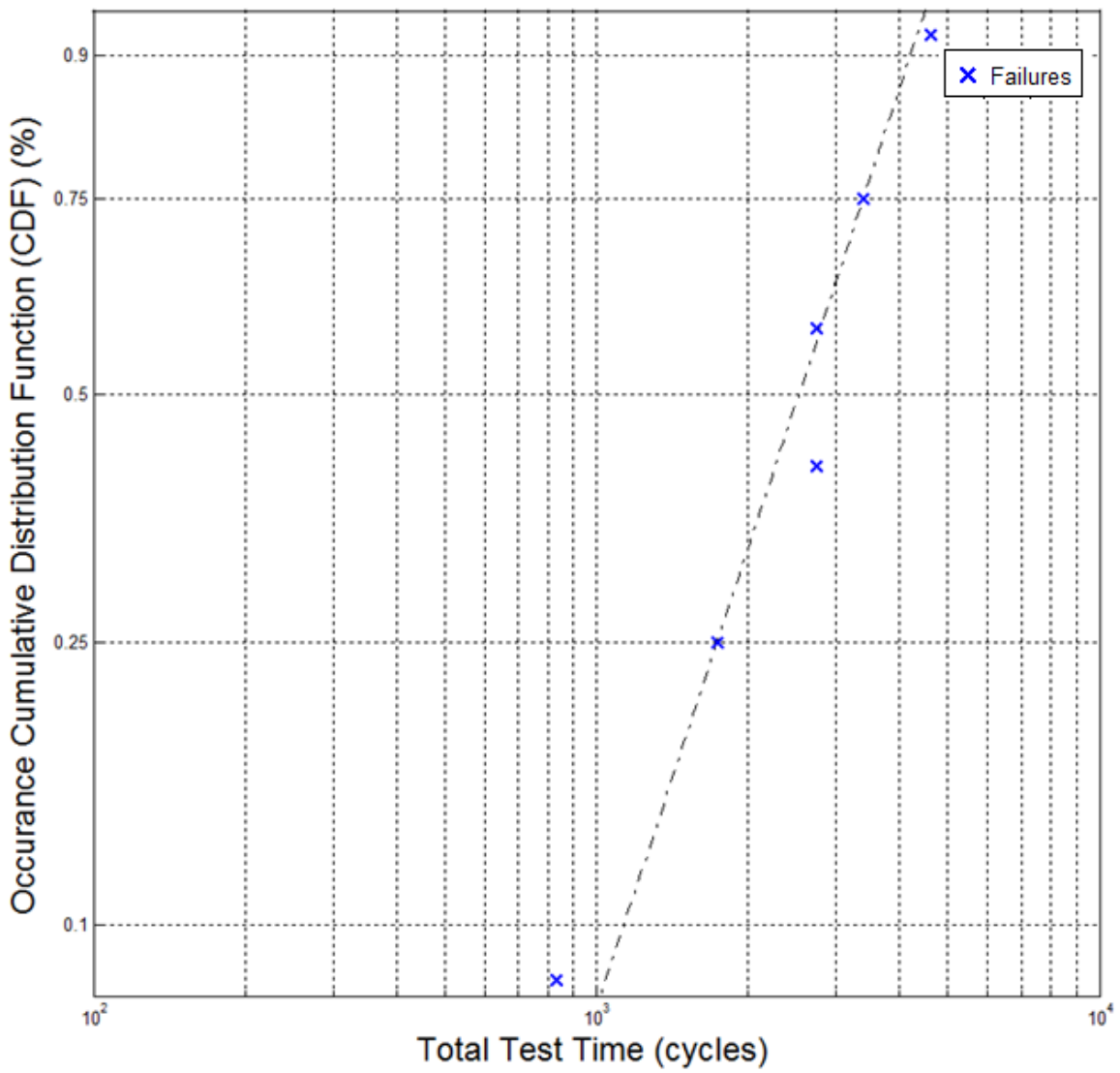

Figure 40: Weibull probability plot of the samples with 420 vias. Location parameter t_0=650.

Three-parameter Weibull was tried also for samples with 1400 vias but the improvements were negligible as presented in Table 7 and the sample size was very low being only three. Thus, it was determined that both two-parameter and three-parameter Weibull analysis were quite unreliable for the samples with 1400 vias.

Equations (18)-(25) were used in order to calculate slope and shape parameters and correlation coefficient for the tested samples. These results are presented in Table 7. The results were used to make Weibull probability plots with Matlab R2014a. In these plots, 1000 random values for a Weibull distribution with given shape and scale parameters were generated and plotted. The results are presented in Figure 41 and in Figure 42. In the plots n/s means number of samples/number of suspensions.

From Table 7, it can be seen that the samples with 420 vias has high correlation coefficient and coefficient of determination which indicates that the data points from samples with 420 vias has a good linear fit. Thus, accurate predictions on reliability can be made according to Weibull

probability plot. Also, the location parameter improved the goodness of the fit in the samples with 420 vias.

Table 7: Calculated Weibull parameters for the tested samples.

Number of samples	3	6	3	6
Number of TSVs/sample	1400	420	1400	420
Scale parameter (η)	1499,34	883,331	4048,169	3106,96
Shape parameter (β)	2,5786	1,005	3,252	1,807
Location parameter (t_0)	0	0	650	650
Correlation coefficient (r)	0,90423	0,963	0,9043	0,98
Coefficient of determination (r^2)	0,81763	0,927	0,8178	0,96
Number of suspensions	0	0	0	0

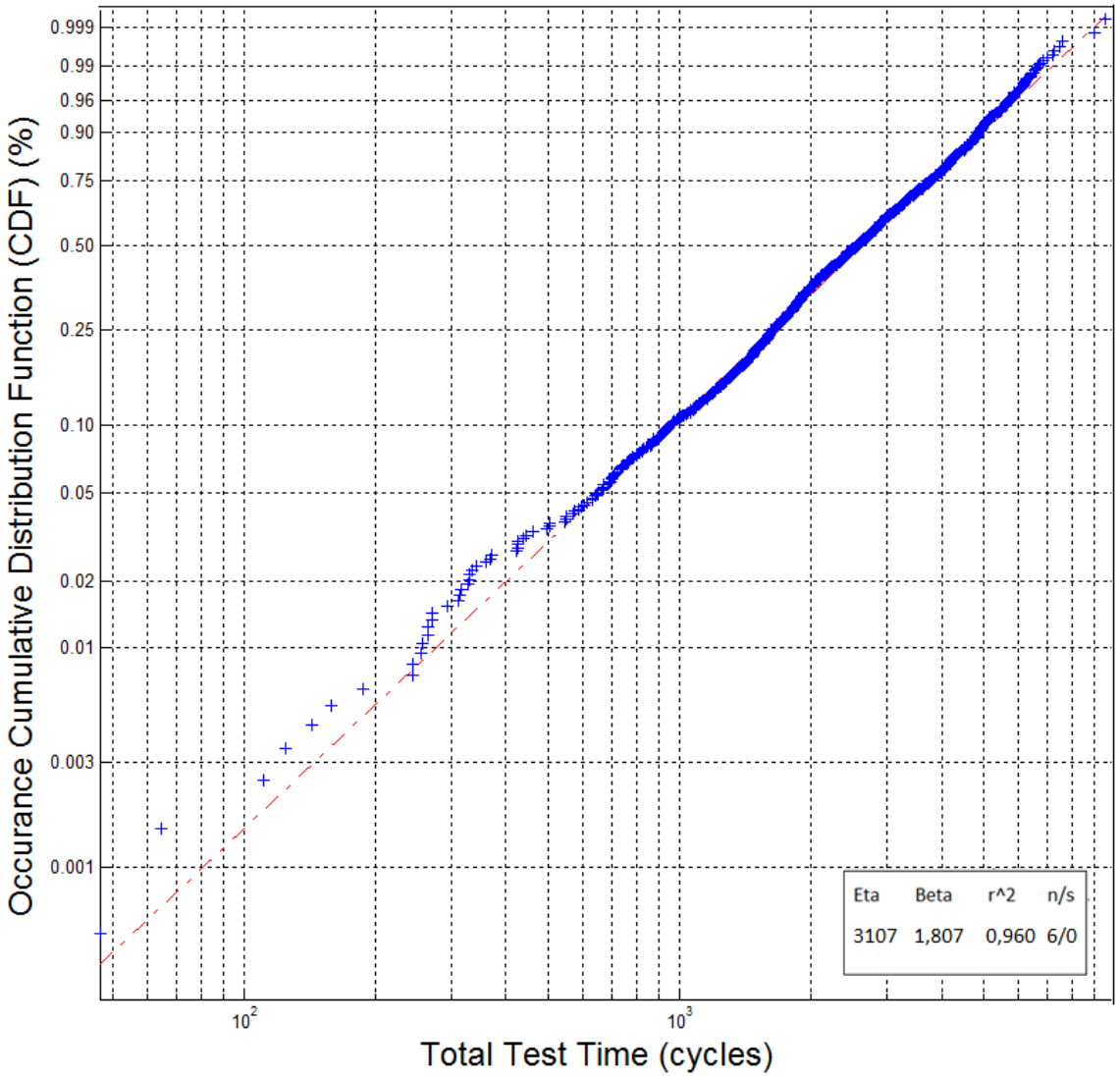

Figure 41: The Weibull probability plot of the samples with 420 vias. 1000 values generated according to scale and shape parameters. Location parameter t_0=650.

The value of scale parameter η indicates the time in which 63,2 % of the samples have failed and the slope parameter β indicates the types of failures present in the population as mentioned earlier in section 4.6.2. As we can see from Figure 41, 63,2 % of the samples with 420 vias have failed at cycle number 3107, likewise the value 1,807 of slope parameter indicates that the failures are caused by wear.

From the plot in Figure 41 we can see that after 1000 cycles approximately 10 % of the samples will fail. Likewise, after 4000 temperature cycles approximately 75 % of the samples will fail. Now, if we consider that only one via per sample breaks down and causes the open circuit, the probability of a random single via to break down after 1000 cycles is 1 / 420 * 0,10 = 0,024 %. However, it is good to take into account that the samples had undergone a series of reliability tests before the thermal cycling test. This worsens the reliability of the samples by causing defects in the structure, but on the other hand aforementioned reliability tests removed infant mortality samples. It is also likely that more than one via per sample fails between the measurements. The likelihood increases the longer the test continues due to accumulation and propagation of the defects. Furthermore, the point of failure does not have to be in TSV, it can also be located, for instance, in redistribution layer causing the open circuit. Also, the used failure criterion is lenient because the samples were considered as failed when open circuits appeared. In some studies the samples are considered as failed if the resistance increases 10 % [40][87] from the initial value. All in all, these results indicate good reliability of the samples under thermal cycling test.

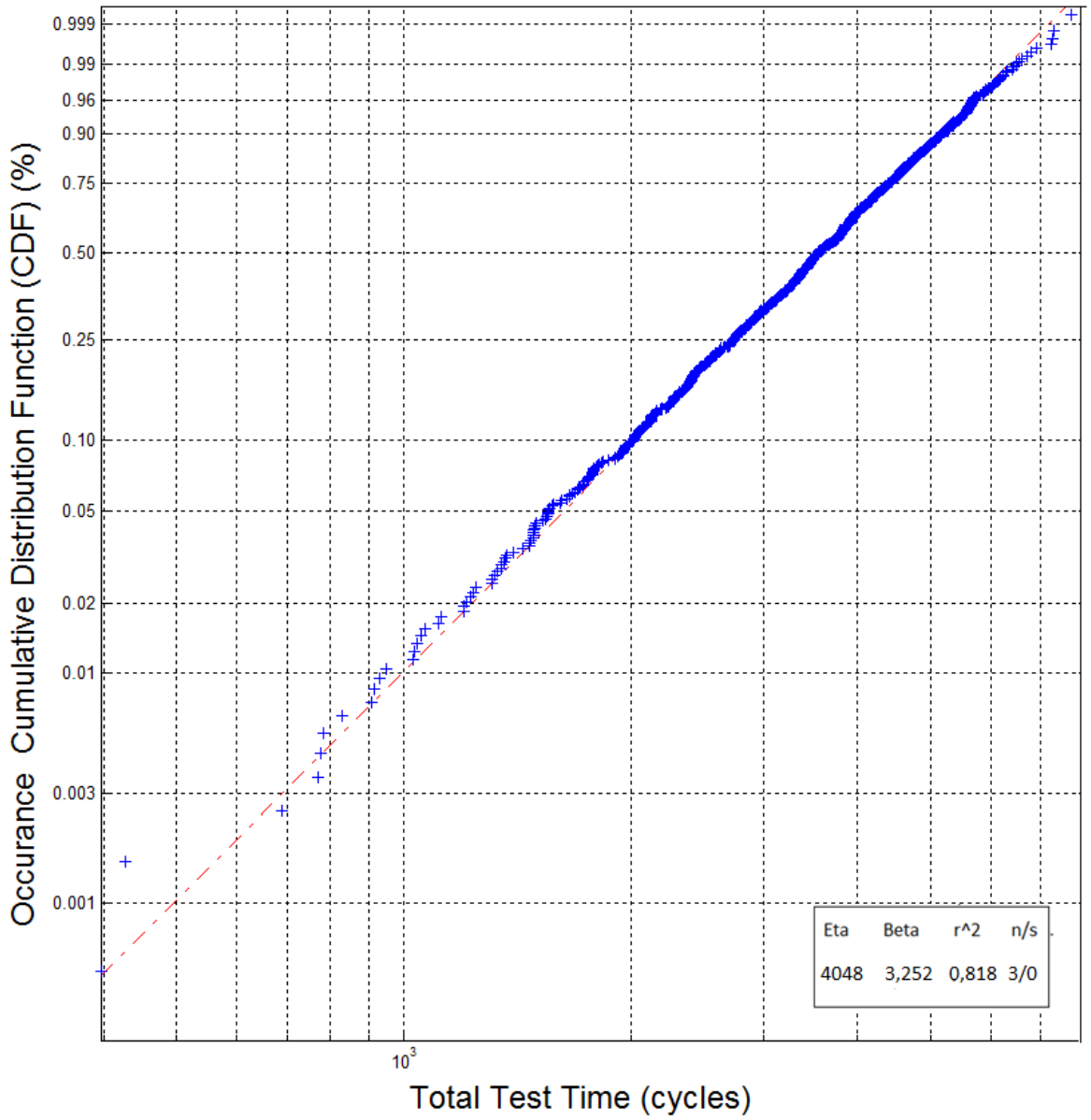

Figure 42: The Weibull probability plot of the samples with 1400 vias. 1000 values generated according to scale and shape parameters. Location parameter t_0=650.

Figure 42 presents Weibull probability plot of samples with 1400 vias. As mentioned earlier, the sample size was really small which affects the credibility of the received data. According to plots in Figure 41 and in Figure 42, the durability of the samples with 1400 vias is better when compared to samples with 420 vias.

8.4. Imaging

Mechanical grinding caused some clear damage to the samples. Nevertheless, the failures that are our interest are open circuits that prevent the flow of electric current through the daisy chain loops, thus the cracks should be large and easily recognizable. Because of this, it is safe to say that the identified failures are formed before the grinding and not caused by it. On the other hand, if the object is to examine small defects the mechanical grinding would not be ideal sample preparation technique, because it would be really difficult to determine what caused the defects.

Figure 43 presents a backscatter electron image of a single via that is electrically fully working. The via dimension values are marked to the image: the tapering angle, top and bottom diameter of the via and the height of the via. Molding the samples in epoxy causes the inability to see the cone-like structure of the tapered via. Nevertheless, the molding keeps the shape of the via relatively intact during the mechanical grinding, when compared to grinding without the epoxy.

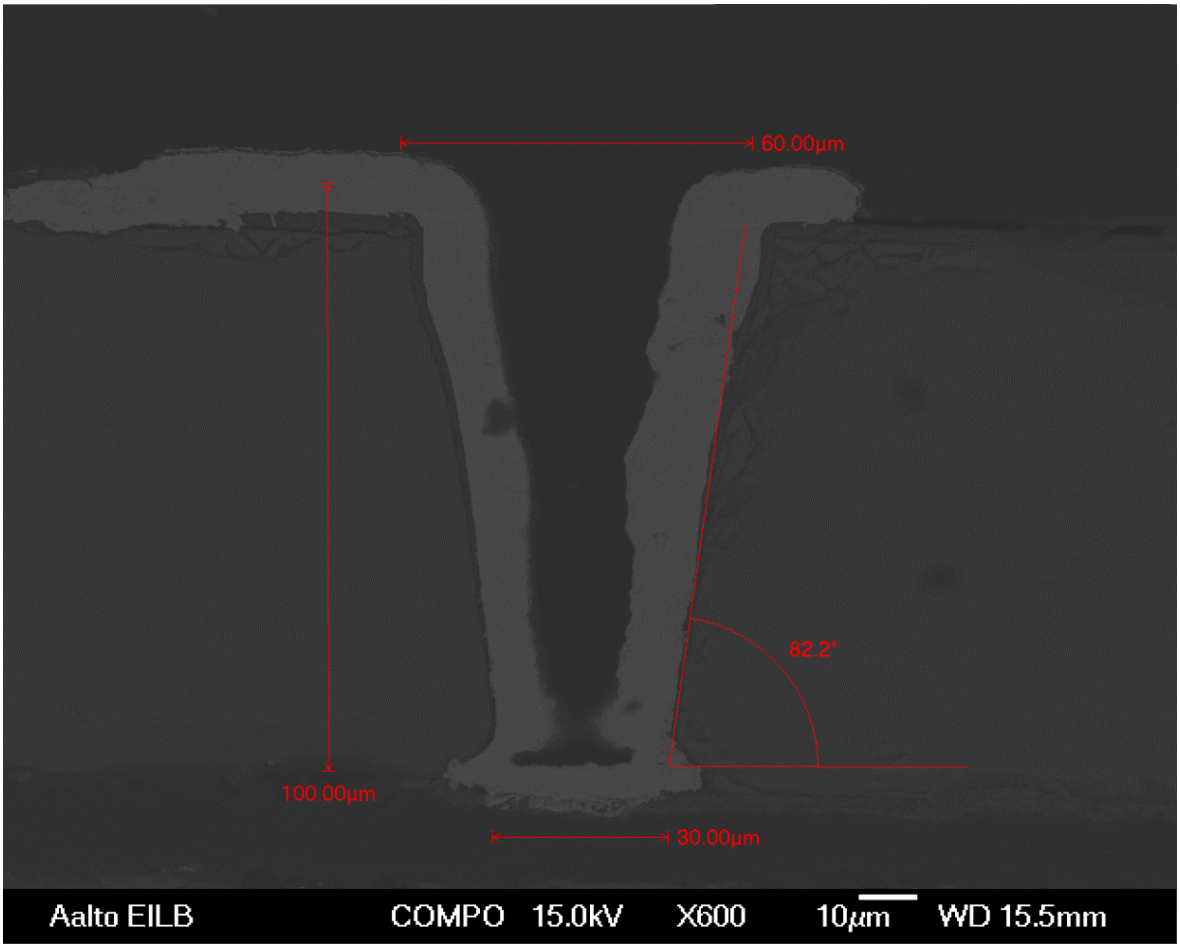

Figure 43: Backscatter electron image of a single via with dimensions values.

Figure 44 presents BSE image of a pair of vias with the pitch of 300 µm. The image presents front-side redistribution layer connection between two vias which enables the daisy chain structure along with the back-side redistribution layer. The thickness of the device wafer is 100 µm which causes the fragility of the wafer. Thus, device wafer is bonded to a sturdy handle wafer with an

adhesive layer to provide mechanical endurance. The vias in Figure 44 are fully functional and the sample did not undergo thermal cycling test.

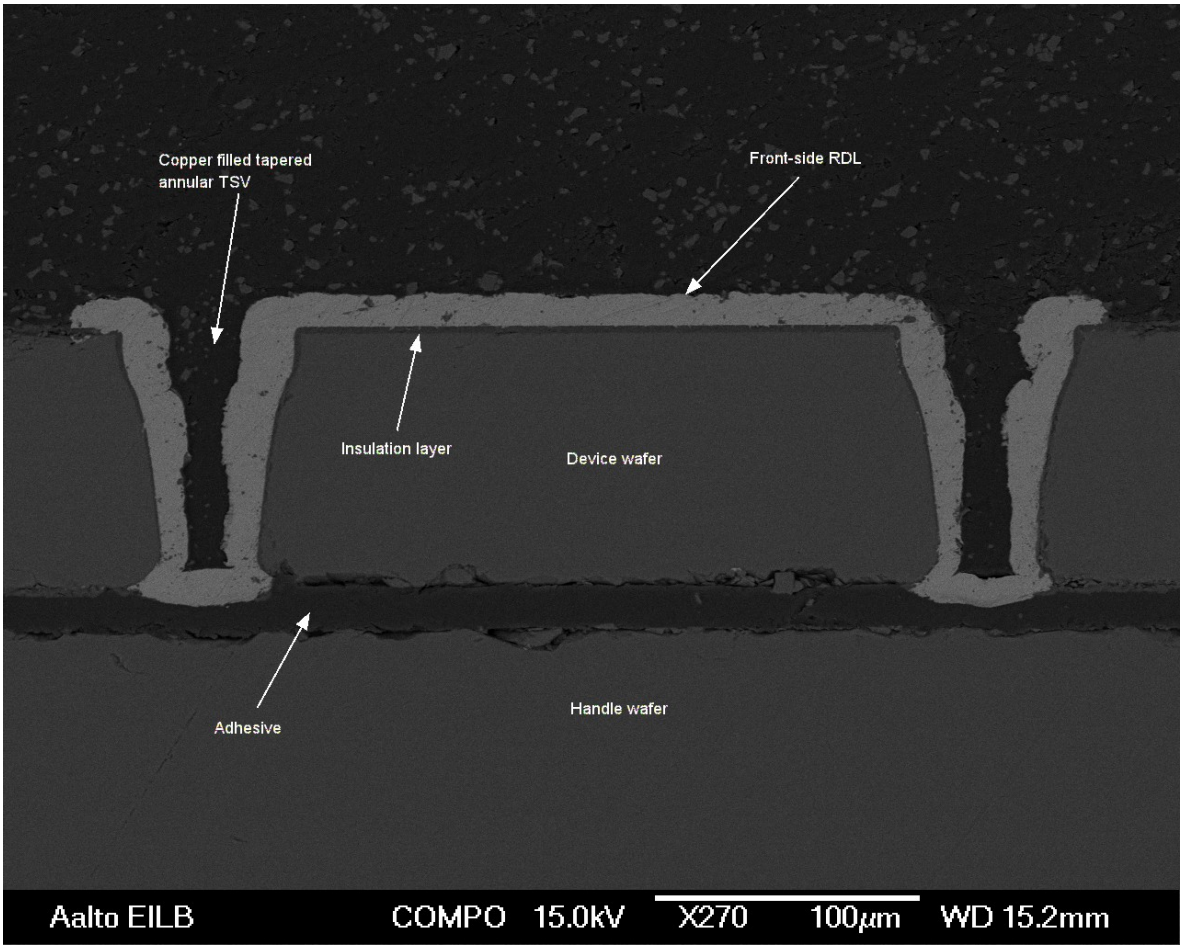

Figure 44: Backscatter electron image of a pair of vias. Important parts of the structure marked to the image.

A failed sample that went through thermal cycling test is presented in secondary electron detector image in Figure 45. Dash lined red rectangular highlights the point of failure which is magnified in Figure 46. Mechanical grinding is clearly caused some damage to the silicon substrate; however the copper region seems to be relatively intact except for the failed part. The image is from the chip that has 1400 vias with a pitch of 90 µm.

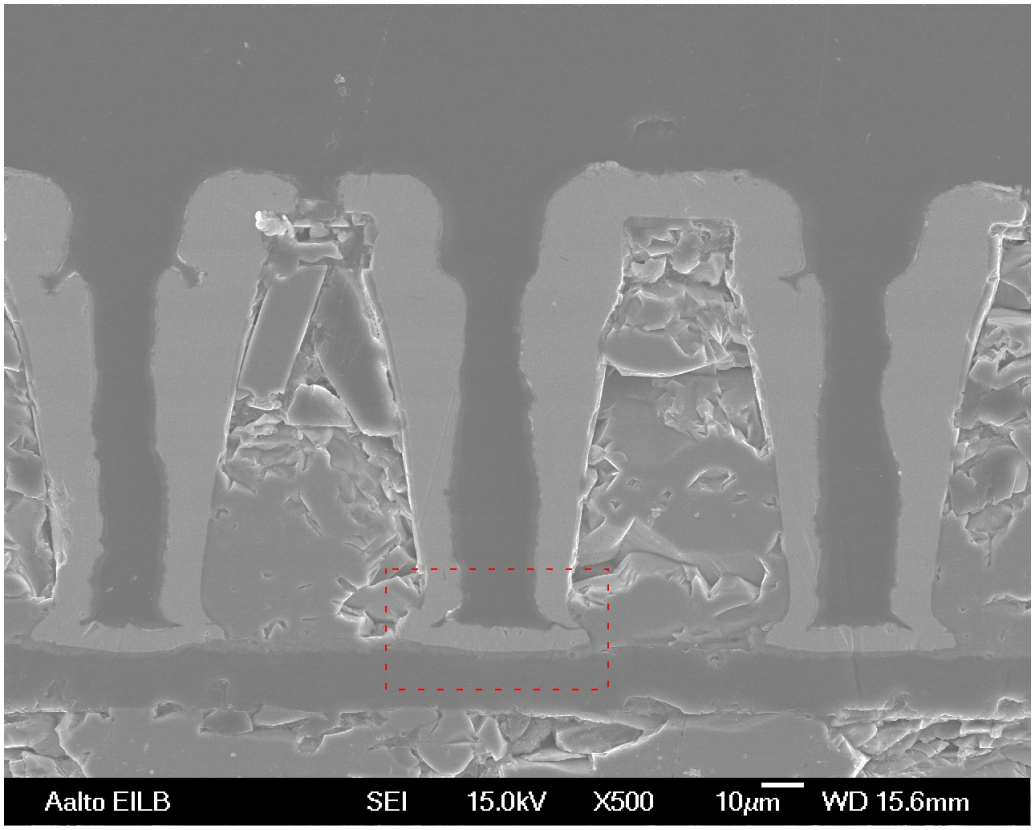

Figure 45: Secondary electron image of the failed TSV structure. The point of the failure highlighted with dash lined red rectangular.

Magnification of the point of failure from Figure 45 is presented in Figure 46. As can be seen from the image, a large crack has completely cut off the electroplated copper at the bottom right of the via causing an open circuit. A noteworthy point is that the failure is exactly at the critical failure area, which endures the greatest strain, according to the conducted FEM simulations.

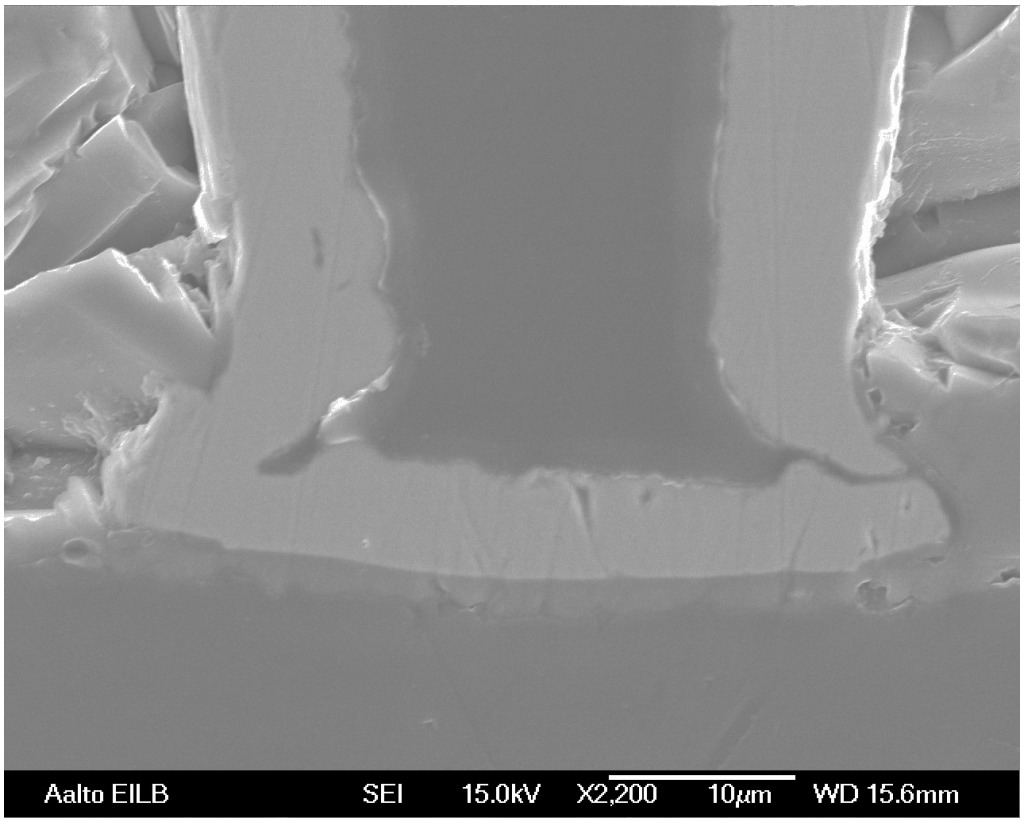

Figure 46: Magnification of the point of failure from Figure 45.

Figure 47 presents a BSE image of failed TSV. The point of failure is again highlighted by a dash lined red rectangular and it is magnified in Figure 48. Again the failure is in a critical failure area just like in Figure 46 although this time the crack is slightly smaller. It is possible that when trying to find the exact point of failure in the TSV chip, the measurement probes caused the reduction of the size of the crack when pushed against the opening of the via.

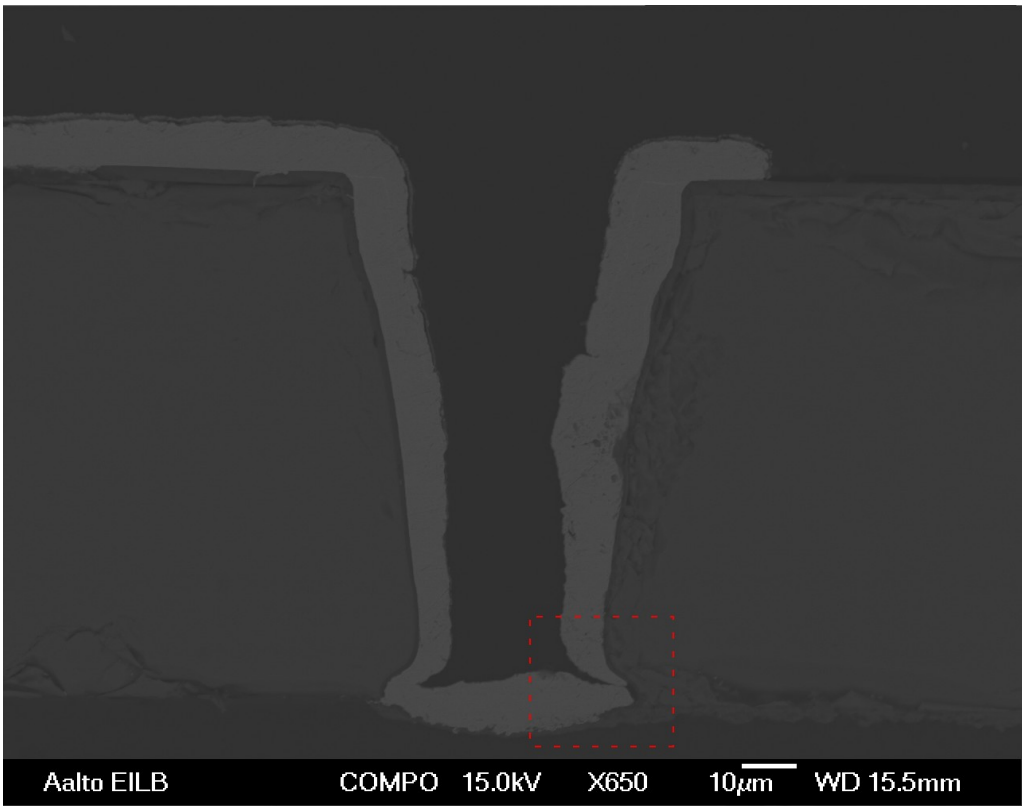

Figure 47: BSE image of a failed sample. The point of failure is highlighted with dash lined red rectangular.

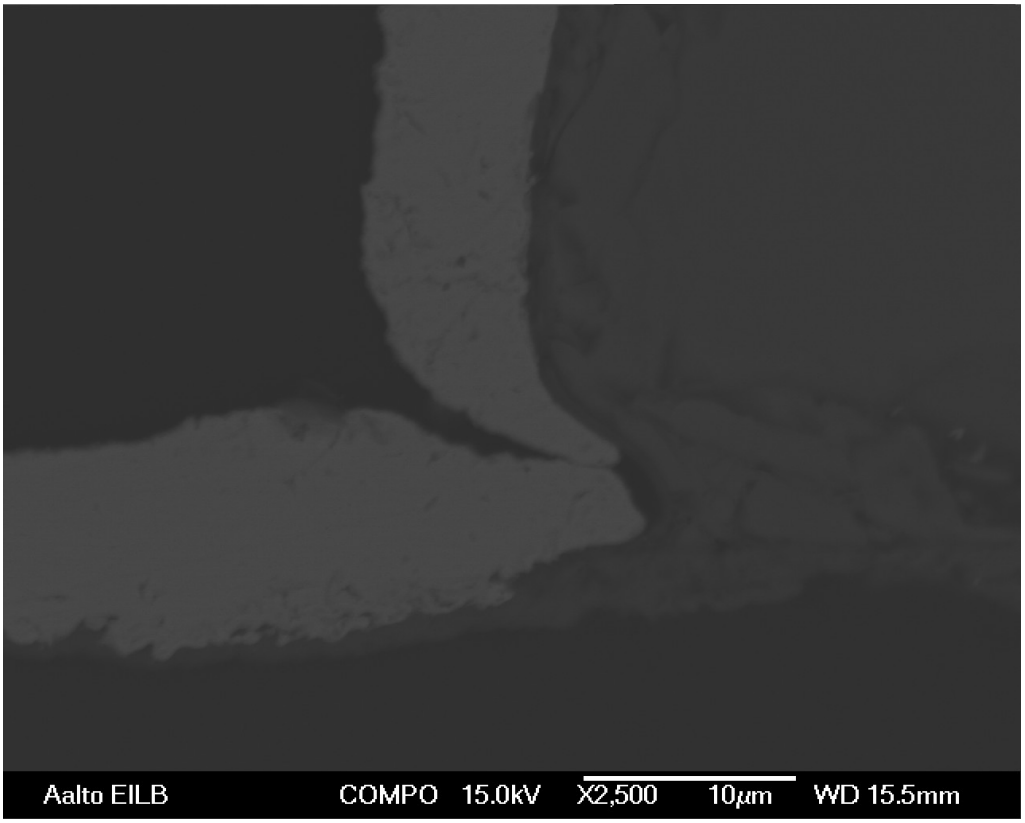

Figure 48: Magnification of the point of failure in Figure 47.

Simulation in Figure 38 indicate that the maximum stress areas in annular tapered via is at the bottom interface between copper and silicon dioxide insulation layer. The defect formation and propagation should be at its highest at this region because of localization of maximum stresses. The cracks should be initiated at the edges of the TSV and then propagate inwards to the center of the via as mentioned by Okoro et al. [39] in their detailed failure analysis of copper filled TSVs. However, in Figure 46 and in Figure 48 cracks seem to initiate from copper inside the via at the intersection of the sidewalls and the bottom of the via. The cracks are getting thinner towards the insulation layer and visible cracks are easily noticeable at the intersections even in electrically working TSVs in Figure 43, Figure 44 and Figure 45. Therefore, deduction can be made that the cracks are initiated from the defects caused by fabrication process.

If the test samples were completely filled, the crack most likely would not propagate through the structure at the same point as in Figure 46 and in Figure 48. For starters, fully filled vias would not have similar aforementioned fabrication defects than annular vias. Therefore, it is more likely that defects would be formed by thermal cycling test at the critical failure points at the edges of vias and from there the defects would propagate through the structure, as presented in Figure 20(a). Secondly, the time for a crack to propagate through solid copper filling would take much longer in fully filled than in annular vias. Therefore, crack propagation along the interfaces causes more damage than propagation through solid copper via in fully filled TSVs as presented by Okoro et al. [39] in their failure study. Hence, the failure mechanisms and the lifetime differ between annular and fully filled vias.

Even though annular vias seem to fail because of crack propagation in copper, it does not mean that it is the only failure location or mechanism. Formation and propagation of voids occur around the whole structure; however it happens at the lower pace in other parts than in maximum stress area. Nevertheless, accumulation of small defects has an effect on electrical performance of the via and crack propagation can happen simultaneously in multiple locations. Cracks between insulation layer and copper, as presented in Figure 19(a), as well as between aluminum metallization layer and copper, might have formed and propagated significantly. Due to used sample preparation methods, these interfacial cracks are hard to detect. Mechanical grinding also damaged surrounding silicon substrates making it almost impossible to identify if there were any cohesive cracks caused by thermal cycling, as presented in Figure 19(b).

When compared to aforementioned study by Frank et al. [10] in which not one sample was failed due to initialization of a crack in fully filled Kelvin TSVs after 500 cycles between -65^{o}C and 150^{o}C, it raises a question about the reliability against crack initialization of the examined samples in this study. Naturally, initialization of a crack in the via is not the only failure mechanism that increases resistance, for instance interfacial delamination could be behind the resistance increase, however only crack propagation failures are noticeable in Figure 46 and in Figure 48. These results indicate that tapered annular vias in this study are more prone to formation and propagation of cracks than fully filled vias in study by Frank et al. [10]. However, it is noteworthy that there were a lot more samples in this study which increases the likelihood of the formation of a failure and the samples had different dimensions than in the study by Frank et al. [10].

Figure 49 presents a secondary electron image of the non-molded sample. This image gives a good visualization of the cone-like structure of the tapered TSVs.

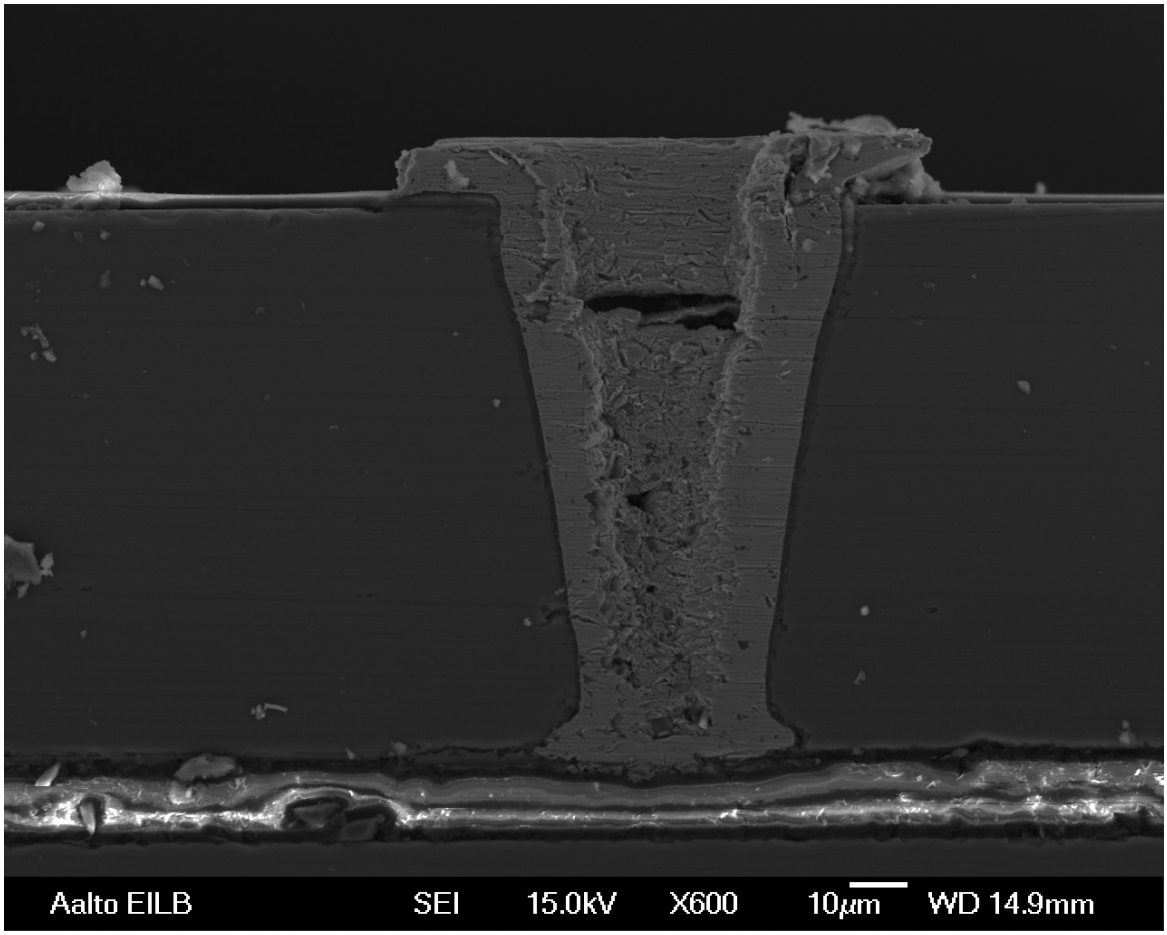

Figure 49: Secondary electron image of the non-molded sample.

9. Conclusion

In this master's thesis the reliability of the copper filled TSVs were investigated via literature survey. Also, experimental studies were carried out to assess the lifetime and the reliability of partially copper-filled tapered blind TSVs. The literature survey was focused on the fabrication process steps of the TSV and the reliability challenges of aforementioned steps. Moreover, the main reliability issues of the TSVs were introduced: diffusion of the copper to active silicon region, dielectric breakdown of the insulation layer, electromigration and thermal reliability. The experimental studies consisted of resistance measurements during thermal cycling test, construction of FEM models, creation of Weibull lifetime distributions, sample preparation and imaging of the test samples with SEM.

Thermal cycling test was conducted with nine samples, six of them had 420 vias and three of them had 1400 vias. Resistance measurements were carried out during the test and the samples were considered as failed when open circuits appeared. All of the test samples failed prior to 4000 temperature cycles.

The reliability results showed that the samples with more vias were more durable than the samples with less vias. This is illogical; samples with more vias should have a higher probability to form an open circuit. The test results can be considered as statistical anomaly, because of the small amount of test samples. Resistance increased evenly in daisy chain loops in all but one sample. Constant resistance increase indicates simultaneous formation and propagation of defects in TSV structures without imminent failure in sight. Whereas, rapid resistance increase indicates propagation of crack to a critical size and thus failure is imminent.

Weibull analysis was carried out based on the measurements during the thermal cycling test. The sample size of the chips with 1400 vias was so small that the analysis results were deemed unreliable. However, Weibull analysis was carried out successfully with 420 via samples. The results show that after 1000 temperature cycles approximately 10 % of the samples will fail and similarly after 4000 temperature cycles approximately 75 % of the samples will fail. Since it is enough that one via breaks and causes open circuit in a chip, a rough estimation was made for a probability of failure for a random single via. The result was that after 1000 cycles a probability for a random via to fail is 0,024 %.

Finite element method simulations indicated that the tapered annular vias are the most reliable via profiles when exposed to thermal stresses. The critical point of failure was the same in every simulation, the intersection between copper and silicon dioxide at the bottom of the via. The failures were noticed exactly at these locations in SEM images. Samples were molded in epoxy and mechanically grinded and polished in order to get cross-sectional images of failures. This method was deemed acceptable even though grinding caused damages to the TSV structure. The failures were open circuits and therefore easily recognizable from the damages caused by grinding.

The fabrication process was deemed to have formed the defects that caused failures. Cracks seemed to initiate from inside the vias at the intersection of the bottom of the via and the via sidewalls and propagate towards the insulation layer. If the defects were caused by thermal cycling, they would initiate from the maximum stress areas at the via edges and then propagate inwards, toward the center of via. Since the origins of the defects were different than simulations indicated, more test samples should be examined with better sample preparation techniques in order to be certain of the cause and the origin of the failures.

10. References

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APPENDIX A

Arithmetic means of measured resistance values during thermal cycling test

Number of cycles	chip 1 (Ω)	chip 2 (Ω)	chip 3 (Ω)	chip 4 (Ω)	chip 5 (Ω)	chip 6 (Ω)	chip 7 (Ω)	chip 8 (Ω)	chip 9 (Ω)
0	72.0	68.5	68.2	72.6	72.4	73.7	65.2	119.2	66.1
184	74.0	69.8	69.6	75.2	73.2	-	68.3	153.5	69.7
378	75.1	70.9	70.2	75.6	74.5	-	71.4	153.9	72.9
618	80.2	74.2	76.9	80.9	80,4	-	82.4	158.3	87.6
1086	81.3	77.3	78.2	81.4	-	-	97.1	161.9	94.3
1421	81.9	81.2	81.7	83.3	-	-	114.6	184.6	104.3
1758	83.4	84.2	88.9	90.3	-	-	129.9	-	112.7
2089	-	-	90.8	92.4	-	-	150.1	-	120.2
2426	-	-	95.0	99.8	-	-	166.6	-	128.4
2738	-	-	100.2	-	-	-	184.7	-	141.3
3071	-	-	103.4	-	-	-	204.7	-	151.2
3598	-	-	111.4	-	-	-	-	-	-
3972	-	-	-	-	-	-	-	-	-