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Dopamine oxidation readout sensor interface in 65 nm CMOS technology

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ABSTRACT OF THE
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Sensing and monitoring of neural activities within the central nervous system has become a fast-growing area of research due to the need to understand more about how neurons communicate. Several neurological disorders such as Parkinson's disease, Schizophrenia, Alzeihmers and Epilepsy have been reported to be associated with imbalance in the concentration of neurotransmitters such as glutamate and dopamine [1] - [5]. Hence, this thesis proposes a solution for the measurement of dopamine concentration in the brain during neural communication.

The proposed design of the dopamine oxidation readout sensor interface is based on a mixed-signal front-end architecture for minimizing noise and high resolution of detected current signals. The analog front-end is designed for acquisition and amplification of current signals resulting from oxidation and reduction at the biosensor electrodes in the brain. The digital signal processing (DSP) block is used for discretization of detected dopamine oxidation and reduction current signals that can be further processed by an external system.

The results from the simulation of the proposed design show that the readout circuit has a current resolution of 100 pA and can detect minimum dopamine concentration of 10 μMol based on measured data from novel diamond-like carbon electrodes [6]. Higher dopamine concentration can be detected from the sensor interface due to its support for a wide current range of 1.2 μA($\pm$600 nA). The digital code representation of the detected dopamine has a resolution of 14.3-bits with RMS conversion error of 0.18 LSB which results in an SNR of 88 dB at full current range input. However, the attained ENOB is 8-bits due to the effect of non-linearity in the oscillator based ADC. Nonetheless, the achieved resolution of the readout circuit provides good sensitivity of released dopamine in the brain which is useful for further understanding of neurotransmitters and fostering research into improved treatments of related neurodegenerative diseases.

Keywords: Dopamine, Neurotransmitter, Neurochemical, Neurosensing, Biosensor, Biomedical, Bioelectronics, Sensor interfaces, Integrated potentiostat, CMOS readout circuits, Mixed signal front-end

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Keskushermoston aktiivisuuden havainnointi ja tarkkailu on muodostunut tärkeäksi tutkimusalaksi, sillä tarve ymmärtää neuronien viestintää on kasvanut. Monien hermostollisten sairauksien kuten Parkinsonin taudin, skitsofrenian, Alzheimerin taudin ja epilepsian on huomattu aiheuttavan muutoksia välittäjäaineiden, kuten glutamaatin ja dopamiinin, pitoisuuksissa [1] - [5]. Aiheeseen liittyen tässä työssä esitetään ratkaisu dopamiinipitoisuuden mittaamiseksi aivoista.

Esitetty dopamiinipitoisuuden lukijapiiri perustuu sekamuotoiseen etupäärakenteeseen, jolla saavutetaan matala kohinataso ja hyvä tarkkuus signaalien ilmaisemisessa. Suunniteltu analoginen etupää kykenee lukemaan ja vahvistamaan dopamiinipitoisuuden muutosten aiheuttamia virran muutoksia aivoihin asennetuista elektrodeista. Digitaalisen signaalinkäsittelyn avulla voidaan havaita dopamiinin hapettumis-ja pelkistymisvirtasignaalit, ja välittää ne edelleen ulkoisen järjestelmän muokattavaksi.

Simulaatiotulokset osoittavat, että suunniteltu piiri saavuttaa 100 pA virran erottelukyvyn. Simuloinnin perustuessa hiilipohjaisiin dopamiinielektrodeihin piiri voi havaita 10 μMol dopamiinipitoisuuden [6]. Myös suurempia dopamiinipitoisuuksia voidaan havaita, sillä etupäärajapinta tukee 1.2 μA($\pm$600 nA) virta-aluetta. Digitaalinen esitysmuoto tukee 14.3 bitin esitystarkkuutta 0.18 bitin RMS virheellä saavuttaen 88 dB dynaamisen virta-alueen. Saavutettu ENOB (tehollinen bittimäärä) on kuitenkin 8 bittiä oskillaattoripohjaisen ADC:n (analogia-digitaalimuuntimen) epälineaarisuuden takia. Saavutettu tarkkuus tuottaa hyvän herkkyyden dopamiinin havaitsemiseksi ja hyödyttää siten välittäjäainetutkimusta ja uusien hoitomuotojen kehittämistä hermostollisiin sairauksiin.

Avainsanat: Dopamiini, Välittäjäaine, Neurokemia, Aivomittaus, Bioanturi, Biolääketiede, Bioelektroniikka, Anturirajapinnat, Sulautettu potentiostaatti, CMOS lukijapiirit, Sekamuotoinen signallietupää

Preface

The work presented in this thesis was carried out in the Electronic Circuit Design Laboratory of the Department of Micro- and Nanosciences at Aalto University. The proposed design was implemented and fabricated on-chip as part of a collaborative project called Neurosens, between other departments in School of Science and Electrical Engineering, funded by Aalto University. As a result, measurement data from the sensor electrodes were provided by the Department of Electronics.

I would like to express my gratitude to my thesis supervisor, Professor Kari Halonen and instructor Marko Kosunen for their guidance and support during the design and implementation of this thesis. I especially appreciate their commitment and devotion to the success of this thesis and for the privilege to implement this thesis as a microchip. I am very thankful to my instructor Marko Kosunen for detailed and clear instructions, valuable advice and suggestions, insights into more complicated concepts and practical contributions during the completion of this thesis.

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I am also thankful to all personnel and researchers at the laboratory for providing a warm and efficient learning environment. I wish to thank Olli Viitala, Tero Tikka, Enrico Roverato and Professor Jussi Ryynänen for their technical support and help throughout the implementation of this thesis and especially towards the submission of the readout chip to fabrication. In addition, I warmly thank my fellow colleagues Jakub Groniz and Shailesh Chouhan with whom I shared a room, for interesting discussions and exchange of ideas. Thanks to Antti Ontronen for cross-checking the Finnish translation of the Abstract.

Finally, I am deeply grateful to my parents for their relentless efforts in teaching and showing me the importance of diligence and hard-work. I am extremely thankful to my family, friends and in-laws for their moral and spiritual support throughout this entire process of studying abroad. I also wish to remember my beloved nephew Ayodeji Taiwo who passed away during the completion of this work. I know you were watching over me and you would forever be missed. Last and most definitely not the least, I would like to express my heartfelt appreciation to my husband Muyiwa Olabode for his patience and tremendous love. This work would not have been accomplished without your support. To God Almighty for the breath of life and for sustaining me through this phase of my life, I am eternally grateful.

Otaniemi, 10.10.2014

Olaitan I. Olabode

Contents

Symbols and abbreviations

Abbreviations

A/D	Analog-to-digital
AC	Alternating current
ADC	Analog-to-digital converter
AE	Auxiliary electrode
AFE	Analog front-end
AP	Action potential
BW	Signal bandwidth
CA	Chronoamperometry
CCO	Current controlled oscillator
CCS	Carboxylated carbonaceous spheres
CE	Counter electrode
CFM	Carbon-fibre microelectrodes
CIC	Cascaded integrated comb
CM	Current mirror
CMOS	Complementary metal-oxide-semiconductor
CMRR	Common-mode rejection ratio
CNS	Central nervous system
CNT	Carbon nanotubes
CT	Computed tomography
CV	Cyclic voltammetry
D/A	Digital-to-analog
DA	Dopamine
DAC	Digital-to-analog converter
dB	Decibels
DBS	Deep brain stimulation

DC	Direct current
DEM	Dynamic element matching
DIFF	Differential
DIFF-CCO	Differential current controlled oscillator
DLC	Diamond-like carbon
DNL	Differential nonlinearity
DNW	Deep N-well
DOQ	Dopamine-ortho-quinone
DORSI	Dopamine oxidation readout sensor interface
DPV	Differential pulse voltammetry
DR	Dynamic range
DSP	Digital signal processing
ECG	Electrocardiography
EEG	Electroencephalography
EIS	Electrochemical impedance spectroscopy
ENOB	Effective number of bits
FFT	Fast Fourier Transform
FOM	Figure of merit
FSCV	Fast-scan cyclic voltammetry
GBW	Gain bandwidth
GC	Gray code counter
GCE	Glassy carbon electrode
HBC	Human Body Communication
I-F	Current-to-Frequency
I/O	Input/Output
IA	Current acquisition
IC	Integrated circuits

ICMR	Input common mode range
ID	Current discretization
INL	Integral nonlinearity
ISM	Industrial, Scientific and Medical
LNA	Low-noise amplifier
LO	Local oscillator
LOD	Limit of detection
LSB	Least significant bit
LVDS	Low voltage differential signalling
MedRadio	Medical Device Radiocommunications Service
MICS	Medical Implant Communication Service
MOS	Metal-oxide-semiconductor
MRI	Magnetic resonance imaging
MWCNT	Multi-walled carbon nanotubes
N-OTA	Miller NMOS-based OTA
OPAMP	Operational amplifier
OSC	Oscillator
OTA	Operational transconductance amplifier
P2S	Parallel-to-serial
PBS	Phosphate buffered saline
PET	Positron emission tomography
PM	Phase margin
POW	Power management module
PSD	Power spectral density
PSRR	Power supply rejection ratio
RE	Reference electrode
REDOX	Reduction and oxidation

RF	Radio frequency
RFIC	Radio frequency integrated circuits
RFID	Radio frequency identification
RHP	Right-half-plane
RMS	Root mean square
S2P	Serial-to-parallel
SAR	Specific absorption rate
SE	Single-ended
SE-CCO	Single-ended current controlled oscillator
SEM	Scanning electron microscopy
SFDR	Spurious-free dynamic range
SIE	Sensor interface electronics
SNDR	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
SPECT	Single photon emission computerized tomography
SQNR	Signal-to-quantization noise ratio
SR	Slew-rate
SWCNT	Single-walled carbon nanotubes
UWB	Ultra Wide Band
VCCS	Voltage controlled current source
VHDL	VHSIC Hardware Description Language
VHSIC	Very High Speed Integrated Circuit
WE	Working electrode
WMTS	Wireless Medical Telemetry Service

Symbols

A_e	Cross-sectional area of an electrode
C_e	Double-layer capacitance of an electrode

I_{bg}	Background current
I_{cell}	Induced electrochemical cell current
I_{ox}	Oxidation current
I_{redox}	Induced redox current
I_{red}	Reduction current
O_I_{ref}	Bias current of the oscillator
O_{bulk}	Oxidized form an electroactive specie
R_{bulk}	Reduced form an electroactive specie
R_{WE}	Working electrode charge-transfer resistance
V_{cell}	Electrochemical cell voltage
V_{CE}	Voltage over the counter electrode
V_{redox}	Applied redox voltage
β	MOS device transconductance parameter
ΔC	Conversion error
ΔF_{osc}	Change or deviation in oscillation frequency
ΔI_{min}	Minimum change in current
ΔT	Total timing error
ΔV_{dd}	Change or deviation in supply voltage
$\epsilon_t(t)$	Timing error or jitter
γ	MOS device bulk threshold parameter
κ	Boltzmann's constant
μ_0	Effective charge carrier mobility of a MOS device
ϕ_F	MOS device strong inversion surface potential
τ_d	Propagation time delay of each inverter stage
C	Conversion codes
C_c	Miller compensation capacitor
C_L	Output load capacitance of the OTA

C_l	Load capacitance of each inverter stage
C_{ox}	Gate-oxide capacitance of a MOS device
D_{OUT}	Data output
DA_{conc}	Dopamine concentration
DIG_OUTM	Negative digital output
DIG_OUTP	Positive digital output
E_I_{ref}	Reference current for subtraction/addition of I_{cell} from the sensor electrodes
f_{-3dB}	-3dB frequency or open-loop bandwidth
f_c	Cut-off frequency of a filter
F_{osc}	Oscillation frequency
F_s	Sampling frequency
g_{ds}	MOS device drain-source transconductance
G_{II}	Gain of output stage of the OTA
G_I	Gain of input stage of the OTA
g_m	MOS device transconductance
I_{bias}	Bias current
I_{ctrl}	Oscillator control current
I_{ds}	NMOS device drain-source current
I_D	MOS device drain current
I_{sd}	PMOS device drain-source current
$meas\_trig$	Sampling clock that triggers measurement of pulses from the oscillator and defines the decimation rate of the ID block
N	Number of stages of the oscillator
n	Digital output code resolution
N_p	Number of pulses from the oscillator or I-F stage
N_s	Number of samples
osc_in	Input signal from the oscillator

OSC_OUTM	Negative oscillator output
OSC_OUTP	Positive oscillator output
p_2	Output pole of the OTA
P_{cons}	Power consumption
P_{osc}	Power consumption of the oscillator
Q_{in}	Quantity of interest from sensor
R_o	Output resistance of each inverter stage
r_o	MOS device output resistance
T_{meas}	Measurement time
T_{osc}	Oscillator period
T_s	Sampling time interval
V_{bias}	Input bias voltage
V_{dd}	Supply voltage
V_{ds}	MOS device drain-source voltage
V_d	MOS device drain voltage
V_{gs}	MOS device gate-source voltage
V_g	MOS device gate voltage
V_{icm}	Input common mode voltage
V_{in}	Bias voltage of OTA1 in the IA block
V_{ov}	Overdrive voltage of a MOS device
V_{ref}	Bias voltage of OTA2 in the IA block
V_{RE}	Voltage at the reference electrode
V_{SB}	MOS device source-bulk voltage
V_{ss}	Ground voltage
V_{th}	MOS device threshold voltage
V_T	MOS device thermal voltage
V_{WE}	Voltage at the working electrode
z_1	Right-half-plane zero of the OTA
M	Multi-bit digital code

1 Introduction

In recent years, the need for real-time monitoring of physiological activities in the human body has accelerated the development of biomedical sensors. Thus, biosensing has become a fast-growing area of research especially the design of implantable and wearable devices for various biomedical applications. The use of biosensors in a wide range of biomedical applications provides possibility for remote monitoring and diagnosis of patients, improved treatment of diseases, compensating or restoring lost function to a part of the human body, further study and analysis of disorders that experts lack sufficient understanding about or that are incurable [7], [8], [9], [10]. An important application area that benefits from this bio-technological advancement is sensing and monitoring of neural activities in the brain.

Neurological activities in the brain are mainly transmitted by neuroelectrical or neurochemical signals that control the central nervous system of the human body. Transmission of neurochemical signals between neurons are carried out by bio-agents or bio-markers known as neurotransmitters. Neurochemical signals are responsible for controlling cognitive, learning and memory functions in the brain. Thus, neurological disorders such as Parkinson's disease, Epilepsy, Schizophrenia, Huntington's disease and Alzeihmers have been associated with deficient or unstable level of neurotransmitters such as glutamate and dopamine [1], [2], [3], [4], [5]. In addition, dopamine as a neurotransmitter undergoes two main reactions during transmission of neurochemical signals. Hence, the goal of this thesis is to detect the oxidation and reduction reaction cycles of dopamine from the biosensor interface in the brain.

Detection of neurological signals has its challenges which define the minimum limits of sensitivity and resolution of the sensor interface. These limitations are due to inherent noise sources that are introduced from surrounding tissues through contact interface with the biosensor. In addition, neurochemical signals have very small signal amplitudes at low frequencies. Thus, the main design requirement of the sensor interface to be able to achieve good signal quality is reduction of noise. Other requirements of the readout sensor interface include high sensitivity, high resolution, large dynamic range and low power consumption [3], [4], [5]. The proposed design of the readout sensor interface is based on a mixed-signal front-end architecture which combines both analog and digital circuits to minimize noise and discretize the detected dopamine current signals for further external processing.

Detection and monitoring of dopamine in the brain plays a vital role in improving the treatment of neurological disorders which may lead to reduced tremors, seizures and ultimately longer life expectancy of patients suffering from related diseases. Furthermore, the possibility of real-time monitoring and analysis of dopamine levels in affected patients will provide further understanding of neurotransmitters. Hence, this thesis presents the design and implementation of a proposed solution for readout of dopamine oxidation and reduction in 65 nm CMOS technology. Concepts related to neurochemical sensing and biomedical readout circuits are discussed in chapter 2. Subsequently, detailed description of the system level design of DORSI is presented in chapter 3. Finally, chapter 4 presents simulation results based on measured data from the sensor and inferences from the results are concluded in chapter 5.

2 Background

From the development of the electron microscope in the 1930s to the design of implantable pacemakers, the importance of advancement in electronics to the study of biology and medical instrumentation is undeniable [7]. The impact of rapid development in the evolving field of bioelectronics has become evident in various application areas such as medicine, environment, forensics and homeland security [7], [8]. Thus, the fusion between biology and electronics has led to remarkable solutions to important needs in the medical industry such as pathogen detection and analysis, disease prevention and treatment, compensating or restoring lost functions like sight, hearing and movement [7], [9]. Furthermore, there have been several bio-electronic innovations over past decades especially in the area of medical imaging, prosthetics and implantable devices; from which some examples are listed below.

- **Medical imaging devices**: electrocardiograph (ECG or EKG) , ultrasound, magnetic resonance imaging (MRI) , computed tomography (CT) , positron emission tomography (PET) and Electroencephalography (EEG) [7], [8].
- **Prosthetics and implantable devices**: cochlear implants, retinal or cortical implant, muscle implants, cardiac pacemaker and defibrillators, glucose monitoring device, implantable neural electrodes and probes [9], [7], [11].

Despite the aforementioned breakthroughs in the development of bio-electronic devices, there are still areas open to further research and new emerging needs related to personalised healthcare. Thus, the demand for wearable, implantable and wireless devices is increasing and providing more research opportunities in a wide range of biomedical applications. In addition, the miniaturization of electronic devices as a result of the exponential growth in semiconductor technology as predicted by Moore's law [1], has also been a driving force behind recent development in the field of bioelectronics. Hence, advances in semiconductor technology and development of bio-compatible materials offer promising prospects for future innovations in their application to life sciences especially in the design of biosensors.

The influence of development in the field of bioelectronics and semiconductor industry on sensing of biological molecules has increased in recent years [7]. Hence, one application area that benefits from the scaling down of electronics upto the nano-scale, is the field of neuroscience where there is a need for development of brain-machine interfaces that use detected neuron signals to control mobility functions in artificial prostheses [10], [13]. Another application that profits from advances in semiconductor technology is the design of closed-loop interfaces for sensing, monitoring, analysis and stimulation of neural activities in the brain [14]. Thus, measurement of dopamine concentration from the brain contributes to the realization of fully-implantable closed-loop interfaces.

[1] Gordon E. Moore, the co-founder of Intel Corporation (formerly Fairchild Semiconductor) predicted in 1965 that the number of components on integrated circuits will double every 18-24 months [12]. Subsequently increasing computational power and speed while the cost and size reduces for each generation of an electronic device.

2.1 Neurotransmitters

Further knowledge about how neurons communicate and transmit information within the central nervous system is of significant value to researchers in the field of neuroscience for improving treatment of neurological disorders and neurodegenerative diseases. Neurons in the central nervous system (CNS) are connected by synapses and communicate through electrical and chemical impulses or signals. Figure 2.1 describes the basic structure of neurons and their interconnections to synapses. In addition, neurons transmit information mainly via electrical signals also known as action potentials (AP) which travel across electrical and chemical synapses (i.e. the gap between two neuron cells). Neurotransmission originates from the neuron cell body where an action potential is initiated and travels along the axon to the synapse. Thus, neurotransmission in the brain can be classified into electrical neurotransmission (i.e. transfer of AP across electrical synapse) and chemical neurotransmission (i.e. transfer of AP across chemical synapse) as illustrated in Figure 2.2.

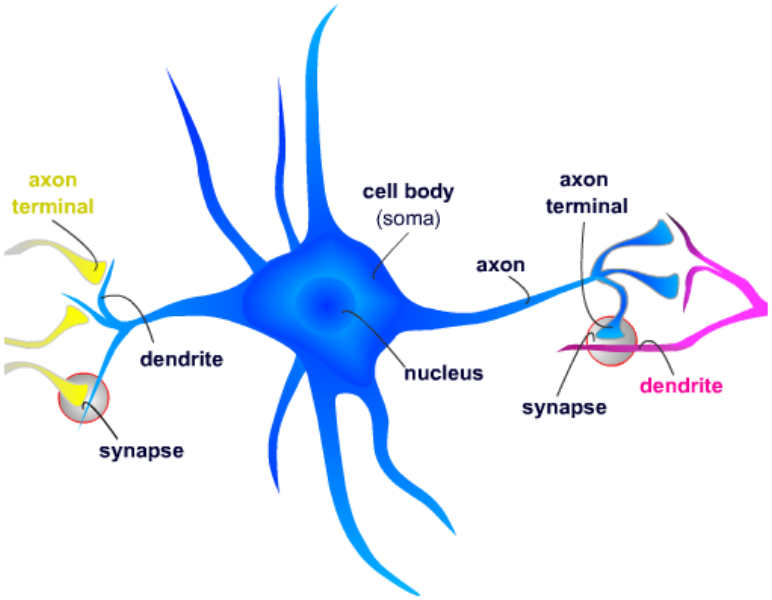


Figure 2.1: Structure of neurons [15].

Electrical neurotransmission occurs rapidly over long distance from the neuron cell body to the axon terminal and across electrical synapses in the order of 150 m/s within the central nervous system [15]. Electrical synapses are conductive by nature due to the existence of synaptic gap junctions between dendrites that aid the transmission of an AP as shown in Figure 2.2. On the other hand, chemical neurotransmission occurs over shorter distance in the order of $(20 - 30)$ nm; across chemical synapses as a result of discharge and absorption of biochemical molecules also known as neurotransmitters [3], [15], [16]. Neurotransmitters are released in chemical synapses which are non-conductive by nature, to provide a "short" between an incoming AP and the synaptic potential that is established within the synaptic cleft as shown in Figures 2.3a and 2.3b [15], [17]. The synaptic cleft is the region of

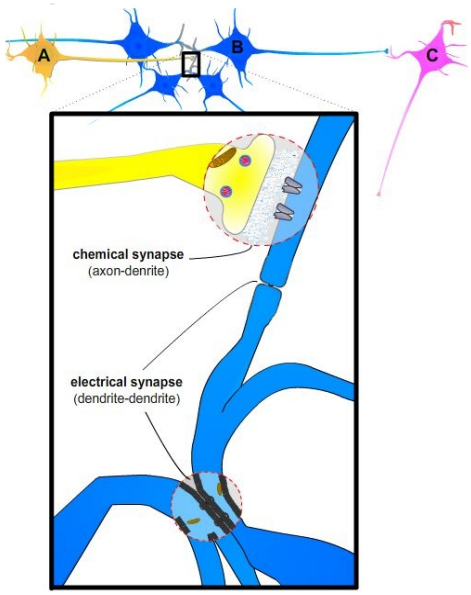
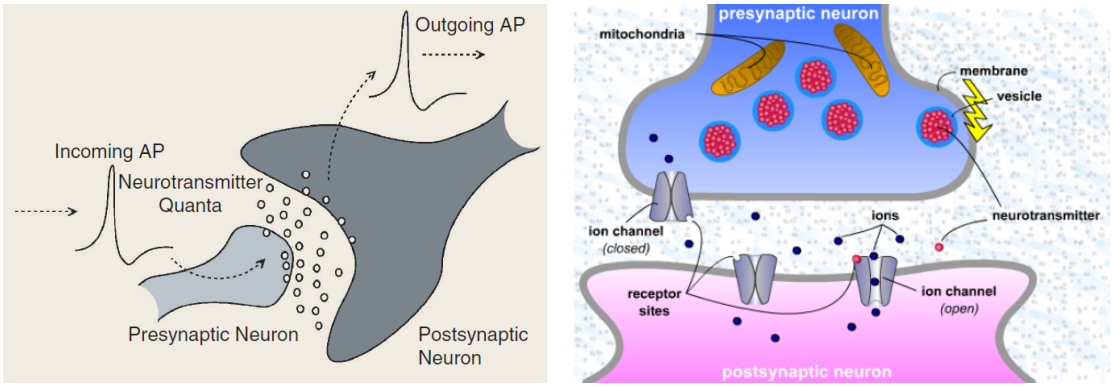


Figure 2.2: Electrical and chemical synapses [15].

$\sim 1\ \mu\text{m}^2$ between axon terminals and dendrites that is filled with extracellular fluid [15], [16]. Hence, transmission of action potentials between pre-synaptic (source) and post-synaptic (target) neurons across the synaptic cleft is carried out chemically by neurotransmitters such as dopamine and glutamate as depicted in Figure 2.3a.

The process of chemical neurotransmission involves the transfer of ions such as sodium (Na^+), potassium (K^+) and calcium (Ca^{++}) through open ion channels when an action potential (in yellow) arrives at the pre-synaptic neuron as illustrated in Figure 2.3b [15], [16], [18]. The ion channels that are attached to the target neuron are opened when neurotransmitters released from vesicles through the pre-synaptic neuron membrane, adhere to post-synaptic receptor sites. The movement of ions from the source neuron to the target neuron induces current flow in the synaptic cleft which changes the electrical properties of the post-synaptic neuron membrane. Thus, producing a synaptic potential in the target neuron which increases as a result of exchange of ions through the open ion channels, until the sum of synaptic potentials of the target neuron is larger than the resting potential of the post-synaptic neuron membrane. This threshold is reported to be within -40 mV to -80 mV and the generated AP is known to last a few milliseconds depending on the type of ion channels, nature of receptors and neurotransmitters [15], [16], [18]. Furthermore, after the transmission of the stimulated outgoing AP, neurotransmitters are removed from the synaptic cleft and absorbed back into the pre-synaptic neuron also known as the process of re-uptake. The absorbed neurotransmitters are recycled and form new vesicles from the energy produced by the mitochondria structures in the pre-synaptic neuron. Hence, the release and re-uptake of electro-active neurotransmitters result in oxidation and reduction reactions during chemical neurotransmission.

Dopamine as a neurotransmitter is known to be primarily responsible for coordination, learning and memory functions in the brain [1]. Other functions of dopamine



(a) AP transfer through chemical synapse [17]. (b) structures at chemical synapse [15].

Figure 2.3: Chemical neurotransmission.

include behavioural changes, blood flow regulation and aiding secretion of hormones that control eating habits, appetite, sense of reward, pain and pleasure [1], [19], [20]. Thus, several cognitive and mobility related disorders have been attributed to imbalance in the concentration level of dopamine released in the brain during communication between neurons. In addition, irregular transmission of dopamine due to deficient or dysfunctional dopamine receptors has also been reported to be linked with various neurological and psychiatric disorders such as Parkinson's disease, Schizophrenia, Huntington's disease, Alzheimers, Epilepsy, senile dementia, drug addiction, depression, bipolar disorder and Tourette's syndrome [1], [2], [3], [5], [14], [6], [20]. In particular, Parkinson's disease has been associated with degeneration of dopamine neurons which leads to reduced concentration of dopamine that is released in the synaptic cleft [15], [19]. Thus, the resulting synaptic potential is insufficient to initiate an AP or the generated AP may occur late which in turn affects subsequent chain of reactions during transmission of information within the central nervous system.

The main cause of Parkinson's disease (i.e. a mobility disorder that results in muscle tremors, stiffness and instability in movement) remains unknown [3],[19]. Current treatments include medications and consumption of food reach in amino acids to increase the level of dopamine released in the brain. An alternative treatment in severe cases of Parkinson's disease is a neurosurgical technique for stimulating regeneration of dopamine neurons known as deep brain stimulation (DBS) [11], [14]. Hence, monitoring of the concentration of dopamine produced after DBS surgery and the response pattern of the generated action potential plays a vital role in improving the treatment of Parkinson's disease and other related disorders. Therefore, miniaturized closed-loop interfaces for real-time monitoring and stimulation of dopamine will provide pharmacologists and neuroscientists with further understanding about the structure and signalling mechanisms of dopamine as a neurotransmitter for development of new therapeutic medications for regulation of dopamine levels, correction or management of receptor abnormalities and regeneration of diminishing neurons.

2.2 Neurochemical sensing

As described in the previous section 2.1, neurotransmitters undergo electrochemical reactions in the brain during transmission of action potentials within the central nervous system. Neurotransmitters are either electrochemically active or non-electroactive by nature. Electrochemically active neurotransmitters such as dopamine, serotonin and histamine; produce reduction-oxidation (redox) currents in the presence of an induced action potential or applied electrical potential [3]. Thus, electroactive neurotransmitters can be directly detected from the brain by electrochemical transduction techniques. On the other hand, non-electroactive neurotransmitters such as glutamate need to be detected indirectly through their reactions with enzymes that produce electroactive biochemicals which can be detected [3], [4], [17].

Enzymatic sensing techniques monitor the products of the catalytic reaction that occurs between the enzyme and the specie of interest. Other quantities monitored by enzymatic indirect transduction include charge transfer, generation and transfer of heat which may result in detectable temperature gradient [21]. In the case of non-electroactive neurotransmitters, the concentration of the resulting electroactive product from the reaction is the quantity that is detected, not the concentration of the originating neurotransmitter. Available methods for in-direct detection of neurotransmitters include optical (based on light emitting reactions also known as chemiluminescence), liquid chromatography (based on separation of chemical ions) and imaging (based on single photon emission computerized tomography(SPECT) or PET) techniques [17], [20], [22]. Another method that can be used in the detection of neurotransmitters is based on affinity sensing techniques which monitor the chemical bonding between biochemical molecules and their corresponding receptors. Quantities such as changes in mass or refractive index can be detected and measured in affinity based biosensors which have been used in monitoring of changes at dopamine receptors [19], [21].

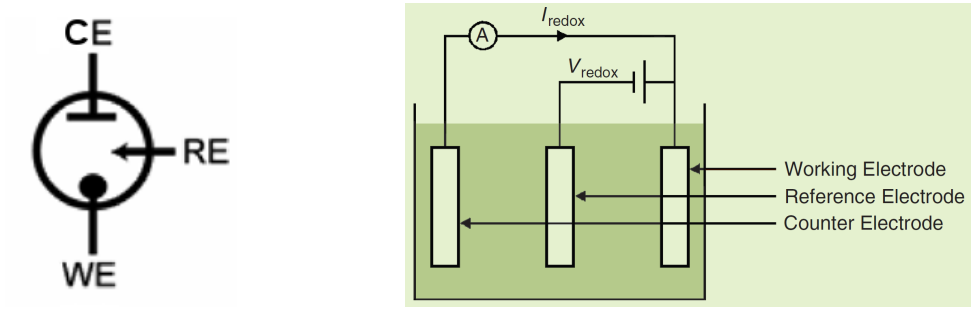
Considering the aforementioned techniques, direct electrochemical detection is the preferred option and most commonly used method for detection of dopamine and other electroactive neurotransmitters. In addition, it provides faster response, reproducible and more sensitive detection of changes in dopamine concentration due to direct relationship between the detected concentration levels and changes in measured currents [20]. Electrical signals induced by the flow of ions between neurons within the extracellular fluid of the synaptic cleft result in detectable forward and reverse currents corresponding to increase and decrease in the concentration of dopamine. Thus, variations in the dopamine concentration of the brain are further translated as activation or deactivation of specific functions within the CNS [1]. Furthermore, electrochemical analysis and measurement of induced currents can be easily integrated into miniaturized bioelectronic devices also known as potentiostats, that can be implanted for monitoring and regulation of dopamine levels.

2.2.1 Operation principle

Neurochemicals and related analytes such as dopamine, glutamate, histamine, adenosine, noradrenalin and serotonin; are monitored with the help of potentiostats which

operate based on electrochemical transduction principle [3], [23], [24]. Electrochemical transduction principle is the process of applying an electrical potential across an electrochemical cell and measuring the induced redox current within the cell. The electrochemical transduction principle was first applied to biosensors by Leland C. Clark Jr. in late 1950s in the design of electrodes used for sensing oxygen in the body or environment [25]. As a follow-up to the oxygen electrodes, Leland C. Clark Jr. designed the first glucose sensor based on the same principle in early 1960s [25]. The electrochemical transduction principle has since become an integral part of the design of biochemical sensors.

The structure of the electrochemical cell used in biosensors that apply the electrochemical transduction principle, is based on two or three electrodes namely working electrode (WE), reference electrode (RE) and counter electrode (CE) as shown in Figure 2.4. The counter electrode is also known as auxiliary electrode (AE) and can be discarded in the case of an electrochemical cell setup that utilizes two electrodes. The working electrode is where the electrochemical reaction occurs and the reference electrode is used for detecting the potential at which the reaction occurred with respect to the working electrode voltage. Therefore, the reference electrode is designed so that it is inert to the solution and the reaction occurring at the WE.



(a) cell symbol [26]. (b) electrochemical analysis setup [17].

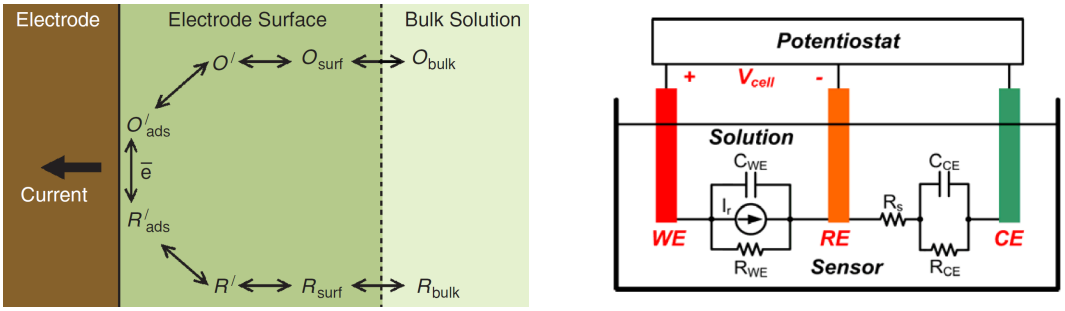
Figure 2.4: Electrochemical cell structure.

Potentiostats used in neurochemical monitoring are usually based on the three electrochemical cell structure as depicted in Figure 2.4b. Thus, the induced redox current I_{redox} is measured through the CE rather than through the RE, thereby minimizing instability in the reference voltage at the RE which is essential in ensuring stable cell voltage (V_{redox}). The readout circuit of the potentiostat is responsible for setting and controlling the cell voltage (V_{cell} or V_{redox}) at which the expected reaction occurs and measures the induced current through the cell (I_{cell} or I_{redox}). Hence, stability of the cell voltage is an important requirement in the design of the potentiostat for reducing inaccuracies in the detection of the corresponding oxidation voltage at which the measured current peaks.

There are several techniques reported for sensing neurochemicals in the brain, but the most common methods are chronoamperometry (CA) and cyclic voltammetry (CV) [3], [27]. The chronoamperometry technique involves the application of constant potential V_{redox} across the WE and RE, and measuring the induced current

I_{redox} through the CE. This method is appropriate for detecting neurochemical or biochemical molecules when the exact potential at which the expected electrochemical reaction occurs is known such as in glucose monitoring [27], [28]. Instead of chronoamperometry, cyclic voltammetry is used when the reaction potential is not accurately known which is the case for dopamine because the redox peak voltage varies for different patients and with the sensor electrode material [6]. However, the implementation of CV is more complex since it involves applying a range of voltages V_{redox} (typically a triangular waveform) across the WE and the RE in order to obtain a full redox current I_{redox} profile of the detected neurochemical. In addition, CV is especially useful for detecting both oxidation and reduction reactions of a neurochemical or biochemical within the forward and reverse voltage sweep of V_{redox}. Hence, this technique is an appropriate option for detection of dopamine where both oxidation and reduction reactions are of interest for studying the release and absorption patterns of dopamine.

Other forms of cyclic voltammetry are differential pulse voltammetry (DPV) and fast-scan cyclic voltammetry (FSCV) . DPV is based on applying a staircase or step-like triangular voltage waveform where the difference in the detected currents before and after each pulse or step is measured against the corresponding potential difference. Thus, very high sensitivity can be achieved with the DPV technique due to reduction in underlying background current [20]. However, the complexity of the design of the waveform generator and subsequently the implementation of the integrated potentiostat is increased. On the other hand, FSCV is based on very high voltage sweep rate of the applied voltage waveform. FSCV has become the preferred option in detection of neurotransmitters due to its high scan rate which has been reported to increase sensitivity and selectivity of the electrodes to neurochemicals [3], [6], [20]. In addition, the response rate of FSCV in neurochemical sensing is comparable to the response time of neurotransmitters released within the synaptic cleft which are swiftly removed during re-uptake process [3], [6]. Thus, the detection of dopamine with high resolution is achieved with FSCV which makes FSCV a well-suited approach for neurochemical monitoring.



(a) electrode-solution interface [17], [29]. (b) cell model [30].

Figure 2.5: Electrochemical transduction principle.

In depth understanding of the chemical interactions that occur at the electrode interface during FSCV is important for the design of the potentiostat. Hence, Figure

2.5a illustrates the electrochemical transformation that occurs between the electrode and the chemical solution or electrolyte which contains the electroactive specie. The bulk solution in Figure 2.5a corresponds to the the extracellular fluid in the synaptic cleft and the electroactive specie of interest is dopamine. Electrons are transferred between both mediums (electrode $\rightleftharpoons$ solution/electrolyte) as a result of redox reactions at the electrode surface. During the forward sweep of the applied voltage, the reduced form of the specie (R_{bulk}) is transformed to its diffused form (R_{surf}) as it approaches the surface of the electrode. The diffused form (R_{surf}) is further transformed to its adsorbed form (R_{ads}) after undergoing a chemical reaction ($R^{'}$) between the diffused form and chemical molecules at the electrode surface which results in electron loss (or oxidation). The oxidized form of the specie in its adsorbed state (O_{ads}) diffuses back into the solution to produce an oxidized form of the specie in its bulk state (O_{bulk}). Hence, the oxidation reaction that occurs during the forward voltage sweep can be simplified as follows, where n is the number of electrons (e^{-}) lost.

$$R_{bulk} \Rightarrow O_{bulk} + ne^{-} \tag{2.1.a}$$

$$R_{bulk} - ne^{-} \Rightarrow O_{bulk} \tag{2.1.b}$$

On the other hand, the reverse of the described process occurs during the reverse sweep of the applied voltage. Thus, the oxidized bulk form of the specie (O_{bulk}) is transformed to its diffused form (O_{surf}) and further into its adsorbed form (O_{ads}) after undergoing a chemical reaction ($O^{'}$) which results in electron gain (or reduction). The reduced form of the specie in its adsorbed state (R_{ads}) diffuses back into the bulk solution to produce the oxidized bulk form of the specie (R_{bulk}). Thus, the following equation holds during the reverse sweep for the reduction reaction of the oxidized form of the electroactive specie, where n is the number of electrons (e^{-}) gained.

$$O_{bulk} + ne^{-} \Rightarrow R_{bulk} \tag{2.2}$$

Therefore, the redox reaction that dopamine as an electroactive neurotransmitter undergoes during FSCV, can be expressed as in Equation (2.3). Equation (2.3) is based on Equations (2.1) and (2.2), where DOQ (dopamine-ortho-quinone) is the oxidized form of dopamine (DA) [3].

$$DOQ + 2e^{-} \Rightarrow DA \tag{2.3}$$

This redox cycle continues for every voltage sweep (V_{redox}) that is applied by the potentiostat across the WE and RE. Figure 2.5b describes the electrical representation of the electrode-solution sensor interface to the potentiostat. The electrical properties of the sensor interface and bio-compatibility issues are further discussed in section 2.2.2.

Electrochemical analysis based on the fast-scan cyclic voltammetry (FSCV) for the detection of dopamine is illustrated in Figure 2.6. The voltage sweep (V_{redox}) that is applied by the potentiostat is based on the scan rate of the FSCV setup

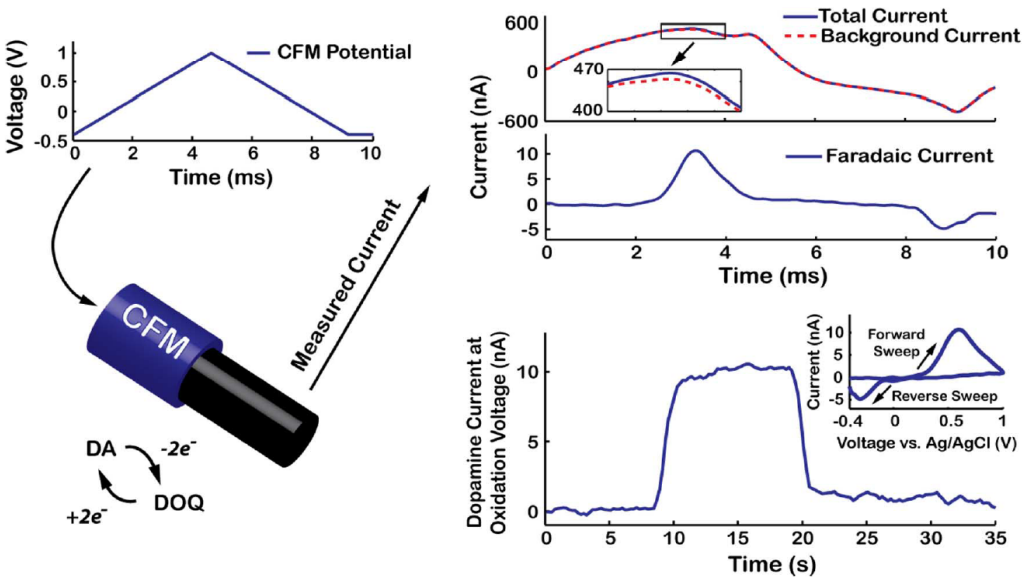


Figure 2.6: Detection of dopamine using FSCV [3].

and the sensitivity range of the working electrode to both oxidation and reduction reactions. Carbon-based electrodes are known to provide very good sensitivity and selectivity to dopamine and other neurotransmitters because they are easily oxidized by carbon molecules [6], [24]. The detected current (I_{cell}) is a combination of the faradaic current from the oxidation and reduction of the neurotransmitter (I_{redox}), and the background current (I_{bg}) from the electrodes. The background current is introduced as a result of local reactions at the electrode surface from residues of adsorbed redox products that have accumulated unto the electrode surface. Hence, subtraction or reduction of background current is necessary to be able to effectively detect the faradaic current due to dopamine which are typically in the order of tens of nano-amperes (nA) depending on the concentration of the released dopamine and the sensitivity of the electrode.

Another advantage for using FSCV technique is that the use of high scan rates aids averaging of generated background current which in turn improves the resolution of the detected faradaic current. In addition, identification of oxidation and reduction current peaks and corresponding voltages serve as indicators of the variation in dopamine concentration which is essential for neuroscientists in understanding more about the release and re-uptake mechanisms of neurotransmitters in the brain and improving treatments of patients with dopamine deficiency or imbalance in dopamine levels.

2.2.2 Sensor interface

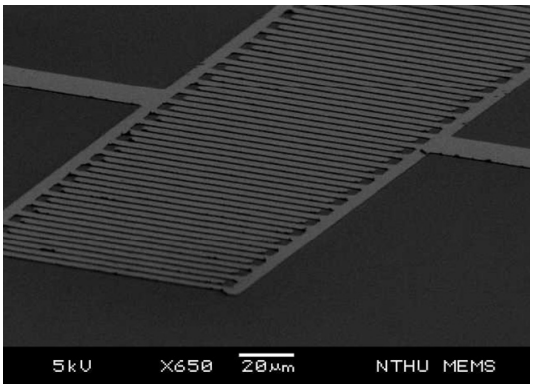
Considering the complex environment of the human body, with thousands of reactions occurring at the same time within few milliseconds, issues such as biocompatibility, sensitivity and selectivity of bio-electronic devices remain main chal-

lenges. In general, sensitivity and selectivity of stimulating and sensing electrodes are important requirements in the design of biosensors. Thus, the structure and selection of materials of the biosensor electrodes have a significant impact on the performance of biosensors. Bio-compatibility of materials used in biosensors is also an important criteria in the selection of electrodes used in bio-sensing, especially in the area of neurochemical monitoring. There are several materials used in the design of electrodes that are utilized in neurochemical sensors. The reference electrode (RE) is usually based on silver/silver-chloride (Ag/AgCl) due to its excellent electrical and chemical characteristics such as small and stable electrode offset voltage, low electrode-solution interface impedance and low charge-transfer resistance [31]. The auxiliary or counter electrode (CE) is often based on noble metals such as platinum (Pt) or gold (Au) due to their bio-compatibility characteristics [3], [20], [32], [33]. The selection of the working electrode (WE) material is the most critical of the three electrodes because the electrochemical reaction occurs at the surface of the working electrode.

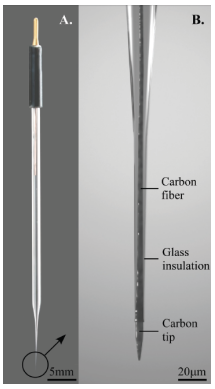
The most common WE materials used in detection of neurotransmitters are mainly a combination of carbon based materials, polymers, metal-oxides and noble metals [20]. Thus, there is more focus on research related to the design of working electrodes and the material used in order to improve its sensitivity, selectivity to the specific neurochemical of interest and biofouling reduction. Biofouling is the process of adsorption or accumulation of residual products from redox reactions onto the surface of the electrode [6]. As a result, the accumulated residue from the redox reactions changes the electrical properties of the electrode over time which causes a voltage drift in the WE voltage [7]. Consequently, the voltage drift in the WE voltage leads to inaccuracies in the measured current peaks and corresponding oxidation-reduction voltage. Hence, minimizing the effect of biofouling plays a key role in improving electrode sensitivity and resolution. Thus, reduction or elimination of biofouling remains an active area of research in the field of biomaterials for biochemical sensing.

The structure and dimensions of electrodes used in biosensing also play a major role in the performance of the biosensor. There are several design structures available for neurochemical sensing, but the most common electrode structures used in neurotransmitter detection are interdigitated electrodes and carbon-based nanostructures such as carbon-fibre electrodes and carbon nanotubes (CNT) as illustrated in Figures 2.7a, 2.7b and 2.8a. Another interesting carbon based nanostructure, that shows promising performance in detection of dopamine, is carboxylated carbonaceous spheres (CCS) as depicted in Figure 2.8b. CCS nanostructures are formed by attaching carboxyl groups to carbon spheres, which are prepared from glucose and finally depositing the CCS on glassy carbon electrodes (GCE), as illustrated in Figure 2.9. The use of CCS results in reduction of biofouling due to less adsorption of redox products at the electrode surface [20].

In addition, CCS also shows high selectivity towards dopamine due to reduced interference from other analytes within the same oxidation potential window such as ascorbic acid and uric acid [6], [20]. CCS provides good selectivity to dopamine as a result of large number of carboxyls that are present on the surface of the CCS-GCE

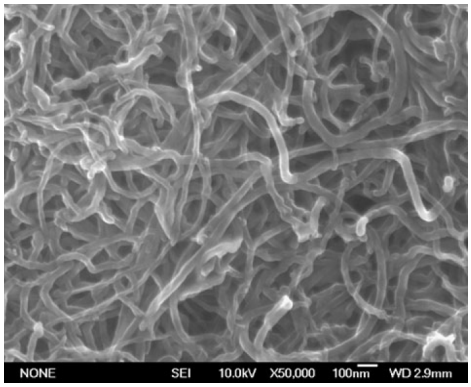


(a) interdigitated [32].

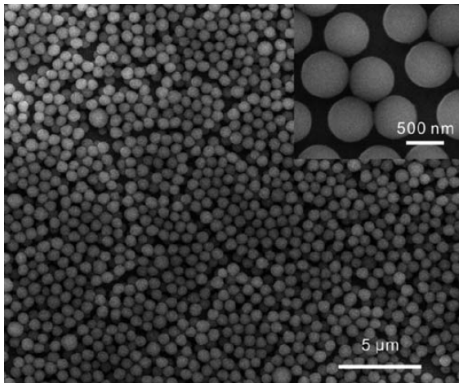


(b) carbon-fibre [33].

Figure 2.7: SEM images of common electrode structures used in neurochemical sensors.



(a) MWCNT [34].



(b) CCS [20].

Figure 2.8: SEM images of other electrode structures used in neurochemical sensors.

electrode [20]. However, one drawback of using CCS is that detection of reduction current peaks has not been achieved and a definite reason for this shortcoming is still under further research. Hence, CCS-GCE electrodes are not well-suited for detection of redox species such as dopamine despite their outstanding performance in terms of sensitivity, selectivity and bio-compatibility.

Furthermore, certain dimensions of electrode structures are vital in optimization of the performance of the electrode and biosensor. Some of these dimensions are the tip-length of carbon-fibre electrodes, gap-distance of interdigitated electrodes and diameter of CNT or CCS. For instance, increase in the tip-length of carbon-fibre microelectrodes (CFM) has been reported to increase the detected current sensitivity [33]. Likewise, increasing the diameter of CCS increases the total surface area that is exposed to the biochemical of interest and in turn increases the sensitivity of the electrode. In contrast to CCS and CFM, the sensitivity of the electrode increases as the gap between the generator and collector plates of the interdigitated electrodes reduces [22]. Typical sensitivity range of carbon-fibre electrodes is around

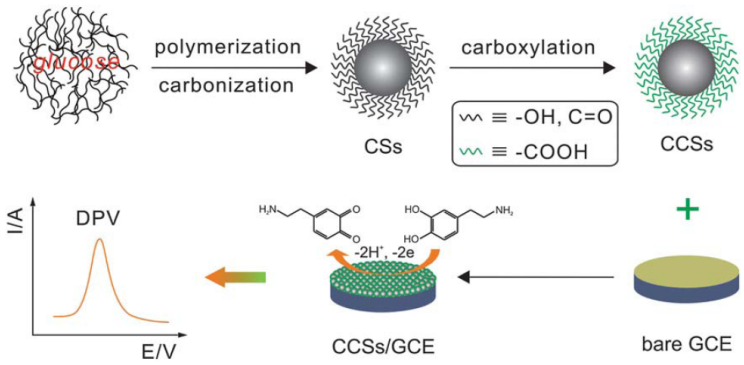


Figure 2.9: Fabrication of carboxylated carbonaceous spheres (CCS) on glassy carbon electrode (GCE) [20].

$(10 - 50)$ nA/μMol which is sufficient to detect dopamine concentrations which are usually within the range of 10 nMol $-$ 1 μMol in the synaptic cleft [3], [6]. Performance comparison between several other carbon-based structures that are used in the detection of dopamine are summarized in Table 2.1. It is important to note that the detection method (CV-based or DPV-based) and scan rates differ in some of the structures which also affects the performance values that are listed in the comparison table below.

Table 2.1: Performance comparison of common working electrode (WE) materials used in dopamine detection

Material and Structures	**Detection limit (μMol)**	**Sensitivity (nA/μMol)**	**Linear range (μMol)**
Nafion/MWCNT [4], [35]	0.07	16.26 ± 1.41	$2 - 20$
Poly-glutamic acid/SWCNT [36]	0.38	250 (i)	$3.3 - 26.6$
Poly-acrylic acid/MWCNT/GCE [37]	0.02	$4 * 10^3$ (ii)	$0.04 - 3$
Methylene blue/MWCNT [34]	0.2	$5.6 * 10^3$	$0.4 - 10$
Graphene modified electrode [38]	2.64	80 (iii)	$4 - 100$
Nitrogen-doped graphene [39]	0.25	~ 30	$0.5 - 170$
Graphene sheets/imprinted polymers [40]	0.1	~ 12.5	$0.1 - 830$
Chitosan-graphene modified electrode [41]	1	20 (iv)	$1 - 24$
Diamond-like carbon (DLC) electrode [6]	10	780 [2]	$10 - 100$
CCS-GCE [20]	0.03	450 (v)	$0.1 - 40$
Carbon-fiber microelectrode (CFM) [3]	0.0167	10.2	$0.125 - 1$
Interdigitated carbon electrodes [32], [22]	10^{-4}	0.57	$2 - 30$

i ii iii iv v estimated value: specific value not explicitly defined in the source

[2]Note: the sensitivity value of the DLC electrode given in Table 2.1 is based on the current density (μA/cm^2) values provided by the source [6].

The performance of the whole read out circuit depends significantly on the interface between the sensor and the potentiostat. The electrical model of the sensor as depicted in Figure 2.5b describes the impedance structure that exists at the sensor-potentiostat interface. Thus, the impedance model provides a means of estimating the input impedance that the potentiostat is expected to support. The total input impedance is based on the surface or faradaic resistances from the working and counter electrodes (i.e. R_{WE} and R_{CE}), inherent resistance from the solution (R_S) and the double-layer capacitances that are formed as a result of separation and accumulation of opposite charges at the WE and CE surface-solution interfaces [26], [30], [31]. The working electrode faradaic or charge-transfer resistance R_{WE} and the double-layer capacitances (i.e. C_{WE} and C_{CE}) have the following relationship with the electrode cross-section area.

$$C_e \propto k_c * A_e \tag{2.4}$$

where C_e is the double-layer capacitance of the electrode, A_e is the electrode cross-sectional area, and k_c is a constant which is estimated to be 0.36 μF/mm^2 [26].

$$R_{WE} \propto \frac{V_{cell}}{I_{cell}} \tag{2.5}$$

Since I_{cell} is directly proportional to A_e, Equation 2.5 can be simplified as:

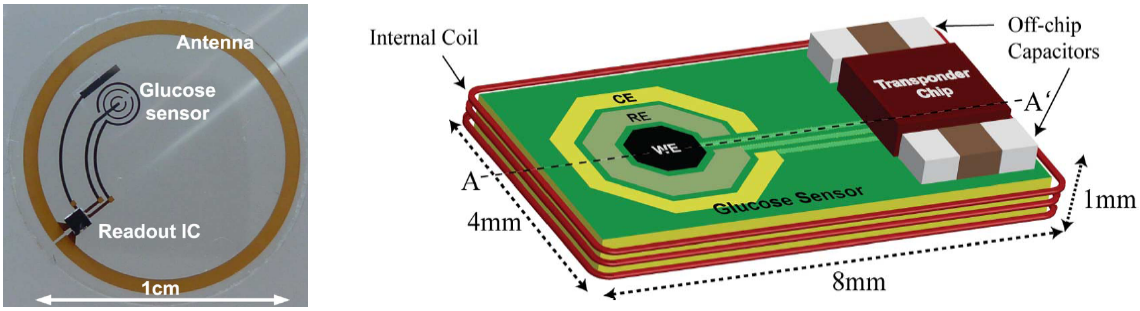
$$R_{WE} \propto \frac{V_{cell}}{A_e} \propto \frac{k_c * V_{cell}}{C_e} \tag{2.6}$$

Therefore, R_{WE} is inversely proportional to the electrode area A_e while C_e is directly proportional to A_e; which implies that R_{WE} is inversely proportional to the double-layer capacitance of the electrode C_e. Hence, increasing the electrode area will result in larger detectable current as a result of reduced surface resistance. Thus, improving the sensitivity and resolution of the sensor. On the other hand, increasing the electrode area, increases the double-layer capacitance which in turn increases the adsorption of products (or biofouling) at the electrode surface. Thus, increasing the background current, which reduces the sensitivity of the potentiostat and ultimately degrades the performance of the whole readout circuit.

In addition, the use of FSCV at high scan rates increases the double-layer capacitances due to its dependence on frequency [31]. There are a few techniques reported for reducing the effect of double-layer capacitances due to fast sweep rates of the cell voltage V_{cell} [24]. These techniques include the use of large amplitude sinusoidal voltammetry, square-wave voltammetry, and fourier transformed alternating current (AC) voltammetry. [42], [43], [44]. Another way to mitigate the effect of double-layer capacitances and to maximize the performance of the sensor is the use of carbon-based materials which are known to provide large surface area whilst having good and stable surface chemistry (i.e. charge-transfer characteristics) [20]. Thus, biofouling is reduced, which makes carbon-based materials and structures more beneficial for biochemical and neurochemical monitoring. As a result, carbon-based materials provide high sensitivity and improved bio-compatibility when compared with other materials.

2.3 Biomedical readout circuits

Emerging need of personalized healthcare and rising demand for devices that offer real-time monitoring of physiological activities in several biomedical applications are the main driving forces behind recent development in the design of biomedical readout circuits. The primary function of readout circuits that are used in biomedical applications is to detect physiological quantities of interest and convert the detected signals to another form (usually electrical or optical) which can be further processed to extract meaningful information about specific phenomena. Typical quantities of interest that are monitored by biomedical readout circuits include biochemicals, thermal changes, bio-electrical signals such as in EEG and ECG. Figures 2.10 and 2.11 present examples of state of the art implementation of biomedical readout circuits used in glucose and neurochemical measurements.



(a) Eye-tear glucose readout [45]. (b) Blood glucose readout [46].

Figure 2.10: Glucose monitoring wireless readout devices.

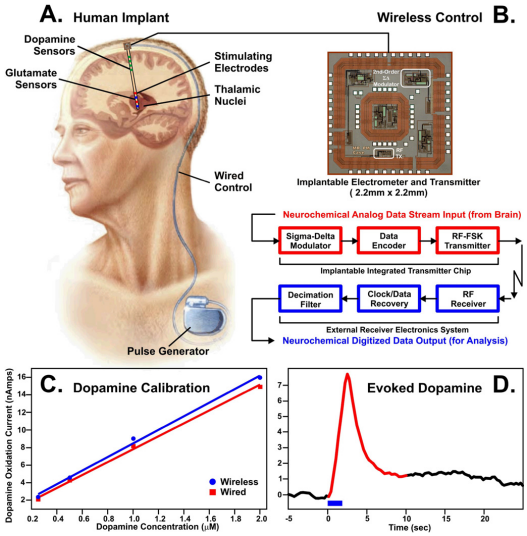


Figure 2.11: State-of-the-art of neurochemical wireless monitoring [14].

A 3 μW wirelessly powered active contact lens glucose sensor for real-time monitoring of glucose from eye tear fluid is shown in Figure 2.10a and similar readout circuit for wireless monitoring of glucose within the blood is illustrated in Figure

2.10b [45]. Multifunctional *in situ* sensing and stimulation of neurotransmitters dopamine and glutamate in the brain is presented in Figure 2.11 which also transmits the detected neurochemical concentration levels across a wireless link operating at a frequency close to 433 MHz [47]. There are other examples of multifunctional, multichannel, low-power and highly sensitive readout circuits for detection of electrical and chemical signals from the brain with outstanding performance reported in literature [3], [4], [48], [49], [50].

2.3.1 System architecture

Biosensors are designed to sense biological quantities and transform them into electrical quantities (Q_{in}) such as changes in resistance, capacitance, current and voltages which are easier to process by integrated electronics. The architectures employed in the design of sensor readout circuits are based on two main approaches. There is the conventional architecture where most of the signal processing is implemented in analog domain and converted to digital domain in later stages. This traditional approach is useful in the initial phase of development of prototypes to investigate how the system should work and study possible non-idealities [11]. However, the drawback of using this approach is that it provides less flexibility. Thus, the current trend in most sensor readout circuits is to digitalize the signal from the sensor as early as possible in order to minimize mismatch errors, provide more programmability and tuneability of analog blocks; and implement compensation techniques to further optimize the performance of the readout circuit [11], [51]. This

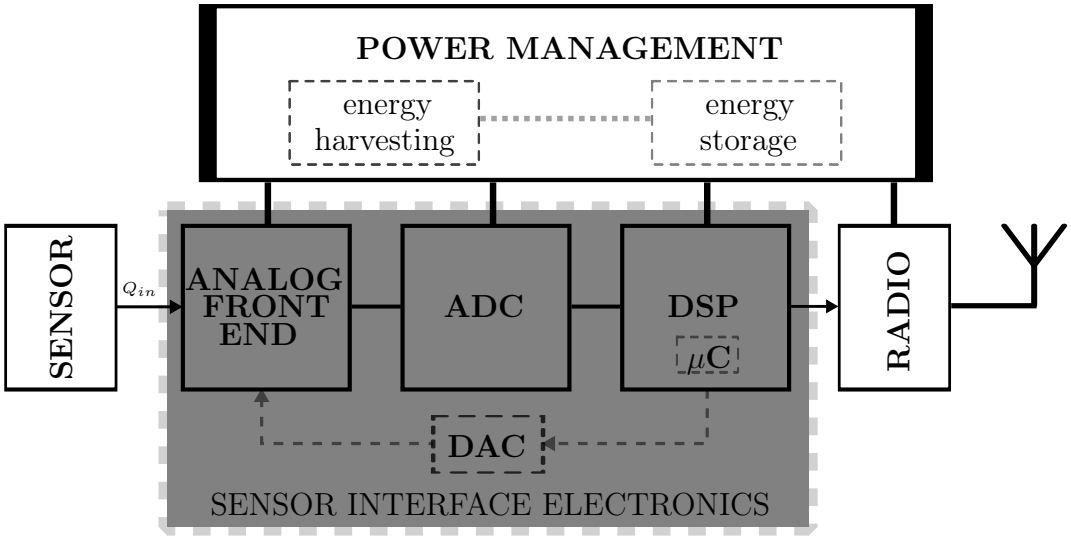


Figure 2.12: Typical system architecture in biomedical readout circuits.

approach is often known as mixed-signal architecture which is based on combination of analog and digital components in the operation of the readout circuit where digital techniques dominate most of the processing of the signal and may also control some aspects of the analog design in a feedback fashion through digital-to-analog converters (DAC) as illustrated in Figure 2.12.

The core processing block of most biomedical readout circuits is defined by the sensor interface electronics (SIE) unit. The SIE unit consists mainly of analog front-end (AFE), analog-to-digital converter (ADC) and digital signal processing (DSP) blocks as presented in Figure 2.12. In addition, for fully-functional implantable biomedical readout circuits, the SIE unit needs to be interfaced to power management (POW) and radio modules. The main function of the POW module is to supply power to the integrated circuits within the SIE core blocks and radio module. Hence, the incoming analog signal (Q_{in}) from the sensor is processed via the SIE unit and the output of the SIE unit is usually in digital form which is transmitted via the radio module to an external system for further processing and visual presentation of the received data. Further details about the main blocks of the readout circuit are described briefly below.

- **Analog front-end (AFE)**: This block interfaces directly with the sensor and consists of signal acquisition circuits. Hence, this block is responsible for acquiring the signal of interest, signal amplification and filtering. The noise generated from this block is usually dominated by flicker noise due to the nature of biosensor signals which have small signal amplitudes and at low-frequencies. Thus, noise optimization of the AFE block plays a critical role in the design and performance of biomedical readout circuits and has a significant impact on detected signal resolution.

- **Analog-to-digital converter (ADC)**: This block is responsible for converting the pre-processed signal from the analog front-end into a form that can be easily processed by the digital signal processing block. Typically, the ADC block receives a continuous signal, samples the received signal periodically in time and outputs a quantized digital representation of the analog input signal. Thus, the discretized output is prone to inaccuracies as a result of quantization error, jitter and aliasing which in turn limits the resolution of the reconstructed signal after conversion. Hence, the ADC block usually consists of sample and hold (S/H) circuits and anti-aliasing filters for minimizing inaccuracies in the digital output codes.

- **Digital signal processing (DSP)**: This block performs post-processing operations on the discretized output from the ADC such as additional filtering, encoding and extracting useful information required by other blocks that it interfaces to, such as the DAC and radio modules. In addition, this block may contain a micro-controller(μC) for implementing more complex and intelligent algorithms which enhance the operation and performance of the readout circuit. The DAC block may be included in the readout circuit for further optimization and programmability of the AFE. The DAC optimizes the AFE block based on the output of previous operations, which depends on the requirements of the biomedical application. The DAC block is especially useful in implementation of feedback systems, for example in closed-loop brain interfaces that also control stimulating electrodes in neurochemical monitoring as shown in Figure 2.11. The DSP block could also be used to implement

modulation of the data to be transmitted before forwarding it to the radio module.

– **Power management (POW)**: This block is especially important in the design of autonomous readout circuits that need to be self-sufficient which is the case in implantable devices. This module typically consists of two main blocks namely the energy harvesting and energy storage blocks which can operate independently or co-dependently as illustrated in Figure 2.12. Thus, biomedical readout circuits are generally implemented either with only the energy storage block or with only the energy harvesting block or with both blocks. The energy harvesting block consists of circuits that collect and transform energy from forms such as radio frequency (RF), light and thermal energy; into electrical energy that can be used to power the readout circuit. In addition, the energy storage block often includes batteries or super-capacitors for storing the harvested electrical energy or for directly powering the readout circuit. However, the main challenge of using only the energy storage block in implantable devices is that it requires periodical surgery for replacement when it eventually runs out of charge. Furthermore, miniaturization of the storage unit in order to increase its lifespan presents another challenge of using only the energy storage block in implantable devices. Likewise, using only the energy harvesting block has its own challenges such as when the power received from the energy source is not sufficient to power the device or if the RF link is broken. Hence, the current trend and recommended approach is to implement both blocks such that the harvested energy is used to recharge the energy storage components [11].

– **Radio**: This module is primarily responsible for transmission of the digital output data from the DSP block to an external system for further analysis and processing. The radio module may also be used to receive the RF signal that is used by the POW module to harvest energy for powering the readout circuit. Hence, the radio module is often implemented as a transceiver and typically consists of radio frequency integrated circuits (RFIC) such as low-noise amplifier (LNA), frequency mixers, local oscillator (LO), baseband filters and antennas. On the other hand, the use of RFID based radio modules in implantable and wearable devices is becoming increasingly popular and promising for reducing power due to the use of passive components in the implementation of the radio module [52]. In addition, the RFIC circuits used in implantable devices are designed to operate at low frequency bands usually within the Industrial, Scientific and Medical (ISM) or Medical Implant Communication Service (MICS) bands or any of the other frequency bands that are allocated to or reserved by different countries and geographical regions as shown in appendix A1. There are other regulations that implantable RFICs are required to fulfil such as limit on maximum allowable data rates and specific absorption rate (SAR) that defines the maximum RF power that is allowed through the body depending on the location of the readout circuit in the body [11]. These standards are in place to reduce signal attenuation

at skin-tissue interface and to minimize the overall impact of RF signals on human body.

Having described the internal blocks of biomedical readout circuits, it is evident that the design of wearable and implantable devices for real-time monitoring of biological quantities and processes requires careful consideration of the system architecture, comprehensive understanding of the system component functions and implementation of underlying circuitry. There are two key design methodologies that govern the selection of circuit topology and architectures that are utilized in the design and implementation of biomedical readout circuits.

One methodology is based on low-noise driven system design with emphasis on reducing the effect of noise from various noise sources on the performance of the whole readout circuit. In general, the sensor limits the overall system performance and the readout circuitry should be designed to cause no harm or degrade the small sensor signal which is the main challenge in the design of sensor interface electronics [51]. Some of the common noise sources known to affect biomedical readout circuits are discussed in section 2.3.2.

The other methodology is low-power driven system design with emphasis on optimizing each block to either operate at low voltages or to consume as low current as possible. An important aspect of designing low-power implantable devices is to adopt energy-efficient techniques especially in the ADC and DSP blocks that often consume a lot of power during signal processing.

2.3.2 Biosignal distortion and noise sources

Achieving good signal quality from biosensors with little or no distortion is the main challenge in the design of biomedical readout circuits. Biosignals such as blood pressure, heart potentials, eye, muscle and brain potentials, biochemical signals and other physiological quantities of interest have characteristics that further complicates their detection and measurement. These characteristics include small signal amplitudes, low frequency components, presence of competing signals within the same frequency range with higher signal amplitudes, interference from other reactions at biosensor interface and rate of occurrence of the biosignal of interest [6]. Hence, biosignals are prone to distortion from various sources and at different stages in the signal life-cycle from signal acquisition to signal readout as depicted in Figure 2.13.

The initial point of distortion of the biosignal is at the sensor interface to the environment where the signal is detected either by chemical, mechanical, optical or electrical methods. The detection is as a result of interaction between the captured biological assay from the sample collected from the region of the biological quantity of interest, and the electrodes or interface structures of the biosensor. However, in reality, the detected signal is not solely as a result of interactions from only the quantity of interest but may also include contributions from local reactions at the sensor interface due to bio-fouling that results in biochemical noise as earlier discussed in section 2.2.2. In addition, the detected signal may also include contributions from chemical or electrical interference as a result of reactions from other quantities that

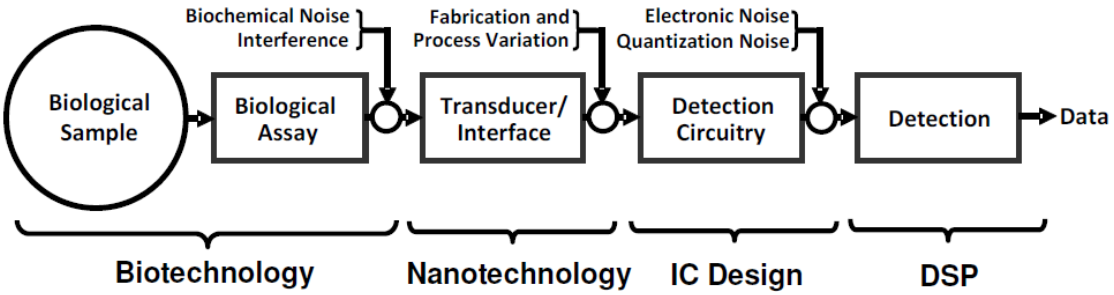


Figure 2.13: Common noise sources in biomedical readout circuits [53].

are not of interest or due to variations in contact impedance and contact potential of the sensor electrodes at the skin or tissue interface. Hence, biosensors are designed to have high selectivity to the specific quantity of interest and to reduce or counter the effect of mismatches in the contact impedance and contact potential at the electrode-skin interface for wearable devices or at electrode-tissue interface for implantable devices. Thus, biosignal attenuation, distortion and interference are reduced due to the use of noble metals or carbon as electrode materials. As a result, these materials are bio-compatible because of their inert nature (i.e. they do not undergo reactions). The use of inert materials increases the contact or interface impedance which can be reduced by increasing the electrode surface area as given in Equation 2.6. The electrode surface area can be increased by using nanostructures such CCS or electrode surface-roughening techniques also known as electrode de-polarisation [31].

Another source of noise and biosignal distortion is at the sensor interface to the detection circuitry where the signal is acquired in electrical form and processed. Distortion of the biosignal occurs due to fabrication and process variations in the electrical properties of the electrodes and characteristics of transistors which introduces mismatches and limits the performance of the readout circuit. Hence, the use of integrated circuits (IC) techniques for compensating non-idealities such as offset and gain errors that occur due to CMOS technology manufacturing process spread should be considered especially in the design of the analog components within the detection circuitry. In addition, dynamic techniques such as chopping, auto-zeroing and dynamic element matching (DEM) can be explored to reduce the effects of flicker noise (also known as $1/f$ noise) and component mismatch, due to the low frequency operation and small bandwidth of biosignals [51], [54].

Other electronic noise sources include thermal noise and shot noise which are related to collisions between charge carriers along conductive channels within metal-oxide-semiconductor (MOS) devices. These collisions result in fluctuations in the input signal also referred to as white noise. Hence, reduction of thermal noise or KT noise is important in sensor readout circuits because it sets the minimum limit of detection of the sensor signal; and more importantly when the readout circuit is based on mixed-signal architecture, to prevent aliasing of under-sampled white noise into the sensor bandwidth [54], [55]. Thus, thermal noise can be reduced by sigma-delta modulation techniques such that errors caused as a result of thermal

noise are modulated out of the sensor signal bandwidth [51], [54]. Another method for reducing thermal noise is the use of digital averaging techniques such as simple, moving, weighted-moving average filtering and successive sample averaging with decimation for anti-aliasing [54], [55], [56]. It is important to note that averaging techniques can only be used to minimize thermal noise but not to reduce flicker noise because the measurement samples of white or thermal noise are uncorrelated whereas that of flicker or $1/f$ noise are correlated between current and prior samples [55], [57]. In addition, there is a limit to which averaging techniques can improve the signal-to-noise ratio (SNR) and signal resolution at the expense of longer measurement time [56]. Hence, an optimum limit on measurement time and sampling frequency should be defined during which the benefits of using averaging techniques are maximized.

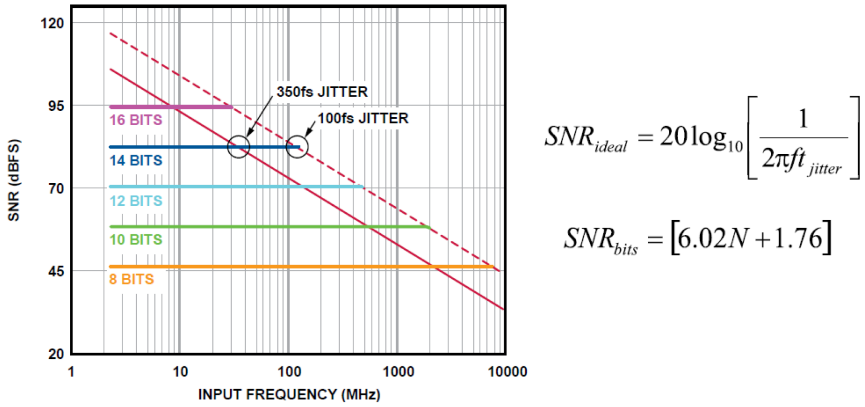


Figure 2.14: Effect of jitter and signal frequency on SNR and resolution of ADCs [58].

Finally, quantization noise and jitter (i.e. timing error as a result of phase noise from sampling of the analog signal) play crucial roles in the performance of biomedical readout circuits. Both noise sources are introduced within the ADC block, before sending the digitized biosignal to the DSP block of the readout circuit for further processing as depicted in Figure 2.13. Quantization noise is inevitable in any digital system because it is as a result of rounding up of the sampled data sequence to the nearest least significant bit (LSB) during conversion of the continuous signal to discretized form. However, the conversion error caused as a result of quantization can be minimized by avoiding unnecessarily high ADC resolution and optimizing the ADC to have very low jitter which in turn improves the signal-to-noise ratio [58]. In addition, lowering the jitter of the ADC, increases the resolution of the ADC for a given signal frequency as illustrated in Figure 2.14. On the other hand, increasing the signal frequency, lowers the resolution of the ADC for a constant jitter of an ADC [58]. Hence, reduction of phase noise and errors caused by jitter in the sampling clock and other sources such as jitter due to supply noise (i.e. variations in supply voltage) and substrate noise, is vital in the design of ADCs especially in biomedical applications given the low frequency range of biosignals [59]. Thus, an optimum resolution must be defined for the ADC that yields reasonable benefits with respect to the noise performance of biomedical readout circuits.

3 Proposed design of the Dopamine Oxidation Readout Sensor Interface

This chapter describes the design and implementation of the proposed readout sensor interface micro-system for detection of oxidation and reduction of dopamine. The proposed micro-system represents the sensor interface electronics (SIE) unit that can be integrated to an extensive and more elaborate readout system as presented in Figure 2.12 for dopamine monitoring. Hence, the scope of this thesis is based on the design of the SIE unit which is referred to as dopamine oxidation readout sensor interface (DORSI) throughout this document. DORSI is designed to interface with a biosensor which operates based on electrochemical transduction principle and three-electrode electrochemical cell structure as depicted in Figure 3.1. The structure of DORSI is based on three main blocks namely analog front-end (AFE), analog-to-digital converter (A/D) and digital system processing (DSP) as illustrated in Figure 3.1. The design of DORSI micro-system is based on mixed-signal front-end architecture where analog and digital techniques are employed in the processing of the measured redox current signals flowing between the working electrode (WE) and counter electrode (CE).

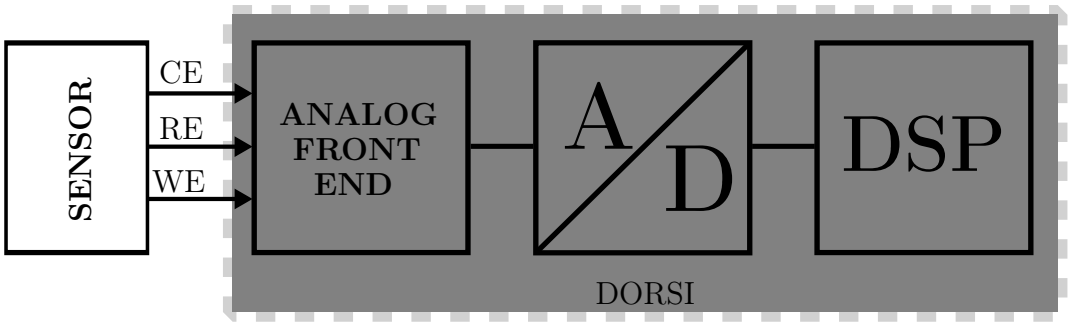


Figure 3.1: System block diagram.

As described earlier in section 2.3.2, the main challenge in the design of sensor interface electronics is the presence of various noise sources at different stages in the biosignal processing that contribute to the overall performance of the readout circuit. Likewise, the design of DORSI also faces similar challenges and limitations set by the biosensor which influenced the design requirements and techniques used to achieve the required specifications for obtaining a functional readout system with good signal quality. Hence, the use of mixed-signal architecture resulted in early digitalization of the acquired current signal and implementation of digital averaging filtering technique for reduction of noise and conversion error. In addition, single-ended and differential conversion approaches were implemented for comparing their effect on conversion gain, sensitivity and noise reduction. The next chapter 4 presents post-layout simulation results of the whole readout system based on measured data from novel carbon-based electrodes that is used for modelling the dopamine sensor electrical characteristics. Finally, the layout implementation of the main blocks of DORSI are presented in the appendix B of this document.

3.1 Design requirements

Understanding the application requirements and sensor limitations are integral aspects of the design of sensor interface circuits. The primary objective of the proposed design of DORSI is to detect dopamine oxidation and reduction current signals from the sensor electrodes. The secondary objective of DORSI is to convert the detected current signals to digital codes. These objectives ensure that the digital codes from the output of DORSI correspond to the concentration of the applied or released dopamine. Hence, the design requirements of DORSI are mainly influenced by the characteristics of dopamine as a neurotransmitter, the low-frequency application area and the sensor impedance model. The sensor impedance model used in the design and simulation of DORSI is based on the electrical (i.e V-I) characteristics extracted from the measured data of the sensor electrodes which are based on novel diamond-like carbon (DLC) materials [6]. The detection method used in the measurement setup is cyclic voltammetry (CV) at a scan rate of 400 mV/s and in the presence of nitrogen purged phosphate buffered saline (PBS) for measuring the background current.

Other requirements that guide the design and optimization of DORSI are defined based on the measurement setup as described in Figure 3.2. The measurement setup is used for evaluating the electrochemical performance of the sensor electrodes in terms of selectivity, response time and sensitivity by extracting the redox current profiles with respect to time and the applied cell voltage. Thus, the measurement setup illustrates key design parameters for the implementation of the integrated electronics or potentiostat circuitry that interfaces with the sensor electrodes. Hence, important design parameters that can be extracted from the sensor measurement setup include cell voltage (V_{cell}) range, CV scan rate which defines the V_{cell} sweep rate, expected redox or faradaic current (I_{cell}) range and an estimate of the expected background current (I_{bg}) range. Thus, these application specific requirements serve as basis for more technical requirements that are defined for each main block in the design of DORSI.

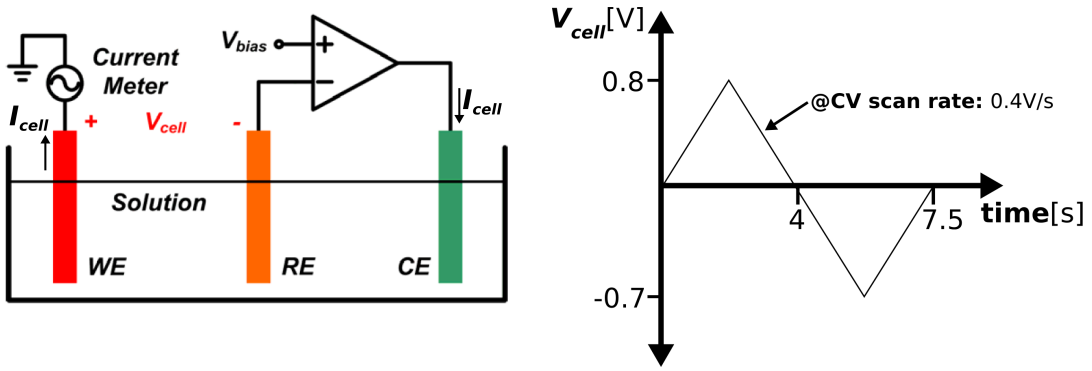


Figure 3.2: Measurement setup of dopamine redox current detection.

The detected dopamine current signal depends on the sensitivity of the sensor electrodes. Hence, the design requirements were tailored based on the minimum

detection limit of the sensor which is 10 μMol for the DLC-based electrodes. The measured oxidation and reduction current data from the sensor electrodes shows that DORSI must be capable of detecting at least 1 nA change in current and the oxidation and reduction potential range of dopamine shows that DORSI must be capable of providing a stable cell voltage (V_{cell}) from -0.7 V to 0.8 V. Furthermore, DORSI should be able to support a wide current range to be able to detect higher dopamine concentrations upto 1 mMol based on DLC electrodes and from other commercial electrodes. In addition, DORSI should be implemented to have low-noise characteristics given the magnitude of the measured background current (approx. tens of nA) which also increases as dopamine concentration increases. Finally, the design of the main components of DORSI should also be optimized for micro-power operation in order to ensure that the overall readout system is energy-efficient while obtaining good signal quality.

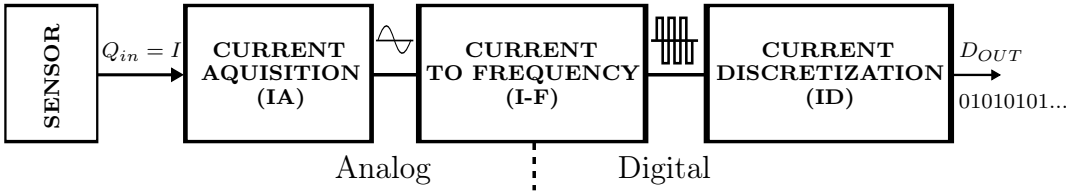


Figure 3.3: Main blocks of signal processing in DORSI.

Based on the description of the measurement setup and aforementioned requirements set by the sensor electrodes, the design of DORSI is divided into three main blocks as described in Figure 3.3. The electrical quantity of interest (Q_{in}) that is available from the sensor is the induced current (I) that is flowing between the working (WE) and counter (CE) electrodes during the CV sweep of the bias voltage (V_{bias}). The acquired current signal is processed along the main blocks of DORSI as depicted in Figure 3.3 and further described in section 3.2. Specific requirements defined for the operation of each main block of DORSI are described briefly below.

- **Current acquisition (IA)** : this block is required to control the cell voltage (V_{cell}) for acquiring the induced redox or cell current (I_{cell}) while sweeping the input bias voltage (V_{bias}). Thus, this block is required to provide stable V_{cell} between -0.7 V to 0.8 V based on the CV forward and reverse sweep of the bias voltage (V_{bias}). In addition, the signal bandwidth is defined based on the transmission time of action potentials (AP) across chemical synapses due to the release and uptake process of neurotransmitters such as dopamine. Typical signal bandwidth for action potentials is around 100 Hz$-$10 kHz, since the chemical neurotransmission process as described in section 2.1 lasts only a few milliseconds [16], [18]. Thus, the IA block is optimized based on the signal bandwidth and the response time of the sensor electrodes which is within few milliseconds ($<$ 10 ms) based on the measured data from the electrodes.

- **Current-to-Frequency (I-F)** : this block is required to convert the acquired current (I_{cell}) from the IA block to frequency. The output of this

block (*osc_out*) is a continuous digital signal whose frequency increases and decreases proportionally to the increase and decrease of the acquired current as illustrated in Figure 3.4. Thus, this block performs the initial sampling of the current signal and provides series of pulses to be quantized by the ID block. In addition, this block must be able to detect a minimum change in current (ΔI_{min}) of 1 nA as defined by the resolution of the sensor electrodes. Hence, this block must be able to convert the minimum change in current (ΔI_{min}) within 1ms or less, given the signal bandwidth and sensor sensitivity. Thus, the I-F block is optimized to have current-to-frequency sensitivity of at least 1 kHz/nA or more.

– **Current discretization (ID)** : this block is required to quantize the continuous sampled signal from the I-F block as discrete values or digital codes. The digital codes at the output of this block are generated by applying integration and decimation methods on the sequence of pulses from the I-F block as the frequency of the pulses changes with respect to the acquired I_{cell}. In addition, this block performs digital signal processing (DSP) functions such as noise averaging and encoding of the digital codes (D_{OUT}). Noise averaging is achieved over a long measurement time (T_{meas}) of the pulses from the I-F block as the sampling time interval (T_s) increases during decimation. Hence, the decimation rate of this block is defined by the sampling frequency (F_s) of this block and the operating frequency F_{osc} of the I-F block as illustrated in Figure 3.4. As a result, the decimation rate defines the current-to-digital code conversion gain of this block based on the number of pulses (N_p) within each sampling interval T_s, where N_p changes as F_{osc} varies. Therefore, the I-F block should be designed to provide a flexible way of tuning its operating frequency F_{osc}. The sampling rate F_s of this block is determined by the desired number of samples (N_s). This implies that the sampling rate of the ADC is not fixed but can be varied based on T_{meas} and N_s. Thus, F_{osc} and F_s are optimized for the ID block to achieve a digital code resolution (n) of 10-bits or more.

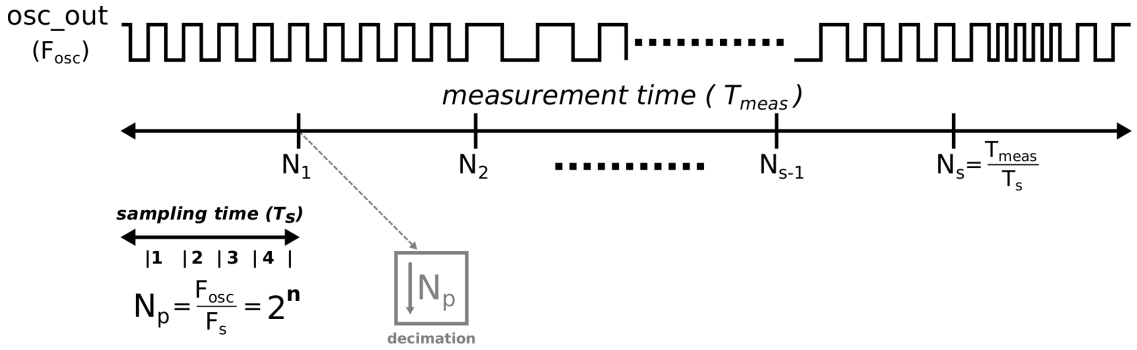


Figure 3.4: Description of the sampling (N_s) and decimation (N_p) rates used in the ID block.

As an example for a current signal bandwidth of 1 kHz, 750 samples is generated from the ID block if a sampling frequency F_s of 10 kHz is applied to the measurement

setup presented in Figure 3.2 with a scan rate (or T_{meas}) of 75 ms. This implies that, if the average operating frequency of the I-F block F_{osc} is set to 10 MHz, then the average decimation rate (i.e. N_p) of the ID block is set to every 1000^{th} count of pulses. In addition, the sampling rate of 10 kHz in this example is defined to be 5 times the Nyquist frequency of 2 kHz but can also be increased. Hence, oversampling can be implemented in the ID block by increasing F_s as discussed further in section 3.2.3. However, oversampling reduces T_s and the decimation rate N_p which is undesirable in averaging band-limited noise but effective in reducing quantization noise as discussed in the next section 3.2.

In summary, the IA block represents the instrumentation component of the readout circuit and plays a crucial role in obtaining good signal quality from the sensor and in the performance of the subsequent blocks (i.e. I-F and ID blocks). It is important to mention that achieving good signal quality should not be traded for low power dissipation. Hence, higher priority is placed on reducing the effect of noise and minimizing conversion errors in the design of DORSI rather than low power consumption. Noise optimization in the IA and I-F blocks is important in improving the signal-to-noise ratio (SNR) and setting the resolution of the readout circuit. Finally, the utmost goal of DORSI is to be able to identify oxidation and reduction current peaks and to provide the corresponding potentials at which they occur. Table 3.1 summarizes the main design requirements of DORSI in order to achieve this goal. It should be noted that the sampling rate of the ID block is not fixed but depends mainly on the signal bandwidth and if oversampling is required.

Table 3.1: Design requirements summary of DORSI

Main blocks	**Parameters**	**Values**
Current acquisition (IA)	V_{cell} range	-0.7 V to 0.8 V [vi]
	I_{cell} range	1.2 μA [vii]
Current-to-frequency (I-F)	current resolution	1 nA
	current sensitivity	$>$ 1 kHz/nA
Current discretization (ID)	signal bandwidth	100 Hz to 10 kHz [viii]
	digital output resolution	10-bit [ix]

[vi] defines required input and output voltage range of 1.5 V [vii] defines required current range of $\pm$600 nA [viii] defines sampling rate which is variable [ix] defines required SNR of at least 60 dB

3.2 System level design

The system architecture and design of DORSI is based on the design requirements described in the previous section 3.1. The sensor signal processing is divided into three main stages namely current acquisition (IA), current-to-frequency (I-F) and current discretization (ID) as presented in Figure 3.5. The IA stage is based on a transimpedance topology for controlling the cell voltage between the reference electrode (RE) and working electrode (WE). In addition as the name implies, the

IA stage is responsible for acquiring the redox current flowing between the working electrode (WE) and counter electrode (CE). The basic structure and operation of the electrochemical cell as well as the process of sensing dopamine from the sensor interface are discussed in section 2.2.

Typically, electrochemical impedance spectroscopy (EIS) is used to extract the electrical characteristics (i.e. charge-transfer resistance R_{CT} and double-layer capacitance C_{DL}) at each electrode-solution interface in order to reveal a more precise sensor interface impedance model [46], [60]. However, since the EIS model of the test electrodes was not available during the design of DORSI, simulations were carried out based on the lumped impedance model as highlighted in Figure 3.8. Hence, the simulation setup of DORSI is based on the measured data of the cell voltage and redox current (V-I) from the sensor electrodes which reveals the non-linear nature of the overall impedance of the sensor.

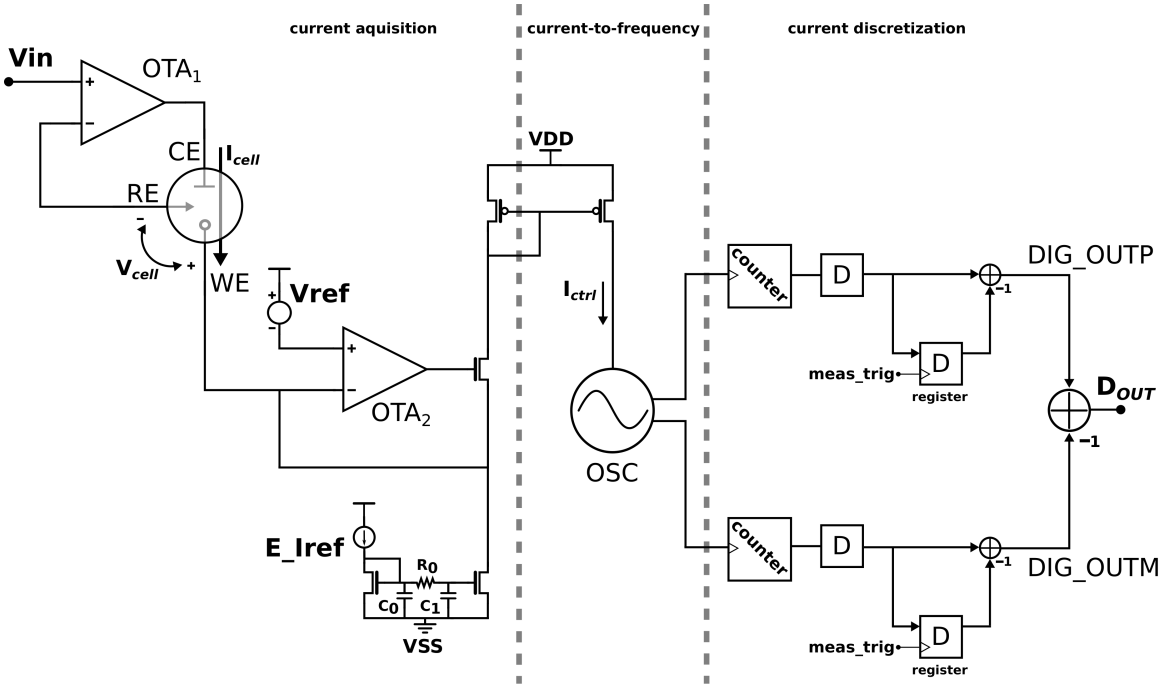


Figure 3.5: Top-level schematic of DORSI.

The I-F stage is responsible for the initial A/D conversion of the acquired current signal and operates based on an oscillator which samples the current signal in frequency domain. Thus, the frequency of the output of the oscillator (OSC) changes as the redox current varies. In addition, the I-F stage provides differential outputs for reducing interference due to supply voltage variations. Hence, current-to-frequency (I-F) sensitivity is increased by reducing the effect of supply interferences. As a result, the differential operation of DORSI increases the dynamic range and gain of the current-to-frequency conversion.

The ID stage consists of counters and registers for implementing the quantizer function of the ADC. The quantization process is based on performing integration and decimation on the sampled differential digital outputs from the I-F stage. In

addition, the ID stage is responsible for DSP functions such as noise filtering with averaging technique and encoding of the discretized data. Hence, increasing the number of samples that is used during noise averaging by increasing the measurement time of the pulses from the oscillator, reduces conversion error and improves the resolution of the readout circuit in terms of effective number of bits (ENOB). Thus, the gain of the ID stage is solely defined by the measurement time and it should be noted that the use of averaging technique in the ID stage does not compensate for conversion errors due to non-linearity from prior stages [61]. The measurement time of the pulses from the oscillator for each decimation event defines the sampling time interval (T_s), which is defined by the $meas\_trig$ clock as depicted in Figure 3.5.

Oversampling can be applied to the A/D conversion by increasing the sampling rate F_s. However, it is more efficient in averaging uncorrelated wide band noise [61]. As a result, oversampling is not very effective in the noise averaging process of the ID stage and in improving the ENOB of the system since the noise bandwidth is limited by the RC low-pass filter that is applied in the I-F stage as described in Figure 3.6. On the other hand, oversampling is effective in averaging out-of-band noise that may remain after the RC-lowpass filter has been applied. Hence, oversampling reduces the quantization noise that is generated in the ID block. In addition, the use of CIC-filters together with decimation (i.e. reduction in sampling rate) prevents aliasing of out-of-band noise into the signal bandwidth after sampling by the oscillator [13], [56], [62].

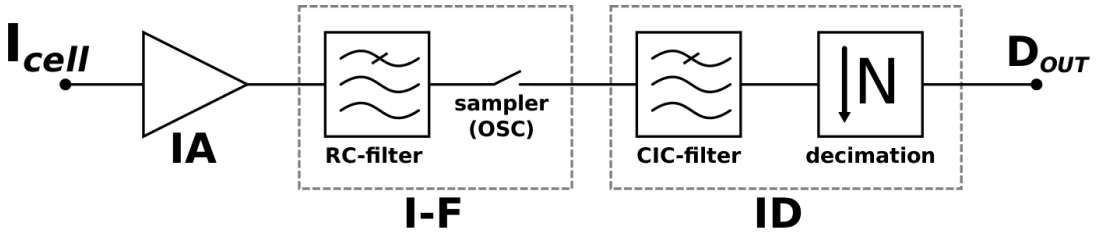


Figure 3.6: Cell current signal life-cycle within DORSI.

Furthermore, the operation of DORSI in single-ended mode can also be simulated by processing only one of the differential outputs from the I-F and ID stages. Thus, providing a possibility to compare the performance of DORSI in differential mode to its performance in single-ended mode. The next sections provide further description about the operation of each signal processing stage and the design of the main components that they consist of such as the operational amplifier in the IA block, the oscillator in the I-F block and the counter in the ID block.

3.2.1 Current acquisition

The current acquisition block is the analog front-end of the readout circuit. This section focuses on the design of the operational transconductance amplifier (OTA) and providing the control current (I_{ctrl}) to the I-F block as depicted in Figure 3.5. Several architectures were explored and the transimpedance structure described in

Figure 3.5 was found to be the most suitable structure to meet the design requirements of DORSI. The main reason for choosing the transimpedance architecture is that it supports detection of bi-directional currents based on the oxidation and reduction reactions occurring at the working electrode (WE). In addition, the topology provides a flexible way of extending the redox current range by adjusting the reference current (E_I_{ref}) that is used for subtraction or addition of the I_{cell} from the sensor electrodes.

The primary function of both amplifiers is to provide a stable voltage over the electrochemical cell which is modelled as described in Figure 3.7. The cell voltage is defined by ensuring that the voltage at the working electrode (V_{WE}) remains at a virtual ground defined by the bias voltage of OTA2 (V_{ref}) while the voltage at the reference electrode (V_{RE}) follows the input bias voltage of OTA1 (V_{in}) . Hence, the cell voltage can be expressed as in the following equation.

$$V_{cell} = V_{WE} - V_{RE} = V_{ref} - V_{in} \tag{3.1}$$

Furthermore, as stated earlier in section 2.2.1, the reference electrode is designed to be inert to the reactions occurring within the cell. Hence, there is no current flowing through the RE and no voltage drop over the RE, therefore its impedance contribution (Z_{RE}) to the overall impedance of the cell is negligible.

Likewise, the impedance of the counter electrode (Z_{CE}) is also regarded as negligible since the voltage over the counter electrode (V_{CE}) is extremely small. The principle of the voltage follower structure ensures that the negative input of OTA follows the positive input of the OTA closely. As a result, having small V_{CE} prevents the output voltage of OTA1 from saturating which allows sufficient voltage headroom or margin to be maintained between the counter electrode voltage and the output of OTA1 within the desired input range. Thus, wider cell voltage range than the required 1.5 V can be achieved and lower supply voltage than 2.5 V can be used. In addition, the contribution of the solution resistances from the CE and WE interfaces (i.e. R_{sc} and R_{sw}) to Z_{CE} and Z_{WE} respectively are also known to be negligible [26], [30], [60]. Lastly, the impedance of the working electrode (Z_{WE}) dominates the total impedance of the cell (Z_{cell}) since the redox reactions occur at the WE. The equivalent circuit and lumped impedance model of the electrochemical cell that is used in the rest of the design and simulation of DORSI are presented in Figure 3.7.

It is important to mention that minimizing the gain error of the OTAs is essential in achieving a stable cell voltage (V_{cell}). Hence, the gain of the OTA must be high enough to minimize the effect of gain error on the acquired cell current and for the voltage-follower configuration to provide accurate and stable output voltage with respect to the input voltage of the OTA. In addition, high and stable gain of the voltage-follower loop in all operating conditions, ensures that the measured redox current and recorded oxidation or reduction potentials accurately correspond to the actual potentials at which the redox reactions occur within the cell. Figure 3.8 illustrates the relationship between the input bias voltage of OTA1 and OTA2 and how they set the cell voltage during the cyclic voltammetry (CV) sweep.

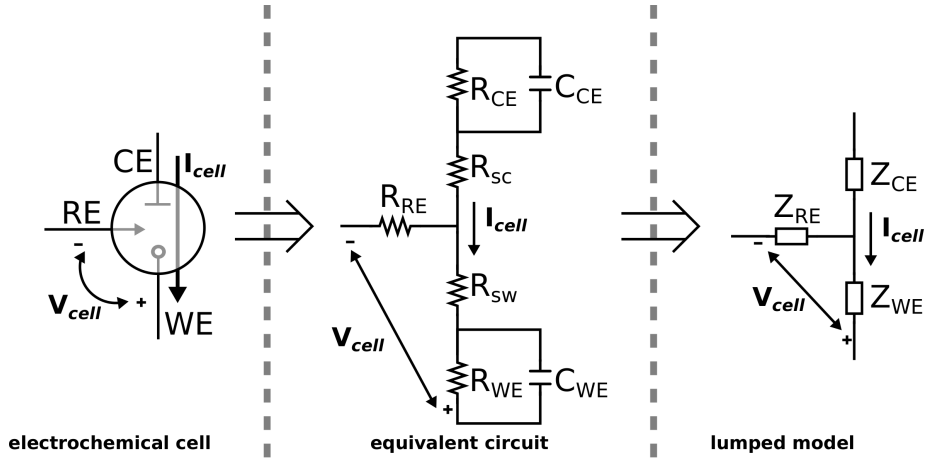


Figure 3.7: Lumped impedance model of electrochemical cell.

Furthermore, Figure 3.8 describes the relationship between the observed redox peaks and the cell voltage at which they occur. Finally, as discussed in section 2.2, the actual measured cell current contains contribution from biochemical noise at the electrode interface that produces background current (I_{bg}) which needs to be subtracted for the redox peaks to be revealed and the precise value of the redox current (i.e. I_{ox} and I_{red}) to be extracted.

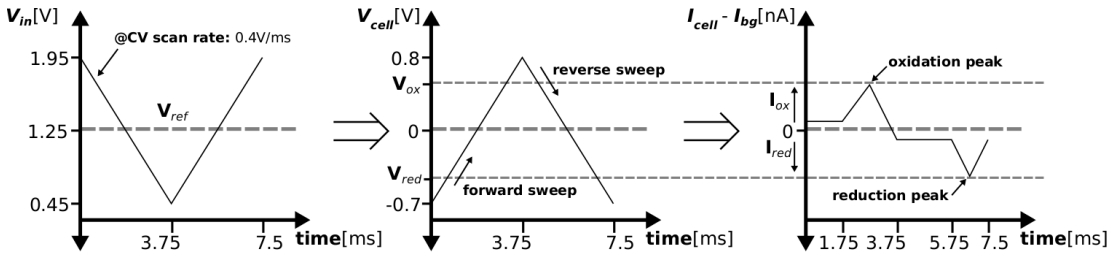


Figure 3.8: V_{in}, V_{ref}, V_{cell}, I_{cell} and I_{bg} relationships.

Following the stabilization of the cell voltage and extraction of the redox currents, the reference current (E_I_{ref}) is used to provide the control current I_{ctrl} to the I-F stage. This implies that the measured redox current is added to or subtracted from the reference current E_I_{ref} as described in the following equation.

$$I_{ctrl} = E\_I_{ref} \mp I_{cell} \tag{3.2}$$

As a result, I_{ctrl} is always a positive value that decreases or increases from the defined bias or reference current E_I_{ref}. In addition, the reference current provides a means of supporting wider range of redox currents based on the sensitivity of the electrodes. The reference current can also be reduced if the detected current range is low, in order to reduce the contribution of E_I_{ref} to the total current and power consumption. The current mirror for the reference current E_I_{ref} also includes a simple RC low-pass filter for reducing the noise from the bias source. The same RC-filter implementation is used at bias current sources in the design of the operational

transconductance amplifier and the oscillator. Thus, the low-pass nature of the filter implies that the filter attenuates high-frequency signals that are outside the bandwidth of interest. The cut-off frequency f_c of the filter is defined by the values of the resistor (R_0) and capacitors (C_0 and C_1) as shown in Equations (3.3).

$$\tau = R_0 * (C_0 + C_1) \tag{3.3.a}$$

$$\omega_c = \frac{1}{R * (C_0 + C_1)} \tag{3.3.b}$$

$$f_c = \frac{1}{2 * \pi * R * (C_0 + C_1)} \tag{3.3.c}$$

It is important to note that the cut-off frequency defines the frequency at which the filter attenuates the signal to half of its full power. Hence, the component values of R_0, C_0 and C_1 should be chosen carefully so that the signal of interest is unaffected. In addition, the values of the RC components also define the time-constant of the signal (τ) which in turn affects the settling time response of the signal. These considerations related to the values of the RC components can be of less importance if the signal path is separated from the bias, which is the case in the configuration of the E_I_{ref} and OTA I_{bias} current mirrors.

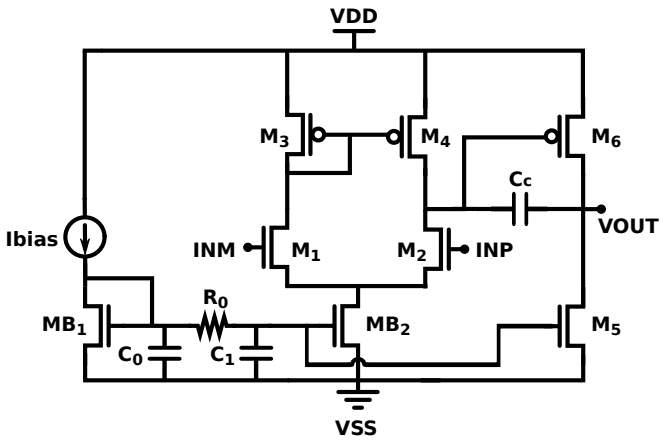
The selection of the OTA architecture is based on the design requirements that were earlier introduced in section 3.1. The main requirement for the OTA is support of wide input and output voltage range of 1.5 V with an input common mode range (ICMR) within -0.7 V to 0.8 V. As a result, a high supply voltage of at least 1.8 V or more is required to be able to support the required ICMR. This relatively high supply voltage limits the design methods that could be used to achieve extremely low power consumption. Thus, optimization of the OTA is geared towards low current consumption in order to achieve low power consumption.

Other requirements include high and stable gain within the required ICMR, low noise characteristics, high common-mode rejection ratio (CMRR) and power supply rejection ratio (PSRR), and good loop stability. Most of these requirements are defined in order to minimize variations and offset in the cell voltage V_{cell}. Another important design requirement is that the OTA should provide low output impedance in order to be capable of driving the high load impedance from the sensor electrodes [57]. Finally, although the slew-rate (SR) and settling time design parameters are not of high importance in the design of the OTA due to the low signal bandwidth, they should still be considered as they affect the settling time of the oscillator in the I-F stage.

Several OTA architectures were investigated and simulated before finally selecting the Miller OTA architecture presented in Figure 3.9. One of the architectures that was explored is the composite-cascode architecture reported in [63], to be well suited for biomedical instrumentation for achieving high gain, low noise and low power operational amplifiers (OPAMP). Although, this OPAMP with composite-cascode stages appears to be a good candidate, simulations revealed that this OPAMP structure is susceptible to process variations due to its subthreshold operation and dependence on threshold voltage. Hence, stability of the composite-cascode amplifier is an issue in this architecture which is a crucial design requirement of the

OTA used in DORSI. Another OTA architecture that was investigated is the folded-cascode architecture for its stability over process corners, good gain and supply noise rejection characteristics [57], [64]. However, the folded-cascode OTA topology is not suitable because it can not provide large enough output voltage swing with available supply voltages.

Lastly, the conventional Miller OTA architecture is investigated and simulations showed that while using the PMOS topology lowers the flicker noise, it consumes much more current than its NMOS counterpart, to be able to attain high and stable gain across the required ICMR and output range. On the other hand, the NMOS based Miller OTA is sensitive to changes in threshold voltage but it is still more stable to process variations when compared to the composite-cascode architecture since the output stage is operating in strong inversion region. In addition, the Miller topology has limited open-loop bandwidth (i.e. f_{-3dB}) but fortunately that is not an issue for biomedical applications where the signal bandwidth (BW) are small and at low frequencies. Thus, the conventional Miller NMOS-based OTA (N-OTA) is selected as the most suitable OTA of the architectures investigated to be used in the design of DORSI.



Component	Dimensions
M1 , **M2** (NMOS)	W= 1µm, L=1µm
M3 , **M4** (PMOS)	W= 2µm, L=1µm
M5 (NMOS)	W= 24µm, L=1µm
M6 (PMOS)	W= 48µm, L=1µm
MB1 (NMOS)	W= 8µm, L=1µm
MB2 (NMOS)	W= 0.4µm, L=1µm
Cc (0.8pF)	W= 12.5µm, L=12.5µm
C0 (1pF)	W= 14µm, L=14µm
C1 (1pF)	W= 14µm, L=14µm
R0 (100KΩ)	W= 1µm, L=16.14µm

Figure 3.9: Conventional Miller N-OTA schematic and dimensions used in DORSI.

The traditional Miller N-OTA presented in Figure 3.9 is designed and optimized for micropower operation while fulfilling the defined requirements. The OTA is a two-stage Miller OPAMP where the input stage is designed to operate in subthreshold to achieve the required ICMR while consuming low current. This provides a possibility for the OTA to operate at lower supply voltage when compared to previously investigated architectures. The N-OTA is designed to operate on single supply voltage of 2.5 V but has been simulated to also operate successfully on supply voltage of 1.8 V while meeting the pre-defined requirements. Hence, the contribution of the power consumed by the OTA to the overall power consumption of DORSI can be reduced.

In addition, the study of transistors operating in subthreshold region reveals an interesting relationship between the MOS device transconductance (g_m) and output resistance (r_o) which is similar to that of a bipolar transistor [64]. By operating in

weak or moderate inversion region, the design of the OTA takes advantage of the subthreshold conduction which as simplified in Equations (3.4), shows the linear relationship between the g_m and the drain current I_D of the MOS device as opposed to the square relationship in strong inversion region [64]. On the other hand, the strong dependence of the transconductance-to-drain current ratio (g_m/I_D) on threshold voltage (V_{th}) makes the performance of the OTA susceptible to process variations. Thus, the design of the OTA is verified to have stable operation across various process corners with monte-carlo simulations.

$$i_D = \frac{W}{L} I_{DO} * exp\left(\frac{q * v_{GS}}{n * kT}\right) \tag{3.4.a}$$

$$g_m = \frac{I_D}{n * V_T},\ V_T = \frac{\kappa * T}{q} \tag{3.4.b}$$

$$\frac{g_m}{I_D} \propto \frac{q}{\kappa * T} \propto \frac{1}{V_{th}} \tag{3.4.c}$$

$$r_o \cong \frac{1}{\lambda * I_D} \tag{3.4.d}$$

where v_{GS} is the gate-source voltage of the MOS device, V_T represents the thermal voltage of the MOS device, n represents the subthreshold slope factor, κ represents Boltzmann's constant, T represents temperature, q is the charge of an electron, λ represents the channel length modulation parameter of the MOS device and I_{DO} is a process dependent parameter [64].

Furthermore, the transconductance g_m and output resistance r_o of transistors operating in subthreshold are independent of device geometry (i.e. W/L aspect ratio) given a constant bias current. Thus, the gain of the OTA is mainly defined by the g_m and r_o of the input and output stages of the amplifier. Hence, the following equations hold for the DC-gain of the N-OTA presented in Figure 3.9 [64].

$$A_{dc} = G_I * G_{II} = \left\{\frac{g_{m2}}{g_{ds2} + g_{ds4}}\right\} * \left\{\frac{g_{m6}}{g_{ds6} + g_{ds5}}\right\} \tag{3.5.a}$$

$$= (g_{m2} * r_{oI}) * (g_{m6} * r_{oII}) \tag{3.5.b}$$

$$= g_{m2} * g_{m6} * \left\{\frac{r_{o2} * r_{o4}}{r_{o2} + r_{o4}}\right\} * \left\{\frac{r_{o6} * r_{o5}}{r_{o6} + r_{o5}}\right\} \tag{3.5.c}$$

$$A_{dc} = \frac{I_{D2} * I_{D6} * q^2}{n_2 * n_6 * (\kappa * T)^2 * (\lambda_2 + \lambda_4) I_{D2} * (\lambda_6 + \lambda_5) I_{D6}} \tag{3.5.d}$$

$$= \frac{1}{n_2 * n_6 * (V_T)^2 * (\lambda_2 + \lambda_4) * (\lambda_6 + \lambda_5)} \tag{3.5.e}$$

As a result of the relationships described in Equations (3.5), the overall DC-gain of the OTA is independent of I_D and the main parameter that offers control of the gain of the amplifier is λ which is inversely proportional to the channel length of the MOS device. Hence, the length of the transistors are designed to be longer

than the minimum length, in order to obtain large output resistance which in turn increases the gain of the amplifier. Unlike the DC-gain, the gain bandwidth (GBW) and slew rate (SR) of the amplifier are dependent on the drain current I_{D2} as shown in Equations (3.6) [64].

$$GBW = \frac{g_{m1}}{C_c} = \frac{g_{m2}}{C_c} = \frac{I_{D2} * q}{(n_2 * \kappa * T) * C_c} \tag{3.6.a}$$

$$SR = \frac{I_{DB2}}{C_c} = \frac{2 * I_{D2}}{C_c} \cong 2 * GBW * n_2 * V_{th} \tag{3.6.b}$$

In addition, Equations (3.6) also show the linear relationship between the SR and the GBW of the OTA which in turn depends on the threshold voltage and drain current of the input transistors (i.e M_1, M_2). Hence, the gain bandwidth of the OTA is limited since the input stage is operating at very low DC currents. Likewise, the slew rate of the OTA is inherently low due to the subthreshold operation of the input stage and low bias currents. Hence, the settling time obtained from the OTA is expected to be long but has been optimized to few tens of μs, so as to avoid significant effect on the settling time of the oscillator. In addition, the GBW is optimized to cover the signal bandwidth and with some overhead. The loop stability of the OTA is also enforced by ensuring high phase margin (PM) which in turn reduces ringing in the settling of the output voltage. The relationship between g_{m6} and g_{m1} plays a major role in attaining high phase margin as the ratio of g_{m6} to the output load capacitance (C_L) defines the output pole while the GBW is defined by the ratio of g_{m1} to the compensation capacitor (C_c) as explained in Equations (3.7) [64].

$$GBW = \frac{g_{m1}}{C_c},\ z_1 = \frac{g_{m6}}{C_c} \tag{3.7.a}$$

$$\therefore \frac{z_1}{GBW} \Rightarrow \frac{g_{m6}}{g_{m1}} \propto PM \tag{3.7.b}$$

$$p_2 = \frac{-g_{m6}}{C_L} \tag{3.7.c}$$

$$\therefore \frac{p_2}{GBW} \Rightarrow \left\{ \frac{g_{m6}}{g_{m1}} * \frac{C_c}{C_L} \right\} \propto PM \tag{3.7.d}$$

According to [64], the ratio of g_{m6} to g_{m1} should be greater than 10 in order to achieve a phase margin of 60^o. Likewise, the ratio of the output pole (p_2) to the GBW should be greater than 2.2 in order to achieve similar phase margin of 60^o [64]. Thus, the OTA is optimized to achieve high PM by placing the right-half-plane (RHP) zero (z_1) at a frequency more than 10 times higher than the GBW which is determined by the g_{m6}/g_{m1} ratio. In addition, the output pole (p_2) is also placed at a frequency more than 2.2 times higher than the GBW as a result of the g_{m6}/g_{m1} ratio and the C_c/C_L ratio. Thus, the value of the compensation capacitor C_c is also optimized with respect to the expected load capacitance C_L of $\sim$ 5 pF which also

contributes to the loop stability performance of the OTA. It should be noted that the loop stability of the OTA is still maintained even with a 10 pF load capacitor C_L due to the high g_{m6}/g_{m1} ratio. Hence, no further compensation techniques are required such as use of nulling resistor for controlling the RHP zero (z_1) in order to obtain good loop stability.

Another observation from Equations (3.7) is that there is a tradeoff between the gain bandwidth (GBW) and the phase margin (PM). This implies that by lowering the GBW, the ratio between the output pole, RHP zero and the GBW increases which increases the PM. Hence, the initial limitation on the GBW as a result of the input stage operating in subthreshold turns out to improve the stability of the OTA.

Finally, the currents flowing through the input and output stages were defined so that there is very small DC currents flowing in the input stage in order to keep it in subthreshold. Then the current flowing through the output stage is defined to be much larger than the bias current of the input stage in order to be able to drive the large capacitive load from the sensor electrodes. Hence, the bias current I_{bias} is divided based on the aspect ratios of the current mirror transistors (i.e M_{B1}, M_{B2}, M_5). The current mirror W/L ratios are optimized to provide current ratios of $1 : 1/20 : 3$ with respect to the bias current. Thus, at a bias current of 1 μA, the OTA is optimized to operate at 50 nA and 3 μA for the input and output stages respectively. In addition, static leakage currents are minimized due to the operation of the input stage in subthreshold and low threshold voltages. Thus, the design of the Miller N-OTA used in DORSI is optimized for low power dissipation which reduces the overall power dissipation of the IA stage. The total power consumption of the IA stage is expected to be around twice the power consumption of a single N-OTA due to the transimpedance architecture which requires two OTAs.

3.2.2 Current-to-frequency conversion

The operation of DORSI continues from the current acquisition (IA) stage to the current-to-frequency(I-F) stage with the transition between the IA and I-F blocks occurring in current-mode as the control current provided by the IA stage is fed directly into the I-F block. Thus, the control current (I_{ctrl}) together with the bias current of the oscillator (O_I_{ref}) defines the operation of the I-F stage. Hence, the operating frequency of this block can be easily tuned by adjusting the bias current of the oscillator (i.e. O_I_{ref}).

In addition, this block crosses both analog and digital domains as depicted in Figure 3.3, since it performs the initial A/D conversion of the varying current signal to frequency. Thereby providing as an output a digital representation of the continuous-time analog signal which serves as an input to the current discretization (ID) stage. As a result, this block performs the initial sampling of the analog signal in frequency domain and the ID block implements further processing of the sampled signal such as quantization and decimation (i.e. reduction in sampling rate). Hence, this block together with the ID block makes-up an oscillator-based ADC of the readout circuit.

The design of the oscillator is based on the conventional ring oscillator architec-

ture with current starved inverter stages which are controlled by I_{ctrl} and O_I_{ref} currents. Thus, the oscillator can be described as a current controlled oscillator (CCO) which is optimized to meet the design requirements earlier described in section 3.1. The initial design phase of the CCO focused on the single-ended (SE) architecture of the oscillator as presented in Figure 3.10. The single-ended CCO (SE-CCO) was first implemented in order to facilitate modularity of the system, re-usability of the SE block and understanding of the system functionality, non-idealities and limitations. Thus, the main priority was to have a functional system before making modifications for more optimization. Hence, the SE-CCO was optimized to provide the required performance, then the bias circuitry was later modified to implement the differential oscillator with the same SE-CCO blocks.

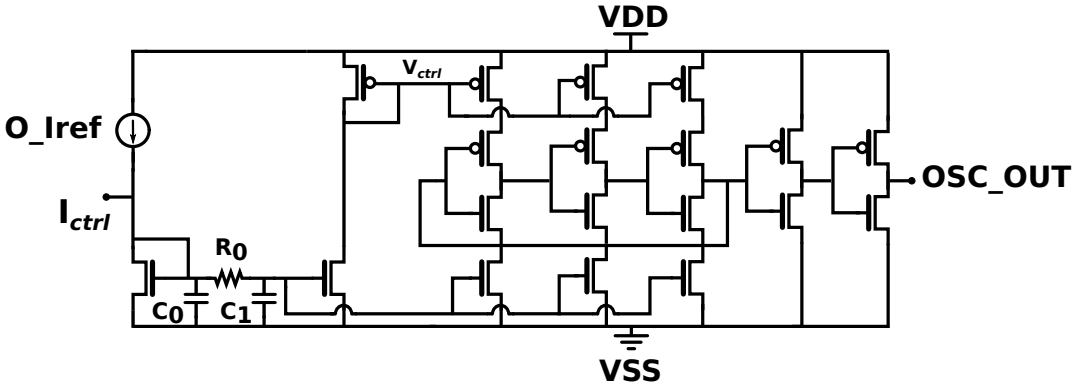


Figure 3.10: Single-ended oscillator schematic.

The performance of the SE-CCO is mainly controlled by the current starved transistors that are connected to the three-inverter stages of the oscillator as they source and sink currents for charging and discharging of the load capacitances of each stage. The load capacitances and the output resistance of each inverter stage determine the delay of each stage which in turn affects the oscillation frequency. It is important to note that the oscillation frequency depends on other parameters as expressed in Equations (3.8), which eventually leads to trade-offs between system requirements such as power consumption and current-to-frequency (I-F) sensitivity [65], [66].

$$F_{osc} \propto \frac{1}{N * \tau_d},\ \tau_d = C_l * R_o,\ R_o \propto \frac{V_{dd}}{I_D} \tag{3.8.a}$$

$$\Rightarrow F_{osc} \propto \frac{I_D}{N * C_l * V_{dd}} \tag{3.8.b}$$

$$\therefore I_D \propto N * C_l * V_{dd} * F_{osc} \tag{3.8.c}$$

$$\Rightarrow P_{osc} \propto N * C_l * (V_{dd})^2 * F_{osc} \tag{3.8.d}$$

where F_{osc} represents the oscillation frequency, N represents the number of inverter stages of the oscillator, C_l represents the load capacitance of each inverter stage, R_o is the output resistance of each inverter stage, τ_d is the propagation time delay

of each inverter stage, P_{osc} represents the power consumed by the oscillator, and I_D is the drain current flowing through each inverter stage which is defined by the combination of I_{ctrl} and O_I_{ref}.

As a result, Equations (3.8) show that increasing the oscillation frequency increases the power consumption of the oscillator. In addition, the power consumed by the oscillator can be significantly reduced by lowering the supply voltage due to the square dependence of P_{osc} on V_{dd}. This implies that, for example reducing V_{dd} by 2, should decrease the power consumption of the oscillator by $\frac{1}{4}$. Moreover, decrease in supply voltage V_{dd} results in minimal trade-off between I-F sensitivity and power consumption since power consumption is reduced by a power of 2, as compared to the effect of the accompanied increase in oscillation frequency F_{osc}. Thus, the SE-CCO used in DORSI is optimized to operate on 1 V supply voltage.

Furthermore, Equations (3.8) show that reducing the output resistance of each inverter stage plays a key role in reducing the delay of each stage which increases the oscillation frequency. The output resistance R_o depends on the channel length of the inverter transistors and the drain current flowing through the transistors in each inverter stage as shown in Equation (3.9). Hence, the output resistance of the SE-CCO is reduced by using short channel lengths for the inverter transistors as shown in Table 3.2, which in turn reduces the total or group delay of the oscillator. The device width of the inverter transistors can also be increased in order to further reduce R_o. However, this increases power consumption due to increase in the gate capacitance of the transistors. The selected aspect ratio ($\frac{W}{L}$) for the inverter transistors are optimized to provide the desired frequency range.

$$R_o = \frac{1}{g_{ds}} = \frac{1 + \lambda * V_{ds}}{\lambda * I_{ds}} \approx \frac{1}{\lambda * I_{ds}} \propto \frac{L}{W} \tag{3.9}$$

The current starved transistors act as current sources (PMOS) and current sinks (NMOS) for the inverter stages. Thus, the current starved transistors are designed with longer channel lengths than those used in the inverter transistors in order to improve current matching between the bias current mirrors and each current source/sink branch of each inverter stage. The bias current mirror transistors are designed to have the same dimensions as the current starving transistors in order to maintain a 1 : 1 current gain ratio.

In addition, the buffer stages are sized to have larger aspect ratio ($\frac{W}{L}$) than those used for the inverter stages in order to increase the driving strength of the oscillator. This is essential in ensuring that the output buffers of the oscillator are able to drive the load from the digital circuits of the ID block. Hence, the buffer stages consume more current due to increase in capacitive load of the oscillator, which contributes to the overall power consumption of the oscillator. It is worth mentioning that power consumption of the oscillator can be reduced by reducing the device width (W) and channel length (L) of the buffer stages while maintaining the same aspect ratio. The decision to use the same L in the buffer stages as in the inverter stages was made in order to maintain good component matching during layout design.

The operation region of the current source transistors (i.e. PMOS current starved transistors) plays an important role in the linearity of the current-to-frequency con-

Table 3.2: Dimensions of the SE-CCO and differential oscillator components

Component	**Current-starved & Bias current-mirror transistors**	**Inverter transistors**	**Buffer transistors**
PMOS	$W = 1.0\mu\text{m}, L = 6.3\mu\text{m}$	$W = 1.0\mu\text{m}, L = 0.84\mu\text{m}$	$W = 3.0\mu\text{m}, L = 0.84\mu\text{m}$
NMOS	$W = 0.4\mu\text{m}, L = 6.3\mu\text{m}$	$W = 0.4\mu\text{m}, L = 0.84\mu\text{m}$	$W = 1.2\mu\text{m}, L = 0.84\mu\text{m}$

version. The drain current I_D of each inverter stage is controlled by the I_{ds} of the current source transistors. Hence, Equations (3.10) show the effect of I_{ds} on the oscillation frequency for the linear region operation of the current source transistors. The oscillation frequency depends linearly on the drain current I_{ds}, and I_{ds} is linearly proportional to the square of the supply voltage V_{dd} as presented in Equation (3.10).

$$I_{ds} = \beta \left\{ [(V_{gs} - V_{th}) * V_{ds}] - \frac{(V_{ds})^2}{2} \right\} * (1 + \lambda * V_{ds}) \tag{3.10.a}$$

$$R_o \approx \frac{1}{\lambda * I_{ds}} \propto \frac{1}{\beta(V_{gs} - V_{th}) * V_{ds}},\ where\ \beta = \mu_0 C_{ox} \left(\frac{W}{L}\right) \tag{3.10.b}$$

$$\Rightarrow F_{osc} \propto \frac{I_{ds}}{N * C_l * V_{dd}} \propto \frac{\beta(V_g - V_{dd} - V_{th}) * (V_d - V_{dd})}{V_{dd}} \tag{3.10.c}$$

$$\therefore F_{osc} \propto I_{ds},\ I_{ds} \propto \left[(V_{dd})^2 - V_{th}\right] \Rightarrow F_{osc} \propto \frac{(V_{dd})^2 - V_{th}}{V_{dd}} \tag{3.10.d}$$

The current source transistors are designed to operate in the linear region but may drift into the saturation region as I_{ds} increases due to increase in control current I_{ctrl} or bias current O_I_{ref} of the oscillator. Thus, the overdrive voltage (i.e. $V_{gs} - V_{th}$) of the current source transistors increases as I_{ds} increases, which reduces the output resistance R_o of these transistors. The dependence of R_o on the overdrive voltage (V_{ov}) leads to an interesting observation in the relationship between the oscillation frequency and the supply voltage V_{dd} as presented in the following Equations (3.11), for the saturation region operation of the current source transistors.

$$I_{ds} = \frac{\beta}{2} \left\{ (V_{gs} - V_{th})^2 \right\} * (1 + \lambda * V_{ds}) \tag{3.11.a}$$

$$R_o \approx \frac{1}{\lambda * I_{ds}} \propto \frac{2}{\beta(V_{ov})^2},\ where\ V_{ov} = (V_{gs} - V_{th}) \propto \sqrt{\frac{2 * L * I_{ds}}{\mu_0 * C_{ox} * W}} \tag{3.11.b}$$

$$\Rightarrow F_{osc} \propto \frac{I_{ds}}{N * C_l * V_{dd}} \propto \frac{\beta}{2}(V_{ov})^2 = \frac{\beta * (V_g - V_{dd} - V_{th})^2}{2 * V_{dd}} \tag{3.11.c}$$

$$\therefore F_{osc} \propto I_{ds},\ I_{ds} \propto \left[\frac{(V_{dd} - V_{th})^2}{2}\right] \Rightarrow F_{osc} \propto \frac{(V_{dd} - V_{th})^2}{2 * V_{dd}} \tag{3.11.d}$$

Equations (3.11) show that the oscillation frequency is also linearly proportional to the drain-source current I_{ds} of the current source transistors even when operat-

ing in saturation region. However, I_{ds} shows a square dependence on the overdrive voltage V_{ov} of the current source transistors. This implies that, for example increasing I_{ds} by a factor of 4, should increase the overdrive voltage V_{ov} of the current source transistors by $\sqrt{8}$. The square relationship between I_{ds} and the overdrive voltage could be a source of non-linearity in the oscillator as I_{ds} increases. Thus, it is essential that both bias current mirror and current source/sink transistors of each inverter stage, remain in the same operating region through out the required frequency range. Further analysis of this effect and other possible sources of non-linearity in the oscillator is required to minimize the linearity error in the current to frequency conversion which in turn improves the ENOB that is obtained from the ID block. In addition, Equation (3.11) shows the relationship between F_{osc} and the supply voltage V_{dd} when the current source transistors are operating in saturation region. Thus, F_{osc} shows about half of the square dependence on supply voltage that is observed in linear region.

Equations (3.10) and (3.11) describe the impact of the output resistance and operating region of the current source transistors on the oscillation frequency. The rest of the equations in this section are related to the operation of the inverter transistors and its contribution to the gain and PSRR of the I-F stage. The rate of change of the oscillation frequency with respect to the minimum change in current (i.e. $\frac{\partial F_{osc}}{\partial I_D}$) is an important factor in the design of the I-F block. This relationship defines the current-to-frequency (I-F) sensitivity and conversion gain as presented in Equation (3.12) based on Equations (3.8).

$$\frac{\partial F_{osc}}{\partial I_D} = \frac{1}{N * C_l * V_{dd}} \tag{3.12}$$

Equation (3.12) shows that high current-to-frequency (I-F) sensitivity is achieved by reducing the number of stages and the propagation time delay between inverter stages. Hence, the use of three inverter stages as an optimum N in the SE-CCO in order to maximize the I-F sensitivity while optimizing the oscillator to meet other design requirements of DORSI. Equation (3.12) also reflects an inverse relationship between V_{dd} and I-F sensitivity. This implies that, increasing the supply voltage requires longer time to charge C_l to V_{dd} which increases the propagation delay τ_d and decreases the oscillation frequency. Hence, the use of lower supply voltage in the design of the SE-CCO also improves the I-F sensitivity since the time required to charge C_l is shorter which makes the oscillator run faster. Alternatively, I-F sensitivity can also be defined as in Equation (3.13) based on Equations (3.9) and (3.8). Equation (3.13) shows that the I-F sensitivity can also be increased by reducing the channel length of the inverter transistors.

$$\Rightarrow \frac{\partial F_{osc}}{\partial I_D} = \frac{\lambda}{N * C_l} \tag{3.13}$$

In addition, the sensitivity of the oscillator to variations in supply voltage can be expressed as the rate of change of the oscillation frequency to the change in supply voltage (i.e. $\frac{\partial F_{osc}}{\partial V_{dd}}$) which has a non-linear dependence on V_{dd} as shown in Equation (3.14). As a result, oscillators are known to have poor power supply rejection ratio

(PSRR) since a small change in V_{dd} leads to significant change in F_{osc} [66]. Thus, reduction of supply noise and improving the PSRR are important factors in the performance of the SE-CCO.

$$\frac{\partial F_{osc}}{\partial V_{dd}} = -\frac{I_D}{N * C_l * (V_{dd})^2} \tag{3.14}$$

Thus, for linear region operation of the inverter transistors:

$$\Rightarrow \frac{\partial F_{osc}}{\partial V_{dd}} \propto -\frac{\beta(V_{gs} - V_{th}) * V_{ds}}{N * C_l * (V_{dd})^2} \tag{3.15}$$

On the other hand, for saturation region operation of the inverter transistors:

$$\Rightarrow \frac{\partial F_{osc}}{\partial V_{dd}} \propto -\frac{\beta(V_{gs} - V_{th})^2}{2 * N * C_l * (V_{dd})^2} \tag{3.16}$$

Furthermore, Equations (3.15) and (3.16) show an important relationship between the threshold voltage of the inverter transistors and V_{dd}-sensitivity of the oscillator, for linear and saturation operating regions respectively. Equations (3.15) and (3.16) show that reducing the threshold voltage of the transistors used in the inverter stages lowers the sensitivity of the oscillator to variations in V_{dd}, which in turn improves the PSRR of the oscillator. Thus, the threshold voltage V_{th} of the inverter transistors are lowered by connecting the bulk and source nodes of each transistor together in order to keep $V_{SB} = 0$ as presented in Equation (3.17.b).

$$V_{th} = V_{T0} + \gamma \left(\sqrt{(2|\phi_F| + V_{SB})} - \sqrt{2|\phi_F|} \right) \tag{3.17.a}$$

$$\therefore V_{th} = V_{T0},\ when(V_{SB} = 0) \tag{3.17.b}$$

where β represents the transconductance parameter, γ is the bulk threshold parameter, V_{SB} is the source-bulk voltage and ϕ_F represents surface potential of the MOS device in strong inversion [64]. In addition, another reason for using long channel lengths for the current-starved transistors is to minimize the effect of supply noise on F_{osc}. Detailed derivations showing the effect of V_{th}, L and other parameters on the V_{dd}-sensitivity of the oscillator are available in appendix C.

Ideally, the oscillation frequency F_{osc} should remain constant when the drain current I_D is constant but this is not the case in reality due to variations in other parameters that F_{osc} depends on. Equations (3.14) and (C12)[3] reveal an interesting relationship between I_D and V_{dd}. This relationship shows that when I_D is constant, the oscillator is operating in a region where deviations seen in the oscillation frequency ΔF_{osc} can be attributed to variations in delay between inverter stages $\Delta\tau_d$ which is mainly controlled by the supply voltage V_{dd}, load capacitance C_l, number of stages N and channel length of the inverter stages.

The time it takes to charge C_l to V_{dd} and to discharge it to the ground voltage V_{ss} in all the inverter stages defines the total or group delay. Hence, the oscillation

[3]Note: referring to an equation in Appendix C

frequency varies inversely with changes in the propagation delay τ_d. In other words, the effect of the delay of each inverter stage due to the aforementioned factors (i.e. C_l, V_{dd}, N, L), dominates the control of the oscillation frequency in this region where I_D is relatively constant or the changes in I_D is small. Thus, the oscillation frequency varies inversely with changes in the supply voltage, for relatively small changes in V_{dd} as presented in Equation (3.18).

$$\Delta F_{osc} \propto \frac{1}{\Delta \tau_d},\ \Delta \tau_d \propto \Delta V_{dd} \tag{3.18}$$

However, as variations in supply voltage increase due to supply noise, the drain current I_D increases. As a result, the linear relationship between the drain current I_D and the oscillation frequency F_{osc} begins to dominate. This behaviour is due to an increase in I_{ds} of the current source transistors as V_{dd} increases based on Equations (3.10) and (3.11) which show the following relationship in Equation (3.19):

$$\Delta F_{osc} \propto \Delta I_D,\ \Delta I_D \propto \Delta V_{dd} \tag{3.19}$$

Thus, the propagation delay τ_d of the oscillator is decreased as the output resistance R_o decreases due to increase in I_D as expressed in Equation (3.20).

$$\tau_d \propto R_o \propto \frac{1}{I_D} \tag{3.20}$$

Hence, this co-dependence of the drain current I_D on the supply voltage V_{dd} and oscillation frequency F_{osc} must be carefully considered when designing oscillators with high PSRR. One way of improving the PSRR is to design the oscillator so that the drain current I_{ds} of the current source transistor is independent of V_{dd}. The other technique that is commonly used is implementing the oscillator with differential delay cells or inverter stages in order to cancel out deviations in oscillation frequency ΔF_{osc} due to variations in supply voltage ΔV_{dd}. In addition, the gain of the current-to-frequency conversion is improved by increasing the PSRR of the oscillator, which reduces the effect of supply noise on the I-F sensitivity.

The noise performance of the oscillator and the whole analog domain is optimized so that the I-F sensitivity is higher than the noise-limited sensitivity in order for changes in the redox current signals from the sensor electrodes to be detected. This implies that, the I-F sensitivity should be higher than frequency deviations (in Hz) caused as a result of current noise. Hence, the RMS current noise in the I-F stage is optimized to be significantly lower than the required current resolution of $1nA$. Thus, the minimum detectable change in current ΔI_{min} is mainly defined by the RMS current noise.

Another benefit of having high I-F sensitivity is that it improves the noise averaging performance of the ID block as the number of pulses increase within the defined sampling interval as earlier illustrated in Figure 3.4. In addition, another noise optimization consideration in the design of the I-F block for improving the resolution of the system is reduction of phase noise and jitter. This is because the effect of phase noise and jitter leads to deviation in oscillation frequency (ΔF_{osc})

which reflects on the performance of the A/D conversion. In other words, the cumulative effect of known noise sources such as flicker noise, thermal noise, supply noise and substrate noise is directly visible as deviations in time domain which is translated after A/D conversion as conversion error (ΔC) [59], [67], [66].

One of the design decisions to minimize the effect of phase noise and jitter is the use of the RC-filter at the bias current source in order to reduce the contribution of flicker and thermal noise from the bias current mirror transistors which reduces fluctuations in the current flowing through them. It is important to note that the values of RC components in this configuration are critical since the signal path is combined with the bias path. Ideally, they should be separated as discussed earlier in section 3.2.1, in order to keep the signal transfer function independent of the noise transfer function which provides more freedom in the selection of RC components. In addition, current matching between the current mirror transistors is improved by increasing the length of the bias transistors, which in turn reduces jitter, phase errors and quantization errors due to component mismatch [68]. The need to reduce the effect of supply noise led to the implementation of the differential oscillator which is presented in Figure 3.11. Other techniques for reducing ΔF_{osc} and ΔC due to supply noise and substrate noise can be implemented in the layout as presented in appendix B.6.2.

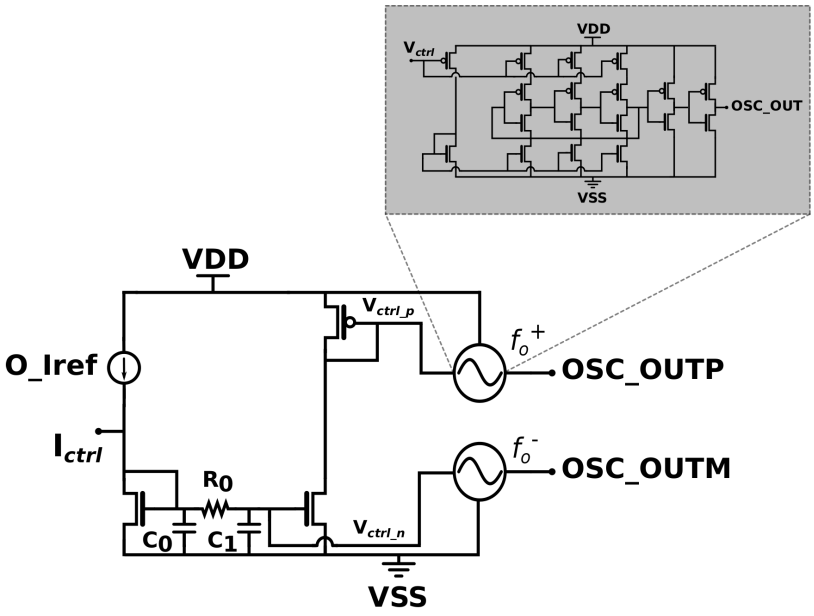


Figure 3.11: Differential oscillator schematic.

The differential oscillator is designed based on the single-ended CCO blocks with a slight modification in the bias circuitry as shown in Figure 3.11. The bias NMOS current mirror controls one SE-CCO and the PMOS current conveyor controls the other SE-CCO. Hence, the current from the PMOS current mirror branch controls the positive output of the oscillator (OSC_OUTP) which in turn controls the positive digital output (DIG_OUTP) of the ID block. Similarly, the current from the NMOS current mirror branch controls the negative output of the oscillator

(OSC_OUTM) which in turn controls the negative digital output (DIG_OUTM) of the ID block. The output signal from OSC_OUTP shows an increase in frequency while the output signal from OSC_OUTM shows the opposite (i.e. decrease in frequency). Thus, both outputs are complementary to each other and when subtracted from each other, they provide twice the current-to-frequency (I-F) sensitivity of a single oscillator. Hence, the differential operation of DORSI improves the linearity of the I-F conversion and increases the conversion gain which improves the resolution attained from the ID stage.

Typically, there is a limit to which increasing the oscillation frequency in order to improve I-F sensitivity and to reduce conversion error can be tolerated, in order to avoid exacerbating non-linearity of the oscillator. This is due to the effect of switching noise on the linearity and accuracy of the current-to-frequency conversion increases as the oscillation frequency increases [69]. Switching noise can be in the form of mismatch in the toggle points of pull-up and pull-down transitions in each inverter stage. This mismatch in toggle points of rise and fall transitions is seen as jitter in time domain and conversion error in the digital output code [66], [69].

In addition, the linearity performance of oscillator-based ADC structures is mainly determined by the current-to-frequency transfer characteristic of the oscillator [70], [71]. Hence, there is a trade-off between the benefit of noise averaging as the oscillation frequency increases, and linearity in the A/D conversion. As a result, it is important to define the frequency range of the oscillator within the limits that provide the most optimal noise averaging-linearity performance. Simulation results show that increasing the oscillation frequency outside the optimal frequency range, degrades the linearity of the oscillator. These simulation results are presented in section 4.1.3, where the oscillator has been optimized to operate at maximum 10 MHz for the required 1.2 μA current range.

On the other hand, the use of differential oscillator provides an alternative for doubling the oscillation frequency without degrading the linearity of the oscillator. Infact, the linearity of the differential oscillator is expected to be better than that of the SE-CCO since some of the linearity errors are cancelled out during subtraction of both digital outputs in the ID stage. Likewise, the PSRR of the differential oscillator is expected to be higher than that of the SE-CCO since the variations in frequency due to supply noise are minimized. However, the power consumption of the overall I-F stage is doubled due to the use of two SE-CCO blocks in the differential oscillator. Thus, the use of low supply voltage is even more important in reducing the power consumption of the differential oscillator. Another advantage of using a lower supply voltage is that there is no need for implementing a level-shifter between the analog and digital domain, which is also operating at 1 V supply voltage. This results in easy integration between the outputs of the oscillator and the current-discretization (ID) block.

3.2.3 Discrete detection of dopamine

The operation of DORSI continues from the current-to-frequency (I-F) stage to the current-discretization (ID) stage with the transition between the I-F and ID blocks occurring in digital domain as the output of the oscillator is fed directly to the ID block for final processing of the redox current signal from the sensor. This block represents the DSP block of the readout circuit which implements additional ADC, noise filtering and encoding functions for discrete detection of dopamine.

The positive digital output (DIG_OUTP) from this block is defined by the positive input signal from the oscillator (osc_inp) while the negative digital output (DIG_OUTM) of this block is defined by the negative input signal from the oscillator (osc_inm) as illustrated in Figure 3.12. Thus, when the digital output stream from DIG_OUTP shows an increase in number of pulses (N_p) within the specified sampling period (T_s) due to increase in frequency of the oscillator, the digital output stream from DIG_OUTM shows the opposite (i.e. decrease in number of pulses within the same sampling time interval). Finally, the digital output code (D_{OUT}) is obtained from the ID block as the difference between both digital outputs DIG_OUTP and DIG_OUTM.

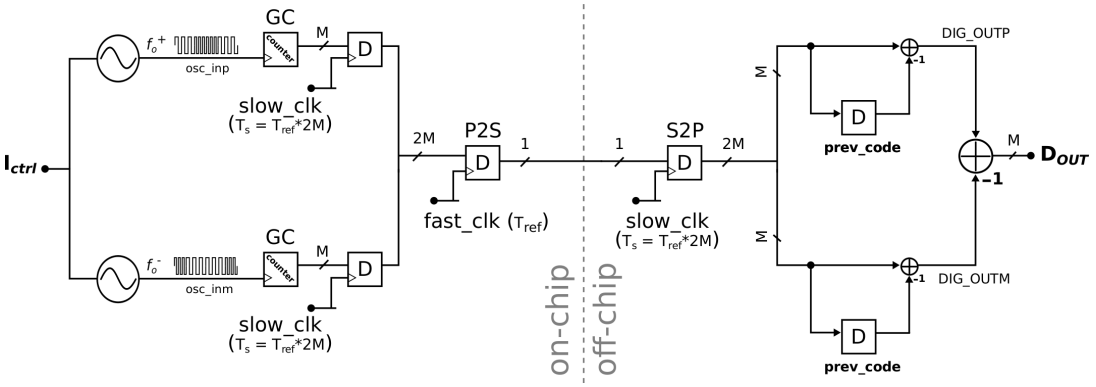


Figure 3.12: Structure and clock distribution of the ID block.

The processing of the output of the oscillator in order to obtain the digital output code involves several intermediate process steps as described in Figure 3.12. Thus, part of the digital signal processing is done on-chip and the other part is done off-chip as post-processing in Matlab. The on-chip part of the ID block performs the integration of the pulses from the oscillator and buffers the differential outputs of the counter into a readout register. The accumulated counter code (i.e. M-bit) is read from the readout register of each differential output and combined to form $2M$-bit code representing both DIG_OUTP and DIG_OUTM outputs. Then, the $2M$-bit code is buffered through the parallel-to-serial (P2S) block for converting the multi-bit digital code (i.e. $2M$) to single-bit code. The serialized single-bit code is propagated as the output of the DORSI chip for further processing by the off-chip algorithm implemented in Matlab.

The post-processing that is performed in Matlab includes a serial-to-parallel (S2P) block that de-serializes the serial output from the chip. The de-serialized

output $2M$-bit code is split into two M-bit codes, where each M-bit code represents each differential output. Then, derivation is performed on the sequence of M-bit code from the S2P block. Thus, the previous M-bit code is subtracted from the current M-bit code in order to obtain the DIG_OUTP and DIG_OUTM output codes. Finally, the difference between DIG_OUTP and DIG_OUTM codes are obtained from the ID block as D_{OUT}, which provides a digital representation of the detected concentration of dopamine.

The design of the ID block is based on a digital counter that is incremented after every period of the input signal from the oscillator (osc_in). This implies that, the counter is incremented at every rising edge of each pulse of the sampled signal from the oscillator. The output of the counter is a multi-bit digital code (M) which is stored in a register and propagated to the P2S block at the rising edge of the $slow\_clk$. The digital code from the P2S block is sampled with the $fast\_clk$ and the de-serialized code is stored in a register off-chip during post-processing. The stored de-serialized code is later subtracted from the next accumulated value of the counter for each decimation event which is triggered by the $slow\_clk$.

Thus, the counter represents the core component of the ID block and performs two main functions. The input signal from the oscillator which is modulated by the redox current from the sensor, is integrated continuously and quantized by the counter. The quantized data periodically undergoes derivation at the rising edge of the sampling clock ($meas\_trig$), which triggers the difference between the previous and current accumulated codes to be evaluated during decimation. The sampling clock $meas\_trig$ defines the sampling interval T_s. The sampling interval T_s defines the decimation rate as depicted in Figure 3.4 and earlier discussed in section 3.1. Hence, the operation of the ID block results in noise averaging based on the principle of cascaded integrated comb (CIC) filters as described in discrete time by Figure 3.13 and Equation (3.21).

$$w[n] = x[n] + w[n-1] \tag{3.21.a}$$

$$y[n] = w[n] - w[n-N] \tag{3.21.b}$$

$$\Rightarrow y[n] = x[n] + x[n-1] + x[n-2] + ... + x[n-(N-1)] \tag{3.21.c}$$

CIC filter based structures are used for implementing decimation or interpolation system functions in various applications related to high data rate processing [72], [73]. These applications include modulation and demodulation in wireless systems and more commonly in digital-to-analog (D/A) and A/D converters [73]. The typical structure of CIC decimation filter is presented in the (A) part of Figure 3.13 and the (B) part of Figure 3.13 shows the structure used in the ID block. Both structures are equivalent in functionality but the CIC filter structure used in the ID block is especially effective in reducing power consumption due to reduced sampling rate before derivation is performed [73]. Hence, the digital output code D_{OUT} from the ID block represents the decimated code and the derivation function is implemented off-chip during post-processing in Matlab.

The use of CIC filters as part of the noise averaging process is known to be effective in preventing aliasing of wide-band noise into the signal bandwidth, which

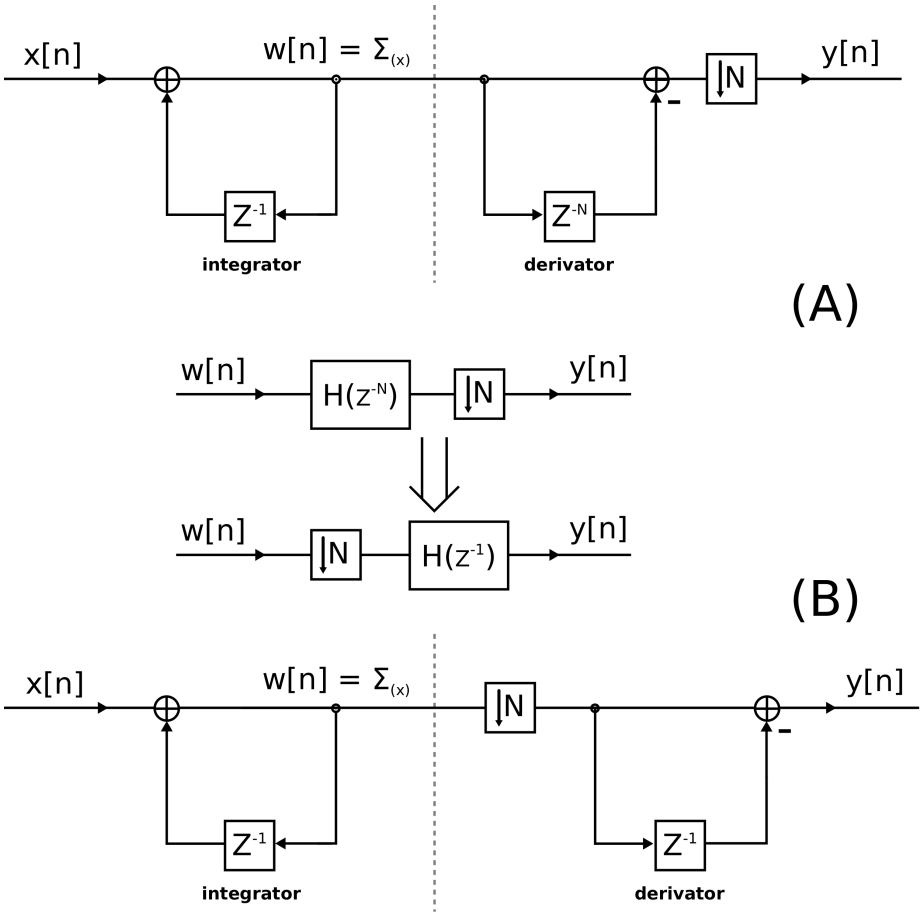


Figure 3.13: Counter filtering principle based on CIC-filter structures.

alleviates the need for an anti-aliasing filter within the ADC [74], [70], [72]. However, it should be noted that a pre-filter can still be applied before the A/D conversion in order to limit the noise bandwidth if necessary.

In addition, the combination of using the oscillator as an integrator together with the counter as a quantizer and differentiator eliminates the need for sample and hold stage during the A/D conversion [13], [74], [70]. Other advantages of using this ADC structure is that it reduces the effect of DC offset and filters high-frequency noise [13], [74], [75]. This is as a result of its inherent low-pass characteristic based on its *sinc* filter transfer function as shown in Equation (3.22). The corresponding frequency response of the *sinc* filter transfer function is presented in Figure 3.14. The transfer

function of the counter based filter is given as follows, based on Equation (3.21):

$$W(z) = \frac{X(z)}{1 - z^{-1}} \tag{3.22.a}$$

$$Y(z) = W(z) * (1 - z^{-N}) \tag{3.22.b}$$

$$Y(z) = \left[\frac{X(z)}{1 - z^{-1}}\right] * (1 - z^{-N}) \tag{3.22.c}$$

$$\Rightarrow H(z) = \frac{Y(z)}{X(z)} = \frac{1 - z^{-N}}{1 - z^{-1}} \tag{3.22.d}$$

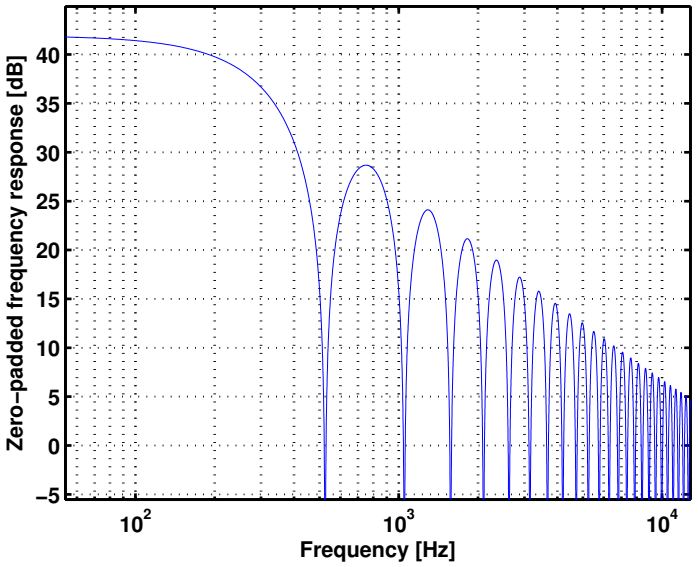


Figure 3.14: Frequency response of counter based filter model.

Noise averaging capabilities of the counter based filter can be improved by increasing the number of samples (N_s) taken within a given measurement time (T_{meas}). The number of samples depends on the pre-defined sampling rate F_s and the measurement time as expressed in Equation (3.23).

$$N_s = \frac{T_{meas}}{T_s} = T_{meas} * F_s \tag{3.23}$$

Hence, N_s can be increased either by increasing the measurement time T_{meas} or by increasing the sampling rate F_s as depicted in Figure 3.15. In addition, increasing the number of pulses counted by the counter within the given sampling interval T_s, also improves the noise performance of the ID block. This in practice means that the operating frequency of the oscillator can be increased in order to generate more pulses for the counter. Hence, the measurement time can be reduced when the oscillator is tuned to operate at higher frequencies. Furthermore, conversion errors due to quantization noise and thermal noise are reduced as a result of increasing

the number of samples used during the averaging process. Thus, the signal to quantization noise ratio (SQNR) is improved which in turn improves the overall signal resolution [75]. Figure 3.15 demonstrates the effect of number of samples N_s on the averaged signal either by altering T_{meas} or F_s. The simulation setup used for generating Figure 3.15 is implemented in Matlab based on the transfer function presented in Equation (3.22). In addition, the effect of oversampling is more evident in the simulation presented in Figure 3.15 since the added random noise is not band limited.

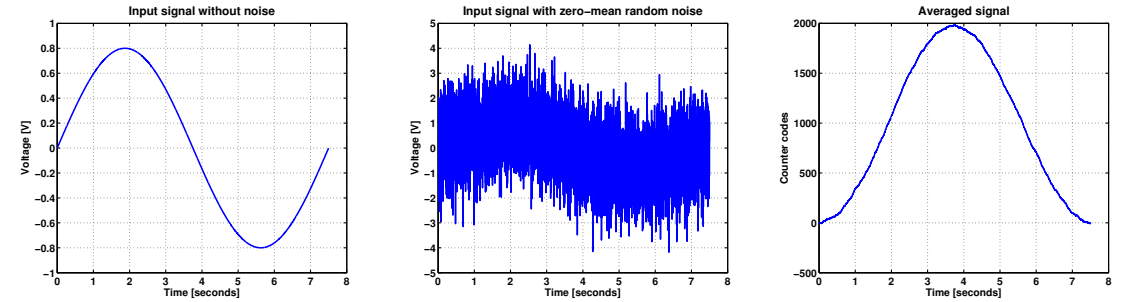
Figures 3.15a and 3.15d illustrate that similar noise averaging performance is achieved either by reducing the measurement time T_{meas} and increasing the sampling rate F_s or vice-versa, as long as the number of samples N_s remains the same. On the other hand, Figure 3.15b shows that increasing F_s without reducing T_{meas}, results in larger number of samples which provides the best signal resolution of the four examples depicted in Figures (3.15a) - (3.15d). However, depending on the desired signal resolution, the measurement time should be defined based on the required conversion rate. Finally, Figure 3.15c shows that reducing T_{meas} without increasing F_s, lowers the number of samples and decreases the noise averaging effect. Thus, Figure 3.15c achieves the worst signal resolution of the four examples given in Figure 3.15 due to poor noise averaging performance. Hence, parameters T_{meas} and F_s must be chosen carefully in order to obtain the required signal resolution.

In addition, the effect of jitter on the A/D conversion plays an important role on the achieved signal quality. Jitter or timing error in the oscillation period contributes to the overall conversion error ΔC in the counter code and if random, it is visible as noise in the counter code. It is important to mention that jitter in the oscillator period is only visible to the counter on threshold crossings of the pulses generated by the oscillator. Hence, the effect of timing error on the output digital code from the counter is visible after each sampling interval T_s and affects the overall quantized data as a cumulative sampled random process during the pre-defined measurement time T_{meas}. As a result, Equation (3.24) holds for all conversion codes C during T_{meas}, where each conversion or counter code is the total number of pulses or periods of the oscillator within each sampling interval T_s.

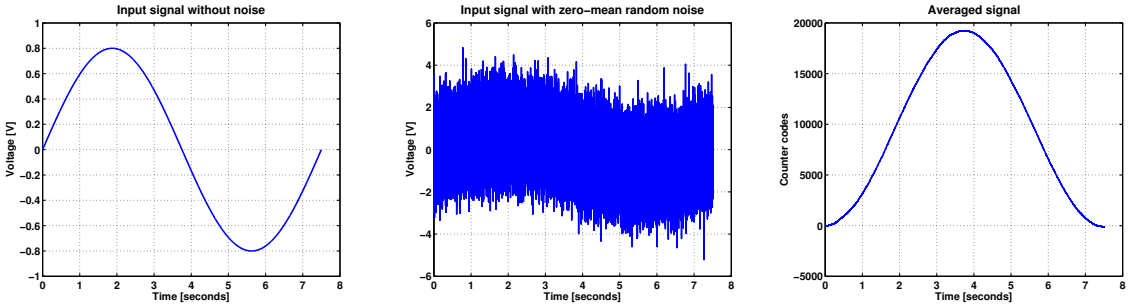
$$\Delta T = \sum_{n=0}^{C-1} \epsilon_t(nT_{osc}) \tag{3.24}$$

where T_{osc} is the period of the oscillator corresponding to the inverse of the oscillator frequency (F_{osc}), $\epsilon_t(t)$ represents timing error or jitter, ΔT is the total timing error and n represents the number of pulses or oscillator periods. Thus, reduction of jitter in the design of the oscillator and increasing the number of pulses (n) or samples (N_s) by increasing the oscillator frequency or sampling rate respectively is vital in minimizing conversion errors in the counter codes which in turn improves the resolution of the detected redox current signal.

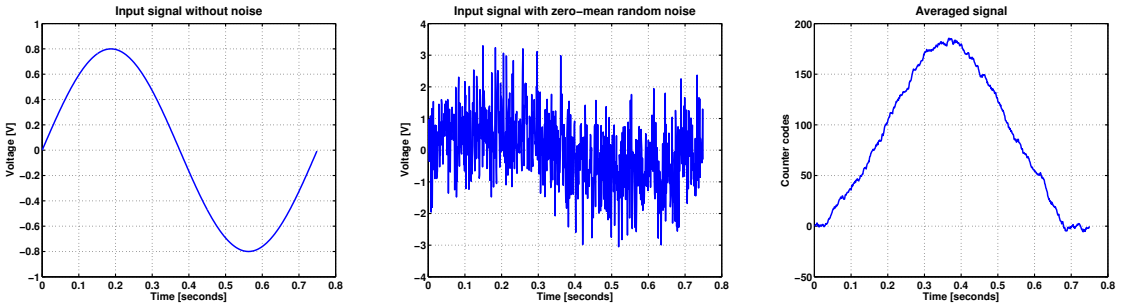
[4]Note: the averaged signals presented in figure 3.15 are modelled in Matlab with 'filter' or 'conv' methods and exhibit $\sim 90^o$ phase shift due to integration of the input sine wave as a result of the transfer function of the counter filter model.



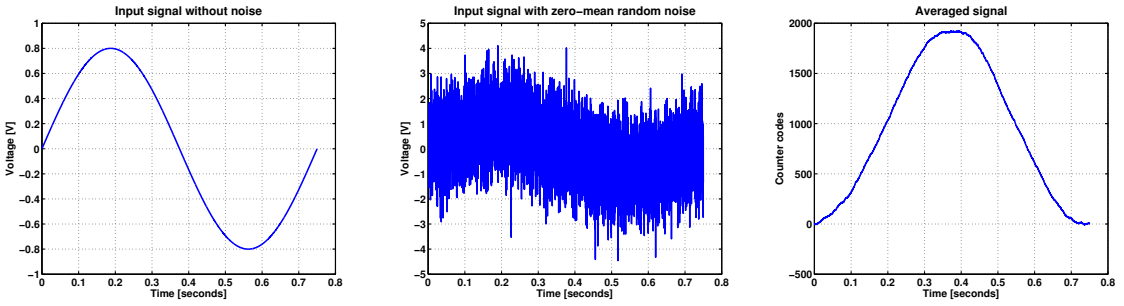
(a) $T_{meas} = 7.5s, F_s = 1KHz \Rightarrow (N_s = 7500)$



(b) $T_{meas} = 7.5s, F_s = 10KHz \Rightarrow (N_s = 75000)$



(c) $T_{meas} = 750ms, F_s = 1KHz \Rightarrow (N_s = 750)$



(d) $T_{meas} = 750ms, F_s = 10KHz \Rightarrow (N_s = 7500)$

Figure 3.15: Effect of measurement time and sampling rate on averaged signal. [4]

Furthermore, the ID block consists of two clock domains as depicted in Figure 3.16. The increment clock domain is controlled by the pulses from the oscillator

while the readout clock domain is controlled by the *meas_trig* clock which defines the sampling time interval T_s. As a result, there is a possibility of timing-violation between the two clock domains. This timing violation could occur when the increment clock event and readout clock events occur at the same time or very close to each other. For example, when the counter is updating the sync register with a new code after an increment event is triggered by the *osc_in* clock, and the ID block also tries to read the latest code from the sync register into the readout register. Hence, the ID block is designed to minimize the effect of possible metastability in the counter codes due to timing violations.

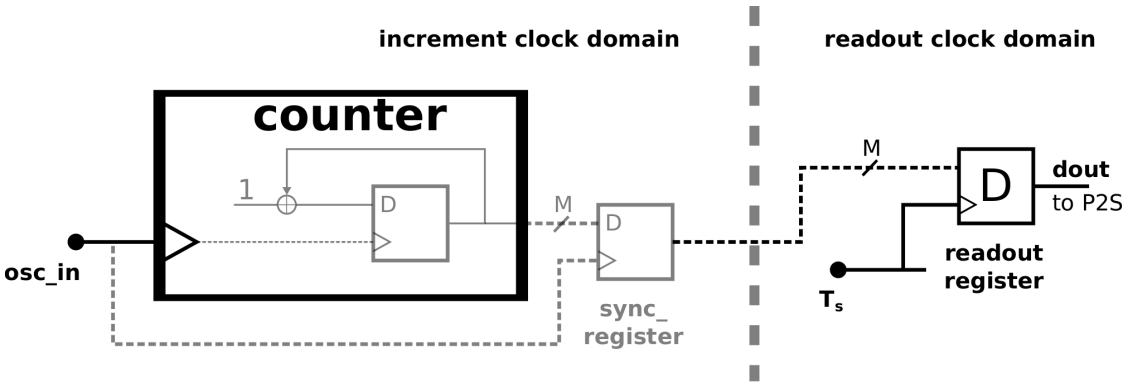


Figure 3.16: Clock domains of the ID block.

Figure 3.17 illustrates the effect of using binary codes as compared to gray codes, if a timing violation occurs when the output of a 2-bit counter is changing from 01 to 10 (i.e. from 1 to 2 decimal code). The timing violation may cause the changing bit to go to an unknown or metastable state which is identified as X in Figure 3.17. The changing bit will eventually settle to either 1 or 0 after some time but the initial metastable state already causes some inaccuracy in the counter output codes which will affect subsequent codes. As a result, the use of gray codes limits the number of bits that are changing to 1 bit as compared to binary codes. Thus, conversion errors caused as a result of possible metastability in the counter output are reduced by using a gray code counter (GC) instead of a binary code counter. The use of gray-encoding of the discretized redox current signal limits the error due to metastability which increases the reliability and accuracy of the digital code representation of the detected dopamine concentration. Thus, making the design of DORSI robust against metastability errors which may occur when a digital system enters an undefined state as a result of synchronization errors that cause two clocked events to happen within close proximity in time or at the same time [76].

Asynchronous clocks may lead to timing violations and using gray code counter minimizes the error seen in the digital output code D_{OUT}. The effect of timing violations is seen as metastability in D_{OUT} and the effect of metastability is mitigated by encoding the counter value as gray codes. Gray codes are typically used to ensure that the system does not enter an intermediate state since only a single bit changes when transitioning from one state to the other as depicted in Figure 3.18 [76], [77]. Thus, the conversion error due to metastability is limited to 1 LSB change in the

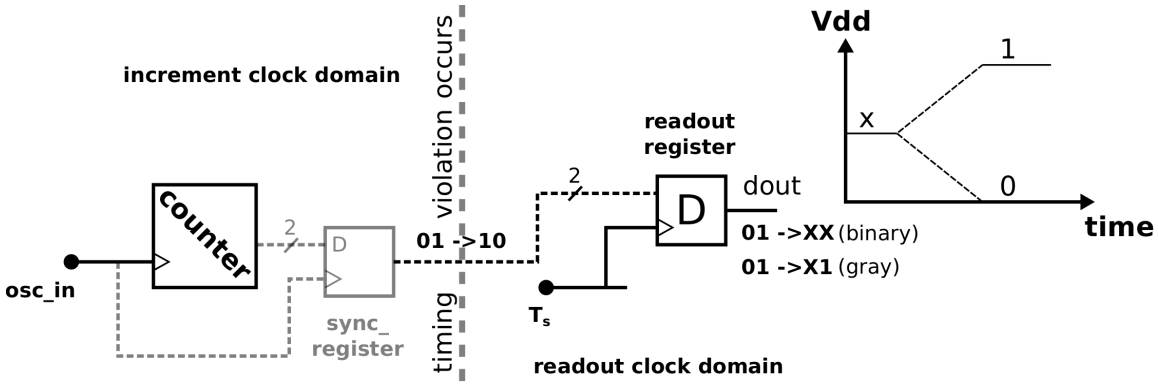


Figure 3.17: Effect of timing violation across clock domains of the ID block.

code. Hence, further errors resulting from the initial error caused by metastability are prevented and the system is restored to a stable state after 1 LSB change in the counter code.

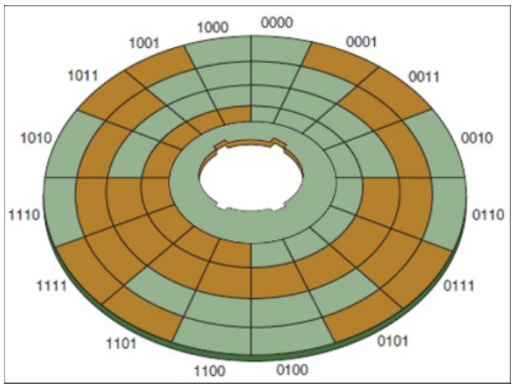
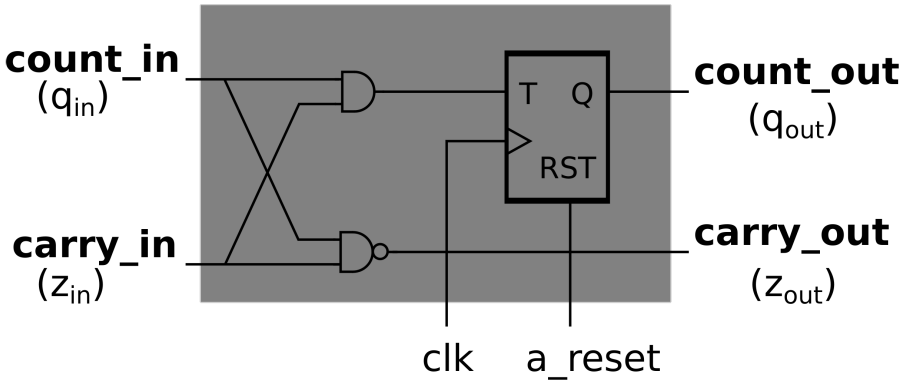


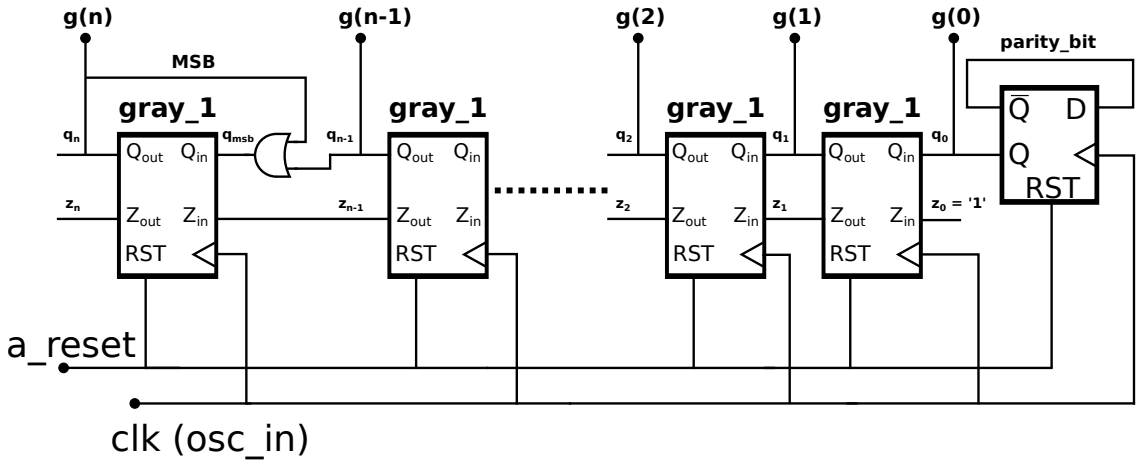
Figure 3.18: Illustration of gray code sequence for a 4-bit counter. [77]

The internal structure of the gray code counter is presented in Figure 3.19. Figure 3.19a shows that the gray counter is based on the characteristics of a T-type flip-flop. That is, the output of the flip-flop (Q) is toggled when the input signal (T) is high and it retains the previous output value (Q) when the input signal (T) is low. The structure of a multi-bit gray code counter is presented in Figure 3.19b which is based on the single-bit gray code counter ($gray\_1$) in Figure 3.19a. In addition, all reset signals in the ID block are designed to be asynchronous and denoted as a_reset.

Finally, the operation of the ID block is presented in Figure 3.20 which describes the relationship between main signals and expected response of the system to important signal transitions. Signal $meas\_trig$ triggers the increment process of the counter and defines the sampling interval T_s. The accumulated gray code (gc_count) is read out as (D_{OUT}) at each rising edge of the $meas\_trig$ signal. The parallel-to-serial (P2S) block is operating at a faster clock rate (i.e. $M * F_s$) than the readout rate (F_s) of the counter. The analog representation of the counter codes is obtained by subtracting the previous gray code value in the d_out register (i.e.



(a) 1-bit GC schematic (*gray_1*).



(b) n-bit GC schematic.

Figure 3.19: Schematic of the gray code counter (GC).

acquired during the previous sampling interval), from the current counter value. The effect of the asynchronous reset is also visible in Figure 3.20 as the counter is zeroed when the actual attained counter code by the next sampling event is much higher. In addition, signal *en_osc_out* is implemented to enable the readout of raw data from the oscillator as *osc_out*.

Lastly, it is important to note that the counter may overflow at some point due to its recursive running sum behaviour [72]. However, the possibility of an overflow depends on the measurement time and the oscillator frequency. As a result, the sampling interval T_s during which the counter code accumulates must be defined

[5]Note: signals in figure 3.20 are not drawn to scale in order to show intermediate transitions and the number of bits (M=8) is only for illustration purpose. The actual number of bits implemented on-chip is M=16.

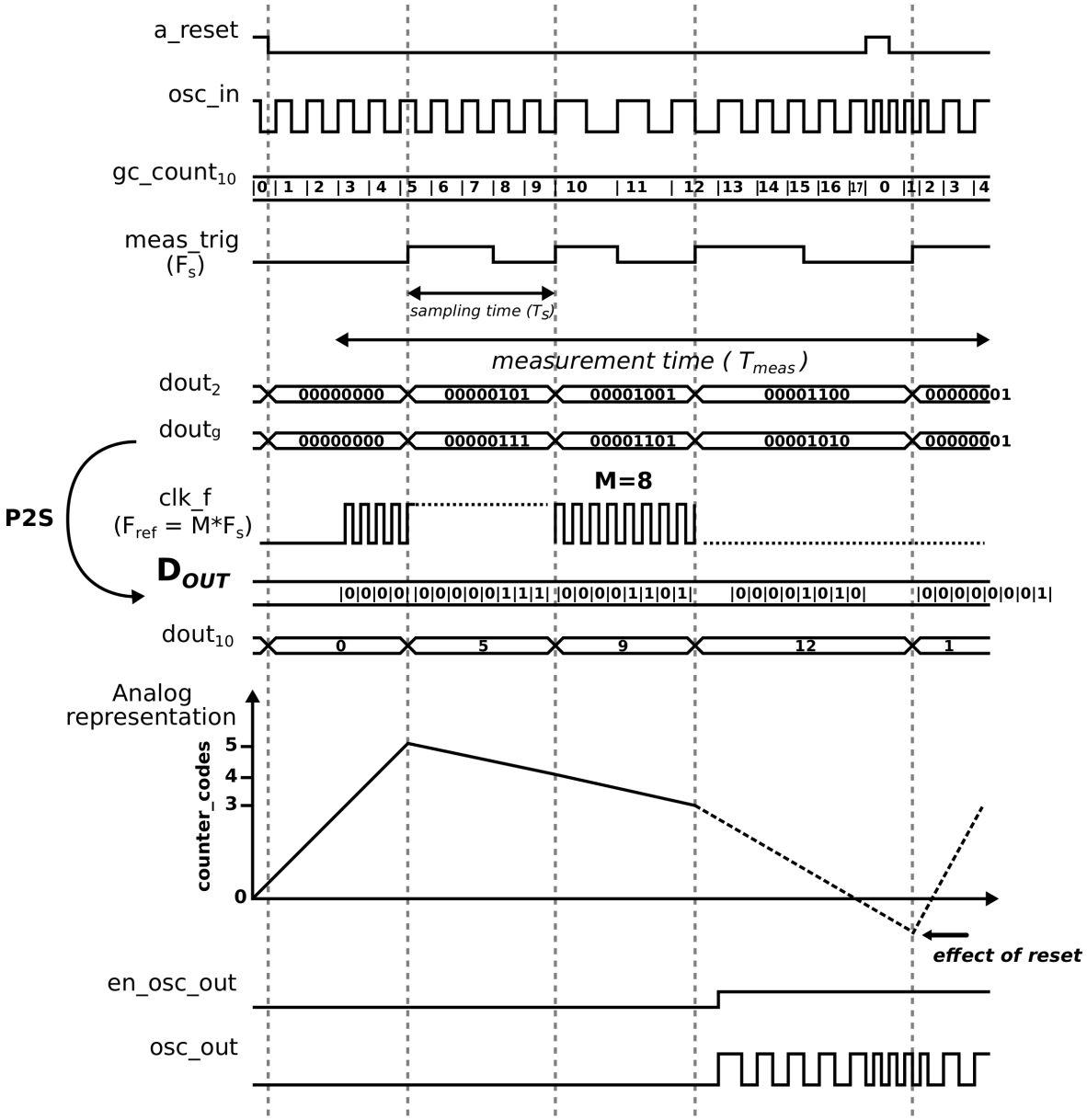


Figure 3.20: Timing diagram illustrating the operation of the ID block. [5]

to accommodate not more than a single overflow. This implies that, the difference in digital output codes between two successive sampling events should not exceed the maximum word length of the counter (i.e. 2^M). Otherwise, an overflow occurs which can be resolved by 2's complement subtraction as long as not more than one overflow occurs within T_s. In addition, the use of gray codes also ensures that the effect of possible overflow on the accuracy of generated counter codes is minimized.

4 Results

This chapter presents simulation results of the main blocks of DORSI in order to verify the system functionality and performance. The simulation setup is based on the proposed design of DORSI as described in chapter 3. The sensor is modelled with the equivalent lumped impedance model of the electrochemical cell model for neurochemical sensing in the brain as depicted in Figure 4.1. Detailed analysis of the cell impedance model is presented in section 3.2.1. The resistor values are selected based on measured voltage-current (V-I) data from novel diamond-like carbon (DLC) sensor electrodes for detection of dopamine. Thus, the required cell voltage V_{cell} range of 1.5 V (i.e. -0.7 V to 0.8 V) and desired cell current I_{cell} range determine the resistor values. The desired I_{cell} range depends on the expected concentration of dopamine and electrode sensitivity as discussed earlier in sections 2.2.2 and 3.1. Hence, the resistor values are selected to support a current range of 1.2 μA. As a result, the working electrode (WE) is selected as 1.25 MΩ since this is where the redox reaction occurs while the counter (CE) and reference (RE) electrodes are selected as 10 kΩ for minimal effect on the stability of V_{cell}. This implies that, the simulation setup of DORSI is designed to support a current range of -560 nA to 640 nA which can be extended or reduced by adjusting the WE resistance and the reference current E_I_{ref} accordingly. The reference current E_I_{ref} is set to 750 nA for all the simulation results presented in this section.

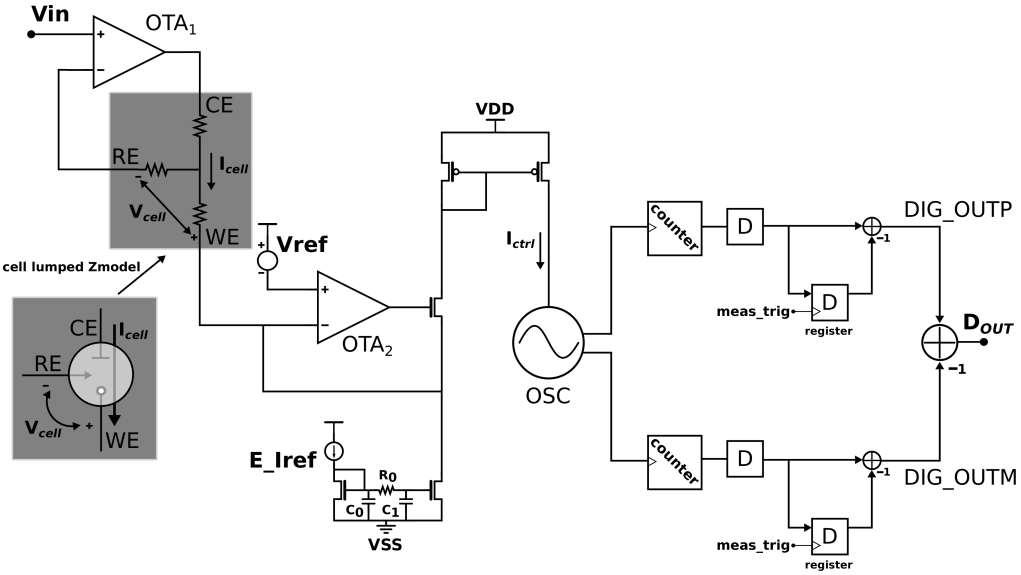


Figure 4.1: Simulation setup of DORSI.

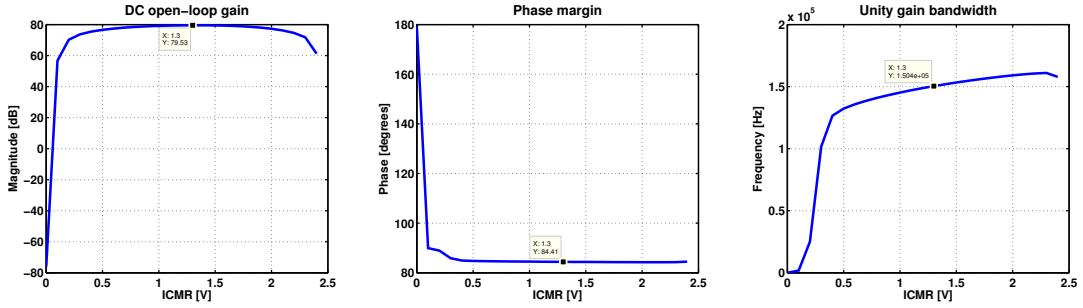
The design of DORSI is implemented in a 65 nm CMOS technology and simulation results related to the analog front end and the digital signal processing (DSP) block are presented in the next sections. Finally, post-layout simulation of the whole readout circuit is presented in order to verify the overall performance of the proposed micro-system as a biomedical readout circuit for detection of oxidation and reduction peaks corresponding to release and up-take of dopamine in the brain.

4.1 Performance of the analog front-end

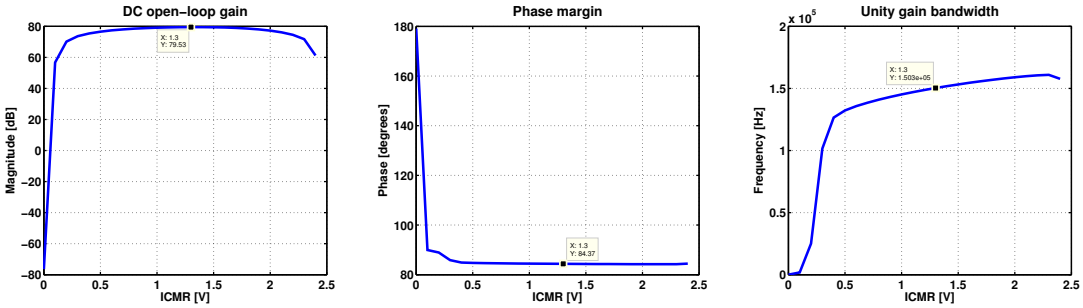
Simulation results presented in this section are related to the current acquisition (IA) and current-to-frequency (I-F) stages of the sensor signal processing. Hence, the performance of the analog front-end is based on two main components namely, the operational transconductance amplifier (OTA) and the oscillator (OSC). These components and related circuits are designed using Cadence Virtuoso IC design tool and their performance is simulated and evaluated with Mentor Graphics Eldo and Ezwave tools. In addition, process corner and monte-carlo simulations are setup and analysed using Mentor Graphics ICanalyst tool for the following temperatures -40 ^{o}C, 27 ^{o}C, 37 ^{o}C and 85 ^{o}C.

4.1.1 Performance of the Operational Transconductance Amplifier

Simulation results related to the selected miller N-OTA architecture and the overall performance of the IA block are presented in this section based on the simulation setup described in Figure 4.1. The main frequency characteristics of the OTA are presented in Figure 4.2 which also shows comparison between the pre-layout and post-layout performance of the OTA. Figures 4.2a and 4.2b show that good component matching is achieved as the post-layout results are as accurate as the pre-layout results. In addition, the results show that the OTA has good loop stability and settling response as a result of the obtained phase margin of 84^o. The achieved gain of 80 dB across the required input voltage range ensures stability of the cell voltage.



(a) Pre-layout performance of the miller N-OTA.

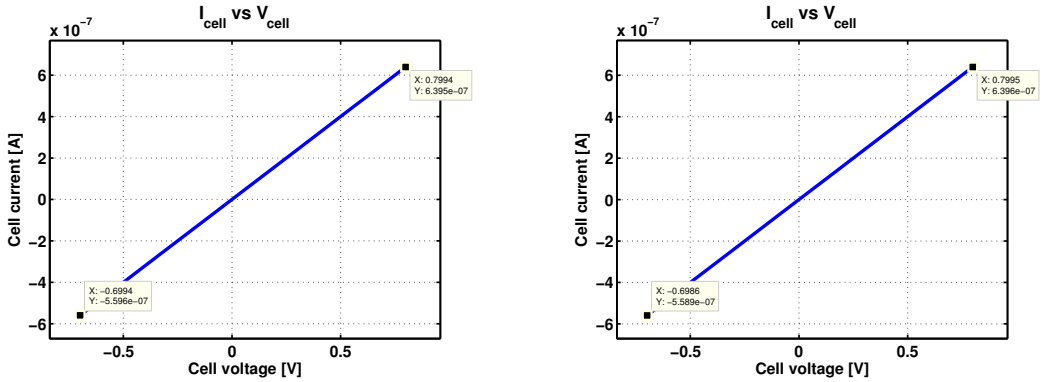


(b) Post-layout performance of the miller N-OTA.

Figure 4.2: Comparison of pre-layout and post-layout performance of the OTA.

The achieved gain bandwidth of 150 kHz is also sufficient for this application given the signal bandwidth of the redox current signals which is between 100 Hz and 10 kHz. Hence, the performance of the selected miller N-OTA architecture meets the required specifications of high gain, good stability, low power consumption, good CMRR and PSRR, wide input and output range as summarized in Table 4.1.

Next, the performance of the IA block in terms of control of the cell voltage and acquisition of the cell current are presented in the following figures. The cell voltage V_{cell} is defined based on equation 3.1 which is the difference between the input voltage V_{in} and the reference voltage V_{ref}. The cell current I_{cell} is defined by V_{cell} and the working electrode resistance R_{WE}. Figure 4.3 shows the relationship between the cell voltage and acquired cell current I_{cell} at supply voltages 2.5 V and 1.8 V. The results presented in Figures 4.3a and 4.3b show that the IA block of DORSI is capable of providing stable V_{cell} also at supply voltage of 1.8 V while maintaining the same current range of −560 nA to 640 nA as obtained at 2.5 V.

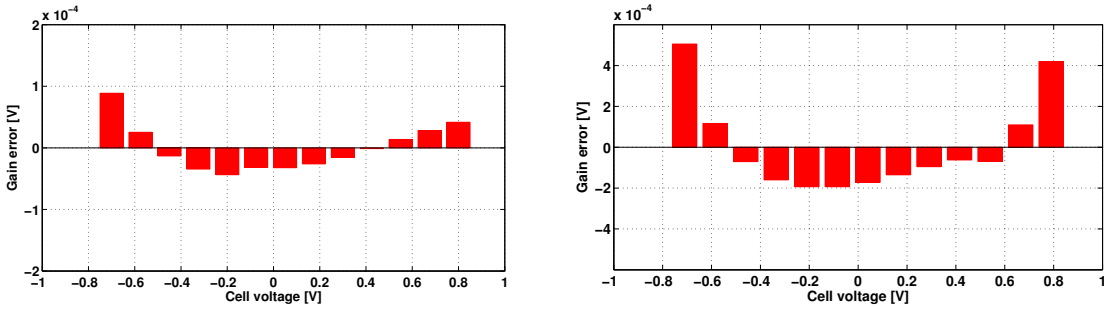


(a) $V_{dd} = 2.5$ V, $R_{WE} = 1.25$ MΩ (b) $V_{dd} = 1.8$ V, $R_{WE} = 1.25$ MΩ

Figure 4.3: Post-layout simulation of V_{cell} - I_{cell} relationship and stability.

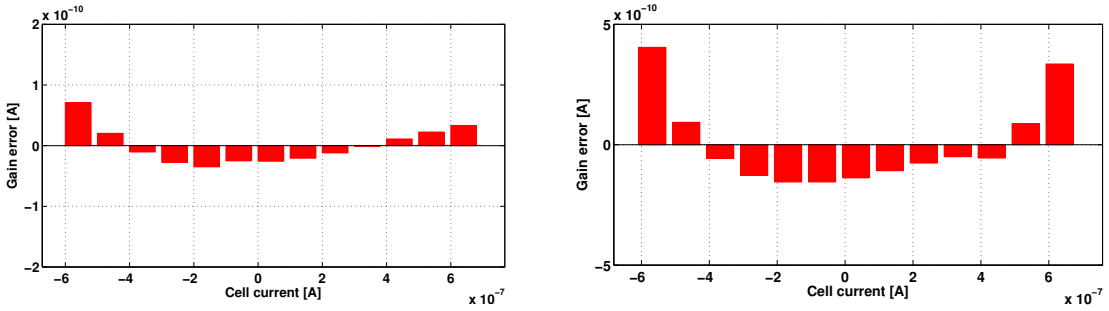
Although, the cell current and cell voltage relationship presented in Figure 4.3 is stable and linear, the effect of gain error can be observed from the data points highlighted on Figures 4.3a and 4.3b. Hence, the following Figures 4.4 and 4.5 present the voltage and current gain error across the required V_{cell} and I_{cell} range respectively. Figures 4.4a and 4.4b show the deviation in cell voltage from the required V_{cell} range of −0.7 V to 0.8 V when the supply voltage is set to 2.5 V and 1.8 V respectively. The cell voltage gain error is higher at the extremes of the V_{cell} range due to decrease in the gain of OTA1 as the input voltage approaches V_{dd} and ground voltage V_{ss}. The cell voltage gain error is also higher when the supply voltage is set to 1.8 V than at 2.5 V due to lower gain at lower input voltage range given the required 1.5 V range. Similarly, Figures 4.5a and 4.5b show deviation in cell current from the required I_{cell} range of −560 nA to 640 nA when the supply voltage is set to 2.5 V and 1.8 V respectively. The cell current gain error is also higher at the extremes of the I_{cell} range and when the supply voltage is set to 1.8 V due to the same reasons as described for the cell voltage gain error.

Furthermore, the effect of high working electrode resistance is simulated in order to measure the performance of DORSI in the presence of additional contact



(a) $V_{dd} = 2.5$ V (b) $V_{dd} = 1.8$ V

Figure 4.4: Post-layout simulation of V_{cell} gain error.



(a) $V_{dd} = 2.5$ V (b) $V_{dd} = 1.8$ V

Figure 4.5: Post-layout simulation of I_{cell} gain error.

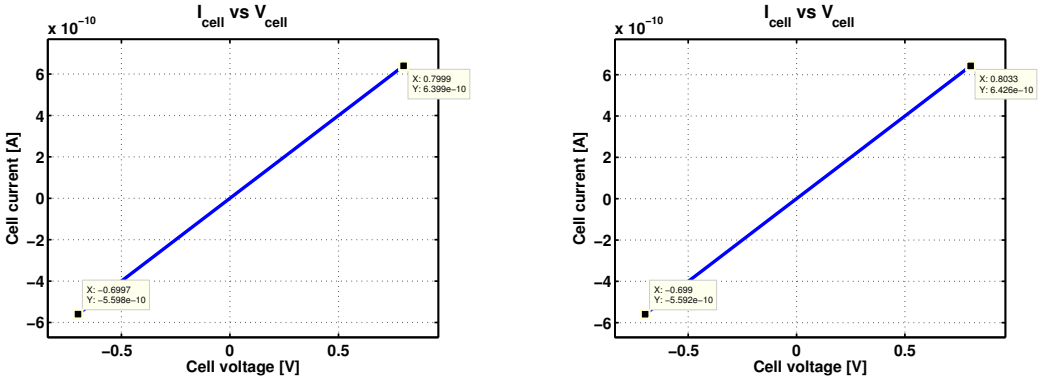
impedance at the sensor interface. Figures 4.6a and 4.6b show that the IA block is still capable of providing stable cell voltage across the required range of -0.7 V to 0.8 V at both 2.5 V and 1.8 V supply voltages. However, increase in WE resistance leads to decrease in the acquired cell current range due to the inverse relationship between the I_{cell} and R_{WE} as presented in Equation (4.1).

$$I_{cell} = \frac{V_{cell}}{R_{WE}} = \frac{V_{ref} - V_{in}}{R_{WE}} \tag{4.1}$$

Hence, the cell current range observed in Figure 4.6 is 1.2 nA compared to 1.2 μA range in Figure 4.3. The decrease in the I_{cell} range is as a result of increase in WE resistance from 1.25 MΩ to 1.25 GΩ.

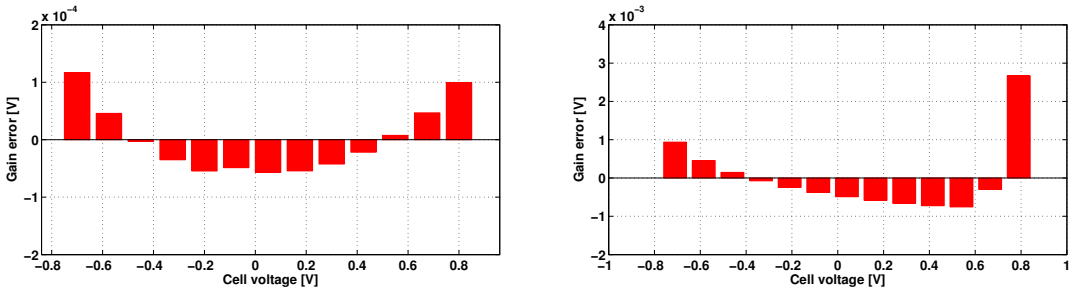
Figures 4.7 and 4.8 present the voltage and current gain error across the required V_{cell} and I_{cell} range for WE resistance of 1.25 GΩ. As with the gain errors presented in Figures 4.4 and 4.5 for WE resistance of 1.25 MΩ, the cell voltage and current gain error observed in Figures 4.7 and 4.8 are also higher at the extremes of the V_{cell} and I_{cell} range respectively. In addition, the gain errors shown in Figures 4.7 and 4.8 are also higher when the supply voltage is set to 1.8 V compared to at 2.5 V due to the same reasons as described earlier due to reduced gain at lower and upper limits of the input voltage range.

[6]Note: simulation results based on post-layout simulation



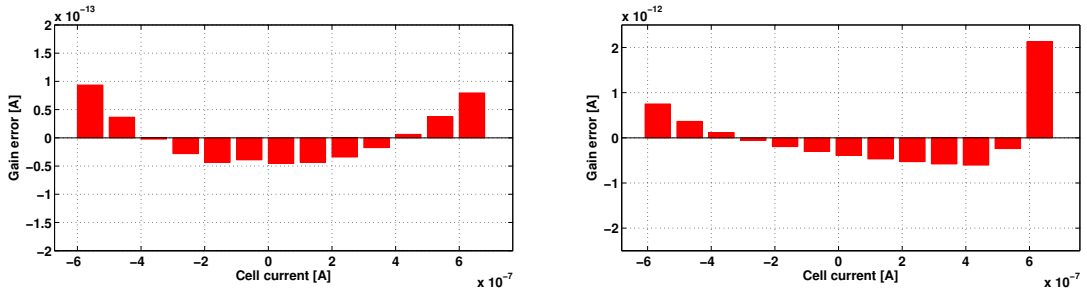
(a) $V_{dd} = 2.5$ V, $R_{WE} = 1.25$ GΩ (b) $V_{dd} = 1.8$ V, $R_{WE} = 1.25$ GΩ

Figure 4.6: Effect of high R_{WE} on V_{cell} - I_{cell} relationship and stability. [6]



(a) $V_{dd} = 2.5$ V (b) $V_{dd} = 1.8$ V

Figure 4.7: Effect of high R_{WE} on V_{cell} gain error.



(a) $V_{dd} = 2.5$ V (b) $V_{dd} = 1.8$ V

Figure 4.8: Effect of high R_{WE} on I_{cell} gain error.

Finally, the power consumption of the IA block is presented which includes contributions from both OTA1 and OTA2, reference current E_I_{ref} as well as the current-conveyor transistors leading to the I-F block. Figure 4.9 shows the power consumption of the IA block with respect to the cell voltage V_{cell}. The cell voltage serves as the control voltage for the whole system which is defined by the applied input voltage V_{in} of OTA1 and the reference voltage V_{ref} of OTA2. Hence, the power consumption of the IA block can be further reduced by optimizing the OTA to consume less current or using a different topology for the IA stage that uses a single OTA.

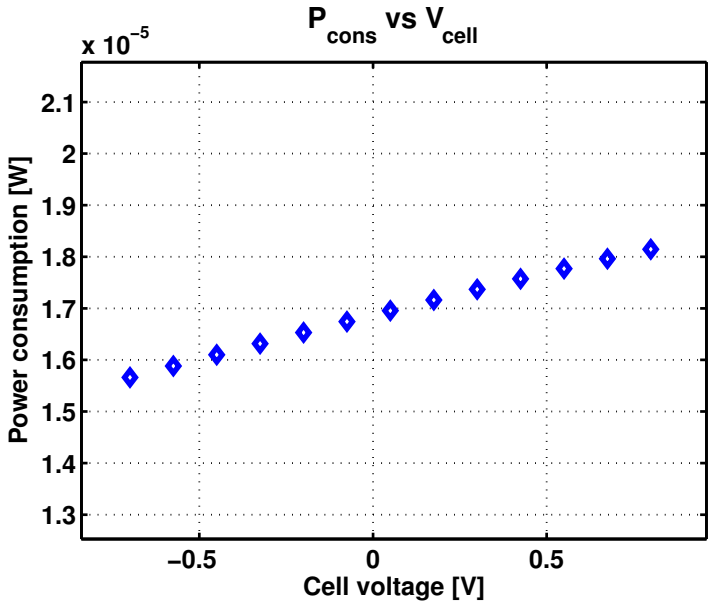


Figure 4.9: Post-layout simulation of power consumption of the IA block.

Other performance results related to the design of the Miller N-OTA based on post-layout simulations are presented in Table 4.1. The simulation setups used in extracting the values in Table 4.1 are based on simulation and measurement techniques presented in [64] and [57].

Table 4.1: Performance summary of the miller N-OTA & IA block

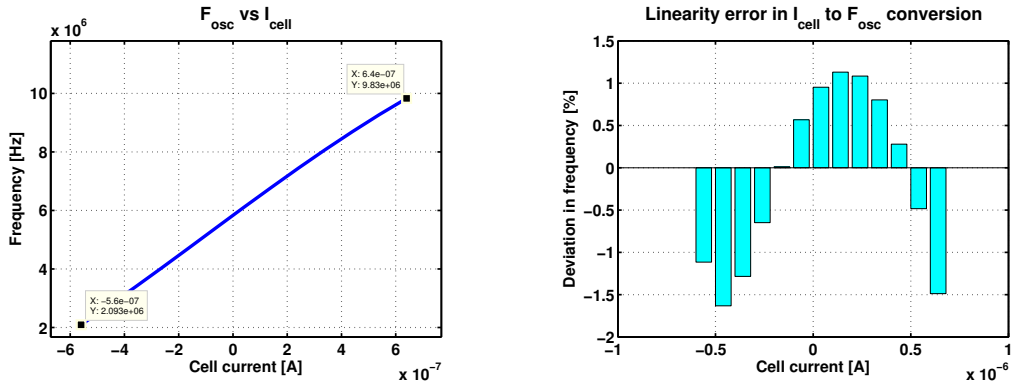
Design parameters	**Simulated results** (2.5V supply, $C_L = 5p$F)
DC open-loop gain	$80dB$
Phase, Gain margin	84.4^o, $34dB$
Unity gain bandwidth (GBW)	$150kHz$
ICMR	$0.2V$ to $2.4V$
Output voltage range	10μV to $2.49V$
DC offset	$4.2mV$
Output impedance	253Ω
CMRR [x]	$95dB$, @$100Hz$ $90dB$, @$100kHz$
PSRR +/−	$67dB$ / $76dB$
Slew rate, settling time	$0.24V/\mu$s, 10μs
Rise time, fall time	7.7μs, 14.9μs
Spectral noise voltage density [xi]	$684n\text{V}/\sqrt{Hz}$, @$1kHz$ $186n\text{V}/\sqrt{Hz}$, @$100kHz$
Power supply bias current	1μA
Power, current consumption [xii] - single OTA ($V_{dd} = 1.8V$) - single OTA ($V_{dd} = 2.5V$)	 5.35μW, 2.95μA 7.55μW, 3μA
Power, current consumption (IA) [xiii] - whole IA block ($V_{dd} = 1.8V$) - whole IA block ($V_{dd} = 2.5V$)	 11.95μW, 6.64μA 16.87μW, 6.75μA

[x] [xi] OTA output voltage noise values referred to input [xii] [xiii] values at V_{icm} midrange

4.1.2 Performance of the single-ended oscillator

Simulation results related to the performance of the single-ended oscillator (SE-CCO) are presented in this section based on the simulation setup described in Figure 4.1. The main goal for providing the results related to the SE-CCO is to be able to draw comparison with the performance of the differential oscillator which is implemented on-chip. The cell current obtained from the IA stage for the configuration shown in Figure 4.3a is used for the simulation results presented in this section. Figures 4.10a - 4.12 provide results related to I-F sensitivity, linearity, power consumption and phase noise performance of the SE-CCO. Figure 4.10a shows that the SE-CCO achieves frequency range of 8 MHz corresponding to the required and acquired cell current range (1.2 μA) which translates to I-F sensitivity of 6.7 kHz/nA.

In addition, the rate of change of F_{osc} with respect to the I_{ctrl} that is observed from Figure 4.10a appears to be relatively linear which supports the analysis presented in section 3.2.2 with reference to Equation (3.12). However, close examination of the accuracy of the I-F conversion is required in order to draw a more realistic conclusion. As a result, Figure 4.10b presents the linearity error in the I-F conversion across the I_{cell} range. The obtained linearity performance shows that the I-F conversion is affected by possible non-idealities in the oscillator. The effect of non-linearity in the I-F conversion is more significant as the frequency increases and directly visible in the digital codes obtained from the ID block. Simulation results related to this observation are later presented in Figures 4.15 and 4.23.

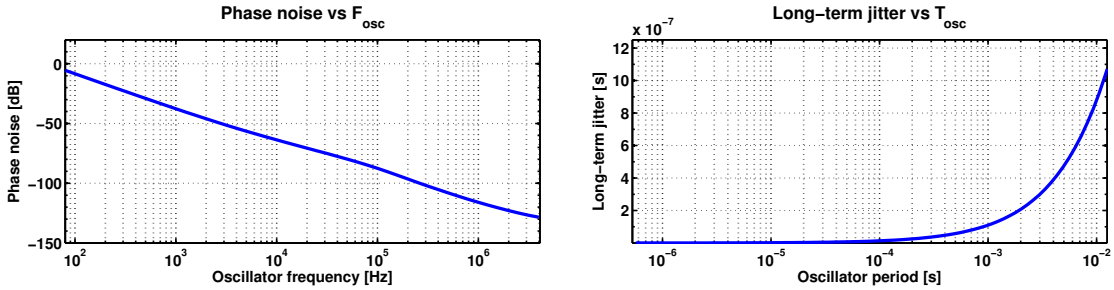


(a) Current-to-frequency (I-F) simulation. (b) Linearity error simulation.

Figure 4.10: I-F performance of the single-ended oscillator (SE-CCO).

The phase noise performance of the SE-CCO is presented in Figure 4.11a with respect to the oscillator frequency F_{osc} range. It should be noted that only one-side of the phase noise spectrum is presented in Figure 4.11a. Thus, the actual frequency range of the oscillator is twice the F_{osc} range shown in Figure 4.11a. In addition, the long-term jitter of the SE-CCO is extracted from the phase noise simulation in order to examine the relative timing error with respect to the oscillator period T_{osc}. Figure 4.11b presents the long-term jitter performance of the SE-CCO. As a result, Figures 4.11a and 4.11b show that most of the phase noise at lower oscillator frequencies and jitter at longer oscillator periods are dominated by contributions from flicker

($\frac{1}{f}$) noise. In addition, Figure 4.11b shows that the long-term jitter increases as



(a) Phase noise simulation. (b) Long-term jitter simulation.

Figure 4.11: Phase noise and jitter performance of the SE-CCO.

the T_{osc} increases. However, the relative timing error (i.e. ratio of long-term jitter to T_{osc}) decreases as oscillator period increases. Hence, the relative timing error at T_{osc} of 10 ms (i.e. actual $F_{osc} = 200$ Hz) is about $\pm 0.01\%$. On the other hand, the obtained period jitter of 0.192 ns at the maximum oscillator frequency of 10 MHz represents $\pm 0.096\%$ of the corresponding oscillator period of the SE-CCO.

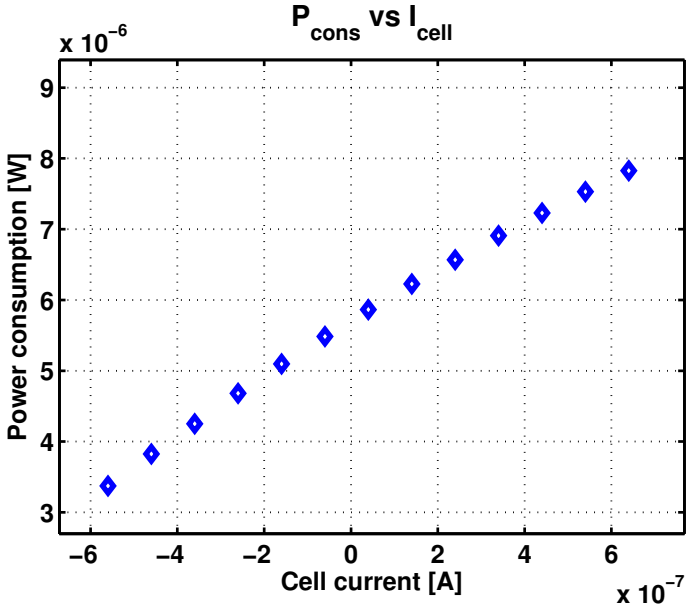


Figure 4.12: Power consumption of the SE-CCO.

The power consumption of the SE-CCO is shown in figure 4.12 with respect to the I_{cell} range. Other performance results related to the design of the single-ended oscillator are presented in Table 4.2. It should be noted that the RMS jitter given in Table 4.2 represents jitter of the oscillator as non-correlated random noise while period jitter refers to cumulative noise from cycle-to-cycle of the oscillator output. In addition, the frequency jitter of 148 Hz represents the output reduced frequency deviation due to current noise. Thus, the attained I-F sensitivity compared to the frequency jitter ensures that the required current resolution of 1 nA is achieved.

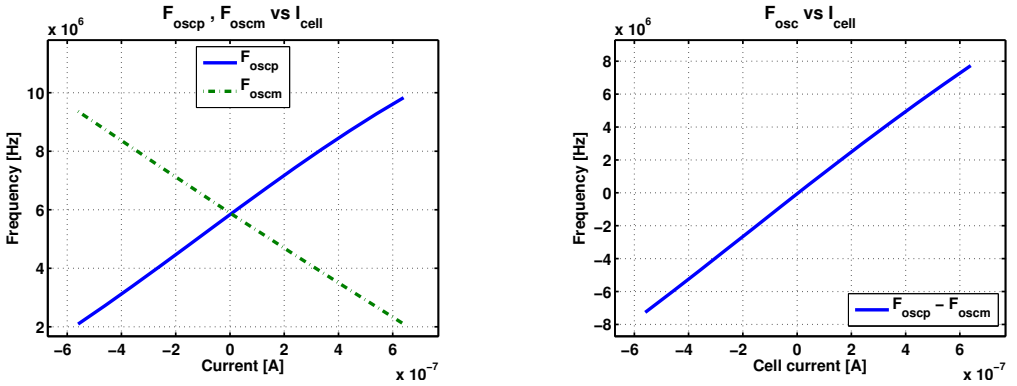
Table 4.2: Performance summary of the single-ended oscillator (SE-CCO)

Design parameters	**Simulated results** (1.0V supply, $I_{cell} = 1.2\mu$A)
Frequency range	$8MHz$
I-F sensitivity	$6.83kHz/nA$
Jitter (period, frequency)	$0.192ns$, $148Hz$
RMS jitter	$4.8ps$
RMS current noise	$119.44pA$
Noise floor	0.44pA$/\sqrt{Hz}$ [xiv]
Vdd sensitivity	$1.958kHz/mV$
Power, current consumption [xv]	5.71μW, 5.7μA

[xiv] value referred to input [xv] values at V_{icm} midrange

4.1.3 Performance of the differential oscillator

Simulation results related to the performance of the differential oscillator (DIFF-CCO) are presented in this section based on the simulation setup described in Figure 4.1. The cell current obtained from the IA stage for the configuration shown in Figure 4.3a is used for the simulation results presented in this section. First, the I-F sensitivity of the DIFF-CCO to the cell current from the IA stage is examined in Figures 4.13a and 4.13b. Then, the linearity performance of the DIFF-CCO is presented in Figure 4.14. Finally, the phase noise performance and power consumption of the DIFF-CCO are presented in Figures 4.16 and 4.17 respectively.



(a) OSC_OUTP and OSC_OUTM. (b) $OSC\_OUTP - OSC\_OUTM$.

Figure 4.13: I-F performance of the differential oscillator (DIFF-CCO).

Figure 4.13a presents the I-F transfer characteristics of each output of the DIFF-CCO which shows the effect of mismatch between both oscillators. As a result, the frequency range of the negative oscillator is slightly lower ($\sim$ 500kHz) than that of the positive oscillator. Figure 4.13b shows that the frequency range of the DIFF-CCO is doubled as compared to each output of the DIFF-CCO. Each output of

the DIFF-CCO has a frequency range of $\sim$ 8MHz and the corresponding frequency range of the DIFF-CCO is 15.5 MHz. Hence, the I-F sensitivity of the current to frequency conversion is doubled (13 kHz/nA) when compared to that of the single-ended oscillator. In addition, the rate of change of F_{osc} with respect to the I_{ctrl} that is observed from Figure 4.13b appears to be relatively linear which supports the analysis presented in section 3.2.2 with reference to Equation (3.12). Figure 4.13a also shows that the negative output of the oscillator OSC_OUTM is more linear than the positive output OSC_OUTP. Thus, the linearity of the DIFF-CCO is slightly improved when the difference of both outputs is taken as shown in Figure 4.13b.

Next, the linearity performance of the DIFF-CCO is further examined as non-linearity in the I-F conversion limits the dynamic performance of the whole system. Linearity error in the I-F conversion of the DIFF-CCO across the I_{cell} range is presented in Figure 4.14. Figure 4.14 shows that the maximum linearity error of OSC_OUTP is about 1.5 times more than that of OSC_OUTM. Hence, the overall linearity error of the DIFF-CCO is slightly reduced by $\sim$ 0.5%. In addition,

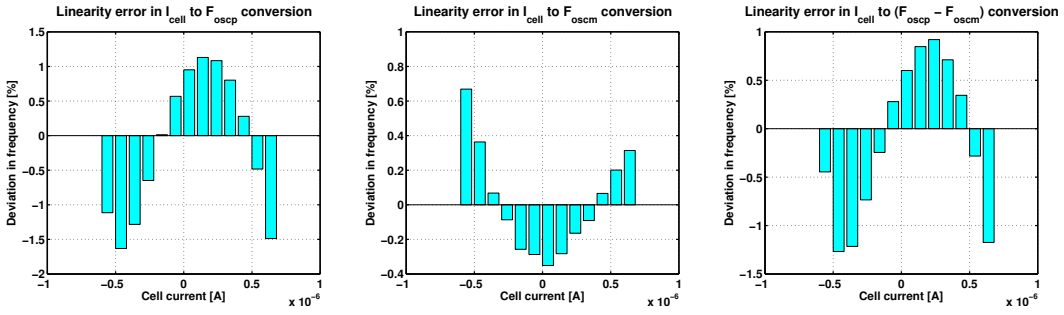
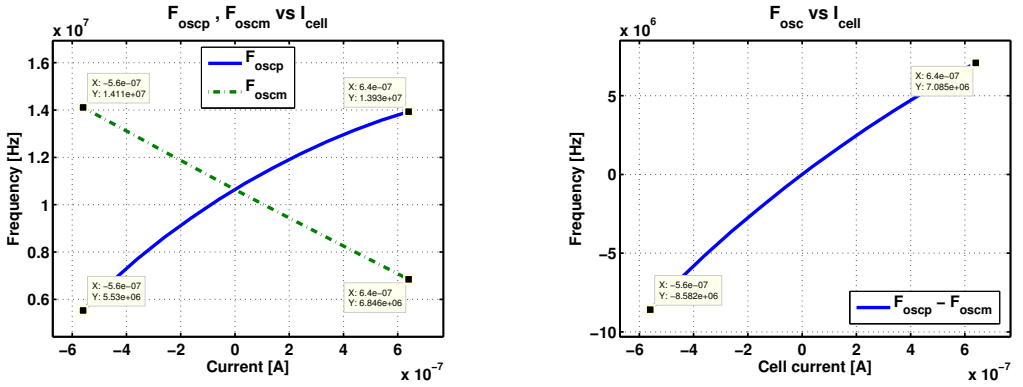


Figure 4.14: Linearity performance of the DIFF-CCO.

OSC_OUTM is about 1.5 times more sensitive to variations in supply voltage than OSC_OUTP due to a design flaw in the bias circuity of the OSC_OUTM branch of the differential oscillator. Hence, the V_{dd}-sensitivity of the DIFF-CCO is not as low as expected. Nonetheless, the achieved V_{dd}-sensitivity of the DIFF-CCO of 1.1 kHz/mV is still lower than that of the SE-CCO which is 1.96kHz/mV. Thus, conversion errors due to supply noise are not completely cancelled out but are slightly reduced when the difference of the digital outputs is taken in the ID stage. As a result, the overall PSRR and linearity performance of the DIFF-CCO can be improved by minimizing mismatch between each oscillator output.

Furthermore, the effect of increasing the oscillation frequency on the linearity performance of the DIFF-CCO is examined. The aim of the simulation presented in Figure 4.15 is to support the discussion in section 3.2.2 that increasing the oscillation frequency degrades the linearity of the I-F conversion. The I-F transfer curve becomes more non-linear as the frequency increases as observed from Figure 4.15 where the maximum frequency of each oscillator is around 14 MHz when compared to Figure 4.13 where the maximum frequency is $\sim$ 10MHz. As a result, the maximum frequency of 10 MHz defines the optimum frequency limit for the DIFF-CCO in order to prevent further degradation in the linearity performance of the A/D

conversion. In addition, an interesting observation is visible from Figures 4.15a and



(a) OSC_OUTP and OSC_OUTM. (b) $OSC\_OUTP - OSC\_OUTM$.

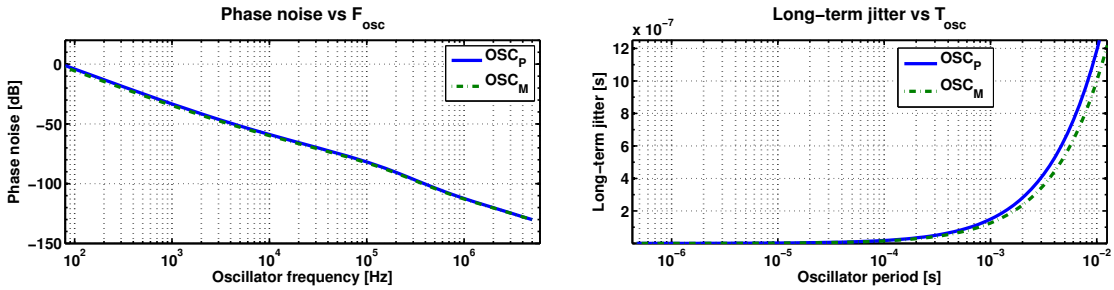
Figure 4.15: Effect of increasing F_{osc} on linearity of the I-F conversion.

4.13b which shows that the negative output OSC_OUTM still remains relatively linear despite the increase in the oscillation frequency. This result is even more interesting because this is the branch of the DIFF-CCO with the design-flaw. Further analysis is required during measurement of the chip in order to understand why the OSC_OUTM branch of the DIFF-CCO behaves this way. However, detailed investigation of this phenomena is left outside the scope of this thesis.

The phase noise performance of the DIFF-CCO is presented in Figure 4.16a with respect to the oscillator frequency F_{osc} range based on the optimum F_{osc} range of 10 MHz. It should be noted that only one-side of the phase noise spectrum is presented in Figure 4.16a. Thus, the actual frequency range of the oscillator is twice the F_{osc} range shown in Figure 4.16a. In addition, the long-term jitter of the DIFF-CCO is extracted from the phase noise simulation in order to examine the relative timing error with respect to the corresponding oscillator period T_{osc} range.

Figure 4.16b presents the long-term jitter performance of each output of the DIFF-CCO. As a result, Figures 4.16a and 4.16b show that the phase noise at lower oscillator frequencies and jitter at longer oscillator periods are dominated by contributions from flicker ($\frac{1}{f}$) noise. The phase noise of the DIFF-CCO at its maximum frequency is -130.16dB which is about 2 dB lower than the phase noise value of the SE-CCO at the same frequency. The phase noise of the DIFF-CCO is lower than that of the SE-CCO due to slightly lower RMS current noise, RMS jitter and phase error (i.e. jitter in radians). In addition, Figure 4.16b shows that the long-term jitter increases as the T_{osc} increases. However, the relative timing error (i.e. ratio of long-term jitter to T_{osc}) decreases as oscillator period increases. Hence, the relative timing error at T_{osc} of 10 ms (i.e. actual $F_{osc} = 200$ Hz) is about $\pm 0.01\%$. On the other hand, the period jitter of 0.196 ns at the maximum oscillator frequency of 10 MHz represents $\pm 0.098\%$ of the corresponding oscillator period of the SE-CCO. In addition, the power consumption of the DIFF-CCO is shown in figure 4.17 with respect to the I_{cell} range.

Other performance results related to the design of the differential oscillator based on post-layout simulations are presented in Table 4.3. It should be noted that the



(a) Phase noise simulation. (b) Long-term jitter simulation.

Figure 4.16: Phase noise and jitter performance of the DIFF-CCO.

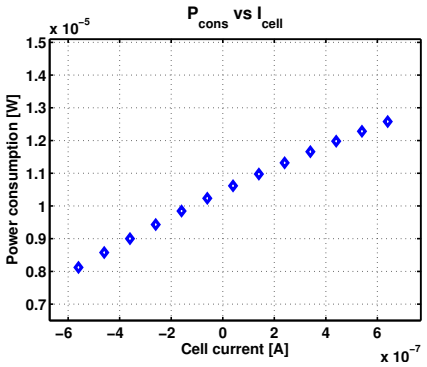


Figure 4.17: Power consumption of the DIFF-CCO.

RMS jitter given in Table 4.3 represents jitter of the oscillator as non-correlated random noise while period jitter refers to cumulative noise from cycle-to-cycle of the oscillator output. In addition, the frequency jitter of 142.8 Hz represents the output reduced frequency deviation due to current noise. Thus, the attained I-F sensitivity compared to the frequency jitter ensures that the required current resolution of 1 nA is also achieved when using the differential oscillator.

Table 4.3: Performance summary of the differential oscillator (DIFF-CCO)

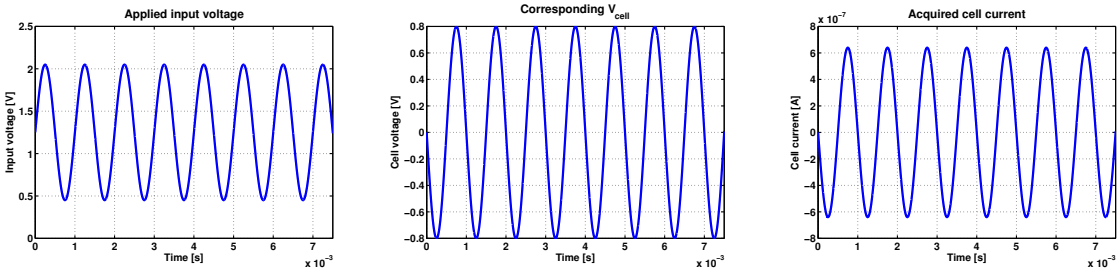
Design parameters	**Simulated results** (1.0V supply, $I_{cell} = 1.2\mu$A)
Frequency range	$15.5MHz$
I-F sensitivity	$13kHz/nA$
RMS Jitter $[F_o^+,\ F_o^-]$	$[4.655ps,\ 4.644ps]$
Jitter (period, frequency)	$0.196ns,\ 142.8Hz$
RMS current noise	$93.71pA$
Noise floor	$0.41\text{pA}/\sqrt{Hz}$ [xvi]
Vdd sensitivity	$1.1kHz/mV$
Power, current consumption [xvii]	10.5μW, 10.46μA

[xvi] value referred to input [xvii] values at V_{icm} midrange

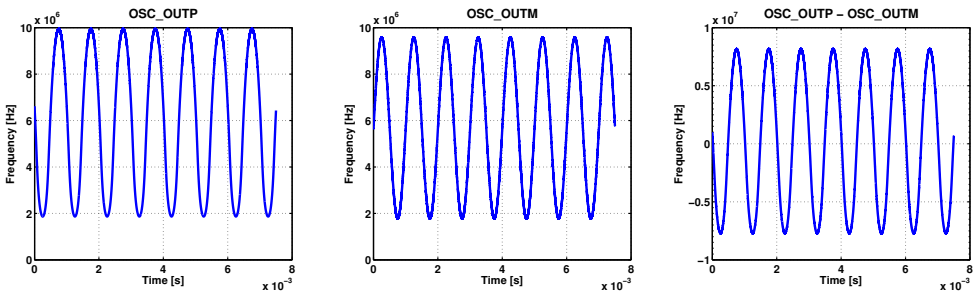
4.2 Performance of the digital signal processing block

Simulation results presented in this section are related to the current discretization (ID) stage of the sensor signal processing. Hence, the performance of the DSP block is based on the conversion of changes in the frequency of the oscillators in the I-F stage to digital output codes. The components of the digital block of DORSI are implemented in VHDL and their performance is simulated with Mentor Graphics Modelsim tool. Synthesis of the VHDL code was carried out using Synopsys Design Complier and layout of the ID block was designed using Cadence Encounter tool for place and route of the generated digital circuits.

The transient simulation setup for the verification of the digital block is described in Figure 4.18 based on the system diagram presented in Figure 4.1. Figure 4.18a shows the relationship between the defined input voltage V_{in} range (i.e. 1.25 V ± 0.8 V), corresponding V_{cell} range (±0.8 V) and detected cell current I_{cell} (±640 nA). Figure 4.18b presents the change in frequency at the output of the oscillators OSC_OUTP, OSC_OUTM and the difference between them. The peak-to-peak frequency range of the oscillators reflects the effect of the slightly wider I_{cell} range since the applied peak-to-peak V_{in} range is 1.6 V. Another observation from Figure 4.18b is that the difference between the oscillators results in twice the frequency range of a single oscillator output. However, the resulting frequency range is slightly non-uniform across the mid-frequency range. The non-uniform distribution is due to mismatch between the OSC_OUTP and OSC_OUTM oscillator frequencies which is visible in Figure 4.18b.



(a) V_{in}, V_{cell} and I_{cell} relationship.



(b) F_{oscp}, F_{oscm} and F_{oscp} - F_{oscm}.

Figure 4.18: Transient simulation setup for the DSP analysis.

Next, Figure 4.19 presents the digital codes generated from output of the ID block based on the simulation setup presented in Figure 4.18. Figure 4.19 shows that the conversion gain of the differential oscillator doubles based on the difference in the digital codes (i.e. DIG_OUTP - DIG_OUTM) when compared with digital output codes from each single-ended oscillator (i.e. DIG_OUTP, DIG_OUTM).

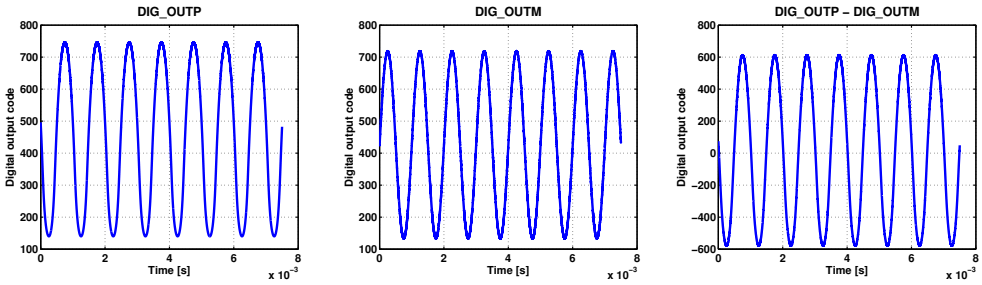
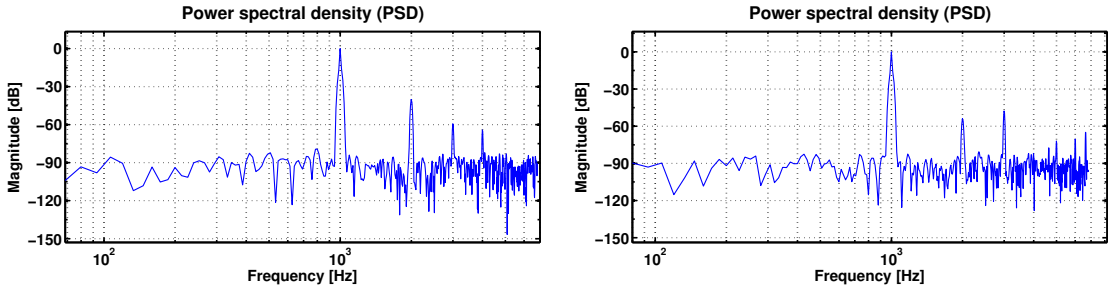


Figure 4.19: Performance of the frequency to digital code conversion.

The following simulation results in Figure 4.20 provide information about the dynamic performance of the A/D conversion with respect to noise and non-linearity of the system. The output power spectrum of the system is determined from the FFT analysis of the digital output codes. Hence, the FFT analysis of the digital codes generated from the single-ended and differential oscillators are presented in Figures 4.20a and 4.20b respectively. The FFT analysis is carried out based on the transient simulation setup described in Figure 4.18 where the input signal is at 1 kHz frequency. However, the simulation time is increased to 75 ms in order to extract more accurate results.



(a) SE-CCO based codes.

(b) DIFF-CCO based codes.

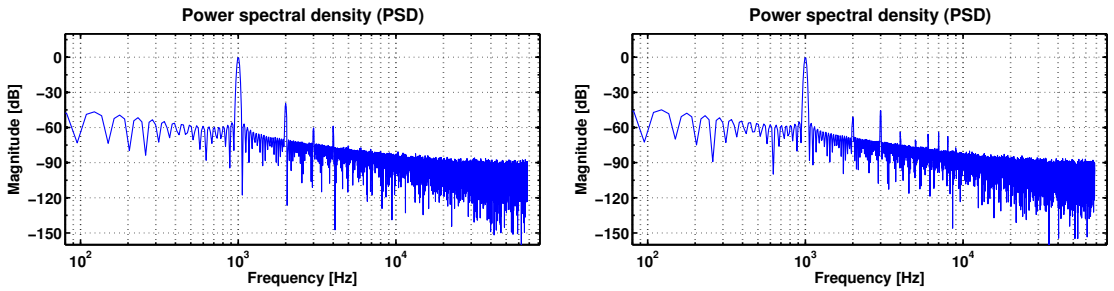
Figure 4.20: Dynamic performance of the ID block based on FFT analysis of the digital output codes with 1 kHz, ±0.8 V sine wave input, $T_{meas} = 75$ ms, $N_s = 10^3$.

The SNR extracted from simulation results presented in Figures 4.20a and 4.20b for the SE-CCO based codes and DIFF-CCO based codes is 80 dB and 82 dB respectively. However, Figures 4.20a and 4.20b also show that the SNDR of the single-ended digital codes is $\sim 40dB$ while that of the differential codes is $\sim 50dB$. The DIFF-CCO has higher SNDR than the SE-CCO due to lower linearity error in the current-to-frequency conversion. The difference between the SNDR and SNR performance of the SE-CCO and DIFF-CCO is due to the effect of harmonic distortion

as a result of non-linearity in the A/D conversion. The effect of the 2^{nd}-harmonic is dominant in the SE-CCO while the 3^{rd}-harmonic dominates the dynamic range of the DIFF-CCO. On the other hand, the 3^{rd}-harmonic of the SE-CCO and the 2^{nd}-harmonic of the DIFF-CCO are $\sim 60dB$. Hence, the ENOB of the ID block can be improved by designing the I-F stage so that the effect of the second and third order non-linearity present in the A/D conversion are cancelled or minimized.

In addition, it should be noted that the SNDR performance of the DIFF-CCO is comparable to results reported in literature for similar application [13]. Thus, the obtained SNDR of 50 dB from the DIFF-CCO provides absolute accuracy (ENOB) of 8-bit resolution. However, the digital output code resolution (n) is mainly determined by the measurement time T_{meas} and n increases as the T_{meas} increases. As a result, a measurement time of 7.5 ms generates about 10-bit digital code resolution as shown in the simulation results presented in Figures 4.19 and 4.22. This implies that around $12 \cdot 10^3$ digital code peak-to-peak range can be achieved by increasing the measurement time from 7.5 ms to 75 ms, which corresponds to higher code resolution of 13.3-bits. However, there is a limit to which increasing the measurement time improves the resolution which is defined by the current noise floor.

Furthermore, the number of samples used in the FFT analysis is increased from 1000 to 10^4 for the 75 ms simulation by increasing the sampling rate Fs. Hence, the sampling interval Ts is reduced from 75 μs to 7.5 μs. The resulting output power spectrum is presented in Figure 4.21. The effect of decimation in the CIC-filter structure of the ID-block is observed in Figure 4.21 as high frequency components of the quantization noise are filtered. This is as a result of the inherent low-pass *sinc* characteristic of the implemented CIC-filter structure as earlier described in section 3.2.3. The visibility of the noise floor is also improved by increasing the number



(a) SE-CCO based codes. (b) DIFF-CCO based codes.

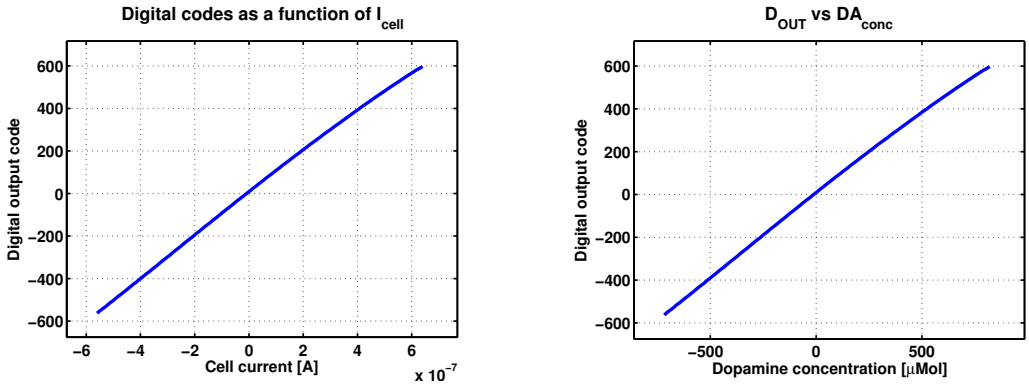
Figure 4.21: Dynamic performance of the ID block based on FFT analysis of the digital output codes with 1 kHz, ±0.8 V sine wave input, $T_{meas} = 75$ ms, $N_s = 10^4$.

of samples and the power spectral density (PSD) results are presented in Figures 4.21a and 4.21b for SE-CCO and DIFF-CCO respectively. As a result, it can be observed from both Figures 4.21a and 4.21b that wide-band quantization noise is suppressed below the noise floor when compared to typical delta-sigma ADC output noise spectrum. In addition, higher SNR performance of $\sim 86dB$ and $\sim 88dB$ are extracted from PSD results in Figures 4.21a and 4.21b for SE-CCO and DIFF-CCO respectively compared to previous values extracted from Figures 4.20a and 4.20b due

to better visibility of the noise floor. The 6 dB increase in the SNR performance is due to the effect of the noise-averaging process of the integrate, decimate and differentiate structure of the ID block. Hence, the digital code resolution (n) of the system is improved by 1-bit, which results in 14-bit and 14.3-bit resolution for the SE-CCO and DIFF-CCO based codes respectively.

However, the effect of harmonic distortion on the resolution of the system still remains visible in Figure 4.21. Thus, the effect of non-linearity in the A/D conversion dominates the dynamic performance of the system. As a result, good linearity is just as important as achieving high sensitivity in oscillator-based A/D converters. On the other hand, achieving good current-to-frequency linearity performance from oscillators is quite challenging due to possible non-linear dependence between the control current I_{ctrl} and oscillation frequency F_{osc} as discussed earlier in section 3.2.2. Hence, one way to further reduce linearity errors is to design the oscillator to operate at lower frequency F_{osc} by increasing the length of the inverter transistors and lowering the bias current of the oscillator O_I_{ref}. However, this improvement is achieved at the expense of increasing the measurement time required to extract enough samples for the A/D conversion in order to achieve good signal quality. Alternatively, calibration techniques can be applied to improve the linearity of the A/D conversion, which in turn improves the dynamic performance of the system.

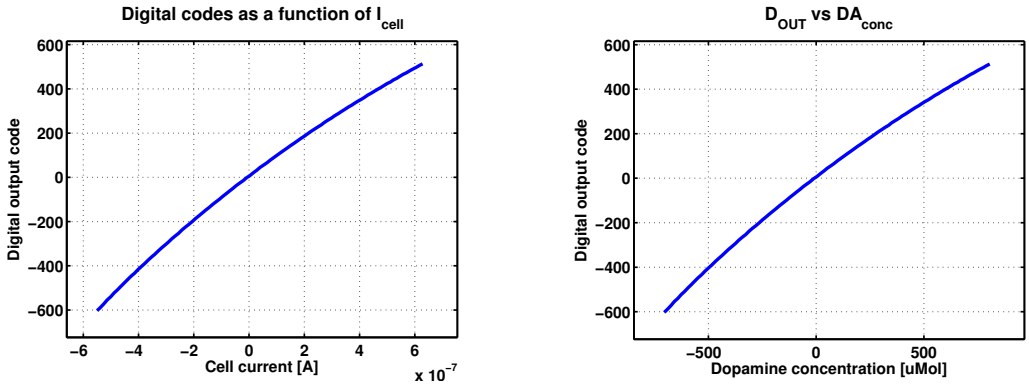
The following Figures 4.22a and 4.22b describe the relationship between the generated digital codes and the acquired cell current as well as the corresponding dopamine concentration DA_{conc}. Both figures are based on 7.5 ms simulation and digital codes extracted from the output of the DIFF-CCO. However, increasing the measurement time to 75 ms results in 10 times the digital output code range presented in Figures 4.22a and 4.22b for the same I_{cell} and DA_{conc} range. Hence, current sensitivity of $\sim$ 100 pA/LSB and dopamine sensitivity of 128.2 nMol/LSB is obtained. It should be noted that 0 μMol dopamine concentration in Figure 4.22b refers to the reference dopamine concentration level from which oxidation and reduction of dopamine occur.



(a) I_{cell} range = 1.2μA. (b) DA_{conc} range = 1.5mMol.

Figure 4.22: Digital output codes from the ID block with respect to detected cell current I_{cell} and corresponding dopamine concentration (DA_{conc}).

Finally, the effect of increasing the oscillation frequency on the linearity of the digital codes is examined. The aim of the simulation presented in Figure 4.23 is to support the discussion in section 3.2.2 that increasing the oscillation frequency degrades the linearity of the I-F conversion. The digital codes presented in Figure 4.23 are based on I-F simulations presented earlier in Figure 4.15. Figures 4.23a and 4.23b show that the current to digital code transfer curve becomes more non-linear as the frequency increases. This observation is based on the I-F simulation presented earlier in Figure 4.15 where the maximum frequency of each oscillator is around 14 MHz when compared to Figure 4.13 where the maximum frequency is $\sim$ 10 MHz. As a result, the maximum frequency of 10 MHz defines the optimum frequency limit for the I-F stage in order to prevent further degradation in the dynamic performance of the A/D conversion.

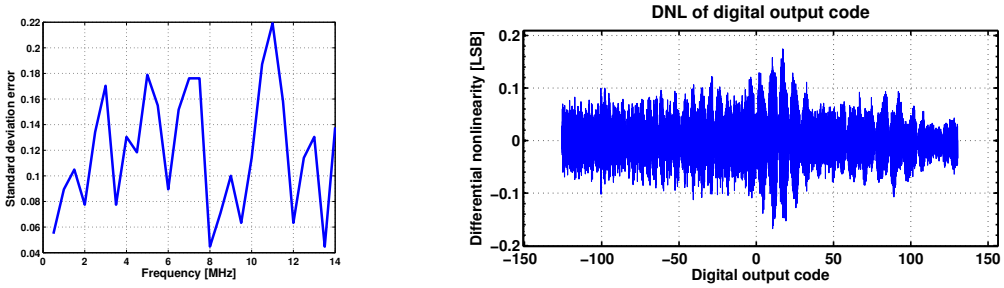


(a) I_{cell} range = 1.2μA. (b) DA_{conc} range = 1.5mMol.

Figure 4.23: Effect of increasing F_{osc} on linearity of the digital codes.

The current discretization block of DORSI is designed to be robust against possible errors due to possible metastability during the operation of the underlying digital circuits. As a result, inaccuracies emanating from possible metastability are minimized to 1 LSB change in the digital output code through the use of gray-encoding. In addition, higher sensitivity of the I-F block allows more samples to be generated for the defined cell current I_{cell} range. Hence, the effect of increase in number of samples N_s decreases the conversion error ΔC visible in the digital output codes from the ID block. Thus, the achieved high I-F sensitivity improves the digital code resolution of the system while reducing the required measurement time to attain the same resolution when compared with lower I-F sensitivity.

Furthermore, the conversion error due to RMS jitter from the DIFF-CCO is presented in Figure 4.24a. Figure 4.24a shows the RMS conversion error obtained at different oscillation frequencies based on the standard deviation error from the expected digital codes. Figure 4.24a also shows that the RMS conversion error is minimized to 0.18 LSB within the optimum F_{osc} range of 10 MHz which corresponds to maximum conversion rate of 10 MSps. In addition, it can be observed from Figure 4.24a that the conversion error increases as the oscillation frequency increases. This is due to the increase in the relative timing error of the oscillator as the oscillator period reduces, as discussed earlier in section 4.1.3 and presented in Figure 4.16.



(a) ΔC based on RMS jitter. (b) DNL of digital codes due to quantization noise.

Figure 4.24: Conversion error (ΔC) analysis of the ID block ($T_{meas} = 7.5ms$).

However, the conversion error in the ID block is dominated by quantization noise as the effect of jitter is minimized as the number of samples increases. Hence, the conversion error ΔC shown in Figure 4.24b represents the quantization error of the A/D conversion which is simulated as the differential nonlinearity (DNL) of the digital output codes. Figure 4.24b shows that the quantization error of the ID block is within ± 0.18 LSB. The accuracy of the quantization error obtained from the DNL of the digital codes increases as the number of points used in the simulation increases. As a result, Figure 4.24b is simulated based on the digital codes from Figure 4.22a but converted to 8-bit code range in order to improve the resolution of the DNL simulation. Alternatively, the measurement time can be increased in order to generate more points for higher code range of 10-bits or more.

Other performance results related to the design of the digital block based on post-layout simulations and sampling rate of 133.3 kHz are presented in Table 4.4. The achieved current sensitivity results in lower current resolution than the defined requirement of at least 1 nA. In addition, the achieved dopamine sensitivity ensures detection of lower dopamine concentration than the detection limit of the DLC test electrodes which is 10 μMol. Thus, DORSI can also be used with more sensitive dopamine sensors with better electrode sensitivity.

Table 4.4: Performance summary of the digital block

Design parameters	**Simulated results (SE-CCO based)**	**Simulated results (DIFF-CCO based)**
Signal-to-noise ratio (SNR)	$86dB$	$88dB$
Dynamic range (DR) [xviii]	$40dB$	$50dB$
Resolution (n)	14-bits	14.3-bits
ENOB	6.4-bits	8-bits
RMS conversion error [xix]	0.25 LSB	0.22 LSB
(within 10 MHz F_{osc} range)	0.22 LSB	0.18 LSB
Current resolution (LOD) [xx]	$\sim 120pA$	$\sim 100pA$
Power consumption	5.56μW	11.2μW

[xviii] Note: values based on SNDR performance of the ID block [xix] Note: values based on rms jitter of the I-F block as given in Tables 4.2 and 4.3 [xx] defines limit of detection

4.3 Post-layout simulation of the readout circuit

The simulation setup of the whole readout circuit is based on the measured data of the cell voltage and redox current (V_{cell} - I_{cell}) from the sensor electrodes which models the overall impedance of the sensor as a voltage controlled current source (VCCS) as illustrated in Figure 4.25. In addition, the readout sensor interface supports an optimum detectable current range of 1.2 μA($\pm$600 nA) but can be extended by varying the electrode bias current.

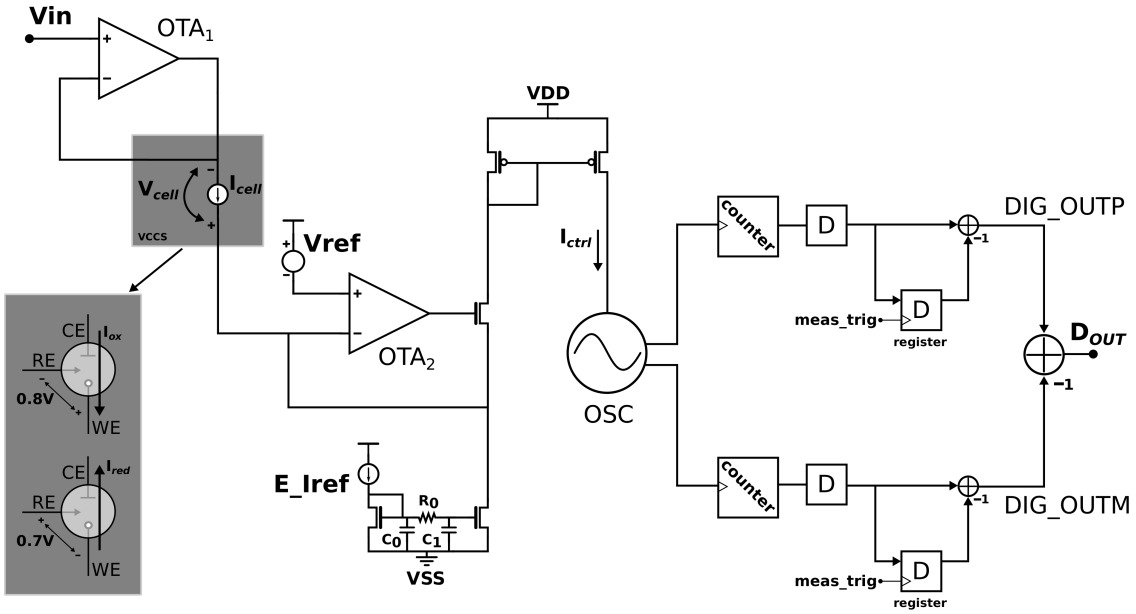
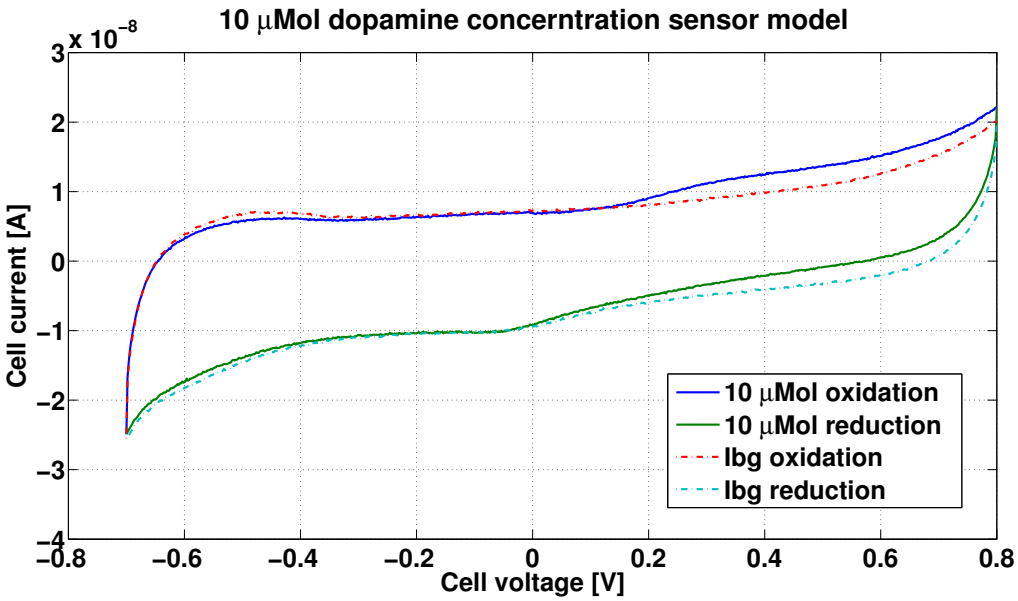
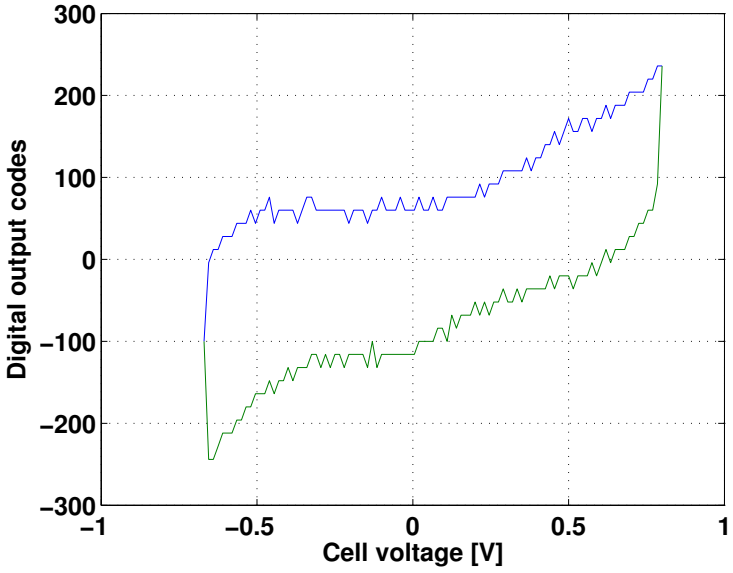


Figure 4.25: Simulation setup of DORSI with electrode data.

The simulation results presented in this section describe the detection of the oxidation and reduction cycles of dopamine as well as the corresponding digital codes extracted from the output of DORSI. Figures 4.26 and 4.27 are based on 10 μMol and 1 mMol of dopamine concentration respectively. Hence, Figures 4.26a and 4.27a present the detected cell current I_{cell} due to the presence of dopamine as well as detected background current I_{bg}. It is important to note that the background current is measured before dopamine is added. Thus, the difference between I_{cell} and I_{bg} reflects the oxidation and reduction peaks. In addition, the corresponding cell voltages at which these peaks occur can be extracted from the cyclic voltammetry results in Figures 4.26 and 4.27. Similarly, the obtained results from the output of DORSI show good correlation between the detected cell current and the extracted digital output codes as presented in Figures 4.26b and 4.27b for 10 μMol and 1 mMol of dopamine respectively. Hence, the oxidation and reduction peaks of dopamine are also visible from the digital code representation of the detected cell current. Although, longer measurement time is required to generate more samples or points to be able to provide smoother curves, the achieved results show that DORSI is capable of detecting the oxidation and reduction cycles of dopamine.

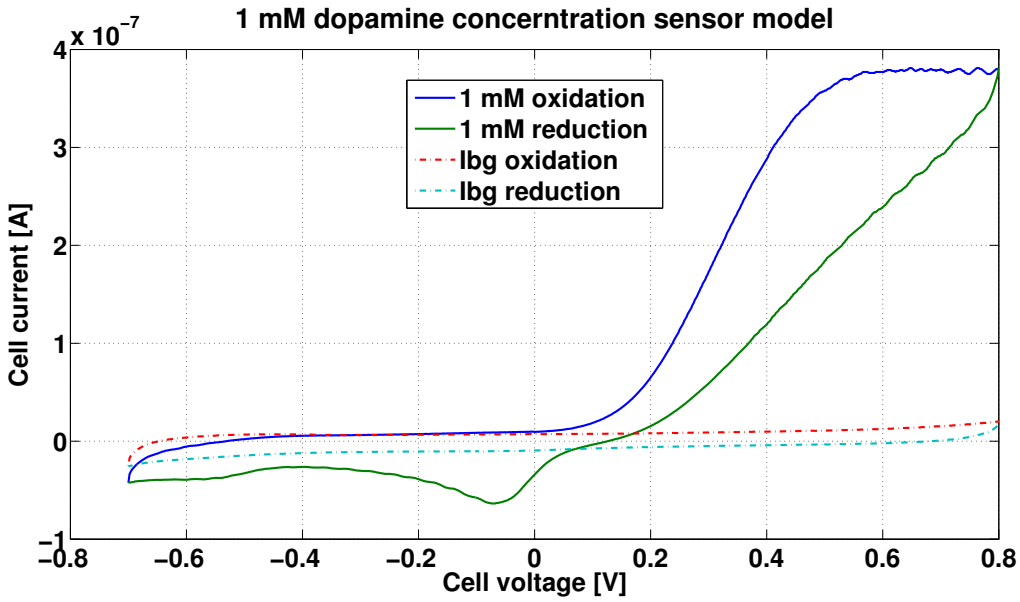


(a) Background current (I_{bg}) and I_{cell} from 10 μMol of dopamine

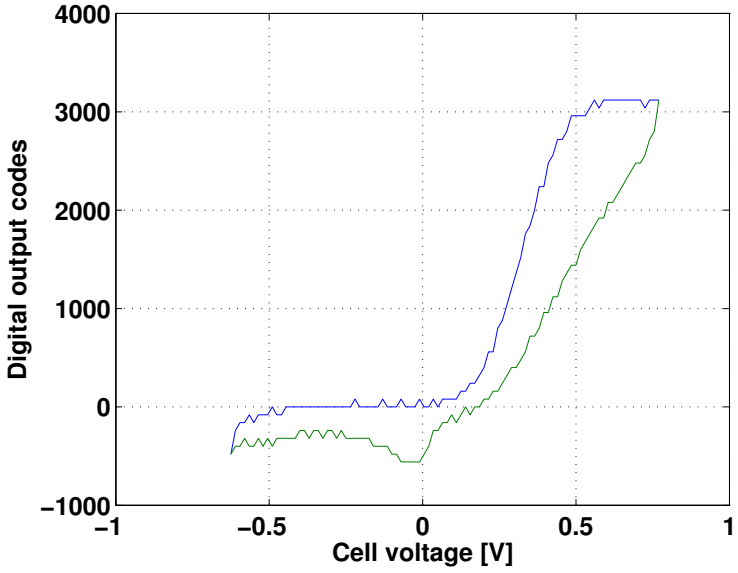


(b) Corresponding digital output codes

Figure 4.26: Simulation of detected current and generated digital codes in the presence of 10 μMol of dopamine based on measurement data from the sensor.



(a) Background current (I_{bg}) and I_{cell} from 1 mMol of dopamine



(b) Corresponding digital output codes

Figure 4.27: Simulation of detected current and generated digital codes in the presence of 1 mMol of dopamine based on measurement data from the sensor.

5 Conclusion

The outcome of this thesis is a micro-system in a 65 nm CMOS technology for detection of dopamine in the brain. The proposed design of the dopamine oxidation read-out sensor interface results in a mixed-signal front-end architecture by integrating both analog and digital circuits for minimizing noise and high resolution of detected current signals. The analog front-end is designed for acquisition and amplification of current signals resulting from oxidation and reduction at the biosensor electrodes in the brain. The digital signal processing (DSP) block is used for discretization of detected dopamine oxidation and reduction current signals that can be further processed by an external system. Hence, the resulting micro-system from this thesis can be described as an integrated potentiostat for detection of dopamine.

The analog front-end is based on a transimpedance architecture that comprises mainly of two operational transconductance amplifiers (OTA) and a differential oscillator for initial detection of dopamine current signals and conversion of detected current signals to digital signals. The performance of the analog front-end shows that the selected OTA design provides high gain of 80 dB which ensures good stability and control of the voltage over the sensor, good loop stability due to the achieved phase margin of 84^o and low power consumption of 5.4 μW. The performance of differential oscillator shows that the sensitivity of the current to frequency (I-F) conversion is doubled when compared to that of the single-ended oscillator. As a result, high resolution of < 1 nA detectable current from the analog front-end is achieved due to high I-F sensitivity (13 kHz/nA). In addition, the analog front-end supports wide current range of 1.2 μA($\pm$600 nA) with RMS current noise of 93.7 pA which results in an SNR of 82 dB from the analog signal processing.

The digital front-end architecture is based on digital signal processing principle of integration and decimation of sampled pulses which averages out noise over the measurement time. The integration and decimation blocks are implemented with a 16-bit gray counter and 16-bit registers at each output of the differential oscillator. The use of the gray counter implies that each bit is encoded as a gray code and ensures that the minimum error due to possible metastability is limited to 1 LSB which makes the system more robust and error-tolerant. The digital front-end also includes a 32-bit parallel to serial interface for buffering the gray encoded bits at the output of the whole system. The performance of the DSP block shows sufficient dynamic range for this application due to the attained resolution of 14.3-bit and obtained RMS conversion error of 0.18 LSB over the desired current range. Thus, the effect of digital averaging technique improves the SNR performance of the system by 6 dB as a result of reduced contributions from thermal and quantization noise. However, the attained ENOB is 8-bits due to the effect of non-linearity in the current to frequency conversion.

Other results related to the performance of DORSI are summarized in Table 5.1 where comparison between operating DORSI in single-ended and differential modes are presented. The signal bandwidth used in calculating the figure of merits (FOM) related to conversion efficiency of the system is 10 kHz based on the knowledge of action potentials occurring typically between 100 Hz and 10 kHz [18]. In ad-

dition, the results presented in Table 5.1 show that DORSI offers better current and dopamine sensitivity based on the differential oscillator structure as opposed to using the single-ended oscillator structure. Although, both approaches provide good sensitivity performance for use in this application, the single-ended structure may be more favourable due to lower power consumption. On the other hand, the differential structure is more energy efficient in terms of conversion efficiency, when compared with the single-ended structure. This is as a result of higher ENOB and dynamic range of the differential structure. Thus, the use of differential oscillator based A/D conversion structure in DORSI provides good performance and with further improvements, looks promising for the detection of dopamine from the brain.

Table 5.1: Performance summary of DORSI

Design parameters	**Simulated results (SE-CCO based)**	**Simulated results (DIFF-CCO based)**
Current sensitivity	$120p$A/LSB	$100p$A/LSB [xxi]
Dopamine sensitivity	$153.8n$Mol/LSB	$128.2n$Mol/LSB [xxii]
Total power consumption Total current consumption	28.1μW, 23.2μW (IA @$1.8V$) 18.02μA	38.6μW, 33.7μW (IA @$1.8V$) 28.4μA
FOM1 $\left(\frac{P_{cons}}{2BW * 2^{ENOB}}\right)$	(16.6, 13.7) pJ/conversion	(7.5, 6.6) pJ/conversion
FOM2 $\left(\frac{P_{cons}}{BW * 10^{\frac{DR}{20}}}\right)$	(28.1, 23.1) pW/Hz	(12.2, 10.7) pW/Hz

[xxi] [xxii] values calculated based on measurement time of $75ms$ and electrode sensitivity of $0.78nA/\mu$Mol of dopamine concentration.

In summary, the readout of dopamine from the brain helps to provide insight into more effective treatments for patients suffering from neurological disorders. Furthermore, the identification of dopamine oxidation and reduction current peaks and corresponding reaction potentials from the sensor interface can be used in future developments to provide a feedback solution that offers possibility to control the stimulation of dopamine based on the current dopamine level of the patient. The detected oxidation and reduction peak potentials help to regulate the voltage applied by neurostimulation electrodes when used in the feedback system for sensing and stimulating dopamine in patients suffering from dopamine-deficient disorders such as Parkinson's disease. These systems are often described as closed-loop interfaces for recording, analysing and stimulating of dopamine and other neural signals in the brain [14], [49], [3]. The field of neurosensing and neurostimulation is an interesting and evolving area of research and offers wide range of opportunities to contribute to the advancement of technology and medicine as their energy-constrained and precision requirements necessitates constant research.

References

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A Available frequency bands for biomedical applications

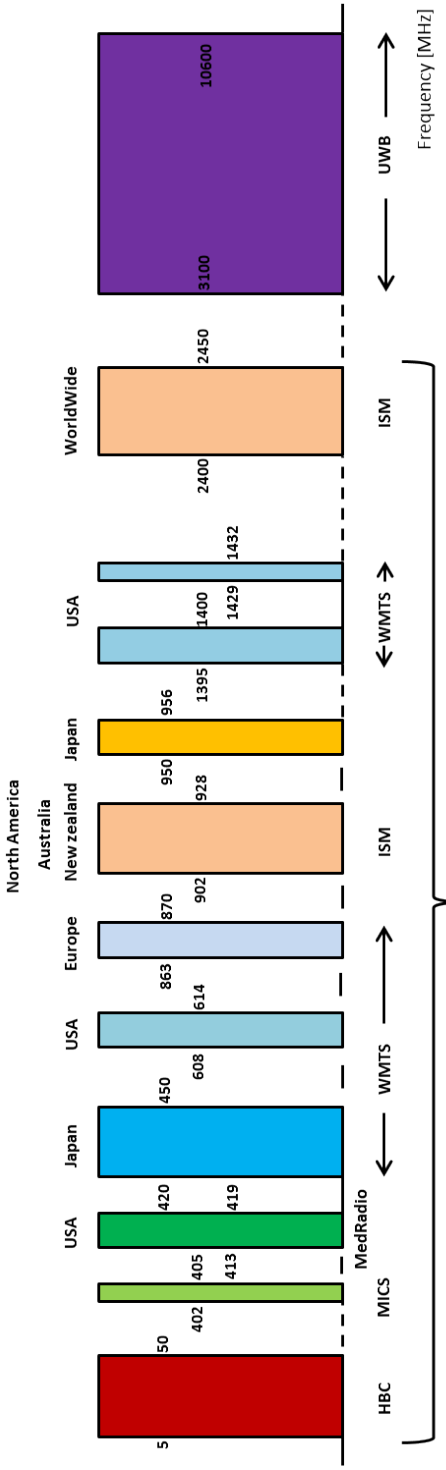


Figure A1: Available frequency bands for biomedical applications [11], [78], [79], [80]

B Layout implementation

The following diagrams describe the organization and implementation of DORSI layout. The layout of DORSI microchip is designed to fit a die-area of $1mm^2$ as a result of using 32 I/O bonding pad-ring. However, the actual area utilized by the main blocks of DORSI is much smaller as illustrated in the floorplan figure B2.

B.1 Hierarchical diagram of DORSI layout

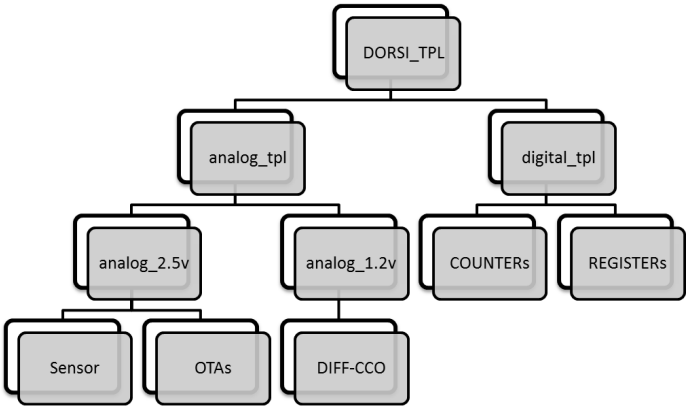


Figure B1: Hierarchical diagram describing the organization of DORSI

B.2 Floorplan diagram of DORSI layout

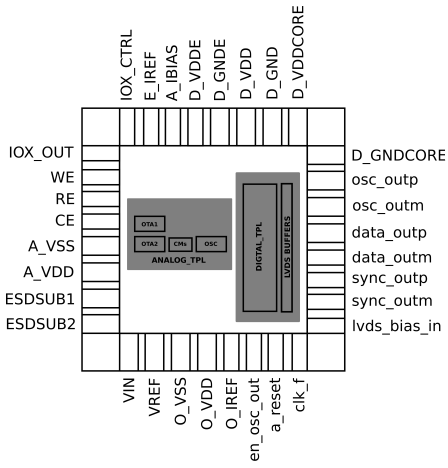


Figure B2: Floorplan diagram describing the arrangement of the I/O pins and placement of the main blocks of DORSI

B.3 Layout implementation of the OTA

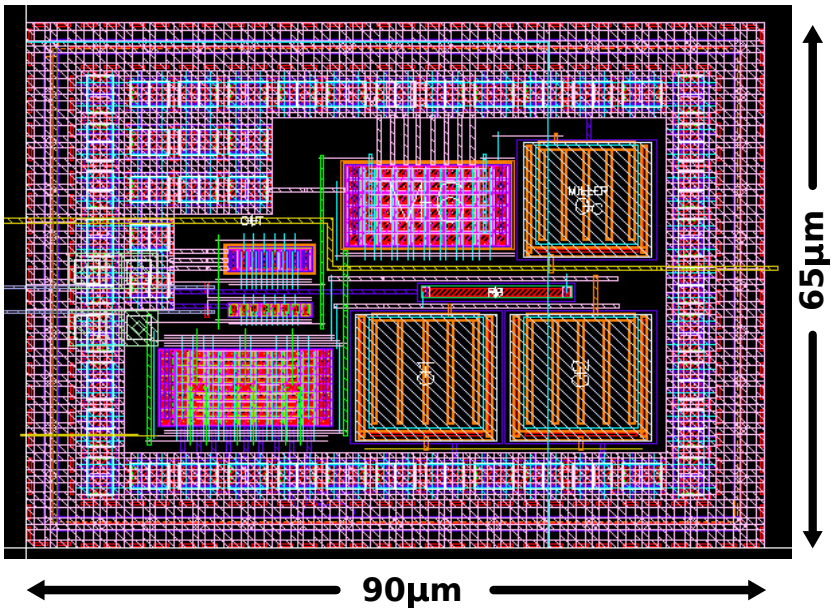


Figure B3: Layout of the miller N-OTA used in DORSI

B.4 Layout implementation of the differential oscillator

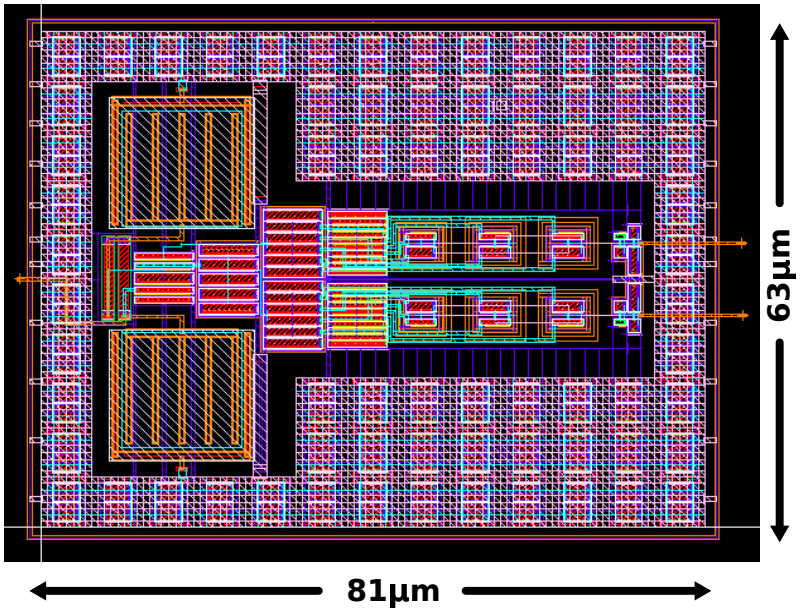


Figure B4: Layout of the differential current controlled oscillator (DIFF-CCO) used in DORSI

B.5 Layout implementation of the digital block

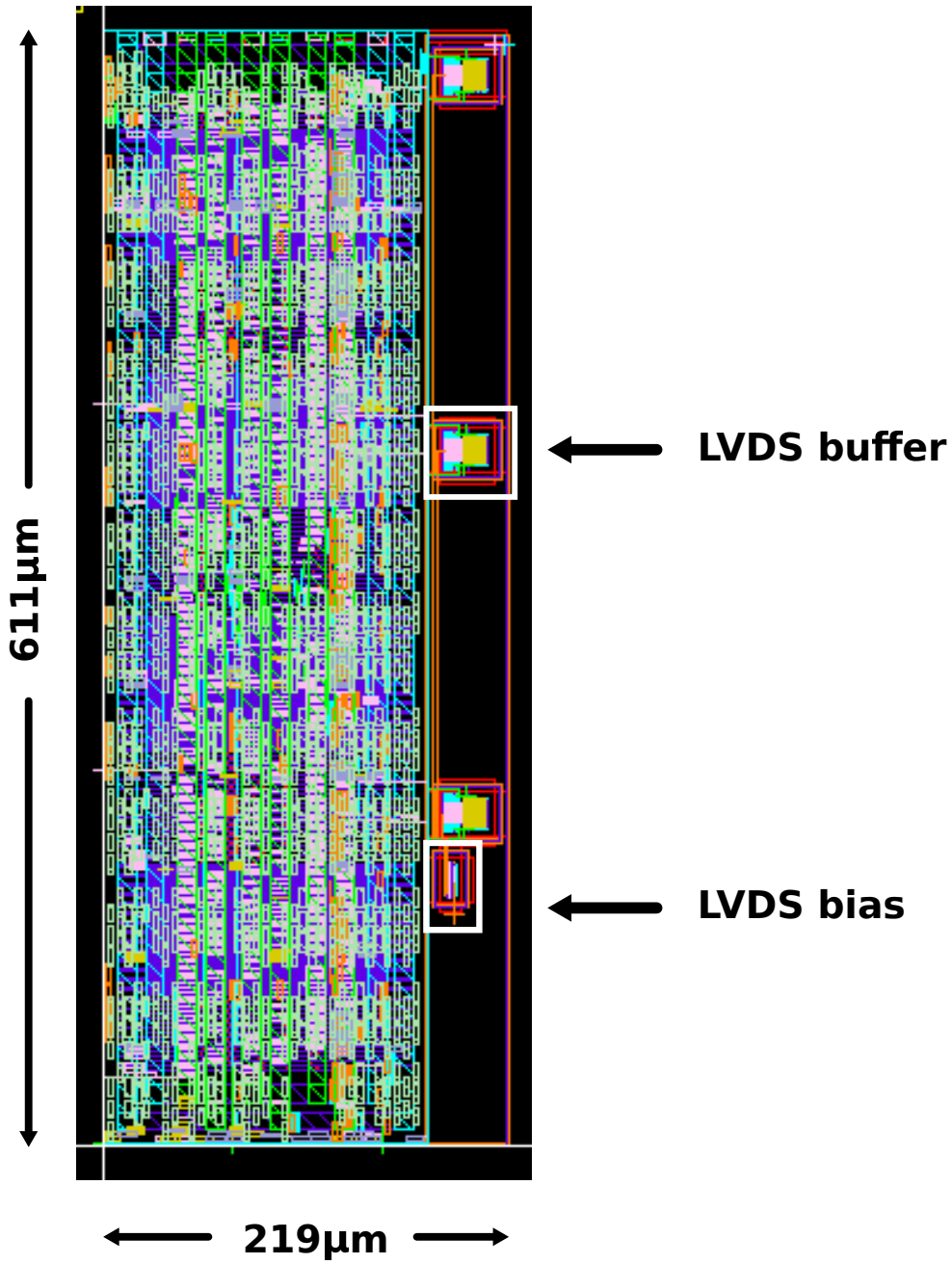


Figure B5: Layout of the digital signal processing (DSP) block used in DORSI with Low voltage differential signalling (LVDS) buffers for minimizing coupling of interferences from the digital outputs to the analog domain of the readout circuit.

B.5.1 Equivalent schematic of the digital block

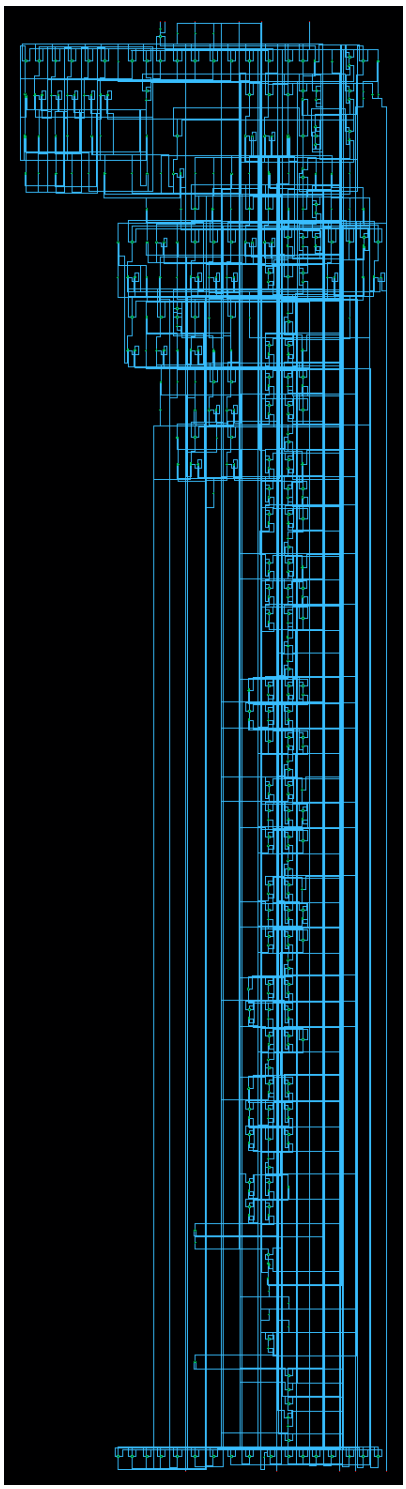


Figure B5.1: Equivalent schematic of the digital block implemented with VHDL

B.6 Layout implementation of DORSI

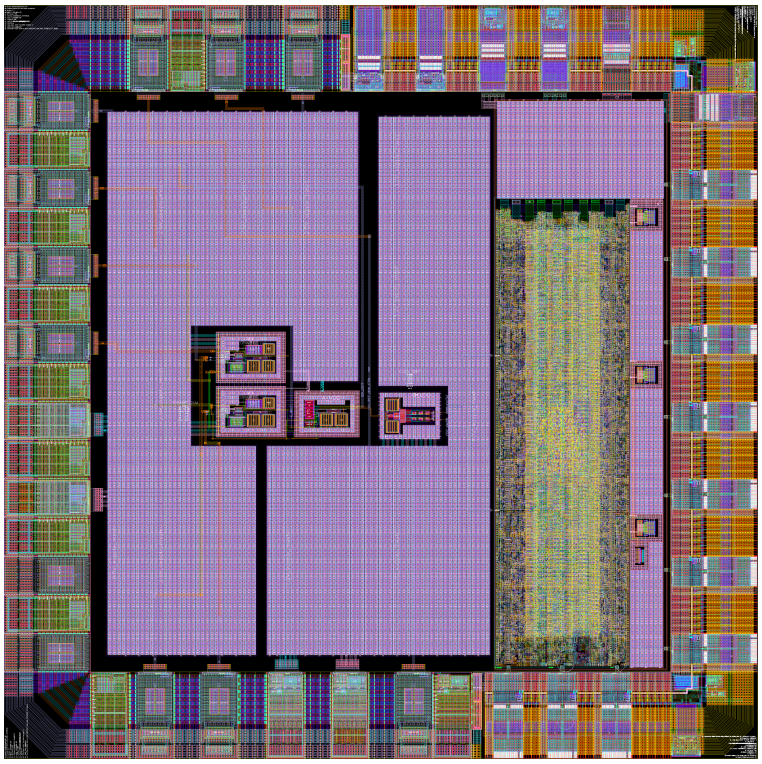
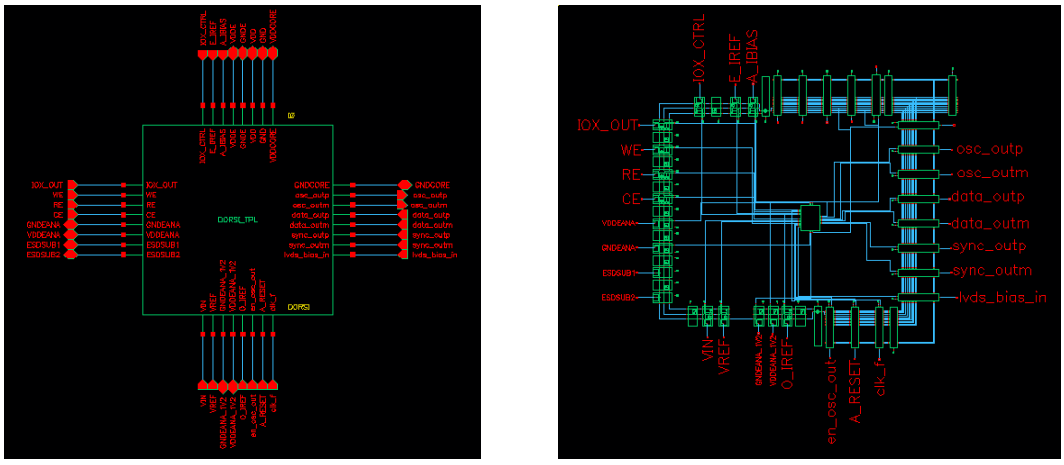


Figure B6: Layout of the top-level cell of DORSI with supply mesh cells visible

B.6.1 Equivalent schematic of DORSI layout



(a) Top cell schematic

(b) Internal schematic

Figure B6.1: Equivalent top level schematic of DORSI layout showing routing between the CORE and the bonding I/O pads

B.6.2 Layout and equivalent schematic of supply mesh cell

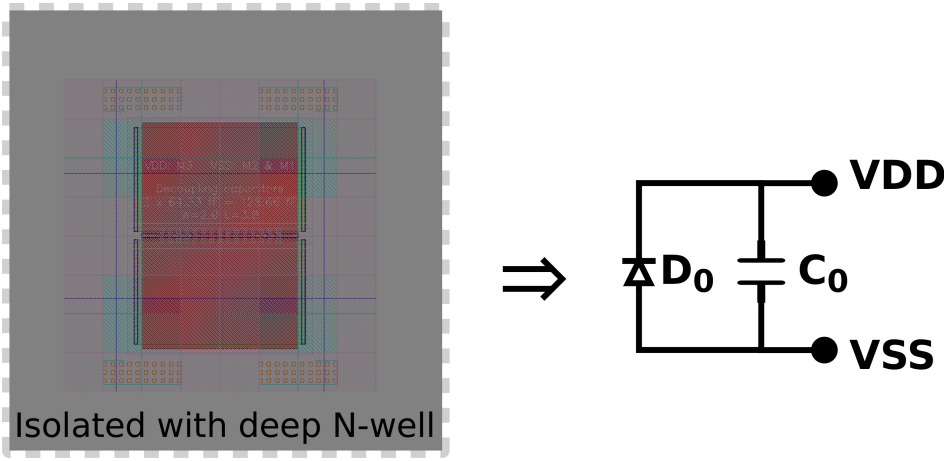


Figure B6.2: Layout and equivalent schematic of each supply mesh cell isolated with deep N-well (DNW) layer for reducing the effect of substrate noise and supply noise

B.6.3 Layout implementation of DORSI without supply mesh

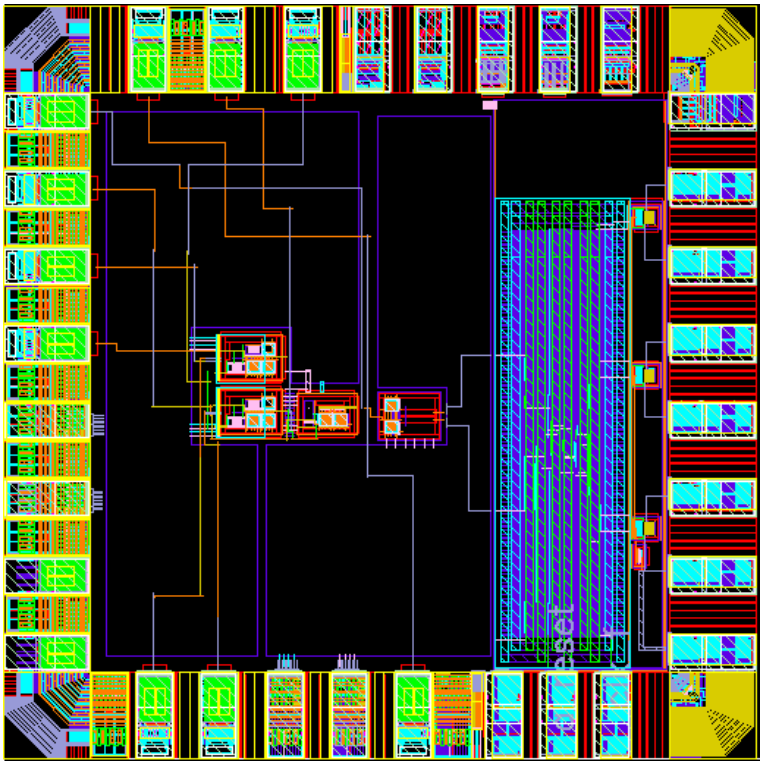


Figure B6.3: Layout snapshot of DORSI top-level cell without supply mesh cells

C Derivations related to sensitivity of the oscillator to variations in power supply

This section provides further analysis of the sensitivity of the oscillator to supply voltage based on the equations derived in section 3.2.2. The expression for oscillation frequency F_{osc} derived in Equation (3.8) is based on the assumption that output resistance ($R_o = \frac{V_{dd}}{ID}$). However, the expression for R_o is more complicated than the assumption made in Equation (3.8). Hence, the analysis in this section aims to reflect other dependencies than those presented in section 3.2.2.

The pull-up and pull-down transitions for rise and fall edges of the pulses from the oscillator output is based on the charging and discharging currents of each inverter stage. Hence, the following equation holds for the slope of each transition based on the drain current I_D, gate capacitance C_l and the output voltage v_{out} of each inverter stage [66].

$$\frac{\partial v_{out}}{\partial \tau} = \frac{I_D}{C_l} \tag{C1}$$

$$\Rightarrow v_{out} = \frac{I_D * \tau}{C_l}, \tau = \frac{C_l * v_{out}}{I_D} \tag{C2}$$

In addition, the period of the ring oscillator T_{osc} is defined by twice the time it takes for each transition to propagate around the ring. Hence, the propagation time (τ) represents the sum of the pull-up and pull-down transition times (τ_P, τ_N). The propagation time delay τ_d also depends on the toggle point of each transition as presented in Equation (C4). The toggle point of each transition defines the threshold crossing for each inverter stage (i.e. $v_{out} \sim \frac{V_{dd}}{2}$) [66]. Lastly, T_{osc} depends on the total propagation time delay τ_d and the number of inverter stages N within the oscillator ring. Thus, the frequency of the ring oscillator is defined as presented in Equation (C6).

$$\tau_d = (\tau_P + \tau_N),\ assume\ \tau_P \equiv \tau_N = \frac{C_l * V_{dd}}{2 * I_D} \tag{C3}$$

$$\tau_d = 2 * \tau_P = \frac{C_l * V_{dd}}{I_D} \tag{C4}$$

$$T_{osc} = N * \tau_d = \frac{N * C_l * V_{dd}}{I_D} \tag{C5}$$

$$\Rightarrow F_{osc} = \frac{1}{T_{osc}} = \frac{I_D}{N * C_l * V_{dd}} \tag{C6}$$

It is important to note that the pull-up and pull-down times may differ between inverter stages in reality. There may also be mismatch in the toggle points of each inverter stage as the inverter transistors move from saturation to linear region and vice-versa during each transition. Thus, the assumptions that τ_P is equivalent to τ_N and v_{out} is approximately $\frac{V_{dd}}{2}$, may contribute to the non-linearity of the oscillator.

Let's consider the inverter transistors controlling the oscillator when they are operating in linear region[64]:

$$I_{ds} = \beta \left\{ [(V_{gs} - V_{th}) * V_{ds}] - \frac{(V_{ds})^2}{2} \right\} * (1 + \lambda * V_{ds}) \tag{C7}$$

Ignoring the channel length modulation $(1+\lambda*V_{ds})$ and $\frac{(V_{ds})^2}{2}$ terms, Equation (C7) can be simplified as:

$$I_{ds} = \beta \left[(V_{gs} - V_{th}) * V_{ds} \right] \tag{C8}$$

$$\Rightarrow g_{ds} = \frac{\partial I_{ds}}{\partial V_{ds}} = \beta (V_{gs} - V_{th}) \tag{C9}$$

$$\Rightarrow R_{ds} = \frac{1}{\beta (V_{gs} - V_{th})},\ where\ \beta = \mu_0 C_{ox} \left(\frac{W}{L} \right) \tag{C10}$$

$$\therefore R_{ds} = \frac{L}{\mu_0 * C_{ox} * W (V_{gs} - V_{th})} \tag{C11}$$

Considering the PMOS current-starved transistors that serve as current sources for each inverter stage, the drain-source current flowing through each inverter stage can be expressed as Equation (C12) based on Equation (C8).

$$I_{ds} = \beta \left[(V_g - V_{dd} - V_{th}) * (V_d - V_{dd}) \right] \tag{C12}$$

Therefore, F_{osc} can be expressed as follows based on Equations (C6) and (C12).

$$F_{osc} = \frac{(\mu_0 * C_{ox} * W) * [(V_g - V_{dd} - V_{th}) * (V_d - V_{dd})]}{L * N * C_l * V_{dd}} \tag{C13}$$

Thus, the rate of change of the oscillation frequency to the change in supply voltage (i.e. V_{dd}-sensitivity of the oscillator) is given as:

$$\frac{\partial F_{osc}}{\partial V_{dd}} = \frac{(\mu_0 * C_{ox} * W) * [(V_{dd})^2 - (V_g * V_d) + (V_{th} * V_d)]}{L * N * C_l * (V_{dd})^2} \tag{C14}$$

In addition, Equation (C17) holds for the V_{dd}-sensitivity of the oscillator when the current source transistors are operating in saturation region, based on Equations (C15) and (C16).

$$I_{ds} = \frac{\beta}{2} \left[(V_g - V_{dd} - V_{th})^2 \right] \tag{C15}$$

$$F_{osc} = \frac{(\mu_0 * C_{ox} * W) * [(V_g - V_{dd} - V_{th})^2]}{2 * L * N * C_l * V_{dd}} \tag{C16}$$

$$\frac{\partial F_{osc}}{\partial V_{dd}} = \frac{(\mu_0 * C_{ox} * W) * [(V_{dd})^2 - (V_g - V_{th})^2]}{2 * L * N * C_l * (V_{dd})^2} \tag{C17}$$

The expression for threshold voltage V_{th} is given as [64]:

$$V_{th} = V_{T0} + \gamma \left(\sqrt{(2|\phi_F| + V_{SB})} - \sqrt{2|\phi_F|} \right) \tag{C18}$$

$$\therefore V_{th} = V_{T0},\ when(V_{SB} = 0) \tag{C19}$$

where β represents transconductance parameter, γ is the bulk threshold parameter, ϕ_F represents surface potential in strong inversion and V_{SB} is the source-bulk voltage [64]. Lastly, β is defined by the following physical parameters of the MOS device. That is, μ_0 represents the effective mobility of charge carrier, C_{ox} is the gate-oxide capacitance, V_g and V_d are the gate and drain voltage, and W and L are the channel length and width.

In summary, the task of optimizing the oscillator against variations in supply voltage is very challenging due to the complex relationship between the oscillation frequency F_{osc} and other parameters as presented in Equations (C14) and (C17). Hence, the relationship between ΔF_{osc} and ΔV_{dd} can be approximated as follows for linear operation region of the current-source transistors based on Equation (C14).

$$F_{osc} \propto \frac{\beta \left[(V_{dd})^2 - V_{th} \right]}{V_{dd}} \tag{C20}$$

$$\Rightarrow \frac{\Delta F_{osc}}{\Delta V_{dd}} \propto \beta \left(1 - \frac{V_{th}}{(V_{dd})^2} \right) \cong \beta \propto \frac{1}{L} \tag{C21}$$

Similar approximation can be extracted from Equation (C17) for saturation operation region as expressed in Equations (C22) and (C23).

$$F_{osc} \propto \frac{\beta}{2} \left[\frac{(V_{dd} - V_{th})^2}{V_{dd}} \right] \tag{C22}$$

$$\Rightarrow \frac{\Delta F_{osc}}{\Delta V_{dd}} \propto \frac{\beta}{2} \left(1 - \frac{(V_{th})^2}{(V_{dd})^2} \right) \cong \beta \propto \frac{1}{2L} \tag{C23}$$

Thus, the oscillator can be optimized for high PSRR by increasing the length and reducing the threshold voltage of the controlling transistors. Finally, depending on the power consumption budget of the application, V_{dd}-sensitivity of the oscillator can be significantly reduced by increasing the supply voltage. For example, doubling the supply voltage will reduce $\frac{\partial F_{osc}}{\partial V_{dd}}$ by $\frac{1}{4}$. However, this is not a viable option for low-power designs like DORSI.