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Ultra-Low Power Incremental Delta-Sigma Analog-to-Digital Converter for Self-Powered Sensor Applications

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ABSTRACT OF THE
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In this thesis an ultra-low power incremental delta-sigma analog-to-digital converter is presented. The converter is designed in 0.18 μm CMOS technology with a single 1.2 V supply voltage, and it operates with a 5 kHz clock signal. The differential input signal to the converter is virtually dc, and it varies from -850 mV to 850 mV around a common-mode voltage of 600 mV.

The delta-sigma modulator has a second order cascade-of-integrators feedback structure, which is realized with switched-capacitor integrators and a one-bit quantizer. The converter's quantization noise requirement is met by appropriate choice of coefficients and oversampling ratio, based on MATLAB simulations on an ideal model of the modulator. The minimum requirements of the amplifiers were determined from simulations with macromodels, and the switch non-idealities were analyzed in transistor-level simulations. It was noticed that switch charge injection causes significant harmonic distortion in the circuit, hence bottom plate sampling was implemented to eliminate the signal-dependent charge injection. Furthermore, the offset and low-frequency noise in the first integrator were attenuated by means of chopper stabilization.

The converter's performance is analyzed in different process corners, at $-40°C$, $27°C$, and $85°C$, and its process mismatch sensitivity is determined via Monte Carlo analysis. The results obtained from both pre- and post-layout simulations indicate complete stability, and acceptable accuracy in all design corners. The minimum signal-to-noise and distortion ratio obtained from corner analysis, is 80.05 dB, which is enhanced up to 7 dB in the best corner, and maximum harmonic distortion is below -80.89 dB. Moreover, the power consumption of the converter did not exceed 1.2 μW in any of the simulations.

Keywords: incremental delta-sigma, delta-sigma, analog-to-digital, switched-capacitor, differential, low-power, energy harvesting

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Tässä työssä esitetään ultramatalatehoinen inkrementaalinen delta-sigma-analogia-digitaalimuunnin. Muunnin on suunniteltu 0,18 μm:n CMOS-teknologialla, ja se toimii 1,2 V:n käyttöjännitteellä ja 5 kHz:n kellotaajuudella. Differentiaalinen tulosignaali on käytännössä dc:llä, ja se vaihtelee 600 mV:n yhteismuotoisen jännitteen ympärillä -850 mV:sta 850 mV:iin.

Delta-sigmamodulaattorissa käytetään kaksiasteista takaisinkytkettyä integraattorikaskadirakennetta, joka on toteutettu kytketty-kondensaattori-integraattoreilla ja yksibittisellä kvantisoijalla. Muuntimen kvantisointikohinavaatimuksien täyttyminen varmistettiin valitsemalla sopivat kertoimet ja ylinäytteistyssuhde käyttäen MATLAB-simulaatioita yhdessä modulaattorin ideaalisen mallin kanssa. Vahvistinten vähimmäisvaatimukset määritettiin makromallitason simuloinneilla ja kytkinten epäideaalisuudet analysoitiin transistoritason simuloinneilla. Varausinjektion huomattiin aiheuttavan piirissä merkittävää harmonista säröä, joten alalevyn näytteistystä (bottom plate sampling) käytettiin signaaliriippuvan varausinjektion välttämiseksi. Lisäksi ensimmäisen integraattorin vahvistimen tulonsiirrosjännitteen ja matalataajuisen kohinan vähentämiseksi käytettiin hakkuristabilointia (chopper stabilization).

Muuntimen suorituskykyä analysoitiin eri prosessikulmissa lämpötiloissa $-40\,^{\circ}\mathrm{C}$, $27\,^{\circ}\mathrm{C}$ ja $85\,^{\circ}\mathrm{C}$, ja epäsovitusherkkyys määritettiin Monte Carlo -analyysin avulla. Simulaatiotulokset sekä piirikuvion perusteella lasketut parasiittiset resistanssit ja kapasitanssit huomioonottaen, että ilman, osoittavat piirin olevan stabiili ja täyttävän tarkkuusvaatimukset kaikissa simuloiduissa kulmissa. Monta Carlo -analyysin perusteella signaali-kohinasuhde on vähintään 80,05 dB:ä ja harmonisen särön kokonaismäärä on enintään -80.89 dB:ä. Tehonkulutus ei ylitä 1,2 μA:a missään simulaatiossa.

Avainsanat: inkrementaalinen delta-sigma, delta-sigma, analogia-digitaali, kytkin-kondensaattori, differentiaalinen, matalatehoinen, energiankeräys

Preface

The work presented in this thesis was performed at Electronic Circuit Design (ECD) Group, Department of Micro- and nanosciences, Aalto University, Espoo, Finland. The designed analog-to-digital converter was implemented inside an energy harvesting chip, which received funding from AUTOVOLT and EffiNano projects, granted by Academy of Finland, and Aalto University, School of Electrical Engineering, respectively.

I would like to express my sincere gratitude to my supervisor, Prof. Kari Halonen, for all his technical help and support. The project goals were definitely unreachable without his guidance. I am also deeply grateful to my advisor, Jarno Salomaa, who patiently corrected all my errors, and described every single detail to me. I greatly appreciate the time he devoted to my work, and all his spiritual support. Here, I would also like to thank my other colleagues, Tuomas Haapala and Mika Pulkkinen, whose friendliness and helpfulness warmed me up during cold winter days. Besides, I am indebted to all personnel and researchers at ECD group who created a calm and efficient working atmosphere in the laboratory.

Finally, I thank my beloved friend, Shahab Haeri, who accompanied me in hard days, and and my parents, whose love keeps the blood circulating in my body.

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Shiva Jamalizavareh

Contents

Symbols and abbreviations

Symbols

γ	process-dependent noise factor
τ	time constant
σ_q^2	rms value of quantization noise at the output of the modulator
σ_{out}^2	rms value of quantization noise at the output of the filter
$A_v(0)$	amplifier dc gain
C_L	load capacitance
C_{min}	minimum allowable capacitor size
C_{ox}	oxide capacitance
C_{unit}	unit capacitor
D	largest deviation of converter's output from desired value
f	frequency
f_B	Nyquist frequency
f_c	amplifier corner frequency
f_I	intermediate frequency for the decimation filter
f_s	sampling frequency
g_{ds}	transistor output conductance
g_m	transistor transconductance
I	current
K	Boltzmann constant
KF	process-dependent flicker noise constant
L	transistor length
M	number of samples
N	number of bits
N_f	amplifier noise figure
ω_τ	amplifier unity gain frequency
R_{on}	switch ON resistance
S_c	switched capacitor thermal noise spectrum
T	temperature
t	time
t_p	propagation delay
V_{cm}	common-mode voltage
Vds_{sat}	transistor saturation voltage
$V_{eq,in}$	equivalent input-referred noise
V_{in}	input voltage
v_n	noise voltage
V_{OH}	comparator's high output
V_{OL}	comparator's low output
V_{out}	output voltage
V_{ref}	reference voltage
V_{th}	threshold voltage
W	transistor width

Abbreviations

ADC	analog-to-digital converter
CIFB	common integrator feedback
CIFF	common integrator feedforward
CMFB	common-mode feedback
CRFB	common resonator feedback
CRFF	common resonator feedforward
CT	continuous time
DAC	digital-to-analog converter
DFF	D flip-flop
DNL	differential non-linearity
ENOB	effective number of bits
FFT	fast Fourier transform
FB	feedback
FF	feedforward
FIR	finite impulse response
GBW	gain-bandwidth product
IIR	infinite impulse response
INL	integral non-linearity
LPF	low-pass filter
LSB	least significant bit
MC	Monte Carlo
MOS	metal-oxide-semiconductor transistor
NMOS	n-channel metal-oxide-semiconductor transistor
NTF	noise transfer function
OSR	over sampling ratio
PMOS	p-channel metal-oxide-semiconductor transistor
S/H	sample and hold
SAR	successive approximation register
SC	switched-capacitor
SINAD	signal-to-noise and distortion ratio
SNR	signal-to-noise ratio
STF	signal transfer function
THD	total harmonic distortion

1 Introduction

The rapid growth of wireless electronic applications such as wireless sensor networks and portable electronic devices has made power consumption one of the most important parameters in electronic circuits performance. The problem arises from the fact that despite the advances in electronic circuits, which enable a highly integrated low-power design, the slow progress of battery technology has limited the scaling of batteries both in size and weight. Furthermore, due to the high cost of wiring and replacing the batteries, power supply has become a critical issue in dense sensor networks [1]. Therefore, alternative power supplies, such as energy harvesters, has received increasing attention in recent years.

Whereas the earliest onset of energy harvesting dates back to invention of windmill and water wheel, today, energy harvesting often refers to exploiting the renewable energy resources available in device environment to power up the device. These resources include solar energy, RF radiation, temperature gradient, vibrational excitation, as well as human power, and can be utilized separately or in combination, to provide the desired power supply.

The potential benefits of energy harvesting are that the lifetime of the low power system is not limited by the finite lifetime of its energy source, and that the weight and volume of the system can be reduced if the size of the energy harvester itself is small [2]. However, considerations in using an energy harvesting source are fundamentally different from those in using a battery, because, rather than a limit on the maximum energy, it has a limit on the maximum rate at which the energy can be used [3]. Besides, depending on the source of energy, the available power may change over time, or with respect to device dimensions. As a result, the use of energy harvesting is currently limited to low- or ultra-low power applications such as wireless sensor networks, and miniature biomedical devices.

Typically, a sensor system consists of a sensor, which generates an electric signal when exposed to a certain physical matter, and an interface that converts the sensor output to a human-readable signal. The interface not only filters out the unwanted noise and distortions, but also amplifies the signal so that its amplitude is well above the noise level. Furthermore, the interface converts the analog output of the sensor to a digital signal to enable digital signal processing in next stages. Digital processing offers numerous advantages over analog processing, including easier and cheaper implementation, higher speed, and lower noise sensitivity.

Since the emergence of commercial analog-to-digital converters (ADC) in 1950s, several types of converters have been proposed and optimized for certain applications. Among these, delta-sigma converters have gained popularity over the past decade, since they offer high resolution without the need for high component matching accuracy, as required in successive approximation register (SAR) converters [4]. This is especially attractive for implementation in scaled technologies where transistors are fast but not very accurate [5].

In addition to accuracy and speed, power consumption of an ADC is also of great importance. In fact, in order for the sensor system to survive on harvested energy, the signal processing circuit, including the ADC, should consume little power.

In delta-sigma ADCs, low power consumption can be achieved by operating the ADC in *incremental* mode, rather than continuously. An Incremental ADC, is a delta-sigma converter which is reset periodically. The decimation filter provides the results between two resets, and the conversion time and accuracy are both determined by the time interval between two resets. Incremental operation also enables a single ADC to be switched between multiple channels, and thus eliminates the need for extra ADCs which are potential sources of power and area consumption. Furthermore, incremental converters exhibit lower offset and gain errors, and higher sample by sample accuracy, which makes them an optimum choice for instrumentation and measurement applications [6].

In present work, a 16-bit incremental delta-sigma converter is designed to interface an integrated temperature sensor in an energy harvesting system. The ADC is designed in 0.18 μm CMOS technology using Cadence Virtuoso, and is evaluated based on power spectrum analysis in MATLAB.

The thesis is organized as follows. Chapter 2 provides an overview of analog-to-digital conversion, particularly delta-sigma conversion, and describes the building blocks of delta-sigma ADCs in details. Chapter 3 goes through the design procedure of the implemented incremental delta-sigma converter, and discusses the results of pre-layout simulation of each block. Furthermore, the chapter presents the results of frequency-domain analyses performed on the designed ADC. This is followed by a description of layout design and post-layout simulations in Chapter 4. Finally, in Chapter 5, conclusions are drawn.

2 Theory

2.1 Analog-to-Digital Conversion

Analog-to-digital converters are typically classified into two main categories, i.e. Nyquist rate and oversampling converters.

Nyquist rate converters are defined as those converters, in which each output level has a one-to-one correspondence with an input value, implying an operation rate equal to signal's Nyquist rate. However, typical Nyquist rate converters operate at 1.5 to 10 times Nyquist rate due to difficulties in realizing practical anti-aliasing filters. Oversampling converters, on the other hand, operate at much higher rates (typically 20 to 512 times Nyquist rate), and hence simplify the requirements placed on anti-aliasing filters by increasing the bandwidth of the sampled signal. Also, with oversampling, analog components have reduced requirements on matching tolerances, and amplifier gain [7]. Besides, as it will be shown next, oversampling converters can provide high accuracy at a reasonable conversion speed.

Apart from circuit implementation, ADCs are usually compared with respect to their accuracy, linearity, and speed. Below, the important parameters in typical ADCs are briefly introduced to provide a mathematical insight into ADC's performance, and avoid subjective discussions throughout the thesis.

2.1.1 Terminology

Resolution is the number of digital output levels, and can be expressed in terms of bits or volts. An ADC with 2^N distinct output levels, has N bit resolution, or equivalently, its least significant bit (LSB) equals $\frac{V_{ref}}{2^N+1}$, where V_{ref} is the reference voltage of the ADC. Ideally, LSB is the minimum input voltage change which causes a change in output digital code. However, there is no guarantee that the output is correct.

Accuracy describes how accurately the output word resembles the input voltage. Absolute accuracy or total error, is usually expressed in terms of Effective Number of Bits (ENOB) which is defined below:

$$ENOB = \log_2(\frac{V_{ref}}{D}) \tag{1}$$

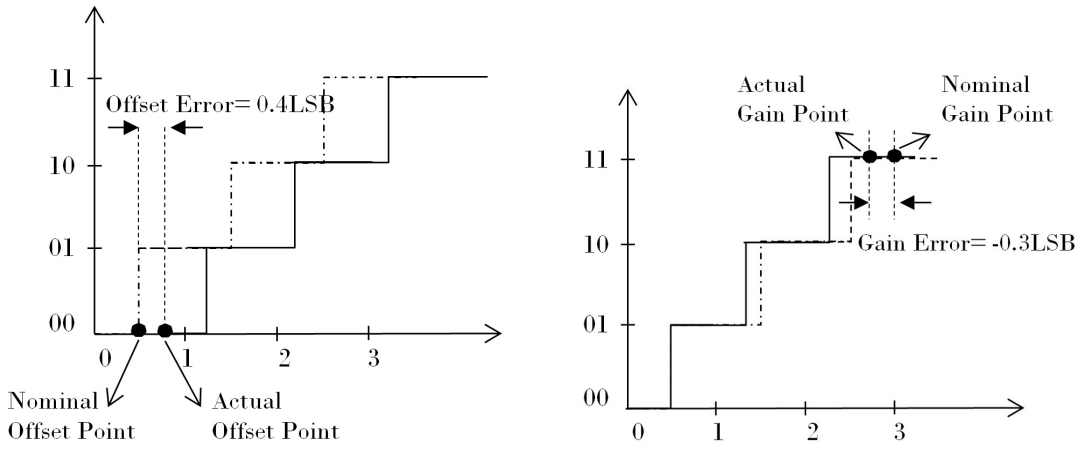
where D is the largest deviation of the input from its ideal value, for a given output code.

Even in an ideal ADC, there is a range of valid inputs that produce the same output word. This signal ambiguity results in an inevitable $\pm LSB/2$ error in the output, and produces what is known as quantization noise.

In addition, there are 4 other factors which contribute to total error: offset error, gain error, differential nonlinearity (DNL), and integral nonlinearity (INL).

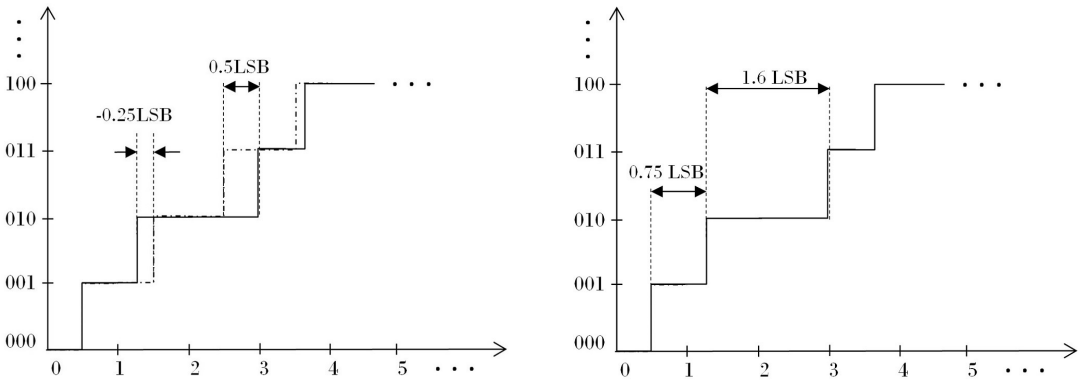
Offset and gain errors are defined as the difference between ideal and actual offset and gain points, respectively (Fig. 1). As the names suggest, offset error affects all the codes by the same amount, whereas gain error causes the same percentage error in each step. Therefore, in most cases these errors can be adjusted to zero

by trimming, and they don't affect the ADC's performance significantly [8]. Conversely, DNL and INL affect the linearity of the ADC, thus they may degrade the performance severely.



(a) Offset Error (b) Gain Error

Figure 1: ADC linear errors.



(a) DNL (b) INL

Figure 2: ADC nonlinear errors.

DNL, is defined as the difference between actual and ideal 1-LSB step widths (Fig. 2(a)). If DNL exceeds 1 LSB, there is a possibility that the one or more of the possible 2^N binary codes are never output (missing codes). The converter may also exhibit non-monotonicity, i.e. the magnitude of the output may get smaller for an increase in the input.

Generally, it can be shown that an alternating DNL of x and $-x$ results in a loss of resolution equal to $\frac{\log(1+3x^2)}{\log(4)}$, which corresponds to 1 bit loss for $x = 1\ LSB$ [9].

The INL, depicted in Fig. 2(b), is the deviation of the values on the actual transfer function from a straight line. This straight line is a line drawn between the end points of the transfer function once the gain and offset errors have been nullified.

With this definition, INL in each step can also be calculated by summing the DNL values from bottom up to that step. Whereas DNL increases the total noise level of the system, INL leads to harmonic distortion in the output power spectrum.

Apart from parameters extracted from ADC's transfer curve, the frequency-domain parameters, such as Signal to Noise Ratio (SNR), and Total Harmonic Distortion (THD) can also be used to evaluate ADC's performance.

Given the output spectrum of an ADC, SNR is defined as

$$SNR = 20\log(\frac{\mid Fundamental \mid}{\sqrt{\sum Noise^2}})\ dB \tag{2}$$

where noise components include all non-fundamental spectral components in the Nyquist range, except for dc and the harmonics of the fundamental signal.

If an ideal Nyquist rate ADC is driven with a sinusoidal input varying from 0 to V_{ref}, and quantization noise is assumed to be randomly distributed from -0.5 LSB to 0.5 LSB, the maximum SNR can be written as: [7]

$$SNR_{Max} = 6.02N + 1.76 \quad dB \tag{3}$$

In order to apply the above equation to non-ideal cases, where ADC's performance is degraded by distortions, SNR should be replaced by *Signal to Noise and Distortion Ratio (SINAD)* which is defined as below:

$$SINAD = 20\log(\frac{\mid Fundamental \mid}{\sqrt{\sum (Noise + Harmonics)^2}})\ dB \tag{4}$$

(3) and (4) result in an expression of absolute accuracy based on output spectral properties which is of great importance in ADC analysis:

$$ENOB = \frac{SINAD\ (dB) - 1.76}{6.02} \tag{5}$$

The above equation shows the total error of the ADC in terms of ENOB; however, it doesn't provide any information on sources of errors and their profiles.

According to [9], error profiles can be partly extracted from the harmonics that appear in output spectrum. In fact, total harmonic distortion quantifies the noise caused by ADC non-linearities, previously expressed in terms of INL and DNL.

$$THD = 20\log(\frac{\sqrt{\sum Harmonics^2}}{\mid Fundamental \mid}) \tag{6}$$

The above discussion reveals that an ADC can be roughly characterized by its frequency-domain behavior. Nonetheless, obtaining an accurate estimate of SNR and THD depends on the accuracy of the computed spectrum.

Next section discusses the intricacies of frequency-domain analysis, as well as popular methods of time-domain analysis.

2.1.2 Methodology

Perhaps, the most straightforward way of analyzing the accuracy of an ADC is to obtain its transfer curve by sweeping the input signal over the entire allowable input range and extracting the output digital codes for all input steps. In this method, known as full-code histogram test, the precision of the final transfer curve strongly depends on the input increment size, which is often less than half LSB. Therefore, for high resolution delta-sigma converters ($N \geq 16$), enormous number of simulations should be done and the analysis takes up much time as well as memory space. Furthermore, in incremental delta-sigma modulators, the simulation time also depends on the oversampling ratio (OSR). To avoid huge simulations, in some linearity tests only a reduced set of codes are tested [10]. According to [11], simulations done with steps equal to or smaller than one-eighth of the required ENOB have acceptable accuracy, although they are not able to determine the DNL and INL precisely.

Another popular method which is widely used in ADC analysis, is frequency analysis of the output of an ADC driven with a pure sinusoidal input. The performance parameters in frequency-domain, such as SINAD and THD can be readily calculated from the output frequency spectrum, and the absolute accuracy of the converter can then be calculated using (5). Also, converter's linearity can be estimated based on THD values. However, in case of delta-sigma modulators, obtaining an accurate spectrum out of Fast Fourier Transform (FFT) is not trivial, and special considerations should be taken into account to avoid erroneous power spectrums. Here it suffices to mention that by using appropriate windowing, a reliable and repeatable output spectrum can be obtained from $64 * OSR$ samples [12]. Therefore, with typical values of OSR, the number of required samples for frequency analysis is significantly less than 2^N samples required in full-code test. Furthermore, it will be shown later in this chapter that the above analyses are also applicable to incremental delta-sigma ADCs, although the narrow frequency band of such converters imposes some limitations on FFT accuracy. Therefore, in this thesis, the designed ADC is evaluated merely by frequency-domain analysis to minimize the simulation time and memory usage.

After introducing the basics of analog-to-digital conversion which apply to all converter structures, in following sections we focus our discussion on delta-sigma ADCs which are a subclass of oversampling converters.

2.2 Delta Sigma ADCs – System level Design

This section presents the theory behind delta-sigma converters and gives a detailed description of ADC's building blocks and their design issues. The section starts with a comprehensive explanation of oversampling and delta-sigma conversion, and continues with a brief discussion of decimation filters. Finally, the section is concluded with a comparison of incremental and conventional delta-sigma ADCs.

As shown in Fig. 3, a delta-sigma ADC can be divided into 3 main stages: the input stage, consisting of an anti-aliasing filter and a sample and hold (S/H) block, the noise-shaping stage, and finally the digital output stage.

The anti-aliasing filter is used to restrict the input bandwidth to Nyquist frequency and prevent aliasing in the sampled signal. The sample and hold block can greatly reduce the errors due to different delay times in the internal operation of the converter, and is necessary in many ADCs. The delta-sigma modulator, converts the sampled analog signal to a noise shaped low resolution digital signal. The shaped signal is then fed into the decimation filter which outputs a high resolution signal at a lower sampling rate.

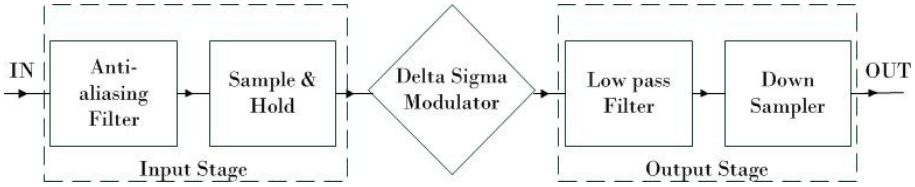


Figure 3: Block diagram of a delta-sigma ADC.

Thanks to the relatively high oversampling ratio, the demands on anti-aliasing filter are relaxed in oversampling converters, and acceptable performance can be achieved using a simple RC filter. On the other hand, the decimation filter plays a significant role in the accuracy of the ADC, and various architectures have been proposed to optimize the post filtering.

2.2.1 Delta Sigma Conversion

The use of shaped quantization noise applied to oversampling signals is commonly referred to as delta-sigma modulation [7]. The delta-sigma modulator modulates the noise to higher frequencies so that it can be eliminated via post filtering without affecting the in-band signal. In the simplest form, noise shaping can be achieved using the structure depicted in Fig. 4.

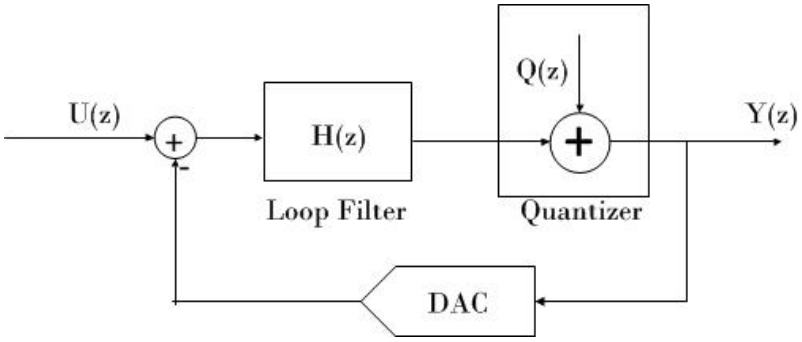


Figure 4: Block diagram of a first order delta-sigma modulator.

The quantizer of Fig. 4, can be generally treated as an additive noise source equal to the quantization noise [7]. By using this linear model for the quantizer, following equations can be derived:

$$STF(z) \equiv \frac{Y(z)}{U(z)} = \frac{H(z)}{1 + H(z)} \tag{7}$$

$$NTF(z) \equiv \frac{Y(z)}{E(z)} = \frac{1}{1+H(z)} \tag{8}$$

According to equation 8, in order to remove the noise from dc, *H(z)* should have a pole at dc, i.e. it should be an integrator described by e.g. $H(z) = \frac{1}{z-1}$. This results in $STF(z) = z^{-1}$, and $NTF(z) = 1 - z^{-1}$. Hence, the input signal will undergo merely a delay, whereas the noise is high-pass filtered through the modulator, leading to an improvement in the in-band SNR which is directly related to the order of noise shaping. This is illustrated in Fig. 5 which shows the output spectrum of an ADC with- and without noise shaping.

Generally, for an Lth-order delta-sigma modulator, the in-band noise decreases $3(2L+1)\ dB$ for every doubling of the sampling rate, providing $(L+0.5)$ extra bits of resolution [12]:

$$SNR_{Max} = 6.02N + 1.76 - 5.17 + 10(2L+1)\log(OSR)\ dB \tag{9}$$

whereas without noise shaping the maximum SNR is given by [12]

$$SNR_{Max} = 6.02N + 1.76 + 10\log(OSR)\ dB \tag{10}$$

Equation 9 indicates a minimum limit for OSR, below which the negative term cancels out the effects of OSR term, and SNR decreases. Therefore, in most applications OSR values higher than 48 are used [13]. The oversampling ratio can be further increased to achieve better noise shaping, but this reaches its limit in high frequency applications, where implementing a high OSR is impossible. In such applications, SNR_{max} can be improved by utilizing higher order loop filters. Higher order modulation also helps reducing the conversion time by reducing the OSR value required for a certain accuracy. However, there exists a trade-off between modulator's order and instability. In other words, the range of input signal values, for which the conversion is performed successfully without leading the ADC to instability, shrinks for higher order loop filters. Furthermore, there is a direct relationship between modulator's order and ADC's complexity, as well as power consumption. Therefore, in low power applications the tendency is usually towards second or third order modulators which offer high accuracy and moderate stability for an acceptable design complexity.

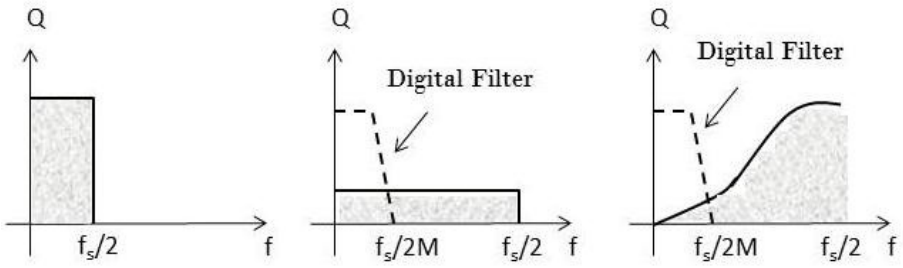


Figure 5: Noise spectrum in a) Nyquist ADC, b)Oversampling ADC, c)Delta sigma ADC, reproduced from [14].

In addition to OSR and the order of the loop filter, quantizer's order also affects the ADC's performance. Generally, use of K-bit quantizer instead of 1-bit quantizer reduces the quantization error by a factor of $2K$, resulting in $6.02NdB$ improvement in SNR. Besides, a multi-bit quantizer can enhance the stability of the modulator, and relax the opamp slewing requirements by reducing the input to the integrators [15]. However, despite all these advantages, single-bit quantizers are more popular in today's delta-sigma ADCs . This is due to the fact that, single-bit delta-sigma modulation is robust against circuit imperfections, owing to the feedback which compensates for deviations in the quantization thresholds. Due to the inherent linearity of a two-level DAC, the deviations in a two-level feedback, only amounts to an offset error combined with a gain error, while deviations from a multilevel feedback would cause harmonics [16]. Furthermore , as it will be shown in section 2.3.3, a one-bit quantizer can be realized using a single comparator, whereas multi-bit quantizers typically require tens of comparators, and are often the largest contributor to the total chip area, and power consumption of an ADC [15].

After all, it's worth reminding that equation (9) is derived based on a white noise assumption for quantization noise, and it doesn't show the irregularities such as idle tones and limit cycles, which may occur due to the non-linear operation of the quantizer. A limit cycle occurs, when the output of the delta-sigma modulator becomes cyclical and enters a periodic pattern [17]. This phenomenon which is a consequence of modulator's instability, results in a set of well-defined harmonics with no noise shaping in the output spectrum. In contrary, idle tones are *irregular* spikes which occur at random frequencies, due to a rational dc input. Idle tones arise from the non-linear nature of the quantizer, and are inevitable in first order modulators. Therefore, higher order modulators are usually preferred in tone-sensitive applications.

2.2.2 Decimation Filter

As described in previous section, delta-sigma modulation does not reduce the overall noise; rather, it pushes the quantization noise to high frequencies where it can be removed via digital filtering. If the decimation filter fails to attenuate the high frequency noise components, they will be aliased into the band due to down sampling, and SNR will degrade. This implies that the accuracy of the delta-sigma converter is limited by the ability of the decimation filter in successful removal of out-of-band noise.

In order to illustrate the functionality of the decimation filter, evolution of the input signal through the delta-sigma ADC has been drawn in Fig. 6.

Fig. 6(a) shows the one-bit digital stream at the output of the delta-sigma modulator which contains substantial amount of out-of-band noise. The decimation filter first reduces the quantization noise through the use of a digital low-pass filter (LPF), resulting in the multi-bit signal $X_lp(n)$. As shown in Fig. 6(b), this also removes any higher-frequency signal content that was originally on the input signal, and thus acts as an anti-aliasing filter to limit the signal to one-half of the output sampling rate, $2f_0$. Finally, $X_s(n)$ is obtained by keeping the samples at a submultiple of oversam-

pling ratio, and discarding the rest of the samples [1]. In practical design, usually the low-pass filter and down-sampler are combined so that modulator's output is directly converted to $X_s(n)$, without producing the redundant signal $X_lp(n)$.

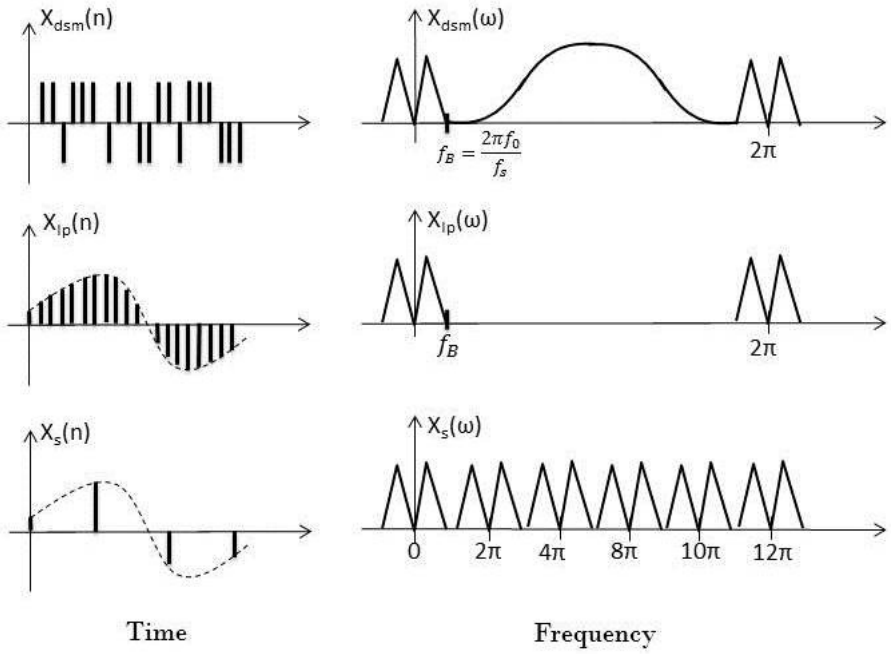


Figure 6: Signal evolution in a delta-sigma ADC, reproduced from [1].

Clearly, the gain response of the LPF is required to be large and flat over the signal band $[0,\ f_B]$, and very small in $[f_B,\ f_s/2]$. Often, it is also desirable to have a flat group delay response in the signal band, a requirement which can be satisfied by using a linear-phase finite impulse response (FIR) LPF. In case of a first order delta-sigma modulator, it may be practical to use a single-stage high order FIR filter, but in general, it is usually more efficient and economical to carry out the filtering and decimation in stages. [12]

The most common filtering stage is a *sinc* filter, which is an FIR filter with $N-1$ delays and N equally valued taps. A *sinc* filter simply computes a running average of the input data stream $v(n)$, and its output $w(n)$ can be described as follows:[18]

$$w(n) = \frac{1}{N}\sum_{i=0}^{N-1} v(n-i) \tag{11}$$

Therefore, as its name implies, a sinc filter is characterized by a sinc transfer function:

$$H_l(e^{j2\pi f}) = \frac{sinc(Nf)}{sinc(f)} \tag{12}$$

or equivalently in $z-$domain

$$H_l(z) = \frac{1}{N}\frac{1-z^{-N}}{1-z^{-1}} \tag{13}$$

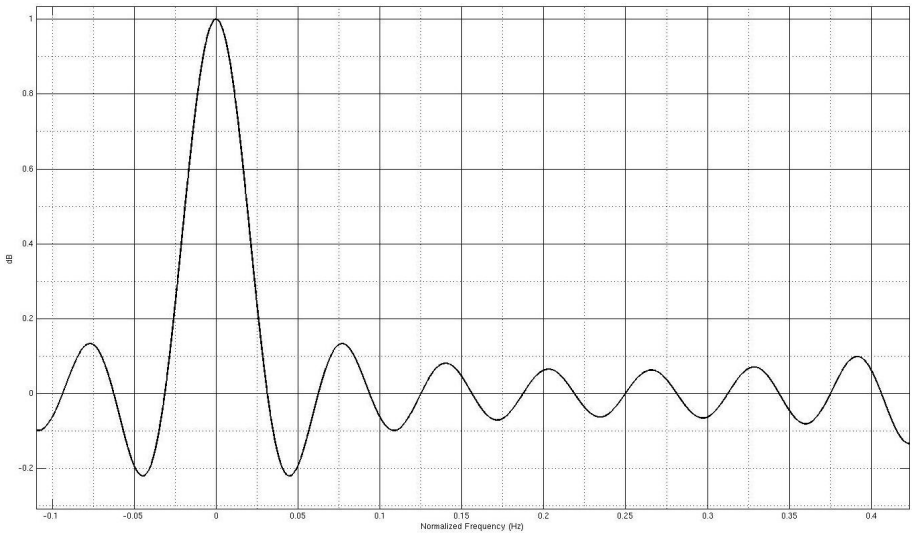


Figure 7: Frequency response of a sinc filter with N=16.

Equation (12) is further illustrated in Fig. 7, which depicts the frequency response of a sinc filter with $N = 32$. It can be clearly seen that the gain of the filter is close to 1 at around $f = 0$, and close to zero near f_s/N and its harmonics. Therefore, in order to attenuate the modulator noise falling at multiples of $\frac{f_s}{OSR}$, $N = OSR$ should be chosen. This results in a noise reduction at the output of the filter, which is proportional to $1/N^2$:[18]

$$\sigma^2_{out1} = \frac{2\sigma_q^2}{N^2} \tag{14}$$

whereas the output noise power of an ideal LPF with unit gain at *dc* is given by:

$$\sigma^2_{out-Ideal} = \frac{\pi^2\sigma_q^2}{3 * N^3} \tag{15}$$

where σ_q^2 is the rms value of the quantization noise present at the output of the modulator.

The above equations show that the *sinc* attenuation, although significant, is N times less than an ideal low pass filter. Hence, a sinc filter is seldom used as a complete decimation filter; rather, it normally forms only one stage of a multi-stage filter. [18]

Generally, there are two important factors which should be taken into account when choosing the right order K of the $sinc^k$ filter for an $Lth-$order delta-sigma modulator. Firstly, the cut off rate of the filter around f_B should be larger than the rate of NTF rise, so that the amount of unsuppressed out-of-band noise left around $f = f_B$ is negligible. Second, the gain response of the filter around multiples of $\frac{f_s}{OSR}$ should be flatter than NTF around *dc*, to guarantee that the folded noise from frequency bands around $\frac{f_s}{OSR}$ and its harmonics, adds little to the in-band noise. These conditions both require that $K > L$, and usually $K = L + 1$ is adequate. As an example, in the first order modulator discussed above, using a $sinc^2$ filter results in an attenuation comparable to the ideal LPF:

$$\sigma_{out2}^2 = \frac{2\sigma_q^2}{N^3} \tag{16}$$

Apart from noise attenuation, the decimation filter must also bring the frequency of the oversampled signal down to f_B. Theoretically, this can be achieved by using a single-stage *sinc* filter, but, due to difficulties of implementing the narrow transition band required in this approach, it is typically more efficient to carry out the decimation in two stages. [18]

As shown in Fig. 8, in a two-stage decimation filter the signal is first sampled down to an intermediate frequency, f_I. Then, the second filter which may have a *finite* or *infinite* impulse response (IIR), decimates the signal from f_I to 2 times f_B. The choice of f_I depends on a number of factors, but typically a f_s/f_I ratio of 4 is optimum.

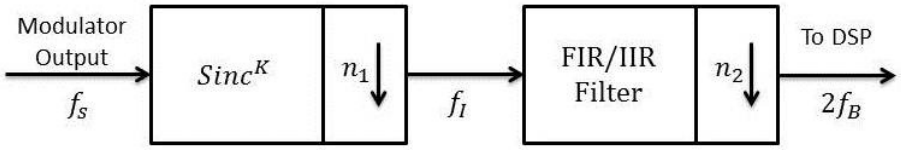


Figure 8: A two-stage decimation filter.

The modulator and the decimation filter described above, both work in a continuous mode, meaning that the input signal is continuously sampled and modulated, and the decimation filter is working in a free-running mode. Interestingly, a delta-sigma modulator can also work in an intermittent mode in which case it's called an incremental delta-sigma converter. Following section describes the operation principles of incremental delta-sigma ADCs, and compares their performance with continuous delta-sigma converters.

2.2.3 Incremental Delta Sigma Conversion

An incremental ADC is a delta-sigma ADC which is reset periodically. Between two resets, the decimation filter provides the conversion result and after each reset, the converter can be switched to convert the signal in another channel, if desired. In this way, power consumption can be decreased substantially due to intermittent operation of the modulator, and a single incremental ADC can be easily time-multiplexed between many channels. The intermittent functioning, however, limits the overall accuracy. In fact, it can be shown that the output quantization noise after M cycles is approximately proportional to $\frac{1}{M^{(2L+1)}}$ for an Lth order delta-sigma ADC, whereas it is proportional to $\frac{1}{M^{(2L)}}$ for an Lth order incremental ADC [19]. This is due to the fact that, as a result of resetting the modulator and the decimation filter, the length of the impulse response of the NTF for an incremental ADC is limited to M samples.

In an incremental ADC, M is usually determined by a reset signal. Reset serves as the trigger signal for the circuit and its falling edge indicates beginning of a conversion. When reset is active, the integrating capacitors are rest, and the quantizer

output is disconnected from signal path. Also, the counters are reset before each conversion. As a result, the number of samples per conversion, and subsequently the accuracy of the results depends on the time interval between two resets. This indicates that in incremental mode, conversion time can be traded off for higher accuracy. Therefore, an adjustable reset signal can be utilized to optimize the number of samples per conversion for each analog input. This also reduces the average power consumption, since the energy per conversion in a delta-sigma ADC not only depends on modulator's power consumption, but also is a function of conversion time.

Now that the principles of delta-sigma conversion are established, and incremental operation has been discussed, it's time to turn our attention to circuit-level implementation of [incremental] delta-sigma ADCs, which is the topic of following section.

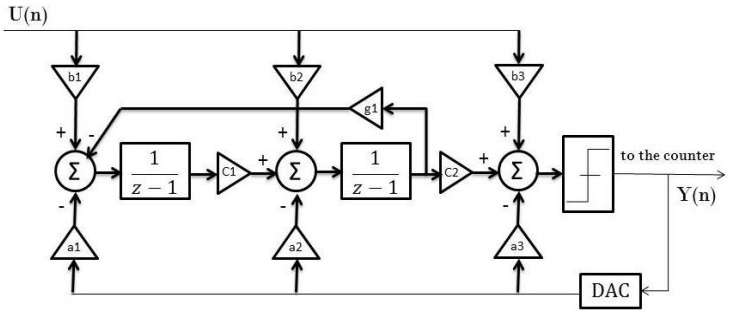
2.3 Delta Sigma ADCs – Circuit Level Implementation.

An Nth order delta-sigma loop filter can be realized by cascading N delaying integrators either in feedback (FB) or in feedforward (FF) form (Fig. 9). Alternatively, every other delaying integrators can be replaced by non-delaying ones so that resonators are formed (Fig. 10). By using resonators, complex zeros can be realized, hence NTF zeros can be adjusted for maximum SNR improvement. However, use of non-delaying integrators increases the opamp slew-rate and bandwidth requirements [20]. Furthermore, in first or second order modulators the zeros must be placed exactly at dc, thus using a resonator-based structure does not improve the noise shaping.

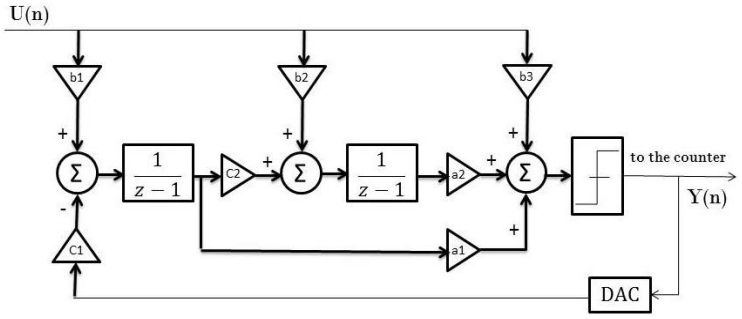
The feedforward topologies exhibit lower distortion compared to their feedback counterparts, since the feedforward path removes the input signal from integrators outputs. Nonetheless, it is worth noting that FF topologies require an additional adder before the quantizer, which corresponds to higher power consumption, and larger chip area. Besides, the lack of a feedback path results in tighter stability limits. Therefore, the FB structure is more widely used in commercial ADCs.

Considering above trade-offs, the optimum topology varies based on the target application. In case of an ultra-low power energy harvester, which is the focus of this thesis, a CIFB structure seems promising, since it offers good stability as well as low power consumption, and relaxes the requirements on the integrators. The latter helps improving the ADC's performance, given the fact that integrator non-idealities, such as finite gain and bandwidth, impose inevitable timing constraints on the converter, and also degrade the SNR.

In following sections, the ADC's building blocks including the integrators and the quantizer are described, and effects of components non-idealities on ADC's performance are discussed in detail.

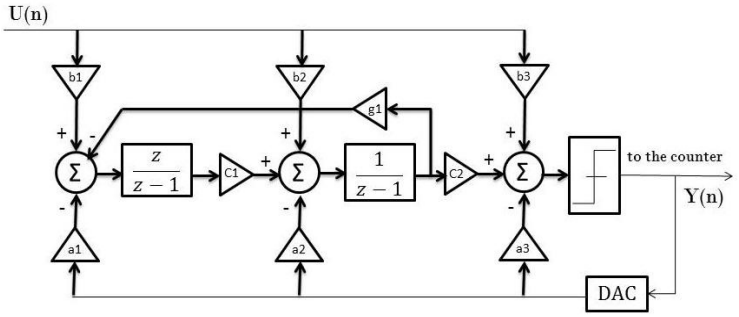


(a) CIFB

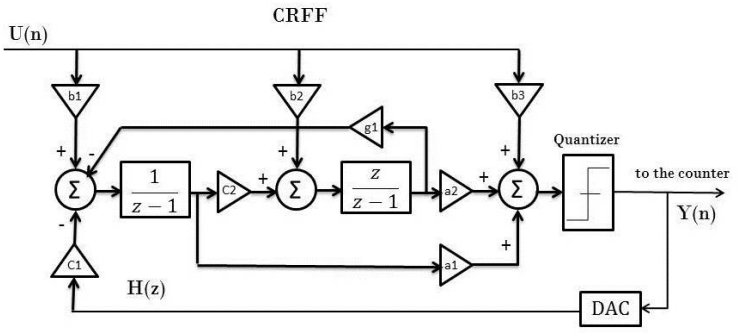


(b) CIFF

Figure 9: Integrator-based delta-sigma topologies.



(a) CRFB



(b) CRFF

Figure 10: Resonator-based delta-sigma topologies.

2.3.1 Switched Capacitor Integrators

The integrators used in a delta-sigma modulator can be realized using common inverting/non-inverting switched capacitor(SC) blocks (Fig. 11). Use of SC integrators eliminates the need for a separate S/H stage before the ADC, and also improves the circuit immunity to parameter variations. However, SC blocks limit the ADC's maximum achievable SNR and speed.

Basically, there are 5 main performance-limiting factors in a SC integrator: thermal and flicker noise, on resistance of switches (R_{on}), finite opamp gain and bandwidth, and finite available current.

The dynamic range in a SC block is fundamentally limited by the thermal noise sampled to the switching capacitor [21]. Thermal noise comes from two main sources, i.e. the amplifier, and the switches.

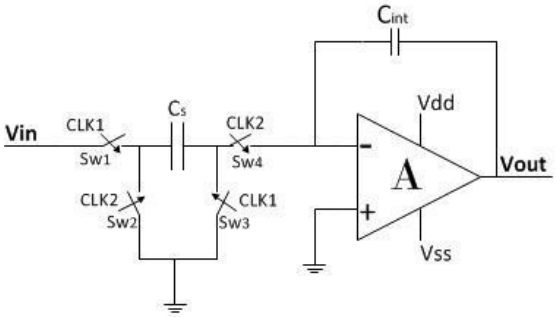


Figure 11: A single-ended SC integrator.

In sampling phase, depicted in Fig. 12(a), the amplifier is disconnected from the switches, and the switched capacitor together with the on resistance of the switches form an RC filter. Therefore, the noise across the capacitor is the thermal noise of the switches filtered by the RC filter:

$$S_c(f) = \frac{8KTR_{on}}{(1+2\pi f\tau)^2} \tag{17}$$

where K is the Boltzmann constant, T is the absolute temperature, and $\tau = 2R_{on}C_s$. The total noise power sampled in C_s is then obtained by integrating the above power spectral density over the entire spectrum:

$$Vc^2_{phase1} = \frac{8KTC_sR_{on}}{4\tau} = \frac{KT}{C_s} \tag{18}$$

which is independent of R_{on}.

In integrating phase depicted in Fig. 12(b), the noise of the amplifier also comes to play, and total noise power is calculated as follows: [22]

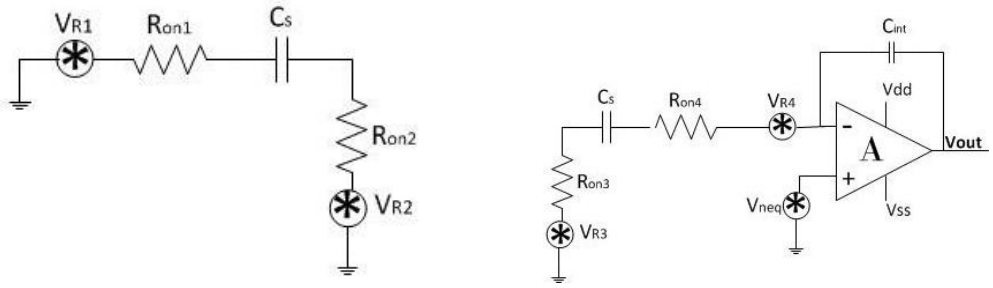
$$Vc^2_{phase2} = (Vc_{-amp})^2 + (Vc_{-Sw})^2 = \frac{1}{4 * C_s(2R_{on} + \frac{1}{g_{m1}})}(\frac{16KTN_f}{g_{m1}} + 8KTR_{on}) \tag{19}$$

where g_{m1} is the transconductance of the amplifier's input pair, N_f is a scaling factor determined by opamp's topology, and Vc_{-amp} and Vc_{-Sw} are the noise contribution of the amplifier and the switch, respectively.

Finally, the total integrator noise is computed by summing the noise from sampling and integrating phases:[22]

$$Vc_{tot}^2 = \frac{KT}{C_s}\left(1 + \frac{2R_{on}g_{m1} + 4N_f/3}{1 + 2R_{on}g_{m1}}\right) \tag{20}$$

The above equation reaches its minimum when $R_{on}g_{m1} \to \infty$, which results in $Vc_{tot}^2 = \frac{2KT}{C_s}$. This indicates that, with negligible noise contribution from the opamp ($R_{on} \gg \frac{1}{gm}$), the maximum achievable SNR is limited by the noise of the smallest switched capacitor in the circuit. Therefore, in a SC integrator, the minimum allowable capacitor value, C_{min}, is determined according to the desired dynamic range.



(a) Sampling Phase (b) Integrating Phase

Figure 12: Noise-equivalent circuit of a SC integrator, reproduced from [22].

If the sampled thermal noise is assumed to be evenly distributed over $[0,\ f_s/2]$, and the entire ADC noise budget is allocated to the first integrator, C_{min} can be computed as below: [12]

$$C_{min} = \frac{KT}{OSR * v_n^2} \tag{21}$$

where v_n^2 is the noise power calculated from target SNR.

Although equation (21) is derived based on the noise of a single integrator, it is generally used in analyzing the delta-sigma ADCs of any order. This is due to the fact that, despite the considerable thermal noise present at the input of all integrators, the noise of each integrator is attenuated by the gain of its preceding stages, thus noise contribution of farther integrators is negligible compared to that of first integrator.

One should also note that C_{min} does not change for a differential integrator, as both signal amplitude and the number of capacitors are doubled at the same time. However, the contribution of opamp white current noise to the overall integrator noise is higher in a differential topology [23], which leads to a slightly higher noise level in a differential integrator.

In addition to the thermal noise of a conducting switch, an off switch can also produce errors in the circuit via three mechanisms: leakage, charge injection, and clock feedthrough. Moreover, the nonlinear capacitors from transistor terminals to substrate, i.e. C_{sb} and C_{db} in Fig. 13, can cause harmonic distortion, and may couple the substrate noise to the signal path. In addition, the gate capacitors C_{gs} and C_{gd} make voltage dividers with circuit capacitors, providing a path for the clock signal to couple to the signal nodes (clock feedthrough). Furthermore, C_{gs} also holds the channel charge, which flows to transistor terminals when the switch turns off, and alters the voltage over sampling capacitor(charge injection).

The error produced by clock feedthrough can be calculated by a voltage division at the input of the integrator:

$$\Delta V = V_{CLK} \frac{C_{SW}}{C_{SW} + C_s} \tag{22}$$

where C_{SW} is the total overlap capacitance of the transistor. This equation shows that clock feedthrough is independent of the input voltage, hence it only introduces offset and gain error.

On the other hand, charge injection shows a linear dependence on channel charge, which is a function of of $V_{in} - V_{th}$:

$$\Delta q = WLC_{ox}(V_{in} - V_{th}) \tag{23}$$

where C_{ox} is the oxide capacitance, V_{th} is the threshold voltage, and W and L are width and length of the transistor, respectively.

Hence, nonlinear dependence of V_{th} on V_{in} introduces nonlinearity in the signal-transfer characteristics.

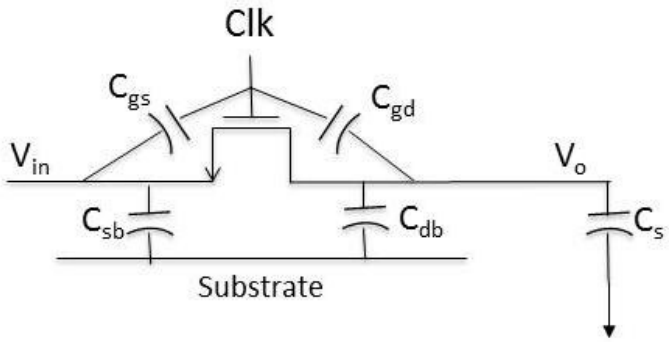


Figure 13: MOS switch and its parasitic capacitors.

One may assume that charge injection can be eliminated using differential circuits. However, although differential signaling removes the *dc* offset and reduces the non-linearities, it can not cancel out the charge injection completely, and the injected charge varies with the differential input voltage as described by following equation:

$$\Delta q = WLC_{ox}[(V_{in2} - V_{in1}) + (V_{th2} - V_{th1})] \tag{24}$$

Similarly, implementing transmission gates instead of single MOS switches helps reducing the charge injection, due to opposite charge injection of PMOS and NMOS, but it can not nullify the effect. Therefore, in high-precision SC circuits, additional techniques should be utilized to eliminate the charge injection errors. One such technique is bottom-plate sampling (Fig. 14). In this technique, the ground switch, M_2, turns off slightly sooner than the main switch, and disconnects the bottom plate of the capacitor from ground (or virtual ground), thereby creating an open circuit for the main switch (M_1). Hence, when M_1 turns off, the channel charge can not flow into the output node of C_s, and V_O is not altered. Besides, given the constant voltage over M_2, the charge injection due to bottom-plate sampling is always constant and its effect can be removed by means of differential signaling.

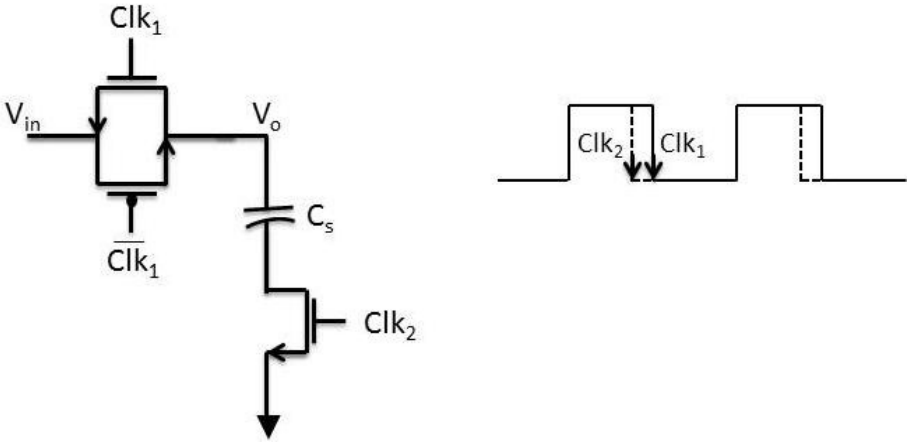


Figure 14: Bottom-plate sampling.

Another prominent source of error in an integrator is the amplifier's finite gain and bandwidth. First of all, finite opamp *dc* gain(A) shifts the NTF poles away from *dc* by a factor proportional to $1/A$, and leads to a leaky integrator, whose *dc* gain is equal to the opamp *dc* gain. In a first order modulator, the shift in NTF pole creates deadbands in response to *dc* inputs, meaning that around some specific *dc* input values, the change in the input does not alter the output. This effect is drastically reduced in a second or higher order modulator, since the loop filter's *dc* gain is proportional to A^N [12]; however with a low loop gain, nonlinearity of the opamp manifests itself. Opamp nonlineairty can degrade the ADC's performance significantly by folding back the high frequency noise to the signal band, and may also produce harmonics in the output spectrum. Therefore, depending on the topology and loop filter coefficients, there exists a minimum limit for amplifier's gain, below which the noise of the amplifier will dominate the thermal noise and the delta-sigma converter would fail to fulfill the requirements.

Second, the converter's speed is limited by settling time of the integrators, which is determined by opamp slew rate and unity-gain bandwidth, ω_τ. The step response of an amplifier in unity feedback configuration consists of a linear and a non-linear settling phase. Whereas linear settling time is a function of ω_τ and input voltage

step, the non-linear settling time is determined by the slew rate and is a function of output voltage step size:[7]

$$t_{linear} = -ln\left(1 - \frac{\Delta V_{out,linear}}{\Delta V_{out,t}}\right)\dot{\tau} \tag{25}$$

$$t_{slew} = \frac{\Delta V_{out,slew}}{SR} = \frac{\Delta V_{out,slew}}{I_{max}} C_{eq} \tag{26}$$

where I_{max} is the maximum available current during slewing, C_{eq} is the equivalent capacitive load seen at the output of the integrator in feedback configuration, and τ is the settling time constant, which is defined as:

$$\tau = \frac{C_{eq}}{g_{m1}} = \frac{C_{eq}}{\omega_\tau \dot{C}_L} \tag{27}$$

C_L is the amplifier's output capacitance that is formed by the opamp parasitic output capacitance C_o and the feedback network (Fig. 11):

$$C_L = C_o + \frac{C_s C_{int}}{C_s + C_{int}} \tag{28}$$

and C_{eq} is calculated from feedback factor β: [27]

$$C_{eq} = \frac{C_L}{\beta} = \frac{C_L\dot{(}C_s + C_{int})}{C_{int}} = C_o + C_s + \frac{C_o C_s}{C_{int}} \tag{29}$$

Equaitons (25) and (26) clearly show the speed limitations caused by finite amplifier slewing current and bandwidth. However, the disruptive effects of amplifier non-idealities on ADC's performance can be successfully overcome if the amplifier is designed properly.

Therefore, following section is devoted to introducing the amplifier topologies which are commonly used in delta-sigma converters, and discussing their properties.

2.3.2 Amplifier

In general, the choice of the amplifier depends on the application requirements such as gain, speed, slew current, voltage swing and total power consumption.

Basically, an amplifier can be realized either in a single stage, or in a series of stages. Single-stage amplifiers achieve a high *dc* gain by utilizing cascode transistors, whereas in two-stage amplifiers the gain is divided between two stages, where the output stage typically consists of only two transistors with common-source topology. As a result, two-stage amplifiers offer larger signal swing, at the expense of added complexity, larger area, and higher power consumption. Therefore, considering the power consumption constraints of the target energy harvester, single-stage OTAs are preferred in this project.

Among single-stage topologies, telescopic and folded cascode OTAs are most commonly used in low power applications.

The telescopic structures, like the one depicted in Fig. 15, are fast and can provide rather high *dc* gains with low power consumption. However, due to presence of a stack of five transistors, the output swing of a telescopic OTA is considerably limited. In addition, the maximum swing depends on input common-mode voltage range ($V_{cm,range}$):

$$\delta V_{outmax} = Vdd - 5V_{dsat} - V_{in-cm,range} \tag{30}$$

Therefore, despite their advantages, telescopic topologies can not be utilized in low-supply applications.

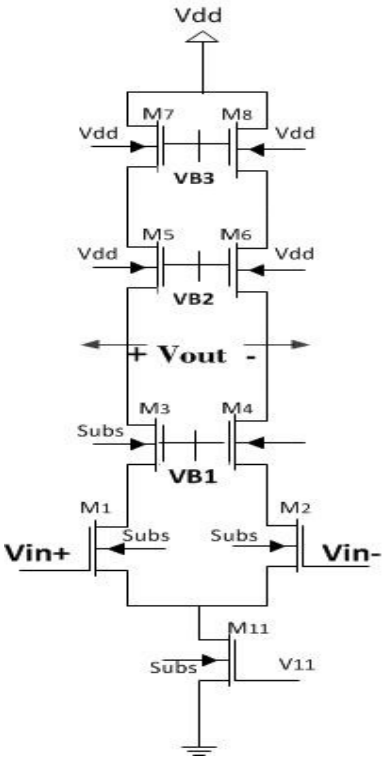


Figure 15: Telescopic OTA.

As shown in Fig. 16, the output swing of a folded cascode OTA is limited only by four transistors, which results in $V_{in-cm,range} + V_{dsat}$ improvement in output swing compared to telescopic structure:

$$\delta V_{outmax} = Vdd - 4V_{dsat} \tag{31}$$

Considering all above, folded cascode amplifiers seem to be an appropriate choice for the target data converter, since they can provide relatively high gain and output swing with low power consumption and complexity.

The gain of a folded cascode differential opamp is determined by the transconductance of its input pair transistors, g_{m1-2}, and output impedance of the amplifier, R_{out}:

$$A_v(0) = g_{m1} R_{out} \tag{32}$$

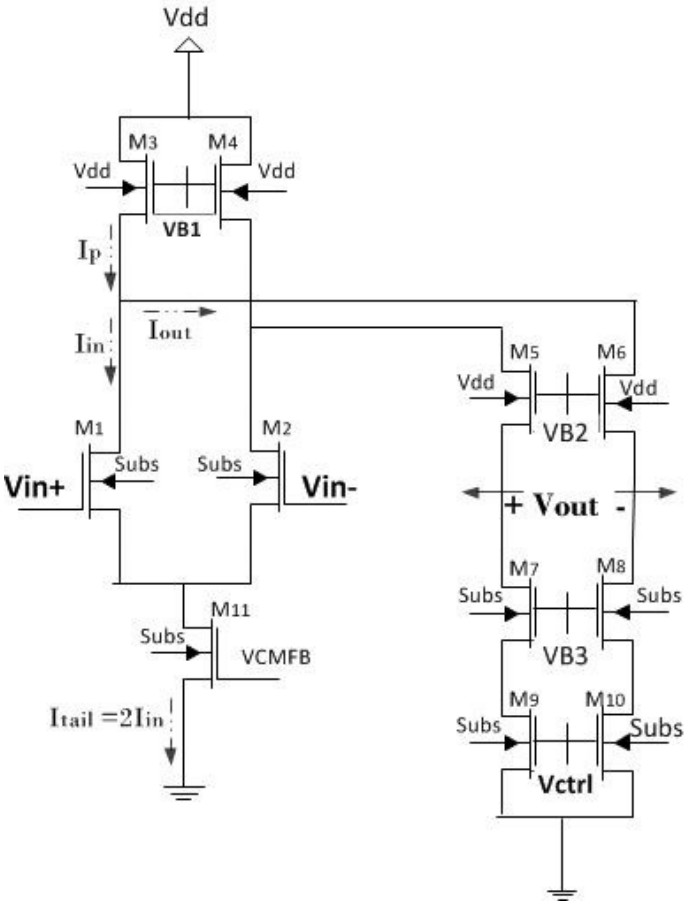


Figure 16: Fully differential folded cascode opamp.

$$R_{out} = \left(\frac{g_{ds6}}{g_{m6}}(g_{ds2} + g_{ds4}) + \frac{g_{ds8}}{g_{m8}} g_{ds10} \right)^{-1} \tag{33}$$

Furthermore, g_{m1} also affects the gain bandwidth product (GBW) , or equivalently ω_τ, of the folded cascode opamp:

$$GBW = \frac{g_{m1}}{C_{L,eq}} \tag{34}$$

where $C_{L,eq}$ is the equivalent load capacitance seen at the output of the amplifier.

Given the dependence of g_m and g_{ds} values on transistor currents, above equations imply that increasing the tail current (I_{tail}) improves the *dc* gain and GBW, whereas increasing the output current (I_{out}) leads to smaller R_{out} and thus lower gain. On the other hand, power consumption, which is the main concern in a low power application, is directly related to transistors currents. Furthermore, since I_{slew} is determined by the current through M_9 and M_{10}, usually the folded cascode amplifier is designed with equal bias currents for input and output stages [7]. In addition, the transconductance values can be optimized by appropriate transistor sizing.

Typically, the differential input pair transistors have the largest $\frac{W}{L}$ ratio in a folded cascode amplifier, since a large g_{m1-2} results in high gain and GBW, and lower noise contribution.

The MOS transistors used in the amplifier exhibit both thermal and flicker noise which can be expressed in terms of transistor properties and technology parmeters:[7]

$$V_n^2 = \frac{4KT\gamma}{g_m} + \frac{KF}{WLC_{ox}fK'} \tag{35}$$

where γ is a process-dependent noise excess factor, KF is the flicker noise coefficient, and f is the frequency.

The first term in (35) describes the thermal noise of the transistor, and the second term represents flicker noise. Now, one can easily see that flicker noise is reduced by increasing the size of the transistor, whereas thermal noise can be reduced by increasing the g_m. Furthermore, as it will be shown next, increasing $g_{m1,2}$ also reduces the input-referred noise of other transistors.

The total noise contribution of all the devices in an amplifier, is usually combined as a single noise voltage at the input of the amplifier. Assuming the noise sources to be uncorrelated, the total input-referred noise of the folded cascode amplifier of Fig. 16 can be calculated as below: [24]

$$V_{eq,in}^2 = 2(V_{n1}^2 + \frac{g_{m3}^2}{g_{m1}^2}V_{n3}^2 + \frac{g_{m9}^2}{g_{m1}^2}V_{n9}^2) \tag{36}$$

where V_{ni}^2 represents the noise produced by transistor M_i. Note that the noise of the cascode devices is omitted from above equation, since their noise voltage is transformed into current through the high output impedance of the underlying current source, thus it has negligible contribution to the overall noise [24].

Equation (36) clearly shows the prominent noise contribution of differential input pair, and indicates that overall noise can be minimized by increasing the transconductance of input transistors. However, this is only valid when the noise of the input pair dominates the total noise, thus there exists a limit above which increasing g_{m1} does not guarantee a reduction in total noise. Furthermore, a large g_{m1} requires either a large $\frac{W}{L}$ ratio or large I_{tail} which correspond to higher area, and power consumption, respectively.

An alternative approach in reducing the noise, is the use of PMOS input pair, given the fact that PMOS transistors typically exhibit less $\frac{1}{f}$ noise. Nonetheless, when thermal noise is a consideration, NMOS input pair is preferable.

Finally, it is worthwhile mentioning that a differential amplifier may not function properly, unless its output common-mode voltage ($V_{out,cm}$) is adjusted appropriately. In a folded cascode amplifier this is usually achieved by means of an external common-mode feedback (CMFB) circuit, which makes a feedback loop from amplifier's outputs to the gates of M_9 and M_{10}. The task of CMFB circuit is to detect the average of the amplifier's outputs, and force it to a predetermined value, by changing the bias of NMOS current source transistors, i.e. by manipulating V_{ctrl}.

CMFB circuits can be designed either with continuous-time(CT) or switched-capacitor approach. The latter is more common in SC circuits, since using a CT CMFB limits the signal swing and may cause nonlinearity.

Fig. 17 shows a switched capacitor CMFB circuit. In this circuit, C_1 generates the average of the output voltages, which is used to create the required control

voltage, V_{ctrl}. The *dc* voltage across C_1 is determined by capacitors C_2, which are switched between nodes of C_1, and two fixed bias voltages, V_{ref} and V_{cmfb}. Hence, the difference between these bias voltages should be designed to be equal to the difference between desired output common-mode level and V_{ctrl}. Here, the size of the capacitors does not affect the CMFB transfer function, but using too small capacitors causes common-mode offset voltage due to the presence of parasitic capacitors, and also switch charge injection. On the other hand, excessively large capacitors may overload the opamp. Therefore, normally C_2 is designed to be within one-quarter to one-tenth of C_1 [7].

Here one should note that, unlike two-stage OTAs, the folded cascode amplifier does not utilize a compensation capacitor, and it stabilizes merely with the load capacitor. Therefore, the input capacitance of all blocks connected to the amplifier's output should be taken into account when designing the amplifier.

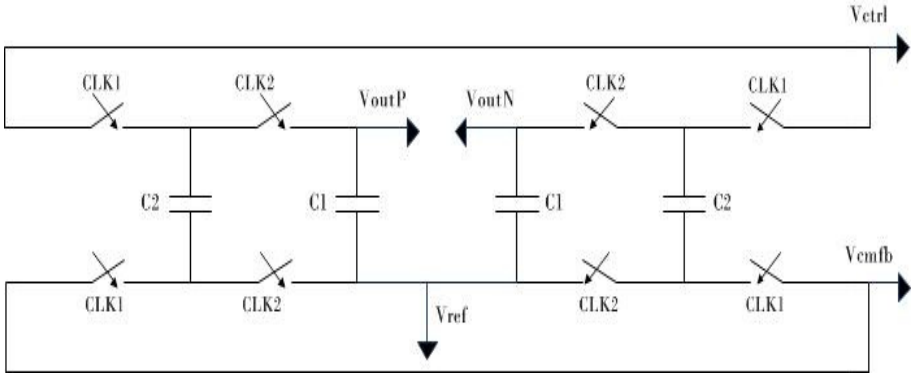


Figure 17: Common-mode feedback circuit.

2.3.3 Quantizer

A one-bit quantizer can be implemented as a comparator whose output toggles between high and low voltage levels, V_{OH} and V_{OL}, based on the polarity of its differential input voltage.

In contrary to other (non-oversampling) types of ADC, comparator design is a minor issue in delta-sigma modulators, because these converters are extremely robust against most comparator imperfections [**?**],[25]. Therefore, many comparator architectures are potentially capable of satisfying the requirements of a delta-sigma ADC. However, since investigation of all existing comparator architectures is beyond the scope of this report, here we limit our discussion to open-loop comparators which are one of the most commonly used structures in delta-sigma ADCs.

Alike integrators, comparators must satisfy both static, and dynamic requirements. As the names imply, static characteristics deal with *dc* performance of the comparator, i.e. gain, input resolution($V_{in}(min)$), and output voltage levels, whereas dynamic characteristics such as slew rate and propagation delay(t_p) describe the transient operation of the comparator.

Input resolution is the minimum input voltage which can be accurately resolved by the comparator, and is a function of amplifier's gain, whereas propagation delay(Fig. 18) is the time it takes for the comparator to completely resolve the input voltage, and thus depends on comparator's slew rate:

$$V_{in}(min) = \frac{V_{OH} - V_{OL}}{A_v(0)} \tag{37}$$

$$t_p = \frac{V_{OH} - V_{OL}}{2SR} \tag{38}$$

Equations (37) and (38) are valid for any comparator architecture; however, the exact relationship between circuit parameters and performance of the comparator can not be derived without specifying the structure.

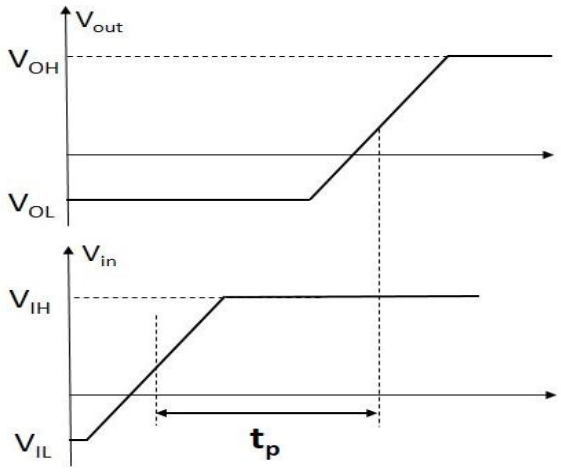


Figure 18: Propagation delay of a comparator.

An *open-loop* comparator uses a high-gain stage to drive its outputs between V_{OH} and V_{OL} voltage levels for small changes in the input voltage. Hence, a two-stage op amp without compensation is an excellent implementation of a high-gain, open-loop comparator.

For the two-stage opamp depicted in Fig. 19, $V_{OL} = Vss$, and V_{OH} is roughly determined by the saturation voltage of transistor M_6. Furthermore, the *dc* gain can be calculated as follows:

$$A_v(0) = (\frac{g_{m1}}{g_{ds2} + g_{ds4}})(\frac{g_{m5}}{g_{ds5} + g_{ds6}}) \tag{39}$$

Therefore, to achieve a higher gain, and subsequently better resolution, smaller currents and larger transistors should be used. This, however, decreases the current driving capability of the comparator, and subsequently results in a lower slew rate. In contrary, higher comparator gain decreases the non-slew propagation delay:[26]

$$t_p \approx \sqrt{\frac{V_{OH} + V_{OL}}{mA_v(0)V_{in}}} = \sqrt{\frac{V_{in}(min)}{mV_{in}}} \tag{40}$$

where m is the ratio of amplifier poles, i.e. $\frac{p_2}{p_1}$.

Here, one should note that Equation (40) is valid as long as the slope of the linear response does not exceed the slew rate; otherwise, slewing will dominate. This usually occurs for large load capacitances.

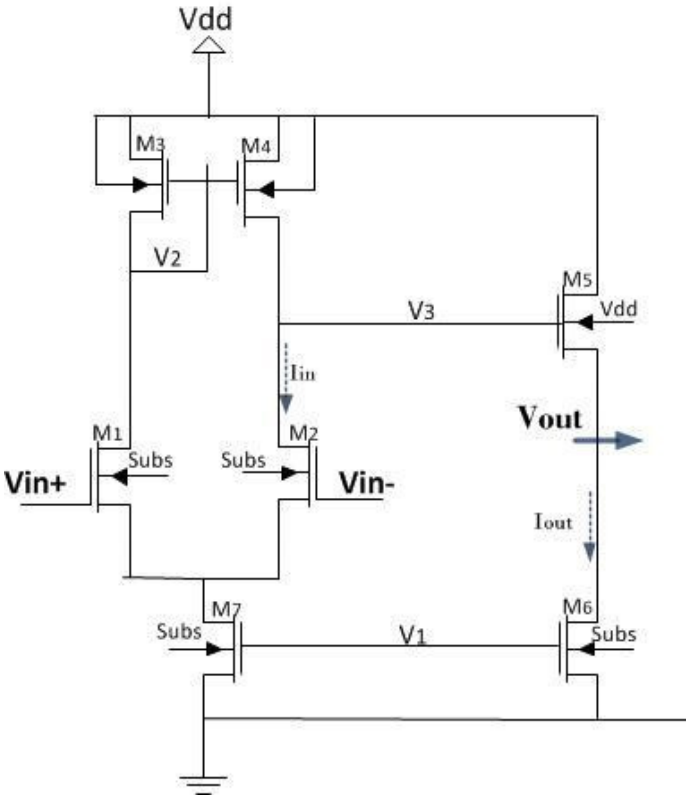


Figure 19: A two-stage opamp.

The two-stage opamp described above is quite simple in operation, and thus can be designed so that it fulfills both resolution and timing requirements of the target ADC without consuming much power. This will be discussed in more details in section 3.3.3

2.3.4 Decimation Filter

As shown in Fig. 20, a *sinc* filter can be realized using a counter and a register. Clearly, it is then possible to build up a $sinc^K$ filter by simply cascading K *sinc* filters. However, in practice, alternative approaches are used to achieve more economical structures. For instance, Fig. 21 depicts a hardware-efficient $sinc^2$ filter, which is made especially simple if N is assumed to be a power of 2. In this filter, the *sinc* filter generates the rectangularly-weigthed sums, while the ramp-weighted sums are generated by conditionally accumulating the output of a counter which wraps to zero every N cycles. The filter output is then an arithmetic combination of these intermediate sum. [12]

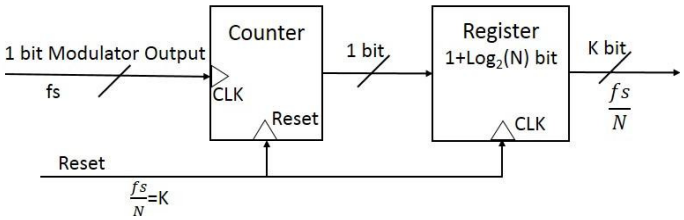


Figure 20: Block diagram of a *sinc* filter.

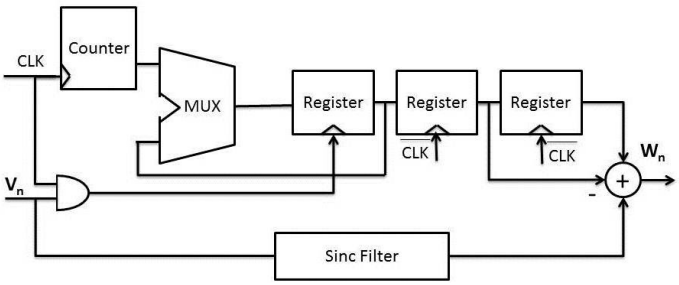


Figure 21: Block diagram of a hardware-efficient $sinc^2$ filter.

The above description of decimation filters, brings us to the end of chapter 2. In following sections, the design procedure of target delta-sigma ADC is described.

3 Design Description

3.1 System-Level Design

The incremental delta-sigma analog-to-digital converter presented in this thesis is responsible for providing an ultra-low power interface for a built-in temperature sensor in an energy harvesting system. The ADC receives the analog output of a temperature sensor and modulates it to digital codes which are filtered by a decimation filter, and finally fed to a display driver (Fig. 22). In this application, the ADC is required to have a minimum accuracy of 14 bits with 16-bit resolution, and its maximum bias current must be limited to 1 μA in order to comply with the stringent power constraints of the energy harvester. On the other hand, temperature changes are quite slow and the output of the temperature sensor is virtually *dc*, thus there is no need for large bandwidth or high speed. Considering these criteria, an incremental delta-sigma converter is an appropriate choice due to its accuracy and low average power consumption.

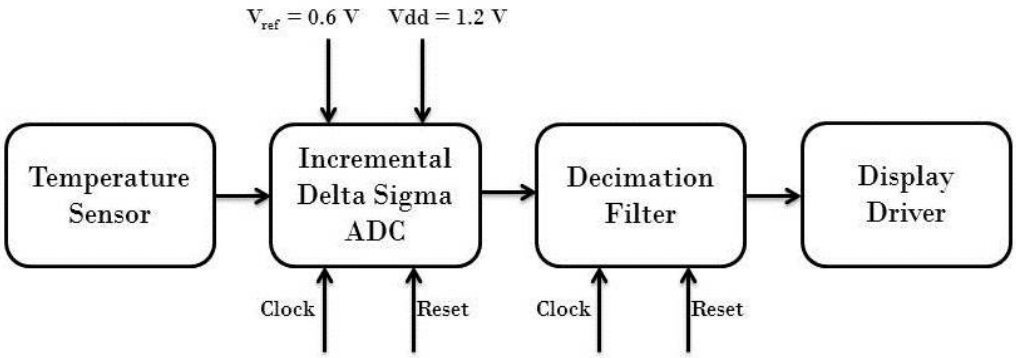


Figure 22: The delta-sigma ADC in the target application.

It was mentioned before that implementing an adjustable reset helps increasing the accuracy, and reducing the power consumption. Nonetheless, given the fact that reset frequency is determined by digital circuitry, and design of digital blocks is not covered in this work, throughout the thesis a constant number of cycles, M, is used in all simulations. The optimum M is defined based on ADC's transfer function, and thus depends on loop coefficients as well as the topology of the ADC.

In this thesis, a second order CIFB modulator is used to ensure stability for the whole input range ($V_{in,range}$), while satisfying the application requirements listed in Table 1. Higher order modulators are avoided, due to their limited stability and higher power consumption. On the other hand, as discussed in section 2.2, first order modulators require a considerably longer conversion time for the same accuracy, and their inevitable idle tones may degrade the performance significantly. Therefore, the choice of a second order modulator is justified according to stability, accuracy, and power consumption requirements. Furthermore, given the fact that both zeros of a second-order NTF fall at dc, the ADC utilizes a CIFB topology to minimize the power consumption, and improve the stability.

Table 1: ADC Specifications

Resolution	16 bit
Absolute Accuracy	14 bit
Clock Frequency	5 kHz
Supply Voltage	1.2 V
Maximum Current	1 μA (active)
Maximum $V_{in-diff}$	850 mV
Input Frequency	Virtually dc

Fig. 23 shows the block diagram of designed ADC, which consists of two switched capacitor integrators realizing the loop filter, a comparator, and a DAC circuit.

In order to find the appropriate loop coefficients that can fulfill the requirements of the ADC with a minimum number of cycles, extensive MATLAB simulations were performed using the mathematical model of the second order CIFB ADC, derived by MATLAB delta-sigma toolbox. Simulation results showed that by using $M = 436$, it is possible to achieve 15-bit accuracy with the loop coefficients listed in Table 2. This was also verified by circuit-level simulations in Eldo, in which the ADC was realized using ideal SC integrators.

As discussed in section 2.3, the loop coefficients determine the capacitor ratios in the SC integrators, and absolute capacitor values should be calculated based on C_{min}, which is the minimum allowable capacitor size dictated by noise requirements of the circuit.

Table 2: Loop Coefficients

a_1	a_2	b_1	c_1	c_2
0.144	0.512	0.071	0.909	1

Assuming 14-bit absolute accuracy and an oversampling ratio of 436, the desired SINAD calculated from (5) is 86.04 dB, and given $|V_{in-max}| = 850\ mv$, the upper

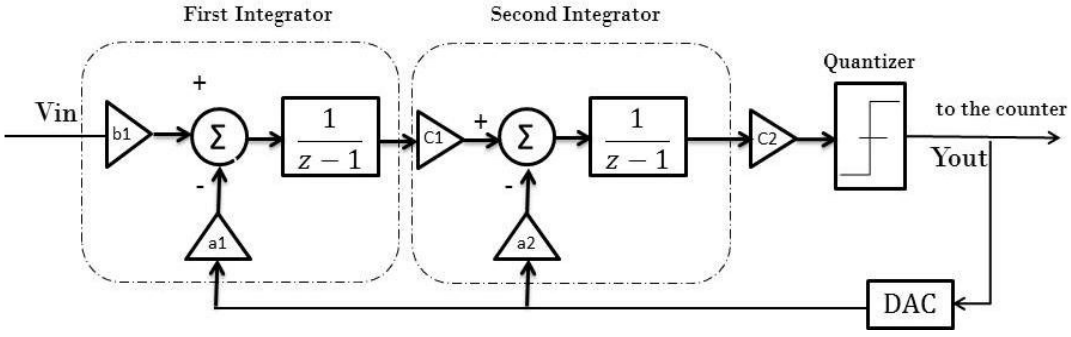


Figure 23: The block diagram of designed delta-sigma ADC.

noise limit is determined as below:

$$v_n^2 < 10^{-0.1SINAD} * \frac{V_{in-max}^2}{2} = 9.074 * 10^{-10} \tag{41}$$

The minimum capacitor size can then be calculated based on equation (21):

$$C_{min} = \frac{2KT}{OSR.v_n^2} = 20.95\ fF \tag{42}$$

where K and T are defined as in (21), and the factor 2 is due to presence of two switched capacitor branches in each integrator.

Above equation indicates that with capacitors larger than 20.95 fF, the modulator can achieve 14-bit accuracy. However, considering the amplifier noise, temperature changes, layout inaccuracies and capacitor mismatches in the actual circuit, the smallest capacitor should be larger than C_{min} to compensate for the added noise. Therefore, in this design a minimum capacitor size of 72 fF is chosen, which corresponds to approximately 5 dB increase in SNR.

One should note that, in practice, the capacitors of each integrator are implemented as a matrix of equally-sized unit capacitors (C_{unit}), thus arbitrary coefficients may not be realizable with a feasible number of unit capacitors. Therefore, as it will be shown in following section, the coefficients are rounded so that the matrix is realized with a minimum number of capacitors, while maintaining the accuracy.

3.2 Circuit-level Design

Fig. 24 shows the schematic of the designed ADC, and Fig. 25 illustrates the clock signals used in the circuit. The converter is realized with a fully differential structure so that common-mode errors, as well as noise and even-order harmonics are eliminated. The differential input voltage varies from $-850\ mV$ to $+850\ mV$ around a common-mode voltage of 600 mV, and the D-flipflop output is either Vss or Vdd. In this design, a reference voltage of 600 mV (V_{ref}) and Vss are used as feedback signals, and the DFF output is used as a select signal which connects either V_{ref} or Vss to the feedback capacitor by turning on the corresponding switches (DAC).

Each integrator consists of an amplifier and two SC blocks which realize the feedback and input path coefficients. In addition, the first integrator utilizes chopper stabilization to remove the amplifier input dc offset and reduce the low-frequency noise.

To implement the switched capacitor blocks, the unit capacitor previously computed in section 3.1, is realized using a $4.3 \cdot 4.3\ \mu m^2$ capacitor, which results in $C_{unit} = 35.91\ fF$. Besides, the initial coefficients of Table 2 are rounded so that each capacitor is an integer multiple of C_{unit}. Finally, the integrating capacitors, i.e. $C_{1,2}$ and $C_{11,12}$ are set to $28 \cdot C_{unit}$ and $10 \cdot C_{unit}$ respectively, and the other capacitor sizes are computed accordingly. Table 3 shows the resulting capacitor sizes along with final coefficients and their relative errors.

In order to define the amplifier minimum requirements, the ADC was simulated with opamp macromodels in Eldo, and the effects of opamp dc gain, and GBW

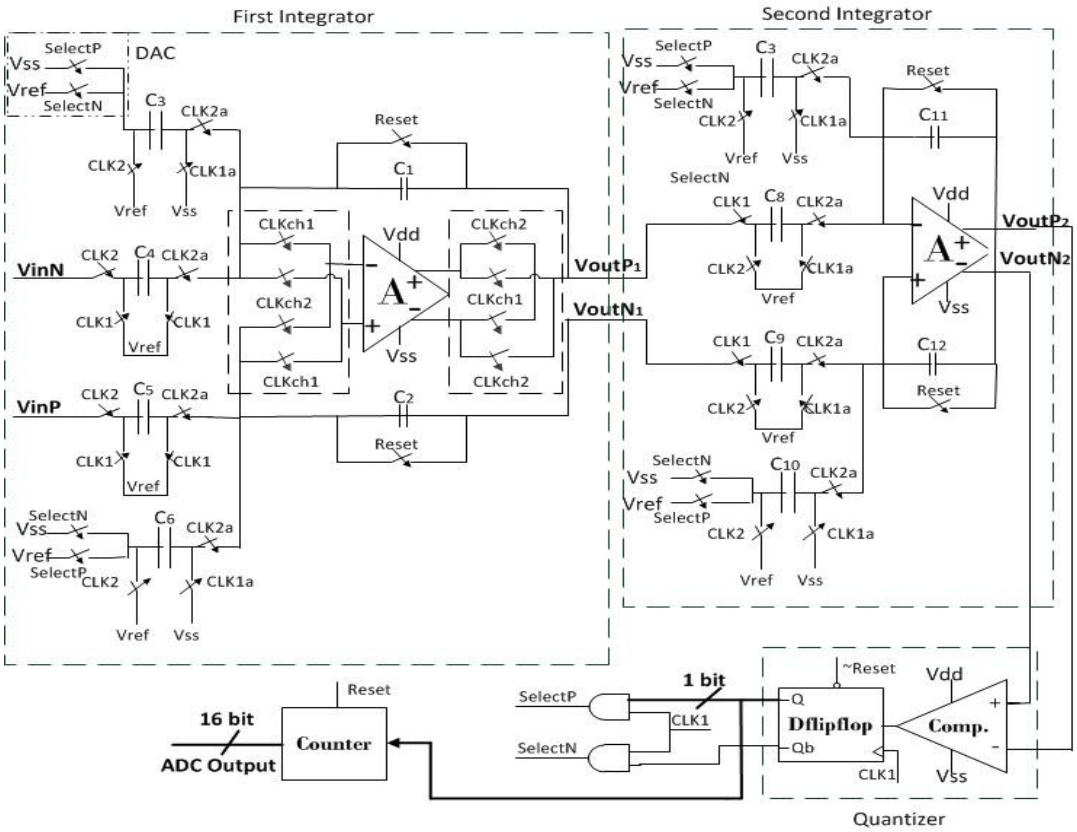


Figure 24: Circuit-level block diagram of designed ADC.

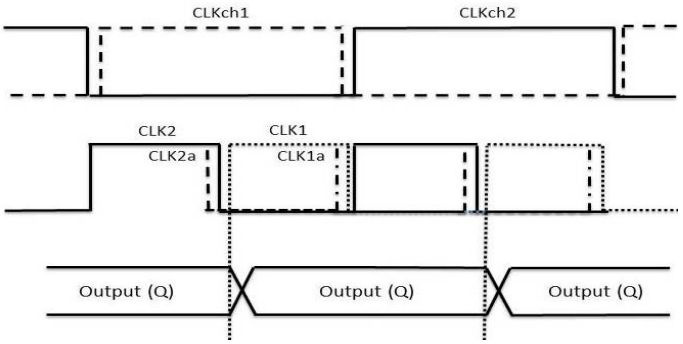


Figure 25: Clock signals implemented in designed ADC.

Table 3: Capacitor Values

	Initial	Implemented	Error(%)	Capacitor Size (C_{unit})	Integrating Capacitor Size (C_{unit})
b_1	0.07123	0.07142	0.27	2	28
a_1	0.14425	0.14286	−0.96	4	28
c_1	0.90909	1.0	10	10	10
a_2	0.51658	0.5	3.21	5	10

variations were studied. Simulation results showed that for the amplifier gains lower than 75 dB, the in-band quantization noise increases substantially, but the total harmonic distortion stays approximately unchanged (Fig.26). On the other hand, the amplifier's GBW affects both the noise and harmonic distortion, and with GBW values less than 100 kHz the ADC can not meet the accuracy requirements (Fig. 27). These simulations imply that the effects of amplifier's finite gain and bandwidth is acceptably small, when the opamp dc gain is over 75 dB, and its GBW is higher than 100 kHz, i.e. 20 times clock frequency. However, to keep some margin, larger gain and GBW requirements were set for the actual design.

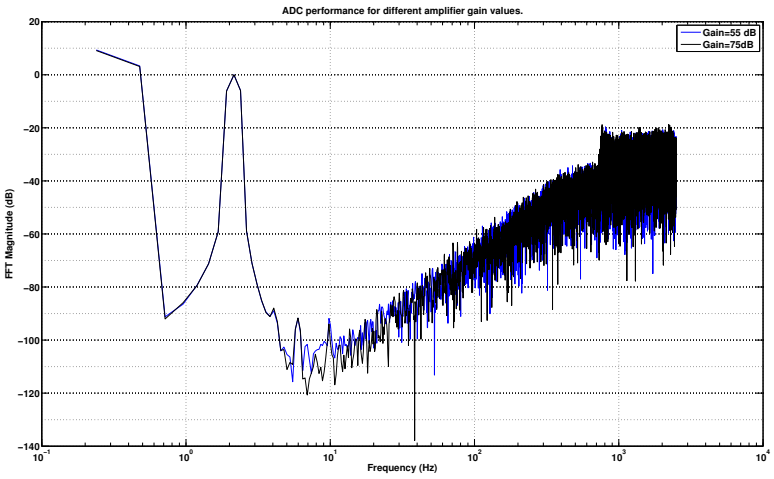


Figure 26: ADC output spectrum for different amplifier dc gain values.

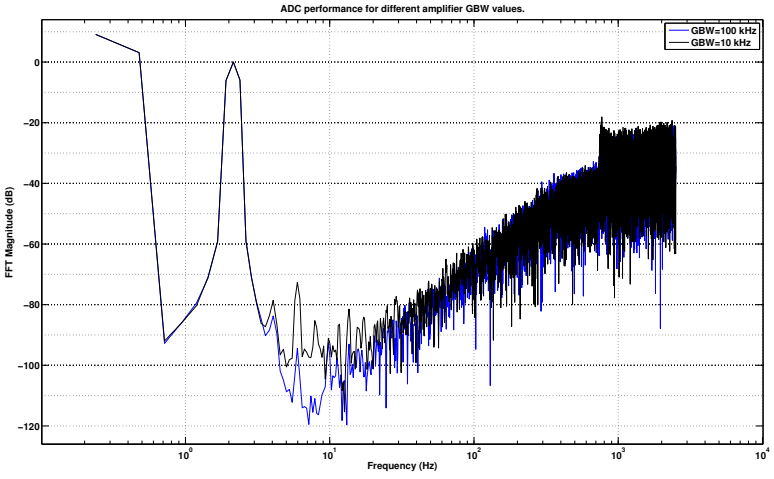


Figure 27: ADC output spectrum for different amplifier GBW values.

As discussed in section 2.2.1, the overall performance of a delta-sigma ADC is primarily determined by the integrators, and the quantizer non-idealities do not

affect the circuit significantly. Nonetheless, power consumption as well as maximum speed of the converter depend on the quantizer properties. In present design, the propagation delay of the quantizer and its maximum bias current are required to be less than 10 μs and 100 nA respectively.

To achieve the above mentioned criteria, both for the integrators and the quantizer, several considerations should be taken into account. These considerations are described in upcoming sections.

3.3 Transistor-Level Design

3.3.1 Amplifier

Fig. 28 shows the amplifer designed in present work together with its bias circuit. The amplifier has a fully differential folded cascode topology, and utilizes an NMOS input pair ($M_{1,2}$) to achieve the required gain with smaller input transistors and subsequently lower input capacitance. Furthermore, the input pair is large and is biased in deep subthreshold region to optimize $\frac{g_m}{I_{out}}$. The amplifier is biased with

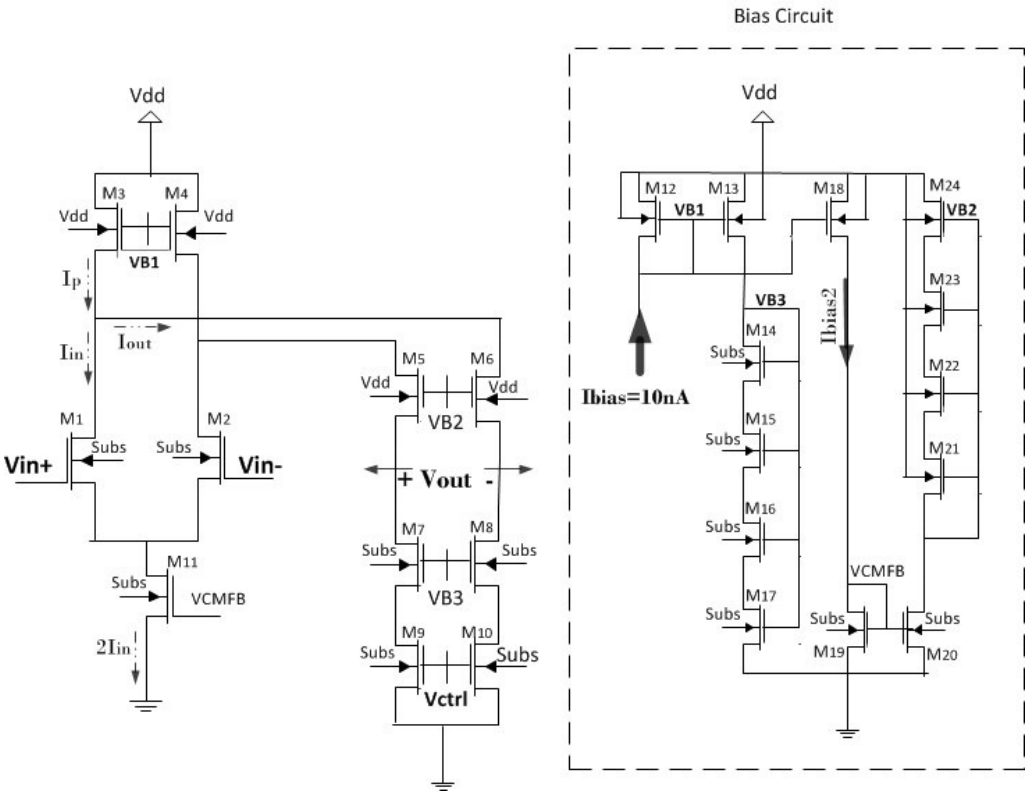


Figure 28: The differential folded cascode amplifier.

3 interrelated current mirrors: The first current mirror which is formed by the tail transistor (M_{11}), and M_{19}, determines the *dc* current through the input pair (I_{in}). Second current mirror consists of PMOS current source transistors ($M_{3,4}$) and M_{12}, and it mirrors the input bias current to produce I_p. Finally, transistors M_9 and M_{10} are sized in a way that they build up a virtual current mirror with M_{19}. The term

virtual arises from the fact that the gates of $M_{9,10}$ are not directly connected to M_{19}; rather, as it will be shown later, V_{ctrl} and V_{cmfb} are connected via a switched capacitor in the common-mode feedback circuit. In fact, given that the current through cascode devices (I_{out}) is fixed by the difference between I_p and I_{in}, the virtual current mirror helps adjusting the output common-mode level by pushing V_{ctrl} towards V_{cmfb}.

The three current mirrors described above, have two common characteristics: first, the transistors in each current mirror are realized with the same length, and current multiplication is achieved only by adjusting the number of equally-sized fingers so as to minimize V_{th} mismatches in mirror transistors. Second, all current mirror transistors are long channel with lengths larger than or equal to 5 μm. The use of same lengths in a current mirror is justified, since due to considerable dependence of V_{th} on transistor length, a linear current multiplication can not be obtained from two transistors with inequal lengths. Besides, utilizing large-channel transistors helps minimizing V_{th} and g_{ds} changes.

Before calculating the mirroring ratios, the current through each branch should be determined. Considering the direct relationship between bias current and transconductance of transistors, larger I_{in} and I_p are generally preferred, as they lead to larger *dc* gains. Moreover, since the amplifier's load is purely capacitive and timing requirements are not stringent, I_{out} can be minimized to reduce the overall power consumption. Therefore, in this design, roughly 35 nA of total 400 nA current is allocated to I_{out}, and the rest is distributed according to table 4.

Table 4: Transistor currents and current mirror ratios in designed amplifier.

	Current(nA)	Mirroring Ratio	Bias Transistor
I_{in}	246.6	16	M_{19}
I_p	156.5	16	M_{12}
I_{out}	33.2	2.5	M_{19}
I_{bias2}	15	1.5	M_{12}

As shown in Fig. 28, the bias circuit also provides the bias voltage of cascode transistors, i.e. $M_{5,6}$ and $M_{7,8}$. As mentioned in section 2.3.2, the output swing of the amplifier is limited by V_{ds-sat} of cascode transistors which is partly determined by VB_2 and VB_3 . Thus, the swing can be maximized by using large VB_2 and small VB_3. This, however, reduces the overdrive voltage of cascode transistors, and can push the transistors out of saturation.

Simulation results showed that by setting VB_2= 650 mV and VB_3 = 550 mV, an output swing of $\pm$275 mV can be reached. However, these bias voltages can not be simply realized by a single diode-connected transistor, since a transistor biased with $V_{GS} \approx 600\ mV$ should have an impractically small $\frac{W}{L}$ ratio in order not to consume a large *dc* current. On the other hand, a cascode bias circuit can not be used either, since it requires extraordinary large $\frac{W}{L}$ ratios. Therefore, two stacks of NMOS and PMOS transistors, i.e. $M_{14} - M_{17}$ and $M_{21} - M_{24}$ are used to produce VB_3 and VB_2 respectively.

Finally, the output common-mode voltage of the amplifier is fixed by means of the common-mode feedback circuit depicted in Fig. 17. As explained before, in each clock cycle the switched capacitor of CMFB circuit (C_1) forces $V_{out}-V_{ref}$ to be equal to $V_{ctrl}-V_{cmfb}$, hence the output common-mode level is, in fact, determined by V_{ctrl}. This clarifies the reason behind building the virtual current mirror discussed above.

Considering the significant role of the amplifier in accurate performance of the ADC, numerous simulations were carried out in order to evaluate the amplifier's behavior thoroughly.

First of all, *ac* simulations were performed, so that the amplifier's gain, GBW, phase margin, and also gain margin could be calculated. Meanwhile, bias currents and voltages were monitored by running a *dc* operating point simulation. These simulations were carried out in three different temperatures and in all design corners to analyze the effects of temperature, as well as fabrication-induced non-idealities on amplifier's performance. One should note that *ac* analysis can not be done with a switched capacitor CMFB, hence in *ac* simulations the output common-mode level is adjusted using three ideal voltage-controlled voltage sources, which produce the required V_{ctrl} voltage for the amplifier. It will be shown later that using a SC CMFB circuit does not affect the opamp's characteristics, and thus the *ac* simulation results are valid. In addition, it's worthwhile mentioning that GBW and subsequently phase margin of the amplifier depend on the load capacitance, hence the load capacitor used in simulations should be equal to the actual capacitance seen at the output of each integrator during sampling. This capacitance can be found using equation (29), and capacitor values in Table 3, which yield $C_{L1} = 778\ fF$ and $C_{L2} = 810\ fF$.

Fig. 29 depicts the magnitude and phase of the amplifier's transfer function obtained from *ac* simulations in $-40°C$, $27°C$, and $85°C$. It can be clearly seen that opamp's gain degrades at high temperatures, whereas its GBW stays unchanged. This is caused by an increase in I_{out} which is due to smaller V_{th} and subsequently larger V_{ov} values at high temperatures, and it's thus inevitable. On the other hand, simulation results obtained from *ac* noise analysis imply that input-referred noise of the amplifier is merely a function of temperature, and does not vary significantly over design corners.

In addition to temperature and process corners, device mismatches also affect the opamp's performance. This can be seen via Monte Carlo (MC) simulations, in which the opamp is simulated in multiple rounds with random parameter variations. Fig. 31 shows the result of MC *ac* simulations at three different temperatures mentioned above. The results show a considerable gain and bandwidth variation over 600 rounds of simulation. The situation is also similar in noise analysis, where MC simulations indicate a ten-fold increase in flicker noise , and roughly 250 % increase in thermal noise from the best design point to the worst one (Fig. 32). Here it should be pointed out that, the change in thermal noise is mostly due to the temperature changes, from nominal $27°C$ to $85°C$, and the mismatch-induced thermal noise variation is negligible. In contrary, the large variation in flicker noise does not arise from temperature changes. On the other hand, the variations in oxide thickness, flicker noise coefficient or transistor dimensions can not cause a ten-fold increase in flicker noise. Therefore, the reason behind this noise behavior should be

sought in the simulator noise models, and analysis methods.

After all, as shown in Table 5, the worst-case characteristics of the opamp still meet the design requirements, thus it does not degrade the overall performance of the ADC.

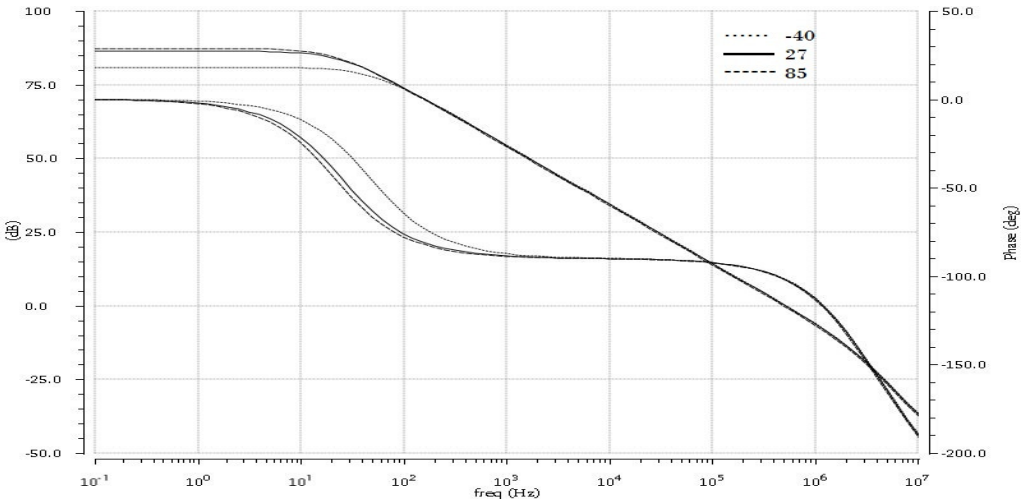


Figure 29: Opamp transfer curve in different temperatures, with $C_L = 800\ fF$.

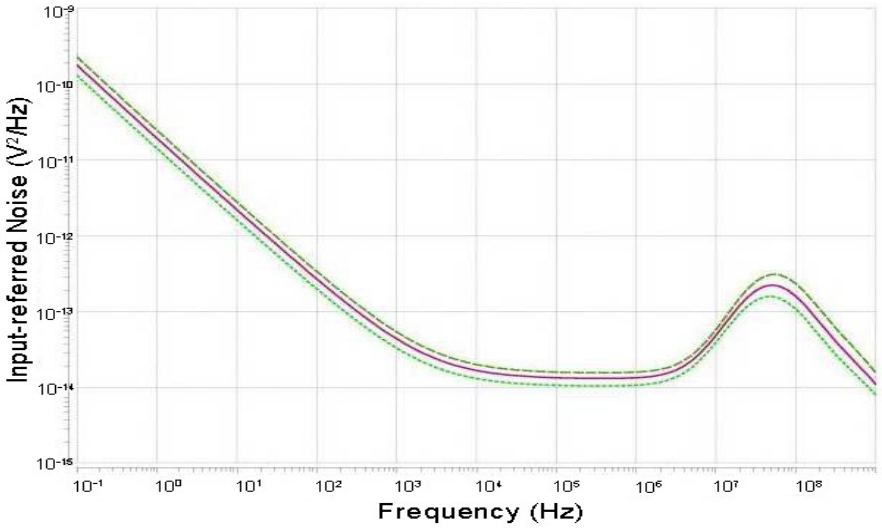


Figure 30: Input-referred noise of the amplifier in different temperatures.

Apart from *ac* characteristics, one can also extract the opamp's *dc* offset by means of MC simulations. To find out the offset, the opamp is connected in a unity feedback configuration, and the differential *dc* output voltage is observed via *dc* analysis in MC environment.

As shown in Fig. 33, in about 50% of simulation points, designed amplifier exhibits an offset lower than 1.5 mV, whereas in 5% of simulations the offset exceeds 4.5 mV. This offset, however, does not cause significant errors in the converter, since in the first integrator it is nullified through the chopper, and in the second integrator

Table 5: Amplifier characteristics in nominal and worst-case conditions.

	Nominal	Worst Case	Required
Gain(dB)	86.2	78.01	75
GBW(kHz)	520.9	499.9	100
PM($^\circ$)	78.08	77.86	60
GM(dB)	32.52	31.91	30
$I_{tot}(nA)$	364.6	465.5	400
Corner Frequency(kHz)	3.9	39.8	$--$
Thermal noise ($\frac{V}{\sqrt{Hz}}$)	114.5 n	124.6 n	$--$

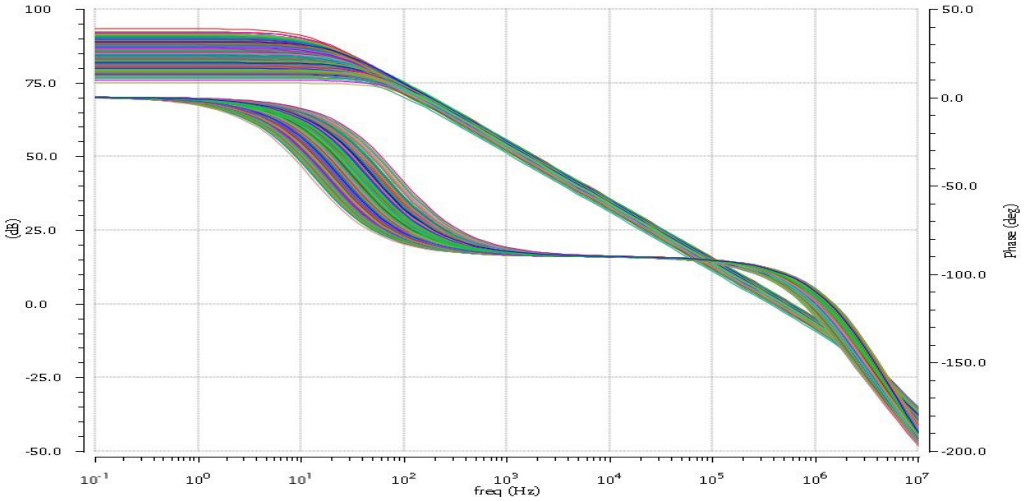


Figure 31: Opamp transfer curve in Monte Carlo simulations.

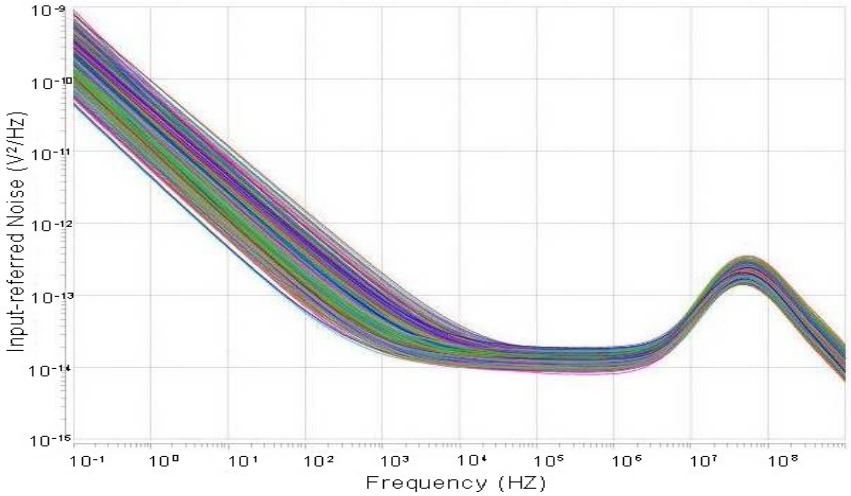


Figure 32: Input-referred opamp noise in Monte Carlo simulations.

it is attenuated by the first integrator's gain. In addition, the offset is small enough to keep the amplifier input voltages in the allowed range.

Finally, a transient simulation is carried out to analyze the switched capacitor

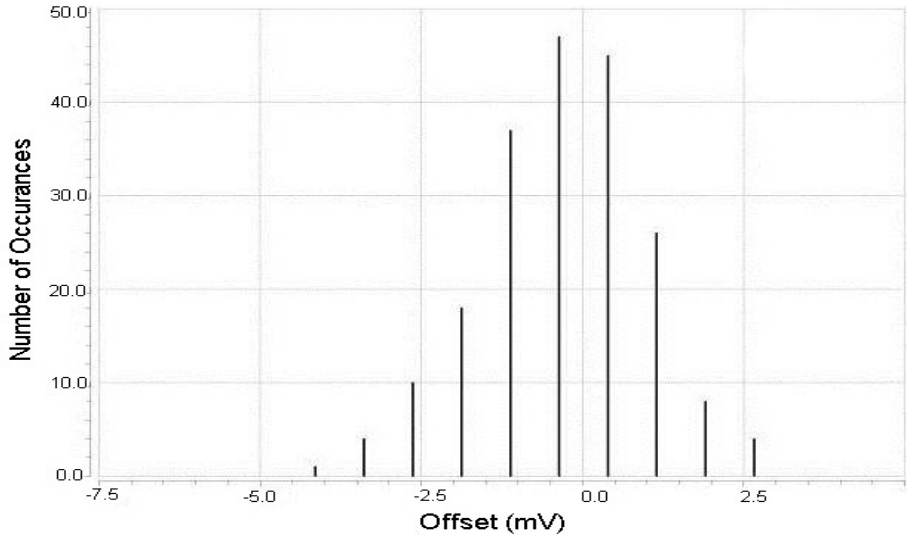


Figure 33: Opamp offset variation in MC simulations.

CMFB circuit. In this simulation, a differential step voltage of 1 μV is applied to the amplifier, and output settling is observed (Fig. 34). One can see that, in nominal situation, the output common-mode level reaches its final value, i.e. 590 mV, in less than 3 ms, which contributes to roughly 3 % increase in the total conversion time. In addition, the 10 mV deviation of the final common-mode value from the desired level can be easily handled by the amplifier, provided that the output swing is adjusted accordingly. Here, it should be pointed out that, this deviation cannot be eliminated since it results from the difference between V_{ctrl} and V_{cmfb}, which is caused by the mismatch between the current through $M_{9,10}$ and M_{19}.

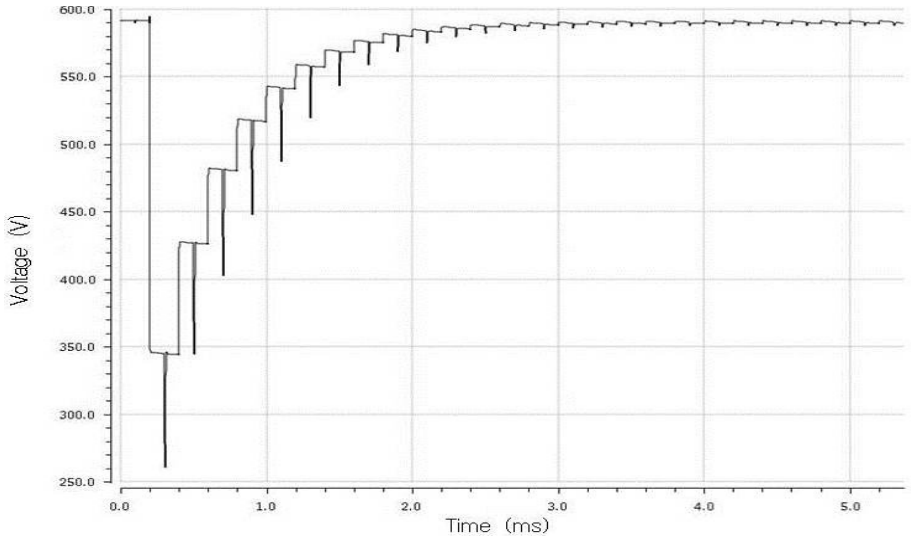


Figure 34: Common-mode settling of amplifier's output.

3.3.2 Switches

In the delta-sigma converter shown in Fig. 24, the switches are incorporated in four main building blocks: amplifiers' common-mode feedback, choppers, DAC, and switched-capacitor blocks.

Undoubtedly, the switches in the SC blocks are the most critical, since their nonlinear behavior directly affects the integrators outputs, and can cause severe harmonic distortion. In the input signal path, where the largest signal swing occurs, the switches must be realized with transmission gates to avoid signal clipping. Furthermore, in order to reduce the signal-dependent leakage and charge injection, the transistors must be sized in a way that PMOS and NMOS contributions cancel out, and an acceptable compromise is found between charge injection and leakage. On the other hand, the charge injection of the switches connected to the reference voltage does not contribute significant error, thus small NMOS transistors are used to minimize the leakage.

The DAC switches may also introduce errors in the converter, since the voltage across them and subsequently their leakage and charge injection is a function of quantizer output. However, since these switches are either connected to V_{ref} or V_{ss}, their non-ideality does not affect the modulator's linearity. This also applies to Reset, and chopper switches which experience approximately the same voltage in every clock cycle.

The requirements on the CMFB switches are even more relaxed, since the non-idealities in the CMFB produce common-mode errors, which are attenuated by amplifiers common-mode rejection ratio.

Considering all above, a number of simulations were performed on transmission gates as well as NMOS switches with different dimensions to find out the most appropriate switch for each block. Finally, given the more prominent effect of charge injection compared to leakage, the DAC and chopper, as well as the Reset switches were realized with transmission gates with $(\frac{W}{L})_n = \frac{250\ nm}{360\ nm}$ and $(\frac{W}{L})_p = \frac{370\ nm}{360\ nm}$. The same transmission gates are also implemented in the switched-capacitor blocks, but the switches connected to V_{ref} are realized with a single NMOS switch with $(\frac{W}{L}) = \frac{250\ nm}{360\ nm}$. Finally, the CMFB circuit is built up of rather larger transmission gates with $(\frac{W}{L})_n = \frac{1\ \mu m}{180\ nm}$ and $(\frac{W}{L})_p = \frac{1.44\ \mu m}{180\ nm}$.

3.3.3 Quantizer

Unlike switched-capacitor integrators, comparator design is not a critical issue in one-bit delta-sigma converters. Therefore, in present work the main focus is on minimizing the power consumption of the comparator, while providing a moderate gain and speed. As stated in Table 6, the comparator is required to deliver a minimum dc gain of 60 dB with a supply current less than 100 nA, to ensure that the total supply current of the ADC does not exceed 1 μA.

Alike the opamps, the designed comparator depicted in Fig. 35 also has a 10 nA bias current, which is mirrored to the input and output branches via transistors M_7 and M_6 respectively. In order to reach the desired gain and speed with minimum power consumption, the mirroring ratios have been designed so that in nominal

conditions $I_{in} = 3.8\ nA$ and $I_{out} = 47\ nA$. Undoubtedly, the current distribution changes with temperature and process variations, leading to a change in gain and power consumption; thus in initial design some margins are left for all comparator parameters to guarantee an acceptable performance under different operating conditions.

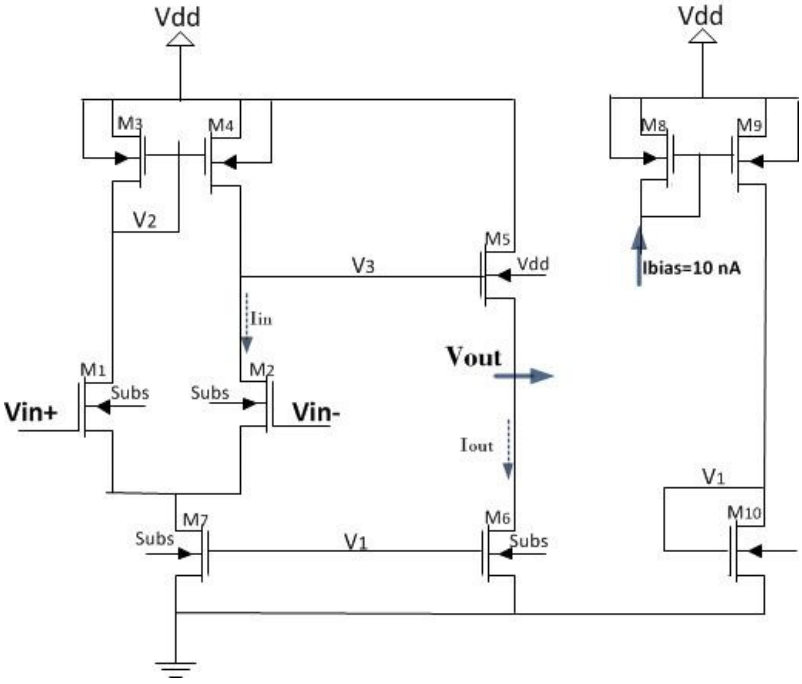


Figure 35: The comparator and its bias circuit.

The gain and bandwidth of the comparator are measured via *ac* analysis, and its power consumption is determined from a *dc* operating point simulation. Table 6 shows the parameters obtained from nominal and Monte Carlo analysis performed in different temperatures, compared to design requirements. The data indicate that despite the considerable variance of comparator's parameters, the worst-case characteristics still satisfy the modulator requirements.

Here, it should be pointed out that, the stability measures such as gain and phase margin are not important in comparator's performance, since it operates in open-loop configuration. In fact, a comparator is typically characterized by its transient step response rather than frequency-domain performance. Therefore, the designed comparator was simulated with different input step voltages and its propagation delay was extracted. Simulation results indicate that the propagation delay is higher than 100 μs for input voltage steps smaller than 1 mV. This, however, does not degrade the ADC's performance considerably, since the comparator errors are shaped by the loop filter. Furthermore, the propagation delay decreases dramatically, as the input step exceeds 2 mV. In other words, the maximum input step size, for which the propagation delay is above 100 μs, V_{inMax}, is limited to 1.8 mV in the worst corner. Fig. 36 depicts the comparator's output in response to a 1 mV step voltage at 200 μs, and Table 6 lists the comparator characteristics in nominal and worst-case

conditions.

Table 6: Comparator characteristics in nominal and worst-case conditions.

	Nominal	Worst Case	Required
Gain(dB)	91.2	68.3	60
BW(Hz)	65.3	52.2	45
Supply Current($n\ A$)	71.5	101.2	100
$V_{inMax}(mV)$	1	1.8	–

Note: Worst corner is different for each parameter.

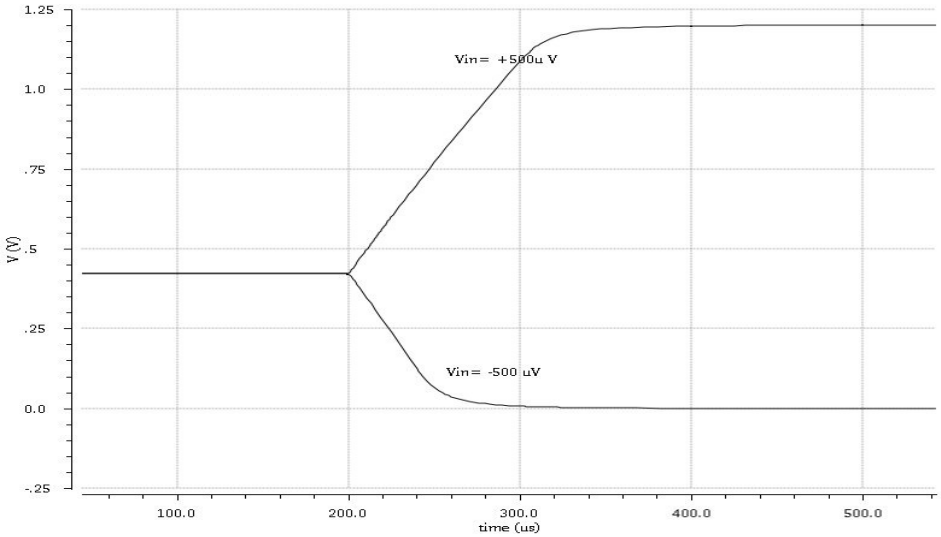


Figure 36: Comparator output for minimum differential input voltage.

After design and verification of all building blocks of the ADC, in following section we analyze the stability as well as accuracy of designed incremental delta-sigma ADC.

3.4 Pre-Layout Modulator Simulations

In order to verify the performance of designed ADC, several simulations were carried out. First, the ADC was simulated with maximum and minimum input voltages, and integrators' outputs were monitored to verify the modulator's stability. In addition, the modulator's power consumption was also extracted from these simulations. Second, a sinewave simulation was performed, and the signal to noise ratio at the output of the ADC was extracted. The simulations were then repeated in various design corners and temperatures to find out the worst-case parameters of the ADC. In following sections the simulation results are discussed in more detail.

In order to analyze the output swing of the integrators, a differential *dc* voltage of $\pm 850\ mV$ is applied to the ADC for 436 clock cycles. Simulation results depicted in Fig. 37 indicate a fast settling for both integrators, and does not show any saturation or clipping in the output. Furthermore, despite the voltage variations, the integrators maintain their stability and accuracy in all design corners.

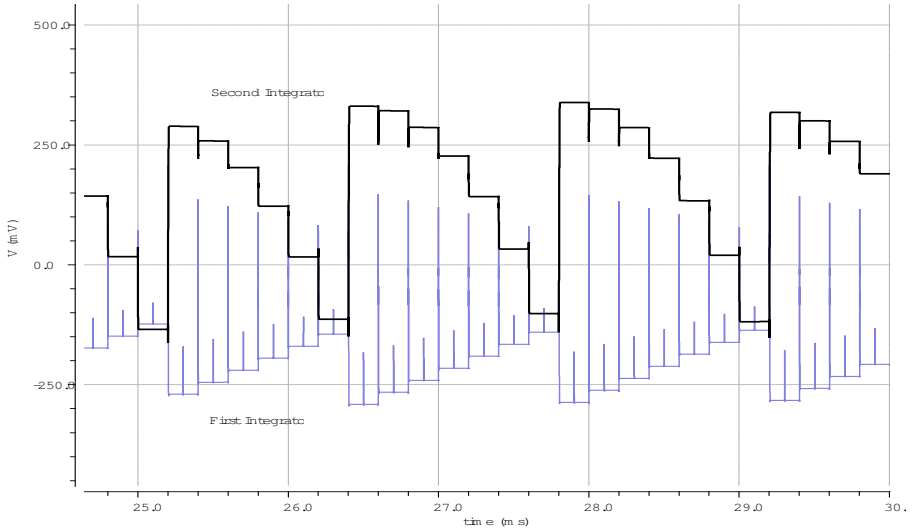
The *dc*-input simulations can also be used to measure the total power consumption of the ADC, which includes both static and dynamic power consumption. The static power consumption is due to the analog blocks, i.e. the amplifiers and the comparator, and is almost constant over time. On the other hand, the switches drive instantaneous currents from the power source, which may cause supply noise. Besides, the average dynamic power consumption of the switches as well as the capacitors adds up to the overall power consumption. According to corner simulations, the highest power consumption occurs in CMOS worst power (CMOSWP), capacitor worst speed (CapWS) corner at $85°C$, in which the total average current in active mode (I_{active}) equals 963.7 nA. On the other hand, the the current driven from the integrators during reset period (I_{Reset}) experiences its maximum, i.e. 1.345 μA, in the same corner at $27°C$. Given the fact that, the high I_{Reset} lasts merely for half a clock cycle, it does not affect the overall power consumption substantially. Nevertheless, it puts additional demands on the voltage supply.

Finally, the sleep current (I_{sleep}) is determined by simulating the ADC with 3 pA input bias current (1 pA for each analog block). The simulations revealed that, despite the negligible sleep current of 450 pA in nominal situation, the converter shows a sleep current as high as 9.37 nA at $85°C$. The leakage current can be associated with the dramatic increase in the leakage current of the switches at high temperatures, which is an inevitable consequence of V_{th} variations over temperature. Table 7 shows I_{active}, I_{sleep} and I_{Reset} in nominal and worst-case conditions.

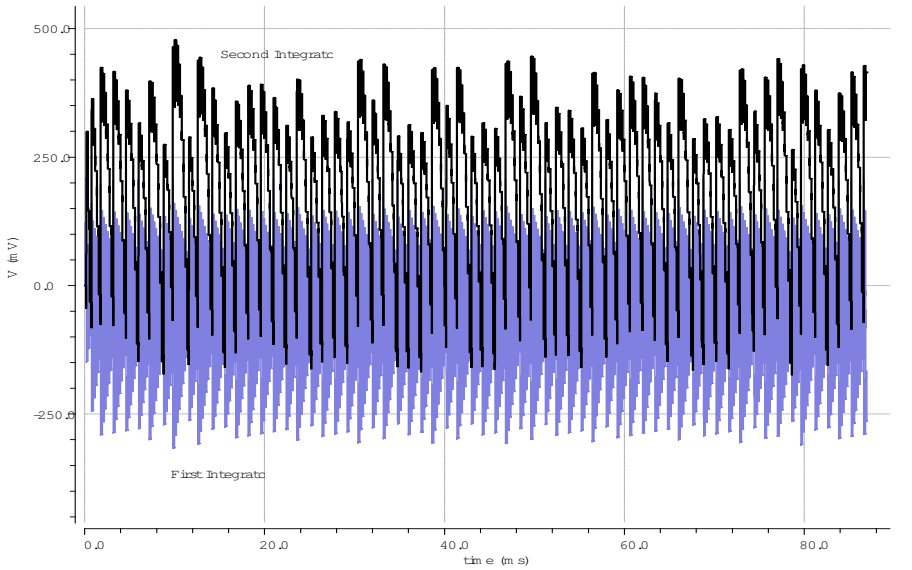
Table 7: Modulator power consumption in different design corners.

	Nominal	Worst Case
$I_{active}(nA)$	793.7	963.7
$I_{Reset}(\mu A)$	1.082	1.345
$I_{sleep}(A)$	454.3 p	9.63 n

Note: Worst-case corner is different for each parameter.



(a) Settling



(b) Bounded Output

Figure 37: The integrators outputs for maximum input voltage.

Fig. 38 depicts the output power spectrum of the designed ADC, which is obtained by performing FFT on modulator's output bitstream. In this simulation, a fullscale sinewave with $f = 3.824\ Hz$ is applied to the ADC for 1.046 s, i.e. 4 times signal period, and the DFF output is sampled in each clock cycle.

The figure clearly shows that, in nominal condition, the in-band noise is well below $-90\ dB$, and the modulator does not exhibit significant harmonic distortion. More precisely, in the nominal simulation, SINAD is 91.4 dB, which corresponds to $ENOB = 15.01$, and total harmonic distortion is roughly $-95.14\ dB$.

The spectrum analysis is also performed in different temperatures and process corners to find out the worst-case characteristics. As shown in Table 8, the minimum

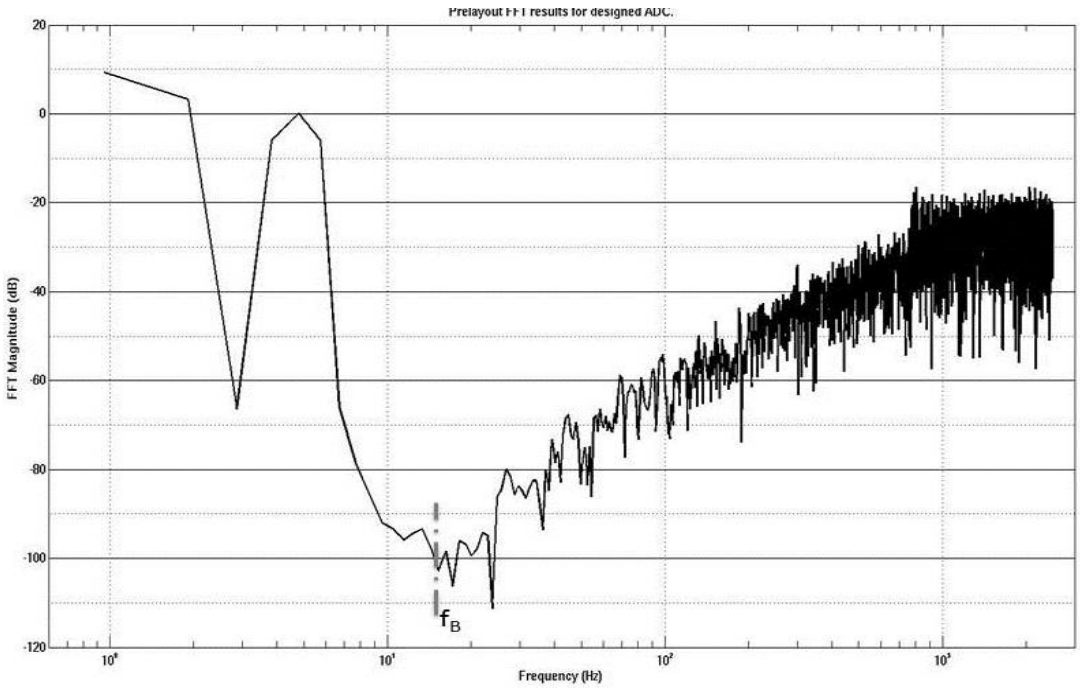


Figure 38: The output power spectrum of designed delta-sigma modulator in nominal conditions.

achievable SINAD is 84.62 dB, which occurs at 85°C in CapWP, CMOSWP corner. In this corner, the SNR is approximately 102.4 dB, whereas the total harmonic distortion (including the third and fifth harmonics) is -84.7 dB. This implies that the performance degradation in the worst-case, can be caused by increased switch leakage at high temperatures, and in CMOSWP corner. Furthermore, in CapWP corner, where the capacitors are smaller, switch charge injection produces a larger error in the integrator's output. Finally, one should note that, due to the small number of sampled bins, and narrow bandwidth of the modulator, the harmonics and noise are not easily distinguishable in the output spectrum, and the reported values for THD are rather pessimistic.

After all, the simulation results listed in Table 8 indicate an acceptable accuracy as well as linearity for designed ADC, since the worst-case SINAD, is roughly 2 dB less than the desired value, and it only occurs in one of the 12 simulated corners, thus the ADC's appropriate performance is verified in at least in 92% of the simulations.

Table 8: Frequency-domain characteristics of designed ADC.

	Nominal	Worst Case	Required
$SINAD(dB)$	92.13	84.62	86.02
$THD(dB)$	-95.14	-84.7	<-86.02
$ENOB$	15.01	13.78	14

4 Layout

4.1 Design

Fig. 39 shows a typical floor plan of an integrated switched-capacitor circuit. Generally, the attempt is to separate the analog and digital circuitry to protect the analog signals from fast transitions of digital signals. Besides, each block is isolated by a guard ring to further reduce the parasitic effects of the neighboring blocks on each other. The guard rings also help stabilizing the substrate (or N-well) potential by providing a low-impedance path to Vss. Substrate stabilization is extremely important, since variations of substrate potential through the wafer can produce substantial mismatch in threshold voltage of the transistors, and alter the coupling through the bottom-plate parasitic capacitances. Therefore, in large capacitor matrices, a ground grid is used in addition to the guard ring to ensure a constant substrate voltage across the matrix.

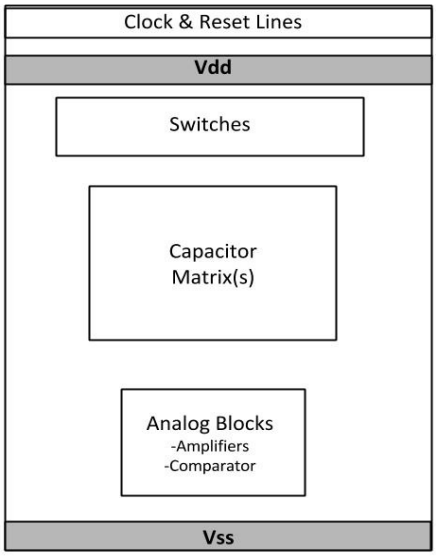
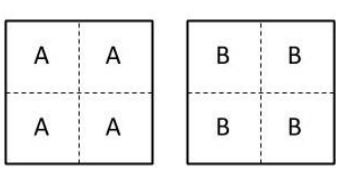


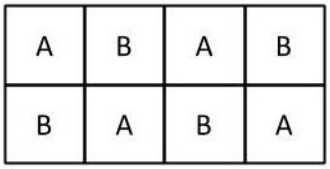
Figure 39: Floor plan of the designed layout.

As discussed in section 2.3.2, the on-chip capacitors are realized as a matrix of unit capacitors, since if each capacitor is implemented as a separate block (as in Fig. 40(a)), the parameter variations across the wafer may cause significant variation in actual capacitor sizes, which will subsequently alter the capacitor ratios. To avoid this, the unit capacitors of all the capacitors in an integrator are placed together within the same matrix in a way that the matrix is symmetrical with respect to its center point (Fig. 40(b)). This structure, known as common-centroid geometry, is capable of eliminating the effect of Nth-order parameter variation, provided that each capacitor is composed of 2^N unit capacitors. On the other hand, the sampling capacitors of the first integrator are quite small compared to the integrating capac-

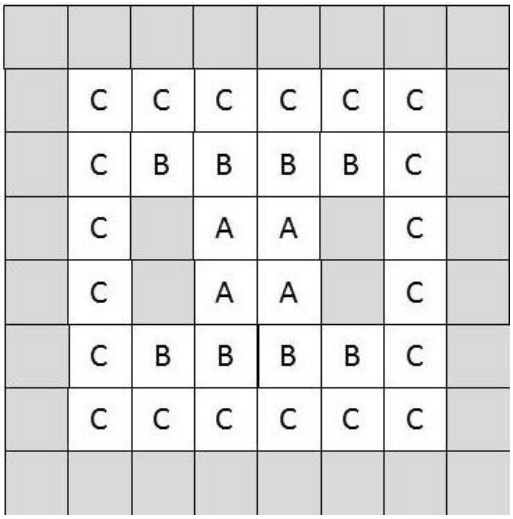
itor, thus they cannot be placed exactly as in Fig. 40(b). Instead, as shown in Fig. 40(c), the smallest capacitors (A) are placed at the center of the matrix, where the parameter variations are smaller, and the feedback coefficient capacitors (B), and the integrating capacitors(C) are located in a common-centroid manner around them. Furthermore, some dummy capacitors are used to reduce the *environmental* differences between the central and peripheral capacitors, and reach a symmetrical square-shaped structure. The resulting structure can thus provide an appropriate matching between the sampling and integrating capacitors, and guarantee an exact capacitor ratio.



(a) Separate capacitors.



(b) Capacitors in common-centroid geometry.



(c) Capacitors in the first integrator.

Figure 40: Capacitor matching with common-centroid geometry.

Common-centroid geometry can also be used in transistor current mirrors to alleviate the effect of through-wafer V_{th} variations on mirroring ratios. To achieve this, all the transistors involved in a current mirror are divided into a number of equally-sized fingers, and the fingers are grouped as shown in Fig. 41. The groups of transistors are then placed in way that the final structure is symmetrical with respect to its center. Besides, in order for all fingers to see a similar environment, each stack of transistors is enclosed by two dummy transistors whose gates are connected to the same gate as the transistors in the stack, but their V_{ds} is zero.

Another matching technique, which is typically used for differential input pair transistors, is the interdigitated finger structure depicted in Fig. 42. In this struc-

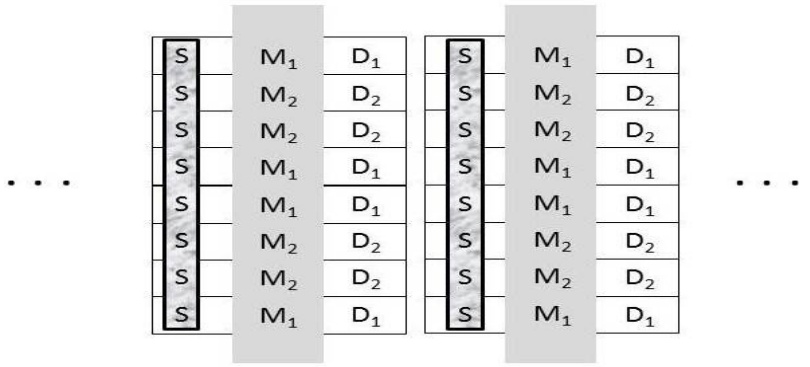


Figure 41: Transistor matching with common-centroid geometry.

ture, the segments of the matched devices are slipped between one another to form a one-dimensional common-centroid array. Thus, the interdigitated fingers can suppress the first-order parameter variations. Furthermore, by using a common source area for paired transistors, the device area can be minimized.

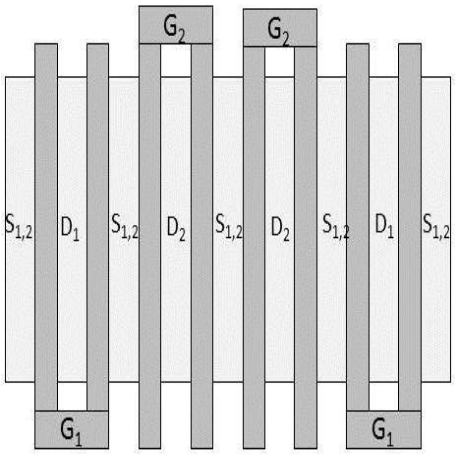


Figure 42: Interdigitated fingers.

In addition to device mismatches, the wiring also causes parasitic effects in the circuit. Generally, the on-chip wires are characterized as RC lines, thus the signals attenuate over the long signal paths, and may also couple to each other. Therefore, certain considerations must be taken into account to avoid on-chip performance degradation.

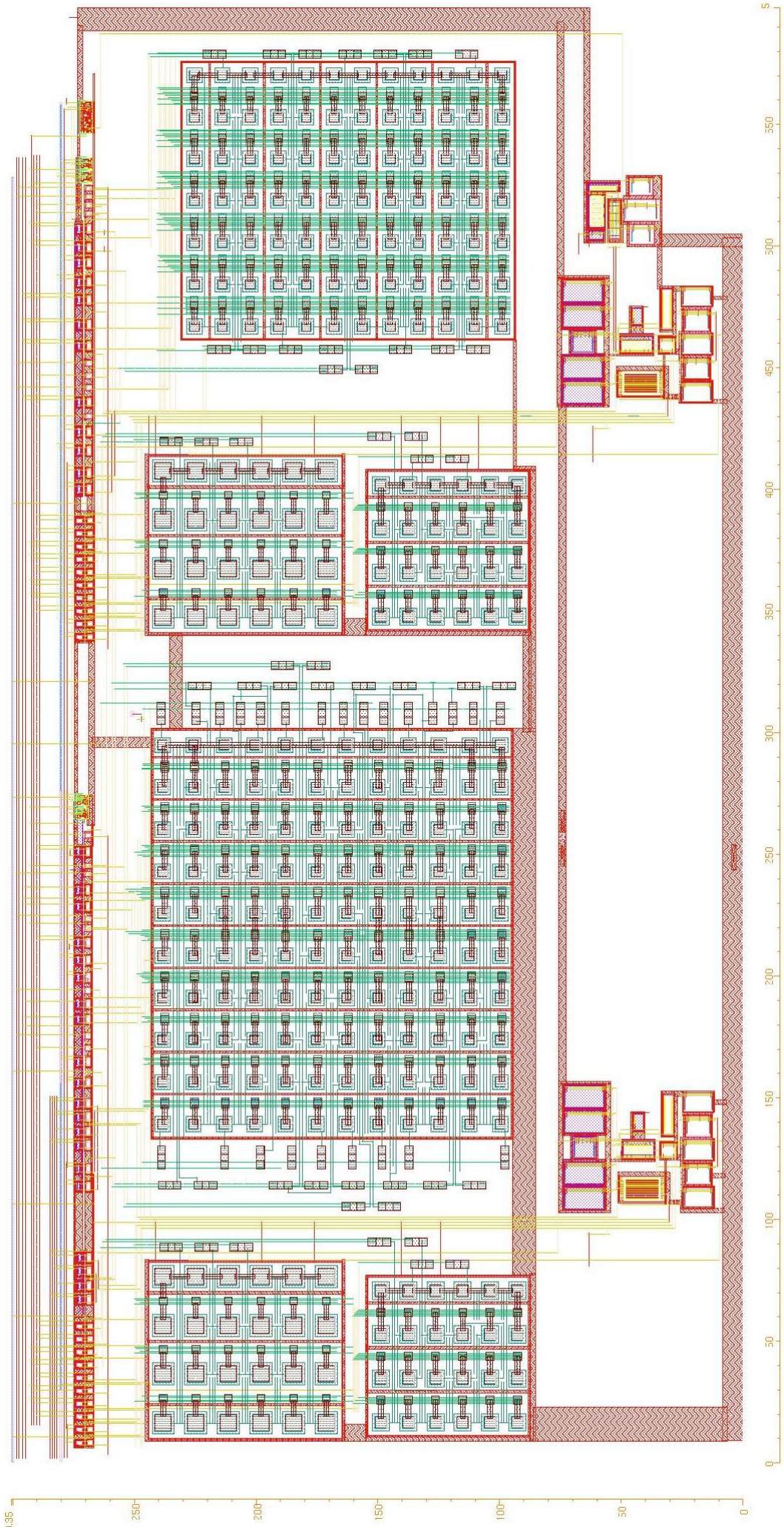
Firstly, there must be a wide, low-impedance path from each device to the supply voltages (Vdd and Vss) to minimize the supply voltage variation through the chip. This is of great importance, since a degraded supply voltage not only affects the output swing of the amplifiers, but also changes the timing characteristics of the digital blocks and can cause considerable mismatch between the devices. Therefore, as depicted in Fig. 39, the wide supply lines are usually located on the top and bottom of the circuit, and wide vertical lines connect each block to the supply lines. Alternatively, a tree pattern can be used to distribute the supply in the circuit.

Secondly, differential signaling must be utilized to eliminate the effect of common-mode parasitics as well as even-order harmonic distortion. The differential lines can also be shielded by two ground lines to further reduce the effect of neighboring devices and connection lines.

Finally, to reduce coupling and cross-talk, an appropriate distance should be always kept between two signals, and the neighboring signals should not run for a long distance in parallel. Furthermore, the wires going through the capacitor matrices must be shielded from each other, as well as the parasitic bottom-plate capacitors, by means of a ground line.

Fig. 43 shows the final layout of the designed ADC. Starting from the top, one can see the clock, reset, and DAC control lines connected to the switches. The capacitor matrices are located below the switches, and are shielded from the other blocks by separate guard rings. Lastly, the amplifiers and the comparator are located beneath the capacitor matrices. As it can be clearly seen in the figure, the capacitor matrices have the largest contribution to the total 300 μm times 600 μm layout area. This huge footprint is mainly due to the extraordinary capacitor process requirements, and is thus inevitable. However, in the common-mode feedback circuit, where the effect of capacitor mismatches is negligible, the peripheral dummy capacitors could be removed, and the unit capacitors could be combined.

After all, the on-chip parasitics can not be completely eliminated, and hence, the on-chip performance usually differs from circuit-level simulation results. Therefore, to accurately analyze the designed ADC, post-layout simulations must be carried out. Following section describes the post-layout simulation results.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4.2 Post-Layout Simulations

In post-layout analysis, all the simulations presented in section 3.4 are repeated with the extracted on-chip parasitics.

4.2.1 Amplifier

Fig. 44 shows the amplifier transfer function obtained from post-layout *ac* analysis in nominal conditions, and Fig. 45 depicts the amplifier's gain and phase variations in Monte Carlo simulations. In addition, both pre- and post-layout simulation data are gathered in Table 9 to simplify the comparison.

It can be clearly seen that, although parasitic-induced errors do not affect the nominal characteristics considerably, they cause a substantial performance degradation in the presence of parameter variations. Particularly, the on-chip parasitic capacitances add to load capacitance, and thus reduce the opamp phase margin. In present design, the phase margin decreases for about 30 % in post-layout MC simulations, leading to a worst-case PM of 51.75°, which is lower than required phase margin. More precisely, in about 10 % of the simulations the phase margin is below 60°, from which 5 % exhibit PM values lower than 52°.

As mentioned in Table 9, the amplifier's power consumption does not vary considerably from pre- to post-layout simulation. In fact, the worst-case amplifier current increases merely 1% in the post-layout simulation, which can be justified given the slight difference between pre- and post-layout transistor properties. However, there exists a large difference between the nominal and worst-case power consumptions, both in pre- or post-layout simulations, which results from g_m and V_{th} variations in Monte Carlo runs.

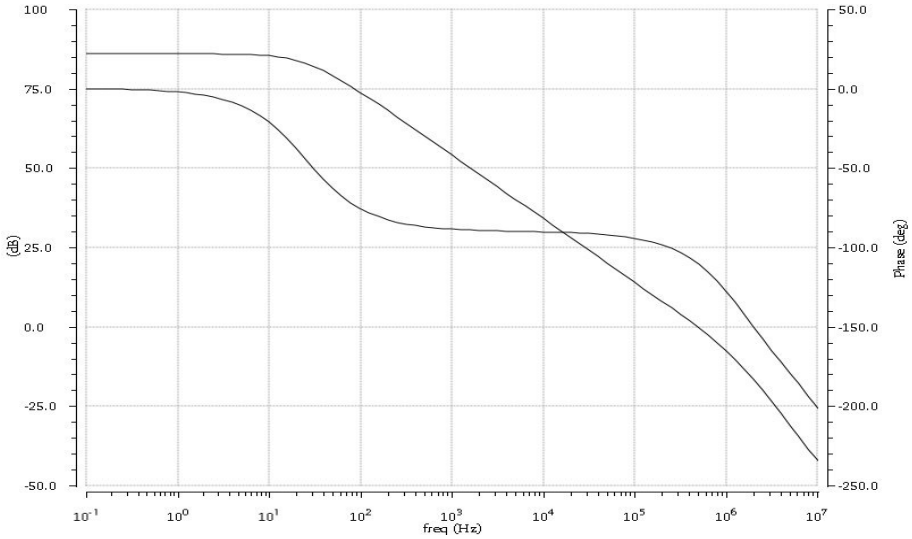


Figure 44: Transfer function of the on-chip amplifier under nominal conditions.

Undoubtedly, the on-chip parasitics also affect the amplifier's noise. This is illustrated in Fig. 46, which shows the input-referred noise of the amplifier in post-layout analysis. The data indicate an increase in both thermal and flicker noise, but

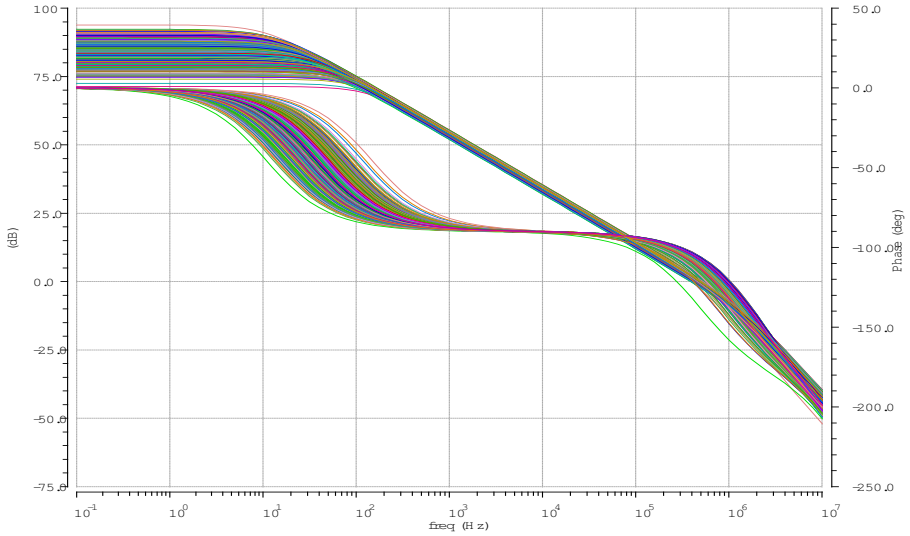


Figure 45: Transfer function of the on-chip amplifier in Monte Carlo simulations.

the latter exhibits a considerably higher change. In fact, the worst-case post-layout flicker noise is about 7 times higher than pre-layout simulations, whereas thermal noise is merely 40 % higher.

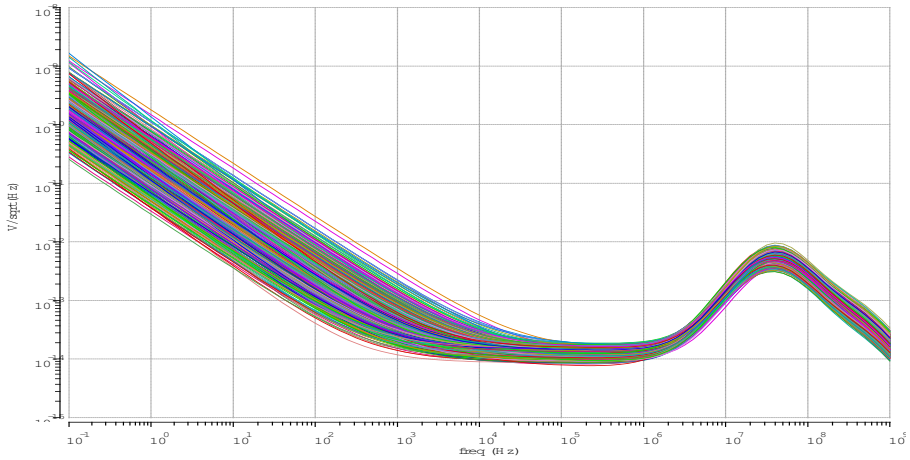


Figure 46: Input-referred noise of the on-chip amplifier.

Apart from *ac* analysis, the opamp offset was also calculated to find out the effect of parasitic-induced mismatches on the differential input pair. Clearly, the post-layout offset variation depicted in Fig. 47 is different from pre-layout simulation results; however, the worst-case offset values and their probability distribution are comparable to Fig. 33. This implies that the interdigitated structure implemented in the differential input pair can successfully suppress the layout parasitics.

Table 9: On-chip amplifier characteristics in nominal and worst-case conditions.

	Nominal		Worst Case		Required
	Post-ayout	Prelayout	Post-ayout	Prelayout	
Gain(dB)	85.87	86.2	71.33	78.01	60
GBW(kHz)	507	520.9	448.74	499.9	100
PM(°)	70.24	78.08	51.75	77.86	75
GM(dB)	31.36	32.52	30.09	31.91	30
$I_{tot}(nA)$	364.6	364.5	465.5	470.1	400
Corner Frequency(kHz)	10.5	3.9	316.2	39.8	−−
Thermal noise ($\frac{V}{\sqrt{Hz}}$)	115.9 n	114.5 n	136.8 n	125.6 n	−−

Note: The worst case is different for each parameter.

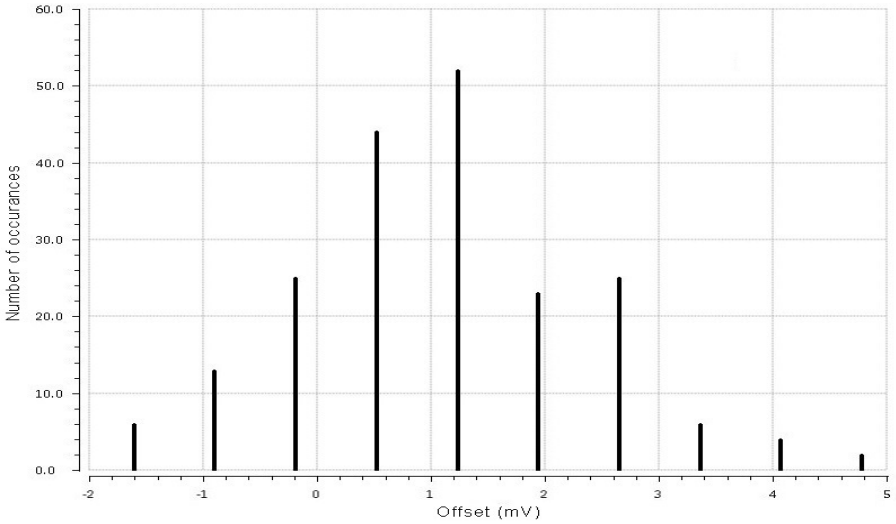


Figure 47: The offset at the input of the on-chip amplifier.

4.2.2 Modulator

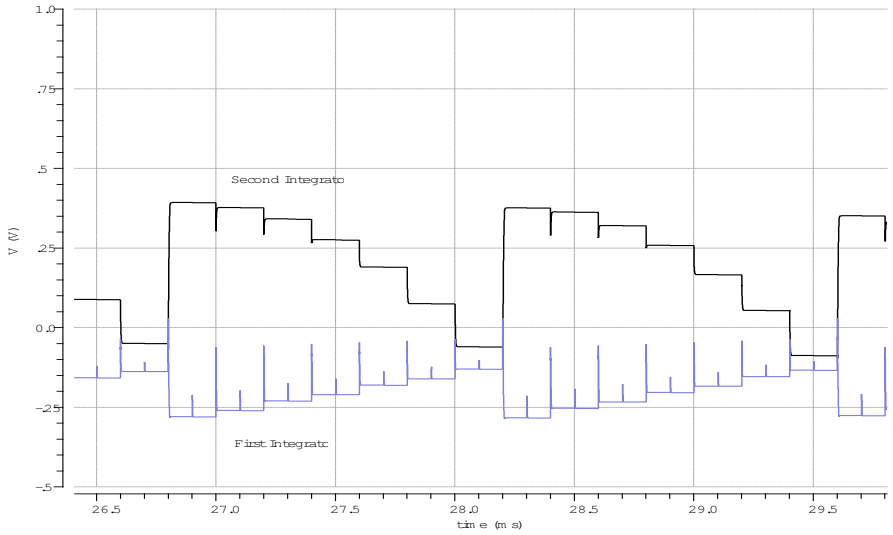
Fig. 48 depicts the integrators outputs in a transient simulation with $V_{in} = -850\,mV$. Alike schematic-level simulations, the implemented integrators are also stable, and exhibit fast settling. Furthermore, the output voltage swing of the integrators does not change significantly from pre- to post-layout simulation.

The current through the ADC has been also observed via Monte Carlo analysis. As listed in Table 10, the active current of the converter is slightly lower in post-layout simulations, and I_{Reset} decreases more than 30 %, so that its worst-case value does not exceed 1 μA anymore. Therefore, the converter guarantees a power consumption less than 1.2 μW in all simulated design points.

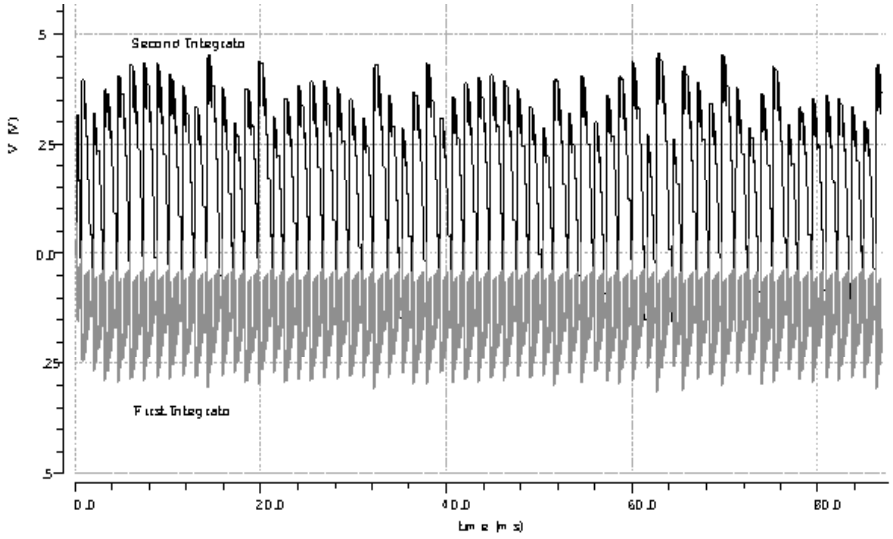
Table 10: Post-layout power consumption of the designed ADC.

	Nominal		Worst Case	
	Post-layout	Prelayout	Post-layout	Prelayout
$I_{active}(nA)$	784.6	793.7	953.4	963.7
$I_{Reset}(A)$	884.5 n	1.082 μ	971.9 n	1.345 μ
$I_{sleep}(A)$	781.2 p	454.3 p	10.06 n	9.37 n

Note: The worst-case design point is different for each parameter.



(a) Settling



(b) Bounded Output

Figure 48: Post-layout integrators outputs for maximum input voltage.

Fig. 49 shows the output power spectrum of designed ADC obtained from the parasitic-extracted layout, compared to the prelayout simulation results. It can be clearly seen that both noise and harmonic distortion are higher in the layout, and the post-layout analysis gives $SINAD = 81.1\ dB$ and $THD = -82.2\ dB$ in nominal conditions, which results in $ENOB = 13.2$. Moreover, the simulations performed in different process corners revealed that the worst-case THD, i.e. $-80.89\ dB$, occurs at the same corner as in prelayout simulations, but its value is about 4 dB higher. However, one should note the the THD values reported in this work, are rather pessimistic, and more realistic results can be obtained by using larger number of bins in the FFT analysis. Table 11 lists the ADC characteristics gathered from numerous pre- and post-layout simulation.

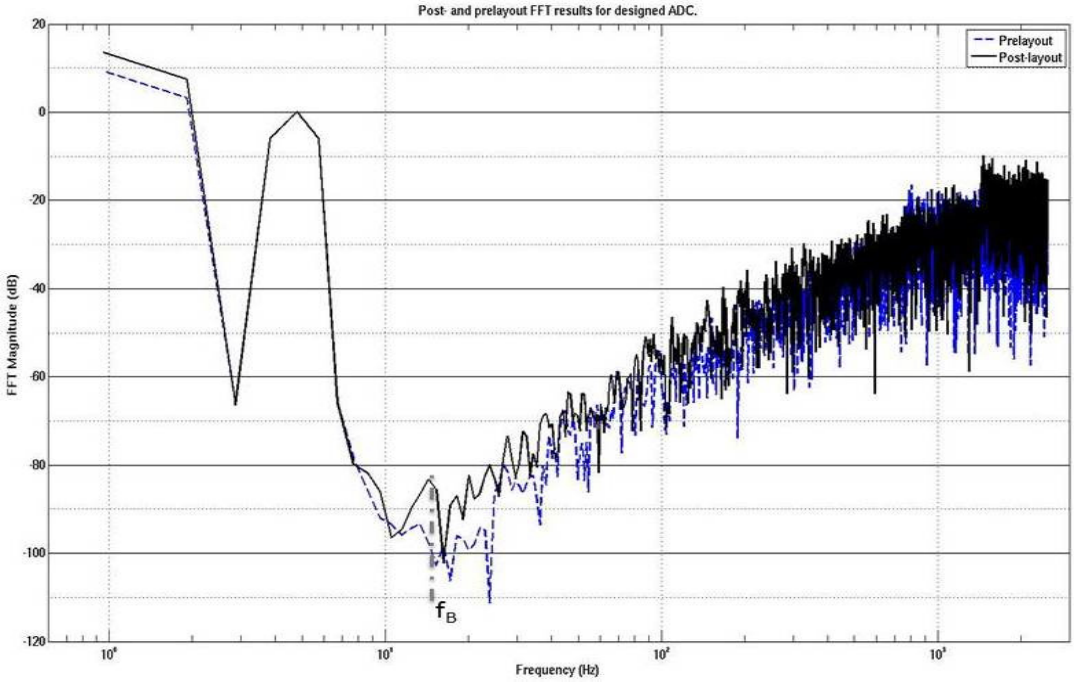


Figure 49: The output power spectrum of designed ADC in nominal conditions.

Table 11: Post-layout frequency-domain performance of designed ADC.

	Nominal		Worst Case	
	Post-layout	Prelayout	Post-layout	Prelayout
$SINAD(dB)$	81.1	91.4	80.05	84.52
$THD(dB)$	-82.2	-95.14	-80.89	-84.7
$ENOB$	13.2	15.01	13	13.8

5 Summary and Discussion

This thesis is focused on design of an ultra-low power 14-bit incremental delta-sigma analog-to-digital converter. The ADC is designed in 0.18 μm CMOS technology, with a single 1.2 V supply voltage, and it operates with a sampling clock frequency of 5 kHz. The ADC requires only a single dedicated 600 mV voltage reference, as it is able to utilize Vss as the other output bit feedback reference.

To achieve the desired accuracy with optimum power consumption, different modulator topologies are studied, and MATLAB simulations are carried out to find out the most appropriate coefficients and oversampling ratio for the delta-sigma modulator. The designed loop filter is then realized using differential switched-capacitor integrators in a second-order CIFB configuration.

Given the deleterious effect of amplifier offset and flicker noise on modulator's performance, chopper stabilization is used in the first integrator to remove the offset, and reduce the low frequency noise. Given that the noise of the second integrator does not affect the modulator significantly, the chopper circuits are only implemented in the first integrator.

In order to minimize the switch signal-dependent charge injection, bottom-plate sampling is used in all switched-capacitor blocks. Furthermore, the switches are realized with small-area transmission gates to further reduce the charge injection.

Finally, the integrators and the whole modulator are simulated in different process corners and temperatures, and the worst-case characteristics are extracted based on power spectrum analysis in MATLAB. The modulator has shown ultra-low power consumption in both pre- and post-layout simulations. In fact, the worst-case supply current of the ADC in post-layout Monte Carlo simulations is 953.4 nA, which is below the $1-\mu A$ limit. Moreover, the worst-case power consumption occurs in roughly 2% of the 600 simulation points, whereas in more than 50% of the simulations the current is well below 950 nA. In addition, the start-up current of the modulator is also less than 1 μA, and thus it does not impose any additional requirements on the power supply. Finally, it is worthwhile mentioning that the designed amplifiers benefit from a 400 kHz GBW, which enables them to operate at frequencies much higher than 5 kHz. Considering all these, the total energy per conversion can be reduced by increasing the clock frequency, without compromising the accuracy. Power consumption can be further optimized by adjusting the number of samples per conversion based on the desired accuracy.

Unlike the power consumption requirements, the ADC fails to fulfill the accuracy requirements in some design corners. As a matter of fact, spectrum analysis of the parasitic-extracted layout indicate a worst-case accuracy of 13.1 bit, which is approximately 1 bit lower than desired accuracy. Nonetheless, as long as the accuracy is not limited by ADC's nonlinearity, the required accuracy can be achieved by operating the modulator for a longer time period, i.e. by using more samples. Furthermore, the worst-case accuracy occurs in about 10% of the design points, and in the rest of the simulations ENOB is greater than 13.4 bit.

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