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RF Power Amplifier for TETRA Base Station

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ABSTRACT OF THE
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Linear power amplifiers are needed in systems, where spectrum efficient modulation methods are used. One of these systems is TETRA (TErrestrial Trunked RAdio). High linearity of power amplifier usually affects negatively its power efficiency. Therefore, different linearization methods are used to keep the power amplifier linear, while its efficiency is increased. Different linearization methods are presented in begining of this study.

The scope of this thesis work is to study LDMOS and GaN transistor power amplifiers and select a suitable transistor to be used in the TETRA base station power amplifier. Using a circuit simulator, LDMOS and GaN transistor characteristics are analysed and power amplifier circuits are designed according the design specifications. Using the information derived from the simulations, a prototype of TETRA power amplifier is constructed. The constructed power amplifier circuit is then measured and the results are compared to simulation data and requirements of the TETRA standard.

Based on the achieved measurement results, the LDMOS transistor is the most suitable choice to be used in TETRA power amplifier. However the study shows, that if the price of the GaN devices goes down, they may challenge LDMOS transistor, as they can offer wide frequency bandwidths with decent power efficiency and acceptable gain.

Keywords: TETRA standard, Base station, Linear power amplifier, LDMOS, GaN

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Lineaarisia tehovahvistimia tarvitaan järjestelmissä, joissa käytetään suureen spektritehokkuuteen pyrkiviä modulointimenetelmiä. Yksi tällaisista järjestelmistä on TETRA-järjestelmä (TErrestrial Trunked RAdio). Lineaariset tehovahvistimet ovat usein huonoja hyötysuhteeltaan. Siksi erilaisia linearisointimenetelmiä käytetään tehovahvistimien linearisointiin, jotta niiden hyötysuhdetta saadaan parannettua. Erilaisia linearisointimenetelmiä on esitelty tämän työn alkupuolella.

Tämän työn tarkoituksena on tutkia LDMOS ja GaN tyyppisiä transistoreja ja niiden sopivuutta TETRA tukiaseman tehovahvistimiksi. Piirisimulaattoria apuna käyttäen LDMOS- ja GaN-transistorien tyypilliset ominaisuudet selvitetään ja annettujen vaatimusten mukaiset tehovahvistinkytkennät muodostetaan. Simulaatioista saatua tietoa hyödyntäen TETRA vahvistimen prototyyppi valmistetaan. Prototyyppivahvistin mitataan ja saatuja mittatuloksia verrataan simultaatiotuloksiin sekä TETRA-standardin asettamiin vaatimuksiin.

Mittaustulosten perusteella LDMOS tyyppinen transistori on tutkituista transistoreista paras vaihtoehto TETRA-tehovahvistimeksi. Selvitys kuitenkin osoittaa, että jos GaN-transistorien hinta laskee, voivat ne tarjota varteen otettavan vaihtoehdon LDMOS-transistoreille TETRA-tukiasemakäyttöön.

Avainsanat: TETRA-standardi, tukiasema, lineaarinen tehovahvistin, LDMOS, GaN

Preface

I would like to thank my employer Cassidian Finland Oy for giving me the opportunity to write this thesis. My gratitude goes to my thesis advisor Kristian Thomasson, M.Sc, for instructing my thesis work. Many thanks go to my colleagues Jukka Luukkainen and Kalle Metso, who have given me advice and shared their expertise throughout the thesis process.

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Sami Multasuo

Contents

Symbols and abbreviations

Symbols

α	transistor conduction angle
β	feedback factor, phase constant
$\Delta\|A\|$	correction to amplitude
$\Delta\|\Phi\|$	correction to phase
ε_r	static relative permittivity, relative dielectric constant
λ	wavelength
μ	geometric stability factor
μ_L	load side geometric stability factor
μ_S	source side geometric stability factor
ρ	metal bulk resistivity normalized to gold
ω_c	angular frequency of carrier signal
$\|A\|$	amplitude of the signal
$Ae^{j\phi}$	complex gain of amplifier
$B_{(k)}$	kth binary digit
$D_\theta(k)$	phase transition in $\pi/4$-DQPSK
f_c	carrier signal frequency
f_e	frequency offset to the edge of used frequency band
G	feedback gain
h	substrate thickness
I_{DQ}	quiescent drain current
I_{ds}	DC drain to source current
I_{max}	saturation limit of the transistor drain current
P_{DC}	DC power
P_{in}	input power
P_L	power delivered to the load
P_{out}	output power level, power delivered to load
P_{tot}	total DC power
R_0	normal resistance
R_d	drain side bias resistor
R_g	gate side bias resistor
R_M	intermediate resistance
R_{opt}	optimum load impedance for power amplifier
R_{th}	thermal resistance from junction to case
$S(1,1)$	input port voltage reflection coefficient
$S(t)$	modulated RF signal
t	conductor thickness
T_j	transistor junction temperature
T_p	transistor package temperature
$tan\delta$	loss tangent
V_{ds}	DC drain to source voltage
V_{GQ}	quiescent gate voltage
V_{gs}	DC gate to source voltage
$V_{gs(th)}$	DC gate to source threshold voltage
v_i	input signal
v_o	output signal
v_p	output of the predistorter
Z_0	normal impedance
Z_1	impedance to be matched
Z_a	impedance in the middle of lowpass matching circuit

Abbreviations

π/4-DQPSK	π/4-shifted Differential Quaternary Phase Shift Keying
π/8-D8PSK	π/8-shifted Differential 8 PSK
ACP	Adjacent Channel Power
AM	Amplitude Modulation
AWR	Advanced Wave Research
BS	Base Station
BW	Bandwidth
dBc	Decibels to the carrier signal level
ETSI	European Telecommunications Standards Institute
GaN	Gallium Nitride
IM	Intermodulation
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LNA	Low Noise Amplifier
MOSFET	Metal Oxide Semiconductor Field-Effect Transistor
MSUB	Microstrip substrate definition in AWR
MWO	Microwave Office
PA	Power Amplifier
PAE	Power Added Efficiency
PCB	Printed Circuit Board
PM	Phase Modulation
PMR	Private Mobile Radio
PSK	Phase Shift Keying
RF	Radio Frequency
RMS	Root Mean Square
TETRA	Terrestrial Trunked Radio
VCO	Voltage Controlled Oscillator

1 Introduction

Nowadays, wireless communication is used everywhere. It is used from near communications systems such as wireless headsets to cellular networks that can cover countries and continents. As there is an increasing number of different wireless systems, the usable frequencies are highly regulated, making it important to use any given frequency as efficiently as possible. This has unavoidably led to situation, where more and more complicated modulation methods are used to match the need. In radio frequencies (RF), use of advanced modulation methods requires high linearity transmitters and as the linearity of a radio transmitter highly depends on the linearity of its power amplifier (PA), and therefore designing a linear power amplifier becomes a critical part of transmitter design process.

Another trend that is guiding the radio transmitter design process and actually any other electronic device design process, is the device's power consumption. Specially in the mobile devices, it is critical to use the available power as efficiently as possible to guarantee longer working periods without charging. In base station radio transmitters, the power efficiency is not that critical, but the generated excess heat in low efficiency transmitters, causes problems. As the PA consumes most of the power in the radio transmitter, its efficiency is critical on overall power consumption of the transmitter. However, there is a conflict between efficiency and linearity of a PA. If the PA becomes more efficient, its linearity suffers and counter-wise. To overcame this conflict, a variety of linearization methods is used and compromises between linearity and efficiency have to be made. Fortunately, the PA design problem is a widely covered area and multiple solutions are available. The key is to select the most suitable one for the situation in hand.

In this thesis, the design process of the PA stage for a Terrestrial Trunked Radio (TETRA) transmitter is presented. The guidelines of the design are set by the TETRA standard, which defines the requirements of the PA as well as how the verification measurements are to be conducted. The TETRA standard and its requirements are discussed in Chapter 2. Also the used modulation, and its characteristics are discussed in that chapter. As mentioned before, the linearity and efficiency are important features of transmitters. To keep the efficiency high enough, linearization methods are often used. Variety of linearization techniques are discussed in Chapter 3, including the Cartesian loop, which is the linearization method used in the current transmitter case.

Chapter 4 deals with the power amplifier design. The design of the PA starts with the selection of a suitable power transistor, based on the needed amplification, output power and other requirements. The power transistor is the base of the whole design, as it is the component, which amplifies the carrier signal to the desired power level. There are different types of transistors used in RF power amplifiers, but in the scope of this thesis, only gallium nitride (GaN) and laterally diffused metal oxide semiconductor (LDMOS) transistors are discussed. Differences between the two transistor types are discussed in Section 4.2. The requirements set by TETRA standard and by the design environment are presented in Section 4.1. In Chapter 4, the whole PA design process is presented, including simulations and theory. Using the

load-pull simulation, transfer characteristics of the selected transistors are studied, and the optimum input and output impedances are found out. Selected input and output impedances define the goal of matching circuitry design, and suitable low-pass matching circuits are constructed. The simulations, based on the manufacturer offered transistor model, are carried out.

In Chapter 5, simulation results are verified by measurements. The selected transistors are assembled to the prototype circuits, according to the simulation results. These demo circuits are used to verify simulation results and other PA design requirements. Modifications to the design are done, if needed, and the measurements according to the TETRA standard are conducted. For the GaN device, measurements are conducted by using test circuitry provided by the transistor manufacturer. These measurements include measuring output power, PA efficiency, temperature of the transistor and linearity. Based on the measurement results, the most suitable solution for the TETRA base station power amplifier is selected.

The selected PA design is implemented to be the last stage in the amplifier chain of the TETRA base station. The design of this implementation is discussed in Chapter 6 at system level, but the actual implementation and testing of the prototype PA is not a part of this thesis.

2 Terrestrial Trunked Radio (TETRA)

2.1 TETRA standard

TETRA is a standard by European Telecommunications Standards Institute (ETSI) and it was designed for the private mobile radio (PMR) systems. The first TETRA standard was published in March 1996 and its development is still ongoing.[1]

TETRA was designed for voice and data services, mainly for public safety, transportation, government and military purposes. TETRA is mainly used in Europe, because of its ETSI approval, but lately it has become more popular outside of Europe also. In May 2008 TETRA technology was used in 103 countries, showing substantial growth in the Asia-Pacific region. [2, 3]

2.2 TETRA characteristics for radio transmission

2.2.1 Modulation

Phase modulations used in the TETRA systems are $\pi/4$-shifted Differential Quaternary Phase Shift Keying ($\pi/4$-DQPSK) and $\pi/8$-shifted Differential 8/PSK (π 8-D8PSK). The modulation rate for $\pi/4$-DQPSK is defined to be 36 kbit/s and 54 kbit/s for $\pi/8$-D8PSK. In the case of $\pi/4$-DQPSK, which is the modulation used in this PA design, each possible bit sequence produces a specified phase transition multiple of $\pi/4$. All possible transitions are presented in Table 1. The carrier separation for the both modulation methods is defined to be 25 kHz.[3, 4]

Table 1: Possible phase transitions in $\pi/4$-DQPSK.

Modulation bits		Phase transition
$B_{(2k-1)}$	$B_{(2k)}$	$D_\theta(k)$
0	0	$+\pi/4$
0	1	$+3\pi/4$
1	0	$-\pi/4$
1	1	$-3\pi/4$

The advantage of $\pi/4$-DQPSK compared to normal DQPSK is that the amplitude of the modulated signal is varying less. As we can see in Figure 1, the phase transition never causes the modulated signal amplitude to cross zero. Another benefit from this modulation, is that the modulated signals peak power is only 3.25 dB higher than the average power level, after the filteration. Therefore, the $\pi/4$-DQPSK modulation grants more room for nonlinearities of the power amplifier.[3]

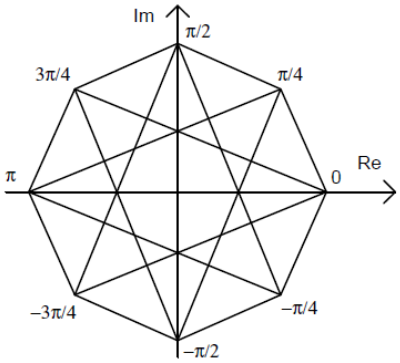

Figure 1: $\pi/4$-DQPSK modulation symbol constellation and possible phase transitions.

2.2.2 Transmission power classes

TETRA transmitter output power of the phase modulated signal is divided to the different power classes. The base station power classes are presented in Table 2. The listed power levels are average powers, and have the tolerances defined in EN 300 394-1.[5]. The power class defines the maximum average output power level that the transmitter is defined to work. However, the transmitter needs to function with lower power levels (classes below the selected power class) also.[4]

Table 2: Nominal output power classes of TETRA BS transmitters.

Power Class	Nominal power per carrier
1 (40W)	46 dBm
2 (25W)	44 dBm
3 (15W)	42 dBm
4 (10W)	40 dBm
5 (6.3W)	38 dBm
6 (4W)	36 dBm
7 (2.5W)	34 dBm
8 (1.6W)	32 dBm
9 (1W)	30 dBm
10 (0.6W)	28 dBm

2.2.3 Adjacent Channel Power (ACP) and unwanted emissions far from carrier

Adjacent channel power (ACP) is a great concern in a TETRA system, because there is no way to guarantee that the adjacent carriers are not used in the same

geographical location. Therefore, the TETRA standard defines strict limits for ACP, as shown in Table 3. The peak power limit during the ramp-up and ramp-down periods of the signal, should not exceed -50 dBc, with the frequency offset of 25 kHz. This is valid for all power classes, except for class 4, the peak power of which, should be under -45 dBc. The limits are carrier frequency dependent and vary with different frequency offsets. In addition, no ACP power level needs to be less than -36 dBm. [4]

Table 3: ACP limits for TETRA BS with different frequency offsets.

Frequency offset	Maximum ACP level ($f_c < 700$ MHz)	Maximum ACP level ($f_c > 700$ MHz)
25 kHz	-60 dBc	-55 dBc
50 kHz	-70 dBc	-65 dBc
75 kHz	-70 dBc	-65 dBc*)
*) 70 dBc for power classes 1,2 and 3		

TETRA standard also sets limits for other emissions further away from the carrier signal. The emissions occurring with frequency offset of 100 kHz or more are to be measured in the frequency range from 9 kHz to 4 GHz. The limits depend on the used carrier signal frequency and transmitter power class. The limits are shown in Table 4. As the limits are related to the carrier signal power level, they can become too tight for smaller output power levels. Therefore, some absolute limits are also defined. For frequency offset smaller than f_e, no limit tighter than -55 dBm is required. Similarly, no limit tighter than -70 dBm is required for frequency offset greater than f_e. [4]

Table 4: Maximum signal power level limits far from carrier.

	Maximum allowed level		
Frequency offset	$f_c \leq 700$ MHz all power classes	$f_c > 700$ MHz power classes 10-4	$f_c > 700$ MHz power classes 1,2 and 3
100 kHz to 250 kHz	-80 dBc	-74 dBc	-80 dBc
250 kHz to 500 kHz	-85 dBc	-80 dBc	-85 dBc
500 kHz to f_e	-90 dBc	-85 dBc	-90 dBc
$>f_e$	-100 dBc	-100 dBc	-100 dBc
*) f_e is the offset to the edge of received band or 5 MHz (10 MHz if carrier frequency is above 520 MHz) whichever is greater.			

3 Transmitter and power amplifier linearization methods

In this chapter a number of linearization methods for transmitters and power amplifiers are reviewed and the Cartesian correction is studied more carefully, as it is used in the TETRA transmitter in question. The linearization methods can be divided in the two subsections, predistortion and feedforward, based on where the signal correction takes place. In the predistortion, modifications to the input signal amplitude and phase are made making output signal after the PA more linear. One of the downsides of this method is that the peak power of the PA cannot be increased. A feedback loop can be also defined as an input correction or predistortion. The feedforward method however, makes the correction to the output signal of the PA, making possible to increase the peak power of it. The feedforward systems can be still divided to three sub-categories: those that function in backed-off levels, those which restore maximum peak power and ones that do both. In generally, predistortion or feedback methods are used in the systems, which are limited by modulation bandwidth (BW) requiring high levels of linearization and feedforward methods are used when wider bandwidths are needed.[6]

3.1 Feedforward methods

As stated in the beginning of Chapter 3, in the feedforward method the correction is applied after the PA, unlike in predistortion and feedback methods. This gives the feedforward method an advantage in the regions of stability and bandwidth limitations. However, the disadvantage is that the correction signal has to be amplified to necessary high power level to be combinable with the original amplified signal. Therefore, used error amplifier sets the limits of feedforward loop by its own distortion properties. An example of a feedforward system is shown in Figure 2.[6]

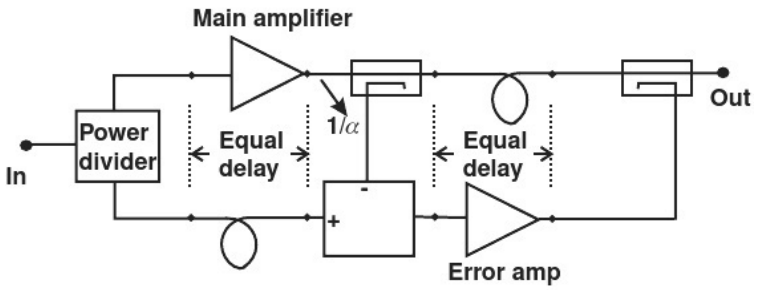

Figure 2: Feedforward system.[6]

Another problem arises from adding the error amplifier signal to the main amplifier signal. Should a 3 dB traditional coupler be used, it would mean losing half of the main amplifier power. On the other hand, if a 10 dB coupler is used, losses are more acceptable, around 0.5 dB, but the power required from the error amplifier is 10 dB higher. A coupling value of 6 dB offers a feasible compromise, resulting in

1.25 dB insertion loss and requiring 6 dB more power from the error amplifier. It is still notable that the power efficiency of the amplifier circuit is lowered as the main amplifier needs to produce the extra power lost in the coupling and the error signal amplifier itself requires some power.[7]

3.2 Predistortion methods

In predistortion method, input signal of the PA is modified so that the output of the PA is more linear than without modifications to the input signal. Usually predistorter is designed so that it cancels out the original third degree distortion. The problem is that canceling out third degree distortion creates other higher order products, that usually exceed the original distortion spectrum. If the inspection is restricted to the third degree model of the PA, the spreading of the spectrum can be easily shown, see equation (1),

$$v_o = a_1 v_p + a_3 v_p^3 \tag{1}$$

where v_p is the output signal of the predistorter. The predistorter also has the characteristics of equation (2), where v_i is the input signal of the PA circuit.

$$v_p = b_1 v_i + b_3 v_i^3 \tag{2}$$

Now v_o can be written in a form of equation (3), which can be expanded to equation (4).

$$v_o = a_1(b_1 v_i + b_3 v_i^3) + a_3(b_1 v_i + b_3 v_i^3)^3 \tag{3}$$

$$v_o = a_1 b_1 v_i + a_1 b_3 v_i^3 + a_3 b_3^3 v_i^9 + 3a_3 b_1 b_3^2 v_i^7 + 3a_3 b_1^2 b_3 v_i^5 + a_3 b_1^3 v_i^3 \tag{4}$$

As the aim is to minimize third order distortion, should be b_3 selected as:

$$b_3 = -\frac{a_3 b_1^3}{a_1} \tag{5}$$

The result is that the v_i^3 component is removed, but the v_i^5, v_i^7 and v_i^9 components are created, thus widening the distorter spectrum. [6]

The basic principle in a predistortion system is, that the parameters of the predistorter are selected based on the input signal amplitude and then corrections to the input signal amplitude and phase are made. See Figure 3 for the flow chart of the predistortion system. In addition to the input signal amplitude monitoring, also the output signal, temperature and other features should be monitored for predistorter parameter selection. The output signal should also be used for updating the parameter table of the predistorter, as the properties of the amplifier circuit change.

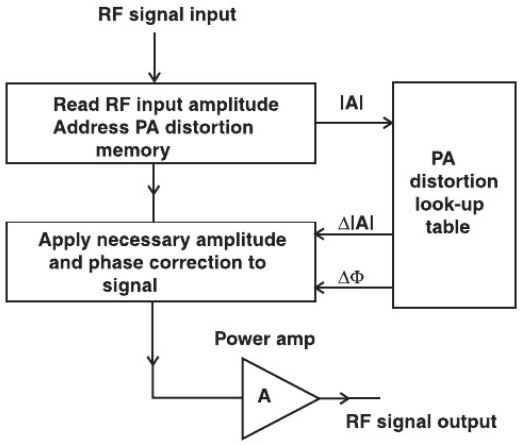

Figure 3: Basic predistortion system flow chart.[6]

3.3 Feedback methods

The negative feedback is the most traditional way to control the amplifier nonlinearities. The basic principle is to reduce gain by providing inverse phase feedback signal to the input of the amplifier. The previous technique is called direct feedback (see Section 3.3.1). As the direct feedback is highly sensitive for phase variations in the feedback path, the technique becomes problematic when used in higher frequencies. Therefore, indirect feedback techniques are also developed offering some possibilities to overcome phase delay problems (see Section 3.3.2).[8]

3.3.1 Direct feedback

The classical direct feedback circuit is shown in Figure 4. Its gain is expressed as in equation (6), where the $Ae^{j\phi}$ is a complex gain, G is a feedback gain and the β is a feedback factor.[8] However, using direct feedback for radio frequencies has two major difficulties. The first problem is to get enough gain with useful reduction to distortions, as the gain is reduced as a function of better linearity. In other words, if the negative feedback loop reduces the overall gain of the system by 10 dB, intermodulation (IM) products are also reduced by 10 dB. This might still be acceptable, but the second problem is more severe.[7]

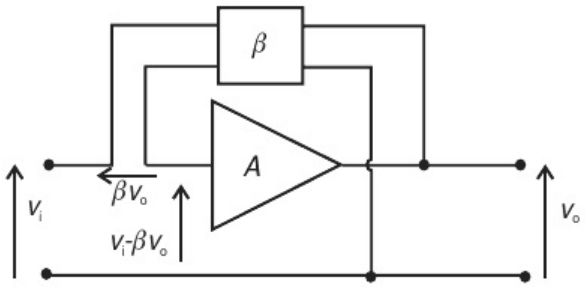

Figure 4: Basic direct feedback amplifier.[8]

$$G = \left| \frac{Ae^{j\phi}}{1 - \beta Ae^{j\phi}} \right| \tag{6}$$

The matched RF transistor causes large delays to the signal path. It means that the inverse phase feedback is impossible to achieve during one RF cycle. The only option is to add more delays at the design frequency so that the inverse phase feedback is achieved, even though a couple of RF cycles later than in input signal. This is possible, if the carrier frequency is not changing significantly. A downside is that stable operation BW becomes rapidly narrower as the delays in the feedback loop grow. Narrow stability BW and modest linearity returns of the negative feedback loop are often too much to overcome. Therefore, indirect feedbacks are more common in RF frequencies.[7]

3.3.2 Indirect feedback in general

Indirect feedback techniques try to force the detected characteristics RF signal to be the same at the input and the output of the PA. These techniques can be called envelope feedback techniques. An example of the envelope feedback system featuring amplitude correction is shown in Figure 5. Some indirect feedback techniques can also detect phase differences between input and output of the PA, and try to correct those. Couple of different techniques are addressed in the following sections separately (see Sections 3.3.3 and 3.3.4).[8]

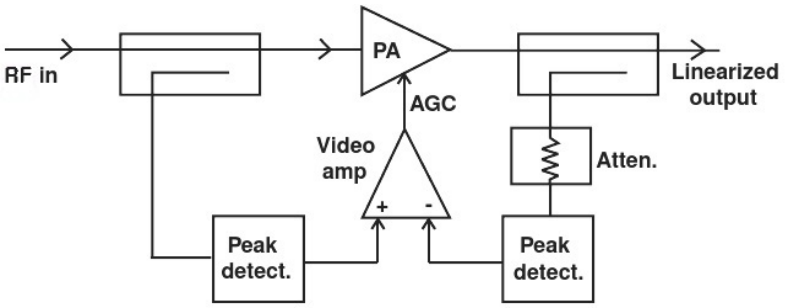

Figure 5: Envelope feedback system.[6]

3.3.3 Indirect feedback – The Polar Loop

The Polar loop is more complicated than simple envelope feedback with amplitude correction, as it also features phase correction (see Figure 6). As can be seen in the figure, the output signal is first down converted and then peak detectors are used to make amplitude comparison. After that, the PA is used to create amplitude modulation (AM) to the RF carrier. Similarly, a phase comparison is done, and a voltage controlled oscillator (VCO) is used to create phase modulation (PM).

The Polar loop has the usual problems of a limited BW resulting from a video signal processing and detection as well as from the phase delays. However, for single carrier systems with narrow BW, the Polar loop can offer substantial improvement to

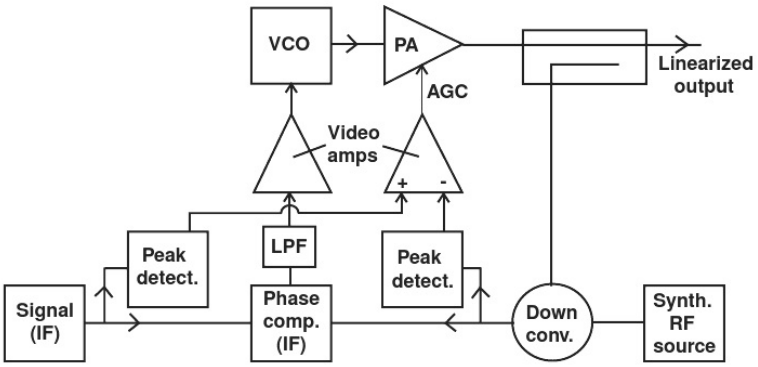

Figure 6: The Polar loop.[6]

IM performance. Being a system level linearization technique, it is fair to compare it to another system level linearization implementation. The Cartesian loop has been reported to have some benefits over the Polar loop (see Section 3.3.4).[6, 8, 7]

3.3.4 Indirect feedback – The Cartesian Loop

The Cartesian loop (see Figure 7) is considered more as a system level linearization method, rather as a PA linearization technique. The Cartesian loop can offer good reduction to IM products in modulation bandwidths smaller than 100 kHz, thus making it a suitable candidate for the TETRA system (see Section 2.2.1) [6, 7].

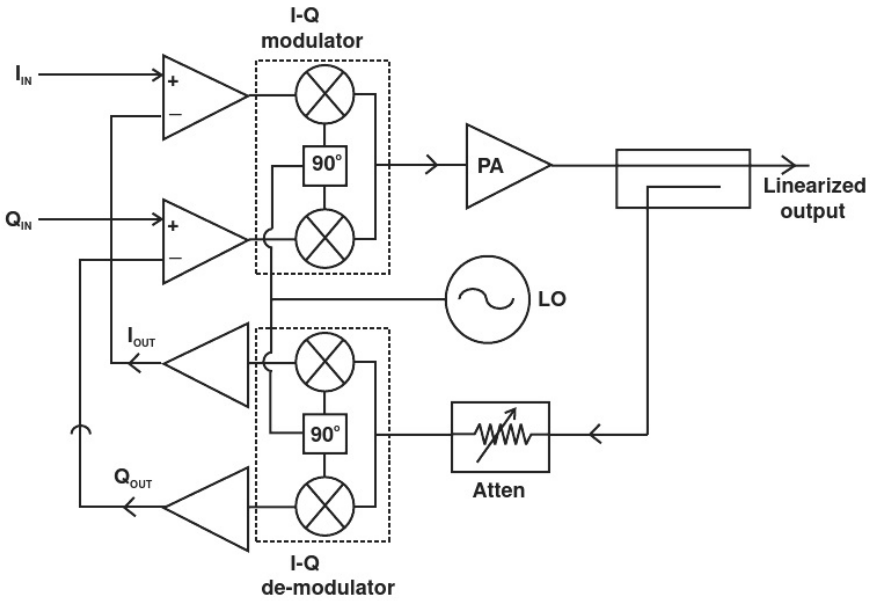

Figure 7: The Cartesian loop linearization system.[6]

In the Cartesian loop, output of the PA is coupled to the feedback path through linear attenuator. The feedback path must be as linear as possible to maximize the correction in the PA output. After the attenuator, the signal is down-converted

with a demodulator to I_{OUT} and Q_{OUT} signals. These signals include distortions caused by PA, and can be compared directly to original I_{IN} and Q_{IN} signals. The comparison is done by differential amplifiers at the input of the vector modulators. The gain of differential amplifiers ensures, that the output will follow closely the input I_{IN} and Q_{IN} signals.

The vector modulators are used to generate the actual RF signal $S(t)$ presented in equation (7),

$$S(t) = I(t)\cos\omega_c t + Q(t)\sin\omega_c t \tag{7}$$

where ω_c is the angular frequency of the carrier signal. The $S(t)$ is then amplified and the corrected signal is formed to the output of the PA. Linearization capabilities of the Cartesian loop depend mainly from two features of the circuit. The first is the gain and BW of the video circuitry, and the second is the linearity of the down-converter demodulators. The second feature is more critical, as any nonlinearities in the feedback path cause undesired corrections to the input signal.[6, 7]

The benefit of using the Cartesian loop linearization over the Polar loop, comes from the symmetry of the two quadrature signal paths, in the terms of gain and linearity. The symmetry reduces unwanted phase shifts that are causing problems in all correction systems.

4 Power amplifier design

In Section 4.1, requirements for power amplifier are presented, taking into account the TETRA standard requirements, previous stages in the amplifier chain, working environment and other requirements. Based on these requirements, a couple of power transistors are selected for the design process (see Section 4.2).

4.1 Requirements for power amplifier

4.1.1 Frequency bands

The designed PA needs to be able to operate in different frequency bands. Matching for those frequency bands can be done separately, but it is desirable to cover multiple bands with the same matching network. The required frequency bands are shown in Table 5. In this thesis, matching is done for the frequency band from 390 MHz to 400 MHz.

Table 5: Carrier frequency bands for the PA to cover.

Frequency bands
335 MHz – 351 MHz
361 MHz – 366 MHz
390 MHz – 400 MHz
420 MHz – 430 MHz
460 MHz – 470 MHz
851 MHz – 869 MHz

4.1.2 PA carrier signal power requirements

All power levels discussed in this section refer to the root-mean-square (RMS) power levels of the TETRA modulated signal. Therefore, the peak power levels are about 3.25 dB higher than the presented values. The PA is designed to power class 3 (see Table 2), delivering 42 dBm power for each carrier. As there are some losses between the power transistor output and transmitter output, the transistor is required to deliver 43 dBm power for a single carrier signal. As the maximum input power level from the amplifier chain is 30 dBm, at least 13 dB of power gain is required.

4.1.3 Linearity requirements

One of the key problems in the PA design is to achieve the desired linearity with high output power levels. In Table 3, the ACP limit for nearest channels (frequency offset of 25 kHz) is defined to -60 dBc for frequencies lower than 700 MHz. As the transmitter uses a Cartesian loop with the linearization capability of about 30 dB, it is possible to approximate that a single PA has to have an ACP smaller

than -30 dBc. Leaving some room for component tolerances and nonlinearities caused by other components, the ACP limit for the PA was set to -40 dBc. For other frequency offsets and carrier frequencies higher than 700 MHz, the decided limit stands proportional to the original TETRA standard limit. These limits are presented in Table 6.

Table 6: ACP limits for a single PA with different frequency offsets.

Frequency offset	Maximum ACP level ($f_c < 700$ MHz)	Maximum ACP level ($f_c > 700$ MHz)
25 kHz	-40 dBc	-35 dBc
50 and 75 kHz	-50 dBc	-45 dBc

4.1.4 Temperature related requirements

The designed PA must withstand changes in the ambient temperature, as defined in the TETRA standard, without breaking other TETRA requirements. The main concern is the reduction in linearity, as the temperature changes directly affect the characteristics of the power transistor. In critical temperatures, some easements to linearity requirements are done. The maximum instantaneous junction temperature is defined for the case where the system is operating in the worst defined environmental and operational conditions. The temperature related requirements are shown in Table 7.

Table 7: Temperature related requirements for the PA.

Requirement	Value
Maximum junction temperature	150 °C
Operational temperatures (The ambient temperature)	-25 – 60 °C

4.1.5 Power supply requirements

The power supply is not predefined, but the input voltage of the power supply is. The power supply has to be able to form the needed drain voltage V_{ds} from the input voltage of 10 to 32 V. The power supply has to be able to match the variations in the power consumption and it needs to be able to maintain the wanted drain voltage in the all specified operation conditions. The power supply design is not in the scope of this thesis.

4.2 Transistor selection

Selecting suitable transistor for the TETRA transmitter is not trivial, as the linearity requirements are quite strict. If the selected transistor cannot produce enough power without saturating, its linearity won't be sufficient. On the other hand, if the transistor is capable of producing too high power levels, driving it under its optimal performance will cause the efficiency to drop. In Sections 4.2.1 and 4.2.2 two transistors types are compared and the selected transistors are presented in Chapter 4.2.3

4.2.1 LDMOS transistors in general

LDMOS transistors are widely used in RF power amplifiers. They offer robustness, high efficiency and they are relatively inexpensive. With LDMOS transistors, required linearity, gain and high output power can be achieved with a single power supply. However, the linearity offered by LDMOS transistors is still inadequate, when the base station amplifiers are considered, resulting in use of linearization methods described in Section 3. [9]

4.2.2 GaN transistors in general

Generally GaN transistors operate much like LDMOS transistors, but they offer wider bandwidths and higher efficiency. The downside is that the GaN devices available today are still quite expensive compared to the LDMOS devices. Operationally the main difference between GaN and LDMOS transistors is that the GaN transistor is in a conductive state, when zero volt is applied to its gate. Negative biasing of the gate is required to keep the transistor closed. GaN transistors also suffer from a quite big temperature drifting, resulting in gain varying a lot depending on the output power level. To compensate the temperature drifting, more complex biasing circuit needs to be used. Another reason to use more complex biasing networks, is caused by the possible instability of the transistor, when small drain voltage is applied. Special biasing sequence needs to be use, to guarantee safe power up and down procedures. [10, 11]

4.2.3 Selected transistors

When selecting a transistor for a power amplifier, one needs to consider several factors. The most important factor is the output power level, as the transistor needs to be able to deliver the wanted power to the load. The used modulation affects the peak power level, and needs to be considered in this case. The design frequency is also important to be taken into account, so that transistor can be matched in the wanted frequency range. Some transistors are internally matched at a certain frequency, which can cause problems. The needed gain is an important requirement and the efficiency of the transistor is also most-valuable, not only for low current consumptions, but also for preventing heating problems. According to the requirements presented in Section 4.1, two transistors were selected for closer

inspection, one GaN and one LDMOS type. The selected LDMOS transistor is BLF6G10-45 from NXP and the selected GaN transistor is CLF1G0060-30 also from NXP. Other vendors and transistor models were also considered, but BLF6G10-45 and CLF1G0060-30 seemed more suitable. [12, 13]

4.3 IV characteristics of the selected power transistors

4.3.1 Power amplifier classes

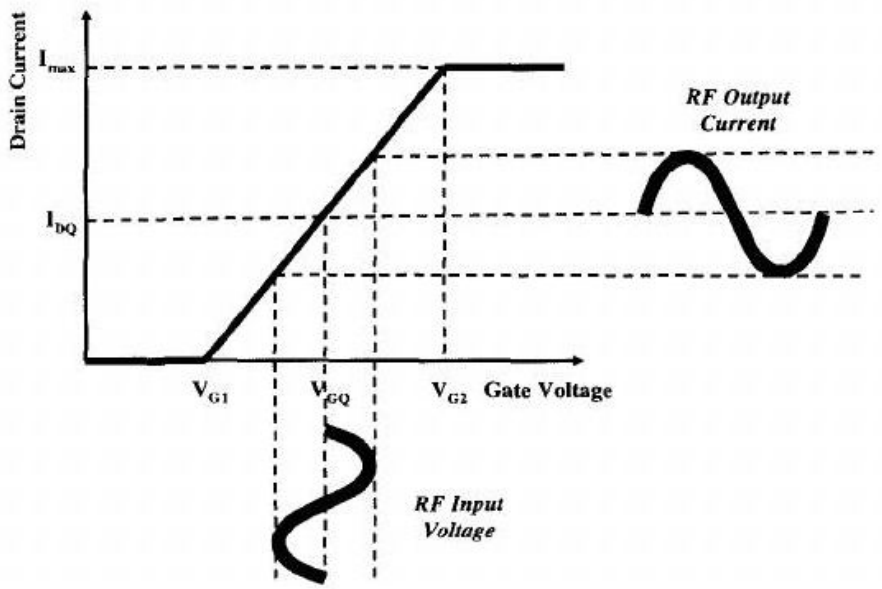

Figure 8: Idealized transfer characteristics of MOSFET power transistor.[9]

The biasing point of the transistor determines the amplifier class. Classically the biasing point of a metal-oxide-semiconductor field-effect transistor (MOSFET) is determined by the gate voltage V_{gs}, which is also called a quiescent gate voltage V_{GQ}. The V_{GQ} causes a quiescent drain current I_{DQ} to occur, depending on the V_{ds}. Figure 8 illustrates how V_{GQ} transfers to the drain current. As I_{DQ} stays all the time in the linear region (above zero and below I_{max}), the PA is biased to class A. If V_{GQ} is selected so that I_{DQ} is zero over half of the RF cycle, the amplifier is called a class B amplifier. This will increase the efficiency of the amplifier, as the DC current consumption is reduced. The drawback is the reduced linearity and the occurrence of harmonic components. The class AB amplifier is biased above a drain current conduction threshold, but lover than in class A, resulting in a decent linearity with higher efficiency than with a class A amplifier. Therefore, class AB amplifier offers the most suitable solution for the TETRA base station amplifiers. Class AB biasing is presented in Figure 9. It can be shown through a Fourier analysis, that reducing the conduction angle in class AB will not affect the fundamental frequency in a viewpoint of current waveforms. [7]

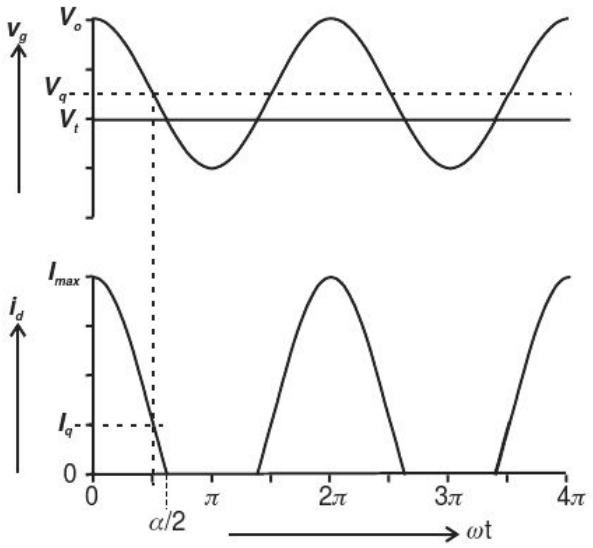

Figure 9: Class AB biasing of power transistor, where V_t is drain current conduction threshold, v_g is gate voltage, v_o drain output voltage, I_{max} is the saturation limit of drain current, I_d is the drain current, I_q is the quiescent drain current and the $\alpha/2$ is the drain current cutoff point. [7]

4.3.2 Biasing point of BLF6G10-45

BLF6G10-45 is designed to deliver maximum power of 45 W to the load with the typical efficiency of 60 %, when working in class AB. Typical I_{DQ}, given in datasheet, is set to be 350 mA and supply voltage, V_{ds}, is typically 28 V. Previous and other important values are presented in Table 8. In Figure 10, the drain current is illustrated as a function of the supply voltage with different gate voltages. The maximum allowed drain current is marked in the figure with a dashed line as well as the typical supply voltage. In Figure 10 it is easy to see that the drain current of 350 mA is achieved with a gate voltage near 2.25 V. As the gate threshold voltage $V_{gs(th)}$ can vary, V_{gs} is defined in Figure 11 for simulation purposes only. [12]

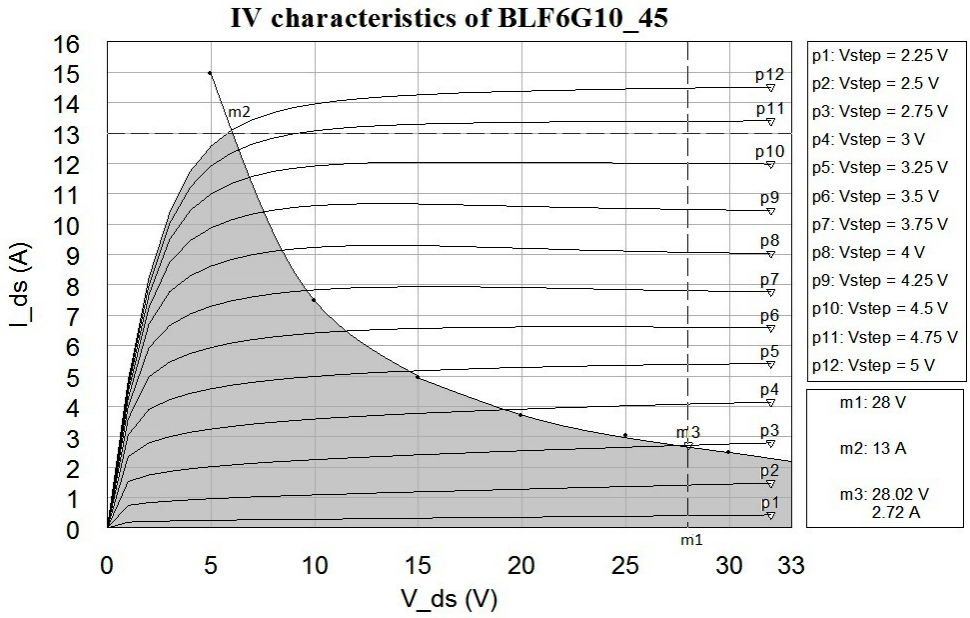

Figure 10: BLF6G10-45 drain current in function of supply voltage with different gate voltages. The gray area in figure presents power level under 45 W delivered to load with efficiency of 60%. The Vstep is the swept transistor gate to source voltage V_{gs}.

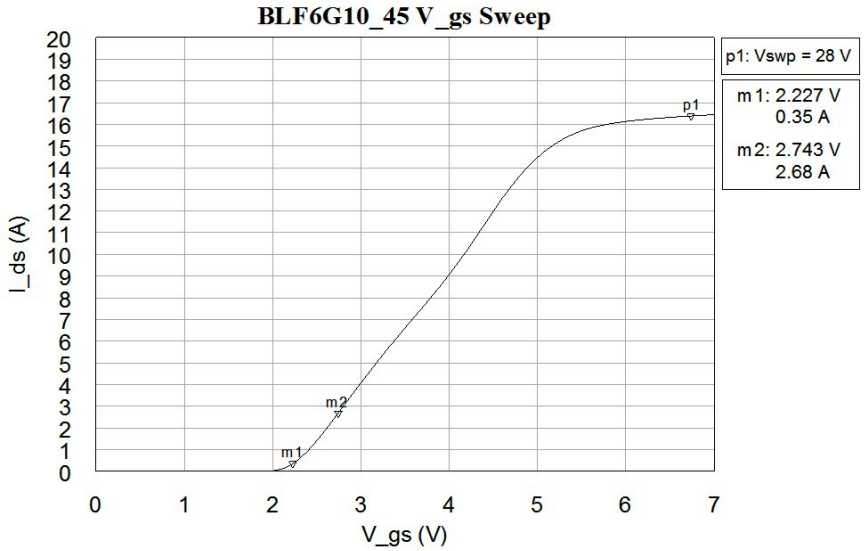

Figure 11: I_{ds} as a function of V_{gs} with supply voltage of 28 V. I_{ds} of 350 mA is achieved when $V_{gs} = 2.227$ V.

Table 8: BLF6G10-45 characteristics.

Parameter	Value
Drain to source breakdown voltage	65 V
Gate to source threshold voltage	1.35 - 2.35 V
Maximum junction temperature	225 °C
Typical gate to source quiescent voltage *)	2.15 V
Typical drain cut-off current **)	12.5 A
Typical efficiency	> 60 %
*) $V_{ds} = 28$ V and $I_{ds} = 430$ mA **) V_{gs} = threshold + 3.75 V and $V_{ds} = 10$ V	

4.3.3 Biasing point of CLF1G0060-30

CLF1G0060-30 is biased similarly as the BLF6G10-45 in Section 4.3.2, but the negative gate voltage must be applied, as the GaN transistors draw substantial current already at zero gate voltage. Typical characteristics of the CLF1G0060-30 are presented in Table 9. The typical quiescent current of the CLF1G0060-30 is defined to be 70 mA. This biasing is near the class B, but still in class AB. As the GaN transistors are in general more linear than the LDMOS transistors, typical value can be used as a start of design process. In Figure 12 the drain current is shown as a function of V_{gs}. [13]

Table 9: CLF1G0060-30 characteristics.

Parameter	Value
Drain to source breakdown voltage *)	150 V
Gate to source threshold voltage	-2.4 - (-1.6) V
Maximum junction temperature	250 °C
Typical drain to source quiescent current **)	70 mA
Typical drain cut-off current ***)	5.1 A
Typical efficiency in wide band operation	> 50 %
*) $V_{gs} = -7$ V and $I_{ds} = 7.2$ mA **) $V_{ds} = 50$ V ***) $V_{ds} = 50$ V and $V_{gs} = 3$ V	

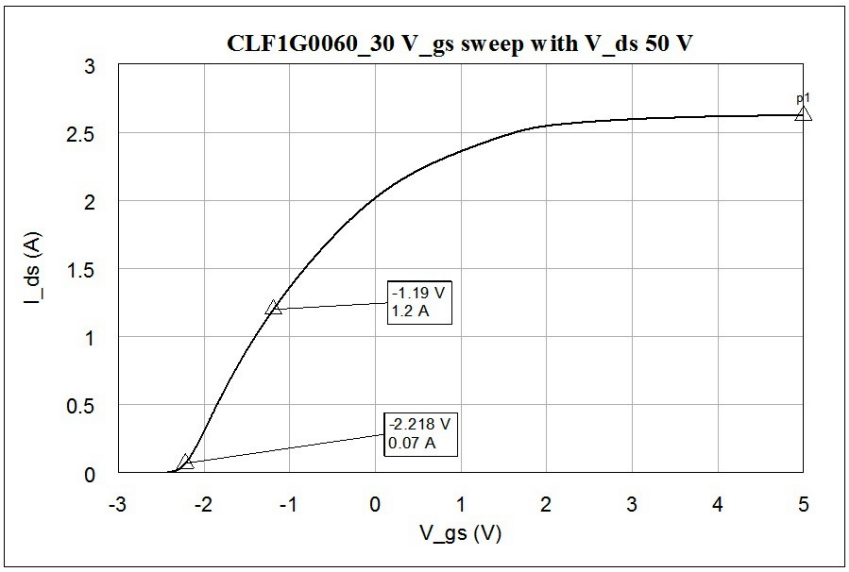

Figure 12: I_{ds} plotted as a function of V_{gs} with a supply voltage of 50 V. I_{ds} of 70 mA is achieved when $V_{gs} = 2.218$ V The current level where 30 W power is delivered to the load with a efficiency off 50 % is marked in as well.

4.3.4 Biasing circuitry

The purpose of the biasing circuitry is to set the biasing point for the transistor without interfering with the RF signal. There are many well studied biasing circuits for different purposes available. An example of biasing circuit suitable for power transistor is presented in Figure 13. In the example circuit, both DC voltages are connected to the transistor through inductors. The reason for this is that inductors offer very little resistance for DC and at the same time effectively block the RF signal from escaping to the bias circuitry. Small capacitors are used to form a RF ground at the input side of the bias inductor. There is also need for bigger capacitors to eliminate transients and other irregularities caused by the supply voltage. In drain side need for this is even bigger, as the large capacitor is also used to even fluctuations in the current. These fluctuations are caused by the varying RF signal envelope. To prevent stability issues, the large capacitor is not directly placed next to the RF short capacitor, but R_g and R_d are used to separate them. Using resistors here, is an effective way to prevent low frequency oscillations. However, on the drain side, an extra inductor is needed in parallel with a resistor R_d, so that the DC current can have a low resistance passage to drain. [7]

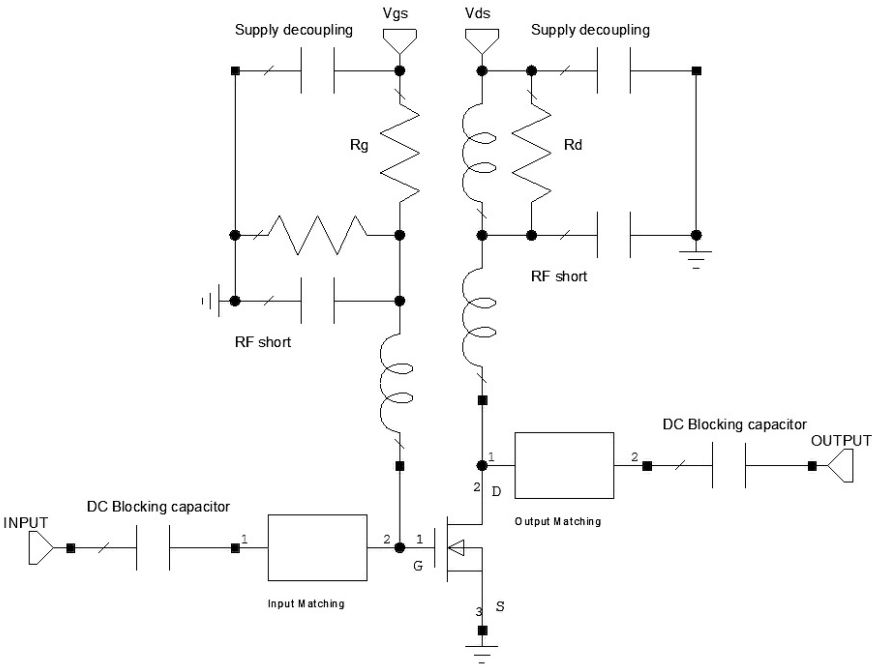

Figure 13: Example of transistor bias circuitry.

4.4 Load-pull simulation

4.4.1 Theory

In the low noise amplifier (LNA) design process, the input impedance of the transistor is matched so that the amplifier will have as small noise figure as possible. In that case, the impedance is usually different from the conjugately matched one. The PA output can be matched to deliver maximum power to the load. The Load-pull technique is a method to find out, what is that optimum output impedance to deliver maximum power to the load. Traditionally, a load-pull measurement is conducted by physically tuning the input and output impedances, while recording the output power level. The optimum load for the PA, R_{opt}, is the impedance, at which the maximum power level is achieved. It should be mentioned, that there is also some correlation between the input and output impedances. Therefore, iteration between the input and output impedance tuning is necessary. [7]

The load-pull measurements can be conducted with commercial equipment (see Figure 14), but as nonlinear models of power transistors and nonlinear circuit simulators have become more reliable, it has become possible to conduct load-pull simulations. In both cases, the process is the same. At first, the input of the PA is matched conjugately, providing close enough matching so that output matching can be tuned. Secondly, the output matching is tuned so that maximum power is delivered to the load. After the desired output matching is achieved, the input matching needs to be tuned again, to get desired amplification. The reason for this is that the output matching also affects the input matching and vice versa. Therefore, multiple iterations between input and output tuning might be required. In

this thesis, Advanced Wave Research (AWR) Microwave Office (MWO) is used to conduct load-pull simulations for various transistors. The conducted simulations are presented in Sections 4.4.2 and 4.4.3. These simulations are used as a base of the design process. [7]

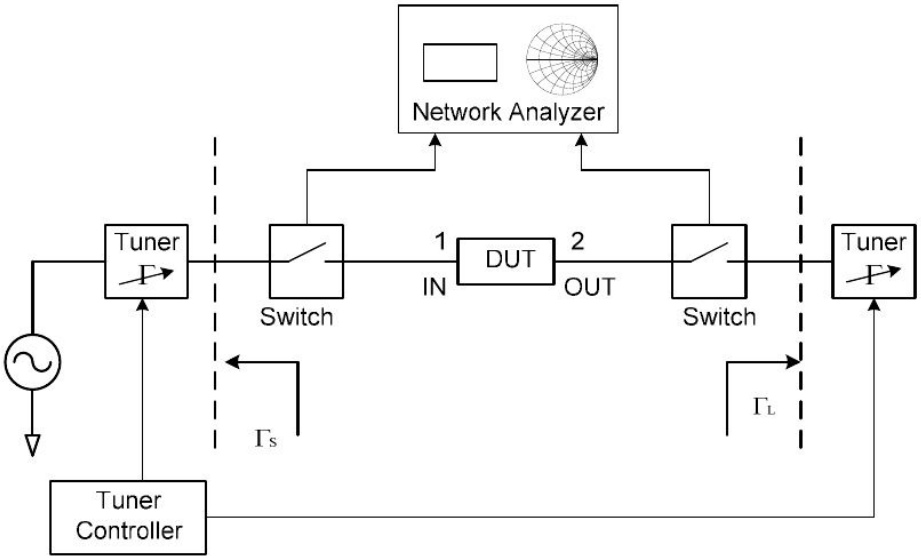

Figure 14: Example of load-pull configuration.[14]

4.4.2 Basic load-pull simulation

At first, input reflection coefficient S_{11} is plotted, so that the transistor's input can be conjugately matched. These plotted values for both transistors are presented in Figure 15. It is clear from Figure 15, that BLF6G10-45 is pre-matched, as the data sheet says. The models used in the simulations are from NXP RF power model library. The transistors were biased as discussed in Section 4.3.4 and no additional circuit elements were used beside the transistor models. [15]

Secondly, load-pull simulations were conducted at frequency of 395 MHz. The achieved results are very idealized, as only transistor models are simulated. However, results are accurate enough to give reference for output impedance matching. At this point, iteration between input and output tuning was not done, because it was left for more realistic case, including biasing circuitry, and microstrip pads for a transistor. The load-pull was done with different input power levels, as the optimum output impedance was noticed to change a little.

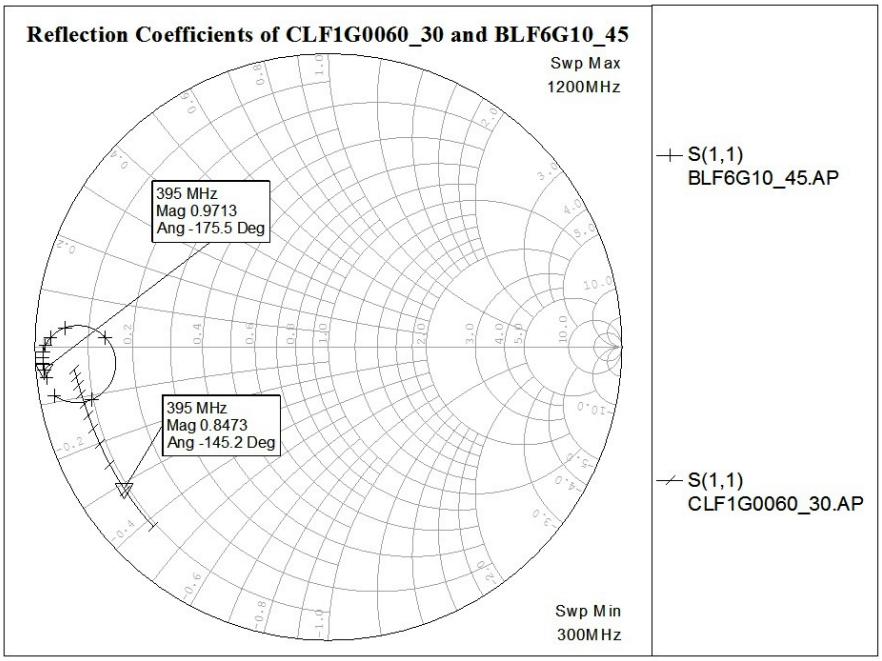

Figure 15: Reflection coefficients of BLF6G10-45 and CLF1G0060-30 plotted with frequency range from 300 to 1200 MHz.

Results of the load-pull simulation for BLF6G10-45 in an ideal case can be found in Figure 16. Even though the maximum output power is an important parameter of the PA design, it is equally important to keep linearity, stability and input matching under control. Therefore, the found optimum impedance for maximum output power is not likely to be the design goal but merely a starting point. One should also notice, that achieved gain in simulation is over 30 dB, which is quite a bit more than what the data sheet defines for typical gain. It is most likely caused by the idealistic nature of the simulation setup. [12]

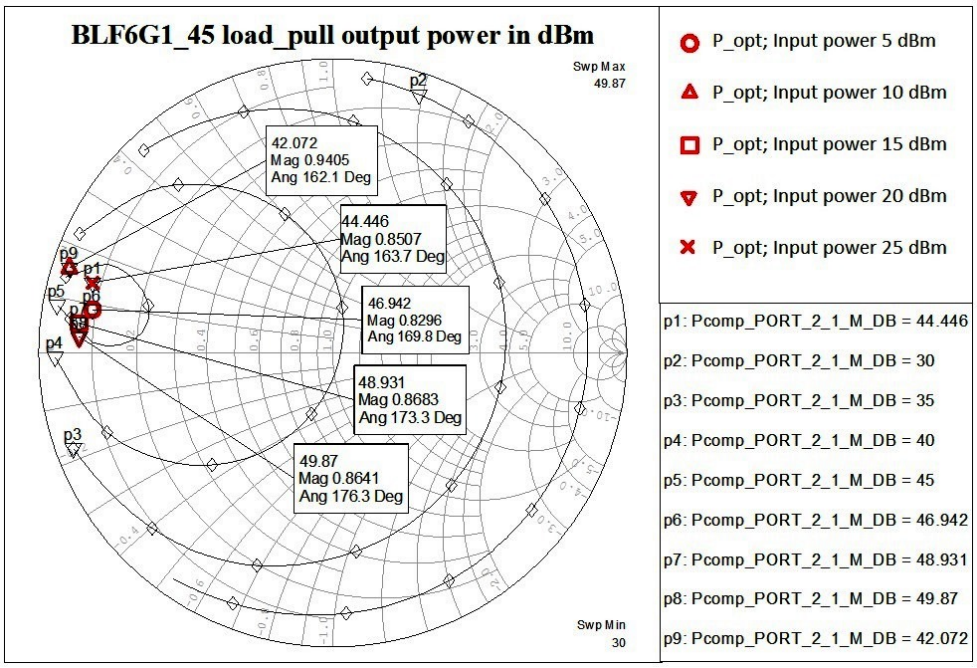

Figure 16: Output power contours plotted with input power level of 15 dBm. Additionally optimum impedance matching points for input power levels of 5, 10, 15, 20 and 25 dBm from top to bottom are presented accordingly.

In the case of CLF1G0060-30, load-pull simulation was done similarly. The results of this simulation can be found in Figure 17. The optimum output impedances for the GaN transistor with different input power levels are more even. With the input power levels of -5 dBm and below, the results are almost identical, but with higher levels, the optimum impedance point changes a little. With input power level of 5 dBm, the transistor model begins to function incorrectly. The gain of the transistor is very high, and undoubtedly is a result of good input matching, which the GaN transistors do not necessarily need. According the test results provided by NXP, GaN transistors can achieve over 15 dB gain with a S_{11} only -3 dB. More precise study is provided in Section 4.4.3.[16]

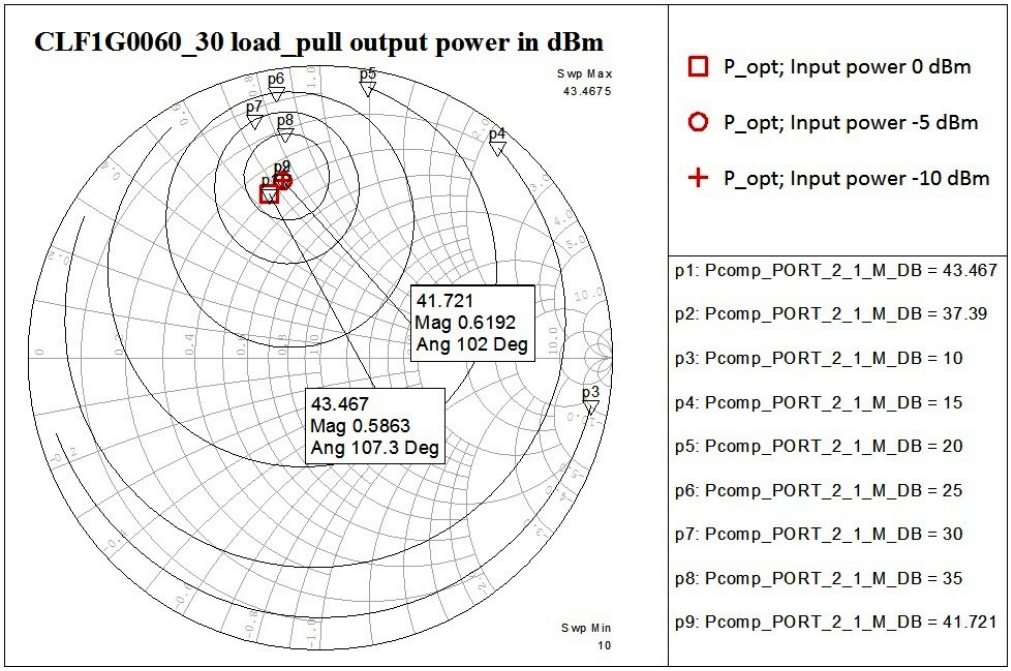

Figure 17: Output power contours plotted with input power level of -5 dBm. Additionally optimum impedance matching points for input power levels of -10, -5, and 0 dBm are presented.

4.4.3 Advanced load-pull simulation

As described in Section 4.4.2, there is a need to add some components to the simulation, to get more realistic results. In this section, biasing network as presented in Section 4.3.4, is added to the load-pull simulations along with microstrip pads and other unideal elements. The sizes of the soldering pads for the transistors gate and drain are defined by the used demo board. Therefore, similar pads are used in the simulation as well. The properties of the used printed circuit board (PCB) or demo board, also define the properties of the used microstrip layer structure in simulation.

The used static relative permittivity or relative dielectric constant ε_r in simulation is defined to be 4.5. The PCB manufacturer gives a range of possible permittivities, but practice has shown that 4.5 is a good enough approximation to be used in simulations. The substrate thickness h is 1.6 mm and even thought the PCB has seven conductive layers, the RF signal paths are using the furthest conductive layer as a ground layer. The conductor thickness t is 0.05 mm and the loss tangent $tan\delta$ is 0.02. The conductor is made of copper, which has an electrical resistivity of 16.78 nΩm. By normalizing the electrical resistivity of gold 24.4 nΩm, we get normalized metal bulk resistivity ρ of 0.688. The electrical resistivity of gold was defined by AWR. All presented properties of PCB are defined in AWR in block called *Microstrip substrate definition* (MSUB) and will be used in all simulations here onwards, if not mentioned otherwise. [17, 18]

The simulation circuit for BLF6G10-45 is presented in Figure 18. Input power is selectable through variable *pwr* and it is varied during load-pull simulations. The

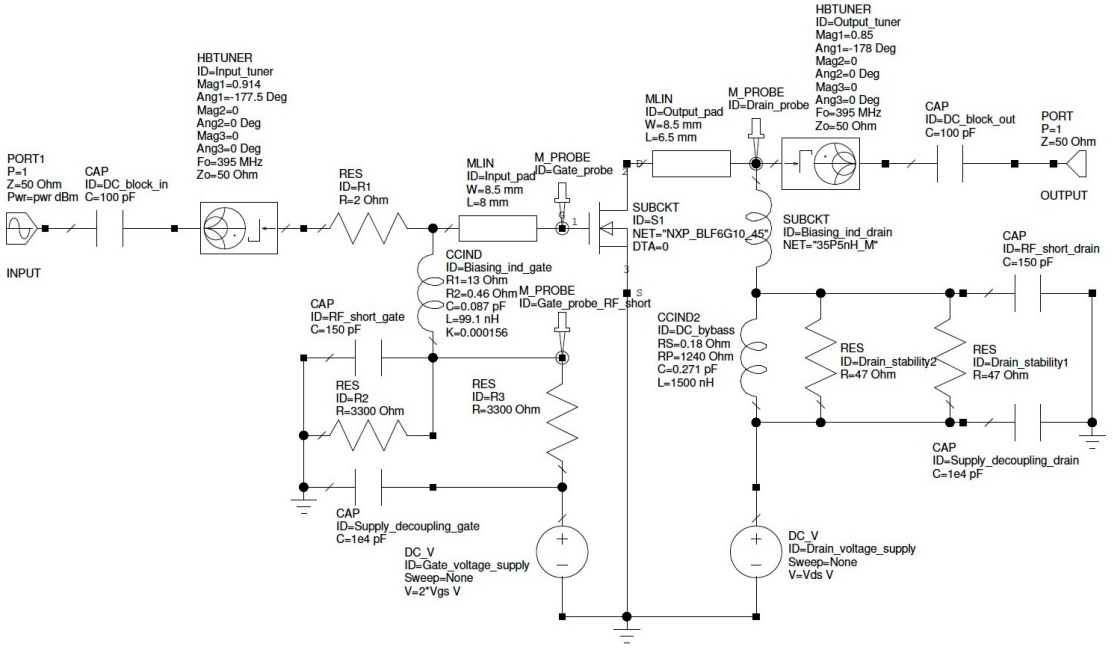

Figure 18: Load-pull simulation setup with bias circuitry and transistor soldering pads.

Harmonic balance lossless tuners (HBTUNER) blocks are used to tune input and output impedances. Ideal voltage sources are used to generate supply voltages, but the biasing circuitry is constructed so that the sources could be also unideal. The Dimensions of the transistor gate and drain microstrip pads can be also seen in the figure. The same circuitry without HBTUNER blocks is also used to simulate small signal reflection coefficients to get the conjugately matched input impedance. There is also an extra resistor added to the transistor gate at the signal path, to provide more room for input matching and to add stability. However, the resistor value should not be too large due to the surface mounted resistors' weak power durability. At the gate side, the voltage supply is defined to have two times the desired gate biasing voltage, as the voltage is divided with two 3.3 kΩ resistors. In the drain side, the supply voltage is directly coupled through two inductors, causing it to drop a little, due to the losses caused by them. This drop is also compensated by increasing the drain side supply voltage. All the lumped elements used in the simulation, other than inductors, are ideal ones. Use of unideal models of inductors is beneficial, as they have the biggest impact to the input and output matching. [19]

The simulated reflection coefficients are presented in Figure 19. The reflection coefficient was plotted from 300 MHz to 2 GHz and the conjugate of the marked value at 395 MHz was used as the initial input match. The load-pull simulation with input power levels from 15 dBm to 30 dBm were conducted. These results can be seen in Figure 20 a). The point $p8$ was selected for output matching, to get optimum power matching. Next, with the selected output matching, load-pull for S_{11} was conducted. These results are presented in Figure 19. To achieve better

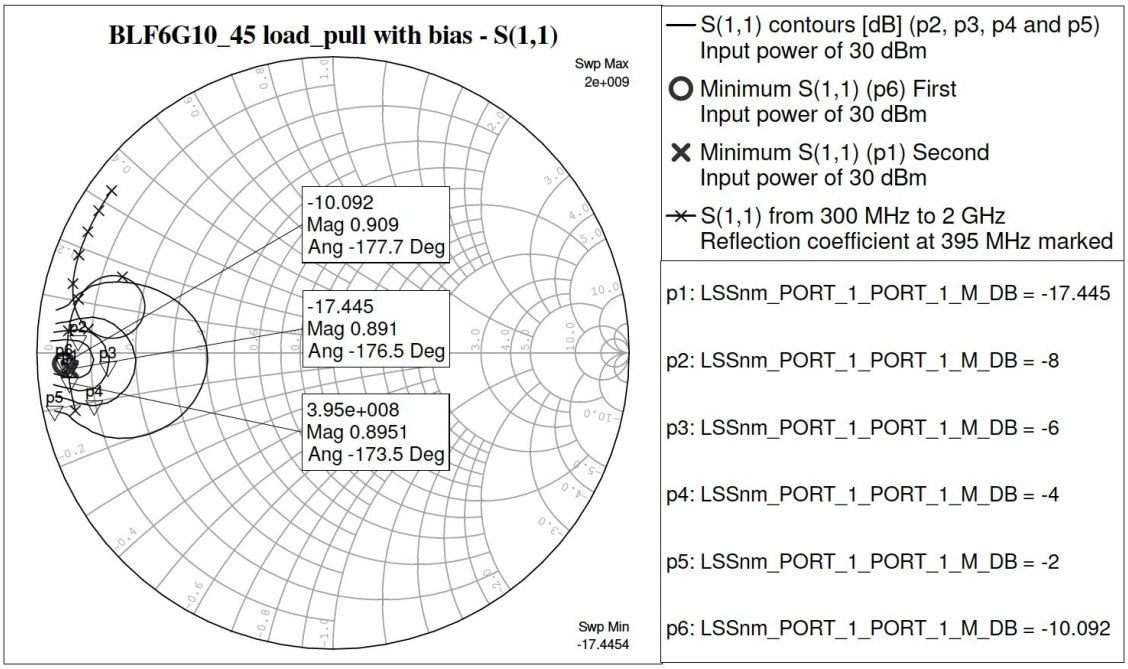

Figure 19: Reflection coefficient from 300 MHz to 2 GHz plotted and its value at the frequency of 395 MHz is presented. Also the minimum of S_{11} with the first and second load-pull iteration rounds are marked along with S_{11} contours.

input matching than with the conjugately matched case, point $p6$ was selected for the input matching, and the load-pull simulation for output power was conducted again. Simulation results can be seen in Figure 20 b). In that figure, also the input reflection coefficient is plotted with different output terminations. Some correlation between the input matching and output termination can be seen, but with the desired output power levels, all terminations are possible. The gain contours are not plotted in Figure 20 *b*) as they are nearly identical with the output power contours. The plotted power contours show, that it is possible to choose any impedance inside the smallest contour plot, to get the desired power output power level of 46 dBm As the smallest plot contour is the limit of 47 dBm output power, it leaves some room for errors.

The results of the load-pull simulation are verified with a simple input power sweep. Input power is swept from low levels to the saturation point and the transistor circuit gain, output power and input reflection coefficient are monitored. With the selected input and output matching impedances, the transistor's 1 dB gain compression point is at the input power level of 27.2 dBm. The corresponding output power level is 48.0 dBm, which is more than sufficient to guarantee linear operation with a TETRA modulated signal with the needed output power level of 43 dBm. See Figure 21 for results.

Next, the load-pull simulation was conducted for CLF1G0060-30. The simulation procedure differs from the one with the LDMOS transistor, as there is stronger correlation between output and input matching. Also, the GaN transistor can achieve

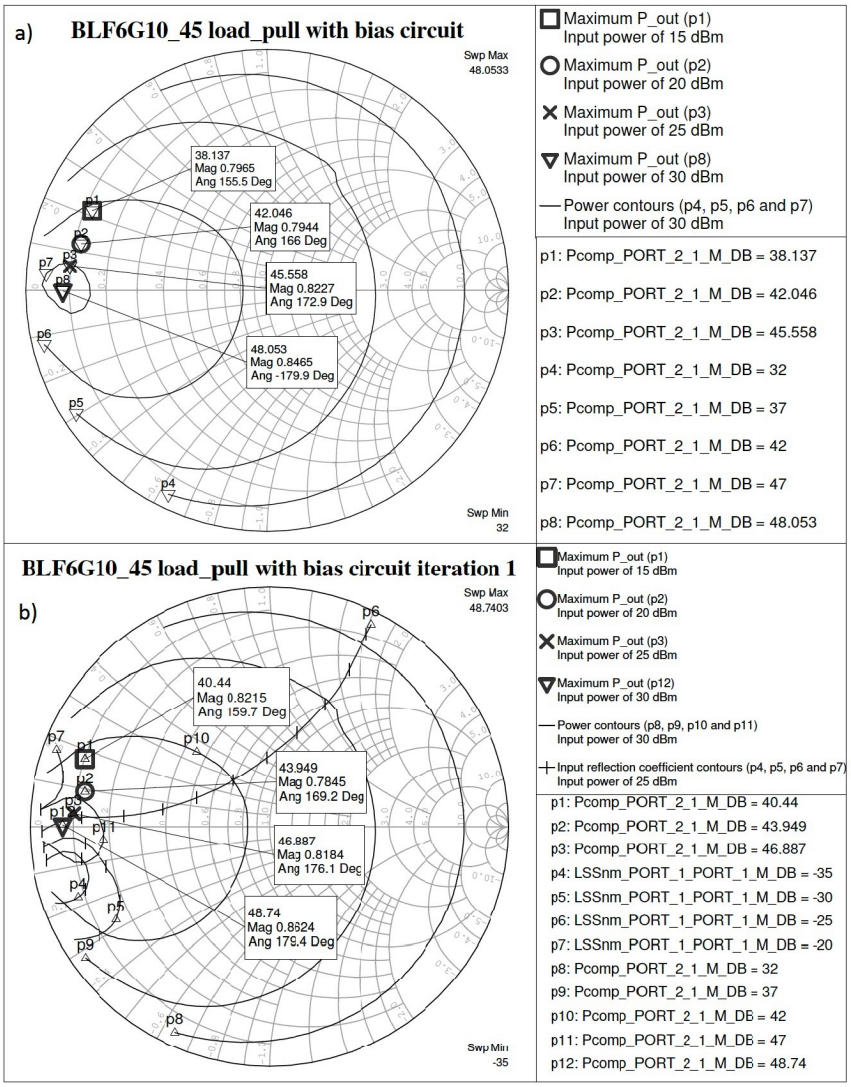

Figure 20: a) Load-pull simulation of BLF6G10-45 with biasing circuitry included. Input is conjugately matched. Optimum impedance matching points with different input powers are marked. b) First iteration round of load-pull simulation after tuning the input matching. Optimum impedance matching points with different input powers are marked.

decent gain without a good input matching. However, mismatch at the input can cause high voltage standing wave ratio (VSWR), which can at the worst case damage or break the transistor. Reflected power can also cause problems in the previous stages in the amplifier chain. Therefore, input matching must not be neglected. As said before, there is greater correlation between the input and output ports of the GaN transistor than with the LDMOS transistor. To present this correlation, the input reflection coefficient is presented as a function of the output impedance in Figure 22.

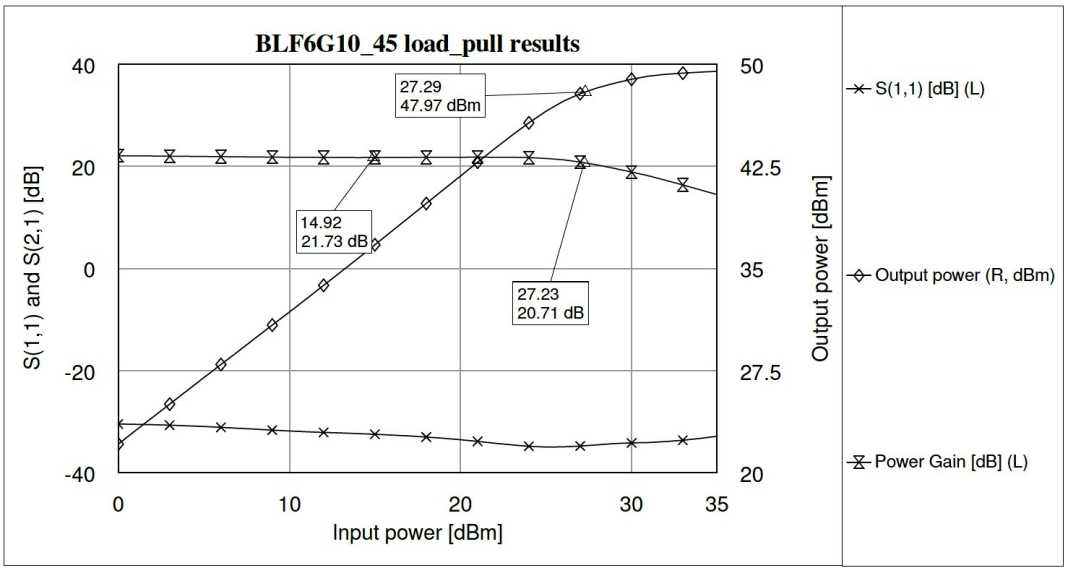

Figure 21: Verification of BLF6G10-45 load-pull simulation. The power gain, output power and input reflection coefficient plotted as a function of input power at the frequency of 395 MHz.

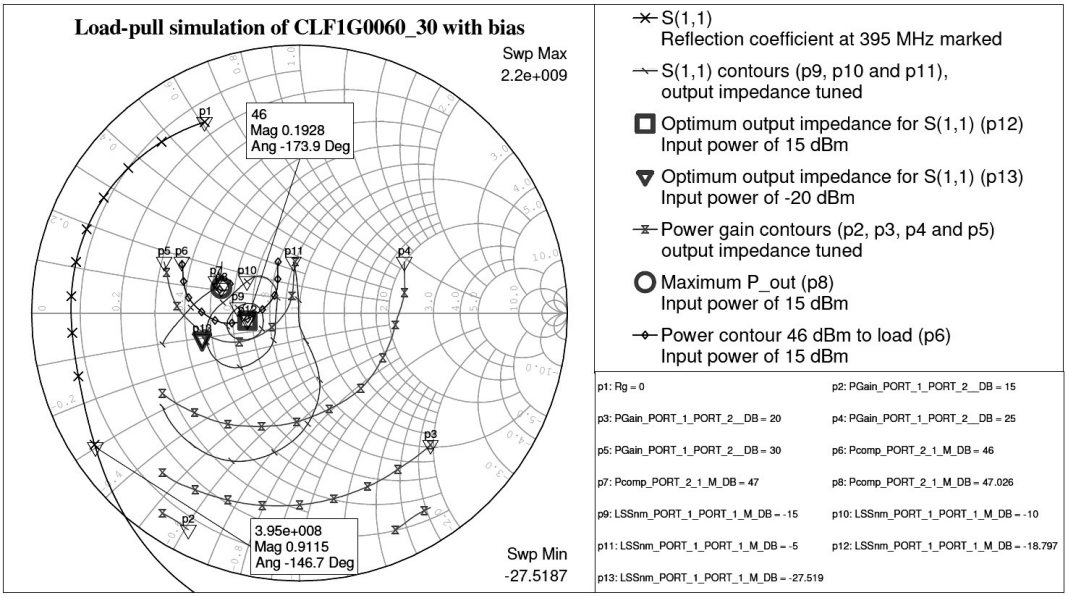

Figure 22: S_{11} plotted from 200 MHz to 2.2 GHz and the input reflection coefficient at the frequency of 395 MHz is marked. Conjugately matched at 395 MHz, the output is tuned to plot S_{11}, power gain and power delivered to load. The optimum load impedance for S_{11} and power delivered to load are marked.

The optimum output impedance, where good input matching can be achieved, changes a little as a function of the input power, see *Optimum output impedance for* S_{11} points $p12$ and $p13$ in Figure 22, but if the optimum output impedance for the higher input power level is selected, good input matching is achievable with all needed input power levels. In Figure 22, also the optimum output impedance for maximum P_{out} is plotted, and the load impedance where output power of 46 dBm is achieved, is presented. The gain contours are not presented, as they correlate with output power contours. The marked impedance point is now selected to be the output matching goal.

Similarly, as with the BLF6G10-45, the load-pull simulation for CLF1G0060-30 can be iterated. However, when the input source-pull simulation was conducted, it was discovered that the conjugately matched input offers near optimum matching with the selected load impedance, and can be used as a design goal. Naturally, the correlation between the input and output of the transistor will cause the optimum input impedance to change along with the output impedance. Therefore, multiple input and output impedance pairs can offer similar transfer characteristics for the transistor. A benefit of using the selected matching is that the output impedance is quite near to 50 Ω keeping the output matching circuit simple.

The conducted source- and load-pull simulation has given the input and output impedance goals for both transistors. It is now possible to design matching circuits, that convert 50 Ω input and output impedances to the desired goal impedances. In Section 4.5 matching circuits are discussed, and possible solutions for the input and output matching circuits for both transistors are presented.

4.5 Matching circuits

The simplest and perhaps the most widely used option to match one impedance to another, is to use a lowpass matching network. In its simplest form, the lowpass network consists of one series inductance followed by a parallel capacitance. The bandwidth that can be achieved with such a matching network, depends strongly on the matching ratio. In other words, if a small impedance needs to be matched to a large impedance, the bandwidth becomes narrow. In the case of power transistors, the impedance to be matched is usually small, and the load impedance large, typically 50 Ω, resulting in a narrow bandwidth. More bandwidth can be achieved, if a multistage network is used. However, the required lumped element values can become too large or small to realize, and alternative matching methods need to be used. In Section 4.5.1, single stage matching network is presented, and lumped element values for desired input and output matching impedances for both transistor models are calculated. Later in that section, a multistage matching network is presented, and simulations with such a network are conducted. [7]

4.5.1 Lowpass matching networks

In Figure 23, an example of a single stage lowpass matching network is presented.

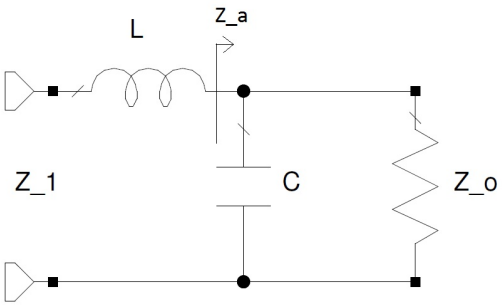

Figure 23: Single stage lowpass matching network. Z_1 is matched to Z_0.

The matching network transforms Z_1 to Z_0 with the series inductance and parallel capacitance. If Z_0 is resistive, R_0, we can calculate the impedance Z_a, which is formed by parallel components C and R_0.

$$Z_a = \frac{R_0}{1 + jR_0\omega C} = \frac{R_0(1 - jR_0\omega C)}{1 + (R_o\omega C)^2} \tag{8}$$

and therefore the real part of the Z_a is

$$Re(Z_a) = \frac{R_0}{1 + (R_o\omega C)^2} = Re(Z_1) \tag{9}$$

Now it possible to calculate the needed capacitance.

$$C = \frac{\sqrt{\frac{R_0}{Re(Z_1)} - 1}}{\omega R_0} \tag{10}$$

The inductor value can be calculated form the following equation

$$\omega L = \frac{R_0^2\omega C}{1 + (R_0\omega C)^2} + Im(Z_1), \tag{11}$$

which simplifies to

$$L = \frac{R_0^2 C}{1 + (R_0\omega C)^2}, \tag{12}$$

if Z_1 is resistive.

Now it is possible to calculate with equations (10) and (11) the needed component values to match the transistors with a single stage matching networks. Calculated matching network element values are shown in Table 10. The results achieved with matching networks correlate with the results achieved with idealistic loads. Good correlation is most likely a result of the used ideal lumped elements in matching circuits, and unideal models need to be used, before similar results can be expected from real-life measurements.

It is usually practical to replace the lumped element series inductors with simple microstrip lines. With microstrips, it is possible to make needed impedances

Table 10: Single stage matching networks for BLF6G10-45 and CLF1G0060-30 to center frequency of 395 MHz.

Matched element	$Im(Z_1)$ [Ω]	$Re(Z_1)$ [Ω]	C [pF]	*)L [nH]	**)L [nH]	Stub length l [mm]
CLF1G0060-30 input	14.93	2.52	34.98	4.41	10.42	58
CLF1G0060-30 output	-1.44	33.89	5.56	9.41	8.83	50
BLF6G10-45 input	1	2.39	36.00	4.29	3.89	23
BLF6G10-45 output	0	3.69	28.53	5.3	5.3	31
*) Calculated with equation (12) **) Calculated with equation (11)						

accurately and there is no need to restrain to the component values offered by the manufacturers. Another benefit is that multiple frequency variants of the PA can be produced to the same layout, simply by changing the place and values of capacitors. However, the downside is, that the needed stub can be quite long in low frequencies, requiring large area in PCB. For example, the needed stub to replace the inductor for CLF1G0060-30 input, would be nearly 58 mm. The length of the required stub can be calculated from equation (13)

$$l = \frac{1}{\beta}\left[n\pi + arctan\left(\frac{\omega L}{Z_0}\right)\right], \tag{13}$$

where l is the length of the stub, $n = 0, 1, 2...$ and the phase constant $\beta = 2\pi/\lambda$.

As said before, single stage matching networks are rarely used, because their narrow bandwidth properties in the case of a large impedance ratio. A solution is to use multiple stages to transform the impedance to the intermediate impedance, before transforming it to the desired impedance. The intermediate resistance R_M can be defined as in equation (14)

$$R_M = \sqrt{R_1 R_0}, \tag{14}$$

where $R_1 = Re(Z_1)$. Compared to single stage matching, a wider frequency bandwidth is achieved. In Figure 24, comparison of one stage matching networks to two stage input matching is done for BLF6G10-45. About 20 MHz increase for the -1 dB frequency bandwidth is achieved. Also the S_{11} -10 dB bandwidth is increased dramatically. Unfortunately, the two stage matching circuit requires nearly double the space compared to the one stage matching circuit.

If a broader frequency bandwidth is desired, it is required to use more complex matching networks. One possibility is to compensate the changing gain with selective mismatch in lower frequencies. Another method is to compensate the gain differences with the lossy equalizing networks. However, in TETRA systems, the required frequency bandwidths are quite narrow, thus making wideband matching unnecessary. Taking into account the need of multiple frequency variants, a simple two stage matching network was selected to be used. Some modifications are

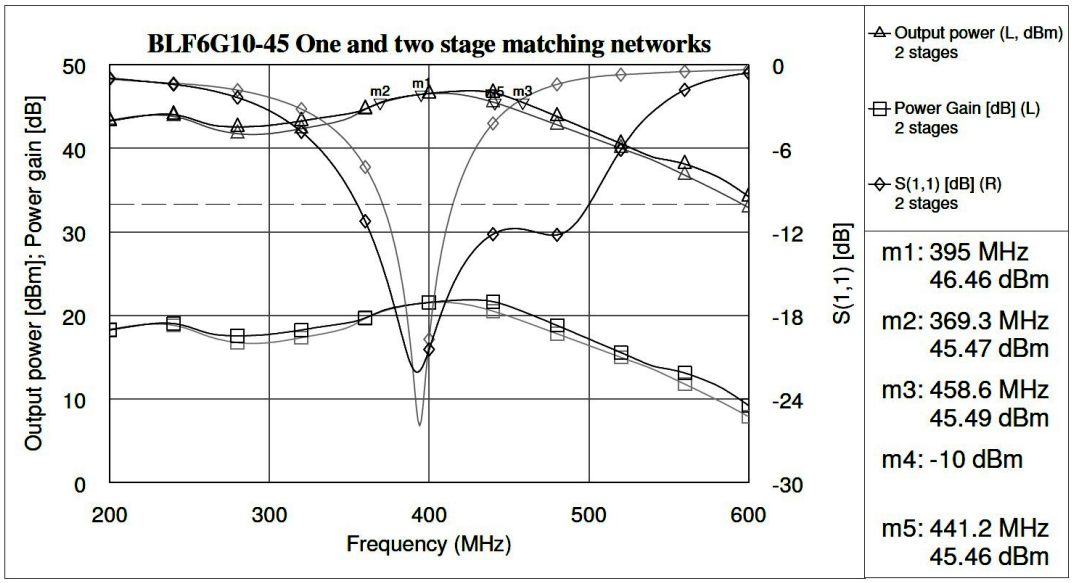

Figure 24: Single stage lowpass matching network compared to two stage input matching and one stage output matching. Darker plots are with two stage matching. The -1 dB output power low and high frequency limits for both cases are marked. Dashed line marks -10 dB for S_{11}.

needed to make matching circuits smaller and to compensate nonlinearities of the used lumped elements. Optimization of matching circuits is described in Section 4.6. [20]

4.6 Matching circuit optimization

As there is limited space available on the PCB board, where the amplifier circuit needs to be constructed, previously presented one and two stage matching circuits need to be modified to fit that space. One option is to use different matching circuit topology, but as the same layout of matching circuitry needs to fit for multiple frequency variants, it is better just to make some modifications to the LC matching network. With AWR, it is possible easily to tune the matching circuitry so that it fits in a smaller space, without losing too much of its functionality.

The used demo board characteristics also affect the matching circuitry, as the aim is to prove, that the selected transistors are suitable for TETRA PA use. On the demo board, transistors gate and drain are connected to 44 mm long microstrip lines, which can be connected to the ground plane, with surface mounted capacitors, from any point along the microstrip line. The width of the microstrip line is 1.5 mm, which means it has an impedance about 70 Ω, thus making the impedance change small after the last capacitor. Using the AWR optimizer, the lowpass matching circuitry was optimized to fit the available space on the demo board.

4.6.1 Prototype matching circuit of BLF6G10-45

Two-stage lowpass type of circuitry was taken to be a base of the optimized matching circuit. The inductors were replaced with 1.5 mm wide microstrip lines and ideal capacitors were used. The AWR optimizer was used to find the optimum positions and capacitor values, so that matching circuits were able to fit in the reserved space. The optimization was done by setting goals for the desired gain, input matching and output power. The ideal capacitors were replaced with the real capacitor models having a nominal value as close as possible to the values given by the optimizer. After the replacement, places along the microstrip were tuned again. In Figure 25, the -1 dB compression point of the amplifier circuit is presented. Two stage LC matching circuits were used both in input and output matching. Compared to the load-pull simulation presented in Section 4.4.3, the achieved maximum output power is about 2 dB lower.

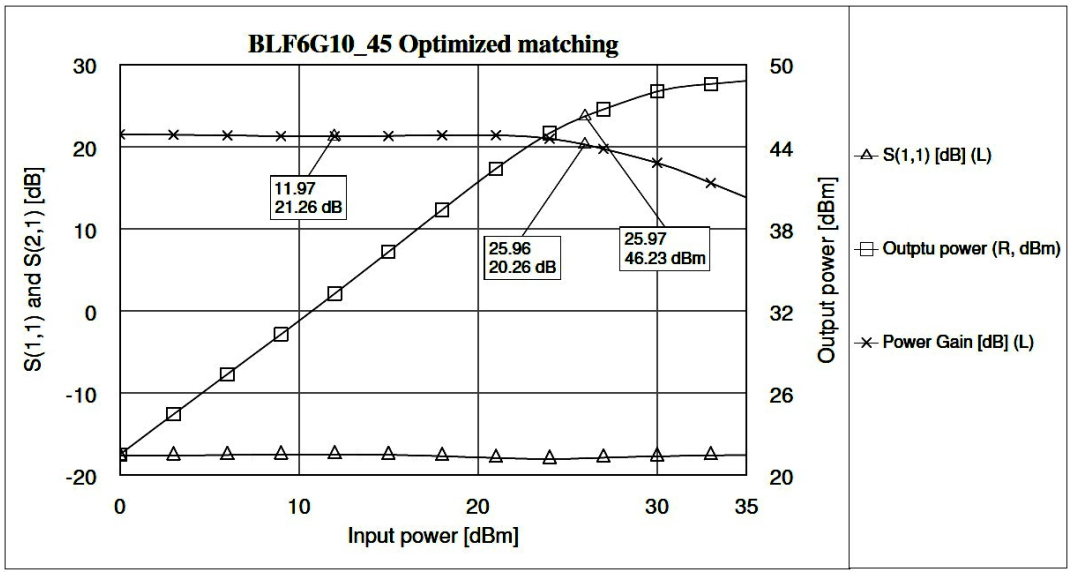

Figure 25: Matching circuit optimized to fit to the demo board. The -1 *dB* compression point is marked.

The achieved output power level is still acceptable and can be improved in prototype construction. Limitations of the used demo board restrain the possible matching circuits and undoubtedly better matching can be achieved, if restrictions are removed. However, it is crucial to be able to compare simulated results to the measured results, so the simulated demo board matching circuit was constructed based on this optimized matching circuit design. The stability of the circuit was also checked by calculating geometric stability factor μ (see Section 4.7), and the circuit were found to be stable from 200 MHz to 600 MHz. The stability factors were calculated by using the small signal scattering parameters, so there is still a possibility of unstable operation at large signal levels. If such an event occurred, more precise stability analysis should be conducted.

4.6.2 CLF1G0060-30 verification board

Due to the given time frame and the short supply of CLF1G0060-30 samples, measurements of CLF1G0060-30 were conducted with a transistor evaluation circuitry provided by the transistor manufacturer. The complexity of required bias controlling, due to the high temperature drift and possible instability with power up and down sequences, also supported the use of the evaluation board. The evaluation board had a very wide frequency band matching, which illustrates very well the best side of the GaN technology. Changes to evaluation board were not allowed, but conclusions of the capability of GaN transistors matched to a narrower bandwidth could still be made.

4.7 Two-port stability

Stability of the two port can be checked with the geometrical stability factor μ. μ defines the distance to the nearest unstable point from the center of the Smith chart in reflection plane. Therefore, if μ is over 1, the circuit is unconditionally stable. The μ for the source and load sides can be calculated from equations (15) and (16)

$$\mu_S = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}^* \Delta| + |S_{21} S_{12}|} \tag{15}$$

$$\mu_L = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}^* \Delta| + |S_{21} S_{12}|}, \tag{16}$$

where

$$\Delta = |S_{11} S_{22}| - S_{12} S_{21} \tag{17}$$

and the * indicates the complex conjugate. [21]

5 Measurements

For the measurements, BLF6G10-45 was assembled on a demo board (see Figure 26). The matching circuits were constructed based on the simulations presented in Section 4.5. The biasing circuitry was implemented as described in Section 4.3.4. Separate laboratory power supplies were used to make the gate and the drain bias voltages. The gate voltage was manually tuned until the desired drain current was achieved. Measuring the gate voltage is not sufficient, as the typical quiescent voltage can vary.

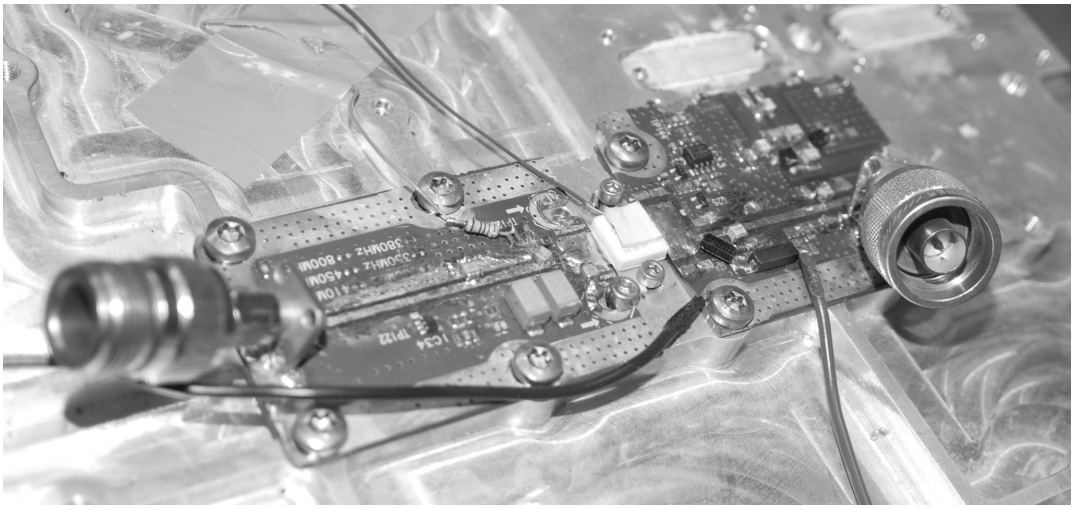

Figure 26: Constructed BLF6G10 demo board.

SMA connectors were soldered to the input and the output of the demo assembly. The SMA connector's signal pin was soldered to DC cut capacitor and the edge of the SMA was attached to the mechanics under the demo board. The whole demo board was also attached to the mechanics. The transistor was placed between two pieces of PCB and the gate and the drain pads were soldered to the microstrip pads on PCB. Transistor's heat sink was also bolted to the mechanics.

5.1 Scattering parameters, output power, efficiency and temperature

To test the capability of the PA design, multiple basic properties were measured, including scattering parameters, current consumption, output power and the transistor package temperature. The measurement setup is presented in Figure 27. A network analyzer was used to generate the input signal, but an external amplifier was needed to get a large enough signal power level. The external amplifier was connected to the directional coupler, which was connected to the designed PA. The output power level of the PA was monitored throughout the measurement. The output of the PA was connected to an attenuator, which was connected back to the network analyzer. The current consumption of the PA was monitored with a

multimeter and the temperature of the power transistor package was measured with a thermometer.

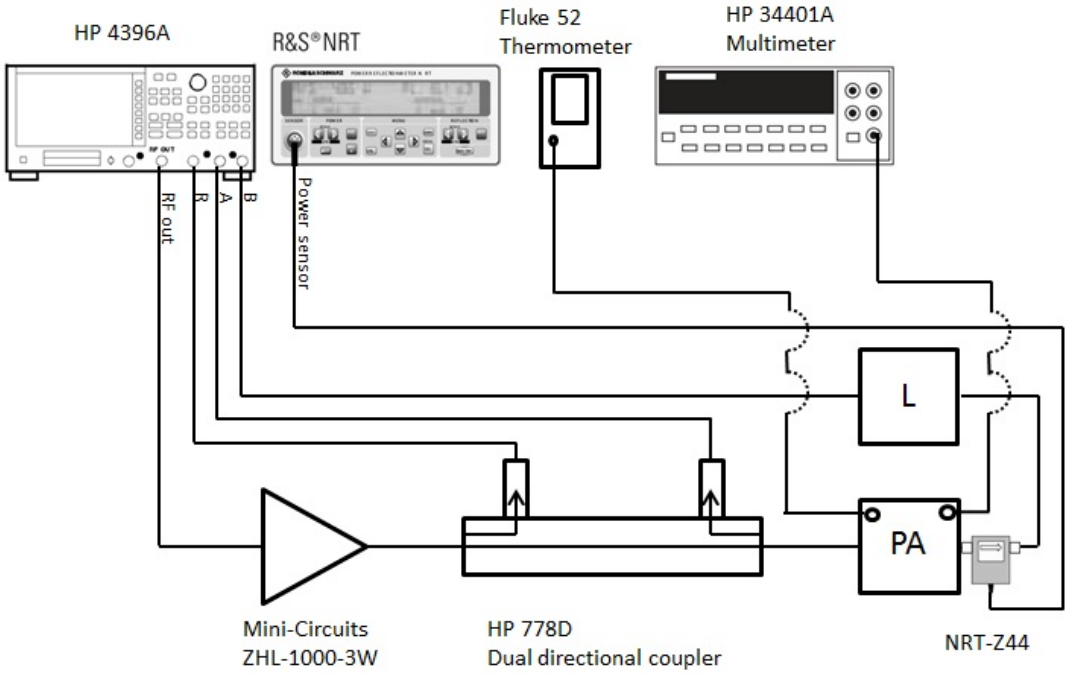

Figure 27: Measurement setup to measure scattering parameters, output power, current consumption and temperature. [22, 23, 24, 25, 26]

The power transistor's junction temperature T_j was calculated from the measured transistor package temperature T_p. Derivation was done with equation (18)

$$T_j = (P_{tot} - P_L) * R_{th} + T_p, \tag{18}$$

where P_{tot} is the total power consumption of the transistor, P_L is the power delivered to the load, and R_{th} is the thermal resistance from a junction to the case defined by the vendor of the transistor. The power added efficiency of the PA can be calculated from

$$PAE = \frac{P_L - P_{in}}{P_{DC}}, \tag{19}$$

where P_{DC} is calculated from the DC current consumption and drain supply voltage. The input power P_{in} is derived from the measured output power and power gain.

5.1.1 BLF6G10-45 scattering parameters and output power

Scattering parameters of BLF6G10-45 were measured as a function of frequency and as a function of output power. The measurement was conducted with the setup presented in Figure 27. The transistor was biased to have a drain voltage of 28 V with I_{dq} of 350 mA. The correct I_{dq} was formed by tuning the gate voltage. External laboratory power supply was used to form the biasing conditions and needed current. In Figure 28, the output power of BLF6G10-45 is plotted and the -1 dB compression point is marked. The achieved -1 dB compression point is a little bit under the desired output power limit of 46 dBm, but as the ACP measurement in Section 5.2.1 shows, the needed linearity is still achieved. For all measured output power levels, S_{11} is steadily under -18 dB and the uncompressed gain is 20.3 dB. All together, the designed PA fulfills the requirements regarding the gain and the maximum output power level.

Comparison to the simulation results is shown in Figure 29. As can be seen, the there is a high correlation between the simulation results and the actual measured results. There is about 1 dB difference in gain at the linear region, and the achived -1 dB compression point is a bit less compared to the simulation results. S_{11} is practically same in both cases.

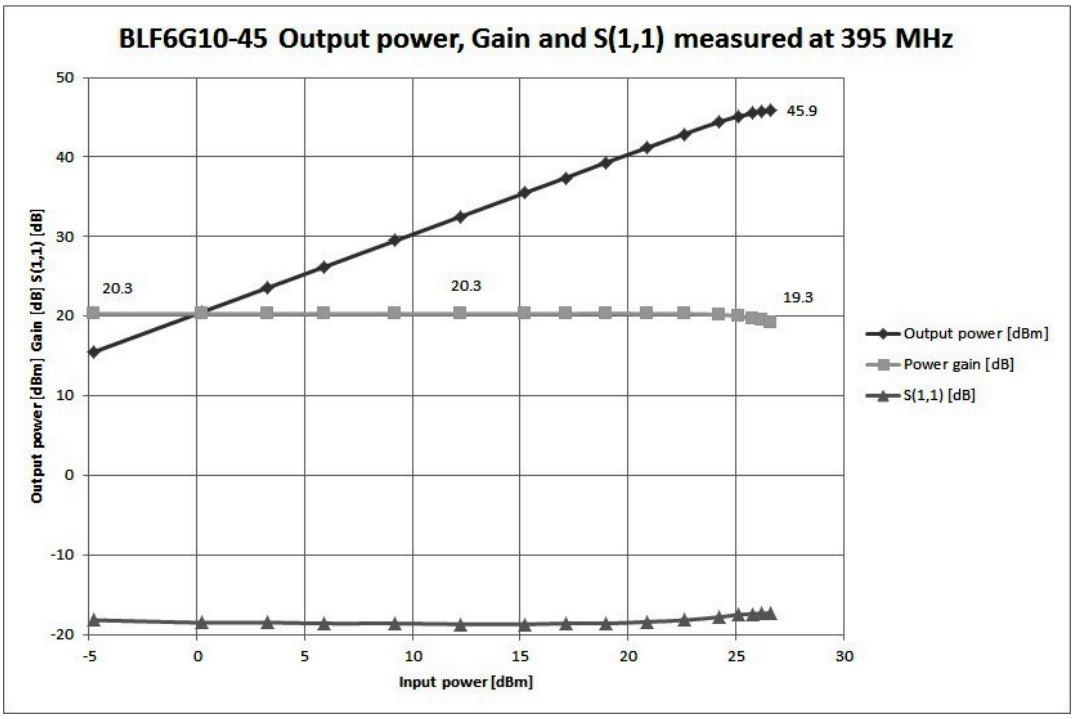

Figure 28: BLF6G10-45 output power, gain and S_{11} as a function of input power. -1 dB compression is achieved when 45.9 dBm is delivered to the load.

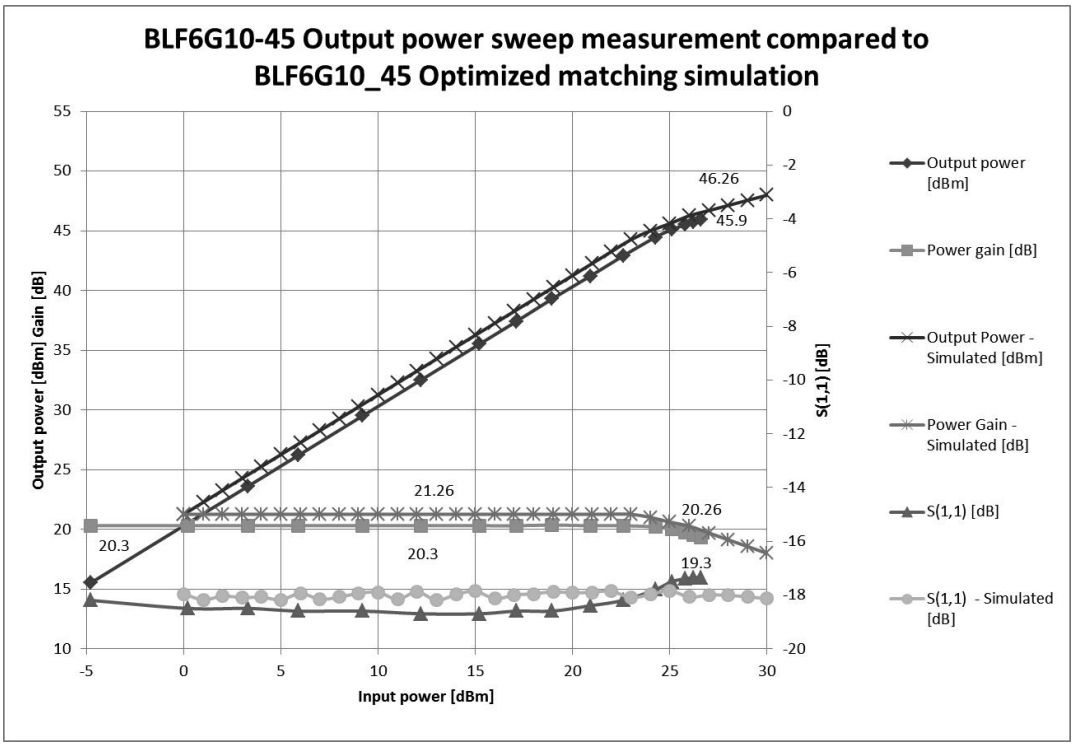

Figure 29: BLF6G10-45 simulation results compared to the measured results. Note that the S_{11} plots are in rigth side y - axis.

5.1.2 BLF6G10-45 temperature and efficiency

During the power sweep measurement, the current consumption and the transistor package temperature were monitored. In Figure 30, the transistor's junction temperature and PAE are plotted as a function of the output power. The achieved PAE is about 45 % at the designed maximum output power level, which is a relatively good result. During the design process, it was discovered, that higher efficiency would lead to insufficient linearity. The plotted transistor junction temperature was calculated from the transistor package temperature. Measured temperature of 89 degrees, is within the design limits. There is also enough room for the temperature to get worse, when the base station is operating in higher ambient temperature.

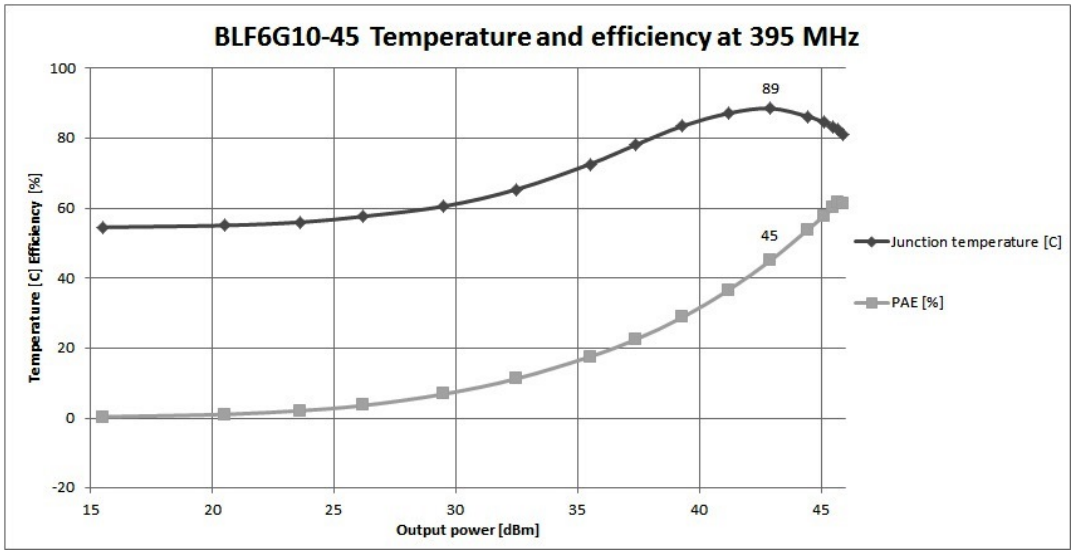

Figure 30: BLF6G10-45 PAE and junction temperature measured. PAE and transistor junction temperature at the output power level of 43 dBm are marked in the figure.

5.2 ACP measurements

The measurement was conducted with IFR 2310 TETRA signal analyzer, which can conduct measurements defined in ETSI, EN 300 394-1. The TETRA modulated signal was generated with the TETRA transmitter in test mode. The transmitter was transmitting pseudorandom data, and its ACP properties, compared to the measured amplifier, were good. An attenuator was used to limit the output power of the transmitter, preventing too large input signals. Also the output of the measured PA was limited with an attenuator to guarantee a safe input power level for IFR 2310. The measurement setup is presented in Figure 31.[27, 5]

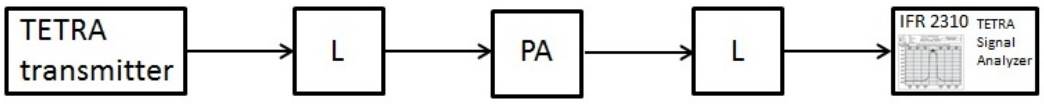

Figure 31: ACP measurement setup.

The allowed power levels for the adjacent channels were defined in Section 4.1.3. With IFR 2310, it is possible to measure the average power levels of three upper and lower 25 kHz channels simultaneously. As the linearity of the PA changes as a function of output power level, the measurement was conducted with several output power levels. The channels right next to the transmitting channel, ±25 kHz, have the highest off-band power levels, and therefore measurement results for those channels are described in detail.

5.2.1 BLF6G10-45 ACP measurement of ±25 kHz

The ACP of BLF6G10-45 was measured with different output power levels. The presented 25 kHz channel power levels are average values measured over 200 bursts, as defined in the TETRA standard. In Figure 32, measured average adjacent channel power levels are presented as a function of output power. With all three measured frequencies, covering the whole design bandwidth, the PA fulfills the design criteria. However, at the designed maximum output power level (43 dBm), the ACP begins to come near the limit of -40 dBc. Therefore, more linear design could be beneficial to avoid problems caused by production and component tolerances. On the other hand, if the linearity is increased, efficiency will suffer. The measurement was at the same time conducted with the channels ±50 kHz and ±75 kHz from the carrier frequency. The ACP with these second and third adjacent channels was over 10 dB better, compared to first adjacent channel, with all measured output power levels, thus fulfilling the requirements.

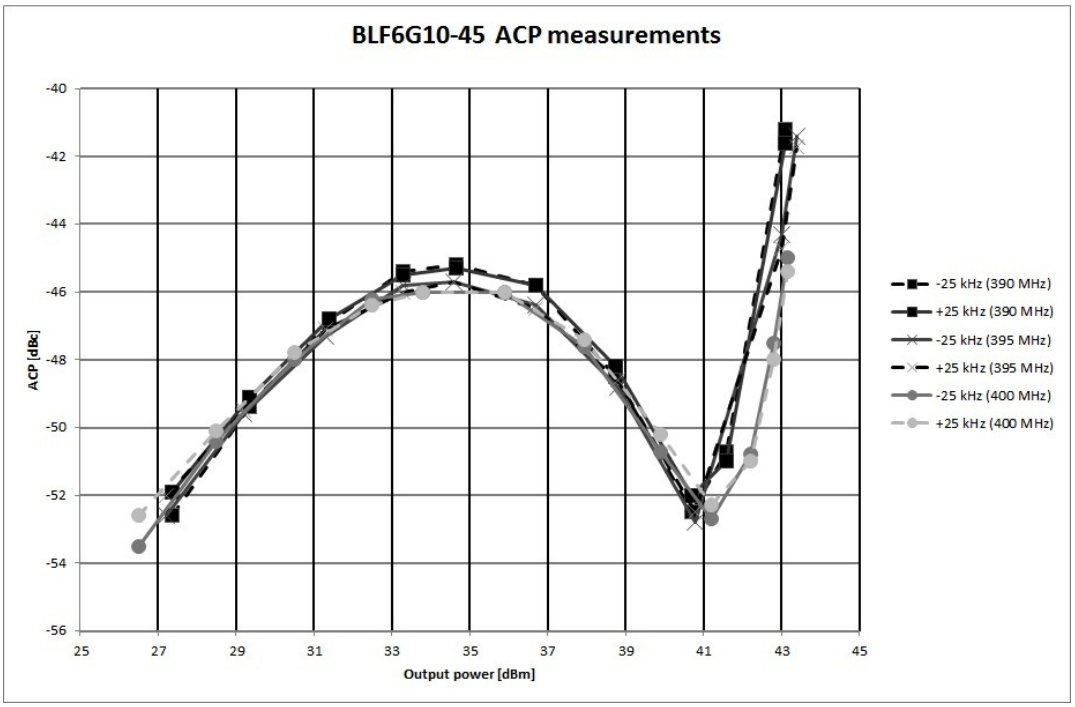

Figure 32: BLF6G10-45 ACP measurement with carrier frequencies of 390, 395 and 400 MHz.

5.3 BLF6G10-45 prototype measured with existing transmitter

To verify the linearity of the selected transistor, the demo assembly of BLF6G10-45 was connected to the Cartesian loop of the existing TETRA base station transmitter. The test setup is shown in Figure 33.

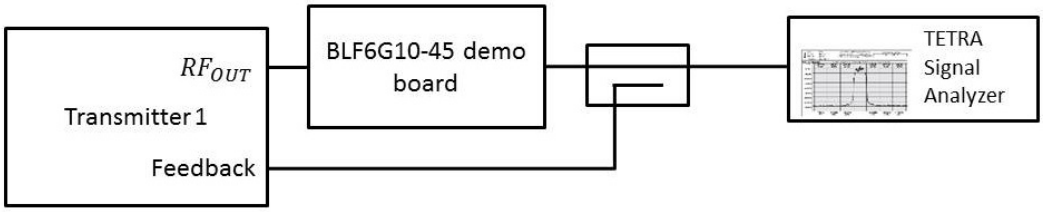

Figure 33: Test setup for the demo assembly included to the Cartesian loop.

The measured results are presented in Table 11. The measurement was conducted using the designed maximum power level of 43 dBm. Three different frequencies were selected from 395 MHz to 400 MHz to cover the upper half of the operating frequency band. Only the upper half of the frequency band was usable due to used filters in the TETRA transmitter in question. With all the measured frequencies with any given frequency offset, the linearized PA fulfills the requirements of the TETRA standard (see Table 3).

Table 11: ACP measurement of BLF6G10-45 when attached to the Cartesian loop.

	Measured power level compared the the carrier signal level [dBc]					
Carrier frequency [MHz]	Frequency offset -75 MHz	Frequency offset -50 MHz	Frequency offset -25 MHz	Frequency offset +25 MHz	Frequency offset +50 MHz	Frequency offset +75 MHz
395	78.5	74.4	66.2	67.1	73.6	77.5
397.5	79.0	75.1	65.6	67.4	73.9	78
400	78.0	75.0	65.1	67.5	74.1	77.9

6 Adding PA to amplifier chain of TETRA base station

The designed PA is added to be a part of the PA chain in TETRA base station transmitter (see Section 6.1). As the TETRA base station can contain multiple transmitters, adding the designed PA to the TETRA base station containing one or two transmitters, is addressed in this section. If the base station in question has two transmitters, two of the designed PA needs two be used in parallel (see Section 6.2).

6.1 The designed PA added to the existing transmitter design

As can be seen in Figure 34, the designed PA is added at the end of the existing PA chain. The existing directional coupler can be left as it is, if another coupler is placed after the added PA, thus making it possible to use the existing design, if wanted. As the designed PA adds gain to the PA chain, the feedback attenuator is tuned to compensate the added gain. It is also possible to use less coupling to the feedback, so that there is no need for an extra attenuation.

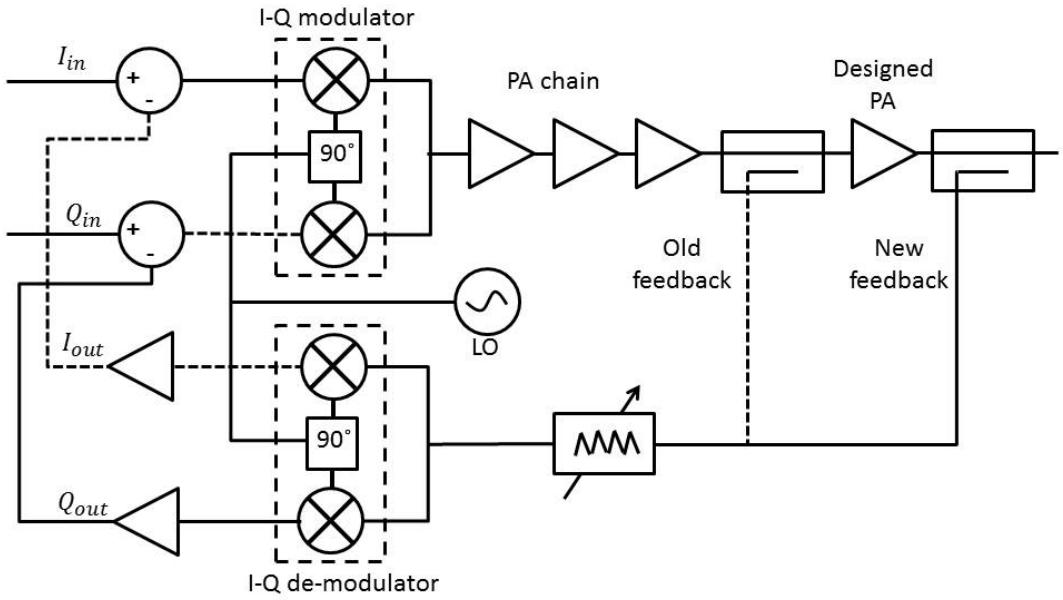

Figure 34: Designed PA added to the existing transmitter design.

The existing transmitter is constructed on a single PCB. The designed PA is

not added to the same PCB with a transmitter, as there is a need to keep the existing design backward compliant. Therefore, the designed PA is implemented on a separate PCB. As it was mentioned before, the TETRA base station can contain multiple transmitters. So it was reasonable to implement two separate PA to the same PCB for two transmitter operation (see Section 6.2).

6.2 The designed PA with two transmitters.

The TETRA base station with the two transmitters can operate in two different modes. In the first mode (see Section 6.2.1), signals from the transmitter are combined to a single feed, thus making possible to use a single antenna for both transmitters. In the second mode (see Section 6.2.2), the combiner is bypassed and each transmitter is used separately.

6.2.1 Two transmitter in combined mode

In a combined mode, the designed PA are used parallel as shown in Figure 35. The existing transmitters are otherwise unchanged, except that the feedback is taken from the designed PA. The signal is fed from the RF output of the transmitter to the designed PA input. The signal is then coupled to the feedback, before it is

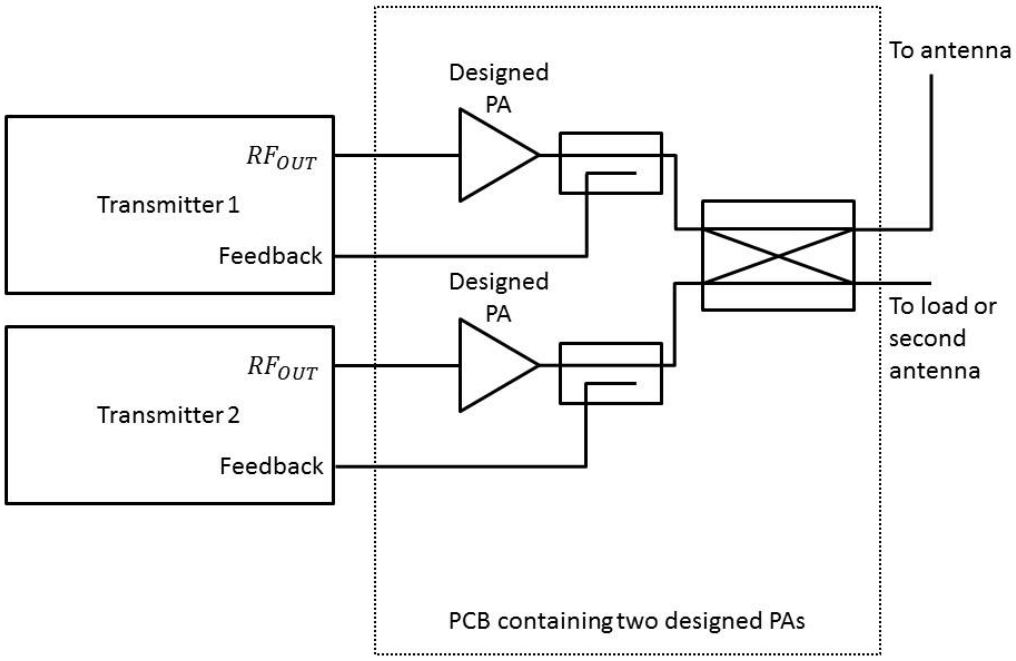

Figure 35: Designed PAs added in combined mode.

combined with the second transmitter signal. Each output of the combiner consists

the both transmitter signals. It is possible only to use one of the combined signals by adding a load to the second output, or it is also possible to use both outputs with separate antennas. The total power going into the antenna is the same as without the combining, minus the losses caused by the combiner, but the power of the each carrier is a half of the power compared to the bypass mode.

6.2.2 Two transmitters in bypass mode

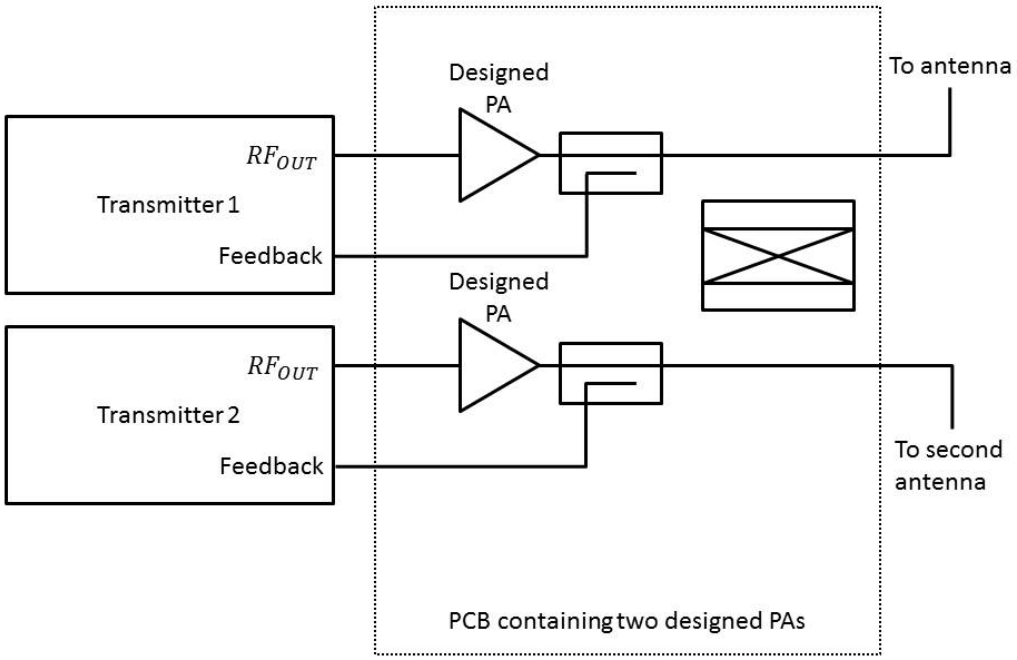

Figure 36: Designed PAs added in bypass mode.

In bypass mode, the combiner is bypassed, and both signals are fed to the separate antennas. Each antenna is fed with a single carrier with a capability of delivering the maximum power. Otherwise the bypass mode is similar to the combined mode.

7 Conclusions

Use of simulation tools were found to be very beneficial in a PA design. The simulations matched the real world scenario so well, that only minor changes were needed to achieve same results in measurements of the actual transistor as in simulations. The correlation between the simulated and the measured results is so high, that the manual tuning with a real transistor can be left minimum, when the frequency variants of the PA are designed.

The selected transistor was capable of delivering enough power, keeping the linearity requirement at the same time, when connected to the Cartesian loop. Further testing without the first prototype of the design would be useless, as the mechanics, used power supplies, connectors, isolators, combiners and other related devices play a role in overall performance of the LDMOS device.

BLF6G10-45 proved to be more suitable to serve as power transistor for the TETRA base station, even though a wider bandwidth could be achieved with CLF1G0060-30. There are several reasons that led to this decision. As the GaN transistors use higher drain voltages, implementing GaN transistor design to the existing all LDMOS system would require new power supply designs. Another reason to use LDMOS device, is the better availability of the transistors. Second sourcing and component delivery times are important features in the transmitter design. The most important factor favoring the LDMOS device, was the cost of the transistor.

However in future, development in manufacturing technology can lead to the situation, where the LDMOS and GaN transistors are about the same price, thus making GaN transistors a more reasonable choice. Even then, the more complex biasing circuitry required by the GaN transistors can cause the use of LDMOS transistors to continue.

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