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Realization of a capacitance-voltage measurement system for semiconductor characterization

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ABSTRACT OF
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Capacitance-voltage (CV) measurements are used widely as an effective method for Metal-Insulator-Silicon structures (MIS) characterization. They are electrical measurements able to provide several informations about semiconductor properties. Physical parameters including average doping density, fixed and mobile oxide charges, doping profile and interface trap density can be determined from a single measurement.
In this work, a complete capacitance-voltage (CV) measurement system has been developed and implemented. After initial testing it was employed as a valuable instrument for material research and semiconductors characterization.
Two different softwares were implemented for data acquisition and following analysis.A study of the precision and the sensitivity properties of the system is also presented.
Examples from the real measurements are discussed along with the main issues about the results interpretation and practical procedures. In particular, some results concern the comparison of silicon oxide and atomic layer deposited (ALD) aluminum oxide devices measurements. Finally, conclusions about correct sample preparation and contact fabrication are presented.
The difficulties and the different attempts during the development of the system are also presented as a starting point for future improvements.

Keywords:	electrical measurements, semiconductor, MOS, capacitance, ALD, oxide charge, interface trap density, profiling
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Preface

This thesis was realized at the Electron Physics Group (EPG) at Aalto University, Department of Micro and Nanosciences. The work was carried out within the PASSI project, funded by TEKES and several industrial partners and coordinated by EPG.
I would like to thank my supervisor Docent Hele Savin for giving me the opportunity to work in her group and for her guidance and understanding throughout the whole process. In addition, I'm really grateful to my instructor Antti Haarahiltunen for the precious support and patient help provided since the first impact with this topic.
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I need also to thank my wonderful family for always supporting me from far away, especially in the difficult moments.
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Symbols and Acronyms

CV	Current-voltage
LF	Low frequency
HF	High frequency
PV	Photovoltaic
MOS	Metal-Oxide-Semiconductor
MIS	Metal-Insulator-Semiconductor
C_s	Depletion layer capacitance
C_{ox}	Oxide layer capacitance
C_{FBS}	MOS flatband capacitance
q	Electric charge
k	Boltzmann constant
T	temperature
ϵ_s	dielectric permittivity constant
λ_i	Intrinsic silicon Debye length
ω	Frequency
u_b	Bulk potential
u_s	Surface potential
v_s	Normalized surface potential
ψ_s	Surface band bending
E_F	Fermi level
E_i	Intrinsic Fermi level
N_A,N_D	Doping impurities concentration
C_{it}	Interface traps capacitance
D_{it}	Interface traps density
R_s	Series resistance

Chapter 1

Introduction

Capacitance-voltage (CV) testing is a technique widely used to characterize semiconductor materials and devices and for the extraction of their physical parameters. The basic principle is to apply a varying voltage to a metal-insulator-semiconductor (MIS) or a Schottky junction and to measure the capacitance of the junction. The relationship between the measured capacitance and the applied voltage is then used to derive many relevant informations about physical properties of the device-under-test (DUT).

This method is particularly used in the industry and in the research field for MOSCAP and MOSFET devices. However a large variety of semiconducting devices can be characterized by CV measurements including Bipolar Junction Transistors, Junction Field Effect Transistors [1], III-V compound devices [2], photovoltaic devices [3], MEMS devices [4], organic field effect transistors displays [5], photodiodes [6], carbon nanotubes [7] and silicon nanowires [8].

A CV measurement system has many important qualities that makes it a valuable support and a necessary tool in many activities related to the IC industry and nowadays increasingly also in the photovoltaic (PV) field. This type of electrical measurement is an effective way to gather informations about materials

and devices. Furthermore, they are easy and fast to perfom and are flexible enough to be used for different kinds of investigation. As an additional advantage, a CV measurement system is considerably cheap compared to other material characterization equipment.
The general nature and the high flexibility degree of CV testing is the reason why it is so widely employed in a range of different disciplines and applications. Researchers and semiconductor manufactures use this technique to evaluate new materials, processes, devices and circuits. In industrial applications, reliability and yield engineers employ CV testing to analyze the results of different processes in the production chain, qualify material suppliers and study failure mechanisms. Using an appropriate hardware instrumentation, correct methodologies and reliable software a CV measurement system allows the extraction of a multitude of physical parameters.
There are however some disadvantages like the fact that these kind of measurements are particularly inaccurate for characterizing any device that has leakage, even for very small amounts. [9]
The measurements can be used to gather informations about average doping concentration, doping profiles and carrier lifetimes. In device analysis CV results can reveal oxide thickness [10], oxide charges, mobile ions from contamination effects and interface trap density. All these tests are commonly performed after each critical step of the fabrication process like gate dielectric and polysilicon deposition and metallization. The results provide an insight on how different processing parameters and chemicals affect the device. CV testing is also employed on finished devices to determine other quantities like the threshold voltage [11] or to model the performance of the final product.
Although CV measurement theory was developed in the late '60s, this topic has been continuously investigated and further

extended in the last fifty years. The challenge remains always to get the most accurate results with increasing resolution. Combination of different measurement procedures have been proposed and also the possibility to perform measurements at very low temperatures. The amount of computational power available nowadays allowed researchers and engineers to develop more complex and accurate software for results analysis. The introduction of new semiconductor structures and materials and the constant scaling towards always thinner dielectrics required the development of new models and analysis tools. For example, many quantum effects like tunneling are normally included in the analysis of the interface properties by CV measurements. One reason for the renewed interest in CV measurements is in the increasing importance that fields like silicon solar cells and MEMS devices have gained. As the silicon photovoltaic industry move towards cleaner processes and new fabrication technologies, CV testing procedures and experiences are borrowed from the IC field both in the industry and in research labs.

In this thesis, the work conducted at Aalto Univeristy's Electron Physics Group for the realization of a complete CV measurement system is presented and discussed. Because of all the reasons mentioned above, this system will provide a valuable help in many different studies about semiconductor material properties and processes. In particular the system was thought as a necessary instrument for the studies related to the interface quality of ALD aluminum oxide for silicon surface passivation. In Chapter 1 the basic theory of semiconductor devices underlying CV measurements is presented. Chapter 2 describes the different parts of the measurement system. The precision and sensitivity are briefly evaluated and some conclusions are presented. Chapter 3 includes some applications of the developed system within the PASSI project, lead by the Electron Physics Group. Although the details of the results are not presented, this chapter provides

some examples of the usefulness of CV measurements in material research.
Finally,the work and results are reviewed and suggestions for further improvements are proposed.

Chapter 2

Theoretical background

2.1 Capacitance-voltage (CV) curves

Two capacitances can be taken into account in a MOS device. Static capacitance can be defined as $C_{stat} = \frac{Q_T}{V_G}$, where Q_T is the total charge density on a "plate" of the capacitor and V_G is the voltage bias applied to it.
More important is the differential capacitance defined as $C = \frac{dQ_T}{dV_G}$ that measures the rate of change of the charge with voltage. The term "capacitance", in the following part of this thesis, will refer to small-signal MOS differential capacitance.
Most of the formulas and theoretical derivations shown in this chapter are presented in [14]. The total capacitance per unit area of a MIS structure in the ideal case (no interface traps, oxide charge or work function difference) is equal to the series resistance of the oxide capacitance and silicon capacitance:

$$\frac{1}{C} = \frac{1}{C_s(\psi_s)} + \frac{1}{C_{ox}} \tag{2.1}$$

Capacitance as a function of gate bias can be measured in steady state applying a small alternating component of voltage (typically AC voltage sinusoidal wave). The measurement has to be performed in the small-signal range, meaning that the amplitude of the applied AC voltage is small enough in order to

have a linear response of AC current to AC voltage.
Non-ideal effects like interface traps and interfacial and oxide charges influence the small-signal range because they affect the velocity of change of the admittance of MOS capacitor with gate bias.

2.1.1 Theoretical low frequency CV curves

The low frequency differential capacitance per unit area of a MOS structure as a function of surface potential can be obtained when minority carriers are able to follow the AC gate voltage and bias voltage ramp for every value of voltage bias.
To derive an analytical formula for LF CV characteristic, we assume that the device is at thermal equilibrium and dopant impurity concentration is uniform in silicon. Poisson's equation can then be solved to obtain the one-dimensional space potential and electric field. The surface charge per unit area at the interface can the be computed from Gauss's law. The electric field is:

$$F_s = Sgn(u_b - u_s)\frac{kT}{q\lambda_i}F(u_s, u_b) \tag{2.2}$$

where

$$F(u_s, u_b) = (2[(u_b - u_s)\sinh u_b - (\cos u_b - \cosh u_s)])^{1/2} \tag{2.3}$$

is the *dimensionless* electric field and λ_i is the silicon intrinsic Debye's length. u_b and u_s are respectively the bulk and surface potential defined as:

$$u_b = \frac{E_F - E_i}{q} \tag{2.4}$$

$$u_s = \frac{E_F - E_i(surface)}{q} \tag{2.5}$$

From Gauss's law the surface charge density is computed as:

$$Q_s = \frac{kT}{q}\frac{\epsilon_s}{\lambda_i} Sgn(u_b - u_s)F(u_s, u_b) \tag{2.6}$$

The definition of the surface differential capacitance is:

$$C_s = -\frac{q}{kT}\frac{\delta Q_s}{\delta u_s} \tag{2.7}$$

Taking the derivative of Eq.[2.6] with respect to u_s and substituting in Eq.[2.7] gives the final formula for C_s at low frequencies:

$$C_s = -Sgn(u_b - u_s)\frac{\epsilon_s}{\lambda_i}\frac{\sinh u_s - \sinh u_b}{F(u_s, u_b)} \tag{2.8}$$

Fig. 2.1 shows an example of theoretical low frequency CV curve. If we think to make a sweep of the gate voltage, the CV curve can be divided into different regions.

In the case of a p-type wafer, for negative gate bias the first region can be defined as *accumulation* region. For very large negative gate bias the hole charge density at the silicon surface contribute to a large differential capacitance C_s so the total differential capacitance of the MOS structure is approximately equal to C_{ox}.
When the gate bias is made less negative the surface hole density decreases making C_s smaller. The point at which the gate bias eventually is equal to zero is called the *flatband* point. For small positive values of gate voltage, holes are repelled from the silicon surface and a depletion layer of ionized dopants is formed. This range of bias is called the *depletion region* . The depletion layer widens when the bias becomes more positive making C_s smaller. Thus, from Eq. [2.1] the total capacitance of the MIS structure C becomes smaller.
As the gate bias increases the surface hole density continues to decrease while the electron density increases. The point at which

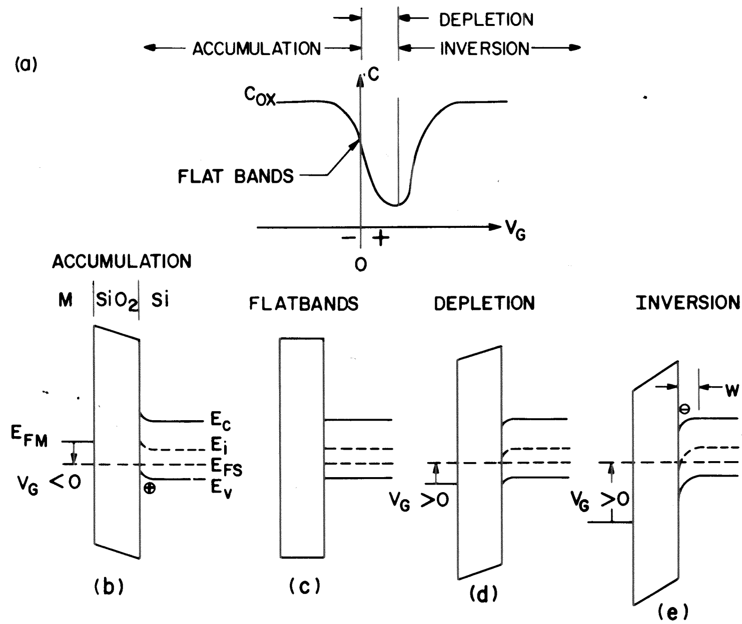

Figure 2.1: Low frequency total capacitance as a function of gate bias and corresponding energy-band diagrams shown in accumulation, depletion, inversion and flatbands. Energy values E_C and E_V are the conduction and valence band edges respectively; E_i is the intrinsic Fermi level; E_{FS} is the Fermi level in the silicon; E_{FM} is the Fermi level in the metal and w is the depletion layer width.

the densities have the same value is called the *onset of inversion* . When the electron surface density exceeds the holes one an *inversion layer* of electrons is formed. For more positive value of gate bias, the differential capacitance C_s continues to increase until it becomes comparable and then exceeds C_{ox}. The total MIS capacitance C from 2.1 then approaches C_{ox} asymptotically.

2.1.2 High frequency CV curves

In this section a quantitative expession for the HF capacitance as a function of surface potential will be presented. At high frequencies, minority carriers do not follow the AC gate voltage but they do follow changes in gate bias. The major difference

between low and high frequency CV curve can be observed in the weak and strong inversion regions, when the majority and minority carriers concentrations are comparable. The assumption is made that the total number of minority carriers is fixed by the gate bias in equilibrium and does not change in response to the AC voltage. In addition, spatial rearrangement of the inversion layer is taken into account:the inversion layer widens and narrows in response to the AC gate voltage.
The HF capacitance can be computed following a reasoning similar to the one used for the low frequency case:

$$C_s = 2C_{FBS}\{1 - e^{-v_{so}} + (\frac{n_i}{N_A})^2 + [(e^{v_{so}-1}\frac{\Delta}{1+\Delta} + 1]\}F^{-1}(v_{so}, u_B) \tag{2.9}$$

where

$$\Delta = \frac{F(v_{so}, u_B)}{e^{v_{so}}}\{\int_0^{v_{so}} \frac{e^{v_s} - e^{-v_s} - 2v_s}{F^3(v_s, u_B)}dv - 1\} \tag{2.10}$$

Although an accurate result is obtained using Eq. [2.10], the approximation from Lindner [15] can be performed taking into account minority carrier redistribution with a deviation at most of 1.5 % from the true capacitance value. In this procedure, the capacitance from Eq. [2.10] becomes gate bias independent beyond a precise value of band banding v_m called the *match point* . The value of capacitance at the match point minimizes the the maximum approximation error.
The formulas used to compute the approximated capacitance value for $p-$type and $n-$type respectively:

$$C_s = 2^{-1/2}C_{FBS}[1 - e^{v_{so}}][(v_{so} - 1) + e^{-v_{so}}]^{-1/2} \tag{2.11}$$

$$C_s = 2^{-1/2}C_{FBS}[e^{v_{so}} - 1][-(v_{so} + 1) + e^{v_{so}})]^{-1/2} \tag{2.12}$$

And adequate approximation for the band bending match point is:

$$v_m = 2.10u_b + 1.33 \tag{2.13}$$

High-frequency CV curves are basic to MOS structures measurements. As explained later, they're necessary for the extraction of interface trap level density using the high-low frequency capacitance method and for the determination of several physical parameters.
However the high-frequency CV curve obtained experimentally is seldom a good approximation to the true CV curve of the device through the whole biasing range. When the flatband region is approached, the majority carrier density decrease sensibly, yielding to more rapid capture and shorter interface trap constants. At the frequencies employed for the measurements, interface traps follow the ac gate voltage over part of the gate bias range. This effect limits the bandgap energy range over which the interface trap level density can be extracted using any method involving a high-frequency CV curve. The departure of the usual 1 MHz CV curve from the ideal high-frequency curve is caused by a stronger capacitive response of interface traps as flatbands region is approached and leads to an estimation of an apparent interface trap level density that is too small. That means that when flatbands region is reached, the measured 1 MHz capacitance rises towards the oxide capacitance value C_{ox} more rapidly than how the true high-frequency capacitance does. This rapid change of capacitance with gate bias affects the slope towards diminishing the stretchout thus yielding to a misleading reduction of the interface trap level density for every method that employs a high-frequency CV measurements. For the regions from flatbands to strong accumulation it has been shown that deviation at 1 MHz is no more than 2% [14].

2.2 Physical parameters from HF CV measurements

A CV curve measurement of a MOS capacitor is a convenient method for the extraction of many material properties. It can provide informations about conductivity type (n-type or p-type), dielectric and silicon properties and also interface quality.
Conductivity type can be reliably determined looking at the shape of HF CV curve. This curve is strongly asymmetric because of the different MOS capacitance values in accumulation and inversion. In a p-type wafer the curve goes from a higher value to a lower one for increasing gate voltage and fixed bulk potential. In a n-type wafer exactly the opposite happens and the curve goes from lower to higher values for the same biasing convention.
To consider reliable the measurements results, it has to be ensured that the sample reached the saturation value for the capacitance in the accumulation. It may happen that the CV curve saturates at a high capacitance because of the large density of interface levels or that oxide breaks down before reaching saturation because of the shift due to large fixed oxide trap density. Accumulation has been achieved only when the measured saturation capacitance equals the theoretical oxide layer capacitance. This value can be computed if the oxide thickness is measured independently i.e. by optical methods (ellipsometry).

2.2.1 Dielectric thickness, fixed and mobile charges

Dielectric thickness can be determined from a single measurement from a HF CV curve in accumulation. In this case the equivalent circuit of the MOS capacitor includes only the oxide capacitance and the series resistance of the device. The thick-

ness of the dielectric film is then:

$$t_{ox} = \frac{\epsilon_s A}{C_{HFmax}} \tag{2.14}$$

Additional informations can be obtained from a HF CV curve about the density of oxide charge.
Oxide charge is different from interface charge because it's independent from gate bias.
There are three types of oxide charge Q_0 important to take into account from the technology point of view. The first type is the oxide fixed charge Q_f. It's located in proximity of the Si-SiO_2 interface and in electrical measurement can be considered as a charge sheet.
The second type is the oxide trapped charge Q_{ot} that can be located at the metal-dielectric or silicon-dielectric interface. It is commonly produced by the injection of hot electrons or holes due to avalanche plasma, photoemission or exposure to ionizing radiation. Ion implantation can also introduce trapped oxide charges and in that case they can be distributed through the whole dielectric film.
The third type of oxide charge is the mobile ionic charge Q_m that is caused usually by the presence of ionized alkali metal atoms like sodium or potassium. This charge can be located at both interfaces in the MIS structure and can drift because the ions are mobile in SiO2 even at low temperatures.
The first two immobile type of oxide charge can be distinguished from the mobile ionic charge using a bias-temperature aging method and in many cases even at room temperature as it will be discussed later.
Fixed and trapped oxide charge density is related to the voltage shift of a CV curve with respect to the theoretical result. Under the assumption that the charge is distributed as a charge sheet at the Si-SiO_2 interface (most common case especially for thermally grown silicon oxide) the surface density can be determined

as:

$$Q_o = C_{ox}(W_{ms} - V_{FB}) \tag{2.15}$$

where W_{ms} is the *work function difference* between the metal and oxide and V_{FB} is the flatband voltage.

For both p-type and n-type silicon, a positive oxide charge density will shift the CV curve towards more negative values of gate bias. The opposite happens for negative oxide charge densities, although the positive case is the most common. Thus from the direction of the shift the polarity of the oxide charge can be determined, while the magnitude of the voltage shift can be used in Eq [2.15] to compute Q_o.

2.2.2 Doping concentration and profile

The easiest way to obtain the silicon doping density in a MIS structure is to use the maximum-minimum capacitance method: it requires one measurement of the maximum high frequency capacitance at a gate bias in strong accumulation and the minimum high frequency capacitance in inversion [19]. This procedure is unaffected by interface trap effects because the capacitance in accumulation is exactly C_{ox} while in inversion interface traps do not contribute to the total capacitance. The best results are obtained in the case of a uniform doping density.
The basic idea is to relate the measured capacitance to the depletion layer width because the width of the depletion layer is maximum when the device is in strong inversion:

$$w_{max} = \epsilon_s(\frac{1}{C_{HF}(min)} - \frac{1}{C_{ox}}) \tag{2.16}$$

Under the assumption of a uniform doping density and neglecting the width of the inversion layer, the doping concentration

N_A (or N_D for n-type wafers) can be computed solving:

$$\frac{N_A}{\ln \frac{N_A}{N_i} + \frac{1}{2}\ln[2\ln \frac{N_A}{N_i} - 1]} = \frac{4kT{\epsilon_{ox}}^2}{q^2\epsilon_s x_o^2}\left(\frac{C_{ox}}{C_{HF}(min)} - 1\right)^{-2} \tag{2.17}$$

where ϵ_{ox} is the dielectric permittivity in the oxide, $n_i$is the intrinsic carrier concentration and x_o is the dielectric layer thickness. Eq. [2.17] is a transcendental equation in N_A and can be solved by iteration. The ionized doping concentration value obtained with the minimum-maximum capacitance method is an *average* in the case of a nonuniform doping profile, so it is an approximation of the true doping density. Even for uniform doping densities Eq. [2.17] will be accurate within 3%.
Differential capacitance measurements can be used to analyze the doping profile $N(w)$ as a function of the distance w from the silicon interface. An accurate description can be obtained for capacitance values in the depletion region, where the free carrier concentration depends strongly on impurity concentration. The ionized impurity profile is related to the slope of the $(1/C_m^2)$ versus gate bias V_G curve, where C_m indicates the capacitance at a given gate bias V_G in depletion.
Neglecting the influence of interface trap, an expression for the ionized impurity profile can be derived using the approach from Van Gelder and Nicollian [21]:

$$N(w) = -2\left[q\epsilon_s \frac{d}{dV_G}\left(\frac{1}{C_m^2}\right)\right]^{-1} \tag{2.18}$$

The depletion layer edge w corresponding to a given capacitance value can then be computed to obtain finally the doping impurity profile:

$$w = \epsilon_s\left(\frac{1}{C_m} - \frac{1}{C_{ox}}\right) \tag{2.19}$$

Eq. [2.18] can be modified to take into account the voltage stretchout due to the presence of interface traps [14]. The fol-

lowing expression leads to a more accurate value for N(w):

$$N(w) = -2\left(\frac{1 - C_{LF}/C_{ox}}{1 - C_{HF}/C_{ox}}\right)\left[q\epsilon_s \frac{d}{dV_G}\left(\frac{1}{C_m^2}\right)\right]^{-1} \tag{2.20}$$

Thus N(w) can be obtained experimentally from high and low frequency CV curves using Eq. [2.20]. The doping concentration still depends on the slope of the high frequency CV curve but now in addition also the measured values for C_{LF} and C_{HF} are needed. The result will be accurate as long as it is possible to obtain reliable measurements for which the contribution of the interface traps to the voltage stretchout correspond to the low frequency interface trap capacitance.

2.2.3 Interface state density

A method was developed by Terman [22] to determine the interface trap capacitance using HF CV measurements. According to this procedure, capacitance is measured as a function of gate bias at a frequency high enough so that interface traps do not respond. Although interface traps do not follow the AC gate voltage they do follow very slow changes in gate bias as the MIS device is swept from accumulation to inversion. This behavior can be observed in a *stretch* of the CV curve along the gate voltage axis, although the capacitance values are not affected.
At high frequencies the total capacitance C_{HF} is given by the series connection of the oxide capacitance and the MIS capacitance:

$$C_{HF} = \frac{C_S C_{ox}}{C_S + C_{ox}} \tag{2.21}$$

being the interface trap capacitance $C_{it}(\omega) = 0$ because ω is too large for any AC response.
The total capacitance curve shape depends on the different band bending ψ_s versus gate bias relationship. The idea of the Terman method is to evaluate the interface trap density from a comparison of the theoretical band bending from a MIS device without interface traps and the band bending corresponding to the measured high frequency CV curve. Since the value of band bending ψ_s corresponding to a given high-frequency total capacitance value C_{HF} is known for the ideal case, then the gate bias voltage V_G corresponding to the same capacitance value can be measured in the real MOS device. In this way a ψ_s versus V_G can be constructed. In high-frequency CV measurements, this relation contains all the informations needed for interface trap density computation. More details are given about the software algorithm in the Matlab software section.
Then the interface trap capacitance C_{it} is determined as a func-

tion of ψ_s as:

$$C_{it}(\psi_s) = C_{ox}\left[\left(\frac{d\psi_s}{dV_G}\right)^{-1} - 1\right] - C_s(\psi_s) \tag{2.22}$$

The interface trap density can then be computed as:

$$D_{it}(\phi_s) = \frac{C_{it}(\phi_s)}{q} \tag{2.23}$$

The method involving low frequency CV measurements to determine the interface trap density was first developed and used by Berglund [16]. Again, a CV curve has to be measured to a specific frequency low enough for minority carrier and interface traps to respond immediately. In this measurements, the additional capacitance C_{it} will contribute to the total capacitance value.
Fig. 2.2 shows the equivalent circuit model of a MIS structure measured at low frequencies in depletion and strong accumulation.

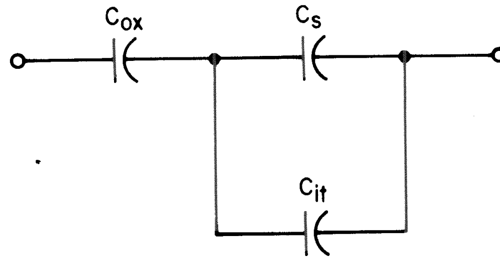

Figure 2.2: Low frequency equivalent circuit of the MOS capacitor with a distribution of interface trap levels over the bandgap. The silicon capacitance per unit area is C_s. The interface trap capacitance per unit area is C_{it} and is given by Eq. 2.23 solving for C_{it}.

From the equivalent circuit it can be seen that this capacitance

can be extracted from the measured values when C_s and C_{ox} values are know using the relation:

$$C_{it} = \left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - C_s \qquad (2.24)$$

where C_{ox} can be measured in strong accumulation and C_{LF} is the measured low frequency capacitance at a gate bias V_g. We can see that $C_s(V_g)$ is needed to obtain C_{it} from Eq. [2.24]. The value of $C_s(V_g)$ can be computed in two steps. First C_s is calculated as a function of the band bending ψ_s if the doping profile is uniform from Eq.[2.8]. When the doping profile is nonuniform the band bending must be determined independently and then used to compute $C_s(\psi_s)$. Then, $C_s(\psi_s)$ can be related to $C_s(V_g)$ if ψ_s versus V_g is known.

Two methods can be used to experimentally determine the relation of ψ_s versus V_g. The first method is the Q-V method, in which the silicon surface band bending is obtained as a function of gate bias directly from a measurement of the charge on the MOS capacitor as a function of gate bias. The second method is to use a high-frequency CV curve following the procedure described for the Terman method application.

The high and low-frequency methods described above to compute the interface trap density have both their advantages and drawbacks regarding the conditions in which they can be performed, the errors introduced in the measurements and the approximations that have to be done in the analysis of the results. One of the most limiting factors is the need for a theoretical computation of C_s and the corresponding band bending that always introduce a certain degree of uncertainty about the approximation made in the numerical computation.

A method to avoid the theoretical computation of C_s has been developed by Castagne' and Vapaille in [17]. They were the first to combine high and low frequency CV curves to obtain a *mea-*

sured C_s.
The value of C_s can be determined using Eq.[2.21] and after substitution in Eq. [2.24] we have:

$$C_{it} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1} \quad (2.25)$$

Eq.[2.25] yields C_{it} as a function of gate bias but the interface trap density has to be obtained as a function of position in the bandgap. In addition, Eq.[2.25] is not valid for gate biases in or near inversion because minority carriers do not follow the high frequency gate voltage.

2.2.4 Errors in extracting interface trap density

In this section, some errors in the capacitance methods previously discussed will be briefly presented. The main source of error common to both low and high-frequency capacitance methods is the need for the theoretical $C_s(\psi_s)$. To compute $C_s(\psi_s)$ the doping profile must be known and every inaccuracy will introduce some degree of uncertainty on the final result. Most of the times the doping profile is assumed to be uniform, but in reality this is seldom the case. Redistribution of the impurities occur for example because of oxidation or implantation. Baccarani et. al. in [18] estimated the error in D_{it} introduced when the impurity redistribution is ignored. In addition, it was found theat the deviation of CV curves from the ideal situation increases with increasing initial uniform doping concentration. As doping density increases, the non-uniformly doped region becomes a larger fraction of the depletion layer width and the uniform doping approximation won't hold anymore.
Spatial non-uniformities of the charge distribution in the oxide along the interfacial plane also cause errors in the calculated $C_s(\psi_s)$ in the same way as interface traps do.

Another error is introduced in the analysis part in the derivation step of the ψ_s versus V_G curve when the high-frequency capacitance method is used. This error can be made acceptable when more precise measurements are performed.
The failure in measuring a true high frequency CV curve is a problem as well, especially near the flatbands or in accumulation, as discussed earlier. This problem is particularly relevant when the combined high and low frequency capacitance method is used to measure directly C_{it}. This limitation emerges in the specific in the weak-to-strong inversion regions.
Besides experimental and intrinsic non-idealities, roundoff errors affect the results during computation. Since all the capacitance methods discussed above all depend on subtraction of C_s from the measured values (C_s + C_{it}) (regardless of whether C_s is computed or measured), roundoff errors are introduced when the value of C_s is considerably large compared to C_{it}.

Chapter 3

Measurement setup

Besides the actual measurements, the main part of this work consisted in the implementation of a complete system for CV measurements and characterization. The solution adopted includes an impedance analyzer to carry out the measurement and a software part for data acquisition and analysis.

3.1 Impedance analyzer and sample preparation

The impedance analyzer model used for the measurements is a HP 4192A connected to a probe station.

Figure 3.1: HP 4192A impedance analyzer

Samples are placed in the station on top of a copper support. A small sheet of thick transparent plastic is inserted between the copper plate and the probe station support in order to reduce the parasitic losses towards the support. A measurement probe is placed on the top contact while the bias is applied to the copper support and thus to the silicon substrate of the sample. The probe station is enclosed in a metallic box that can be opened to insert the sample and then closed. This allows to obtain the measurements in a dark environment in order to avoid generation of carriers.
The results of the measurements consist directly of the real and imaginary part of the impedance seen between the probes. Measurement data are affected by the parasitic impedance of the wires, of the the copper contact and even by the metallic enclosure. The scheme of Fig. 3.2 shows the parasitic elements existing in the impedance analyzer measurement system between the unknown device and the measurement terminals. These undesired elements are present as resistive and reactive factors in series and conductive and susceptive factors in parallel with the test component. This non-idealities become actually part of the sample that instrument measures so their effects have to be taken into account and eliminated. Separate open and short-circuit measurements are needed to correct the data.

The HF curves are measured at the frequency of 1 MHz and the limit for correct machine operation is 13 MHz. Although many parameters can be changed to perform the measurements, all the settings were chosen in order to have optimal measurements' conditions or resolution in the results. The oscillation level is usually set to 0.05 V in order to have a 3 digit resolution and to guarantee a small-signal condition for the sample. [12]
During the measurement sessions some practical issues have

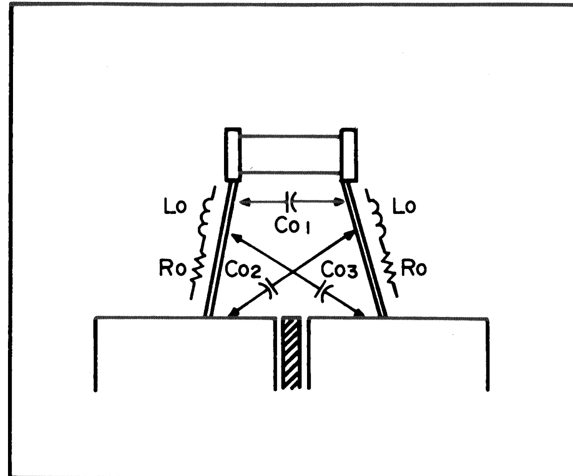

Figure 3.2: Parasitic elements incident to the DUT connections introduced by impedance analyzer test leads.

been noticed that help to obtain reliable results. Before sweeping the voltage, a bias has to be applied to the substrate in order for the MOS sample to be in the strong inversion or inversion region. Depending on the quality of the sample, it may happen that some waiting time is required before starting the voltage sweep. Some time is then needed for the generation of carriers in the device to reach an equilibrium state.
The voltage can then be swept in the direction going from the inversion region to the accumulation one on the CV curve. This allows to minimize the probability that the MOS sample goes into a deep-depletion region during measurements. The theoretical reason behind this practice is that in many cases, in the specific with silicon substrate that has a long minority carrier lifetime, the sweep rates used in the measurements are too fast for generation to follow but slow enough for recombination to follow. At room temperature the system is usually not in equilibrium when gate is swept in the direction of increasing inversion, but is in equilibrium in the opposite direction, namely from inversion to accumulation. [14]

The impedance analyzer has to be connected to a computer through a GPIB connector in order to be controlled by the Labview software.

3.2 LabView

A software has been developed using the G programming language of NI LabView. This simple software allows the user to control the impedance analyzer using a computer and was thought explicitly to automate and perform fast CV measurements. The user interface is basically a reproduction of the impedance analyzer front panel and allows the user to set most of the standard parameters available plus some additional features included in particular for CV measurements.
The computer has to be connected to the machine through a GPIB interface serial cable. The software then can send strings of BASIC commands to the impedance analyzer and acquire the data from the machine. The commands sent to the machine follow a built-in BASIC syntax described in detail in the HP 4192 user's manual [12]. The user has to provide the parameters for the commands in the proper fields of the graphic interface. The required input values are: the starting and final value of voltage bias and the step value for the sweep, the starting and final frequevalue and the resolution for the frequency sweep. These data are expressed respectively in volts (V) and Hertz (Hz) using a scientific notation. For CV measurements both starting and final frequency fields have to be set to the same value (1 MHz for the standard procedure) with a resolution value different from 0. When different values of frequency are provided the software performs a double loop to perform a sweeping of both voltage bias and operating frequency for conduction-voltage measurements.
A switch allows the user to perform the measurements in the series or parallel mode. When in parallel mode the results of the measurement are epressed in the form $G+iB$ while in series mode the impedance will be presented in the form $R+iX$. As it will be explained later in more detail, all the measurements have

to be performed in parallel mode except the single measurement for the setup short circuit resistance that has to be set in the series mode.
In addition to the usual impedance analyzer features, the Labview software includes specific additional settings. The user can set a double sweep in both directions from negative to positive voltage bias in order to check for possible hysteresis effects. It's also possible to set the delay time in the sweep of the voltage bias in order to be sure that the sample reaches the equilibrium state before the actual measurement in case of samples with high carrier generation lifetime.
After the acquisition, data are saved in a spreadsheet format with ".xls" extension for successive analysis.
The results are plotted after each measurement loop in a graphical form and are visualized in two charts at the bottom of the front panel. The chart on the right shows the CV curve while the one on the left shows the plot of the real part of the conductance vs. voltage bias for a given frequency. The capacitance values are computed from the imaginary part of the measured conductance using the formula:

$$C = \frac{B_i}{2\pi f} \tag{3.1}$$

where B_i is the i_{th} measurement point and f is the measurement frequency. Although this plot gives a first indication about the reliability of the results, it has to be considered that these values need to be corrected because parasitic elements and series resistance might affect the measured value.

Fig. 3.3 shows the screenshot of the Labview software.

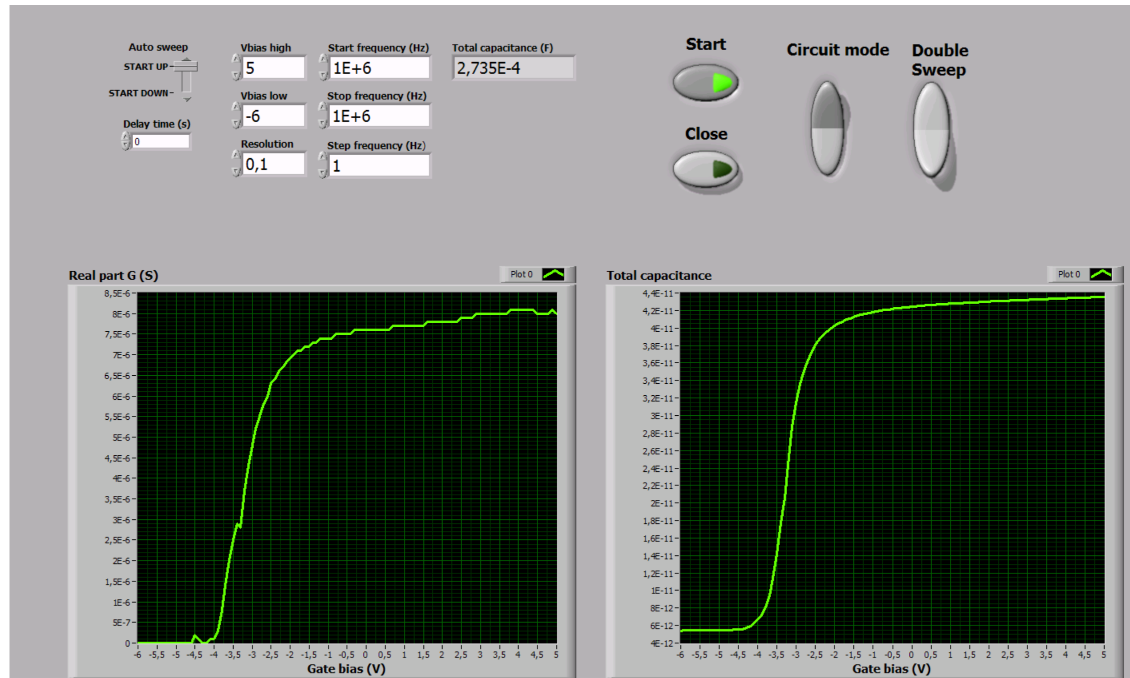

Figure 3.3: Screenshot of Labview front panel.

3.3 Matlab

The Matlab software allows the user to process the raw data acquired using the Labview interface. The software has been developed in a script version and in a modular version that includes a GUI. It requires a few user-provided parameters in order to get the correct results for different materials and devices. The input parameters are: the raw data spreadsheet with the measurement points, the contact area of the measured MOS capacitor, the dielectric constant of the insulating layer and the metal-oxide work function.
The contact area has to be known from the area on the mask, while the work-function of the metal-oxide system can be found in specific tables. The dielectric constant may be not know for a material under specific processing conditions and parameters. It can be anyway determined from the analysis of ellipsometry optical measurements or fitted with the Matlab code when the thickness of the sample has already been measured optically.
Even if the measurements were taken in different order the spreadsheet need to be formatted as illustrated in the following table:

Table 3.1: Spreadsheet data format

Real part	Imaginary part	Voltage bias	Frequency
Short-circuit R	Short-circuit X	0	1 MHz
Open-circuit G	Open-circuit B	0	1MHz
Series-resistance G	Series resistance B	(Accumulation bias)	1 MHz
G_1	B_1	Starting voltage	1 MHz
...	...	...	...
G_n	B_n	Final voltage	1MHz

where n is the number of steps (measurement points) defined as $\frac{V_2 - V_1}{resolution}$ with V_1 and V_2 being the initial and final value for the gate bias voltage sweep. As we can see from table 3.1, the first

three rows need to be the measurements performed for the correction of non idealities introduced by the measurement setup and for taking into account the sample series resistance.
The Matlab software performs the corrections according to the following formulas:

$$G_m = \frac{G(1 + GR_0) + R_0 B^2}{(1 - \omega L_0 B + GR_0)^2 + (\omega G L_0 + R_0 B)^2} + G_0 \tag{3.2}$$

$$jB_m = j\left(\frac{B(1 - \omega L_0 G^2) - \omega R_0 B^2}{(1 - \omega L_0 B + GR_0)^2 + (\omega G L_0 + R_0 B)^2} + \omega C_0\right) \tag{3.3}$$

where G_m + jB_m is the total admittance measured between the impedance analyzer probes and G + jB is the sample admittance. Fig the other parameters are the undesired parasitic elements The first three row of the spreadsheet file containing the

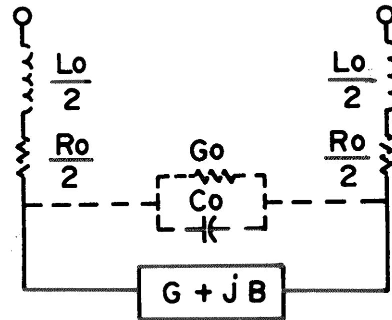

Figure 3.4: Equivalent circuit of the residual parameters introduced by the parasitic elements of the impedance analyzer measurement system. This model has been used to derive the system made of Eq.[3.2] and [3.3] to correct measurement data.

raw data are used to define the open circuit parasitic admittance G_0 + jB_0 and the short-circuit impedance R_0 + jX_0. The software uses the data to solve the system of the two equations 3.2 and 3.3 for every measurement point.

Series resistance can be the cause of serious errors in the extraction of interfacial properties and doping profiles from the measurements. It can also limit the sensitivity of the small-signal steady methods. Series resistance can arise from different sources and not always can be made negligible. Including the effect of the series resistance is particularly crucial in the case of leaky dielectrics due to very thin insulating layers or poor materials or technology. In this specific cases the series resistance value can be used to reconstruct the CV curve from the raw data as explained in [24] [25]. In most cases, the most general approach is to measure series resistance and then apply it as a correction to the measured admittance.
Fig. 3.5 shows the equivalent circuit model of a MIS structure measured at low frequencies in depletion (a) and strong accumulation (b). At a given frequency the greatest effect on the measured admittance occurs in strong accumulation. For this bias, the accumulation layer capacitance C_A is in parallel with Y_{it} the interface trap admittance. This model can be simplified because C_A is large and shunts Y_{it}. The correspondent equivalent circuit becomes the one in Fig. 3.5 (c). Because $C_A >> C_{ox}$ an additional semplification leads to the final model (d) used for the corrections.

To determine the series resistance R_s the MIS sample is measured when it's biased into strong accumulation.The value of R_s is computed with the following formula after the corrections for the setup have been applied to the raw data:

$$R_s = \frac{G_m}{G_m^2 + \omega^2 C_m^2} \tag{3.4}$$

The oxide layer capacitance is then determined starting from the equivalent circuit of the MOS structure in strong accumulation, substituting the series resistance R_s of Eq. [3.4] in the relation

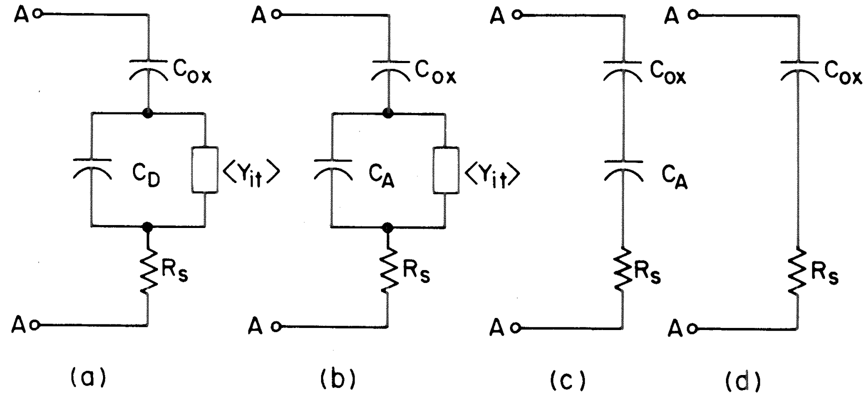

Figure 3.5: (a) Equivalent circuit of the MIS capacitor in depletion including series resistance R_s. (b) Equivalent circuit of the MIS capacitor in strong accumulation. (c) simplified version of (b); (d) simplified version of (b) that can used to extract values of C_{ox} and R_s

$C_m = C_{ox}/(1 + \omega^2 R_s C_{ox}^2)$ obtaining the formula:

$$C_{ox} = C_m \left[1 + \frac{G_m}{\omega C_m}^2 \right] \tag{3.5}$$

The oxide capacitance value is then used to get the oxide layer thickness, using the values for capacitor area and oxide dielectric permittivity inserted by the user in eq. 2.1.
Once the oxide layer thickness is known, the software is then able to determine the average doping concentration for the given sample using the high-low capacitance method described in section 2.2.3. Matlab solves the trascendental equation 2.17 by iteration with respect to N_A (or N_D for n-type wafers). Flat band capacitance and voltage are then computed to determine the net effective charge density Q_0 using Eq. 2.15. The doping profile as a function of the junction depth (here indicated by ω) $N(\omega)$ is computed using Eq. 2.18.
The software then performs the computation for the theoretical high and low frequency total capacitance of the MOS sample in order to be then compared with the measurement data. First

the surface band bending u_s is determined and then the HF and LF theoretical capacitances. After this step, the software fits the measured total capacitance with the theoretical one and plots together the three graphs on a capacitance vs. voltage chart.
A stand alone version of the software including a graphic user interface (GUI) has been developed in order to help the user to easily analyze the measurements. The GUI is shown in Fig. ??.
The GUI allows the user to select a spreadsheet file through a

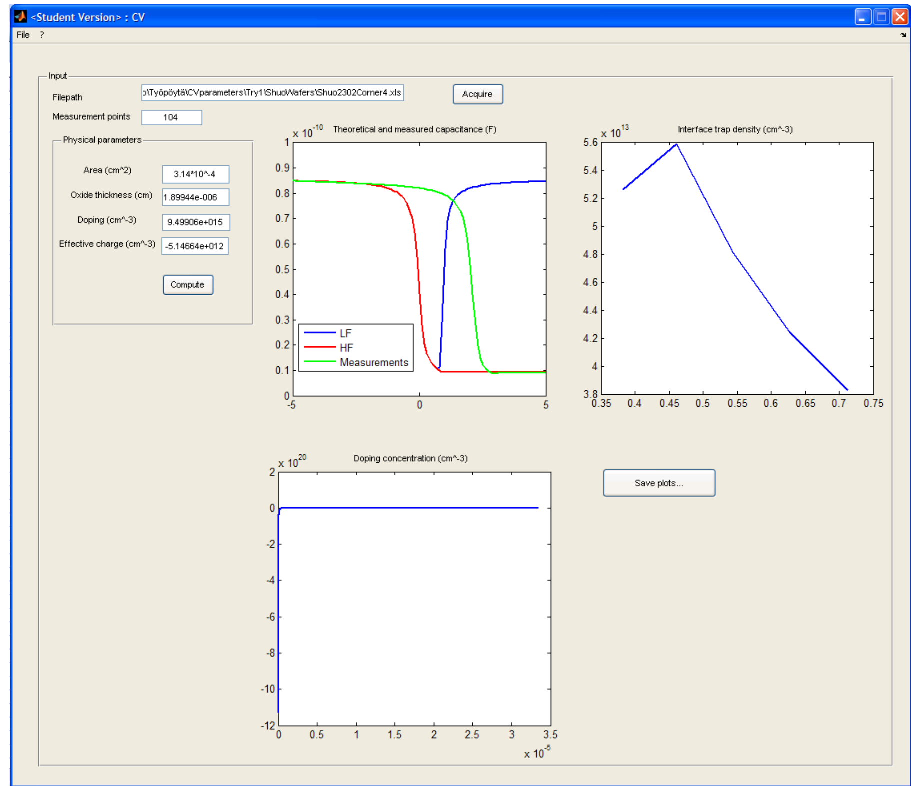

Figure 3.6: Screenshot of graphic user interface (GUI) of the Matlab software that has been developed.

dialog box and has three input fields for the contact area, the number of measurement points and the dielectric constant of the insulating material. On the left side of the window, three text boxes show the physical parameters computed by the software, namely the oxide thickness, the average doping concentration

and the net effective charge. Three plot boxes are used on the right to visualize the results for the theoretical and measured CV curves, the doping profile vs. depletion region width and the profile of the density of states vs. band bending. The results can then be saved in a spreadsheet and the plots in separate .jpg files.

3.4 Low frequency CV measurements

Within the work for this thesis, it was originally planned to implement a low frequency (LF) CV measurements setup along with the HF one. The combined use of HF and LF measurement data allows to have a better approximation and more precise values when extracting all the parameters as described in Sec. 2.2.3.
It was attempted to employ firstly the ramp rate method to perform quasistatic CV (QSCV) measurements [23]. While high frequency measurements are generally made using AC voltage, the low frequency ones are executed usually almost at DC. These measurements are made using two Source-Measure Units (SMU) connected to the gate and the substrate of the device and stepping a DC voltage while measuring the resulting current or charge. Basically the device under test is charged up to a specific DC voltage using a Source-Measure Unit (SMU) as a current source. Once the device is totally charged, a current of the opposite polarity is forced to discharge the device. One SMU measures the voltage as a function of time and the other one measures the discharge current. From the measured voltage (V), the current (I) and the time (t) , the capacitance (C) is derived as a function of voltage and time.
Unfortunately this method was not feasible using the present equipment version, namely the HP 4155 Semiconductor Parameter analyzer. The machine doesn't allow to measure exactly the current during the sample short discharging time. The alternative tjat was attempted was originally proposed by [20] exploit the basic capacitance relation:

$$C = \frac{I}{\left(\frac{dV}{dt}\right)} \tag{3.6}$$

The measurement were made using the Semiconductor Parameter Analyzer (SPA) and the same probe station used for the high frequency CV measurements. The SPA measures the values of current and voltage between the Source-Measuring Units (SMUs). Two SMUs were employed for the LF CV measurements: one connected to the metal gate and the other connected to the substrate. The SMU connected to the gate was used to supply a constant value of current to the sample, both in the negative and positive polarity. The second SMU supplied a constant voltage equal to 0 the substrate. The gate voltage was measured as a function of time. The results are a set of voltage values and the corresponding instant in time. From this two vectors of point, the derivative $\frac{dV}{dt}$ can be approximate numerically with discrete numerical differences. Using these results in Eq. 3.6, the total capacitance C can be determined.
This method is valid and flawless considered the theory. Anyways, after the first measurements and successive analysis, the practical difficulties suddenly became apparent.
One obvious complication is the presence of a derivation step in the process to compute the total capacitance. This step introduces intrinsically a high degree of imprecision in the result, due to the finite numerical approximation. One way to reduce this effect is to increase the resolution of the measurement points, namely increasing the number of sampling instants. Unsatisfactory results were obtained even when the number of sampling instants was the maximum allowed by the internal memory of the SPA.
In order to keep a slow rate of change in the gate voltage for the sample to be in equilibrium, a very low value of current has to be used. The optimal current value for sample used specifically in this thesis work was close to the lower limit the SPA could provide, 100 fF. Anyways the biggest issue is that with such low current values, the noise introduced during the mea-

surement strongly affects the results. The combination of these two effects made the accomplishment of useful LF CV measurements basically impossible. Fig. 3.7 shows how the data look like using Eq. [3.6] after the derivation step. A moving average algorithm was applied to the vector in order to reconstruct the data, but the values are still not satisfactory to be used in a comparison with the theoretical curve.

Although the results were not as expected, they weren't totally

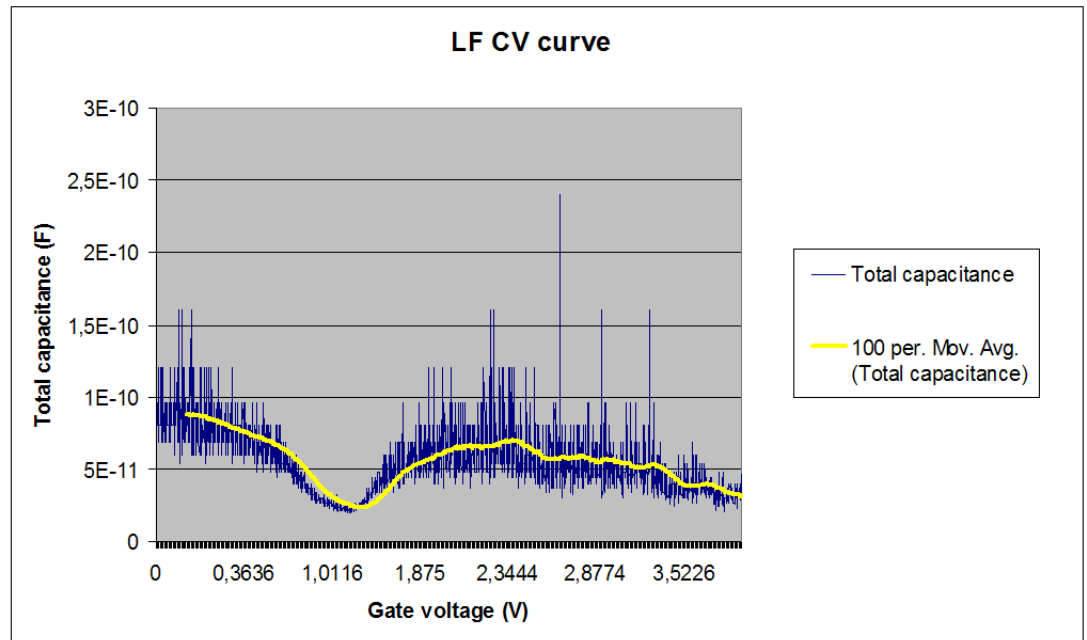

Figure 3.7: Low frequency CV measurement. The blue series is the total capacitance value using Eq. [3.6] . The yellow series are the data points obtained applying a moving average smoothing filter.

useless either. The LF CV curve shape is clearly visible even though it's really noisy. Due to higher current value used during the measurements, the sample was not able to reach effectively the same capacitance value in the strong inversion region as in accumulation. One way to improve this practice would be to find a way to carry out very low-current measurements in which the sample is shielded in order to reduce as much as possible

the presence of parasitic elements and noise from surroundings. Unfortunately this was not possible to be accomplished during the time given for this thesis work but it still remains as possible future extension for a complete high and low frequency CV measurement setup system.

3.5 Precision of measurement system

The precision of CV measurements was evaluated for the implemented measurement system. As defined in [26], the precision of a measurement system, also called reproducibility or repeatability, is the degree to which repeated measurements under unchanged conditions show the same results.
This system property was investigated performing a set of different measurements on the same sample and comparing the variations in the results. Between consecutive measurements the setup was completely disassembled, the wires and probes disconnected and the sample removed from the probe station support. This procedure was repeated ten times. The precision of the measurement system was evaluated studying the variations on the maximum and minimum capacitance of the measured CV curve. The sample was a MOS structure with a n-type CZ silicon substrate, a 27 nm thick silicon oxide layer and aluminum contacts. The area of the contacts was $3{,}5344\times10^{-4}cm^2$.
Fig. 3.8 shows the result of the precision test for the value of the maximum capacitance measured in accumulation. Fig.3.9 is a plot of the results of the same test for the minimum capacitance. The variance over the two set of data was computed leading two the two results $\sigma_{max} = 6.2541 \times 10^{-13}$ F and $\sigma_{min} = 5.0244 \times 10^{-14}$ F. As we can see from the computed variance values, for our data samples the results for the maximum capacitance measurements are ten times more far away from the average value than the minimum capacitance results. Anyway

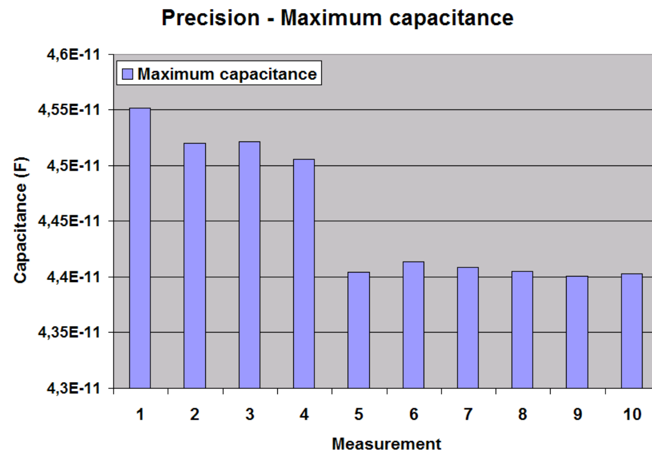

Figure 3.8: Plot of the results for the precision test for maximum capacitance after ten measurements.

the order of magnitude of the variance indicates that this difference is in in the order of 0.1 pF. As we shall see in the next section, these variations in the measurements can be considered too small and they don't affect the final results of the computations. The system can be then considered to have a satisfactory level of precision.

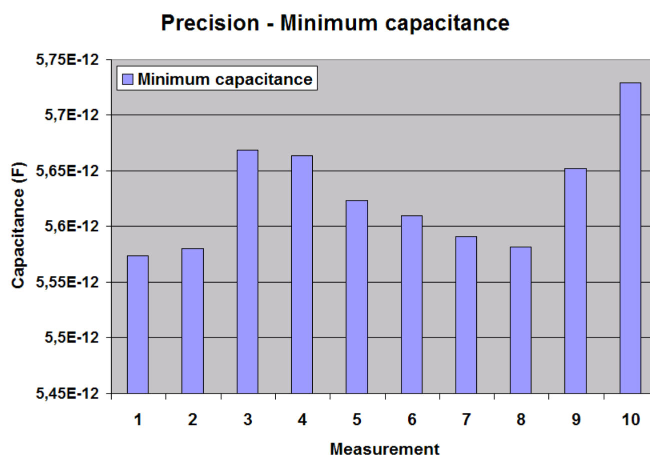

Figure 3.9: Plot of the results for the precision test for minimum capacitance in strong inversion for ten measurements.

3.6 Sensitivity analysis of the measurement system

In this section a brief sensitivity analysis of the measurement system is presented. The scope of this study is to provide to the end user a reasonable estimation of the error bounds in case of unexpected variations in some of the input parameters. Neglecting user generated human errors, sources of faulty results are for example undesired variations in the manufacturing process (i.e. contacts fabrication) or during the measurement session (i.e. impossibility to obtain a reliable CV curve from measurement).
From the discussion of the previous section, we assume that the precision of the measurement setup is high enough to neglect a detailed sensitivity analysis that includes a statistic perturbation of the whole set of input raw data. The remaining input data supplied by the user for analysis is the contact area of the MIS device that has been measured. It often happens that the area of the contacts after the deposition of the contact metal is substantially different from the nominal contact area used for

the lithography mask or during evaporation. Since most of the times the dimension of the contacts are not verified again after deposition, the user who performs the CV measurement in turn gives as an input to the software a different value from the actual one on the sample. When the are of the contact and thickness of the dielectric film are small this could lead to misleading results. In this part, the relationship between a perturbation in the contact area input value and some of the output values will be studied. Firstly it was attempted to provide a detailed analytical study starting from the algorithms used in the software by means of general error propagation theory models. The idea was to express every computation as a function of the input parameters that were to be varied and then perform a linear approximation of the output variations using partial derivatives for each function [27]. Due to the presence of transcendental equations and of several loop in the data fitting part, this approach was discarded and a numerical computation method was implemented.
The analysis is performed using a sample MOS structure. The full analysis of this sample including physical parameter extraction and verification is presented in the next chapter.
The basic idea of this brief analysis is to start from the correct results and corresponding input parameters, and see how the different computations, rounding and fitting operations affect the final result when the input values are changed.
Using the example presented in Chapter 4, we know that the contact area is $A_0 = 0.0601$ cm^2. The magnitude of the maximum relative error was defined as $\Delta A = 50$ % A_0, although in reality this is an exaggerate variation in the capacitance. A vector of points A_i being $0.5A_0 \leq A_i \leq A_0$ uniformly spaced in order to have $A_{i+1} = A_I + 0.05A_0$ was given as input to the Matlab software. The corresponding output for the doping density N_d, the net effective charge N_{eff} and the oxide thickness t_{ox}

were computed along with the respective relative error. If we define R_0 the correct result corresponding to the input A_0, the relative error was computed as $\epsilon = \frac{R_i - R_0}{R_0}$, where R_i is the output of the computation of the corresponding perturbed input A_i. The following table presents the numerical result of the analysis.

Table 3.2: Numerical results of sensitivity analysis for area input parameter variation. The row in bold characters is the correct unperturbed value.

Area (cm^2)	N_A (cm^{-3})	N_{eff} (cm^{-2})	t_{ox} cm
0,0331	1,68E+16	5,45E+12	1,49E-06
0,0361	1,4E+16	4,99E+12	1,62E-06
0,0391	1,18E+16	4,61E+12	1,76E-06
0,0421	1E+16	4,28E+12	1,89E-06
0,0451	8,67E+15	3,99E+12	2,03E-06
0,0481	7,55E+15	3,74E+12	2,16E-06
0,0511	6,63E+15	3,52E+12	2,3E-06
0,0541	5,86E+15	3,33E+12	2,43E-06
0,0571	5,22E+15	3,15E+12	2,57E-06
0,0601	**4,67E+15**	**3,00E+12**	**2,70E-06**
0,0631	4,21E+15	2,85E+12	2,84E-06
0,0661	3,80E+15	2,72E+12	2,97E-06
0,0691	3,46E+15	2,60E+12	3,11E-06
0,0721	3,15E+15	2,50E+12	3,24E-06
0,0751	2,89E+15	2,40E+12	3,38E-06
0,0781	2,65E+15	2,30E+12	3,51E-06
0,0811	2,45E+15	2,22E+12	3,65E-06
0,0841	2,26E+15	2,14E+12	3,78E-06
0,0871	2,10E+15	2,07E+12	3,92E-06

Fig. 3.10 is a plot of the relative error ϵ for each output variable vs. relative variation in the input. As expected, the relative error in the oxide thickness depends linearly on the relative error in the input area following from Eq.[2.14]. The error is instead non-linear for the doping density and the net effective charge. Anyway for small variation in the input area value within 10% the output error can be considered linearly affected. It's worth

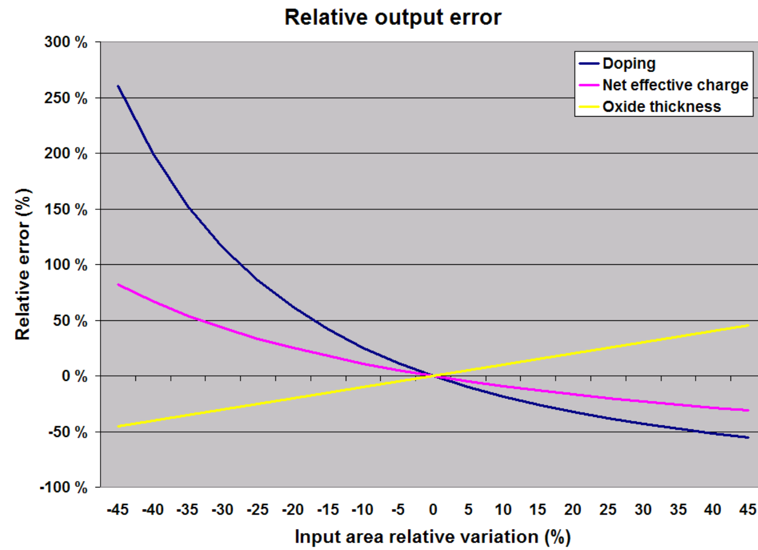

Figure 3.10: Plot of the relative output error ϵ vs. input area relative error. Both quantities are expressed as percentages. It can be seen that all the quantities behaves reasonably linearly for input variations within 10% range.

to notice that the relative error is actually increasing faster when the area is underestimated than in the opposite case.
As discussed earlier, sometimes is difficult to measure a true HF CV curve. The main problems arise i.e. when the sample is not in equilibrium in the inversion region and during the sweep enters the deep-depletion region. The measurement results are then usually lower than the expected ones. In other cases it's difficult to obtain a flat CV curve in accumulation and a small slope still exist in the graph.
A second sensitivity analysis was performed to exstimate the output variation for sources of errors coming from wrong measurements. The minimum and the maximum value of capacitance were varied and the effect of this perturbation was computed on the output parameters. A complete analysis should include a statistical study of the error introduced by the random perturbation of every measurement point. Since in this sensitivity analysis we chose to neglect the profiling features of

the software, just the two extreme values of capacitance can be used reliably without losing too much information.
In the first analysis, the maximum value of capacitance measured in accumulation, corresponding in theory to the oxide layer capacitance, was varied of 20 % relatively to the correct value. Table 3.3 shows the result of the numerical computation.

Table 3.3: Numerical results of sensitivity analysis for maximum capacitance variation. The row in bold characters is the correct unperturbed value.

Area (cm^2)	N_A (cm^{-3})	N_{eff} (cm^{-2})	t_{ox} cm
6,14E-09	5,15E+15	2,27E+12	3,38E-06
6,3E-09	5,09E+15	2,34E+12	3,3E-06
6,45E-09	5,03E+15	2,41E+12	3,22E-06
6,6E-09	4,97E+15	2,48E+12	3,14E-06
6,76E-09	4,92E+15	2,56E+12	3,07E-06
6,91E-09	4,87E+15	2,63E+12	3E-06
7,06E-09	4,82E+15	2,7E+12	2,94E-06
7,22E-09	4,78E+15	2,77E+12	2,88E-06
7,37E-09	4,74E+15	2,85E+12	2,82E-06
7,52E-09	4,7E+15	2,92E+12	2,76E-06
7,68E-09	**4,66E+15**	**2,99E+12**	**2,7E-06**
7,83E-09	4,63E+15	3,07E+12	2,65E-06
7,99E-09	4,59E+15	3,14E+12	2,6E-06
8,14E-09	4,56E+15	3,22E+12	2,55E-06
8,29E-09	4,53E+15	3,29E+12	2,5E-06
8,45E-09	4,5E+15	3,37E+12	2,46E-06
8,6E-09	4,48E+15	3,44E+12	2,41E-06
8,75E-09	4,45E+15	3,52E+12	2,37E-06
8,91E-09	4,42E+15	3,6E+12	2,33E-06
9,06E-09	4,4E+15	3,67E+12	2,29E-06
9,21E-09	4,38E+15	3,75E+12	2,25E-06

Fig. 3.11 is a plot of the relative error ϵ for each output variable vs. relative variation in the input. It can be seen that the computed net effective charge is the quantity most affected by variations in the nominal correct value of input oxide capacitance.

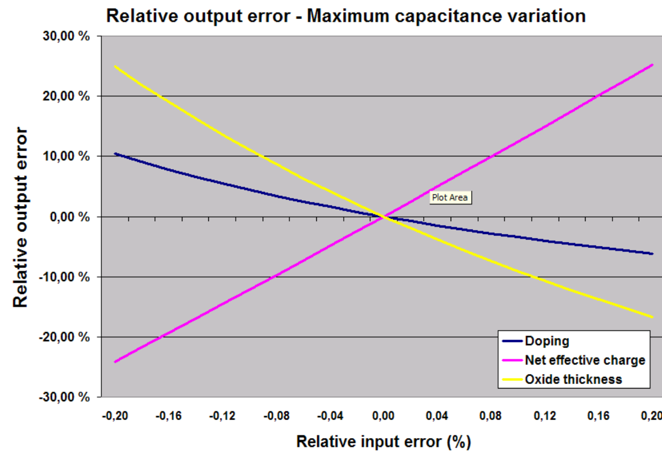

Figure 3.11: Plot of the relative output error ϵ vs. maximum capacitance measurement relative error. Both quantities are expressed as percentages. The three output relative error quantities behave linearly for the whole range of input variation.

A second analysis was performed to determine how variations in the minimum measured capacitance affect the results of the computations. This quantity is determined for bias voltages in inversion region and it often happens that a wrong value is measured. As mentioned above, this happens when the sample enters for example the deep depletion region and the measured value can be considerably lower than the expected one. Furthermore, an undesired increase in this value can be observed when the measurements are not carried out in a totally dark environment. In that case the carrier generation process induced by light can bring the sample out of the equilibrium condition and the measurement results are higher than expected. Although this variations amount to a small percentage of the expected value, in this analysis the minimum capacitance was varied in a 20% range. The following Table 3.6 presents the numerical results.

As expected, the computation for oxide layer thickness is not

Table 3.4: Numerical results of sensitivity analysis for minimum capacitance variation. The row in bold characters is the correct unperturbed value.

Area (cm^2)	N_A (cm^{-3})	N_{eff} (cm^{-2})
9,36E-10	2,67E+15	2,84E+12
9,59E-10	2,84E+15	2,86E+12
9,83E-10	3,01E+15	2,87E+12
1,01E-09	3,19E+15	2,89E+12
1,03E-09	3,38E+15	2,91E+12
1,05E-09	3,58E+15	2,92E+12
1,08E-09	3,78E+15	2,94E+12
1,1E-09	3,99E+15	2,95E+12
1,12E-09	4,21E+15	2,97E+12
1,15E-09	4,43E+15	2,98E+12
1,17E-09	**4,66E+15**	**2,99E+12**
1,19E-09	4,9E+15	3,01E+12
1,22E-09	5,15E+15	3,02E+12
1,24E-09	5,41E+15	3,03E+12
1,26E-09	5,68E+15	3,05E+12
1,29E-09	5,95E+15	3,06E+12
1,31E-09	6,24E+15	3,07E+12
1,33E-09	6,53E+15	3,09E+12
1,36E-09	6,83E+15	3,1E+12
1,38E-09	7,14E+15	3,11E+12
1,4E-09	7,47E+15	3,12E+12

affected by fluctuations in the minimum capacitance value. The doping density is affected in an opposite fashion compared to variations in the maximum oxide capacitance value. Anyway the effect of minimum capacitance fluctuations on doping density computation are more severe than for the maximum capacitance case. From Fig. 3.12 it can be seen that this effect amounts up to 40 % in relative output error for the minimum capacitance at the extreme of the curve, three times larger than the corresponding variation for oxide layer capacitance. On the other hand, the net effective charge value is lightly affected even by 20 % change in minimum capacitance value. The relationship between the output relative error and the input variation for the minimum capacitance is still linear although the slope of the curve is really small.

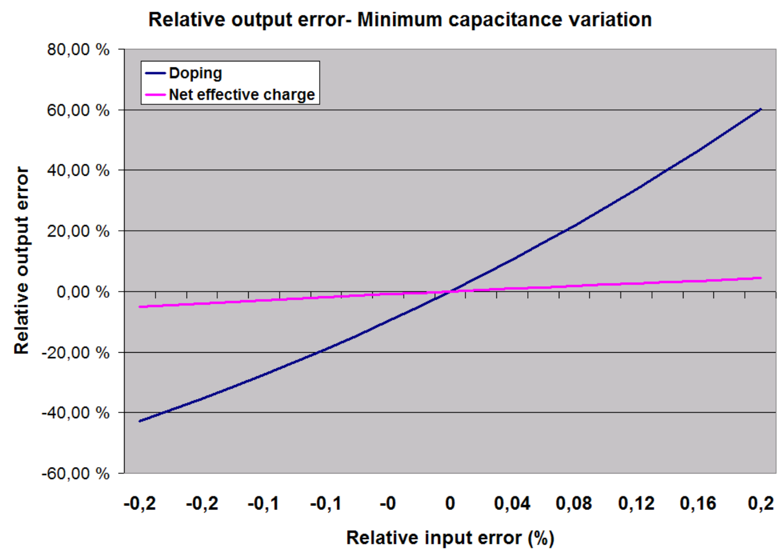

Figure 3.12: Plot of the relative output error ϵ vs. minimum capacitance measurement relative error. Both quantities are expressed as percentages. The two output relative error quantities behave linearly for the whole range of input variation.

Chapter 4

Examples of measurements

Within the activity conducted for this thesis work, the CV measurement system has been used to analyze many samples, both for test and verification and for material research purposes. In particular, CV measurements have been used to investigate the properties of aluminum oxide - silicon interfaces, for aluminum oxide deposited with ALD process.
In this chapter some examples from the measurement conducted in the Electron Physics Group laboratory will be reported.
In the first section the samples' fabrication process will be described briefly, focusing on the characteristics relevant to CV measurements.

4.1 Sample fabrication

CV measurements are performed essentially on tipical metal-insulator-silicon (MIS) structures.

The CV measurement system implemented as the result of this thesis work has been tested and used on different types of MIS structures. Although the general structure of the samples was similar, some characteristic changed regarding the insulator material, the front contacts shapes and deposition methods and

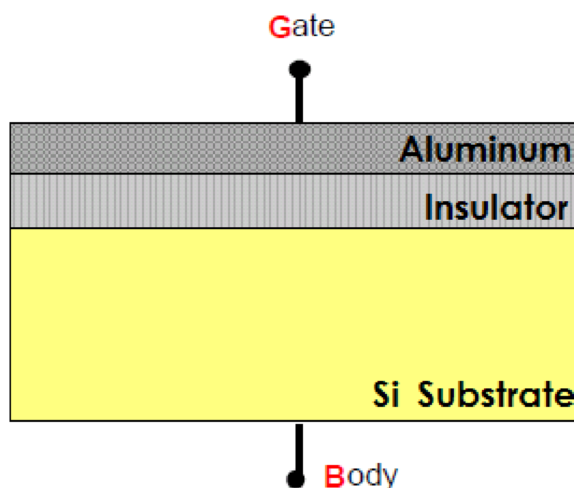

Figure 4.1: Basic structure of a metal-insulator-silicon (MIS) device.

the back contact fabrication.
The substrate material used was CZ silicon for all the samples. The substrate was doped with n or p-type impurities in different samples, with resistivity in the range 2.7 - 3 Ω.
The insulator material used was silicon oxide or aluminum oxide. In the first case, a layer of silicon oxide was grown using a thermal oxidation process in the furnace. In the latter case, aluminum oxide was deposited using Atomic Layer Deposition (ALD). The CV measurements focused on the Al_2O_3 interface properties when the deposition parameters and the processing conditions were varied. The front contacts were fabricated using aluminum deposited with thermal evaporation. Firstly, deposition by sputtering was used but then it was noticed that this process introduced a high density of defects at the interface, affecting the results of CV measurements. The thickness of the contacts was in the range 200-300 nm while the shape was varied in order to have an oxide capacitance in accumulation in the range 30 - 140 F.
The fabrication of the back contact will be described next in a more detailed way because it's strongly related to the sample

preparation for measurements. The presence of a thin (around 1.2 nm) SiO_x layer between aluminum oxide and silicon is reported in the literature for ALD processes [28]. The formation of this layer has been assumed to be the result of the exposure of the substrate to the O_2 plasma in the initial ALD cycles. However, annealing processes lead to the formation of a similar layer independently from the initial interface [29] [30]. Although it was claimed that this SiO_x could play an important role with respect to Al_2O_3 passivation mechanism [31] [32], its presence was neglected for what concern CV measurements.

4.1.1 Contact formation

The preparation of the sample before the measurements is an important step to obtain reliable results. Particularly important is the choice of the technique for the realization of a good ohmic contact in the back surface of the sample. Different solutions have been tried and a proper one has been chosen that ensures reliable results and easiness in processing.

4.1.1.1 Aluminum + oxide

The first attempt was to have the backside entirely coated with evaporated aluminum metal contacts. Since the samples had usually an oxide layer on both sides, a huge capacitance is present also on the backside. According to our first analytical consideration, this capacitance is big enough to be a short circuit in the frequency of interest for HF CV measurements in accumulation and strong inversion. Anyways this solution was discarded because some non-idealities were observed in the measurements for voltage ranges for which the sample is in accumulation and depletion region. The results were compared

with the ones from InGa backcontact samples, fabricated with the same process and having same front contact size. Although no further investigation was made about the underlying mechanisms, these undesired effects were attributed to the bad ohmic contact and the influence of a large capacitance on the back surface.

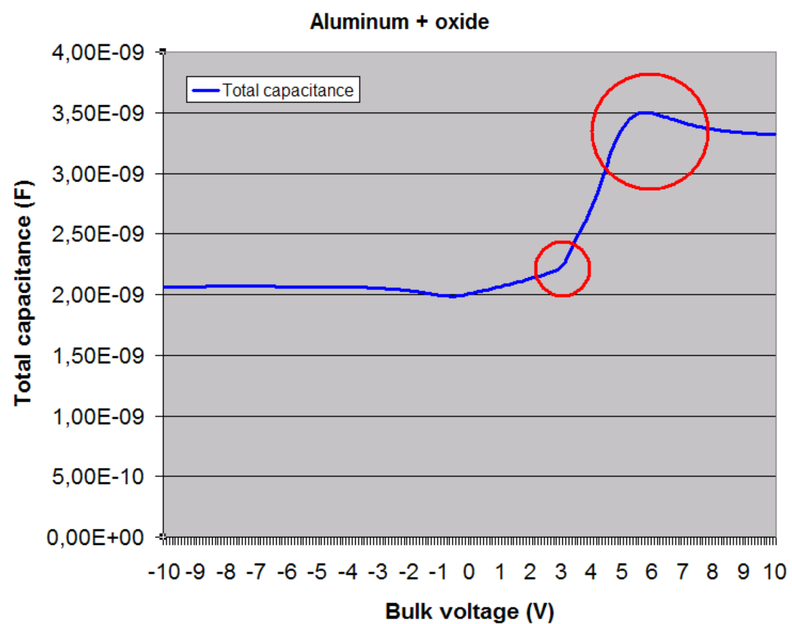

Figure 4.2: Example of a CV curve measured on a sample prepared with evaporated Aluminum on the back surface to make the contact. The sample was a MOS device with p-type silicon substrate, silicon oxide insulating layer and aluminum front contacts. The red circles shows the undesired effects in the results.

4.1.1.2 Bare aluminum

The second method was to include an additional manufacturing process to remove the oxide layer on the backside by chemical etching. Evaporation has then been used to deposit an aluminum layer on the back surface. In this way a good ohmic con-

tact was formed between the silicon surface and the aluminum layer. The results were considerably good. This method was avoided because of the increased time and effort needed for the additional samples' processing steps compared to the obtained results.

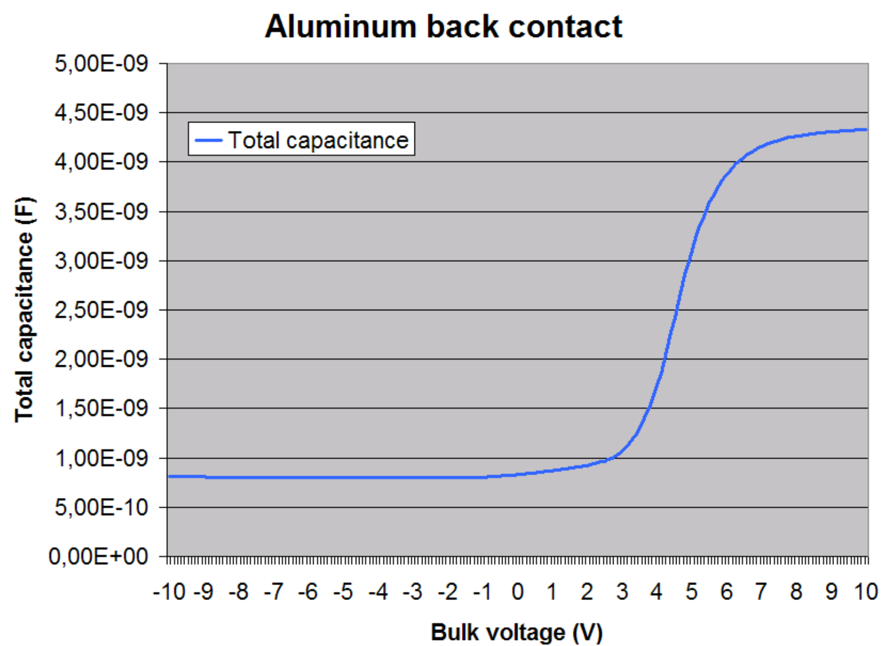

Figure 4.3: Example of a CV curve measured on a sample prepared with aluminum to make the backcontact after backside oxide removal. The sample was a MOS device with p-type silicon substrate, silicon oxide insulating layer and aluminum front contacts.

4.1.1.3 InGa eutectic

The last option is to prepare an ohmic contact on the back surface by means of InGa eutectic. An eutectic is a mixture of chemical components that has a single chemical composition that solidifies at a lower temperatures than any other composition made of the same elements. The back surface is first scratched carefully with a diamond-tip pen or with a tiny piece of sand-paper to generate a high density of surface defect and remove the oxide layer on the back. A small amount of InGa eutectic is then deposited on the surface of the sample and is applied to the area where the contact has to be made by scratching again with the diamond-tip pen or sandpaper. The entire process is fast and can be performed in less than 5 minutes. This option has been preferred to the first twos because it offers the best trade-off between the easiness and the time required to make the contact and the quality of the results. Of course the InGa eutectic contact is a "dirty" processing method and considerations have to be made to take into account a careful handling of the samples in following steps.

4.1.1.4 Front contact blistering

During the measurement a particular effect was observed on the front contacts. When a bias is applied in a such a way that the sample is biased in strong inversion, bubbles or craters appear on the surface of the front contact where the voltage is applied. It must be kept in mind that in the specific setup prepared for CV measurements in our lab, a constant zero voltage is applied on the gate of the sample while the biasing voltage is applied to the substrate. The blistering effect appears only for values higher than a certain voltage and until a limit value the density of blisters seems proportional to the applied voltage. The follow-

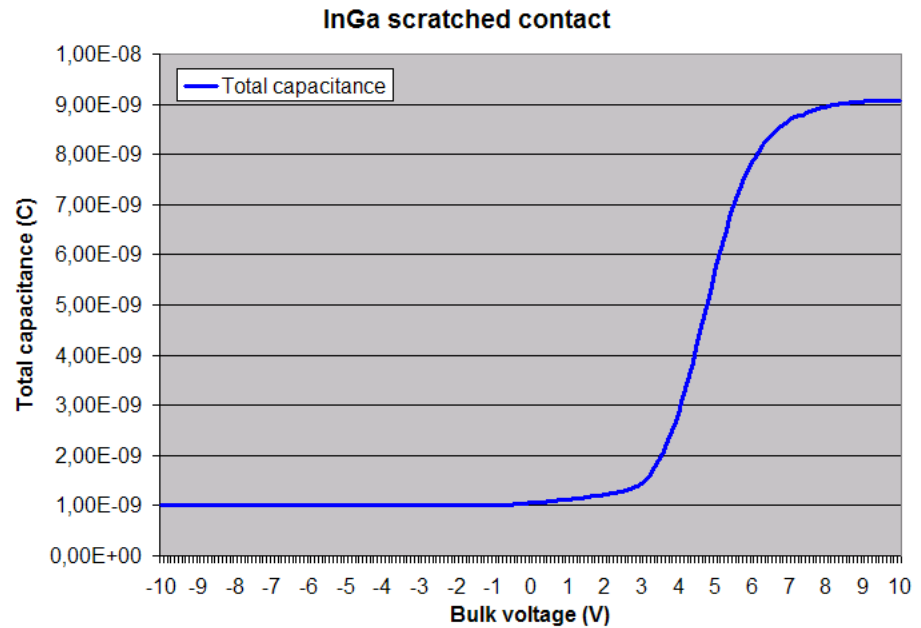

Figure 4.4: Example of a CV curve measured on a sample prepared with InGa eutectic to make the backcontact. The sample was a MOS device with p-type silicon substrate, silicon oxide insulating layer and aluminum front contacts.

ing pictures,taken using an optical microscope with a camera, show the surface of a front contact before and after applying the voltage. The sample was a MIS device with a p-type substrate, a 10nm thick insulating layer of aluminum oxide deposited by ALD and aluminum front contacts. Contacts are 250 nm thick, radius is 100 μm and they were made by thermal evaporation. The threshold voltage at which the blistering appears is -5 V. The appearance of the blisters can be observed with a optical microscope and the time-span of the process is less than 1 second.

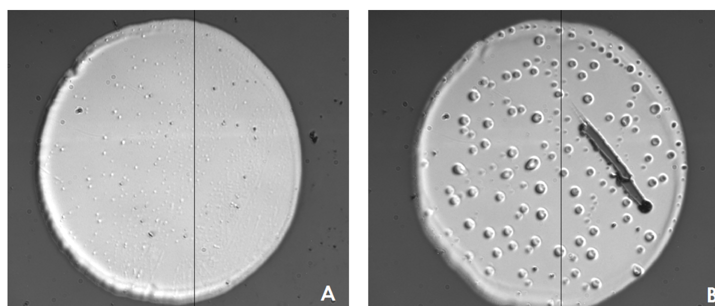

Figure 4.5: A) Front contact of a MIS device before applying any biasing voltage. Some blisters can be observed initially on the surface. B) Front contact after applying a strong inversion biasing voltage. Blisters or craters appears on the surface.

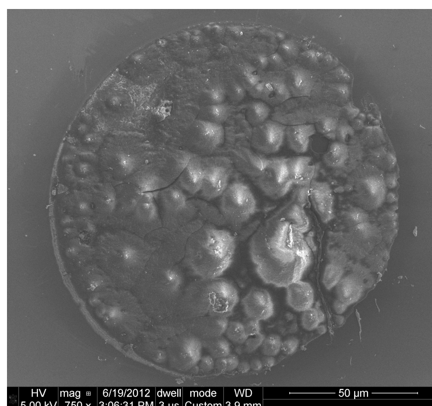

Figure 4.6: SEM top view picture of an aluminum contact after applying a voltage in inversion. Blistering can be clearly observed on the surface. Picture by Mikhail Erdmanis.

4.2 MIS parameter extraction

In this section some examples of parameters extraction from real CV measurements are presented. Both cases are included with samples having thermally grown silicon oxide or ALD aluminum oxide as insulating layer.

The samples were measured using the HP 4192A impedance analyzer and a Labview software to acquire data. Open and short-circuit measurements were executed in order to correct the

measured impedance. The results were then saved in a spreadsheet for analysis.
The first sample is a MOS device. The substrate is CZ silicon with resistivity in the range 2.7 - 3 Ω. The insulating layer is 27nm thick SiO_2 (silicon oxide) thermally grown. The front contacts are fabricated with thermally evaporated aluminum. They are circular shaped with a radius of 1.4 mm and a thickness of 250 nm. The thickness of the silicon oxide layer was measured optically with the ellipsometer. Fig 4.7 shows a plot of the capacitance vs. voltage curve computed directly from the raw data using Eq. [3.1]. The second example is from a MIS

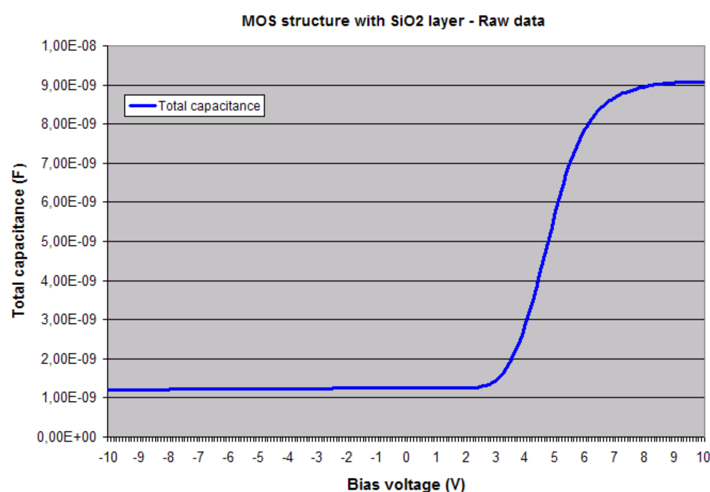

Figure 4.7: Total capacitance vs. voltage curve extracted from raw measurement using Eq.[3.1].The sample is a MOS device with p doped substrate and SiO_2 dielectric layer. No corrections were performed on the data.

structure. The materials and the fabrication processes are similar as in the previous case. The differences are the insulating layer this time Al_2O_3 deposited by ALD and the area of the contacts that now have a radius of 100μm. The thickness of the aluminum oxide layer is determined accurately from the number of deposition cycles and the thickness of an atomic layer to be 20 nm. This value has been confirmed by ellipsometry measure-

ment. Differently from the previous case, the relative dielectric constant of ALD aluminum oxide is not exactly known. After the deposition the sample has been annealed. Since the dielectric constant is related to the lactice properties of the material, the value changes depending on the deposition process used, the following annealing and thermal processes. In the specific case of ALD aluminum oxide, the thickness of the dielectric layer was exactly determined, so the value of the relativ dielectric constant was determined from the total capacitance value in accumulation solving Eq.[2.14] for ϵ_s. The following figure presents the total capacitance computed from raw data of ALD aluminum oxide MIS device measurements.

The raw data were then analyzed using the Matlab software

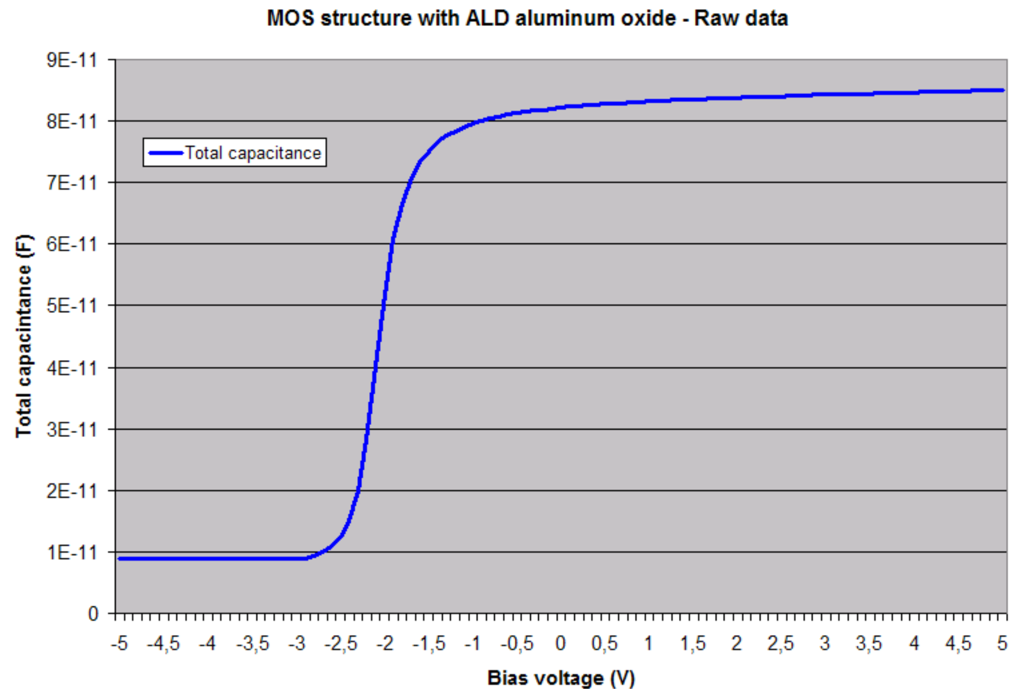

Figure 4.8: Total capacitance vs. voltage curve extracted from raw measurement using Eq.[3.1].The sample is a MOS device with p-type substrate and ALD Al_2O_3 dielectric layer. No corrections were performed on the data.

in order to extract important physical properties and compare the results with the theory. In the following part the results are briefly presented and commentd
For the MOS sample with silicon oxide firstly the oxide capacitance and the series resistance the sample were computed to be C_{ox} = 7.678 nF and R_s = 5.165 Ω. The oxide thickness was computed using Eq. [2.14] to obtain t_{ox} = 27.03 nm as in the optical measurements. The software then computed the average doping density assuming a uniform ionized dopant distribution, using the minimum-maximum capacitance method and Eq.[2.17]. The result is $N_A = 4.66 \times 10^{15} cm^{-3}$ that corresponds to a resistivity of 2.99 Ω, in perfect agreement with the resistivity range given by the substrate wafer manufacturer. The total capacitance at flatbands and the flatband voltage were then extracted from the measured curve and compared with the theoretical curve in order to obtain the surface fixed charge density at the silicon-silicon oxide interface and the net effective charge. Using Eq.[2.15] the results were a surface charge density $Q_o = 5.045 \times 10^{-7}$ C and a corresponding net fixed oxide charge density $N_{eff} = 3.153 \times 10^{12}$ cm^{-2}. The sign and magnitude of the charge distributions are evident from a comparison of the measured CV curve with the theoretical curve computed for the same doping density. The stretchout of the slope of the measured CV curve in the depletion region indicates the presence of interface traps. Fig. 4.9-A shows a plot of experimental and theoretical CV curves for this sample.
. The density of interface trap charges has also been computed for a range of bias voltage for which the sample is in depletion region. Fig. 4.10 shows the interface trap charges density computed used the Terman method on the measurement data. A similar process was used to analyze ALD Al_2O_3 sample. In this case, however, a certain degree of uncertainty exists about the exact value of the dielectric permittivity constant of ALD alu-

minum oxide. It was assumed that the ALD process resulted in a precise thickness of 20 nm and then the dielectric constant value was fitted in order to match that value, using Eq. [2.14] and capacitance measurement in strong accumulation. The relative dielectrive permettivity constant was found to be $\epsilon_r = 4.37$ and the result was verified by means of optical measurements. The series resistance resulted to be $R_s = 98.06 \quad \Omega$ and the oxide capacitance was $C_{ox} = 84$ pF. The ionized dopant impurity concentration was computed using Eq.[2.17] leading to $N_A = 4.6 \times 10^{15}$ cm^{-3} that corresponds to a resistivity value of 3.04 Ω, in agreement with the data from the manufacturer for the initial substrate doping.
Fig.4.9-B shows a comparison of the theoretical and measured CV curves. In this case, the right shift of the measured CV curve in comparison to the theoretical curve means that there's a oxide charge density with negative polarity. The flatband voltage has indeed a negative sign and net effective charge density was computed to be $N_{eff} = -3.65 \times 10^{12}$ cm^{-2}.

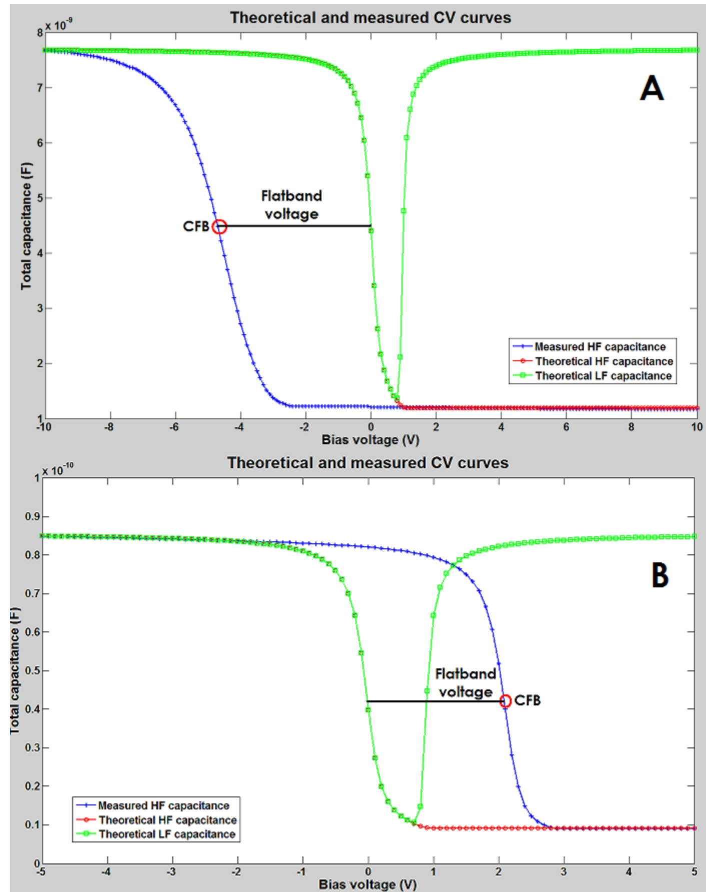

Figure 4.9: A - Comparison of theoretical and experimental CV curves for the Al-SiO_2-Si sample. It can be observed that the measured CV curved is shifted to the left compared to the theoretical results. This shift depends on the amount of oxide fixed charges. The value of the total capacitance C_{FB} at flatband is indicated on the curve.
B - Al-Al_2O_3-Si sample. The measured CV curved is shifted to the right compared to the theoretical results.

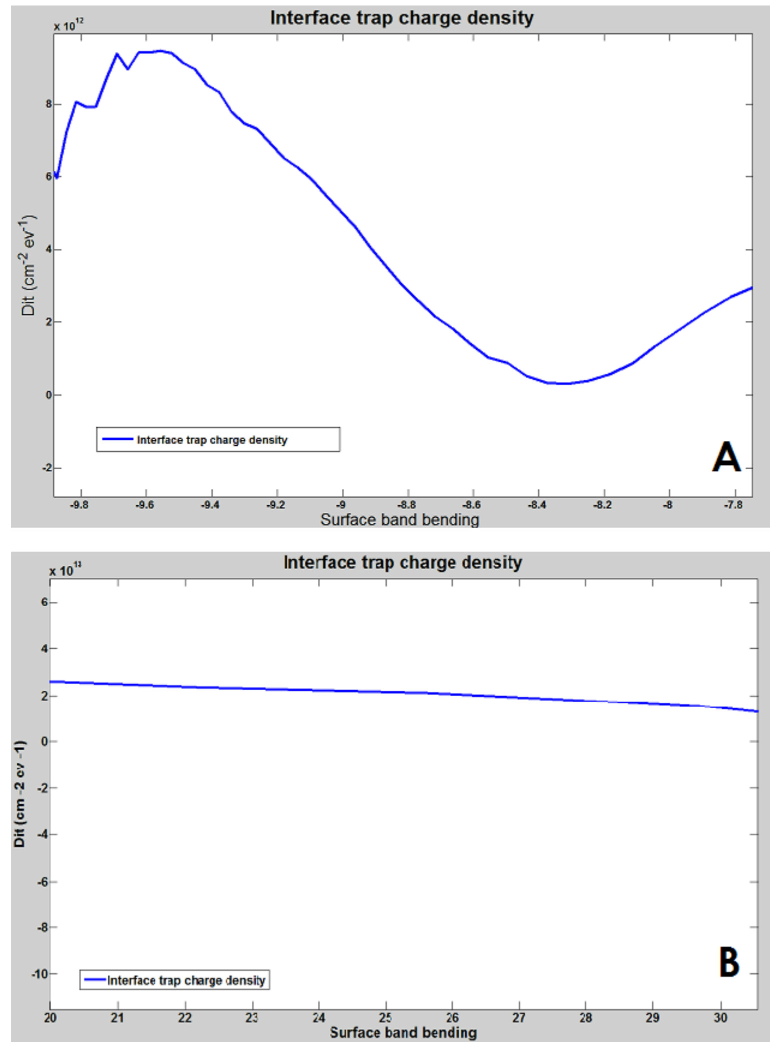

Figure 4.10: A - Plot of D_{it} vs. surface band bending for a MOS sample with SiO_2 dielectric layer computed using Terman method. Data are shown only in the range of band bending values corresponding to bias voltages for which the sample is biased in depletion region and weak inversion.
B - Plot of D_{it} vs. surface band bending for a MOS sample with Al_2O_3 dielectric layer.

Chapter 5

Examples of applications

The CV measurement system was developed and employed within the framework of the PASSI project which aims to study the passivation effects of ALD aluminum oxide on silicon wafers for photovoltaic applications. The project is lead by the Aalto University's Electron Physics Group in collaboration with partners from the industry.

In particular, CV measurements have been used for different tasks related to material research for the characterization of the interface after different ALD aluminum oxide processes in collaboration with Beneq Oy. Although Al_2O_3 has been already studied and confirmed as an excellent passivation agent on p-type doped silicon surfaces, the passivation mechanism itself and the properties of the Al_2O_3/Si interface are not well understood yet. A set of measurements was carried out to study the changes in net effective charge and interface trap density for samples in which the ALD process used different chemicals as precursors. In addition, also the effect of following processing steps and thermal treatments like annealing and firing was characterized with CV measurements.

The results of CV measurements were then compared with the ones from charge carrier lifetime measurements. The final goal is to find a correlation or a relationship between the change in

net effective charge and interface quality and the charge carrier lifetime to understand which mechanisms improve the ALD process for surface passivation.
Fig. 5.1 is a plot from CV measurements of a set of sample with ALD aluminum oxide as insulator layer. The samples have the same structure and the same precursor was used for the deposition. After the ALD step, the three samples were treated thermally in different ways. One of the sample did not go through further processing. A second one was annealed at 400°. On the third one, a firing step after annealing was applied. The plot shows how the oxide charges and the interface trap charge density values are modified during different fabrication processes. The results are in general agreement with in the literature [33], although in this specific example a full comparison can't be presented because the precursors used were different. Several

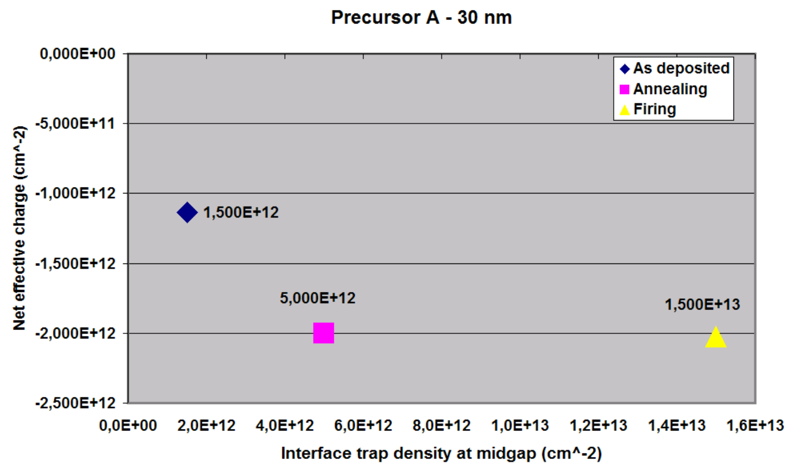

Figure 5.1: Net effective charge and density of interface trap charges for three ALD aluminum oxide MIS samples. The samples are identical but different thermal treatments were applied after deposition. Substrate is p-type silicon and contact area is A = $3.14 \times 10^{-4} cm^2$.

samples have been so far analyzed, trying to study the quality of different ALD precursors and the effect of different thermal treatments and fabrication parameters.

Chapter 6

Conclusions

The realization of a full CV measurement system was carried out as the largest part of this thesis. In this work, the system was presented and analyzed. A study about the performances of the system in terms of properties like precision and sensitivity was also conducted. The results were satisfactory although there is still room for improvement. During the system calibration tests, the results of the software analysis were in agreement with the data from the optical measurements and from the data already known from the fabrication process. This establishes the CV system as a new investigation tool for all the users of the Electron Physics Group.

Another considerable part of the work in this master thesis was the characterization of different set of samples by CV measurements for research purposes regarding passivation properties of ALD Al_2O_3. The main challenge was to learn the correct procedures about how to measure reliably the samples and how to interpret the results.

As a result of the analysis, CV measurement provided further insight and data when used together with charge carrier lifetime measurement. Due to the specific nature of the samples, there are no existing results in the literature available for comparison. However the conclusion drawn from CV data analysis were

anyway consistent with fundamental theoretical considerations and hopefully will provide additional value to future research activity.

Although the final outcome of this work can be considered satisfactory, it is somehow natural to hope for a further improvement or extension of the system.In particular, in this thesis, the difficulties and the divergencies from the initial project have been presented with the hope that they will represent a promising starting point for who will continue to develop this topic.
Without any doubt the main improvement should start from the main failed attempt, namely the inclusion of low-frequency CV curves in the measurement system. As discussed in the main part of this thesis, LF CV curves would provide additional information about the sample and would reduce the error bound and increase the detection limit. There are basically two ways to accomplish this: an upgrade in the lab equipment or the development of a method to reduce the noise in very low current measurements. Althought the second option requires some additional time and creativity, it is probably the best trade-off between easiness and cost. Furthermore a development of a software analysis for conductance method data is expected to be realized. The impedance analyzer currently used and the LabView software already allow the user to perform conductance measurements. Anyway some calibration for the measurement parameters and an extension of the Matlab code is required in order to analyze the results. The advantage would be the opportunity to gain additional information about capture coefficients which amongst density affect the charge carriers lifetime.
For what concern the software part, improvements could be applied to the code in two different ways. The first one is to in-

clude more advanced computations that would take into account for example interface proximity effects and statistical variations. The second approach to code improvement would be a detailed study for the algorithm optimization in order to reduce the computation time and the resolution of the results. Nevertheless this issue is less critical.

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