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LOW-POWER FRONT-ENDS FOR CAPACITIVE THREE-AXIS ACCELEROMETERS

Doctoral Dissertation

Mika Kämäräinen

Aalto University
School of Science and Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences

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Abstract

This thesis consists of six publications and an overview of the research topic. The overview concentrates on background information of the capacitive accelerometers and front-ends. The publications focus on two low-power front-ends that were implemented for capacitive three-axis accelerometers and their operation as a part of an interface.

The switched-capacitor front-ends that were implemented are based on the charge-balancing structures, namely a self-balancing bridge and a $\Delta\Sigma$ front-end, which convert the capacitive acceleration information to analog and digital signals, respectively. Both structures operate mechanically in open-loop configuration and are capable of reducing the effects of the electrostatic forces and displacement-to-capacitance conversion.

According to the performance comparison presented in this thesis, both interfaces, which were implemented around the front-ends, exhibit competitive performance when compared to the commercial products of the day.

Keywords capacitive three-axis accelerometer, electrostatic forces, front-end, power consumption

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Matalatehonkulutuksiset anturietuasteet kapasitiivisille kolmiakselisille kiihtyvyysantureille

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Työn ohjaaja	

Tiivistelmä

Tämä väitöskirja koostuu kuudesta julkaisusta ja tutkimusaiheen yhteenvedosta. Yhteenveto keskittyy kapasitiivisten kiihtyvyysantureiden ja anturietuasteiden taustatiedon käsittelyyn. Julkaisuiden keskipisteenä ovat kaksi toteutettua matalatehonkulutuksista anturietuastetta kapasitiivisille kolmiakselisille kiihtyvyysantureille ja näiden anturietuasteiden toiminta osana anturirajapintaa.

Toteutetut kytkin-kapasitanssi anturietuasteet perustuvat varauksen tasapainottaviin rakenteisiin, itsetasapainottuva silta ja $\Delta\Sigma$ anturietuaste. Jälkimmäinen rakenne muuntaa kapasitiivisen kiihtyvyysinformaation digitaaliseksi ja ensimmäinen rakenne analogiseksi jännitteeksi. Kummatkin rakenteet toimivat mekaanisesti avoimen silmukan kokoonpanossa ja ovat kykeneviä vähentämään sähköstaattisten voimien sekä poikkeamasta kapasitanssiksi muunnoksen vaikutuksia.

Väitöskirjassa esitetyn suorituskykyvertailun mukaisesti kummatkin anturirajapinnat, jotka ovat rakennettu anturietuasteiden ympärille, ovat kilpailukykyisiä tämänpäivän kaupallisten tuotteiden kanssa.

Asiasanat anturietuaste, kapasitiivinen 3-akselinen kiihtyvyysanturi, sähköstaattiset voimat, tehonkulutus

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Preface

The research for this thesis was carried out in the Electronic Circuit Design Laboratory, Aalto University School of Science and Technology (formerly Helsinki University of Technology), Espoo, Finland, during the period 2004-2010. The main results of the research were achieved in two projects. The first project "Capacitive Sensor Interface" (CAPACIF) was carried out from 2004 to 2006 and was funded jointly by the Nokia Research Center, VTI Technologies, and the Finnish Funding Agency for Technology and Innovation (TEKES). The second project "Miniaturized Capacitive Sensor Interface" (MINICIF) was carried out from 2006 to 2008 and was funded by VTI Technologies and TEKES. From 2008 to 2010 I had the privilege of participating in the Graduate School, Faculty of Electronics, Communications and Automation, which partially funded the research. In addition, during these two years the Centre of Excellence program (SMARAD2) was another funder of the research. I was also honored to have scholarships from the Ulla Tuominen Foundation and the Walter Ahlström Foundation. I am extremely grateful for all the above mentioned financiers for making the research work possible.

Also, I am pleased that VTI Technologies and the Nokia Research Center permitted us to publish the results of the research. Furthermore, I would like to thank VTI Technologies for providing the sensor elements and making the rate table measurements possible. I am grateful to the staff of VTI Technologies and the Nokia Research Center who participated in our projects, and especially to Mr. Teemu Elo, Dr. Teemu Salo, Mr. Tero Sillanpää, and Mr. Kimmo Törmälehto for their valuable comments and discussions. Mr. Teemu Elo also deserves thanks for his time and assistance in the rate table measurements.

I would like to express my gratitude to my supervisor, Professor Kari Halonen, for giving me an interesting research topic and an opportunity to work in such an inspiring working environment as the Electronic Circuit Design Laboratory. I would also like to thank Professor Kari Halonen for his encouragement and trust during these years. I am deeply grateful to Professor Gary K. Fedder from Carnegie Mellon University, Pittsburgh, PA, USA and to Associate Professor Remco Wiegerink from the University of Twente, Enschede, The Netherlands, for their time to review this thesis, and for their valuable comments and suggestions.

I wish to thank the whole staff of the Electronic Circuit Design Laboratory. It has been an honor to work with such motivated, talented and great persons as those in our laboratory. In particular, I want to highlight the contribution of the following persons. I wish to warmly thank the team members with whom I had the privilege to work (in alphabetical order): Dr. Jere Järvinen, Dr. Lauri Koskinen, Dr. Marko Kosunen, Dr. Mika Laiho, Erkka Laulainen, Dr. Matti Paavola, and Dr. Mikko Saukoski. Together we have achieved great results. Words cannot de-

scribe how grateful I am to my super-talented instructor Dr. Mikko Saukoski. I would not have made it this far without his unlimited support, great ideas, and encouragement. You are an amazing person, Mikko. With Dr. Matti Paavola, who is the most hard-working and reliable person I know, I have co-operated closely from the beginning of our projects. We have shared a lot of tough and glorious moments and I am very grateful of all the days we have worked together. Lasse Aaltonen was the examiner of my Licentiate's thesis and I would like to thank him for numerous valuable discussions and comments during these years. In addition, I wish to thank (in alphabetical order) Lasse Aaltonen, Dr. Jere Järvinen, Dr. Mika Laiho, Dr. Matti Paavola, and Dr. Mikko Saukoski for all the free-time activities we have spent together. During the years I have had the privilege to work with many great personalities, such as my office colleagues, and have shared many good conversations and moments (in alphabetical order of the people not mentioned above): Saku Hämäläinen, Artturi Kaila, Antti Kalanti, Jussi Mustola, Tero Nieminen, Jussi Pirkkalaniemi, Pasi Rahikkala, and Timo Speeti. Additionally, I would like to express my heartfelt gratitude to our secretaries Anja Meuronen, Lea Söderman, and Helena Yllö for interesting discussions and for helping me through all the practical matters.

My mother Hilkka, father Paavo, and brother Jukka have always had time for me. There are no words which could fully describe my gratitude for you. You have given me so much unconditional support and love. Without that I could not have achieved anything. During my life, I have had the possibility to get know many amazing people, all of whom have had an impact on the direction of my life. I am extremely grateful to all of them.

Finally, I would like to thank my girlfriend, Jaana. You are my sunshine who makes my every day memorable and worth living. You have supported, loved and encouraged me so much. I am so grateful that I met you. I love you.

Helsinki, October 2010

Mika Kämäräinen

Contents

List of Publications

[**P1**] M. Paavola, M. Kämäräinen, J. Järvinen, M. Saukoski, M. Laiho, and K. Halonen, "A 62μA interface ASIC for a capacitive 3-axis micro-accelerometer," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, USA, Feb. 2007, pp. 318–319.

[**P2**] M. Paavola, M. Kämäräinen, J. A. M. Järvinen, M. Saukoski, M. Laiho, and K. A. I. Halonen, "A micropower interface ASIC for a capacitive 3-axis micro-accelerometer," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 12, Dec. 2007, pp. 2651–2665.

[**P3**] M. Kämäräinen, M. Saukoski, M. Paavola, J. A. M. Järvinen, M. Laiho, and K. A. I. Halonen, "A micropower front end for three-axis capacitive microaccelerometers," *IEEE Transactions on Instrumentation and Measurements*, vol. 58, no. 10, Oct. 2009, pp. 3642–3652.

[**P4**] M. Kämäräinen, M. Paavola, M. Saukoski, E. Laulainen, L. Koskinen, M. Kosunen, and K. Halonen, "A 1.5μW 1V 2$^{\text{nd}}$-order $\Delta\Sigma$ sensor front-end with signal boosting and offset compensation for a capacitive 3-axis micro-accelerometer," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, San Francisco, CA, USA, Feb. 2008, pp. 578–579.

[**P5**] M. Paavola, M. Kämäräinen, E. Laulainen, M. Saukoski, L. Koskinen, M. Kosunen, and K. Halonen, "A 21.2 μA $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer," in *Proc. IEEE Asian Solid-State Circuits Conference*, Fukuoka, Japan, Nov. 2008, pp. 101–104.

[**P6**] M. Paavola, M. Kämäräinen, E. Laulainen, M. Saukoski, L. Koskinen, M. Kosunen, and K. A. I. Halonen, "A micropower $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 11, Nov. 2009, pp. 3193–3210.

Author's contribution

The results of this thesis are based on two projects which were carried out in 2004-2006 and 2006-2008, respectively. The common goal of the projects was to design and implement a low-power interface for a capacitive three-axis accelerometer. The supervisor of the projects was Prof. Kari Halonen. Dr. Mikko Saukoski was the project manager in the first project and partly during the second one (until the end of the year 2007), after which Dr. Matti Paavola continued his work. In addition to the author, Dr. Matti Paavola, Dr. Jere Järvinen, Dr. Mikko Saukoski, and Dr. Mika Laiho worked in the first project, while those who worked in the second project besides the author were Dr. Matti Paavola, Mr. Erkka Laulainen, Dr. Mikko Saukoski, Dr. Lauri Koskinen, and Dr. Marko Kosunen. During the projects, Dr. Mikko Saukoski instructed the author. Dr. Matti Paavola was instructed by Dr. Mika Laiho, mainly during the first project. In the course of the projects, Mr. Lasse Aaltonen contributed with much valuable discussion and advice.

The publications of [P1, P2, P3] and [P4, P5, P6] are based on the results of the first and the second projects, respectively. As a general rule, the publications were written in cooperation, and the first author had the main responsibility for the article.

[P1] A 62μA interface ASIC for a capacitive 3-axis micro-accelerometer

In the interface, the author was responsible for the circuit design, implementation, and measurements of the front-end. Dr. Matti Paavola was responsible for the clock generators and voltage, current, and temperature reference circuit and Dr. Jere Järvinen was responsible for the analog-to-digital converters (ADCs). Dr. Mikko Saukoski performed the system-level design, together with the design of the dynamically biased operational amplifiers. Mr. Pasi Rahikkala, Mr. Tapio Rapinoja, and Mr. Olli Viitala assisted in the layout drawing. The system measurements were carried out mainly by the author and Dr. Matti Paavola.

[P2] A micropower interface ASIC for a capacitive 3-axis micro-accelerometer

In the interface, the author was responsible for the circuit design, implementation, and measurements of the front-end. Dr. Matti Paavola was responsible for the clock generators and voltage, current, and temperature reference circuit and Dr. Jere Järvinen was responsible for the ADCs. Dr. Mikko Saukoski carried out the system-level design, together with the design of the dynamically biased operational amplifiers. Mr. Pasi Rahikkala, Mr. Tapio Rapinoja, and Mr. Olli Viitala assisted in the layout drawing. Ms. Sanna Heikkinen assisted in the ADC measurements. The system measurements were performed mainly by the author and Dr. Matti Paavola.

[P3] A micropower front end for three-axis capacitive microaccelerometers

The author was responsible for the circuit design, implementation, and measurements of the front-end. The voltage and current references designed by Dr. Matti Paavola were used in the measurements. Moreover, the whole interface considered in the publications [P1, P2] was used in some measurements.

[P4] A 1.5μW 1V 2$^{\text{nd}}$-order $\Delta\Sigma$ sensor front-end with signal boosting and offset compensation for a capacitive 3-axis micro-accelerometer

The author had the main responsibility for the circuit design, implementation, and measurements of the front-end. Dr. Matti Paavola had the main responsibility for the layout drawing and Dr. Mikko Saukoski contributed by designing the required charge pumps, special switches, and clock generator of the front-end. Moreover, in close collaboration, the circuit design, implementation, and measurements of the first prototype of the decimator were carried out by Mr. Erkka Laulainen under the guidance of Dr. Lauri Koskinen and Dr. Marko Kosunen.

[P5] A 21.2 μA $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer

In the interface, the author had the main responsibility for the circuit design, implementation, and measurements of the front-end. In addition, in the front-end, Dr. Matti Paavola had the main responsibility for the layout drawing and Dr. Mikko Saukoski contributed by designing the required charge pumps, special switches, and clock generator. Dr. Matti Paavola had the responsibility for the circuit design, implementation, and measurements of the frequency reference, the voltage and current reference, the reference voltage buffers, and low-dropout regulators. Mr. Erkka Laulainen had the responsibility for the corresponding tasks for the second prototype of the decimator and he was instructed by Dr. Lauri Koskinen and Dr. Marko Kosunen. The system measurements were carried out by the author and Dr. Matti Paavola.

[P6] A micropower $\Delta\Sigma$-based interface ASIC for a capacitive 3-axis micro-accelerometer

In the interface, the author had the main responsibility for the circuit design, implementation, and measurements of the front-end. Moreover, in the front-end, Dr. Matti Paavola had the main responsibility for the layout drawing and Dr. Mikko Saukoski contributed by designing the required charge pumps, special switches, and clock generator. Dr. Matti Paavola had the responsibility for the circuit design, implementation, and measurements of the frequency reference, the voltage and current reference, the reference voltage buffers, and low-dropout regulators. Mr. Erkka Laulainen had the responsibility for the corresponding tasks for the second prototype of the decimator and he was instructed by Dr. Lauri Koskinen and Dr. Marko Kosunen. Mr. Mika Pulkkinen assisted in automating the rate table measurements. The system measurements were carried out by the author and Dr. Matti Paavola.

Symbols and Abbreviations

ΔC	Capacitance change caused by acceleration
Δd	Change in the distance that is induced by acceleration
Δx	Relative distance between the mass and the frame
ω_0	Resonance frequency
$\overline{B}$	Bit average of one-bit output
ϕ_1	Clock phase, non-overlapping with ϕ_2; measurement phase
ϕ_2	Clock phase, non-overlapping with ϕ_1; reset phase
ε_0	Permittivity of vacuum, $8.85419 \cdot 10^{-12}$ F/m
ε_r	Relative permittivity of the insulator
A	Overlapping plate area
a	Acceleration
a_n	Noise floor, in $\mu\text{g}/\sqrt{\text{Hz}}$
a_{max}	Maximum acceleration
BW	Bandwidth
C	Capacitance
C_0	Capacitance with $\Delta d = 0$
C_{CBN}, C_{CBP}	Compensation and boosting capacitors
C_{DAC1}	Digital-to-analog converter capacitor
C_{DN}, C_{DP}	Sensor capacitors
C_D	Capacitance of the single capacitance accelerometer
C_f	Feedback capacitor
C_I	Integration capacitor
D	Damping factor
d	Distance between the capacitor plates
d_0	Initial distance between the capacitor plates

E_C	Energy of the capacitor
E_{tot}	Total energy of the system
E_V	Energy of the voltage source
F_D	Damping force
$F_{es,C_{DN}}$	Electrostatic force of C_{DN}
$F_{es,C_{DP}}$	Electrostatic force of C_{DP}
F_{es,C_D}	Electrostatic force of C_D
F_{es}	Electrostatic force
F_n	Noise density of the thermal noise force, in $\mathrm{N}/\sqrt{\mathrm{Hz}}$
F_s	Spring force
f_s	Sampling frequency
F_{tot}	Total force affecting the mass
g	Gravity of the earth, 9.81 $\mathrm{m/s^2}$
g_m	Transconductance
$H(s)$	Transfer function
I_{dd}	Current consumption
I_D	Biasing current
k	Spring constant
k_B	Boltzmann constant, $1.380658 \cdot 10^{-23}$ J/K
k_{eff}	Effective spring constant
k_{es}	Electrostatic spring constant
m	Mass
Q	Quality factor
$Q_{C_{DN}}$	Charge of C_{DN}
$Q_{C_{DP}}$	Charge of C_{DP}
Q_C	Charge of the capacitor
Q_D	Charge of C_D

Q_V	Charge of the voltage source
R_f	Feedback resistance
R_m	Mechanical resistance
T	Absolute temperature
V	Voltage
$V_{B,max}$	Absolute maximum biasing voltage
V_B	Biasing voltage
V_{dd}	Supply voltage
V_{OFF}	Offset voltage
V_{OS}	Offset voltage source
V_{OUTN_CS}	Output voltage with inverted reference voltages
V_{OUTP_CS}	Output voltage with non-inverted reference voltages
V_{OUT}	Output voltage
V_{REF}	Reference voltage
V_{SIG}	Signal voltage
X_f	Absolute x-directional displacement of the frame
X_m	Absolute x-directional displacement of the mass
$\Delta\Sigma$	Delta-sigma
A/D	Analog-to-digital
ADC	Analog-to-digital converter
ASIC	Application-specific integrated circuit
BiCMOS	Process technology which includes both bipolar and MOS transistors
CDS	Correlated double sampling
CLKG	Clock generator of the front-end
CMOS	Complementary metal-oxide-semiconductor
CS	Chopper stabilization

DAC	Digital-to-analog converter
DDA	Differential difference amplifier
DRIE	Deep reactive ion etching
DSP	Digital signal processor
ESP	Electronic stability program
FOM	Figure of merit
FREF	Frequency reference
GPS	Global positioning system
HF	Hydrofluoric acid
ICMFB	Input common-mode feedback
IREF	Current reference
KOH	Potassium hydroxide
LDO	Low-dropout regulator
MEMS	Microelectromechanical system
MOS	Metal-oxide-semiconductor
MST	Microsystems technology
NMOS	N-type MOS transistor
OTA	Operational transconductance amplifier
PCB	Printed circuit board
PMOS	P-type MOS transistor
PolySi	Polycrystalline silicon
REFBUF	Reference voltage buffer
RIE	Reactive ion etching
SBB	Self-balancing bridge
SC	Switched-capacitor
SEM	Scanning electron microscope
SiO_2	Silicon dioxide

SNR	Signal-to-noise ratio
SOI	Silicon-on-insulator
SYSCLK	System clock generator
TNEA	Total noise equivalent acceleration
TREF	Temperature reference
VREF	Voltage reference

1 Introduction

1.1 Background

Today, the world is mobile. Handheld electrical devices provide applications such as real-time global communication, watching television, listening to music, video recording, and searching for information from the internet, which earlier were possible only with large non-portable devices. The small size, low power consumption, and reasonable prices of the handheld devices have been made possible by the development of microelectronics.

Less than 70 years ago, in 1947, the starting point of microelectronics was witnessed when Bardeen and Brattain managed to build point-contact transistors and, later, Shockley conceived the junction transistor. The transistors made possible the reduction of the size and power requirements and the portability of the devices. In the late 1950s, important steps were taken, as the planar silicon transistor and fabrication process were developed [1], which laid the foundations for the batch fabrication of thousands of identical electrical devices on a single wafer. Nowadays, these microchips include millions of transistors, and the minimum line widths of the processes are on a nanoscale. Microelectronics is a big business; according to Databeans, merely the revenue from microprocessors is $37.2 billion and the total size of the semiconductor market is $258.3 billion in 2010 [2].

The development of microelectronics enabled mechanical components and systems, more generally microelectromechanical systems (MEMS), or microsystems technology (MST), as it is known in Europe, to be miniaturized. By using the same methods as in microelectronics, micromachined components such as pressure sensors and ink-jet nozzles can be fabricated. Similarly to microelectronics, cost-efficient batch fabrication has accelerated the interest in MEMS devices. At present, MEMS applications are becoming general for consumers, as they are found in products such as automobiles, mobile phones, cameras, and toys, which have increased the size of the MEMS markets significantly. According to the market research of Yole Développement [3], the size of the MEMS markets was $7.1 billion and 2 billion units were fabricated in 2007. These values are expected to reach $14 billion and 6.7 billion units by 2012. While the traditional leading ink-jet nozzle markets are freezing near $2 billion [3], the inertial sensor markets are rising, from $1.8 billion (2008) to $3 billion (2013) [4].

Micromachined inertial sensors can be divided into acceleration and angular rate sensors [5], in other words accelerometers and gyroscopes, respectively. Important milestones, such as the first batch-fabricated accelerometer, published by Roylance and Angell in 1979 [6], as well as the first single-chip gyroscope, published by Geen et al. in 2002 [7], are among the factors which have made the success of inertial sen-

sors possible. Nowadays inertial sensors are utilized substantially in automotive and consumer applications. Today's automobiles incorporate safety applications which are based on accelerometers and/or gyroscopes, such as airbags, active suspension, electronic parking brakes, electronic stability program (ESP), and rollover detection. Correspondingly, nowadays, consumer electronics include inertial sensors in, among other applications and devices, pedometers, game controllers, hard disk drive protection systems in laptops, camcorder and camera image stabilization, display orientation, and dead reckoning in global positioning system (GPS). Automotive applications have traditionally dominated the markets, but as the prices of inertial sensors have dropped, their use in consumer electronic applications has been growing fast. In 2008 the market shares of the automotive and consumer electronics were 46% and 36% for accelerometers and 58% and 27% for gyroscopes, as the total sizes of the markets were $1.0 and $0.8 billion, respectively [4]. Accelerometers, especially, are becoming general in mobile phones. It has been projected that one third of the mobile phones shipped in 2010 use accelerometers, which is up from one fifth in 2009 and one eleventh in 2008 [8]. To proportion this growth to the fact that more than a billion mobile phones are sold yearly, in 2009 1.2 billion [9], the accelerometer markets are promising.

Traditionally, accelerometers have been capable of detecting only unidirectional acceleration. By using three-axis accelerometers, all the three vector components of linear acceleration, x-, y-, and z-directional, can be evaluated. The capability to detect the acceleration in any direction enables more applications to be used than single-axis detection does. Smart phones and game controllers, such as the Apple iPhone 3G [8], Google Nexus One [10], Nokia N97 [11], and Nintendo Wii [12], utilize three-axis accelerometers. In order to connect a three-axis accelerometer in a consumer product, sensor interface electronics have to be used which convert the acceleration information into a convenient format for the electrical application, such as a digital signal. In consumer electronics, not only is small size important, but it is also important that the interface has low power consumption, and thus the lifetime of the battery is not limited by the accelerometer application. The selection of the accelerometer mechanism is important from the viewpoint of power consumption. Capacitive accelerometers have advantages such as high sensitivity, good dc response and noise performance, low drift, low temperature sensitivity, and low power dissipation [13], which make them attractive for low-power applications. Capacitive accelerometers are currently the most widely used accelerometers [14]. Nowadays, an accelerometer including a capacitive three-axis accelerometer and low-power interface has been integrated in a 2 mm x 2 mm product [15, 16] which is suitable for portable devices such as the above-mentioned handheld electronic devices.

1.2 Research Contribution

The results of this thesis are based on two discrete-time front-ends of the low-power interfaces of capacitive three-axis accelerometers. In the interface, the front-end is

the part which converts the capacitive accelerometer information into a convenient format for the electrical application, such as an analog or digital signal, and maximizes the linear range of the accelerometer. The low-power front-ends that were implemented reduce both the most significant factors limiting linearity, namely the effects of the electrostatic forces and displacement-to-capacitance conversion.

In the front-end of the first interface, the single-ended self-balancing bridge (SBB) was chosen as the starting point [17]. The transfer function of this structure is ratiometric, linearizing the displacement-to-capacitance conversion. In addition, the topology achieves charge balance, reducing the effects of the electrostatic forces. The differential low-power front-end that was developed converts the capacitive three-axis accelerometer information into analog voltage which is converted to a digital signal by an analog-to-digital converter (ADC). The first interface was published in [P1, P2] and the front-end is described in more detail in [P3]. An earlier version of the front-end was published in [18]. The author was responsible for the design of the front-end and he was instructed by Dr. Mikko Saukoski. The other team members were Dr. Matti Paavola, Dr. Jere Järvinen, and Dr. Mika Laiho.

The second front-end is based on the mechanical open-loop $\Delta\Sigma$ converter topology, the functional principle of which is presented in [19]. In the front-end that was implemented, by using the idea of the structure, the acceleration information of the capacitive three-axis accelerometer is converted directly to a digital signal. As in the earlier front-end, the topology achieves charge balance and its output is ratiometric. One of the main challenges compared to the first front-end was a low 1-V voltage supply. The front-end was first published in [P4]. The front-end and the interface were studied in [P5, P6]. The author was responsible for the design of the front-end and he was instructed by Dr. Mikko Saukoski. The other team members were Dr. Matti Paavola, Mr. Erkka Laulainen, Dr. Lauri Koskinen, and Dr. Marko Kosunen.

More detailed descriptions of the contributions of the publications can be found in the section: Author's contribution. Other publications relating to the topic in which the author was responsible include [20, 21].

1.3 Organization of the Thesis

This thesis is organized into four chapters. Chapter 2 introduces background information about capacitive accelerometers, including the mechanical and electrical properties of single-axis accelerometers and their manufacturing methods and structures, as well as the operating principles of the capacitive three-axis accelerometers that have been published.

Chapter 3 studies the effects of displacement-to-capacitance conversion and the elec-

trostatic forces. In addition, different front-end topologies for capacitive single-axis accelerometers are introduced. Even if the discussion focuses on the discrete-time topologies, the continuous-time front-end structures are not completely omitted. The discrete-time front-end structures are divided according to their abilities to reduce the effects of the electrostatic forces.

In Chapter 4, the front-ends and interfaces that have been implemented are briefly introduced and compared, both mutually and with a force-feedback implementation. The thesis is concluded by a performance comparison in which the interfaces of the thesis are compared with commercially available low-power accelerometers.

2 Capacitive Accelerometers

Several device types have been used to implement micromachined accelerometers, also known as micro-accelerometers[1], such as piezoresistive, capacitive, tunneling, and thermal devices [13]. Generally, these devices consist of a mass which is supported from a frame with springs, as shown in Fig. 2.1[2]. The acceleration of the frame can be defined by an electrical change which is caused by the displacement of the mass.

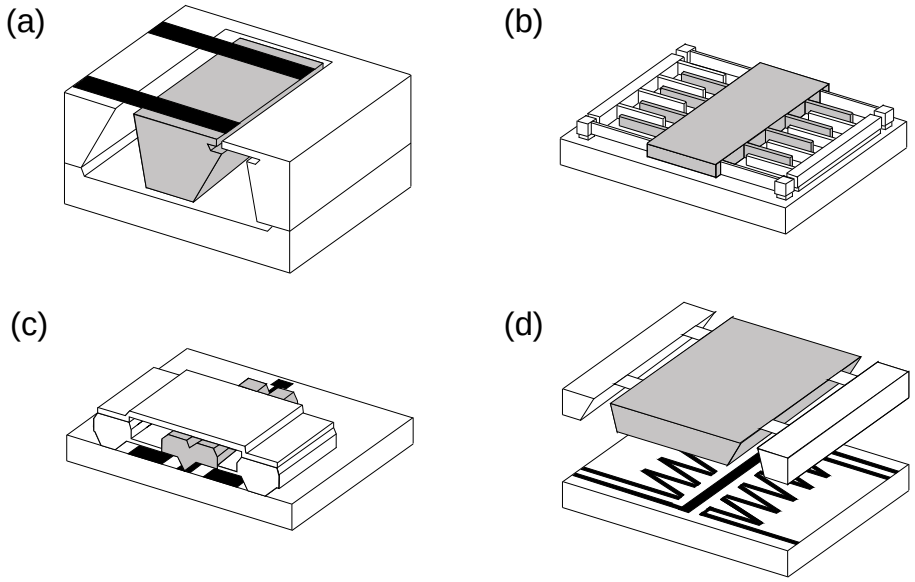

Figure 2.1: (a) Piezoresistive [22], (b) capacitive [13], (c) tunneling [23], and (d) thermal devices [24].

As mentioned in Section 1.1, capacitive accelerometers have a lot of advantages, such as high sensitivity, good dc response and noise performance, low drift, low temperature sensitivity, and low power dissipation, which make them suitable for low-power applications. With the use of a front-end, the capacitive acceleration information of the capacitive accelerometer can be converted to a convenient format for an electrical application, such as an analog or digital signal.

In order to be able to implement front-ends, the fundamentals of capacitive accelerometers have to be understood. Therefore the purpose of this chapter is to give a brief introduction to capacitive accelerometers. The mechanical functionality

[1] In this thesis, for the sake of simplicity, the word micro-accelerometer is usually replaced by the word accelerometer.

[2] As a general rule, the figures in the thesis have been drawn by the author. The references in the captions indicate the publications which were models for the drawings. The author had to make simplifications and interpretations to achieve illustrative three-dimensional figures.

and properties of the accelerometers are studied first mathematically and then, by using the understanding of the mechanical operation, the capacitive accelerometer is modeled electrically. After the modeling, the different methods used to fabricate capacitive accelerometers are discussed. Finally, different implementations of capacitive three-axis accelerometers that have been published are introduced.

2.1 Mechanical Operation of an Accelerometer

Generally, an accelerometer is modeled with a proof mass, a fixed frame, a spring, and a dashpot, as shown in Fig. 2.2. In this model, the mass is supported from the frame by the spring, and the damping of the dynamic movement of the mass is described by the dashpot. By analyzing the displacement of the mass, the acceleration of the fixed frame can be solved in the following way.

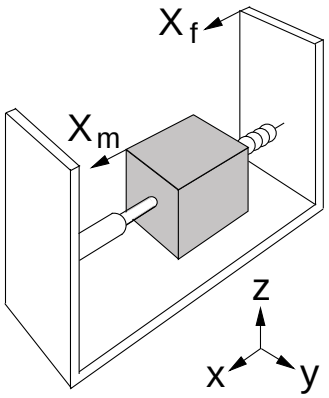

Figure 2.2: Accelerometer modeled with a mass, a frame, a spring, and a dashpot.

At the beginning, it is defined that the frame and the mass move only x-directionally and have separate absolute x-directional displacements X_f and X_m, respectively, as shown in Fig. 2.2. Furthermore, the relative distance between the mass and the frame is determined to be

$$\Delta x = X_f - X_m \,. \tag{2.1}$$

In the case, where the acceleration of the frame $\ddot{X}_f$ changes[3], there are two forces which balance the change of the distance Δx, namely the spring and damping forces. According to Hooke's law, the spring exerts the restoring spring force

$$F_s = k\Delta x \,, \tag{2.2}$$

[3]In this analysis the dots define how many times the corresponding variable is differentiated with respect to time.

where k is the spring constant. The damping of the dynamic movement of the mass is expected to be viscous and therefore it causes the restraining force

$$F_D = D\Delta\dot{x}\,, \tag{2.3}$$

where D is the damping factor and $\Delta\dot{x}$ is the velocity of the mass in respect to the frame.

By summing the above-mentioned forces and by using (2.1), the following force balance equation can be written to the mass

$$m\ddot{X}_m = m\left(\ddot{X}_f - \Delta\ddot{x}\right) = D\Delta\dot{x} + k\Delta x\,, \tag{2.4}$$

where m is the mass of the proof mass. By taking the Laplace transform from (2.4), the mechanical transfer function from the acceleration of the frame $\ddot{X}_f$ to the distance Δx can be written as

$$H(s) = \frac{\Delta x(s)}{\ddot{X}_f(s)} = \frac{1}{s^2 + \frac{D}{m}s + \frac{k}{m}}\,. \tag{2.5}$$

By comparing (2.5) to the transfer function of the second-order low-pass filter,

$$H(s) = \frac{1}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}\,, \tag{2.6}$$

it can be seen that the resonance frequency

$$\omega_0 = \sqrt{\frac{k}{m}}\,, \tag{2.7}$$

the quality factor

$$Q = \frac{\sqrt{mk}}{D}\,, \tag{2.8}$$

and the dc sensitivity

$$H(0) = \frac{m}{k} = \frac{1}{\omega_0^2}\,. \tag{2.9}$$

As in electrical devices, there are noise sources in mechanical devices. The mechanical noise of the accelerometer stems primarily from the Brownian motion of the gas molecules surrounding the proof mass and the losses caused by the proof mass suspension or anchors [13]. Brownian motion can be modeled as a thermal noise force, the noise density of which in $\mathrm{N}/\sqrt{\mathrm{Hz}}$ for any mechanical resistance R_m is

$$F_n = \sqrt{4k_BTR_m}\,, \tag{2.10}$$

where k_B is Boltzmann constant and T the absolute temperature [25]. For accelerometers, R_m=D, and the total noise equivalent acceleration (TNEA) in $(\mathrm{m/s^2})/\sqrt{\mathrm{Hz}}$ is [13]

$$TNEA = \frac{\sqrt{4k_BTD}}{m}\,. \tag{2.11}$$

According to the above functions, a high-accuracy accelerometer, in other words a mechanically highly sensitive and low-noise accelerometer, can be achieved with a large m. The sensitivity can also be increased by lowering k. However, according to (2.9), the higher the sensitivity is, the lower the resonance frequency is, and thus a slower time response is achieved. Furthermore, the damping of the step response is defined by Q. The optimal step response is obtained with a Q value of 0.5, which offers the fastest step response without overshoot or ringing [14]. In consequence, the parameters of the accelerometers have to be balanced to obtain the right accuracy and time response.

2.2 Electrical Model of a Capacitive Accelerometer

In a single capacitance accelerometer a proof mass and a fixed electrode, which is attached to the frame, form a capacitor, as shown in Fig. 2.3. The capacitance of this parallel-plate capacitor is

$$C_D = \frac{A\varepsilon_0\varepsilon_r}{d}\,, \tag{2.12}$$

where A is the overlapping plate area, ε_0 the permittivity of the vacuum, ε_r the relative permittivity of the insulator, and d the distance between the capacitor plates.

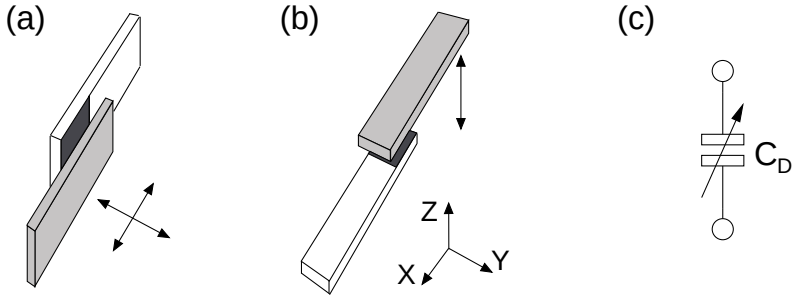

Figure 2.3: Capacitance comprising a fixed electrode and (a) a horizontally or (b) a vertically movable proof mass. (c) Electrical model for a single capacitance accelerometer.

Depending on the structure of the capacitive accelerometer, the proof mass usually moves horizontally or vertically relative to the fixed electrode, as illustrated in

Fig. 2.3(a) and (b), respectively. Therefore a mechanical displacement of the mass, caused by acceleration, changes the capacitance C_D, via the variation of d or A, by a magnitude of ΔC. Because of the structures of the capacitive accelerometers that are used, the analyses presented in this thesis are based on parallel-plate capacitors with variable d.

The larger the capacitive sensitivity $\Delta C/g$ of the capacitive accelerometer is relative to C_D, $g = 9.81\ m/s^2$, the higher the output signal of the front-end usually is. Similarly to the mechanical sensitivity given in (2.9), $\Delta C/g$ can be improved by increasing m and reducing k. It is worth noting that the factors that limit the capacitive sensitivity are not only a reasonable ω_0 and Q, but also the dimensions of the capacitive accelerometer. First, a large m typically means a large A. In some applications the capacitive accelerometer is integrated into the microchip with the interface electronics, and thus to minimize the die area a large A is not desirable. Second, the deflection of the mass is limited by d, and thus to prevent the collision of the mass with the fixed electrode, a margin has to be left. Moreover, the larger the maximum deflection of the mass is, the more non-linear the displacement-to-capacitance conversion is, as discussed in Section 3.1.

With a differential capacitive accelerometer, such as the one shown in Fig. 2.4, the output signal of the front-end can also be increased. In this kind of structure a vertically movable mass is between two fixed electrodes, and thus it can be modeled as a capacitive half-bridge, illustrated in Fig. 2.4(b). With the use of the parallel-plate model, the sensor capacitances can be written as

$$\begin{aligned} C_{DP} &= \frac{A\varepsilon_0\varepsilon_r}{d_0 - \Delta d} = C_0 \left(\frac{d_0}{d_0 - \Delta d} \right) , \\ C_{DN} &= \frac{A\varepsilon_0\varepsilon_r}{d_0 + \Delta d} = C_0 \left(\frac{d_0}{d_0 + \Delta d} \right) , \end{aligned} \tag{2.13}$$

where d_0 is the initial distance between the capacitor plates, Δd the change in the distance that is induced by acceleration, and C_0 the capacitance with $\Delta d = 0$[4]. It can be seen that under acceleration, $\Delta d \neq 0$, the capacitances C_{DP} and C_{DN} change in such a way that one capacitance increases, whereas the other decreases. With a proper front-end structure the information of both capacitors can be utilized, and therefore the output signal is larger than with a single capacitance accelerometer. Front-end structures for differential capacitive accelerometers and the linearization of the capacitive accelerometer are discussed in Chapter 3. All the accelerometers used in this thesis are based on differential capacitive accelerometers.

[4]In the analysis presented in this thesis, for the sake of simplicity, the tilting movement of the mass has not been taken into account.

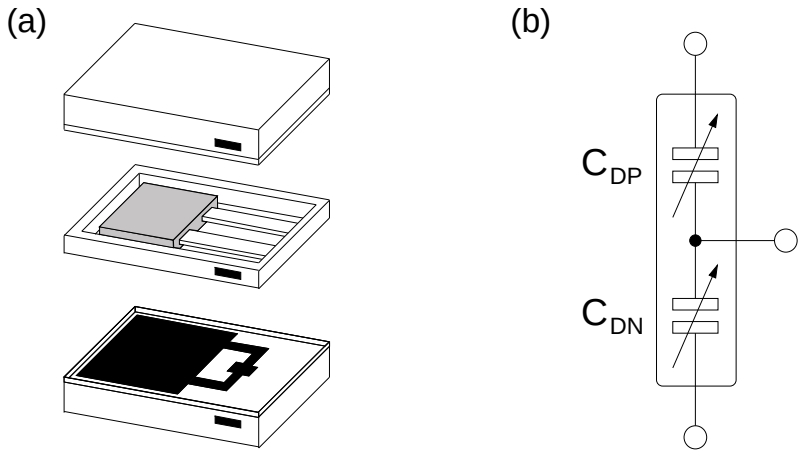

Figure 2.4: (a) Structure and (b) model of the differential capacitive accelerometer.

2.3 Micromachining Technologies

In the previous sections, methods to improve the properties of accelerometers by using proper structures with optimal device parameters were introduced. However, these improvements can be made only if they are feasible with the micromachining technology that is used.

Micromechanical structures, such as capacitive accelerometers, are implemented by using different micromachining technologies. Silicon has excellent mechanical properties, for example strength, elasticity, linearity, and stability [26], and hence it is a suitable material for micromechanical structures. The methods used in the micromachining of the silicon, such as etching and patterning, are similar to the manufacturing methods used in microelectronics. Generally, the micromachining technologies are divided into two categories, bulk and surface micromachining.

In bulk micromachining a micromechanical structure is realized by removing the material of the bulk of the silicon wafer. In practice, the removal is realized by etching processes, which are divided into wet and dry etching.

Wet etching is a chemical process in which the areas of the silicon wafer which are not protected by optical patterned layers, such as silicon dioxide (SiO_2), are removed by exploiting wet chemical etchants. Depending on the etchant that is used, the directionality of the etching is isotropic or anisotropic, omnidirectional or directional, respectively. Most of the wet-etching processes are isotropic [27]. Anisotropic wet etching is achieved by using etchants which etch in specified directions faster than in others; for example, an etchant based on potassium hydroxide (KOH) etches silicon for the (100) plane approximately 100 times faster than the (111) plane, and thus better-defined diagonal plane structures are achieved than with isotropic wet

etching, as can be seen from Figs. 2.5(a) and (b).

In contrast, dry etching does not utilize wet chemical etchants, but chemical, physical or physical/chemical techniques. In chemical techniques, the unprotected areas of the material are reacted with the reactive species of plasma that are diffused and absorbed on the surface. After the reaction, the volatile by-products desorb from the surface and diffuse into gas. The by-products are pumped out of the etching system. With this kind of plasma etching an isotropic etching result is achieved. More perpendicular sidewalls are usually attained by using physical dry etching methods such as ion milling, in which the surface of the material is bombarded vertically with chemically inert ions. This momentum transfer induces bond breakages and releases the surface material. The disadvantage of ion milling is that the speed of the etching, the etch rate, is almost independent of the material, and thus the protective layers are also etched. A dry etching method which combines both chemical and physical techniques is reactive ion etching (RIE). In RIE the wafer is bombarded with chemically reactive ions and the atoms of the surface are released. With RIE a perpendicular etching result are attained, as can be seen from Fig. 2.5(c).

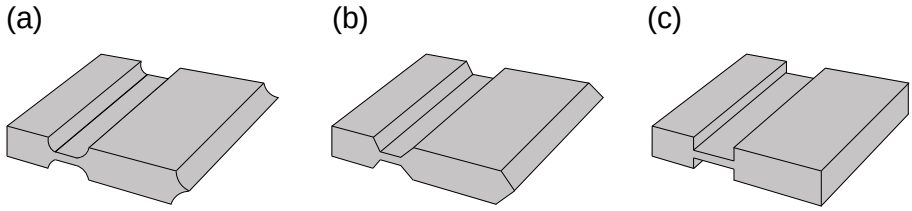

Figure 2.5: Bulk-micromachined silicon by (a) isotropic, (b) anisotropic wet etching, and (c) RIE.

To achieve precise dimensions, and thus the parameters determined for the accelerometers, the depth of the etching has to be controlled. A straightforward method is to adjust the etching time, but more accurate results are realized by using etch-stop techniques, such as doping-selective etching and electrochemical etch-stop in wet etching [27], or protective layers in dry etching.

In contrast to bulk micromachining, in surface micromachining micromechanical structures are implemented by sequentially depositing layers and removing selected parts of the layers on top of the wafer. Surface micromachining is commonly realized by a sacrificial layer technology, which utilizes two kinds of materials, sacrificial and structural layers. In practice, sacrificial and structural layers, such as SiO_2 and polycrystalline silicon (PolySi) layers, respectively, are alternately deposited and patterned on a wafer. At the end of the process the sacrificial layers are etched, for example with hydrofluoric acid (HF), and the remaining structural layers form a micromechanical structure, such as a capacitive accelerometer, in accordance with Fig. 2.6.

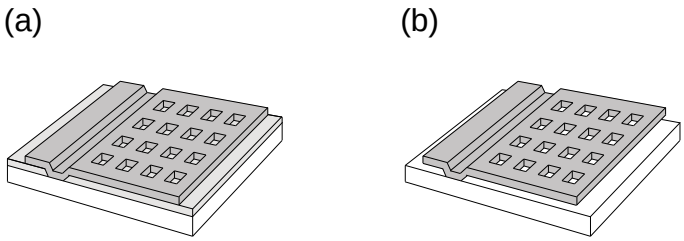

Figure 2.6: Surface-micromachined accelerometer (a) before and (b) after etch of the sacrificial layer.

Both bulk and surface micromachining have their advantages and disadvantages. Generally, the main advantage of bulk micromachining is the possibility of realizing thick and heavy structures and thus, according to (2.9) and (2.11), highly accurate accelerometers. On the other hand, the more complex bulk-micromachined structures, such as the accelerometer in Fig. 2.4, require an additional wafer bonding process, such as silicon fusion or anodic bonding. In the case of bonding glass and silicon there is a possibility of a large temperature coefficient as a result of thermal mismatch between the bonded wafers and poor long-term stability as a result of the slow relief of built-in mechanical stresses [5]. Contrary to bulk micromachining, in surface micromachining the same fabrication process can be utilized for the accelerometer and the microelectronic interface circuit, thus enabling compact and low-cost capacitive accelerometers to be fabricated. However, there are challenges in accommodating and optimizing thick vertical layers and high-temperature annealing, which are required in surface micromachining, with microelectronic processes which require a planar substrate. Commonly, one of the main challenges in surface micromachining is the permanent adhesion of the thin layers caused by the surface tension of the water when the structure is rinsed after the release etching. Efficient methods to prevent this adhesion are, for example, to use supercritical drying or thick layers. Nevertheless, the use of thin layers requires the fabrication of the release etch holes, which not only intensify the etching, but reduce damping, and therefore the mechanical noise of the accelerometer (2.11), as in the capacitive accelerometer shown in Fig. 2.6[5].

The division of bulk and surface micromachining is not complete. One interesting process, which has the features of both micromachining technologies, is silicon-on-insulator (SOI)[6]. By using different methods, such as the implantation of oxygen and fusion bonding of layers, thin layers of silicon and oxide can be processed upon a silicon substrate layer, as shown in Fig. 2.7(a)[7]. Implementations have been pre-

[5]The reduction of the damping is not valid if the mass moves horizontally.

[6]In the literature SOI is sometimes defined as bulk micromachining; in the opinion of the author SOI fulfills the characteristics of both techniques.

[7]Generally, the silicon and oxide layers above the silicon substrate are thinner than described in Fig. 2.7(a).

sented where the accelerometer is micromachined on the SOI wafer and the CMOS interface electronics are processed on the same wafer [28]. In addition, the mass of the accelerometer is increased by keeping some part of the silicon substrate layer, as shown in Fig. 2.7(b).

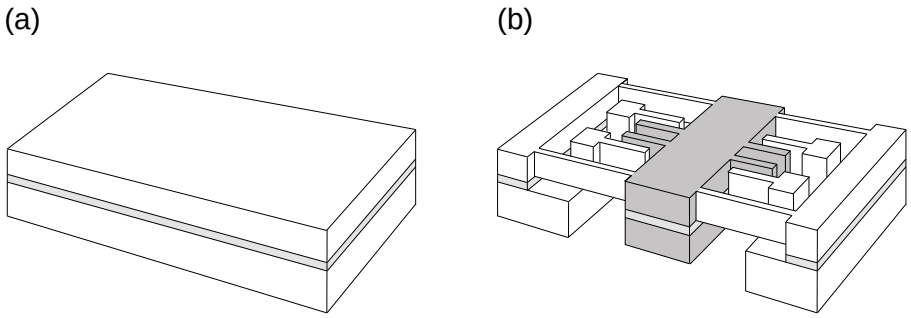

Figure 2.7: SOI (a) wafer and (b) capacitive accelerometer [29].

The purpose of the above introduction is to illustrate the properties of the micromachining methods of capacitive accelerometers. The area is broad and therefore the reader who is interested in the details of the techniques is recommended to familiarize themselves with works on the subject such as [1, 26, 27, 30].

2.4 Capacitive Three-Axis Accelerometers

The accelerometers discussed in the previous sections are capacitive single-axis accelerometers, which are capable of measuring acceleration only along one axis, whereas capacitive three-axis accelerometers can define the acceleration in all directions. In the following presentation the structures and operating principles of capacitive three-axis accelerometers are introduced.

There are several methods to implement a capacitive three-axis accelerometer. A straightforward implementation is to mount three capacitive single-axis accelerometers in a package. However, this implementation has disadvantages, such as increased packaging size and cost [31], as well as the difficulty in aligning the accelerometers exactly in three orthogonal directions [32]. Therefore sophisticated monolithic structures have been developed, which, in this thesis, are divided into three-mass, one-mass, four-mass, and other structures.

In three-mass structures, three single-axis accelerometers are integrated and accurately aligned through lithography as a monolithic capacitive three-axis accelerometer. Generally, in these devices, the horizontal directions, the x- and y-axes, are sensed by using horizontal comb finger structures like those shown in Fig. 2.8(a)

whereas the vertical direction, the z-axis, is sensed by a parallel plate structure, such as in Fig. 2.8(b). In the surface micromachined implementations of [33, 34], the comb finger structures form differential capacitive accelerometers in horizontal directions. The vertical direction is sensed by a single capacitance accelerometer and fixed reference capacitance. One reason for this may be that an additional electrode above the proof-mass requires a more complex fabrication process [5], such as in [35]. In the SOI implementation of [36] all directions are sensed with single capacitance accelerometers. In [37], by using a technology which combines bulk and surface micromachining, both the horizontal and vertical directions can be defined by differential capacitive accelerometers, as shown in Figs. 2.8(c) and (d).

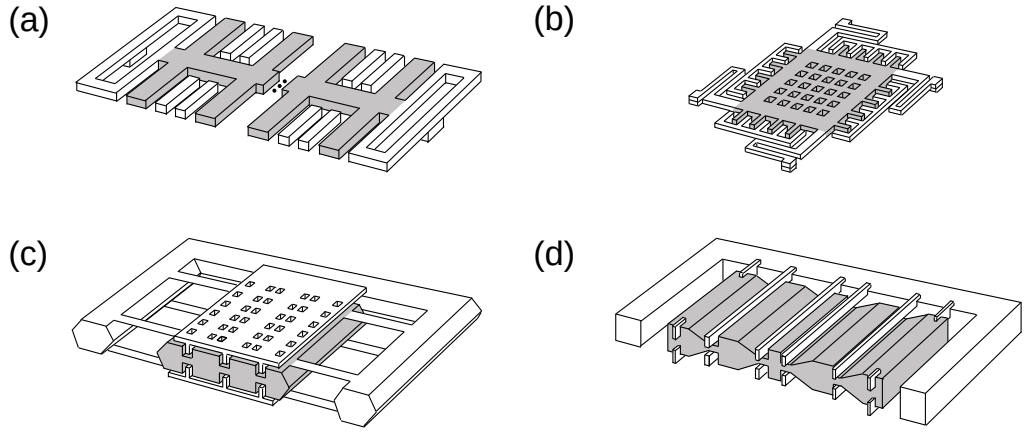

Figure 2.8: (a) A comb finger horizontal [38] and (b) a parallel plate vertical surface micromachined capacitive accelerometer [39]. A vertical (c) and horizontal (d) capacitive accelerometer fabricated with a combined surface and bulk micromachining technology [37].

In one-mass structures, capacitive accelerometers are composed of one movable mass and the fixed electrodes surrounding the mass. As a general rule, the one-mass capacitive three-axis accelerometers that have been published are bulk-micromachined, as in [32, 40, 41, 42], but there is also at least one surface-micromachined structure [43]. In the structures of [40] and [41] the mass and four electrodes form four single capacitance accelerometers, as can be seen from Figs. 2.9(a) and 2.10(a). In horizontal acceleration, the mass tilts and two of the capacitances decrease and the other two increase, whereas in vertical, z-directional, acceleration the mass shifts in parallel and all the capacitances decrease or increase, as shown in Fig. 2.9(b). The mass of [32] operates in the same way as those in the implementations of [40, 41], but there is a fifth electrode in the middle of the four electrodes and a reference capacitor beside the accelerometer, as illustrated in Fig. 2.10(b). The four single capacitance accelerometers are mounted in such a way that only the opposite capacitors increase and decrease in horizontal acceleration. In vertical acceleration all five capacitors change in parallel. Therefore the horizontal accelerations are detected from the

difference between the opposite capacitors and the vertical acceleration from the difference between the fifth capacitor and the reference capacitor. The operation of [42] is similar to [32], but there are five electrodes both under and above the mass, as shown in Fig. 2.10(c). Therefore all the directions can be detected with differential capacitive accelerometers. In the surface-micromachined implementation of [43], shown in Fig. 2.10(d), under horizontal acceleration, the mass moves in parallel and these directions are detected by differential in-plane capacitive accelerometers. The vertical acceleration, on the other hand, is detected by a single capacitance accelerometer and a fixed reference capacitor.

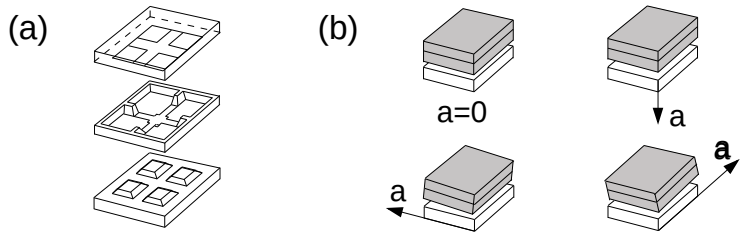

Figure 2.9: (a) One-mass capacitive three-axis bulk-micromachined accelerometer [40], and (b) its operating principles in different circumstances of acceleration.

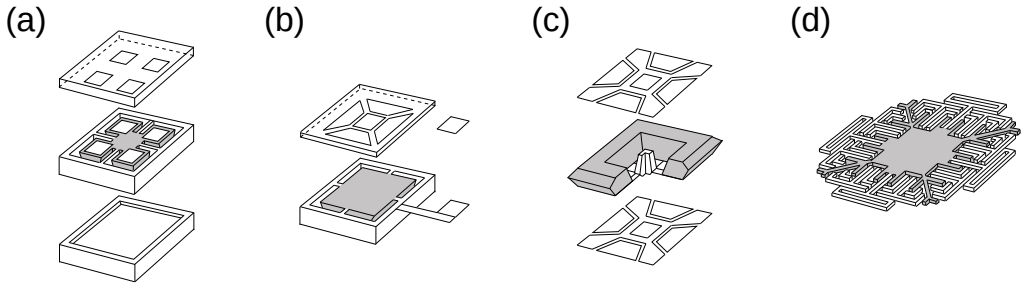

Figure 2.10: One-mass capacitive three-axis bulk-micromachined (a) [41], (b) [32], (c) [42], and surface-micromachined (d) [43] accelerometers.

In four-mass capacitive three-axis accelerometers, the accelerations are defined from the displacements of the four individual proof masses. The implementations of [44, 45] have been fabricated by using SOI wafers and deep reactive ion etching (DRIE). The accelerometer of [44] consists of four triangular proof masses which have their own fixed electrodes below and above them. Therefore the accelerometer consists of four differential capacitive accelerometers. Because the center of gravity of each mass is below the supporting springs, under horizontal acceleration, as depicted in Fig. 2.11(a), the opposite masses are rotating in reversed directions, whereas the other two masses hold still. Under vertical acceleration, however, all four masses are rotating in the same direction, as shown in Fig. 2.11(b). The operating principle of [45] is very similar to that of [44], but the four masses are

square-shaped, as illustrated in Fig. 2.11(c), and the electrodes are only above the masses. The accelerometer is not compact compared to the later implementation of the main author [46, 47], where the masses are replaced more closely, as can be seen from Fig. 2.11(d). The operating principle is similar to that in the previous structure, but in this implementation, the displacements of the masses are achieved by using slanted beams and the fabrication is realized by wet-etching a silicon wafer.

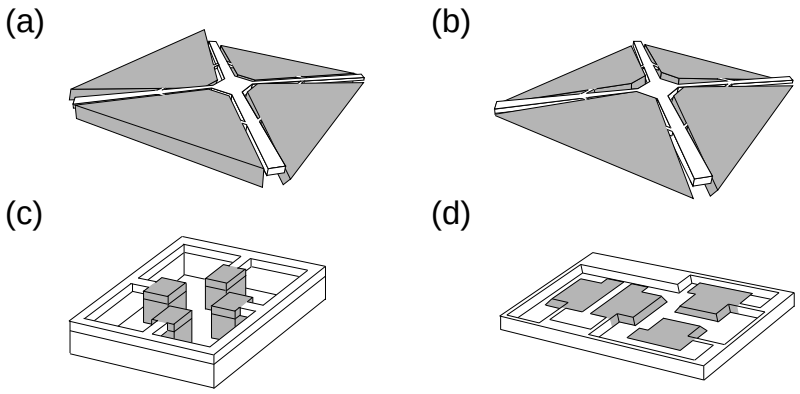

Figure 2.11: The four-mass capacitive three-axis accelerometer of [44] under (a) horizontal and (b) vertical acceleration, and implementations (c) [45] and (d) [46, 47].

Some other structures of capacitive three-axis accelerometers which are not fabricated by traditional micromachining are cubic and CMOS-MEMS devices. In cubic structures, three differential capacitive accelerometers are formed by a mass which is inside the six electrode faces, as shown in Fig. 2.12(a). In the implementation of [48], a cubic three-axis accelerometer is fabricated by micromachining a silicon wafer which is folded in the end. The materials that were used are non-standard; for example, the mass is supported from the electrodes by polydimethylsiloxane springs.

CMOS-MEMS accelerometers are implemented by micromachining CMOS wafers. The metal layers work as etching masks and together with vias they form the masses and electrodes of a capacitive comb finger accelerometer. As was noticed from the aforementioned structures, the differential capacitive accelerometers in vertical structures are difficult to implement if there is no layer above the mass. In CMOS-MEMS structures, the vertical motions of the comb fingers and frequent connection alternatives make possible differential accelerometers in the z-direction, as can be seen from Fig. 2.12(b). In the implementation of [31], the z-direction was implemented by means of an imbalanced proof mass, as shown in Fig. 2.12(c).

According to the above introduction, each of the capacitive three-axis accelerometers consists of single capacitance and/or differential capacitive accelerometers. The structure of the accelerometer defines the topology of the front-ends which are stud-

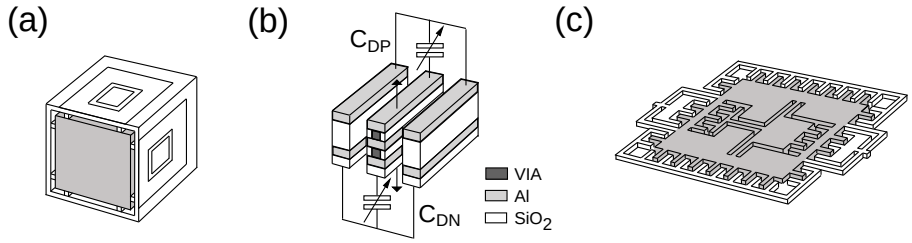

Figure 2.12: (a) Cubic device [48], (b) vertical CMOS-MEMS differential capacitive accelerometer [49], and (c) three-axis CMOS-MEMS capacitive accelerometer [31].

ied for capacitive single-axis and three-axis accelerometers in the following chapters 3 and 4, respectively. In the publications of this thesis, a four-mass structure which is based on the implementation of [44] was used in [P1, P2, P3] and a three-mass structure in [P4, P5, P6].

2.5 Discussion

In this chapter, background information on capacitive accelerometers was discussed. At the beginning, the mechanical operation of the accelerometer was studied. It was noticed that by using large-mass and small-spring constant accelerometers both high sensitivity and low mechanical noise are achieved. However, in the optimization of these parameters, the resonance frequency and quality factor have to be taken into account in order to achieve a sufficient time response.

After the mechanical study, the capacitive accelerometer was modeled electrically. Depending on the structure of the accelerometer, the capacitive accelerometer was modeled with one or two parallel-plate capacitors, which represent single capacitance or differential capacitive accelerometers, respectively. All the capacitive accelerometers used in this thesis are based on the differential structures.

After the modeling, micromachining technologies were introduced. The technologies were divided into surface and bulk micromachining methods. Depending on the method used different mechanical parameters are easier to implement; for example, with bulk micromachining a large mass is easier to achieve than with surface micromachining. On the other hand, with surface micromachining both the electronics and the accelerometer can be integrated on the same chip.

The foundation achieved from the previous mechanical and electrical modeling, as well as the micromachining technologies, made it possible to understand the different implementations of capacitive three-axis accelerometers. The structures and oper-

ating principles of the capacitive three-axis accelerometers that have been published were discussed at the end of the chapter. This way, the implementations of the front-ends of the capacitive three-axis accelerometers, discussed in Chapter 4, are easier to understand. In the implementations of this thesis the three- and four-mass capacitive three-axis accelerometers are used.

In the following Chapter 3, the fundamentals of the front-end for capacitive single-axis accelerometers are introduced.

3 Front-End Circuits for Capacitive Accelerometers

As mentioned in Section 1.2, the front-end is the part of the interface which converts the capacitive acceleration information into a convenient form for an electrical application, such as an analog or digital signal. In addition, the front-end maximizes the linear range of the capacitive accelerometer. Usually, the non-linearity is caused by the displacement-to-capacitance conversion and the electrostatic forces. The latter are a consequence of the biasing, whereas the former results from the structure of the capacitive accelerometer. The electrostatic forces cause not only non-linearity, but in the worst case a phenomenon called pull-in, in which the mass and the fixed electrode snap together.

The purpose of this chapter is to introduce the front-end topologies which are suitable for differential capacitive accelerometers. Before the introduction, the effects of displacement-to-capacitance conversion and the electrostatic forces are discussed. The actual presentation of the front-ends is concentrated on discrete-time front-ends, because the topologies of the thesis are based on switched-capacitor (SC) circuits. The topologies that are discussed are divided according to their abilities to reduce the effects of the electrostatic forces. Continuous-time front-ends are not omitted entirely, but some topologies are covered briefly before the chapter concludes with discussion.

3.1 Displacement-to-Capacitance Conversion

The effects of displacement-to-capacitance conversion can be seen, for example, by modeling a single capacitance accelerometer as a parallel-plate capacitor,

$$C_D = \frac{A\varepsilon_0\varepsilon_r}{d_0 - \Delta d}\,. \tag{3.1}$$

In (3.1) term Δd is in the denominator, and thus C_D is not directly proportional to Δd. The linear displacement-to-capacitance conversion can be achieved with a parallel-plate structure, in which $\Delta d \ll d_0$, when the following approximation

$$C_D \approx \frac{A\varepsilon_0\varepsilon_r}{d_0}\left(1 + \frac{\Delta d}{d_0}\right) = C_0 + \Delta C \tag{3.2}$$

is valid[8]. Furthermore, there are front-end topologies which linearize displacement-to-capacitance conversion, even with larger values of Δd. These structures are discussed in Section 3.3.2.

[8]It is worth noting that in the structure of Fig. 2.3(a), as the mass moves horizontally in the x-direction, the change of A is linearly proportional to the movement of the mass, and therefore, the displacement-to-capacitance conversion is also linear.

3.2 Electrostatic Forces

In order to convert the capacitive acceleration information of the capacitor into an analog or digital signal, the capacitor has to be biased. Generally, the capacitor is biased with a constant voltage or charge [50]. Regardless of the biasing method used, the attractive electrostatic force is engaged between the plates of the capacitor. Next, the magnitudes of these electrostatic forces are derived for the constant voltage and charge biasing methods, respectively.

The magnitude of the electrostatic force of a capacitor which is biased with a constant voltage can be solved by using the following approach, as in [14]. In practice, the change in the total energy of the system E_{tot}, including the capacitor and the constant voltage source, is analyzed, because the electrostatic force is defined as

$$F_{es} = -\frac{\mathrm{d}E_{tot}}{\mathrm{d}\Delta d}\,. \tag{3.3}$$

The energy of the capacitor is

$$E_C = \frac{1}{2}CV^2 = \frac{1}{2}Q_C V\,, \tag{3.4}$$

where C is the capacitance of the capacitor, V the voltage of the constant source, and Q_C the charge of the capacitor, which is

$$Q_C = CV\,. \tag{3.5}$$

As V is constant, the variation of C causes the change in Q_C, and thus the change of E_C is

$$\mathrm{d}E_C = \frac{1}{2}V^2\mathrm{d}C\,. \tag{3.6}$$

In proportion, the energy stored in the constant voltage source is

$$E_V = Q_V V\,, \tag{3.7}$$

where Q_V is the charge of the voltage source. Because the system is closed, it can be written

$$\mathrm{d}Q_C = -\mathrm{d}Q_V\,. \tag{3.8}$$

Accordingly, the change of E_V is

$$\mathrm{d}E_V = -V^2\mathrm{d}C\,. \tag{3.9}$$

Since $E_{tot} = E_C + E_V$, the electrostatic force can be written as

$$F_{es} = -\left(\frac{\mathrm{d}E_C}{\mathrm{d}\Delta d} + \frac{\mathrm{d}E_V}{\mathrm{d}\Delta d}\right) = \frac{1}{2}\frac{\mathrm{d}C}{\mathrm{d}\Delta d}V^2\,. \tag{3.10}$$

By substituting (3.1) into (3.10), the electrostatic force of the single capacitance accelerometer is achieved:

$$F_{es,C_D} = \frac{1}{2}\frac{A\varepsilon_0\varepsilon_r V^2}{(d_0 - \Delta d)^2} = \frac{1}{2}\frac{Q_D^2}{A\varepsilon_0\varepsilon_r}\,, \tag{3.11}$$

where Q_D is the charge of the capacitor C_D.

In constant charge biasing, the charge stored in the capacitor, Q_C, is constant and according to (3.4) and (3.5) the total energy of the system is

$$E_{tot} = \frac{1}{2}\frac{Q_C^2}{C}\,. \tag{3.12}$$

Therefore the electrostatic force of the single capacitance accelerometer is achieved by substituting (3.1) into (3.12) and using (3.3), thus resulting in

$$F_{es,C_D} = \frac{1}{2}\frac{Q_D^2}{A\varepsilon_0\varepsilon_r}\,, \tag{3.13}$$

where Q_D is the constant charge stored in the capacitor C_D.

By comparing (3.11) and (3.13), it can be seen that the electrostatic force in constant voltage biasing is dependent on Δd, whereas in constant charge biasing it is constant. Consequently, in constant charge biasing the offset resulting from the electrostatic forces is also constant, whereas constant voltage biasing causes a signal-dependent offset, which causes non-linearity. The offset can be removed by using a differential capacitive accelerometer, in which case there are two opposite forces which balance each other, but in constant voltage biasing the non-linearity remains[9]. Even if the offset and the nonlinearity properties are better with constant charge biasing than with constant voltage biasing, it is difficult to maintain a constant charge in the capacitor as a result of leak resistors [50]. One approach to implementing constant charge biasing is to refresh the charge in the capacitor, as was done in [51].

3.2.1 Effects of the Electrostatic Forces

As mentioned in Section 2.2, all the accelerometers used in this thesis are based on differential capacitive accelerometers. Furthermore, the operating frequencies of the accelerometer are slow, starting from dc. Therefore, the effects of the electrostatic forces are analyzed, as in [18], for a differential capacitive accelerometer in static acceleration circumstances.

[9]It is worth noting that the electrostatic forces do not have effect on the structure of Fig. 2.3(a); if it is differential, a fixed electrode is also on the right-hand side of the mass, and the mass is in the middle of these fixed electrodes. As the mass moves horizontally in the x-direction, the electrostatic forces of the sensor capacitors are equal, even if constant voltage biasing is used.

In static acceleration circumstances, the relative distance between the mass and the frame is constant, and thus $\Delta\dot{x} = \Delta\ddot{x} = 0$, as well as $\ddot{X}_m = \ddot{X}_f$. According to (2.4), two forces are acting on the mass, namely a force induced by the static acceleration $m\ddot{X}_m$ and the restoring spring force $k\Delta x$. In addition, as the capacitors C_{DP} and C_{DN} are biased with the constant voltage V_B, the electrostatic forces are engaged. By converting (2.4) for capacitive accelerometers, $\Delta x = \Delta d$, and by combining (2.13) and (3.10), the following force balance equation can be written to the mass

$$ma = k\Delta d - \frac{1}{2}A\varepsilon_0\varepsilon_r V_B^2 \left(\frac{1}{(d_0 - \Delta d)^2} - \frac{1}{(d_0 + \Delta d)^2} \right) , \tag{3.14}$$

where $\ddot{X}_m$ is replaced with acceleration a, for the sake of simplicity.

By reorganizing the terms, the following fifth-order polynomial,

$$k\Delta d^5 - ma\Delta d^4 - 2kd_0^2\Delta d^3 + 2mad_0^2\Delta d^2 + \left(kd_0^4 - 2\varepsilon_0\varepsilon_r A V_B^2 d_0\right)\Delta d - mad_0^4 = 0\,, \tag{3.15}$$

is achieved for Δd. To illustrate the effects of the electrostatic forces, the polynomial is solved numerically by using the practical parameters of the capacitive accelerometer, shown in Table 3.1. The solutions for three different bias voltages are plotted in Fig. 3.1.

Table 3.1: Parameters of a capacitive accelerometer.

ϵ_r	m	k	A	d_0
1	1 mg	5 N/m	1 mm^2	5 μm

The effects of the electrostatic forces can be seen from Fig. 3.1. In the case of a zero biasing voltage, Δd is linearly proportional to a. When V_B is increased to 1 V, the electrostatic forces cause non-linearity, and the mass touches either one of the electrodes if a is more than approximately ± 16 m/s^2. This electrostatic effect is known as pull-in. As the V_B is increased to 4 V, not only are distortion and pull-in detected, but a significant change in the slope can also be seen. The explanation for this effect is that the electrostatic forces reduce k by the factor k_{es}, which is called the electrostatic spring constant. According to the analysis of Section 3.2, the non-linearity is expected, but the electrostatic spring constant and pull-in need further surveying.

Electrostatic Spring Constant

To solve the electrostatic spring constant, the electrostatic forces of the capacitors

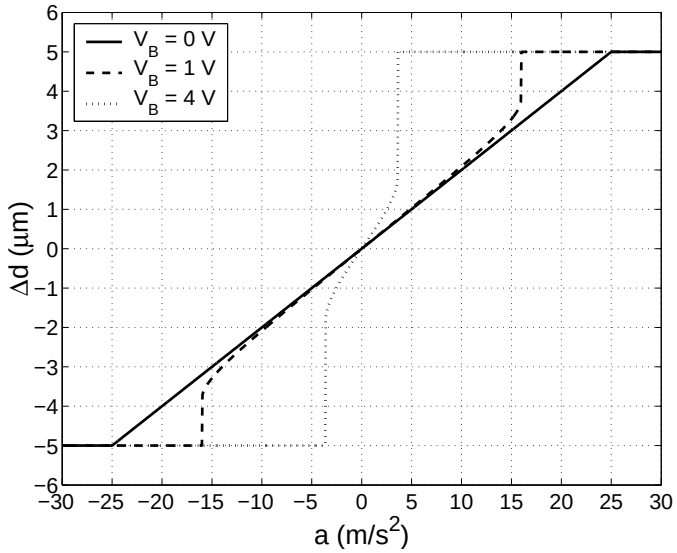

Figure 3.1: Solution of (3.15) for three different values of V_B.

C_{DP} and C_{DN} are reformulated, by using the Taylor series, in the following form

$$\begin{aligned} F_{es,C_{DP}} &= \frac{1}{2}\frac{A\varepsilon_0\varepsilon_r V_B^2}{(d_0-\Delta d)^2} \approx \frac{1}{2}\frac{A\varepsilon_0\varepsilon_r V_B^2}{d_0^2} + \frac{A\varepsilon_0\varepsilon_r V_B^2}{d_0^3}\Delta d\,, \\ F_{es,C_{DN}} &= \frac{1}{2}\frac{A\varepsilon_0\varepsilon_r V_B^2}{(d_0+\Delta d)^2} \approx \frac{1}{2}\frac{A\varepsilon_0\varepsilon_r V_B^2}{d_0^2} - \frac{A\varepsilon_0\varepsilon_r V_B^2}{d_0^3}\Delta d\,. \end{aligned} \tag{3.16}$$

In this approximation, two first terms of the series are used, and it is valid if $\Delta d \ll d_0$. Therefore, the approximation is appropriate for the study of the slope in the vicinity of the origin. By substituting (3.16) into (3.14), the force balance function can be written as

$$ma = \left(k - \frac{2A\varepsilon_0\varepsilon_r V_B^2}{d_0^3}\right)\Delta d\,. \tag{3.17}$$

Now the effective spring constant can be defined as

$$k_{eff} = k - \frac{2A\varepsilon_0\varepsilon_r V_B^2}{d_0^3}\,. \tag{3.18}$$

It can be seen that in the presence of the electrostatic forces, the effective spring constant is reduced by the term

$$k_{es} = \frac{2A\varepsilon_0\varepsilon_r V_B^2}{d_0^3}\,, \tag{3.19}$$

which is the electrostatic spring constant. Even if the input range of the accelerometer is narrowed, the electrostatic spring constant can be utilized, for example, to control the sensitivity by adjusting the biasing voltage or to increase the sensitivity of the rigid accelerometer.

Pull-In

The proper solutions for (3.14) are real and $\Delta d \leq d_0$. From these solutions, unstable are those in which the small deflection causes the snapping of the mass in the fixed electrode, in other words the pull-in effect. If the stiffness of the system is obtained, the stability of the solutions can be studied [14]. The stiffness reveals the operation of the system in the vicinity of the solutions. The negative stiffness values show that the system is stabile, even if the mass is deflected slightly from the equilibrium point, whereas the solutions with positive stiffness values are unstable and the pull-in effect occurs. In order to solve the pull-in points, the solutions of the stiffness are analyzed.

According to (3.14) the total force F_{tot} affecting the mass, in the coordinate system defined by the frame, is

$$F_{tot} = ma - k\Delta d + \frac{1}{2}A\varepsilon_0\varepsilon_r V_B^2 \left(\frac{1}{(d_0 - \Delta d)^2} - \frac{1}{(d_0 + \Delta d)^2} \right) . \tag{3.20}$$

By differentiating F_{tot} with respect to Δd , the stiffness of the mass is achieved

$$\frac{\partial F_{tot}}{\partial \Delta d} = -k + A\varepsilon_0\varepsilon_r V_B^2 \left(\frac{1}{(d_0 - \Delta d)^3} + \frac{1}{(d_0 + \Delta d)^3} \right) . \tag{3.21}$$

As the roots of (3.21) define the pull-in points, it can be solved that the biasing voltage causing the pull-in, the pull-in voltage, is

$$V_B = \sqrt{\frac{k}{A\varepsilon_0\varepsilon_r} \left(\frac{1}{(d_0 - \Delta d)^3} + \frac{1}{(d_0 + \Delta d)^3} \right)^{-1}} . \tag{3.22}$$

Therefore, by substituting different values of Δd into (3.22), the maximum allowed biasing voltages for the given displacements of the mass can be defined. Fig. 3.2 shows the pull-in voltages for the capacitive accelerometer shown in Table 3.1.

From Fig. 3.2 it can be seen that the displacements are in line with the results shown in Fig. 3.1. In addition, it can be seen that the absolute maximum biasing voltage is the case where Δd is zero, when (3.22) can be written as

$$V_{B,max} = \sqrt{\frac{kd_0^3}{2A\varepsilon_0\varepsilon_r}} . \tag{3.23}$$

To convert the maximum biasing voltages of Fig. 3.2 to be a function of acceleration, first a is solved from (3.14)

$$a = \frac{1}{m} \left[k\Delta d - \frac{1}{2}A\varepsilon_0\varepsilon_r V_B^2 \left(\frac{1}{(d_0 - \Delta d)^2} - \frac{1}{(d_0 + \Delta d)^2} \right) \right] . \tag{3.24}$$

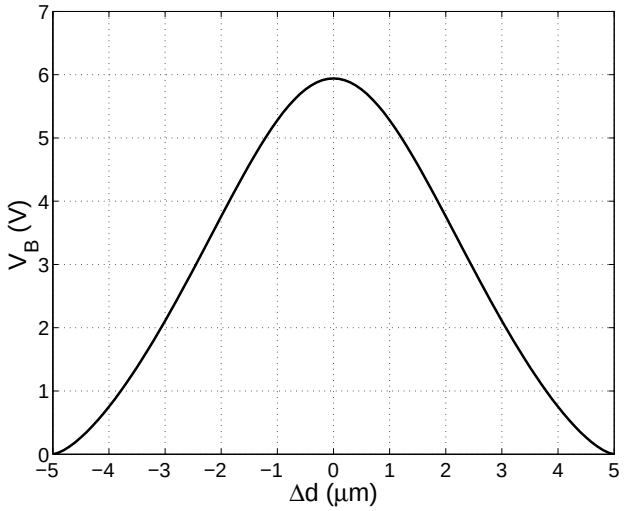

Figure 3.2: Maximum allowed biasing voltages as a function of the displacement of the mass.

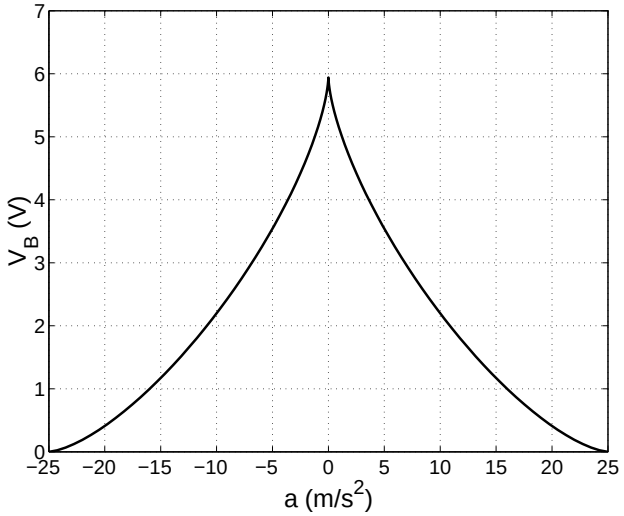

Figure 3.3: Maximum allowed biasing voltages as a function of acceleration.

Then, by substituting the points of the curve of Fig. 3.2 into (3.24), Fig. 3.3 is achieved. By comparing Figs. 3.1 and 3.3, it can be seen that the maximum accelerations are consistent with the results of the biasing voltages that are used.

Generally, it is realistic to design the biasing voltage and the parameters of the capacitive accelerometer in such a way that a margin is left for greater displacements than the maximum acceleration requires. Moreover, the front-end contributes to the effects of the electrostatic forces. In the following section, the discrete-time front-end topologies are divided according to their ability to reduce the effects of the electrostatic forces.

3.3 Discrete-Time Front-Ends

In discrete-time front-ends, the acceleration information is sampled. The sampling causes the folding of noise into the frequencies from dc to half of the sampling frequency, which is a disadvantage compared to continuous-time front-ends. However, discrete-time front-ends are implemented with SC circuits, which typically consist of capacitors, switches, and operational amplifiers. Therefore, including a capacitive accelerometer in the SC topology is straightforward and thus simple low-power front-ends can be implemented. Furthermore, some of the SC front-end topologies take into account the effects of displacement-to-capacitance conversion and the electrostatic forces. The following SC front-end topologies for differential capacitive accelerometers are divided, according to their abilities to reduce the effects of the electrostatic forces, into these categories: mechanical open-loop, mechanical open-loop charge-balancing, and mechanical closed-loop front-ends[10].

3.3.1 Mechanical Open-Loop Front-Ends

In mechanical open-loop front-ends, the mass can deflect freely and the structures do not take the electrostatic forces into account. Therefore the adjustment of the parameters of the accelerometer and the biasing voltage are the methods to ensure the proper operation of the accelerometer in the presence of the electrostatic forces.

SC Voltage Amplifier

A simple mechanical open-loop discrete-time front-end is shown in Fig. 3.4(a). In this front-end a differential capacitive accelerometer is connected to an SC voltage amplifier. The operating principle of the front-end is based on the charging of the

[10]For the sake of simplicity, in this thesis 'mechanical open-loop' and 'open-loop' front-end are synonyms, as are 'mechanical closed-loop' and 'closed-loop' front-ends.

capacitors and the transferring of the charges. To understand the operation of the front-end of Fig 3.4(a), the charge transitions are explained.

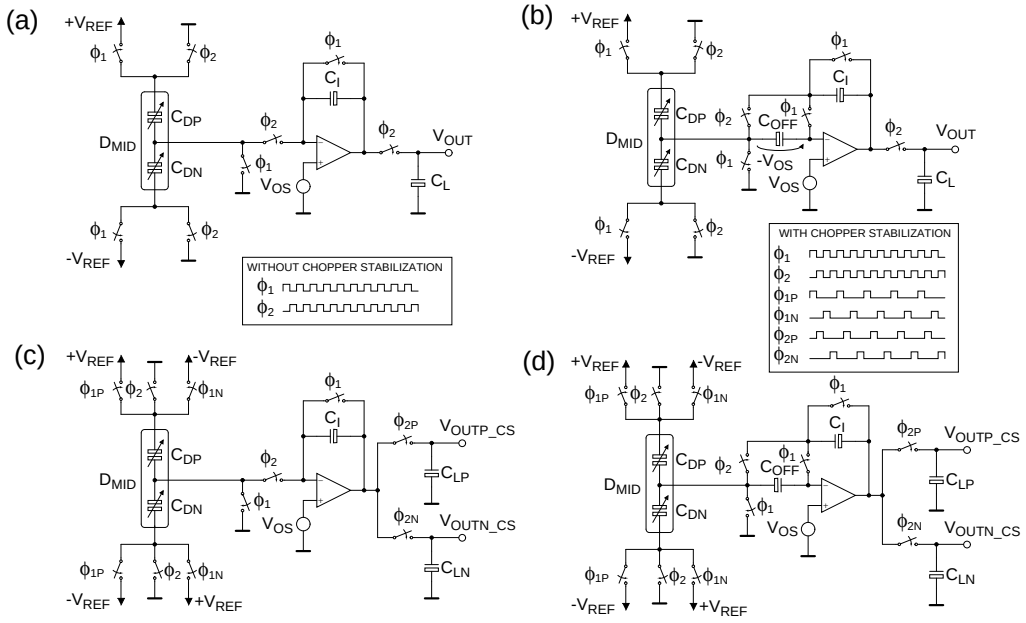

Figure 3.4: SC voltage amplifier front-end: (a) without CDS and CS; (b) with CDS; (c) with CS, and (d) with CDS and CS.

As can be seen from Fig. 3.4(a), the switches of the front-end are controlled by alternately changing clock phases ϕ_1 and ϕ_2. To prevent the loss of the charge, during the transitions, the clock phases have to be non-overlapping. In phase ϕ_1 the sensor capacitors C_{DP} and C_{DN} are charged against the reference voltages, $V_{REF} = |+V_{REF}| = |-V_{REF}|$, and ground, and the integration capacitor C_I is discharged. In phase ϕ_2, the sensor capacitors are discharged. In the node D_{MID}, the input current of the amplifier is zero, and hence the charge is transferred in the top plate of C_I. The operational amplifier loads the same amount of charge, but opposite in sign, in the bottom plate of C_I. Therefore the output voltage of the amplifier is

$$V_{OUT} = \frac{C_{DP} - C_{DN}}{C_I} V_{REF} \,. \tag{3.25}$$

The same voltage is also loaded into the capacitor C_L and the value is stored until the next phase ϕ_2. This continuous-amplitude and discrete-time voltage signal can be converted into a digital signal by using an ADC. In practice, the output of the operational amplifier could be directly connected to the sampling capacitor of the ADC, making the structure more compact.

The SC voltage amplifier is suitable for low-power applications, because it includes only one operational amplifier. However, in low-frequency applications a disadvantage is the sensitivity to the offset and the $1/f$ noise of the amplifier. The sensitivity

can be analyzed by connecting a voltage source V_{OS} to the input of the operational amplifier, as shown in Fig. 3.4(a). The offset voltage changes the amount of the charges that are transferred and the output voltage can be defined by using the previous method, as

$$V_{OUT} = \frac{C_{DP} - C_{DN}}{C_I} V_{REF} + \left(\frac{C_{DP} + C_{DN}}{C_I} + 1 \right) V_{OS} \,. \tag{3.26}$$

Generally, the offset and 1/f noise can be reduced by using correlated double sampling (CDS) or/and chopper stabilization (CS). Correlated double sampling reduces the low-frequency noise by high-pass filtering, whereas chopper stabilization translates it to an out-of-band frequency [52].

Correlated double sampling is implemented by adding an error storage capacitor C_{OFF} and a switch, as can be seen from Fig. 3.4(b). Now, in phase ϕ_1, a voltage $-V_{OS}$ is stored over C_{OFF}. In phase ϕ_2, the top plate of C_{OFF} is connected to the input of the operational amplifier, and the charge and the voltage V_{OS} remain constant during the clock phase. In consequence, the voltage of D_{MID} is zero, $-V_{OS} + V_{OS} = 0$, and the offset voltage does not affect the output voltage of the front-end and it is equal to (3.25). The elimination of the noise of V_{OS} decreases as the frequency increases, because the value of the stored error in phase ϕ_1 is less equivalent with the new value in phase ϕ_2. This explains the high-pass filtering of the noise.

In chopper stabilization, the sensor capacitors C_{DP} and C_{DN} are biased with non-inverted and inverted reference voltages in turn, as can be seen from Fig. 3.4(c). The output voltages of the outputs are

$$V_{OUTP\_CS} = V_{SIG} + V_{OFF} \,, \tag{3.27}$$

$$V_{OUTN\_CS} = -V_{SIG} + V_{OFF} \,, \tag{3.28}$$

where

$$V_{SIG} = \frac{C_{DP} - C_{DN}}{C_I} V_{REF} \,, \tag{3.29}$$

$$V_{OFF} = \left(\frac{C_{DP} + C_{DN}}{C_I} + 1 \right) V_{OS} \,. \tag{3.30}$$

In practice, the signal voltage V_{SIG} is modulated with the sampling frequency f_s whereas the offset voltage V_{OFF} is not modulated, as shown in Fig. 3.5. The demodulation of V_{SIG} can be implemented, for example, from the digital output values by taking the difference between the outputs, or by multiplying every second sample by -1, as shown in Fig. 3.5(a) and (b), respectively. In the first method V_{SIG} is doubled, V_{OFF} is reduced, and the sampling frequency is halved. In the latter method, the signal amplitude and the sampling frequency do not change. However, a low-pass filter has to be used to filter V_{OFF} from half of the sampling frequency.

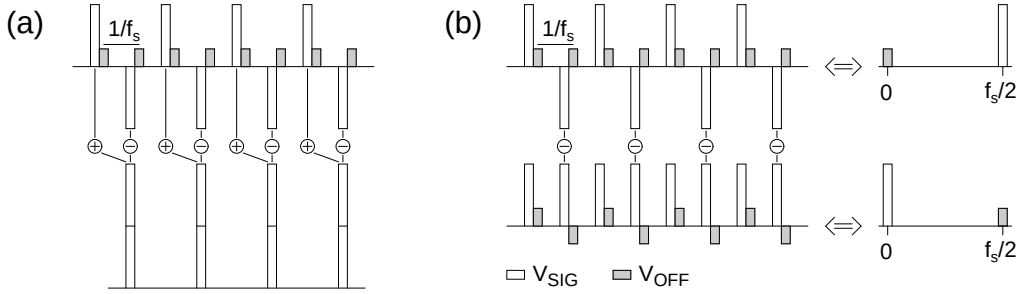

Figure 3.5: Demodulation with (a) taking the difference between the sequential samples or (b) multiplying every second sample by -1.

Correlated double sampling and chopper stabilization are effective methods for reducing the low-frequency noise, and are not mutually exclusive, as can be seen from the front-end shown in Fig. 3.4(d). However, correlated double sampling is a discrete-time method, unlike chopper stabilization, and thus suffers from the folding of thermal noise in the frequencies from dc to half of the sampling frequency. Generally, in the discrete-time circuits, if the sampling frequency is increased the noise is folded to a wider bandwidth, and thus the noise floor is lower. If the sampling frequency is doubled, the noise floor is reduced by approximately 3 dB; however, this is at the expense of increased power dissipation of the front-end, which is because of the fact that the operational amplifiers have to operate faster.

$\Delta\Sigma$ Converter

An SC topology which utilizes a high sampling rate is the $\Delta\Sigma$ converter. By adding a differential capacitive accelerometer at the input of the second-order $\Delta\Sigma$ converter, as shown in Fig. 3.6, the capacitive acceleration information can be converted directly into the digital domain.

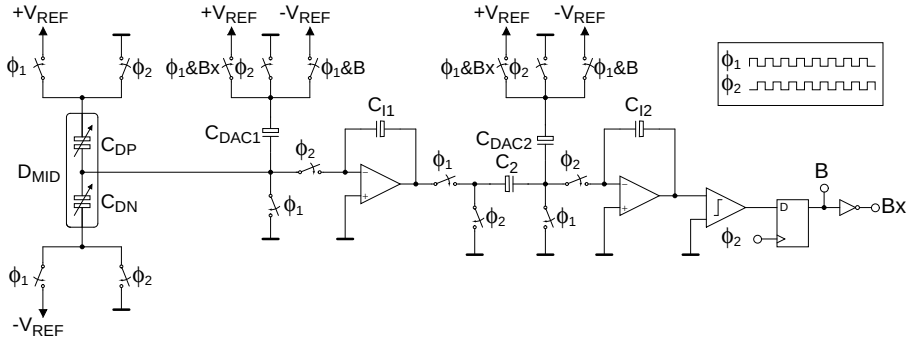

Figure 3.6: $\Delta\Sigma$ converter.

The operation of the $\Delta\Sigma$ converter can be understood by analyzing the charges fed into the first integrator. The average charge transferred into the first integrator has to be zero; otherwise, the output of the $\Delta\Sigma$ converter is not balanced. Therefore, by using Fig. 3.7, the equation for the average charge, transferred from the digital-to-analog converter (DAC) capacitor C_{DAC1} and the sensor capacitors C_{DP} and C_{DN} to the node D_{MID}, can be written as,

$$-C_{DP}V_{REF} + C_{DN}V_{REF} - C_{DAC1}V_{REF}(1-\overline{B}) + C_{DAC1}V_{REF}\overline{B} = 0\,, \qquad (3.31)$$

where $\overline{B}$ is the bit average of the one-bit output and it can be solved to be

$$\overline{B} = \frac{1}{2}\frac{C_{DP} - C_{DN}}{C_{DAC1}} + \frac{1}{2}\,. \qquad (3.32)$$

Therefore, the output of the $\Delta\Sigma$ converter is uniform to the SC amplifier (3.25), but the output signal is independent of V_{REF}. Even if V_{REF} does not influence $\overline{B}$, it affects the signal charge. In practice, the smaller the V_{REF} is, the smaller signal charge generated by $C_{DP} - C_{DN}$ is, and thus smaller the achieved signal-to-noise ratio (SNR) is.

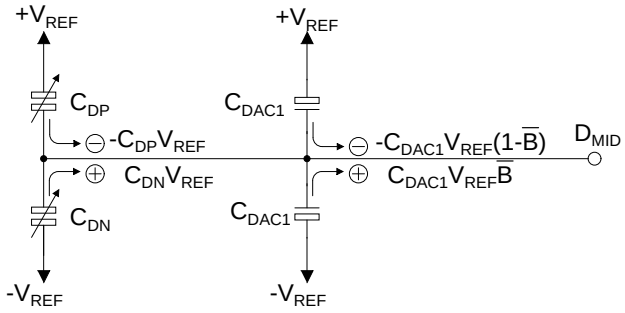

Figure 3.7: The average charges transferred in the first integrator of the $\Delta\Sigma$ converter.

The $\Delta\Sigma$ converter is suitable for low-frequency applications because of its ability to shape the quantization noise from low to high frequencies efficiently. In the first-order $\Delta\Sigma$ converter, the noise is reduced by 9 dB, by doubling the sampling frequency, whereas in the second-order $\Delta\Sigma$ converter the same value is 15 dB. In principle, the additions of the integrator and feedback branches increase the noise attenuation, but these structures have stability considerations [53]. Furthermore, the second-order $\Delta\Sigma$ converter is robust, and the feedback loop attenuates errors originating from the second integrator and comparator. Even if the first integrator is sensitive to the low-frequency noise and the offset of the operational amplifier, these can be reduced by using correlated double sampling and chopper stabilization, as was done in [P4, P5, P6].

Overall, the direct digital conversion and the robustness of the $\Delta\Sigma$ converters are benefits compared to, for example, the SC voltage amplifier, where the output of the SC front-end is converted with a separate ADC. In addition, the resolution of the Nyquist-rate ADCs is limited to a 10-12-bit range as a result of component matching and circuit non-idealities [54]. The disadvantages of the $\Delta\Sigma$ converter are the high sampling frequency and the need for a digital low-pass filter and a downsampler, a decimator, to suppress the high-frequency quantization noise and to lower the bandwidth. Depending on the technology that is used, the silicon area of the decimator can be significant, compared to the other circuit blocks of the interface.

3.3.2 Mechanical Open-Loop Charge-Balancing Front-Ends

In mechanical open-loop charge-balancing front-ends, the mass deflects according to the acceleration. The difference from the mechanical open-loop front-ends described in Section 3.3.1 is that the sizes of the electrostatic forces of the sensor capacitors of the differential capacitive accelerometer are equal, in other words balanced. Next, these kinds of front-ends, namely the self-balancing bridge and $\Delta\Sigma$ front-end topologies, are introduced.

Self-Balancing Bridge

In the self-balancing bridge [17], the front-end changes the voltage of the sensor middle electrode D_{MID} to the value where the charges in the sensor capacitors C_{DP} and C_{DN} are equal. In the self-balancing bridge, shown in Fig. 3.8, there are two clock phases, the measurement phase ϕ_1 and the reset phase ϕ_2. In phase ϕ_2, the output voltage V_{OUT} is loaded into C_4, leading to the voltage of D_{MID} being equal to V_{OUT}. In phase ϕ_1, the capacitors C_{DP} and C_{DN} are connected to the reference voltages and the difference between the charges is integrated, causing a change in V_{OUT}. Repeating the clock phases, the voltage of D_{MID} achieves a value where the charges in the capacitors C_{DP} and C_{DN} are equal, and no charge is integrated. In that case, the output voltage is

$$V_{OUT} = \frac{C_{DP} - C_{DN}}{C_{DP} + C_{DN}} V_{REF} \,. \tag{3.33}$$

By substituting (2.13) into (3.33), the output voltage can be rewritten as

$$V_{OUT} = \frac{\Delta d}{d_0} V_{REF} \,. \tag{3.34}$$

Therefore, the output voltage of the front-end is ratiometric; in other words, the output voltage is linearly proportional to Δd, and, hence, to the acceleration. This

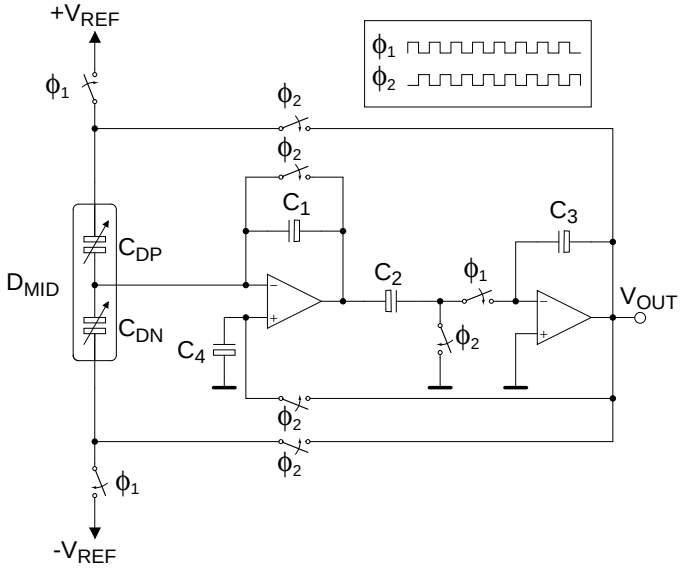

Figure 3.8: Self-balancing bridge.

is an advantage compared to the open-loop front-ends discussed in Section 3.3.1. In these front-ends, the outputs are linearly proportional to the capacitance difference $C_{DP} - C_{DN}$, but do not remove the effect of the displacement-to-capacitance conversion, which can be seen by rewriting the term by using (2.13), as

$$C_{DP} - C_{DN} = A\varepsilon_0\varepsilon_r \frac{2\Delta d}{d_0^2 - \Delta d^2}\,. \tag{3.35}$$

By calculating the biasing voltages over the capacitors C_{DP} and C_{DN}, using the output voltage of (3.34), the following charges in the capacitors C_{DP} and C_{DN} are achieved

$$\begin{aligned} |Q_{C_{DP}}| &= \left| \frac{A\varepsilon_0\varepsilon_r}{d_0 - \Delta d}\left(1 - \frac{\Delta d}{d_0}\right) V_{REF} \right| = \frac{A\varepsilon_0\varepsilon_r}{d_0} V_{REF} = C_0 V_{REF}\,, \\ |Q_{C_{DN}}| &= \left| \frac{A\varepsilon_0\varepsilon_r}{d_0 + \Delta d}\left(\frac{\Delta d}{d_0} + 1\right) V_{REF} \right| = \frac{A\varepsilon_0\varepsilon_r}{d_0} V_{REF} = C_0 V_{REF}\,. \end{aligned} \tag{3.36}$$

Because the charges are the same in the capacitors C_{DP} and C_{DN}, according to (3.11), the electrostatic forces are equal,

$$|F_{es,C_{DP}}| = |F_{es,C_{DN}}| = \frac{1}{2}\frac{A\varepsilon_0\varepsilon_r}{d_0^2} V_{REF}^2 = \frac{1}{2}\frac{C_0^2 V_{REF}^2}{A\varepsilon_0\varepsilon_r}\,. \tag{3.37}$$

According to the above analysis, the self-balancing bridge reduces the effects of the displacement-to-capacitance conversion and the electrostatic forces.

$\Delta\Sigma$ Front-End

The charge balance can also be achieved by using a $\Delta\Sigma$ converter topology, which is named as a $\Delta\Sigma$ front-end in this thesis. In [19], a similar structure to that in Fig. 3.9 is presented. The operation of the front-end is based on either of the sensor capacitors C_{DP} or C_{DN} being connected to the reference voltage, and then discharged in the integrator, in clock phases ϕ_1 and ϕ_2, respectively. Because the average integrated charge has to be zero, the sum of the average charges discharged from the capacitors C_{DP} and C_{DN} has to be equal. Therefore, the charge balance is achieved, and the effective electrostatic forces are equal. In addition, by summing the integrated charges, as in Section 3.3.1, the following charge equation is achieved:

$$-C_{DP}V_{REF}\left(1-\overline{B}\right)+C_{DN}V_{REF}\overline{B}=0\,, \tag{3.38}$$

and thereby the bit average of the one-bit output is

$$\overline{B}=\frac{1}{2}\frac{C_{DP}-C_{DN}}{C_{DP}+C_{DN}}+\frac{1}{2}\,. \tag{3.39}$$

From (3.39), it can be seen that the output of the $\Delta\Sigma$ front-end is ratiometric, as in the self-balancing bridge.

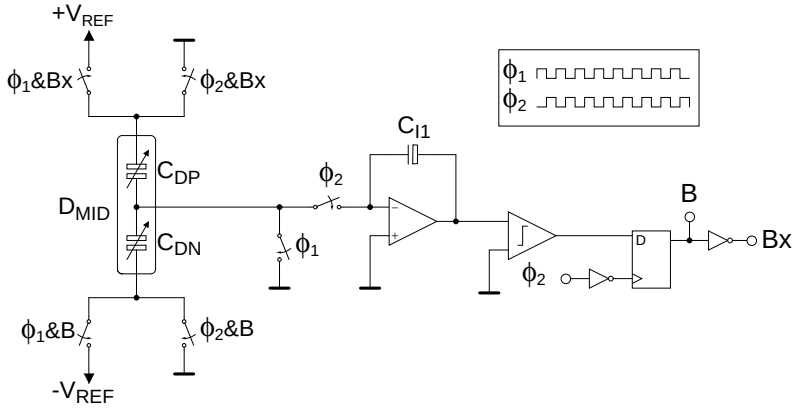

Figure 3.9: $\Delta\Sigma$ front-end.

In [P4, P5, P6], a signal boosting and offset compensation is developed for the $\Delta\Sigma$ front-end. The effect of this technique is studied by adding the capacitors C_{CBP} and C_{CBN}, as shown in Fig. 3.10, to the $\Delta\Sigma$ front-end. In practice, the capacitances reduce, sink, the charges integrated from the capacitors C_{DP} and C_{DN}. By using the above method, the bit average of the one-bit output is derived as

$$\overline{B}=\frac{1}{2}\frac{C_{DP}-C_{DN}-(C_{CBP}-C_{CBN})}{C_{DP}+C_{DN}-(C_{CBP}+C_{CBN})}+\frac{1}{2}\,. \tag{3.40}$$

From (3.40), it can be seen that by using equal capacitors C_{CBP} and C_{CBN}, the denominator of $\overline{B}$ can be reduced, and thus the signal is larger, boosted, but (3.40)

is no longer ratiometric. Another purpose of the capacitors is to compensate for the parallel parasitics of the capacitors C_{DP} and C_{DN}. If these parallel parasitics are C_{CP} and C_{CN}, for C_{DP} and C_{DN}, respectively, it can be seen from (3.40) that if the values of the capacitors $C_{CBP} = C_{CP}$ and $C_{CBN} = C_{CN}$ are adjusted, the parasitics do not have an effect on (3.40). With these constraints, (3.40) is ratiometric, even in the presence of the parallel parasitics. The implementation of this signal boosting and offset compensation can be implemented with a single capacitor matrix, as was done in [P4, P5, P6].

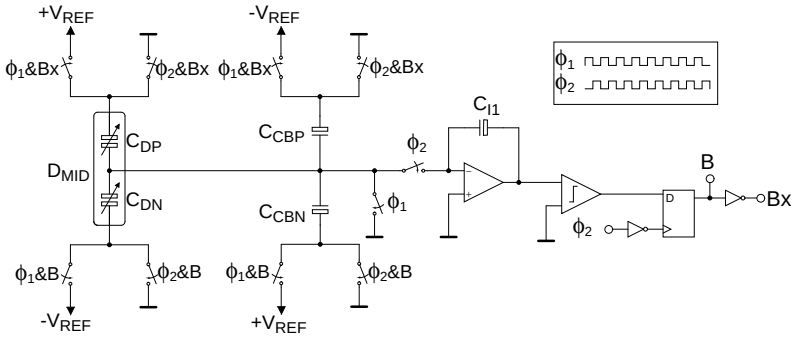

Figure 3.10: $\Delta\Sigma$ front-end with the signal boosting and offset compensation.

Ratiometric SC Front-End without Charge Balance

Even if the structures that were introduced above are charge-balancing and ratiometric, a ratiometric front-end is not in general necessarily charge-balancing. For example, in the implementation of [55], which is shown in Fig. 3.11, the output voltage is ratiometric:

$$V_{OUT} = \frac{C_{DP} - C_{DN}}{C_{DP} + C_{DN}} V_{REF} \,. \tag{3.41}$$

However, the front-end does not achieve charge balance in either of the clock phases. In phase ϕ_1 the voltage over the sensor capacitors C_{DP} and C_{DN} is constant, equal to V_{REF}, and thus, when the capacitors C_{DP} and C_{DN} are not equal, the charges are different. In phase ϕ_2, the output voltage $(\Delta d/d_0)\, V_{REF}$ is biased over both capacitors. Therefore, as the capacitors C_{DP} and C_{DN} are not equal, the charges are different in both clock phases. In consequence, the topology does not balance either the charges or the electrostatic forces, in spite of the fact that it is ratiometric.

3.3.3 Mechanical Closed-Loop Front-Ends

In the mechanical closed-loop front-end the mass is kept in position by using feedback. In practice, the feedback is implemented with electrostatic forces which balance the movement of the mass, which may be the reason why these front-ends are

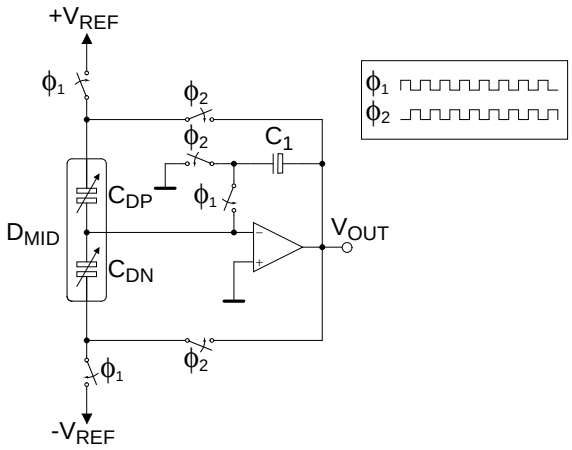

Figure 3.11: Ratiometric SC front-end.

called force-feedbacks. Next, the topology of the force-feedback is introduced on a general level, and an example case is discussed in Section 4.1.

Fig. 3.12 shows a typical force-feedback topology. The structure is based on a $\Delta\Sigma$ converter, which by using force-feedback, keeps the mass in position in the presence of acceleration. As can be seen from the topology, there are differences compared to a basic $\Delta\Sigma$ converter. In the loop, the two integrators are replaced by a capacitive accelerometer, which fulfils the same transfer function, but in this case from the force to the displacement. The following capacitance-to-voltage conversion is usually realized with a mechanical open-loop front-end, and the output voltage is amplified to achieve the required loop amplification. The compensator can be implemented, for example, with a lead filter to guarantee the stability of the loop. To convert the output to digital pulses, a comparator is used for the quantization, as is generally the case in $\Delta\Sigma$ converters. Since the output bits contain the acceleration information, it is used to control the force transducer. As in $\Delta\Sigma$ converters, the low-pass filtered and down-sampled digital acceleration information is achieved by using a decimator.

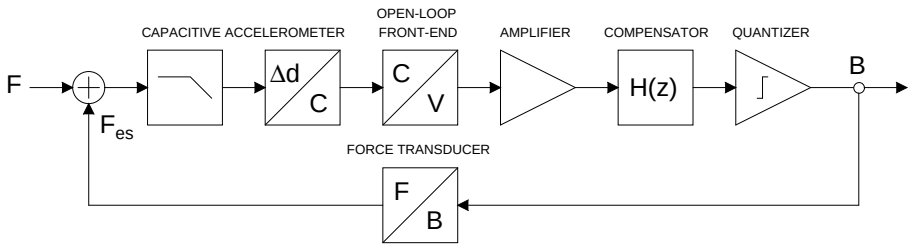

Figure 3.12: $\Delta\Sigma$ force-feedback topology.

It can be deduced that by using the force-feedback topology many advantages are achieved, such as wide bandwidth, good linearity, and a wide dynamic range. In

a force-feedback, the electronics make possible the high gain and bandwidth of the loop. Hence, the closed-loop bandwidth can be extended beyond the bandwidth of the proof mass [38]. Because ideally the mass does not move, the linearity is not reduced by the displacement or the electrostatic forces. In addition, the high-oversampling $\Delta\Sigma$ converter provides an inherent high-resolution digital output signal. The force-feedback has been a popular topology to implement the readout electronics for a capacitive accelerometer. After the first force-feedback structure was presented by Henrion et. al. [56], many competent implementations have been published [33, 57, 58, 59, 60, 61, 62, 63, 64].

Compared to the open-loop front-end topologies, the force-feedback topologies are more complex, since an open-loop front-end is a part of the structure. The complexity means more electronic circuitry, which increases the power consumption. Furthermore, to achieve the electrostatic forces needed to keep the mass in position, a sufficient voltage has to be used. Depending on the accelerometer, the voltage requirement can be substantial. For example, if the accelerometer has a maximum acceleration of a_{max}, the required compensating electrostatic force can be written as

$$ma_{max} = \frac{1}{2}\frac{A\varepsilon_0\varepsilon_r V_B^2}{d_0^2}\,. \tag{3.42}$$

Therefore, the biasing voltage requirement is

$$V_B = \sqrt{\frac{2ma_{max}d_0^2}{A\varepsilon_0\varepsilon_r}}\,. \tag{3.43}$$

In practice, this means a biasing voltage of approximately 10.5 V for the accelerometer shown in Table 3.1, if the maximum acceleration is 2 g[11]. According to the complexity of the mechanical closed-loop front-end and possible high-voltage requirement for the feedback, the open-loop topologies seem to be more suitable for low-voltage low-power front-ends.

3.4 Continuous-Time Front-Ends

In contrast to the discrete-time front-ends discussed above, continuous-time front-ends provide the accelerometer information as a continuous signal. Consequently, continuous-time front-ends do not suffer from the folding of the noise, as the discrete-time front-ends do. To illustrate the other properties of continuous-time front-ends, some topologies are briefly discussed.

[11]It is worth of noting that the voltage for the force-feedback can be increased from the lower supply voltage to this level by using charge pumps. However, the devices, such as switches, which are connected to this voltage have to tolerate this high voltage, which excludes the use of low-voltage CMOS processes. Additionally, the control of such switches may be complex.

Fig. 3.13(a) shows a continuous-time charge integrator. By defining the sum of the currents flowing into the negative input of the operational amplifier, which is zero, the following output voltage is obtained:

$$V_{OUT} = -\frac{C_{DP} - C_{DN}}{C_f} V_{REF} \,. \tag{3.44}$$

From (3.44) it can be seen that the output signal of the continuous-time charge integrator is similar to the case of the SC voltage amplifier, (3.25). However, unlike in the SC voltage amplifier, in this front-end the negative input is not dc-biased. Therefore, the leakage currents cause the saturation of the output of the operational amplifier, and thus the structure is not practical. By connecting a resistor R_f in parallel to the capacitor C_f, as shown in Fig. 3.13(a), the dc bias current can be fixed. The front-end is known as a transimpedance amplifier and its output voltage is

$$V_{OUT} = -\frac{sR_f \left(C_{DP} - C_{DN}\right)}{1 + sR_f C_f} V_{REF} \,. \tag{3.45}$$

From (3.45) it can be seen that the transfer function has the form of a high-pass filter, and thus to convert the low-frequency acceleration signals the corner frequency has to be lowered by increasing C_f or/and R_f. Increasing C_f lowers the amplitude of the output voltage, whereas the large passive R_f demands a lot of silicon area. By using a transimpedance amplifier with a differential operational amplifier and by connecting the dc voltage source V_{REF} to the middle electrode, according to Fig. 3.13(b), the acceleration signal can be converted into differential form. The structure is used in gyroscopes [65, 66] and in these implementations the large feedback resistors are implemented more area-efficiently with transistors. Even if large resistors can be achieved, the front-ends shown in Figs. 3.13(a), with the resistor R_f, and (b) are not capable of reading dc acceleration signals, because of the high-pass filtering.

By using modulation, the dc acceleration signal can be read with a continuous-time front-end. Fig. 3.13(c) shows a practical implementation of [67]. In this front-end the middle electrode is connected to the sinusoidal voltage V_{CAR}. As a result of this, in the outputs of the transimpedance amplifiers the acceleration information is amplitude-modulated with V_{CAR} as the carrier. By using diode rectifiers and low-pass filters, the acceleration information is amplitude-demodulated, and then converted to single-ended with the instrumentation amplifier A_{INA}.

Continuous-time front-ends provide some techniques which are used in SC front-ends. As mentioned in Section 3.3.1, chopper stabilization translates low-frequency noise to the higher frequencies. In other words, chopper stabilization is based on the modulation and thus can also be used in continuous-time front-ends, as was done in the high-performance implementation of [68]. In addition, with continuous-time front-ends, it is possible to implement force-feedbacks, as the implementations of [69, 70, 71, 72] did.

Even if continuous-time voltage sensing is shown to have a much lower noise level

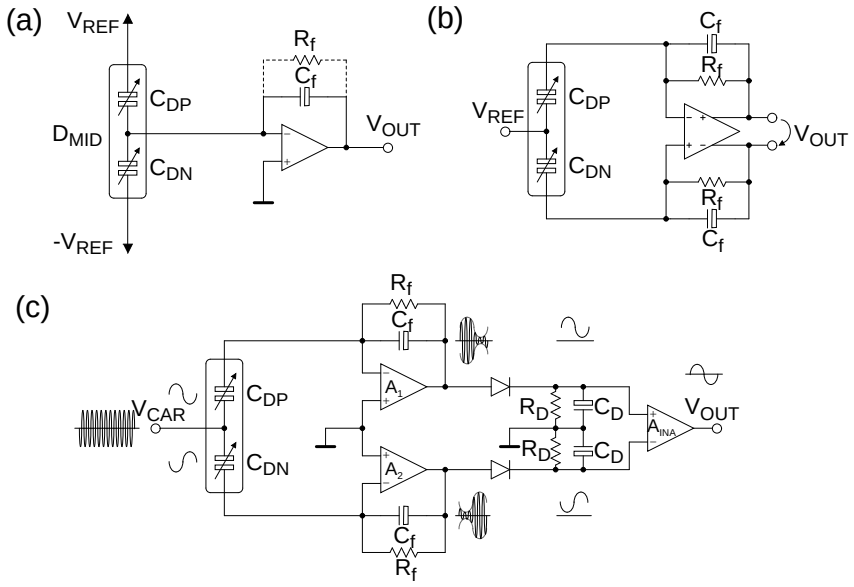

Figure 3.13: Continuous-time front-ends: (a) charge-integrator and (b) transimpedance amplifier, and (c) modulating topology of [67].

than similar SC implementations [73], the continuous-time front-ends were not chosen for the implementations of this thesis. The main reason was the electrostatic forces. To the best of the author's knowledge, there are no continuous-time front-end topologies which reduce the effects of the electrostatic forces and are suitable for low-power front-ends. Therefore, the discrete-time charge-balancing structures of Section 3.3.2 were chosen as more appropriate starting points for the front-ends considered in this thesis.

3.5 Discussion

In this chapter, front-ends for capacitive single-axis accelerometers were discussed. First, the effects of the displacement-to-capacitance conversion and the electrostatic forces were studied. It was noticed that the electrostatic forces cause not only non-linearity, like the displacement-to-capacitance conversion, but also electrostatic spring constant and pull-in. The electrostatic spring constant can be utilized for the adjustment of the spring constant, whereas the pull-in leads to the failure of the capacitive accelerometer.

Because the front-ends discussed in this thesis are based on switched-capacitor topologies, the discussion of the front-ends concentrated on discrete-time structures. The front-ends were divided according to their abilities to reduce the effects of the electrostatic forces. First, mechanical open-loop structures were analyzed. In these

front-ends the mass can deflect freely, and thus the adjustment of the parameters of the accelerometer and the biasing voltages are the methods to ensure the proper operation of the capacitive accelerometer in the presence of the electrostatic forces. Next, mechanical open-loop charge-balancing structures were studied. In these structures the mass can also move freely, but the electrostatic forces of the sensor capacitors are equal. Finally, mechanical closed-loop structures were introduced. The operation of these structures is based on the mass being kept stationary with electrostatic forces. Mechanical closed-loop structures, force-feedbacks, provide a wide bandwidth, good linearity, and wide dynamic range. However, the structures are more complex compared to those of mechanical open-loop structures, and thus consume more power. In addition, depending on the parameters of the capacitive accelerometer, the voltage for the feedback has to be high in order to achieve sufficient electrostatic forces. Therefore, mechanical open-loop charge-balancing structures seem to be more appropriate for low-voltage low-power front-ends.

At the end of the chapter, continuous-time front-ends were also briefly discussed. Continuous-time front-ends do not suffer from the folding of the noise as discrete-time front-ends, and thus they usually achieve a lower noise level. However, the continuous-time front-ends were not implemented in this thesis, because to the best of the author's knowledge there are no continuous-time topologies which reduce the effects of the electrostatic forces and are suitable for the low-power front-ends.

In the following chapter, Chapter 4, front-ends for capacitive three-axis accelerometers are discussed and compared.

4 Front-Ends for Capacitive Three-Axis Accelerometers

In Section 2.4, capacitive three-axis accelerometer structures were discussed. The structure of the accelerometer has a significant effect on which kind of front-end topology can be utilized. Designing a front-end for three different capacitive single-axis accelerometers is straightforward, since the masses are unconnected, as shown in Fig. 4.1(a). Consequently, three different front-ends can be utilized. However, capacitive three-axis accelerometers are usually micromachined on the same substrate and the masses have the same potential, as shown in Fig. 4.1(b). Therefore, the front-end has to be capable of preventing the engagement of the capacitance changes of the other masses. Generally, only a few front-ends which are able to read sensors of this kind have been published. Continuous-time front-ends were used in the implementations of [42] and [48]. In the latter case, the front-end is based on the modulating structure discussed in [67]. In the front-end of [42] the different axes are modulated to their own frequencies, and a force-feedback is used to keep the mass in position. The discrete-time implementation of [74] is a low-power SC implementation. However, the results of the front-end are based on simulations. An interesting discrete-time front-end and one that is often referred to is the force-feedback implementation of [38].

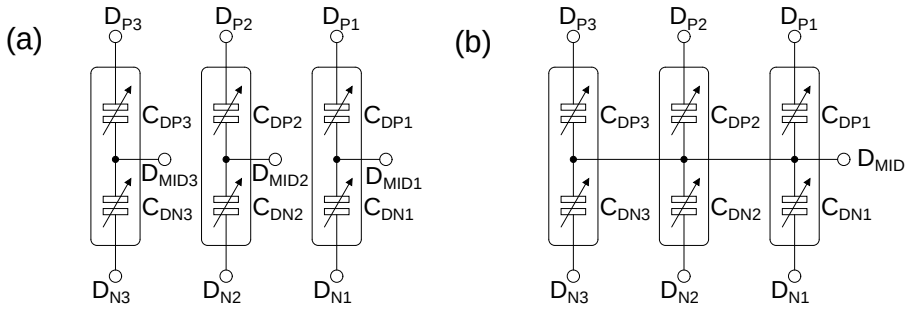

Figure 4.1: Capacitive three-axis accelerometer with (a) unconnected masses and (b) common middle electrode.

At the beginning of this chapter, three different front-end implementations for capacitive three-axis accelerometers will be introduced. The first implementation is the force-feedback front-end of [38] and the other two are the open-loop charge-balancing front-ends of this thesis. The introduction highlights the solutions to the question of how to read capacitive three-axis accelerometers and compares the implementations on a general level. The interfaces are also briefly discussed, because the front-end has an effect on the other blocks of the interface. For the same reason, in order to achieve an objective performance comparison, the interfaces should be compared, rather than the front-ends. Therefore, at the end of the chapter, before

the discussion, the commercial low-g low-power capacitive three-axis accelerometer products are utilized in the performance comparison.

4.1 Force-Feedback Front-End

The following force-feedback front-end for a capacitive three-axis accelerometer was implemented by Lemkin and Boser [38]. The $\Delta\Sigma$ force-feedback topology that was used is similar to that shown in Fig. 3.12. In the force-feedback, the accelerometer operates as a second-order integrator and the capacitance-voltage conversion is implemented with a charge integrator in which the force-feedback is included. The amplification is provided by three preamplifiers and the compensation is realized by a lead filter. The quantization is carried out by a comparator. The following discussion concentrates on the open-loop front-end and the force-feedback.

The open-loop front-end, including the force-feedback, and the clock phases are shown in Fig. 4.2. The operation of the front-end is divided into five operating phases. In the first phase, feedback, the accelerometer is disconnected from the charge integrator to prevent the overdriving of the operational amplifier A_1. The force-feedback is based on one-bit operation. Depending on the bit, a biasing voltage V_{FB} is connected to the outer node of the sensor capacitor C_{DP} or C_{DN}, D_P or D_N, whereas the middle electrode D_{MID} and the other outer electrode are grounded. Therefore, the attractive electrostatic force is generated over the capacitor C_{DP} or C_{DN}. As a result, the mass tends to move to the node connected to V_{FB}. In practice, by using a high sampling frequency, the position of the mass is nearly constant.

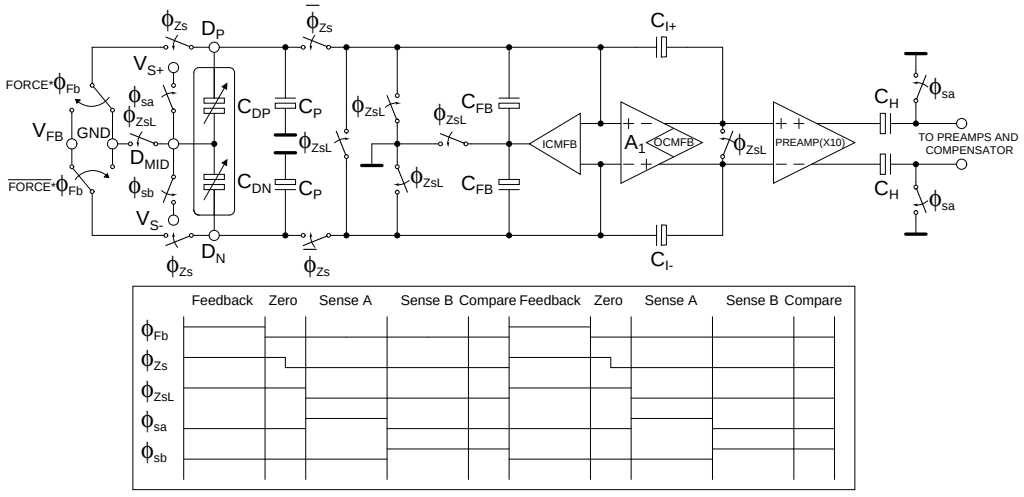

Figure 4.2: Charge integrator front-end with force-feedback.

After the feedback, the capacitive acceleration information is converted into analog voltage by using a charge integrator in two sensing phases, sense A and sense B,

respectively. Before the sense phases can be performed, a zero phase has to be carried out. In this phase the electrostatic forces of the capacitors C_{DP} and C_{DN} are reset by grounding all the nodes of the accelerometer, and then the accelerometer is connected to the charge integrator. At the end of the zero phase the biasing of the amplifier A_1 is completed, and the switches in the input and the output of the amplifier A_1 are opened. In the sense A and sense B phases, D_{MID} is connected to the reference voltages V_{S+} and V_{S-}, respectively. In the output of the charge integrator, these pulses cause voltage differences which are proportional to the capacitance difference of the capacitors C_{DP} and C_{DN}. In the amplifier A_1, an input common-mode feedback (ICMFB) is utilized. Without ICMFB, the inputs of the amplifier A_1 vary, which demands the sufficient common-mode rejection ratio and input common-mode range of A_1. In addition, the gain and offset errors caused by the variations in the inputs of A_1 are removed by ICMFB. When the output is settled in the sense B phase, the output of the last preamplifier is sampled by the compensator. In the compare phase, the output of the compensator is quantized, and then the front-end starts to perform the next feedback phase.

The method used to feed voltage pulses in D_{MID} makes the front-end differential, thereby increasing the output signal, improving the power-supply rejection ratio, and reducing the common-mode errors. Furthermore, by multiplying the number of front-ends, it is possible to read the masses of the capacitive three-axis accelerometers, which have the common middle electrode, simultaneously. In the front-end, correlated double sampling was implemented to reduce the dc offset and 1/f noise of the amplifier A_1. In addition, the mismatch of the capacitors C_{DP} and C_{DN} is reduced by connecting a binary weighted capacitor array in parallel with the sensor capacitors. The capacitive three-axis accelerometer, which has a separate mass for each direction, and the electronics were integrated on a 4×4-mm^2 microchip by using surface micromachining. The electronics were integrated on the wafer with a 2-μm CMOS processing. The interface draws 27 mA from a 5-V supply, while the sampling rate is 500 kHz. The measured noise floors for the x-, y-, and z-directions are 110, 160, and 990 $\mu g/\sqrt{\text{Hz}}$, respectively.

4.2 Charge-Balancing Front-End with Analog Output

The first front-end designed and described in this thesis is a part of the low-power interface shown in Fig 4.3. The front-end was designed for a four-mass capacitive three-axis accelerometer, similar to that shown in Figs. 2.11(a) and (b). In the interface, the front-end converts the capacitive acceleration information into an analog voltage which is converted into digital form in the ADC. The 2-MHz clock signal for the clock generator of the front-end is contrived in the system clock generator (SYSCLK). The currents and the reference voltages of the front-end are provided by the voltage, current, and temperature reference (V/I/TREF). The controlling of the front-end is achieved by using a digital signal processor (DSP), which, in the

measurements, was implemented with computer software.

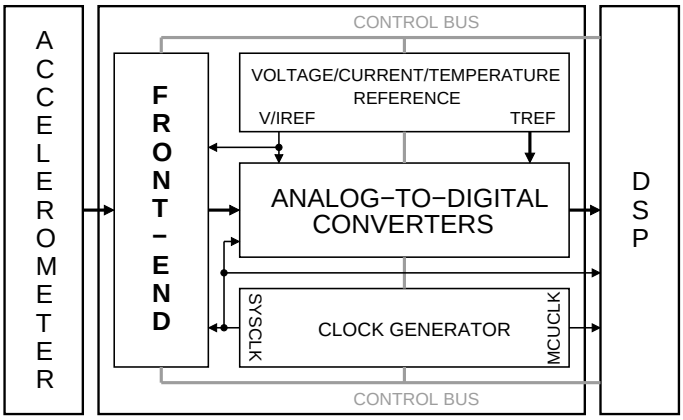

Figure 4.3: Low-power interface for a capacitive three-axis accelerometer [P1, P2, P3].

In order to design a low-power front-end which is able to reduce the effects of the electrostatic forces and the displacement-to-capacitance conversion, a self-balancing bridge was chosen as a starting point for the design. As discussed in Section 3.3.2, the operation of the self-balancing bridge is based on the fact that the voltage of the middle electrode changes to the value where the charges, and hence the electrostatic forces of the sensor capacitors C_{DP} and C_{DN}, are equal. In addition, the output voltage of the self-balancing bridge is ratiometric, and thus it linearizes the displacement-to-capacitance conversion. The low-power front-end that was developed and features time-multiplexing, differential mode operation, correlated double sampling, and chopper stabilization, is shown in Fig. 4.4.

Because of the common middle electrode of the capacitive three-axis accelerometer, the acceleration information of the four masses cannot be read simultaneously with four front-ends, as in the implementation of [38]. In this case each self-balancing bridge would try to change the voltage of the middle electrode. Furthermore, the capacitances between the outer nodes, D_{Pn} and D_{Nn}, with $n = 1, 2, 3,$ or 4, cause the engagement of the other masses to the read mass. These capacitances can be substantial, especially when the sensor element and the microchip are connected in a printed circuit board (PCB). In the front-end that was designed, shown in Fig. 4.4, the not-read masses are silenced by short-circuiting the outer nodes of the sensor to the middle electrode D_{MID}, and each of the masses is read alternately by using time-multiplexing.

In practice, the time-multiplexing is implemented in such a way that the read of the mass is started at the beginning of phase ϕ_2. In consequence, in the single-ended mode, the previous output voltage of the mass, stored in the capacitor C_{3Pn} or C_{3Pn_CS}, where CS indicates that the mass is read with inverted reference voltages,

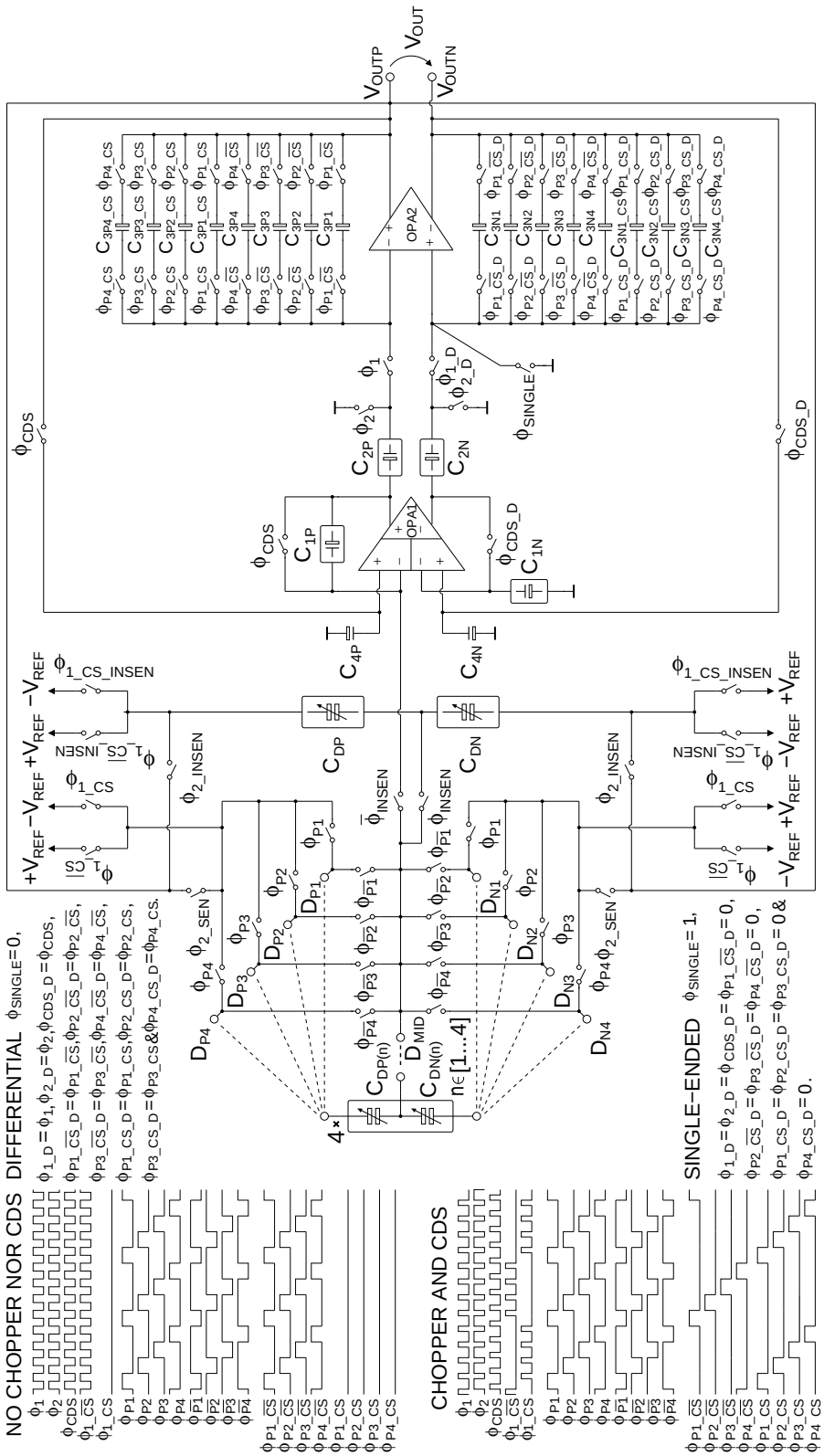

Figure 4.4: Self-balancing bridge front-end for a four-mass capacitive three-axis accelerometer [P1, P2, P3].

is loaded into the middle electrode D_{MID} via the capacitor C_{4P}. In phase ϕ_1 the new value is measured and the new output voltage is stored in the capacitor C_{3Pn} or C_{3Pn_CS}. Compared to the simultaneous reading which the front-end of [38] provides, the sampling frequency has to be four times higher in the time-multiplexing to achieve the same output data rate. However, in the time-multiplexing the number of the devices, amplifiers, capacitors and switches, and thus the silicon area, can be reduced.

As in the implementation of [38], the front-end was implemented as a differential circuit which provides a differential voltage to ADC and thus makes possible a more effective use of the signal range in the ADC. By using the differential difference amplifier (DDA) [75], the single-ended integrated charge from D_{MID} is converted to a differential signal. The latter part of the differential front-end was implemented by adding the capacitors and switches, and using the differential amplifier $OPA2$. To compare the differences between the single-ended and differential modes, both operating modes were implemented in the same front-end.

In the front-end that was designed, the operational amplifiers dominate the current consumption. Therefore, tail current-boosted Class-AB operational amplifiers [76] are used. In contrast to the conventional slew rate-dominated amplifiers, in the operational amplifiers that were designed the bias current increases quadratically proportional to the differential input voltage, and thus faster settling is achieved. In addition, the input pairs of the amplifiers are dimensioned in such a way that the transistors are in weak inversion under quiescent conditions. In consequence, the current efficiency g_m/I_D, where g_m is the transconductance of the transistor and I_D the biasing current, is maximized. Even if the supply voltage of the front-end is nominally as low as 1.8 V, the cascode structures can be utilized in the operational amplifiers, as in the implementation of [38].

An effective method to reduce the current consumption of the operational amplifiers is to lower the sampling frequency. However, as was discussed in Section 3.3.1, the sampling frequency affects the noise. By lowering the sampling frequency, the high-frequency noise is folded to the narrower bandwidth and thus the noise floor rises. Furthermore, when the sampling frequency is lowered, the leakage currents of the switches have to be taken into account. In the front-end that was designed it was noticed that the significant leakage currents are caused by the switches which are connected to the reference voltages $-V_{REF}$ and $+V_{REF}$. The leakage current of those switches is caused by subthreshold currents. By lengthening the transistors of these switches, the threshold voltages were increased and the leakage currents minimized.

The first interface that was designed for a ±4-g capacitive three-axis accelerometer was implemented with a 0.13-μm BiCMOS process. The active area of the interface and the front-end are 0.51 and 0.30 mm^2, respectively. The current consumption of the interface and the front-end are 62.9 and 18.3 μA from a 1.8-V supply, respectively, when each of the four masses are sampled at 1.04 kHz in the differential

mode. The measured noise floors of the interface in the x-, y-, and z-directions are 482, 639, and 662 $\mu g/\sqrt{Hz}$, respectively, when correlated double sampling, chopper stabilization, and the differential mode are used.

4.3 Charge-Balancing Front-End with Digital Output

The second front-end designed and described in this thesis is a part of the interface shown in Fig. 4.5. The front-end was designed for a three-mass capacitive three-axis accelerometer. In the interface, the front-end converts the capacitive information directly into a digital signal which is low-pass filtered and downsampled in the decimator. The supply and the reference voltages and currents are generated by the low-dropout regulator (LDO1) and the voltage and current reference (V/IREF), respectively. The reference voltages are scaled and buffered by the reference voltage buffers (REFBUFs). The frequency reference circuit (FREF) provides the main clock signal for the clock generator of the front-end (CLKG).

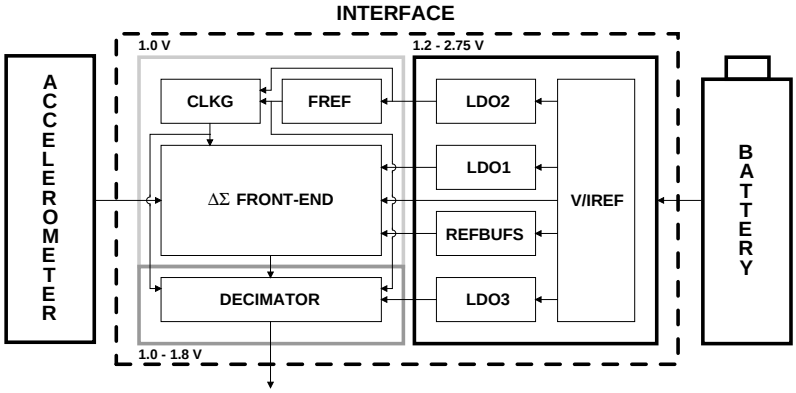

Figure 4.5: Low-power interface for a capacitive three-axis accelerometer [P4, P5, P6].

The $\Delta\Sigma$ front-end was chosen to be a starting point for the front-end that was designed, because of its abilities to reduce the effects of the electrostatic forces and displacement-to-capacitance conversion. As discussed in Section 3.3.2, the operation of the front-end is based on the smaller sensor capacitor being sampled more often than the larger one. Thus the average charges and the electrostatic forces are equal in both sensor capacitors. Moreover, the output of the $\Delta\Sigma$ front-end is ratiometric, and thus linearizes the displacement-to-capacitance conversion. In the interface that was designed, the supply voltage of the front-end is regulated to 1 V. As discussed in Section 3.3.3, to generate sufficient electrostatic forces for the force-feedback, this supply is rather low, as is the 1.8-V supply voltage of the first

front-end. Furthermore, by using open-loop charge-balancing structures, less complicated front-ends with lower power consumption can be implemented. Therefore the selection of the open-loop charge-balancing front-end topologies was justified for both implementations of this thesis.

The main reasons why the $\Delta\Sigma$ front-end was selected instead of the self-balancing bridge, as in the first front-end, were inherent analog-to-digital (A/D) conversion and the limitations of the lower supply voltage. In practice, with the $\Delta\Sigma$ front-end, the digital acceleration information is achieved with the same number of operational amplifiers as the analog acceleration information in the self-balancing bridge. As the output signal is directly digital, it was decided to implement the front-end as a single-ended one to achieve simpler structure and lower power consumption than with the differential conversion. From the viewpoint of the low supply voltage, the variable voltage of the sensor middle electrode causes the change in the input voltage of the first operational amplifier of the self-balancing bridge, and thus demands a sufficient input common-mode range. The input range of the operational amplifiers is limited in the 1-V supply voltage, and thus the constant input voltages of the operational amplifiers of the $\Delta\Sigma$ front-end are more practical. In the front-end that was designed, the input voltage of the PMOS-input operational amplifiers is 0.1 V.

The front-end that was developed, with time-multiplexing, correlated double sampling, chopper stabilization, and signal boosting and offset compensation, which was discussed in Section 3.3.2, is shown in Fig. 4.6. The capacitive three-axis accelerometer that was used has three masses, not four masses as in the first front-end. The middle electrode of the accelerometer is common for all the three masses. As in the first front-end, it was decided to utilize time-multiplexing. The not-read masses are silenced by short-circuiting the outer nodes of the accelerometers $D_{P(n)}$ and $D_{N(n)}$, where $n = 1, 2,$ or 3, in the middle electrode D_{MID}, as in the first front-end. The operational amplifier of the first integrator and the comparator are time-multiplexed, but there is one second integrator for each mass and for the non-inverted and the inverted reference voltages which the chopper stabilization demands. Six second integrators make it possible for the integrator to transfer the charge from the capacitors $C_{DAC2\_(nX)}$ and $C_{2\_(nX)}$ to the integrator capacitor $C_{I2\_(nX)}$, where $X = P$ or N, while the other masses are read, leaving time for the operational amplifier to settle. When the mass in question is read again, in phase A the output is ready to be sampled by the comparator. In the same phase the sensor capacitor $C_{DP(n)}$ or $C_{DN(n)}$ is charged to that of the reference voltage $-V_{REF}$ or $+V_{REF}$, defined by the output bit. At the beginning of phase B, the comparator solves the new bit, and $C_{DAC2\_(nX)}$ is charged to $-V_{REF}$ or $+V_{REF}$, defined by the bit. The change of the bit is delayed in the mass switching, because without it, discharging error is possible. In practice, in the proper operation of phase B, the charge of the capacitor $C_{DP(n)}$ or $C_{DN(n)}$ is integrated by the first integrator, and the second integrator samples the new output voltage of the first integrator. If the bit changes between the clock phases A and B, the charge of the capacitor $C_{DP(n)}$ or $C_{DN(n)}$ would be discharged by the short-circuiting and thus no charge is integrated in the first integrator.

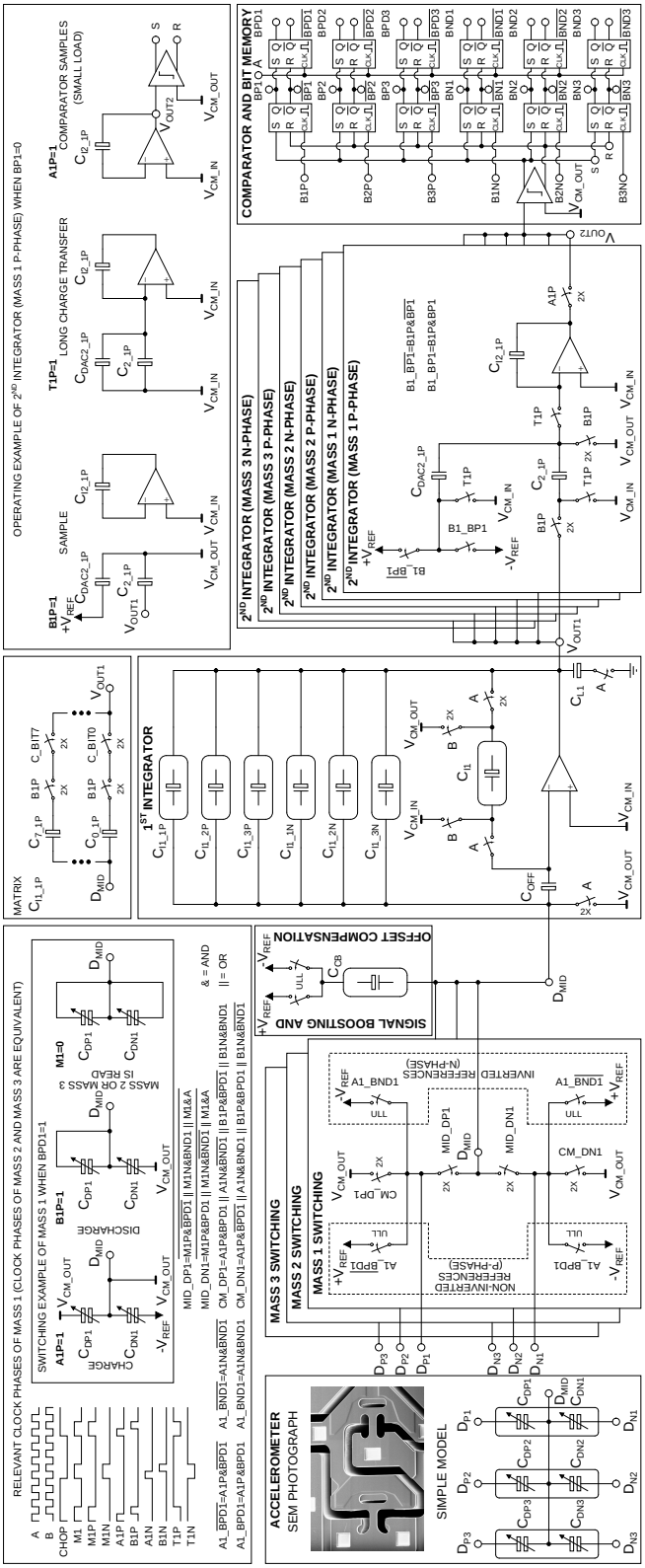

Figure 4.6: $\Delta\Sigma$ front-end for a three-mass capacitive three-axis accelerometer [P4, P5, P6]. A scanning electron microscope (SEM) image courtesy of VTI Technologies, Vantaa, Finland.

To save the current consumption, as in the first front-end, a tail current-boosted Class-AB operational amplifier [76] with enhanced dc gain [77] is used in the first integrator. In the second integrators a current mirror operational transconductance amplifier (OTA) with enhanced dc gain is utilized. The dynamic latch with zero static power consumption is used as a comparator [78]. The 1-V supply voltage is not enough for using cascode stages, and thus the dc gains of the amplifiers are moderate, with simulated values of 50 dB and 45 dB for the first and the second operational amplifiers, respectively. According to the simulations, these gains are sufficient to suppress the quantization noise in the signal band. In addition, the errors in the second integrator and the comparator are high-pass filtered, which relaxes the requirements of these devices.

The sampling frequency was minimized, as in the first front-end, to achieve lower power consumption. The front-end operates in 1- or 25-Hz-bandwidth modes. In order to achieve a sufficient (>20 dB) mechanical attenuation of folding out-of-band interferers with a typical mechanical bandwidth of 100 Hz, in the slower 1-Hz mode, each of the masses is sampled at a sampling frequency of 4.096 kHz. Because of the chopper stabilization, the mass is read with non-inverted and inverted reference voltages and thus, by using the difference demodulation, shown in Fig. 3.5(a), the practical sampling frequency is 2.048 kHz per mass. To prevent the leakage currents, especially in the sensitive node D_{MID}, a special ultra-low-leakage switch, similar to the one presented in [79], was developed; these are marked as ULL in Fig. 4.6. In contrast to the first front-end, the 1-V supply is not sufficient to achieve proper resistances in the floating transmission gates, and thus the gate voltages of NMOS devices are increased by using charge pumps [80], marked as 2X.

The second interface for the ±4-g capacitive three-axis accelerometer was implemented by using a 0.25-μm CMOS process. The active area of the interface is 1.73 mm^2, from which 0.53 mm^2 is allocated for the front-end. In the 1- and 25-Hz modes the current consumption of the interface from a 1.2−2.75-V supply is 21.2 and 97.6 μA, respectively. Corresponding values for the front-end, from a 1-V regulated supply, are 1.2 and 20.5 μA. In the 1- and 25-Hz modes, the measured noise floors of the interface in the x-, y-, and z-directions are 1080, 1100, and 930 $\mu g/\sqrt{\text{Hz}}$, and 360, 320, and 275 $\mu g/\sqrt{\text{Hz}}$, respectively, when correlated double sampling and chopper stabilization are used, but signal boosting and compensation are not utilized.

4.4 Performance Comparison

In the previous chapters, the comparison of the published front-ends for the capacitive three-axis accelerometers concentrated on the differences between the implementations. To make an objective performance comparison, the most important parameters have to be taken into account. Commonly, the performance comparison is made by utilizing a generally accepted figure of merit (FOM), such as Walden's

FOM used for ADCs [81]. However, to the best of the author's knowledge, this kind of FOM does not exist for accelerometers. Therefore, in this thesis, as in the publication of [P6], the following FOM in units of (μW $\cdot$ μg/Hz) is defined

$$FOM = \frac{V_{dd} I_{dd} a_n \sqrt{BW}}{BW}, \tag{4.1}$$

where V_{dd} is the supply voltage, I_{dd} the current consumption, a_n the noise floor and BW the bandwidth. In consequence, the FOM includes the most relevant performance parameters and the smaller the FOM is, the better the performance of the accelerometer is.

As mentioned at the beginning of this chapter, a more objective performance comparison is achieved if the interfaces are compared, because the front-end has a notable influence on the performance of the other parts of the interface, which cannot be seen by comparing the front-ends. For instance, the current consumptions of the front-ends of this thesis are less than 30% of the total current consumptions of the interfaces [P2, P6]. Therefore, the following performance comparison is realized for commercial accelerometers, including a capacitive three-axis accelerometer and an interface, which are intended for low-power applications.

Fig. 4.7 shows the updated FOMs of the commercially available low-g, low-power accelerometers. The accelerometers have a digital output unless stated otherwise. As a general rule for the parameters, the following values are used: the typical supply voltage and current consumption, the maximum noise floor, and the minimum signal bandwidth. If the typical supply voltage is not introduced, the average value of the minimum and the maximum is used. In the case of devices which have different operating modes, the one which minimizes the FOM is used. To clarify the interpretations of the datasheets, the values used for the parameters are shown in Table 4.1[12].

According to Fig. 4.7, accelerometers are grouped according to their minimum supply voltage. By comparing the ones implemented in this thesis with the other digital output interfaces, it can be seen that the first interface is still competitive among the products of the day. In addition, even if the second interface has a remarkably lower minimum supply voltage than the other interfaces, it has competitive FOMs, especially in the 25-Hz mode. Overall, it is encouraging that in all the low-power products, the front-ends operate mechanically in open-loop configuration, confirming that the decision not to concentrate on the force-feedback structures was justified.

[12]The sizes of the implementations [P2] and [P6] report the dimensions of the unpackaged microchip of the interface, whereas the sizes of the products define the dimensions of the packaged accelerometer.

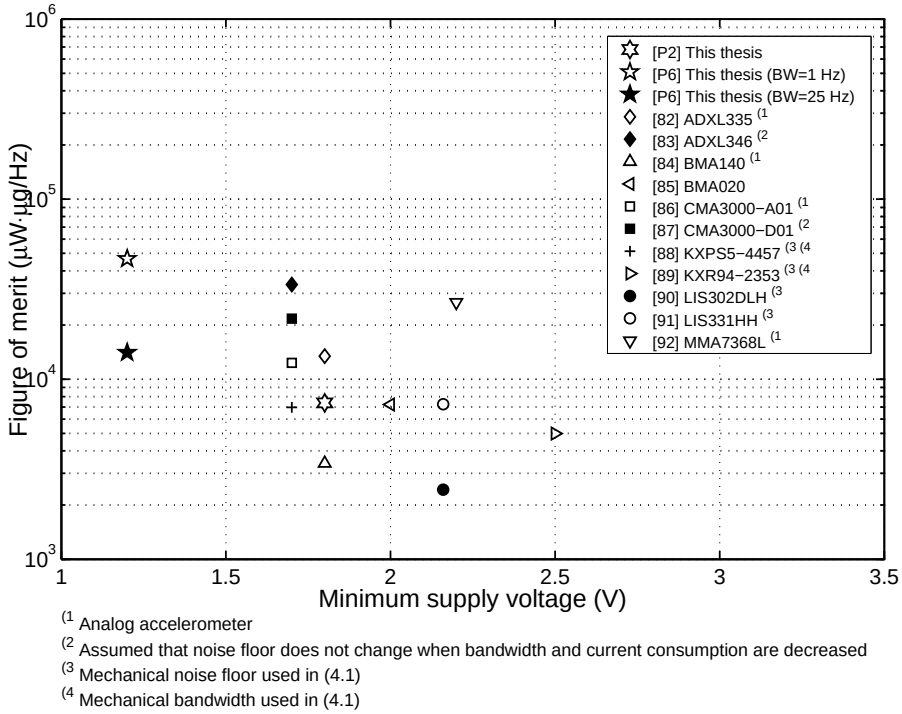

Figure 4.7: Performance comparison with commercially available, low-g, low-power accelerometers. Typical FOMs are plotted as a function of the minimum reported supply voltages.

Table 4.1: Parameters used in the performance comparison.

Accelerometer	V_{dd} (V)	I_{dd} (μA)	a_n $\left(\mu g/\sqrt{Hz}\right)$	BW (Hz)	FOM ($\mu W \cdot \mu g/Hz$)	Size (mm)
[P2] This thesis	1.8	62.9	662	100	7.495	1.66x1.66
[P6] This thesis	2	21.2	1100	1	46.640	2.17x1.90
[P6] This thesis	2	97.6	360	25	14.054	2.17x1.90
[82] ADXL335	3	350	300	550	13.432	4x4x1.45
[83] ADXL346	2.6	55	829	12.5	33.530	3x3x0.95
[84] BMA140	3	200	220	1500	3.408	3x3x0.9
[85] BMA020	2.8	200	500	1500	7.230	3x3x0.9
[86] CMA3000-A01	2.5	180	300	120	12.324	2x2x0.95
[87] CMA3000-D01	2.5	11	2230	8	21.682	2x2x0.95
[88] KXPS5-4457	1.8	700	175	1000	6.973	5x3x0.9
[89] KXR94-2353	3.3	950	45	800	4.988	5x5x1.2
[90] LIS302DLH	2.5	10	218	5	2.437	3x5x0.8
[91] LIS331HH	2.5	10	650	5	7.267	3x3x1
[92] MMA7368L	3.3	400	350	300	26.674	3x5x1

4.5 Discussion

In this chapter, the front-ends for capacitive three-axis accelerometers were discussed. At the beginning, it was mentioned that capacitive three-axis accelerometers are usually implemented on the same substrate, and thus the masses have the same potential. To prevent engagement of the capacitance changes in other directions, the common middle electrode structure has to be taken into account. Generally, not many front-ends have been published for these kinds of capacitive three-axis accelerometers.

In the presentation of the front-ends, three different implementations were introduced and compared. The first topology was the force-feedback of [38] and the other two were the mechanical open-loop charge-balancing structures of this thesis. The comparison concentrated on the differences between these implementations, whereas the comparison at the end of the chapter focused on comparing the performances of the three-axis accelerometer systems discussed in this thesis with those of the commercial products. Because the front-end has a notable influence on the other building blocks of the interface, the performance comparison was performed for the interfaces in order to achieve a more objective result. The comparison method was based on an FOM which included the most relevant performance parameters. In the comparison, commercially available, low-g, low-power accelerometers, including a capacitive three-axis accelerometer and an interface, were used. According to the comparison, it was noticed that both interfaces are still competitive with today's products. In addition, the later interface has a remarkably lower minimum supply voltage than the other interfaces.

5 Conclusions

In this thesis, two low-power interfaces for capacitive three-axis accelerometers were introduced. The focus of the thesis was on the front-ends of the interfaces. The front-end is the part of the interface which converts the capacitive acceleration information into a convenient form for electrical applications, such as an analog or digital signal, and maximizes the linear acceleration range. Generally, the non-linearity is caused by the effects of the displacement-to-capacitance conversion and the electrostatic forces. A force-feedback is an effective structure to reduce the non-linearity, because it ideally keeps the position of the mass fixed. However, the complex structure and high-voltage demand of the electrostatic force-feedback are not suitable features for low-power and low-voltage front-ends. Therefore, mechanical open-loop charge-balancing structures which are capable of reducing the effects of the displacement-to-capacitance conversion and the electrostatic forces were utilized in this thesis.

In the first interface, the self-balancing bridge was chosen as a starting point for the front-end. The topology changes the voltage of the middle electrode of the capacitive accelerometer to a value in which the charges of the sensor capacitors, and thus the electrostatic forces, are equal. Furthermore, the analog output of the front-end is ratiometric, which linearizes the displacement-to-capacitance conversion. The front-end was developed to be suitable for a ±4-g four-mass capacitive three-axis accelerometer by using time-multiplexing. In addition, the performance of the front-end was improved by adding the following options: correlated double sampling, chopper stabilization, and single-ended-to-differential conversion. In the interface, the analog output voltage of the front-end is converted into the digital domain by an ADC. In the implementation, a 0.13-μm BiCMOS process was utilized. The active areas of the interface and the front-end are 0.51 and 0.30 mm^2, respectively. The current consumption of the interface and the front-end are 62.9 and 18.3 μA from a 1.8-V supply, when each of the masses is sampled at 1.04 kHz in the differential mode. When correlated double sampling, chopper stabilization, and differential mode are used, the measured noise floors are 482, 639, and 662 $\mu g/\sqrt{\text{Hz}}$ in the x-, y-, and z-directions, respectively. These results yield a 10-bit dynamic range for a 100-Hz signal bandwidth.

The front-end of the second interface was based on the idea of connecting the capacitive accelerometer as a part of a $\Delta\Sigma$ converter. In this kind of $\Delta\Sigma$ front-end, the smaller sensor capacitor is sampled more often, and thus the average charges, as well as the electrostatic forces, are equal. Moreover, the output of the front-end is ratiometric. One of the main benefits, compared to the self-balancing bridge, is that the $\Delta\Sigma$ front-end inherently converts the capacitive acceleration information into the digital domain. The front-end was designed to be suitable for a ±4-g three-mass capacitive three-axis accelerometer by utilizing time-multiplexing. To improve the performance, the following properties were added to the front-end: second-order $\Delta\Sigma$

conversion, correlated double sampling, chopper stabilization, and signal boosting and offset compensation. By using a 0.25-μm CMOS process, the interface and the front-end were integrated on an active silicon area of 1.73 and 0.53 mm^2, respectively. The interface provides two operating modes for the 1- and 25-Hz bandwidths, and the current consumptions for these modes from a 1.2−2.75-V supply are 21.2 and 97.6 μA, respectively. The corresponding values for the front-end are 1.2 and 20.5 μA from a 1-V regulated supply. In the 1- and 25-Hz modes, when correlated double sampling and chopper stabilization are utilized, the measured noise floors in the x-, y-, and z-directions are 1080, 1100, and 930 $\mu g/\sqrt{\text{Hz}}$, and 360, 320, and 275 $\mu g/\sqrt{\text{Hz}}$, respectively. Therefore, a 12-bit dynamic range is achieved in both operating modes.

According to the performance comparison of the thesis, both interfaces are able to compete with the commercial low-g, low-power capacitive three-axis accelerometers. Furthermore, the second interface has a significantly lower minimum supply voltage than the commercial accelerometers. Regardless of these performance results, there is still room for future work. First, there are pressures to further lower the power consumption of the interfaces. As the functionalities of hand-held devices increase, the power consumption of the existing applications has to be lowered in order to maintain the battery lifetime. Moreover, it is possible that in future handheld devices will be able to harvest all or the most of their energy from sources such as light, heat, motion, or ambient RF energy. Because of the limited energy of the harvesters, electrical applications should operate with ultra-low power consumption. Second, this thesis concentrated on discrete-time charge-balancing front-end topologies, even if these structures usually have a higher noise level than the continuous-time topologies, as a result of the noise folding. Therefore it would be interesting to develop low-power continuous-time front-ends which are capable of reducing the effects of the electrostatic forces and displacement-to-capacitance conversion.

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