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INTEGRATED INTERFACE ELECTRONICS FOR CAPACITIVE MEMS INERTIAL SENSORS

Doctoral Dissertation

Lasse Aaltonen

Aalto University
School of Science and Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences

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School of Science and Technology
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Department	Department of Micro and Nanosciences
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Opponent(s)	Professor Pieter Rombouts
Supervisor	Professor Kari Halonen
Instructor	

Abstract

This thesis is composed of 13 publications and an overview of the research topic, which also summarizes the work. The research presented in this thesis concentrates on integrated circuits for the realization of interface electronics for capacitive MEMS (micro-electro-mechanical system) inertial sensors, i.e. accelerometers and gyroscopes. The research focuses on circuit techniques for capacitive detection and actuation and on high-voltage and clock generation within the sensor interface.

Characteristics of capacitive accelerometers and gyroscopes and the electronic circuits for accessing the capacitive information in open- and closed-loop configurations are introduced in the thesis. One part of the experimental work, an accelerometer, is realized as a continuous-time closed-loop sensor, and is capable of achieving sub-micro-g resolution. The interface electronics is implemented in a 0.7-μm high-voltage technology. It consists of a force feedback loop, clock generation circuits, and a digitizer. Another part of the experimental work, an analog 2-axis gyroscope, is optimized not only for noise, but predominantly for low power consumption and a small chip area. The implementation includes a pseudo-continuous-time sense readout, analog continuous-time drive loop, phase-locked loop (PLL) for clock generation, and high-voltage circuits for electrostatic excitation and high-voltage detection. The interface is implemented in a 0.35-μm high-voltage technology within an active area of 2.5 mm^2. The gyroscope achieves a spot noise of 0.015 $^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$ for the x-axis and 0.041 $^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$ for the y-axis.

Coherent demodulation and discrete-time signal processing are often an important part of the sensors and also typical examples that require clock signals. Thus, clock generation within the sensor interfaces is also reviewed. The related experimental work includes two integrated charge pump PLLs, which are optimized for compact realization but also considered with regard to their noise performance. Finally, this thesis discusses fully integrated high-voltage generation, which allows a higher electrostatic force and signal current in capacitive sensors. Open- and closed-loop Dickson charge pumps and high-voltage amplifiers have been realized fully on-chip, with the focus being on optimizing the chip area and on generating precise spurious free high-voltage signals up to 27 V.

Keywords Capacitive sensor, CMOS, MEMS, accelerometer, gyroscope, charge pump, PLL

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Integroitua rajapintaelektroniikkaa kapasitiivisille MEMS inertia-antureille

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Tiivistelmä

Tämä väitöskirja koostuu 13 julkaisusta sekä tutkimusaiheen yhteenvedosta. Väitöskirjassa esitetty tutkimus käsittelee integroitua elektroniikkaa, jolla voidaan toteuttaa kapasitiivisten MEMS (mikroelektromekaaninen järjestelmä) inertia-anturien, eli kiihtyvyys- ja kulmanopeusanturien, vaatima elektroninen rajapinta. Tutkimus keskittyy kapasitiivisen lukemisen ja käytön mahdollistaviin piirirakenteisiin sekä korkeajännite- ja kellosignaalien tuottamiseen osana mikroelektronista anturirajapintaa.

Väitöskirjassa esitellään elektroniikkaa, jolla kapasitiivinen informaatio voidaan lukea niin avoimen kuin suljetun silmukan kiihtyvyys- ja kulmanopeusantureissa, sekä yhteenveto antureiden ominaisuuksista. Kokeellisen työn ensimmäinen osa, kiihtyvyysanturi, on toteutettu jatkuva-aikaisena suljetun silmukan rakenteena ja se pystyy havainnoimaan alle mikro-g:n luokkaa olevia kiihtyvyyksiä. Elektroniikka on toteutettu 0.7 μm:n korkeajänniteteknologialla ja se sisältää suljetun silmukan elektroniikan, kellopiirit sekä analogia-digitaalimuuntimen. Toisessa kokeellisen työn osassa esitellään analoginen 2-akselinen kulmanopeusanturi, joka on optimoitu kohinan ja lisäksi erityisesti tehonkulutuksen sekä pinta-alan suhteen. Toteutus sisältää pseudo-jatkuva-aikaisen elektroniikan kulmanopeusinformaation lukemiseksi, analogisen ajosilmukan ja vaihelukitun silmukan (PLL) kellonsignaalin tuottamiseksi. Toteutukseen sisältyy myös korkeajännite-elektroniikkaa sähköstaattisen herätteen ja anturilta saatavan signaalinvirran voimistamiseksi. Anturin rajapinta on toteutettu 0.35 μm:n korkeajänniteteknologialla ja sen pinta-ala on 2.5 mm^2. Anturi saavuttaa kohinatiheyden 0.015 $^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$ x-akselille sekä 0.041 $^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$ y-akselille.

Koska esimerkiksi koherenttia detektiota ja diskreettiaikaista signaalinkäsittelyä sovelletaan usein antureissa, väitöskirjassa tarkastellaan myös kellosignaalin tuottamista. Aiheeseen liittyvä kokeellinen työ sisältää kaksi integroitua varauspumppu-PLL-piiriä, jotka on optimoitu pinta-alan suhteen ja tarkasteltu myös vaihekohinan osalta. Väitöskirjassa on esitelty myös korkeajännitteen tuottaminen mikropiirillä, mikä mahdollistaa sekä sähköstaattisen säädön että kapasitiivisen signaalin lukemisen tehostamisen. Avoimen ja suljetun silmukan Dickson-varauspumput sekä korkeajännitevahvistimet on toteutettu täysin integroituna ja optimoitu pinta-alan suhteen siten, että tarkkojen korkeajännitesignaalien tuottaminen onnistuu aina 27 V asti.

Asiasanat Kapasitiivinen anturi, CMOS, MEMS, kiihtyvyysanturi, kulmanopeusanturi, varauspumppu, PLL

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Preface

The work reported in this thesis was carried out in the Electronic Circuit Design Laboratory, Helsinki University of Technology (currently part of Aalto University, which was established in 2010), Espoo, Finland, during the years 2004-2010. The research work was funded by VTI Technologies, Vantaa, Finland, by the Finnish Funding Agency for Technology and Innovation (TEKES), first in the project "Integration of Radiocommunication Circuits" (RADINT) and later in other research projects, and by the Academy of Finland under the Centre of Excellence program (SMARAD2). The work was also supported by the Graduate School of Electrical and Communications Engineering, by the Nokia Foundation, by the Finnish Foundation for Technology Promotion (TES), and by the Jenny and Antti Wihuri Foundation. I want to thank all the financiers. In addition, I want to acknowledge VTI Technologies for providing the sensor elements.

I would like to thank my supervisor, Professor Kari Halonen, for the chance to work in the laboratory and for the interesting research topic in which I had a great opportunity to immerse myself. I am also grateful for the chance to carry out the research work very independently. Professor Haluk Külah from the Middle East Technical University, Ankara, Turkey and Professor Michael Kraft from the University of Southampton, Southampton, United Kingdom are acknowledged for reviewing this thesis and for their valuable remarks and suggestions.

I would also like to thank Dr. Teemu Salo, Mr. Teemu Elo, Mr. Kimmo Törmälehto, and Mr. Tero Sillanpää from VTI Technologies for the valuable discussions regarding the research topic, and for their comments both on the research work and on the publications.

The work at the Electronic Circuit Design Laboratory has been both intense and relaxed at the same time. I am grateful to my colleagues for creating this great atmosphere. In particular, I want to thank my present and former colleagues who also worked with sensors. First I want to thank Dr. Mikko Saukoski, with whom I started my work at the laboratory. With Mikko it was always possible to share ideas and he was indispensable in pointing out and solving errors and problems on countless occasions. Mikko is also a coauthor of many of the publications and he greatly helped in improving the quality of these papers. I also want to thank Pasi Rahikkala, Mikail Yücetas, Timo Speeti, Jarno Salomaa, Mika Pulkkinen, Jakub Gronicz, Jakub Bruzdzinski, Antti Kalanti, Sanna Heikkinen and Dr. Marko Kosunen for their contributions to the same sensor projects as I have been working with. Additionally, I want to thank Mika Kämäräinen, Matti Paavola, Väinö Hakkarainen, Dr. Mika Laiho, and Jonne Lindeberg for our many discussions, both on and off the research topic, as well as for the leisure activities. My former room-mates in work room I313b, Dr. Ilari Teikari, Dr. Johan Sommarek, and Dr. Olli Väänänen deserve thanks for introducing me to the proper way to do research. I also wish to thank

the secretaries, Helena Yllö, Anja Meuronen, and Lea Söderman, who made it possible to solve practical issues smoothly.

I want to warmly thank my parents Raimo and Lea for the support they have always given me. I am also deeply thankful to my sweet wife Iina for bringing essential contents to my life. Despite my heavy workload, you have made it possible for me to complete this thesis, and at the same time, to be together with my son Valto and follow his first steps in this world, allowing me to have those memories that are most valuable to me.

In Espoo, Finland,
August 30, 2010.

Lasse Aaltonen

Contents

List of Publications

This thesis consists of an overview and of the following publications which are referred to in the text by their Roman numerals.

I L. Aaltonen, P. Rahikkala, M. Saukoski, and K. Halonen, "High-resolution continuous-time interface for micromachined capacitive accelerometer," *Int. J. Circ. Theor. Appl.*, vol. 37, no. 2, pp. 333–349, Mar. 2009.

II L. Aaltonen and K. Halonen, "Continuous-time interface for a micromachined capacitive accelerometer with NEA of 4μg and bandwidth of 300Hz," *Sens. Actuators A*, vol. 154, no. 1, pp. 46–56, Aug. 2009.

III L. Aaltonen and K. Halonen, "High resolution analog-to-digital converter for low-frequency high-voltage signals," in *Proc. Int. Conf. Electronics Circuits and Systems*, St. Julian's, Malta, Sept. 2008, pp. 1245–1248.

IV L. Aaltonen and K. Halonen, "Integrated high-voltage PID controller," in *Proc. Baltic Electronics Conf.*, Tallinn, Estonia, Oct. 2008, pp. 125–126.

V L. Aaltonen, T. Speeti, M. Saukoski, and K. Halonen, "An interface for a 300°/s capacitive 2-axis micro-gyroscope with pseudo-CT readout," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, San Francisco, CA, USA, Feb. 2009, pp. 344–345.

VI L. Aaltonen and K. Halonen, "Pseudo-continuous-time readout circuit for a $300^\circ/s$ capacitive 2-axis micro-gyroscope," *IEEE J. Solid-State Circuits*, vol. 44, no. 12, pp. 3609–3620, Dec. 2009.

VII L. Aaltonen and K. A. I. Halonen, "An analog drive loop for a capacitive MEMS gyroscope," *Analog Integrated Circuits and Signal Processing*, vol. 63, no. 3, pp. 465–476, June 2010.

VIII L. Aaltonen and K. Halonen, "On-chip charge-pump with continuous frequency regulation for precision high-voltage generation," in *Proc. IEEE Prime '09*, Cork, Ireland, July 2009, pp. 68–71.

IX T. Speeti, L. Aaltonen, and K. Halonen, "Integrated charge-pump phase-locked loop with SC-loop filter for capacitive microsensor readout," in *Proc. IEEE Int. Symp. Circuits Syst.*, Taipei, Taiwan, May 2009, pp. 1373–1376.

X L. Aaltonen, M. Saukoski, and K. Halonen, "Design of clock generating fully integrated PLL using low frequency reference signal," in *Proc. Eur. Conf. on Circuit Theory and Design*, Cork, Ireland, Aug. 2005, pp. 161–164.

XI L. Aaltonen, M. Saukoski, I. Teikari, and K. Halonen, “Noise analysis of comparator performed sine-to-square conversion,” in *Proc. Baltic Electronics Conf.*, Tallinn, Estonia, Oct. 2006, pp. 103–106.

XII L. Aaltonen, M. Saukoski, and K. Halonen, “On-chip digitally tunable high voltage generator for electrostatic control of micromechanical devices,” in *Proc. IEEE Custom Integrated Circuits Conf.*, San Jose, CA, USA, Sept. 2006, pp. 583–586.

XIII L. Aaltonen, M. Saukoski, and K. Halonen, “Fully integrated charge pump for high-voltage excitation of a bulk micromachined gyroscope,” in *Proc. IEEE Int. Symp. Circuits Syst.*, Kobe, Japan, May 2005, pp. 5381–5384.

Author's Contribution

The contribution of the author to the publications [I-XIII] is examined in this section. In general, Kari Halonen acted as the supervisor of all the work done.

In [I] the author was responsible for the system-level design, most of the circuit-level design, and writing the manuscript. Pasi Rahikkala designed the GmC oscillator and the buffer for the carrier, while the author was involved as an instructor and provided the design specifications for the oscillator. Mikko Saukoski participated on commenting the manuscript, and contributed to the design by drawing the layout of the low-pass filter.

In [II], which reports the upgraded version of the design in [I], the author is responsible for the manuscript and for upgrading the design.

In [III], which reports the design of the digitizer in [II], the author is responsible for the design and the manuscript.

In [IV], which reports the design of the controller in [II], the author is responsible for the design and the manuscript.

In [V] the author is responsible for the system-level design, most of the circuit-level design and writing the manuscript. Timo Speeti designed the phase-locked loop, for which the system-level ideas, including the switched-capacitor loop filter, and design specifications, were provided by the author, who was also involved as an instructor. Together with Mikko Saukoski, the author developed the initial ideas for the pseudo-continuous-time readout.

In [VI], which reports the detailed sense readout in [V], the author is responsible for the implementation and the manuscript.

In [VII], which reports the drive loop in [V], the author is responsible for the design and the manuscript.

In [VIII], which reports the charge pump in [V], the author is responsible for the design and the manuscript.

In [IX], which reports the design of the phase-locked loop in [V], Timo Speeti designed the phase-locked loop, for which the system-level ideas including the switched-capacitor

loop filter, and design specifications were provided by the author, who was also involved as an instructor. The manuscript was written by Timo Speeti and revised by the author.

In [X] the author was responsible for the circuit-level design and writing the manuscript. Mikko Saukoski was involved in commenting on the manuscript and was responsible for the design of the system, which included the circuit in [X]. The measured results of [X] are reported in Section 4.3.

In [XI] the author was responsible for the analysis and writing the manuscript. Mikko Saukoski was involved in commenting on the manuscript and Ilari Teikari provided assistance with the related math. The theoretical results in [X] are compared with the measured results in Section 4.3.

In [XII] and [XIII] the author was responsible for the design and writing the manuscripts. Mikko Saukoski was involved in commenting on the manuscripts and was responsible for the design of the system, which included the devices reported in [XII] and [XIII].

Symbols and Abbreviations

β	Parameter defining the sidelobe attenuation in a Fourier transform of the Kaiser window
ΔC	Signal part of a sensor capacitance
Δf	Frequency offset
ΔT	Measurement time
ϵ_0	Permittivity of vacuum, $8.8542 \cdot 10^{-12}\ \mathrm{F/m}$
η	Power efficiency, P_{out}/P_{in}
∞	Infinite
$\mathcal{L}(\Delta f)$	Phase noise, relative SSB phase noise power at Δf
$\Delta\Sigma$	Delta-Sigma, refers to quantization noise shaping properties of data converters or modulators
ω	Angular frequency, $\omega = 2\pi f$
ω_c	Carrier frequency, $\omega_c = 2\pi f_c$, in a vibratory gyroscope typically $\omega_c = \omega_{0d}$
ω_0	Resonance frequency, $\omega_0 = \sqrt{k_x/m}$
ω_{det_ac}	Frequency of the ac detection voltage V_{det_ac}, $\omega_{det\_ac} = 2\pi f_{det\_ac}$
ω_{sa}	Sampling frequency, $\omega_{sa} = 2\pi f_{sa}$
Ω_z	Angular velocity about the z-axis
$\overline{\Omega}, \Omega$	Angular velocity
$\overline{\phi}$	Symbol for an inverted clock phase, $\overline{\phi} = \mathrm{NOT}\phi$
$\overline{a_m}$	Acceleration of a body with respect to the inertial system, $\overline{a_m} = d^2\overline{r_m}/dt^2$
$\overline{a_r}$	Acceleration of the origin of a reference system with respect to the inertial system, $\overline{a_r} = d^2\overline{r_r}/dt^2$
$\overline{a_{cor}}$	Coriolis acceleration
$\overline{a_{mr}}$	Acceleration of a body with respect to the reference system, $\overline{a_{mr}} = d^2\overline{r_{mr}}/dt^2$
$\overline{F}, F$	Force

$\overline{i}, \overline{j}, \overline{k}$	Unit vectors in the direction of x_1- ,y_1- and z_1-axis, respectively
$\overline{r_m}$	Position vector for a body with respect to the inertial system
$\overline{r_r}$	Position vector of the origin of a reference system with respect to the inertial system
$\overline{r_{mr}}$	Position vector for a body with respect to a reference system
ϕ	Symbol for a clock phase; Phase
ϕ_d	Phase shift inflicted by TIA at ω_{det_ac}
ϕ_e	Phase error
$\phi_n(t)$	Fluctuating phase, phase noise in the time domain
ϕ_{in}	PLL input (reference) phase
ϕ_{out}	PLL output phase
ϕ_{VCO_pn}	Noise at the output of a VCO, phase noise
σ_{abs}	Absolute jitter
σ_{jper}	Period jitter
τ	Pulse length
τ_p	Time constant of a single pole LPF, the corresponding pole frequency is equal to $f = 1/(2\pi\tau_p)$
A	Area
a	Acceleration
A_V	Voltage gain of an amplifier
a_x	Acceleration in the x-direction, $a_x = d^2x/dt^2$
a_y	Acceleration in the y-direction, $a_y = d^2y/dt^2$
$A_{x\_\omega c}$	Oscillation amplitude of a 2-DoF resonator in the x-direction
B	Sample of a bit stream
B_{ave}	Average value of a bit stream
C	Capacitance
c	Effective contribution of white noise sources to the phase noise
C_0	Static part of a sensor capacitance

c_f	Effective contribution of flicker noise sources to the phase noise
C_p	Parasitic capacitance
C_s	Sensor capacitance
C_A	The differential capacitance in an integrated capacitor, capacitance per stage in a charge pump
C_{BP}	Parasitic capacitance accociated with the bottom plate of an integrated capacitor
C_{fb}	Feedback capacitance
C_{TP}	Parasitic capacitance accociated with the top plate of an integrated capacitor
D	Symbol for a diode; Damping coefficient
D_x, D_{xx}	Damping coefficient in the x-direction
D_{out}	Digital output
D_{xy}, D_{yx}	Magnitude of nonproportional damping in a 2-DoF resonator
D_{yy}	Damping coefficient in the y-direction
E_c	Energy stored in a capacitor
E_{tot}	Total energy stored in a system
f	Frequency
f_0	Constant (average) frequency, center frequency
f_c	Carrier frequency
f_s	Signal frequency
f_{CP}	Clock (pumping) frequency in a charge pump
f_{det_ac}	Frequency of the ac detection voltage V_{det_ac}
F_{es}	Electrostatic force
F_{ext_n}	Mechanical noise force in a 1-DoF system
F_{ext_x}, F_{ext_y}	Total external force in the x- and y-direction
F_{ext}	Overall external force in a 1-DoF system
F_{i_x}, F_{i_y}	Force due to acceleration in the x- and y-direction

F_i	Force due to acceleration in a 1-DoF system
F_{net_x}, F_{net_y}	Total force in the x- and y-direction
F_{net}	Overall force, $F_{net} = F_i + F_{ext}$
f_{s_max}	Maximum signal frequency
f_{sa}	Sample rate, sampling frequency, $f_{sa} = 1/T_{sa}$
f_{sbw}	Signal bandwidth
F_{spr}	Spring force
G	Constant gain
G_T	Gain from acceleration to force, for micromechanical sensors $G_T = m$
G_R	Gain from (proof mass) position to voltage, comprises G_{T2} and the constant gain of the readout
G_{T2}	Gain from (proof mass) position to capacitance
G_{T3}	Gain from voltage to (electrostatic) force
h	Height of a plate capacitor; Height of fingers in a comb capacitor
$H_{C/F}$	Transfer function from force (e.g. induced by acceleration) to capacitance in a capacitive sensor
$H_{LF}(z)$	Transfer function of a loop filter in the z-domain
H_{RES}	Transfer function of a resonator
H_R	Transfer function of the electronic interface
$H_{sinc\_\tau}(s)$	Sinc-TF in Laplace domain
H_S	Transfer function of the complete electromechanical sensor
I	Current
I_0	Bias current (dc)
I_s	Signal current through a capacitive interface
I_{HH}	Load current of a charge pump
I_{leak}	Leakage current
I_{out}	Output current

I_Z	Input to a loop filter of a PLL
k_B	Boltzmann constant, $1.38065 \cdot 10^{-23}$ J/K
k_e	Electric spring constant
k_{xx}	Mechanical spring constant in the x-direction
k_{xy}, k_{yx}	Magnitude of anisoelasticity in a 2-DoF resonator
k_x	Mechanical spring constant
k_{yy}	Mechanical spring constant in the y-direction
M	Symbol for MOSFETs
m	Mass
M_{fb}	Feedback MOSFET for the realization of dc feedback
m_{frame}	Mass of the reference frame
m_x	Vibrating mass in the x-direction
m_y	Vibrating mass in the y-direction, $m_y = m_x + m_{frame}$
N	Number of stages in a charge pump; Division ratio in a PLL
n, r	Variable integer
n_0	Constant integer
N_B	Number of bits, word length
N_Q	Quantization noise
N_{sa}	Number of samples
P	Power
Q	Quality factor, $Q = \sqrt{k_x m}/D$; Charge; Symbol for bipolar transistors
q	Elementary charge, $1.60218 \cdot 10^{-19}$ C
R	Resistance
r_1, r_2, r_3	Scalar terms for defining the vector $\overline{r_{mr}}$ in the direction of of x_1- ,y_1- and z_1-axis, respectively
R_{bias}	Resistor for dc biasing
R_{fb}	Feedback resistance

s	Frequency variable in Laplace domain
$S/N_L(\Delta f)$	Relative SSB noise power at offset Δf from the center frequency of a sampled sine
$S_\phi(f)$	Frequency domain representation of $\phi_n(t)$
$s_{ct}(t), S_{ct}(s)$	Continuous-time signal in time and Laplace domains
$s_{pt}(t), S_{pt}(s)$	Impulse train in time and Laplace domains
$s_{sah}(t), S_{sah}(s)$	Continuous-time sample-and-hold signal in time and Laplace domains
SW	Symbol for switches
T	Absolute temperature
T_{sa}	Sampling period, time between two successive samples
V	Voltage
V_a, V_{as}	Amplitude of a sinusoidal signal
V_D	Voltage across a conducting diode
V_m	Bias voltage (dc), partly defines V_{det}
V_n	Voltage density of white noise
$V_n(t)$	Noise voltage in the time domain
$V_s(t)$	Sinusoidal signal with amplitude V_{as} and frequency f_s in the time domain
V_T	Thermal voltage, 25.9 mV at 300 K
v_x	Velocity in the x-direction, $v_x = dx/dt$
v_y	Velocity in the y-direction, $v_y = dy/dt$
V_{bias}	Bias voltage (dc)
V_{DD}	Positive supply voltage
V_{det_ac}	Voltage (ac) used for the detection of a capacitive signal, ac detection voltage
V_{det}	Voltage (dc) used for the detection of a capacitive signal, dc detection voltage
V_{HH}	Output voltage of a charge pump
V_H	Hysteresis voltage

V_{incm}	Input common-mode voltage
V_{in}	Input voltage
V_{m_ac}	Bias voltage (ac), partly defines V_{det_ac}
$V_{n\_rms}, V_{n\_rms\_out}$	Noise voltage, rms
V_{n_sa}	Voltage density of white noise after sampling
V_{nf}	Flicker-noise voltage, also known as $1/f$-noise voltage, or pink noise voltage
$V_{osc}(t)$	Sinusoidal signal with amplitude V_a and frequency f_0
V_{out_filt}	LP filtered output voltage
V_{out}	Output voltage
V_{ref}	Reference voltage
V_{VCO}	Input to a VCO
w	Width of a plate capacitor
w_0	Nominal overlap of the fingers in a comb capacitor
x	Position of a body with respect to a reference system in the x-direction; Position, displacement
x_0	Nominal spacing between capacitor electrodes; Coordinate axis in the inertial system
x_0, y_0, z_0	The three coordinate axes in the inertial system
x_1, y_1, z_1	The three coordinate axes in a reference system
x_m	Position of a body with respect to the 1-DoF inertial system
x_r	Position of the reference system with respect to the 1-DoF inertial system
y	Position of a body with respect to a reference system in the y-direction
Z	Impedance
z	Frequency variable in z-domain, $z = e^{j\omega T_{sa}}$ when determining the frequency response of a z-domain system
Z_{fb}	Feedback impedance
1-DoF	One-Degree-of-Freedom

2-DoF	Two-Degree-of-Freedom
ABS	Automatic Braking System
ac	Alternating Current
ADC	Analog-to-Digital Converter
ADPLL	All Digital Phase-Locked Loop
AlN	Aluminium Nitride
ASIC	Application Specific Integrated Circuit
BP	Band-Pass
CDS	Correlated Double Sampling
CM	Common-Mode
CMOS	Complementary Metal-Oxide-Semiconductor
CSA	Charge Sensitive Amplifier, transcapacitance amplifier
CT	Continuous-Time
DAC	Digital-to-Analog Converter
dc	Direct Current
DCO	Digitally-Controlled Oscillator
DPLL	Digital Phase-Locked Loop
DT	Discrete-Time
EM	ElectroMechanical
EMI	ElectroMagnetic Interference
ESC	Electronic Stability Control
ESD	ElectroStatic Discharge
FFT	Fast Fourier Transformation
FS	Full-Scale
GmC	Transconductance-Capacitor
HDL	Hardware Description Language
HPF	High-Pass Filter

HV	High-Voltage
IC	Integrated Circuit
LC	Inductance-Capacitor
LP	Low-Pass
LPF	Low-Pass Filter
MEMS	Micro-Electro-Mechanical System
MM	Mode-Matched
MNOS	Metal-Nitride-Oxide-Semiconductor
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
NMOS	N-channel MOS transistor
NTF	Noise Transfer Function
OSR	OverSampling Ratio
PD	Proportional-Derivative
PDM	Pulse-Density Modulation
PFD	Phase-Frequency Detector
PLL	Phase-Locked Loop
PMOS	P-channel MOS transistor
PSRR	Power Supply Rejection Ratio
PWM	Pulse-Width Modulation
PZT	Lead Zirconium Titanate
RC	Resistor-Capacitor
rms	Root Mean Square
RTZ	Return to Zero
S/H	Sample-and-Hold
SC	Switched-Capacitor
SI	Switched-Current

SNR	Signal-to-Noise Ratio
SOI	Silicon-on-Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
SQNR	Signal-to-Quantization Noise Ratio
SSB	Single SideBand
STF	Signal Transfer Function
TF	Transfer Function
TIA	TransImpedance Amplifier
TRA	TransResistance Amplifier
VCO	Voltage-Controlled Oscillator

1 Introduction

1.1 Background

MEMS is the commonly used acronym for microelectromechanical systems, and refers to miniature devices combining both electrical and mechanical components. Despite the definition, MEMS is also sometimes used to refer to purely micromechanical components. In general MEMS devices possess features on a micrometer scale and aim to combine multiple functions into a system with total dimensions that are typically smaller than a few millimeters.

The success and versatility of electronics in general was first made possible by the invention of the transistor at Bell Research Laboratories [1] in 1947, and further by that of the integrated circuit (IC) at Texas Instruments [2] and at Fairchild Semiconductor [3] in 1958. The technology for producing ICs also formed the basis for the development of MEMS. The research in the field was driven by the new possibilities that micromachined silicon devices brought, including compatibility with IC technology and the properties of silicon as a mechanical material [4]. The adaptation of IC technology also meant that batch fabrication techniques were available for the micromechanical components. The automotive, medical, and aerospace industries benefited from the smaller size, lower cost, and higher reliability offered by silicon-based microdevices when compared with the old macroscopical systems. The demand allowed the production volumes and related revenues for the microsensors to increase. The mass fabrication of miniature silicon-based pressure sensors and accelerometers could be seen by the end of the ’80s [5].

The readout of the mechanical information, further processing of the signal obtained from the mechanical device, and different calibration and compensation schemes contributed to the development of dedicated integrated interface circuits and complete MEMS devices. In fact the term MEMS was not introduced until 1987 [6]. The complete MEMS, including the mechanical element and dedicated electronic interface, also eased the spread of the MEMS technology into new application areas. The fact that the performance and accessibility of the complete MEMS device is often largely dictated by the electronic interface has maintained the interest of related research for more than two decades now.

Currently the MEMS market is dominated by inkjet printer heads, pressure sensors, inertial sensors, optical devices, including digital microdisplays, and microphones [7]. The market size, at present roughly 7 billion USD, has remained roughly flat from 2007 to the current date as a result of the economic downturn, but is expected to resume growth in 2011 [8]. The inertial sensor market, starting from accelerometers and extending to gyroscopes during roughly the last decade, forms approximately one quarter of the whole

MEMS market. This market share has been largely dominated by the automotive industry, where applications such as airbag control, automatic braking system (ABS), electronic stability control (ESC), and tilt detection, to mention but a few examples, require both accelerometers and gyroscopes. Recently, inertial sensors have been used increasingly [9] also in consumer electronics, which, in fact, is expected to start to dominate the inertial sensor market in 2011 [10]. Hard drive protection in laptops, control in game consoles, image stabilization in cameras, and orientation detection in cell phones are just a few common applications of this category.

1.2 Electronics and MEMS Inertial Sensors

Currently, the smallest commercial accelerometers [11, 12] are only roughly 4 mm^3 in volume. These tiny accelerometers, comprising a micromechanical sensor element and microelectronic interface, can offer not only straightforward digital access to acceleration information, but also acceleration information for three sensitive axes. It is clear that a dedicated IC, i.e. an application-specific integrated circuit (ASIC), is required for the realization of a compact and easily accessible interface for a mechanical sensor, as in the case of the miniature accelerometer.

An example of an interface ASIC for a capacitive micromachined vibratory gyroscope is shown in Fig. 1.1 [13]. The chip offers two analog angular velocity outputs, and requires only external bypass capacitance for the reduction of ripple in the supply voltage. Obviously, the optimization of the size of the ASIC is an important aspect in designing the electronics. However, effort is also put into meeting the requirements in terms of noise and power consumption.

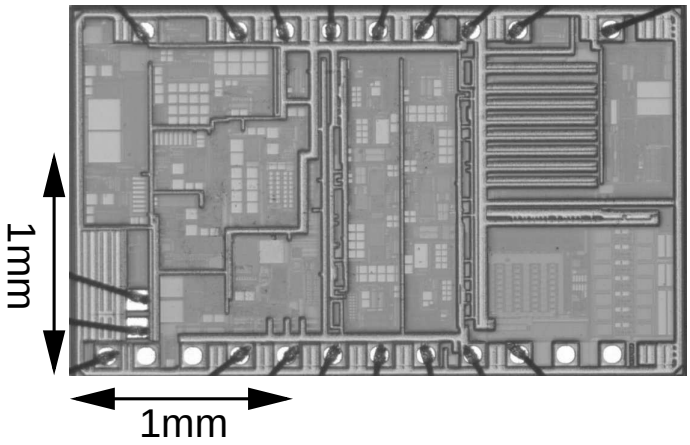

Figure 1.1: A microphotograph of an example ASIC, which realizes the complete analog interface for a 2-axis capacitive MEMS gyroscope [13].

Especially in capacitive sensors, where the sensor element is often low-noise, the electronic interface is an essential component in achieving high performance, also for the complete sensor. Low noise and low power is often a desired combination, especially in battery-powered systems, but is often difficult to realize in practice. Meeting the requirements in terms of, for example, maximized performance, minimized power consumption, or minimal chip area, or an optimal combination of all the three parameters, makes the design of the electronic interface a demanding task.

The development of interface electronics is addressed in this thesis with a focus on providing strong background information on different methods and auxiliary circuits for reading capacitive information and how the circuitry affects, for example, the performance, the supply current, and the chip area consumption. On-chip generation of local high voltages and clock signals using charge pumps and phase-locked loops are studied in order to identify how these circuits affect and potentially improve the operation of the capacitive sensors.

1.3 Organization of the Thesis

This thesis covers interface electronics for capacitive inertial microsensors, i.e. accelerometers and Coriolis vibratory gyroscopes. In this thesis the latter type of sensor is generally referred to as a gyroscope, unless otherwise explicitly stated. The first part of the thesis provides a comprehensive overview of the research topic. First, a general introduction to the electronics is provided in Section 2 by reviewing capacitive accelerometers and gyroscopes, and briefly also sensors based on other transduction mechanisms. The actual microelectronic open- and closed-loop interfaces for transforming the capacitive information into analog voltage or digital information are studied in Section 3 for both accelerometers and gyroscopes. In Section 4 the use of sinusoidal reference signals and phase-locked loops are examined for clock generation purposes, and, finally, fully integrated charge pump-based low-power high-voltage generation for capacitive interfaces is studied in Section 5.

The second part of the thesis comprises the published articles. The results of the research work including the theoretical and the experimental results are reported in these articles.

2 Micromachined Accelerometers and Gyroscopes

2.1 Theory of Operation

The inertial sensors measure the force affecting an inertial or proof mass resulting from acceleration. Detecting the magnitude and direction of the force, however, is not always a trivial matter, as the measurement must be made in the accelerating reference system without significantly affecting the operation of this system. If a reference system, such as a mobile phone, watch, or digital camera is considered, macroscopic sensors are usually out of the question. MEMS sensors, being minimal in size, can easily be taken advantage of without significantly affecting the size or operation of the device to be measured. In order to provide an understanding of the operation of an accelerometer or a gyroscope, the motion of a proof mass in an accelerating reference system, and with respect to an inertial system, is reviewed next [14].

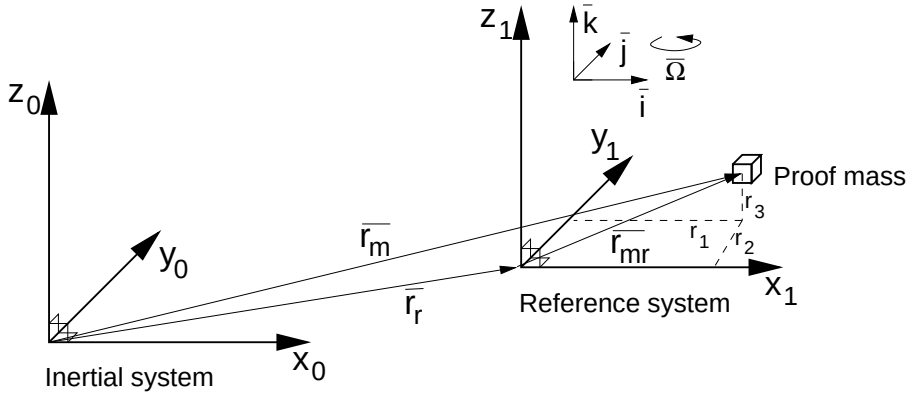

Figure 2.1: A proof mass located within a reference system that is moving arbitrarily with respect to an inertial system.

The inertial system in Fig. 2.1 is fixed or moving with a constant velocity. Newton's second law for a particle in an inertial system,

$$\overline{\Sigma F} = m\overline{a_m}, \tag{2.1}$$

states that a net force $\overline{\Sigma F}$ acting on a particle with mass m causes it to accelerate $\overline{a_m}$. Here the subindex m refers to the proof mass in the inertial system. The proof mass, which transforms the measured variable, i.e. the acceleration, into force, is located within a reference system. The vector expressing the location of the proof mass in the inertial system $\overline{r_m}$ is composed of a vector pointing to the origin of the reference system $\overline{r_r}$ and a vector pointing from the origin of the rotating reference system to the proof mass $\overline{r_{mr}}$. The latter of the two terms can be constructured using the unit vectors of the reference

system $\overline{i}$, $\overline{j}$, and $\overline{k}$, which change with time as a result of the rotation of the reference system, and proper scalar terms r_{1-3} to scale the unit vectors. The position $\overline{r_m}$ can thus be written as

$$\overline{r_m} = \overline{r_r} + \overline{r_{mr}} = \overline{r_r} + r_1\overline{i} + r_2\overline{j} + r_3\overline{k}. \tag{2.2}$$

If the reference system is assumed to be both rotating and in translational motion at the rate and direction given by $\overline{\Omega}$ and $d\overline{r_r}/dt$, respectively, the velocity of the mass in the inertial system can be written as

$$\frac{d\overline{r_m}}{dt} = \frac{d\overline{r_r}}{dt} + \frac{\partial\overline{r_{mr}}}{\partial t} + \overline{\Omega} \times \overline{r_{mr}}. \tag{2.3}$$

Here the first term is due to the velocity of the reference system, the second term to the motion of the proof mass in the reference system:

$$\frac{\partial\overline{r_{mr}}}{\partial t} = \frac{dr_1}{dt}\overline{i} + \frac{dr_2}{dt}\overline{j} + \frac{dr_3}{dt}\overline{k}, \tag{2.4}$$

whereas the last, third term is due to the rotation of the reference system about its origin. In order to find the acceleration of the proof mass in the inertial system, (2.3) must be differentiated one more time with respect to time, giving

$$\overline{a_m} = \frac{d^2\overline{r_m}}{dt^2} = \frac{d^2\overline{r_r}}{dt^2} + \frac{\partial^2\overline{r_{mr}}}{\partial t^2} + 2\overline{\Omega} \times \frac{\partial\overline{r_{mr}}}{\partial t} + \frac{d\overline{\Omega}}{dt} \times \overline{r_{mr}} + \overline{\Omega} \times \overline{\Omega} \times \overline{r_{mr}}. \tag{2.5}$$

It is also interesting to find the acceleration of the proof mass in the reference system, which is simply given as

$$\overline{a_{mr}} = \frac{\partial^2\overline{r_{mr}}}{\partial t^2} = \frac{\overline{\Sigma F}}{m} - \frac{d^2\overline{r_r}}{dt^2} - 2\overline{\Omega} \times \frac{\partial\overline{r_{mr}}}{\partial t} - \frac{d\overline{\Omega}}{dt} \times \overline{r_{mr}} - \overline{\Omega} \times \overline{\Omega} \times \overline{r_{mr}}, \tag{2.6}$$

where (2.1) was used. The first term is due to the acceleration of the mass in the inertial system a_m, the second due to the acceleration of the reference system a_r, the third is the Coriolis acceleration, the fourth is the acceleration created as a result of the changing rotation rate of the reference system (Euler acceleration), and the last term is the centrifugal acceleration. The significance of these terms in an accelerometer and gyroscope will be examined next.

2.2 Capacitive inertial sensors

In capacitive inertial sensors, the position of the proof mass in the reference system is measured by detecting a signal capacitance. The capacitance is formed between an electrode attached to the proof mass and a fixed electrode attached to the reference system. Hence, a change in the distance between the electrodes is converted to a change in the capacitance.

In general, the capacitive sensor element together with the electronic circuitry that measures the capacitance, can be designed for good dc response, a simple structure, and high sensitivity. The performance of the complete MEMS sensor can be optimized, for example, for low power and cost [15], in battery-operated or autonomous consumer applications, or for a very high resolution and dynamic range, for example, in seismic measurements [16]. The challenge related to capacitive interfaces is the sensitivity to electromagnetic interference (EMI), because of the high impedance of the capacitive sense nodes. This challenge is typically translated to the proper design of the interface, in order to prevent the cross-coupling of unwanted signals, and packaging, in order to shield the element and the interface from external disturbances.

2.2.1 Accelerometer

The operation of an accelerometer can be derived using the typical model for a single-axis accelerometer shown in Fig. 2.2, which is an ideal one-degree-of-freedom (1-DoF) resonator. If the parameter of interest for the accelerometer is the translational acceleration and motion only, it can be assumed that $\overline{\Omega} = d\overline{\Omega}/dt = 0$, when comparing Fig. 2.2 with the system in Fig. 2.1. In practice, accelerometers can be realized to detect translational accelerations with respect to any combination of the x-, y-, or z-axis and are referred to as single-, two-, or three-axis accelerometers depending on the number of axes measured. Three additional dimensions also exist for rotating motion, and the detection of all the components of angular acceleration, in addition to all the translational components, would result in a six-axis accelerometer. For the equation of motion that will be introduced next, a single-axis accelerometer is considered for the detection of translational acceleration only.

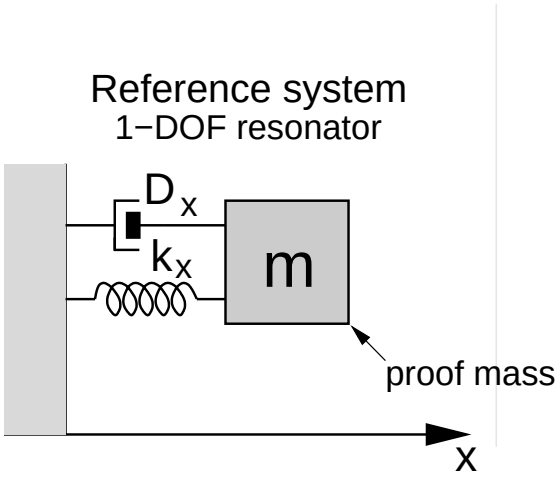

Figure 2.2: A linear 1-DoF resonator, which models a single-axis accelerometer. The variable x is the position of the proof mass in the reference system.

The proof mass is anchored to the reference system, typically via a compliant silicon beam, modeled in Fig. 2.2 as a linear spring with spring constant k_x. The spring force $F_{spr} = -xk_x$ acting on the proof mass is dependent on the negative position of the proof mass in the reference system. When comparing with the coordinate system in Fig. 2.1, this spacing corresponds to the position vector $\overline{r_{mr}}$. Since the resonator is a 1-DoF system, $\overline{i} \cdot \overline{r_{mr}}$ is replaced by x. Similarly, $\overline{i} \cdot \overline{r_r}$ and $\overline{i} \cdot \overline{r_m}$ are expressed as x_r and x_m, respectively. Now the position of the proof mass in the inertial frame is given as $x_m = x + x_r$.

In addition to the spring force, a force component that depends on the velocity dx/dt of the proof mass is always present. This force component is responsible for the energy lost in the resonator. The losses are due to, for example, material losses, anchor losses, mode conversion losses, and, especially, viscous losses, typically caused by any existing air damping [7]. The losses are modeled in the resonator in Fig. 2.2 as a dashpot damper with linear damping D_x. The resulting damping force is $F_{damp} = -D_x dx/dt$.

The proof mass of the sensor element accelerates in the inertial frame and hence the corresponding force is equal to (2.1) or $\Sigma F = md^2x_m/dt^2$, and can be calculated using (2.5). Now that the reference system is assumed to be in translational motion only, only the first two terms in (2.5) are considered. Hence, the sum of the forces affecting the proof mass can be written as

$$\begin{aligned} -F_{spr} - F_{damp} + \Sigma F &= F_{ext} \\ xk_x + \frac{dx}{dt}D_x + \left(\frac{d^2x}{dt^2} + \frac{d^2x_r}{dt^2}\right)m &= F_{ext}. \end{aligned} \tag{2.7}$$

The term F_{ext} depicts the total external force affecting the proof mass. If the force generated as a result of the acceleration of the reference system $-md^2x_r/dt^2$ is expressed as $F_i = -ma_r$, (2.7) can be rewritten as

$$F_{net} = F_i + F_{ext} = -ma_r + F_{ext} = xk_x + \frac{dx}{dt}D_x + \frac{d^2x}{dt^2}m. \tag{2.8}$$

The minus sign can be imagined by assuming that the reference system, for example a car where the accelerometer is placed, starts to accelerate with constant acceleration in the positive direction of x. The inertia of the sensor proof mass resists the acceleration, but the spring force makes the proof mass follow the reference system. The position of the mass in the reference system, however, remains negative, as the spring force compensates for the inertial force caused by the acceleration.

External forces, F_{ext}, typically affecting the proof mass in a capacitive sensor, include the electrostatic force, which is described in more detail in Section 2.3, and the mechanical noise. Gravitation-induced forces can also be included in F_{ext}. The *density* of the noise-inflicted force caused by thermal fluctuations [7], also referred to as *Brownian noise*, can be written as

$$F_{ext\_n} = \sqrt{4k_B T D_x}, \tag{2.9}$$

where k_B is the Bolztmann's constant and T the absolute temperature. By setting $|F_i| = F_{ext\_n}$ the equation can be solved for mechanical noise-equivalent acceleration,

$$a_{r\_n\_dens} = \frac{\sqrt{4k_BTD_x}}{m}. \tag{2.10}$$

Hence, the effect of mechanical noise is most efficiently reduced by using a larger proof mass, which is also a reason why Brownian noise is not an issue in macroscopic systems. In addition to the larger mass, the reduced damping also allows a smaller noise-equivalent acceleration.

From the electronics design point of view, it is feasible to write (2.8) in the Laplace domain. This allows the linear transfer function to be formed from the total force affecting the proof mass to the displacement of the proof mass,

$$H_{RES}(s) = \frac{x}{F_{net}} = \frac{1}{k_x + D_x s + ms^2}. \tag{2.11}$$

The second-order equation can be written in a general form as

$$H_{RES}(s) = \frac{1}{k_x} \frac{\omega_0^2}{\omega_0^2 + \frac{\omega_0}{Q}s + s^2}, \tag{2.12}$$

where the quality factor (Q-value) $Q = \omega_0 m/D_x$ and the natural frequency $\omega_0 = \sqrt{k_x/m}$.

2.2.2 Second-Order Transfer Function: Quality Factor

The quality factor is inversely proportional to the damping and hence offers a way to improve the inherent noise properties of the mechanical resonator. The increased Q-value also means a stronger response of the system at the resonance frequency. Thus, when the quality factor is increased, the dynamic behavior of the resonator also changes. This is depicted by the gain transfer functions, $|H_{RES}(j\omega)|$, in Fig. 2.3 and corresponding phase transfer functions, $\angle H_{RES}(j\omega)$, both plotted for a linear system, for which the Q-value is changed. The step responses for the same linear system are shown in Fig. 2.5.

For a device where the signal band starts from dc, such as a typical accelerometer, the increased quality factor increases the maximum gain of the device considerably. Although the signal band of interest can be limited below the resonance frequency, high out-of-band gain can still result in problems with linearity and tolerance of high-frequency interferers [7]. It is also evident that reducing the quality factor excessively will result in reduced bandwidth and increased noise. The same phenomena can also be observed in the time domain in Fig. 2.5. Now the high Q-value results in very slowly decaying ringing after the step response, and for the lowest quality factor the settling is also slowed down. In

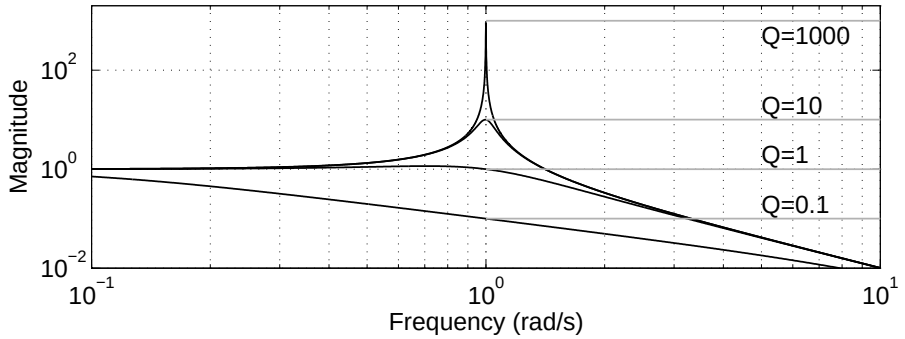

Figure 2.3: The effect of quality factor Q. The gain transfer functions are plotted for (2.12), where $\omega_0 = 1\ \mathrm{rad/s}$, $k_x = 1\ \mathrm{N/m}$ and $s = j\omega$.

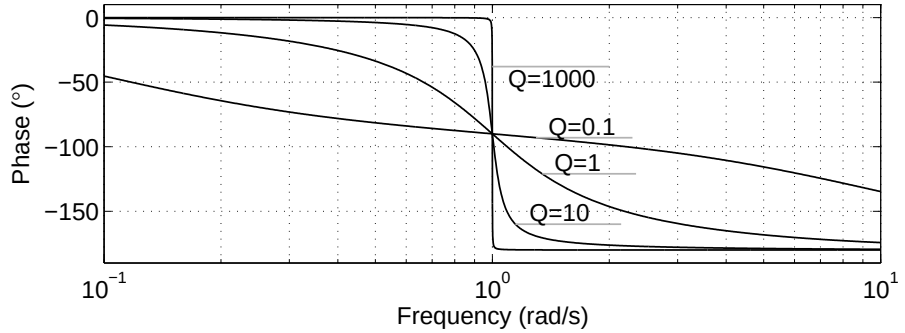

Figure 2.4: The effect of quality factor Q. The phase transfer functions are plotted for (2.12), where $\omega_0 = 1\ \mathrm{rad/s}$, $k_x = 1\ \mathrm{N/m}$ and $s = j\omega$.

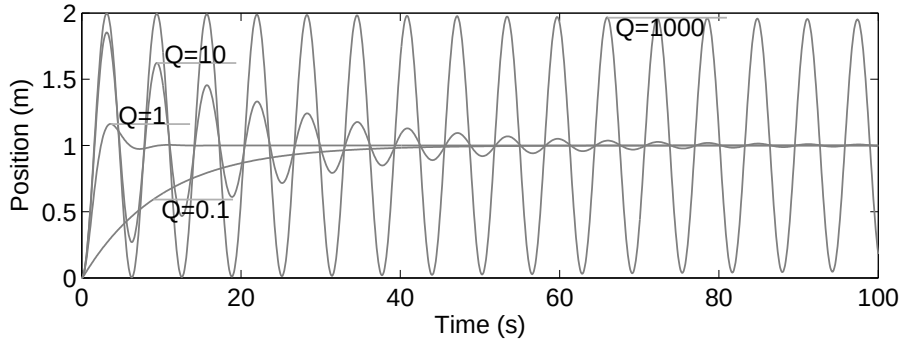

Figure 2.5: The step responses plotted for (2.12), where $\omega_0 = 1\ \mathrm{rad/s}$ and $k_x = 1\ \mathrm{N/m}$ and the quality factor Q has four different values.

fact the settling time, the time the system needs for settling to the final value with a predetermined precision, is at its minimum for a second-order system with $Q = 0.5$. For this Q-value the system is said to be *critically damped*. Similarly, for Q-values > 0.5 the system is *under-damped* and for Q-values < 0.5 *over-damped*.

2.2.3 Vibratory Gyroscope

A vibratory gyroscope measures the rotation of the reference system about its sensitive axis, or axes. Like accelerometers, a gyroscope can be realized to measure the rotation about one, two, or three axes. The example system in Fig. 2.6 models the operation of a gyroscope which detects the rotation about the z-axis. The reference system is now rotating about the z-axis at rate Ω_z. The inner mass of the system is capable of moving in the xy-plane and forms a two-degree-of-freedom (2-DoF) resonator.

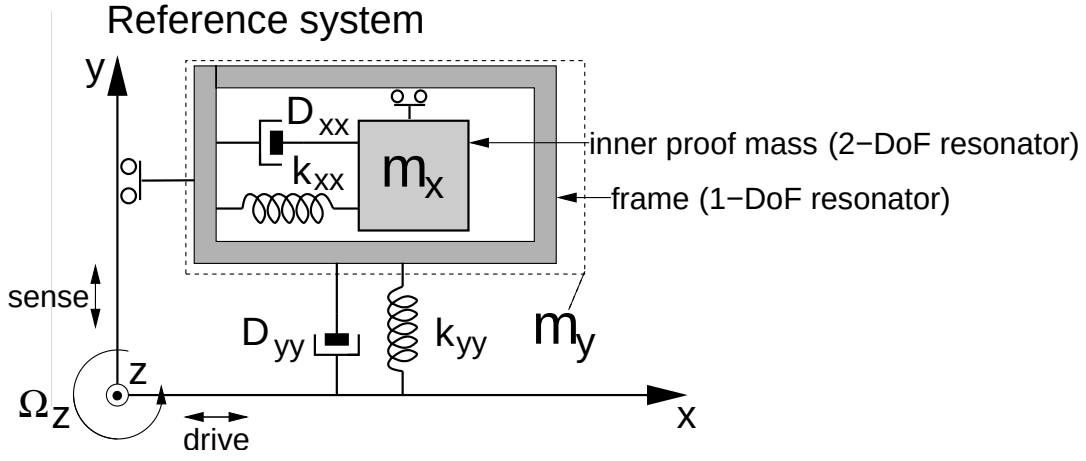

Figure 2.6: An ideal resonator system, which models a single-axis vibratory gyroscope. The mass m_y includes both the inner mass m_x and the mass of the frame m_{frame}.

The proof mass residing in the frame is free to move only in the x-direction with respect to the frame, whereas the frame, together with the inner mass, is limited to movement in the y-direction. The corresponding damping and spring constants for the two resonators are labeled as D_{xx} and k_{xx} in the direction of the x-axis, and D_{yy} and k_{yy} in the direction of the y-axis. The proof mass of the inner resonator is m_x, whereas the mass of the y-axis resonator m_y comprises both the frame m_{frame} and m_x. As in the case of an accelerometer, the x- and y-axes model the position of the proof mass in the reference system. When comparing the 2-DoF resonator with the coordinate system in Fig. 2.1, $x = \overline{i} \cdot \overline{r_{mr}}$ and $y = \overline{j} \cdot \overline{r_{mr}}$. The equation of motion for the 2-Dof system can be expressed as [17, 18]

$$\begin{aligned} &\begin{bmatrix} k_{xx} & k_{xy} \\ k_{yx} & k_{yy} \end{bmatrix} \begin{bmatrix} x \\ y \end{bmatrix} + \begin{bmatrix} D_{xx} & D_{xy} \\ D_{yx} & D_{yy} \end{bmatrix} \begin{bmatrix} v_x \\ v_y \end{bmatrix} + \begin{bmatrix} m_x & 0 \\ 0 & m_y \end{bmatrix} \begin{bmatrix} a_x \\ a_y \end{bmatrix} \\ &= \begin{bmatrix} F_{net\_x} \\ F_{net\_y} \end{bmatrix}, \end{aligned} \tag{2.13}$$

where $v_x = dx/dt$, $v_y = dy/dt$, $a_x = dv_x/dt$ and $a_y = dv_y/dt$. The forces F_{net_x} and F_{net_y} comprise the inertial forces , F_{i_x} and F_{i_y}, the proof masses experience as a result

of the acceleration of the reference system and the external forces, F_{ext_x} and F_{ext_y}, in the x- and y-directions respectively. The off-diagonal terms k_{yx}, k_{xy}, D_{xy}, and D_{yx} determine the magnitude of *anisoelasticity*, which results from mechanical imperfections, and *nonproportional damping* in a gyroscope [18].

Ideally the off-diagonal terms are zero, in which case both resonators behave like 1-DoF systems and the transfer functions can be written in the x-direction as

$$H_{RES\_x}(s) = \frac{x}{F_{net\_x}} = \frac{1}{k_{xx} + D_{xx}s + m_x s^2} = \frac{1}{k_{xx}} \frac{\omega_{0d}^2}{\omega_{0d}^2 + \frac{\omega_{0d}}{Q_d}s + s^2} \tag{2.14}$$

and in the y-direction as

$$H_{RES\_y}(s) = \frac{y}{F_{net\_y}} = \frac{1}{k_{yy} + D_{yy}s + m_y s^2} = \frac{1}{k_{yy}} \frac{\omega_{0s}^2}{\omega_{0s}^2 + \frac{\omega_{0s}}{Q_s}s + s^2}. \tag{2.15}$$

The position, velocity, and acceleration in the y-direction within the reference system are the same for the inner mass and the frame. The position and motion of the frame in the x-direction are zero. Now the frame is used for the detection of the Coriolis acceleration, and the inertial force component in the y-direction, F_{i_y}, can be solved using (2.5). The acceleration and force in the y-direction must be evaluated separately for the frame and the inner mass, as some force components in the y-direction depend on the motion in the x-direction. The force $F_{i\_y} = m_y a_y - (\overline{j} \cdot \overline{a_m}) m_{frame} - (\overline{j} \cdot \overline{a_m}) m_x$ can therefore be expressed as

$$F_{i\_y} = -m_y a_{r\_y} - 2m_x v_x \Omega_z - m_x x \frac{d\Omega_z}{dt} + m_y y \Omega_z^2. \tag{2.16}$$

In addition to the translational acceleration of the reference system $\overline{j} \cdot d^2\overline{r_r}/dt^2 = a_{r\_y}$, the rotation about the z-axis also contributes to F_{i_y} through the inner mass. The Coriolis force term being measured is in this case given as $-2m_x v_x \Omega_z$. The force is proportional not only to the rotation rate of interest Ω_z, but also to the velocity. Clearly the maximization of the Coriolis force requires the maximization of the velocity, in this case in the x-direction.

The resonator in Fig 2.6 is set to oscillate, driven, in the direction of the x-axis and the Coriolis force couples the vibration from the x-axis to the y-axis. We can now assume that the position of the x-axis resonator

$$x(t) = A_{x\_\omega c} \sin \omega_c t, \tag{2.17}$$

in which case the velocity

$$v_x(t) = A_{x\_\omega c} \omega_c \cos \omega_c t. \tag{2.18}$$

In order to maintain a constant gain from Ω_z to the Coriolis force

$$F_{i\_y\_cor} = -2m_x v_x \Omega_z = -2m_x \Omega_z A_{x\_\omega c} \omega_c \cos \omega_c t, \tag{2.19}$$

the amplitude of the velocity $A_{x\_\omega c}\omega_c$ in the x-direction should be constant. As expressed by (2.19), the Coriolis force appears as an amplitude-modulated signal in a vibratory gyroscope. The Coriolis force is detected by the accelerometer which the y-axis resonator forms. Because of the characteristic functionalities, the resonator that is set to oscillate is generally referred to as the *drive resonator* or *primary resonator*, whereas the accelerometer is referred to as the *sense resonator* or *secondary resonator*.

The Coriolis force is clearly just one of the components of the net force F_{net_y}, which comprises all the inertial forces defined in (2.16), and external forces including gravitation, electrostatic forces, and noise (2.9). All the additional force components can be considered as more or less significant perturbation terms, but nonetheless should not significantly affect the operation of the gyroscope. The effect of, for example, parasitic translational vibrations can be attenuated by selecting a sufficiently high ω_c to ensure that the spurious components will not contribute to the output of the gyroscope. The perturbation forces, however, can also become upconverted by the motion along the x-axis. For example, the term $-m_x x\frac{\Omega_z}{dt} = -m_x A_{x\_\omega c}\sin\omega_c t\frac{d\Omega_z}{dt}$ is proportional to the changing rotation rate and to the position in the direction of x-axis and hence appears at the drive frequency [19].

When considering the potential perturbation terms, it is also clear that the assumption of non-zero off-diagonal terms in (2.13) is not justified. Although the off-diagonal terms are in fact non-zero, they are typically small enough in order that (2.14) and (2.15) are valid with sufficient accuracy, and simply contribute to the net forces F_{net_x} and F_{net_y}. Now that the sense resonator is sensitive along the y-axis, the non-zero terms of interest are those contributing to F_{net_y}. Using (2.13), (2.17), and (2.18), the force component resulting from the off-diagonal terms can be written as

$$F_{par\_y} = -k_{yx}x - D_{yx}v_x = -k_{yx}A_{x\_\omega c}\sin\omega_c t - D_{yx}A_{x\_\omega c}\omega_c\cos\omega_c t. \tag{2.20}$$

If the net force F_{net_y} in (2.15) is assumed to be composed of merely F_{par_y} and $F_{i\_y\_cor}$, it can be written as

$$F_{net\_y} = -k_{yx}A_{x\_\omega c}\sin\omega_c t - (2m_x\Omega_z + D_{yx})A_{x\_\omega c}\omega_c\cos\omega_c t. \tag{2.21}$$

The k_{yx}- and D_{yx}-related parasitic force components or, in fact, any parasitic signal components in a vibratory gyroscope, at the same frequency as the motion along the driven axis, can be separated into two groups, the *in-phase* and *quadrature* components. The in-phase components are, as the term implies, in phase with the Coriolis signal, whereas the quadrature components possess a 90° phase difference when compared with the Coriolis signal. The *mechanical quadrature*, defined by k_{yx}, is typically the most significant contributor to quadrature signals [20]. More information about potential sources of parasitic signals can be found in [17], while their effect on the sensor output is studied in [21].

2.2.4 Resonance Frequencies and Operation of a Vibratory Gyroscope

In a second-order system, which both the resonators in a vibratory gyroscope also form, the gain at the resonance frequency is directly proportional to the Q-value of the system. Hence, the drive resonator in a capacitive gyroscope, where the magnitude of the electrostatic force is limited, is typically set to oscillate at the resonance frequency $\omega_c = \omega_{0d}$ and the Q-value is increased by operating the sensor element in a vacuum. If the mechanical properties, rather than the available excitation force, are limiting the oscillation amplitude, the excitation at the resonance frequency allows a minimal excitation voltage in any case and, therefore, reduced cross-coupling.

The design of the accelerometer, the sense resonator, depends on the desired separation of the resonance frequencies, ω_{0d} and ω_{0s}, of the drive and sense resonators, respectively. The operation of the gyroscope can be approximately divided into three regions: $\omega_{0d} \ll \omega_{0s}$, $\omega_{0d} < \omega_{0s}$ and $\omega_{0d} = \omega_{0s}$.

When $\omega_{0d} \ll \omega_{0s}$, the sense resonator operates in *low-pass mode*, where the gain is purely determined by the spring constant k_{yy}. The result can be obtained by setting $s = j\omega << \sqrt{k_{yy}/m_y}$ in (2.15) and assuming that the system is underdamped. In this region the phase shift from the signal, i.e. the Coriolis force, to the displacement is approximately zero, as is the sensitivity of the gain to varying Q-value.

As ω_{0s} is reduced and approaches ω_{0d}, but the condition $\omega_{0d} < \omega_{0s}$ is met, the *resonance gain* is taken advantage of while the gyroscope is still operating in the low-pass mode. The increase in gain, compared to operation in the region $\omega_{0d} \ll \omega_{0s}$, is equal to $\omega_{0s}^2/(\omega_{0s}^2 - \omega_{0d}^2)$, which is independent of the Q-value provided that it is high enough [22].

The third region corresponds to *mode-matched operation*, where the two resonance frequencies are equal. In this mode the high gain attained at the resonance is taken advantage of, as in the case of the drive resonator. If the resonances are exactly matched, the gain is higher by Q compared to operation in the mode $\omega_{0d} \ll \omega_{0s}$. However, the gain is very sensitive to even a slight mismatch between the resonances and directly proportional to the Q-value. In addition, in open loop the $-3dB$-signal band is limited to $\omega_{0s}/2/Q_s$. Because of these characteristic features, when the focus is on pursuing mode-match operation, active mode matching can be used to tune ω_{0s} to match with ω_{0d} and closed-loop operation to increase the signal bandwidth and to reduce the sensitivity to the Q-value [23]. At the expense of a somewhat more complex interface, noise performance is typically improved because of the stronger capacitive signal in a mode-matched gyroscope.

An example of the operating modes is depicted in Fig 2.7, where two frequency bands of 600 $\mathrm{rad/s}$ are plotted. The lower band (LP) corresponds to operation in low-pass mode with a resonance gain of about 6, whereas the upper one (MM) corresponds to a mode-

matched gyroscope. The gain and phase of the nominal transfer function, (2.15), are plotted with $\omega_{0s} = 80\,\mathrm{krad/s}$, $Q_s = 100$, and $k_{yy} = 1\,\mathrm{N/m}$. The parameter variations are marked in the figure. The absolute value of the gain is higher in the mode-matched case. However, the sensitivity of the gain is also high, making the use of an open-loop sensor problematic.

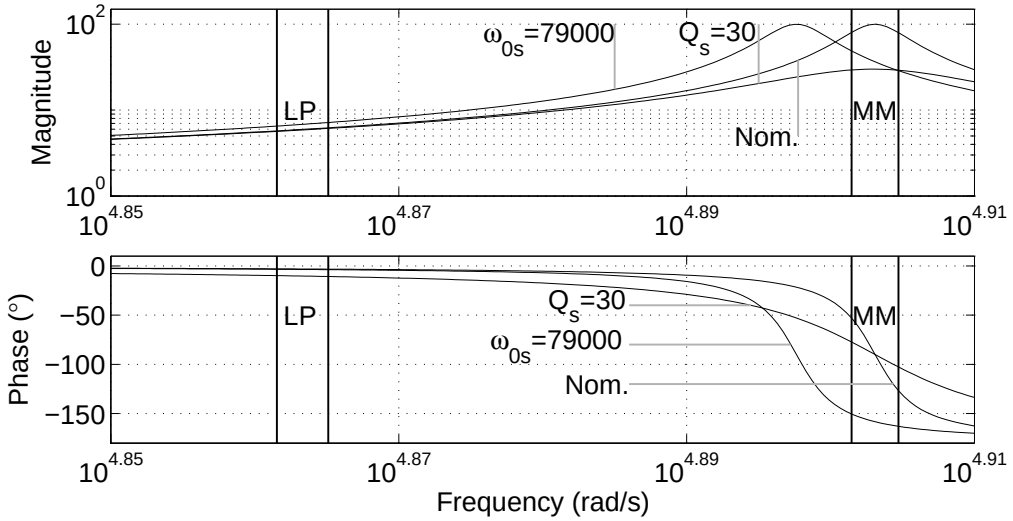

Figure 2.7: An example of varying sense resonator transfer function. The two regions labeled LP and MM correspond to low-pass operation and mode-matched operation, respectively.

2.3 Capacitive Actuation and Detection of Position

Capacitive interfaces are immensely pervasive, and are basically formed between any two isolated conductors. A capacitive interface can also be used for both detection and actuation. These features make capacitive interfaces versatile, but also set challenges: care must be taken that neither parasitic capacitive cross-coupling nor undesired electrostatic forces degrade the properties of the sensor.

The three main configurations for capacitive interfaces are shown in Fig. 2.8. In the figure, as in general, a single signal capacitor can be split between the static capacitance C_0, which usually dominates the total capacitance value, and the signal capacitance ΔC. The first interface configuration, the single variable capacitor shown in Fig. 2.8 (a), is created between a static electrode and a moving electrode attached to the proof mass of the resonator. When a second static electrode is added to form a second capacitor, in such a way that the sensitivity of the capacitance to the proof mass position is opposite compared to

the first capacitor, the differential half-bridge shown in Fig. 2.8 (b) is obtained. The differential full-bridge shown in Fig. 2.8 (c) requires four isolated electrodes, two of which lie in the moving structure. In addition to making possible the capacitive detection of position, each of the signal capacitors exerts an electrostatic force on the moving electrode, thus influencing the properties of the underlying mass-spring system. The electrostatic forces and the properties of the position-to-capacitance conversion will be studied in the next section.

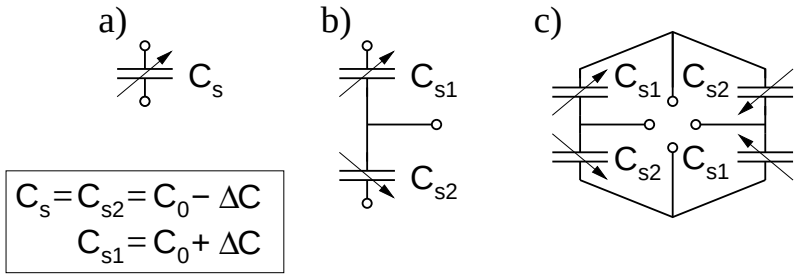

Figure 2.8: Different configurations for capacitive interfaces: a) single capacitor, b) capacitive half-bridge, and c) capacitive full-bridge.

2.3.1 Structure and Properties of Capacitive Interfaces

A parallel plate capacitor has high sensitivity from a change in the spacing between the capacitor plates to a change in the capacitance value. Therefore it is commonly used for the detection of position (displacement) in capacitive sensors. The structure of a parallel plate capacitor is depicted in Fig. 2.9. The moving plate, the rotor, is attached to the seismic element of the sensor, whereas the other plate, the stator, is stationary. The area of the plates is defined as $A = hw$, and the nominal spacing between the plates, x_0, changes as a function of the external signal that is applied. The variable x corresponds to the change in the gap. The plates of the capacitor are usually separated by air or a vacuum, while the permittivity of a vacuum, ϵ_0, can also be used to approximate the permittivity of air. When a voltage V is applied across the capacitor C_s, the amount of energy stored in the capacitor is equal to

$$E_c = \frac{C_s V^2}{2} = \frac{VQ}{2} = \frac{Q^2}{2C_s}, \tag{2.22}$$

where

$$C_s = \epsilon_0 A/(x_0 - x) \tag{2.23}$$

and Q is the charge of the capacitor. The effect of fringing fields is ignored. A non-zero voltage causes an electrostatic force, which attracts the plates of the capacitor. The force,

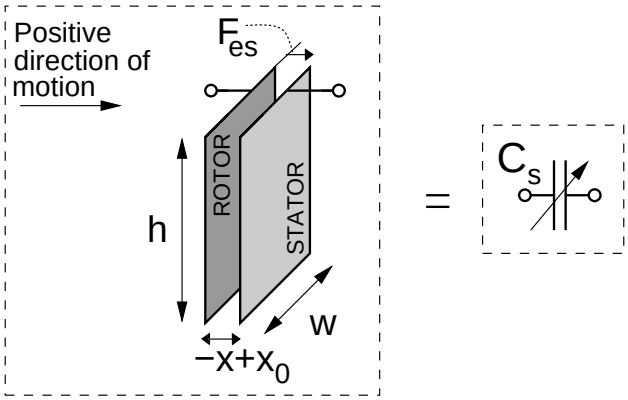

Figure 2.9: A parallel plate capacitor.

also marked in Fig. 2.9, is defined as

$$\begin{aligned} F_{es} &= -\frac{dE_{tot}}{dx} \\ &= \frac{dE_c}{dx} = \frac{\epsilon_0 A}{2(x_0 - x)^2} V^2, \end{aligned} \tag{2.24}$$

which is attained, as the total energy in the capacitor biasing system, dE_{tot}, is reduced by the same amount of energy, dE_c, as is fed to the capacitor [7]. When the displacement (position) x is obtained from the mass-spring-damper system in Fig. 2.2, which depicts the structure of a sensor element (resonator), the dynamics of the resulting system can be expressed by rewriting (2.8) as

$$m\frac{d^2x}{dt^2} + D_x\frac{dx}{dt} + k_x x = F_i + F_{es}, \tag{2.25}$$

where F_{es} is assumed to be the only component of F_{ext}. By substituting (2.24) into (2.25), x becomes a non-linear function of the force F_i. When $x \ll x_0$, (2.25) can be linearized and written as,

$$m\frac{(dx)^2}{dt^2} + D_x\frac{dx}{dt} + \left(k_x - \frac{\epsilon_0 A}{x_0^3}V^2\right)x = F_i + \frac{\epsilon_0 A}{2x_0^2}V^2. \tag{2.26}$$

The term $-\epsilon_0 A V^2/x_0^3 = k_e$ is the electric or electrostatic spring constant, which lowers the total spring constant. The effect is known as *electrostatic spring softening*.

Pull-in is an extreme phenomenon related to electrostatic forces. Pull-in occurs when the electrostatic force in (2.25) increases more rapidly as a function of x than the restoring spring force. A characteristic parameter, the pull-in voltage, can be calculated for the system. At voltages higher that the pull-in voltage the system cannot reach a stable value of displacement, except after collision with the stator. Pull-in can also be considered as a value of x, at which the spring constant $k_x + k_e$ turns negative and causes the total spring force to change its sign. Theoretically, for any non-zero bias voltage a possibility

of instability resulting from pull-in exists as x approaches x_0. Any non-zero force F_i in (2.25), for example resulting from acceleration, will affect the position of the proof mass. A change in the position, i.e in the distance between the rotor and stator, also denotes a different pull-in voltage. In fact the correlation between the pull-in characteristics and external acceleration has been utilized to design an accelerometer in [24].

In gyroscopes, especially in those operating in the low-pass region, the motion of the sense resonator is practically small enough for the approximation $x \ll x_0$ to be valid. On the one hand, in accelerometers the maximum value of x can be large enough to cause non-linearity. The problem can be relieved by utilizing *constant charge* biasing or *charge control* in order to maintain constant charge [25].

When the charge Q of the sensor capacitance is kept constant, the electrostatic force can be rewritten as

$$F_{es} = -\frac{dE_{tot}}{dx} = -\frac{dE_c}{dx} = -d\left(Q^2\frac{x_0 - x}{2\epsilon_0 A}\right)/dx = \frac{Q^2}{2\epsilon_0 A}, \tag{2.27}$$

which is attained as, with an ideal charge source, the total energy E_{tot} is equal to the energy in the capacitor E_c. By substituting (2.27) in (2.25), x remains a linear function of the external force F_i, and hence, electrostatic forces will not affect non-linearity, even in the presence of large displacements.

In order to be able to create a constant charge in the sensor capacitor(s), discrete-time circuits are needed. For example, two different switched-capacitor circuits for constant charge operation will be introduced in Sections 3.1.7 and 3.1.8.

The non-linearity resulting from electrostatic forces can also be reduced by means of mechanical design. A comb transducer is shown in Fig. 2.10 (only three of N parallel capacitors are shown). A typical comb structure, such as that in Fig. 2.10, is able to generate a lateral position-independent force, and is commonly referred to as a comb actuator or comb drive.

The capacitance for the comb structure, when parasitic fields are ignored, can be ex-

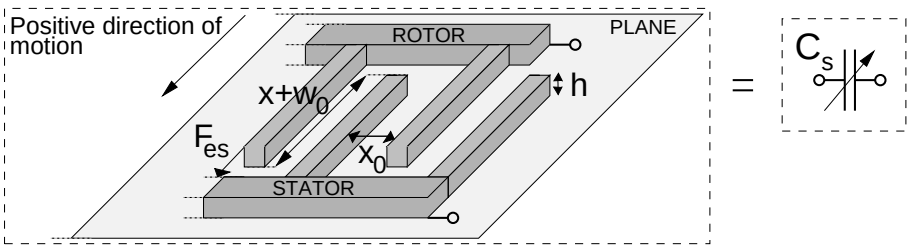

Figure 2.10: A comb capacitor.

pressed as

$$C_s = N\frac{\epsilon_0 h(x + w_0)}{x_0}. \tag{2.28}$$

The variable x corresponds to a change in the overlap of the capacitor fingers with a nominal value of w_0, h is the height of the fingers, and x_0 the constant spacing between the fingers. Now, both the gain, dC_s/dx, from position to capacitance, and the electrostatic force

$$F_{es} = \frac{\epsilon_0 h}{2x_0}V^2 \tag{2.29}$$

are independent of the variable x, when voltage V is applied across the capacitor. The comb actuation and detection are therefore applicable for microstructures with a large amplitude of motion. On the other hand, the position-independent gain is achieved at the expense of a smaller dC_s/dx per area unit when compared with the parallel plate capacitor. A further comparison between comb and parallel plate structures for the arbitrary amplitude of motion is presented in [26], with the focus on the detailed modeling of the parallel plate detection.

Electrostatic forces are clearly not the only source of non-linearity in the sensor element. In addition to the non-linear force-to-displacement conversion, where the electrostatic forces are the source of non-linearity, the distortion is inflicted within the sensor element by the position-to-capacitance conversion. Although the capacitance of a lateral comb structure is theoretically linearly dependent on the displacement x (see (2.28)), the parallel plate capacitor allows a linear gain dC_s/dx only if $x \ll x_0$. With this approximation valid, the gain can be written as

$$G_{T2} = dC_s/dx \approx \frac{\epsilon_0 A}{x_0^2} \tag{2.30}$$

for a single parallel plate capacitor. Similarly, for a comb capacitor

$$G_{T2} = dC_s/dx = N\frac{\epsilon_0 h}{x_0}, \tag{2.31}$$

where, theoretically, no approximation is required. Using these gain terms, the signal capacitance in Fig. 2.8 can be expressed as a linear function of position, $\Delta C = G_{T2}x$.

When the condition $x \ll x_0$ is not met, ΔC becomes a non-linear function of position in a parallel plate capacitor, as (2.23) indicates. However, the linearity can be improved by using a differential configuration, either a half-bridge or full-bridge (see Fig. 2.8), in which case the even-order harmonic components of the capacitive signal will be suppressed. The non-linearity of the position-to-capacitance transducer can be further reduced, or theoretically eliminated in a differential parallel plate transducer, by using *ratiometric* detection.

The systems with ratiometric output usually refer to the output voltage being proportional to the supply voltage. However, the term is also used to refer to the detection of capacitances. In ratiometric detection, instead of the absolute value of the capacitive signal of

interest being detected, the ratio between the differential and the common-mode capacitance is read. For example, if the interface electronics for a differential half-bridge sensor is designed to implement a ratiometric readout, the analog output signal of the sensor is of the form

$$sensor\_output = V_{det}\frac{C_{s1} - C_{s2}}{C_{s1} + C_{s2}}, \tag{2.32}$$

which is equal to $V_{det}x/x_0$ when $C_{s1}(x) = C_{s2}(-x) = (2.23)$, or equal to $V_{det}x/w_0$ when $C_{s1}(x) = C_{s2}(-x) = (2.28)$. Thus, the analog output is directly proportional to both the detection voltage V_{det} and the position x, even in the case of parallel plate sensor capacitors. However, the non-linearity is not fully canceled, if the sensor includes a torsional (tilting) sensor element (sketched in Fig. 3.28) [27]. Even with a torsional element, the ratiometric detection allows the linearity to be improved by roughly 10 dB compared to the detection of the absolute differential capacitive signal.

2.4 Other Types of Inertial Microsensors

Capacitive sensors represent one method to detect the signal of interest; however, several other transduction mechanisms can be utilized as well. Many of the sensor elements are based on a similar structure, where the proof mass is attached to the reference system via compliant beams, as depicted in Fig. 2.11 for an accelerometer. The differences often result from different methods for the detection of the proof mass position, and in Fig. 2.11 (a) the already familiar method of capacitive detection is shown for comparison. The applicability of a certain type of inertial sensor for a certain application depends on many characteristic features of the sensor. Typical features include, for example, cost and performance-related parameters, while performance is qualified via parameters such as resolution, full-scale signal range, stability of offset and gain, non-linearity, shock and interference tolerance and supply current consumption. Different types of sensors typically have different strengths and weaknesses depending on the transduction mechanism; some of these will be introduced next to allow a rough comparison [28].

2.4.1 Microaccelerometers

A *piezoresistive accelerometer* was introduced as early as in 1979 [29] and is still a widespread and vastly utilized type of an accelerometer. The functionality of a piezoresistive microaccelerometer is depicted in Fig. 2.11 (b), where piezoresistors are realized using material exhibiting high piezoresistivity, e.g. silicon. The acceleration induces a shift in the position of the proof mass, which further changes the stress, especially in the spring structure and attached piezoresistor. The stress-induced change in resistance is detected in order to resolve the effective acceleration. The ease of realizing a compact

piezoresistive sensor element and detecting a resistive signal are the important benefits of piezoresistive accelerometers. The detection of resistances, however, consumes dc supply current, making a piezoresistive accelerometer less optimal for ultra-low-power applications. In addition, the noise of the signal resistors can be significant compared to the actual resistive signal, making it difficult to attain ultra-low-noise performance. [7]

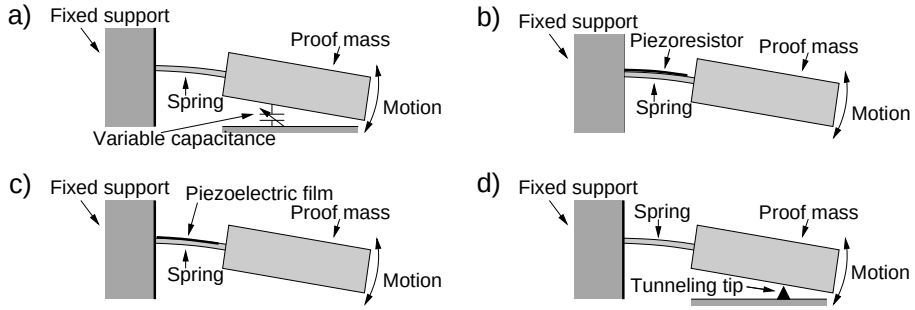

Figure 2.11: Illustration of the detection of motion in a) capacitive, b) piezoresistive, c) piezoelectric, and d) tunneling accelerometers. The fixed support is in the same coordinate system as the reference system whose acceleration is being measured.

Piezoelectric accelerometers are able to self-generate a charge that is dependent on stress. An illustration of a microsystem for the generation of acceleration-dependent stress is shown in Fig. 2.11 (c). For example, films of piezoelectric material, e.g. aluminum nitride (AlN), can be processed at a location where the maximum acceleration-induced stress is attained. Although piezoelectric microaccelerometers are self-generating, the change in the charge, i.e. the signal current, is proportional to the magnitude of the change in the stress, i.e. in the acceleration, and is essentially zero at dc. Hence, piezoelectric accelerometers cannot measure dc acceleration and the signal current is limited in microscale at low frequencies [30, 7]. On the other hand, the low-noise signal detection and low power consumption make piezoelectric position detection more attractive for macroscopic accelerometers and for applications where only ac signals need to be detected, such as vibratory gyroscopes.

Tunneling Accelerometers are a class of accelerometers capable of reaching very high resolutions. The structure of a tunneling accelerometer (see (d) in Fig. 2.11) resembles a traditional, for example, capacitive sensor, where the distance between the proof mass and a static electrode is measured. In a tunneling accelerometer, however, the distance between a tunneling tip, positioned on one of the electrodes, and the counter electrode is maintained at roughly 10 *Å*, small enough to allow a tunneling current in the order of a nanoampere to flow [31]. For proper accelerometer operation, the position must be maintained with the precision of an ångström because of the exponential ratio between the tunneling current and the distance between the two electrodes. Hence, tunneling accelerometers always operate in a closed loop. In fact, the loop must be very fast in order for the sensor to tolerate ac accelerations, and, for example, in [31], the full-scale acceleration is only about 1 mg, although the noise floor is as low as 20 $\mathrm{ng}/\sqrt{\mathrm{Hz}}$. In addition,

when the feedback force is attained using electrostatic coupling, the required feedback voltage is commonly tens of volts. On the other hand, when noise is considered, tunneling accelerometers are very resistant to the noise of the electronics because of the very high sensitivity of a tunneling element. This also means that the mechanical noise, together with tunneling-related noise, typically limits the noise performance of the sensor. The very high sensitivity of the tunneling current also makes the tunneling accelerometer very sensitive to even the slightest changes in the tunneling surfaces, increasing the variation of offset considerably.

Thermal accelerometers are based on thermal transduction. In one of the first thermal accelerometers [32] a proof mass was suspended between two rigid electrodes – a structure similar to that in some capacitive accelerometers. Instead of capacitive detection of the motion in the proof mass, the rigid electrodes were realized to function as heat sinks where thermopiles were used to detect the temperature. A heater was attached to the proof mass, creating an acceleration- and position-dependent heat transfer. The difference in the amount of heat transferred resulted in a temperature difference between the heat sinks. The temperature difference was measured using the thermopiles. The next-generation thermal accelerometer [33] was realized with no solid proof mass. Instead of a moving proof mass, the acceleration-dependent heat transfer was now attained by allowing a heater element to create a small hot air bubble. Using two temperature sensors, located symmetrically beside the heater, allowed the acceleration-dependent change in the free convection of the air bubble to be detected. In general thermal accelerometers have greater tolerance to external disturbances, such as electromagnetic interferences. However, they tend to consume a moderately large amount of power because of the heating element, despite the fact that the device is sealed on a package level to isolate the accelerometer from the external air flow.

Like thermal accelerometers, *optical accelerometers* aim for improved EMI tolerance. High resolutions can also be achieved and both open- and closed-loop designs are possible. In optical accelerometers a proof mass is anchored to a rigid frame via a suspension and, as in capacitive or piezoresistive accelerometers, is displaced as a result of acceleration. The resulting displacement is detected. In an integrated optical accelerometer the detection is performed by allowing the proof mass motion to affect the intensity of the light detected. In [34] the light source is realized as a laser on a gallium arsenide chip. The photodiodes that are used for the detection of light are also located on the same die. The photocurrent that results from the motion of a bulk silicon accelerometer is measured using an off-chip transimpedance amplifier, which allows the acceleration to be resolved with a noise floor of 25 $\mu\mathrm{g}/\sqrt{\mathrm{Hz}}$. With only the interface electronics missing, the implementation approaches the level of maximum integration the multi-chip optical sensor can achieve.

Resonant accelerometers are basically oscillators, where a micromachined resonator is operated in a closed loop in such a way that the resonance frequency defines the oscilla-

tion frequency. The sensitivity to acceleration arises as the resonance frequency changes as a result of external acceleration. The motivation to develop resonant accelerometers has been an improved tolerance to EMI and the possibility of direct digital output, while high performance should also be attainable. The challenge in resonance accelerometers is the small signal, at a maximum about 1000 $\mathrm{Hz/g}$, whereas more typically the sensitivity is below 100 $\mathrm{Hz/g}$. In a recent resonant accelerometer in [35], where a two-chip solution is adapted and capacitive detection and actuation is used, a sensitivity of about 100 $\mathrm{Hz/g}$ or 1000 ppm in the relative frequency shift resulting from 1 g acceleration is achieved. In order to be able to detect the small signal with high accuracy, the amplitude of the oscillation must be well controlled. Precise amplitude control, such as the one proposed in [35], is important in order for the non-linear behavior of the resonator not to diminish the sensor performance. In addition, the frequency shift, produced by acceleration, is also challenging to detect. A phase-locked loop (PLL) can be used for the frequency demodulation, but the accuracy requirements for the PLL become stringent. In addition, digital interfacing by calculating the length of the clock periods received from the oscillator can require a stable clock at a frequency well above megahertz. Simple counting of the periods received from the oscillator can easily limit the attainable signal bandwidth. Hence, the design of the interface electronics for a resonant accelerometer poses a challenge.

The actual micromechanical structure that defines the proof mass, suspension, and means of detecting the position varies significantly, depending on the fabrication technology and properties of the accelerometer, but also on the operational principle. More details about the mechanical design can be found, for example, in [28].

2.4.2 Microgyroscopes

Most of the MEMS gyroscopes are based on the detection of Coriolis acceleration. The mechanical sensor element can, for example, be based on the traditionally used tuning fork structure that is illustrated in Fig. 2.12, but other mechanical structures have also been used to realize a vibratory gyroscope [28, 36]. The tuning fork can still be used to depict the operation, also sketched in Fig. 2.12, where the two tines of the fork are forced into oscillation, driven in the direction of one axis. Rotation about the axis perpendicular to the driven axis couples the oscillation in the direction of the third, sense, axis. Like in the case of accelerometers, the capacitive sensing of the Coriolis acceleration and generation of the drive mode oscillations is just one way to realize a microgyroscope.

The dual nature of piezoelectric interfaces, similarly to capacitive interfaces, makes possible both a self-generated detection current and actuation with zero static current consumption. A piezoelectric interface can, for example, be used to attain a higher excitation force for the driven resonator, compared with the use of an electrostatic force, and it requires no dc bias. For example, in the tuning fork gyroscope in [37], a monolithic lead

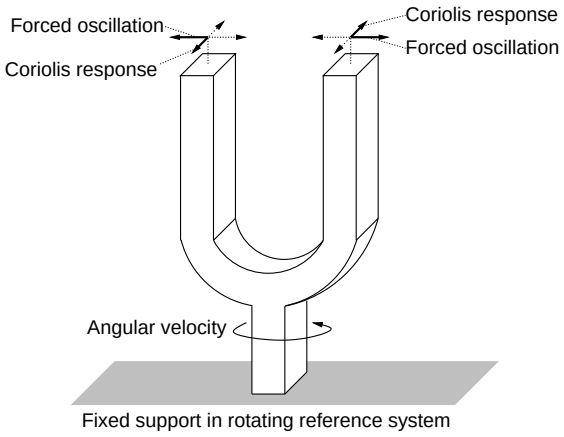

Figure 2.12: Typical functionality of a tuning fork gyroscope.

zirconate titanate (PZT) structure is proposed to replace the traditionally used quartz, because of its stronger piezoelectric properties, which can potentially result in a gyroscope with a higher performance. The measured resolution of about 0.01 $^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$ in [37] was, however, lower than expected. As an ultimate application, the piezoelectric phenomenon can be utilized to implement the gyroscope in a simple solid mass [36], which deforms in oscillatory fashion and realizes the sensitivity to the Coriolis force. The omission of the suspension structures or mechanical parts increases the tolerance of the gyroscope to high mechanical shocks.

The piezoresistive detection of sense motion has also been applied, thanks to the simple device fabrication and ease of detecting the resistive signal. For example, in [38] the piezoresistive sense is combined with an electromagnetic drive to form a vibratory gyroscope. However, the detection of the already minute Coriolis force using piezoresistive detection results in a noisy output signal. In addition, similarly to accelerometers, in gyroscopes too piezoresistors exhibit strong temperature sensitivity.

Tunneling offers an additional alternative for the detection of the sense motion induced by the Coriolis force. The method has been studied, for example, in [39], where the initial performance tests demonstrate a noise floor of 27 $^\circ/\mathrm{h}/\sqrt{\mathrm{Hz}}$, which could be reduced to the level of the Brownian noise floor 3 $^\circ/\mathrm{h}/\sqrt{\mathrm{Hz}}$. The properties of a tunneling gyroscope are similar to those in tunneling accelerometers, and, for example, closed-loop sense operation is basically mandatory to make possible a constant tunneling current.

Micromachined *rotational gyroscopes* are the microsized versions of traditional macroscopic gyroscopes, which are based on the conservation of the angular momentum of a spinning wheel, or rotor. The operating principle is not typically applied in MEMS gyroscopes, simply because of the difficulty of micromachining the required mechanical components, e.g. the bearings. However, a rotating gyroscope can be realized by levitating the rotating wheel. For example, a capacitive micromachined rotational gyroscope

is reported in [40], where altogether five closed control loops are utilized to realize the levitating effect. The control loops also provide the output for the sensor, as the feedbacks nullify all the transitions of the spinning rotor. The levitation control structure for a single spinning rotor is able to detect angular velocity about two axes and translational acceleration about three axes. No IC implementation of the highly complex interface circuitry was shown in [40]. Other methods for realizing levitating microgyroscopes have also been reported [36].

Other types of gyroscopes also exist that aim for miniaturized size and often utilize micromachining for the realization of small mechanical structures. The Coriolis effect is utilized in a convective gyroscope, where the angular rate is detected by observing changes in the direction of the gas flow. The traditional macroscopic optical gyroscopes, capable of achieving high performance, are based on the Sagnac effect. Microgyroscopes based on the same effect have been researched, for example, by using optical MEMS technology. Further information on these and also other types of miniaturized gyroscopes can be found in [36].

2.5 Fabrication of Microsystems

The mass production of microstructures, e.g. sensors, relies on batch fabrication, which is illustrated in Fig. 2.13. In batch fabrication thousands of individual microstructures can be formed simultaneously on a common substrate that is typically a silicon wafer. The techniques involved in creating microstructures include depositing materials on the wafer and patterning the wafer or the deposited layers by photolithography and etching. After the microstructures are complete, the wafer is diced and the separated microstructures are packaged, often together with the interface electronics, either as a separate die or on the same chip. The microfabrication techniques can be divided into *surface micromachining* and *bulk micromachining*, which are briefly reviewed next [7].

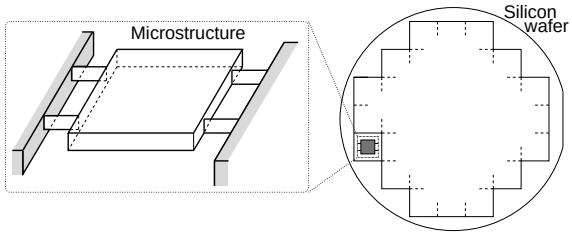

Figure 2.13: Illustration of batch fabrication.

2.5.1 Surface Micromachining

In surface micromachining [41] the mechanical microstructures are formed by depositing and patterning thin films on a substrate, often a silicon wafer. The films that are grown

can be categorized as sacrificial layers that will be removed and structural layers that define the actual microstructures. An illustration of a process for creating surface micromachined devices is shown in Fig. 2.14. The processing starts by depositing a layer of sacrificial material (b), such as silicon dioxide, on a substrate wafer (a). The layer is patterned and etched (c). A structural layer, such as polysilicon, is deposited on the sacrificial layer (d), and patterned and etched (e) to form the desired microstructures. Finally, the microstructures are released (f) by etching away the remaining sacrificial layer that is accessed via the edges and holes in the structural layer. More complex devices can be created by increasing the number of structural layers. Surface micromachining can be used to implement membranes and interdigitated structures that are commonly used to create, for example, inertial sensors with a capacitive interface.

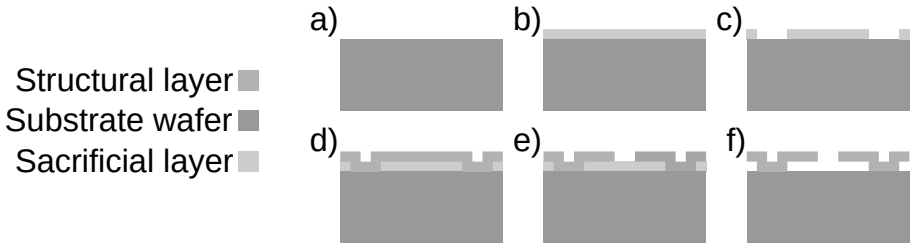

Figure 2.14: Illustration of process steps for realizing surface-micromachined devices.

The microdevices formed by depositing films are typically thin, less than 5 μm thick, reducing the total mass of the microdevices. For example, inertial sensors, where the proof mass is in the order of micrograms, are prone to mechanical noise. On the other hand surface micromachining can be combined with the processing of integrated circuits, which allows MEMS to be created on a single chip. The system-level integration allows considerably smaller parasitic capacitances caused by the interconnections between the electronics and the mechanics, resulting in improved noise performance.

2.5.2 Bulk Micromachining

Bulk micromachining covers the techniques where a large amount of material is removed from the substrate and the device is part of the substrate. With this definition, the (silicon-on-insulator) SOI-based micromachining techniques can also be included under the bulk MEMS category. In an SOI wafer two silicon wafers with thicknesses of a few tens of microns and several hundred microns are bonded with silicon dioxide (typically 1-2 μm) between them.

Bulk micromachining involves different etching techniques to shape an existing substrate, typically silicon. The key element in etching is the etchants, which can be divided into

wet and dry etchants. A wet etchant refers to the use of a liquid solution, whereas dry etchants are in the form of a vapor or plasma. The regions exposed to the etchants are defined using masking layers, such as silicon dioxide or silicon nitride, which are resistant to etching. The characteristics, including the etch rate, CMOS compatibility, and price, depend on the etching technique used [42].

The ready bulk micromachined structure can be as thick as the whole structural or substrate wafer, i.e. several hundred micrometers, as in the example in Fig. 2.15, where two cover wafers are bonded on both sides of the device, in order to form a capacitive parallel plate interface and, for example, allow the device to operate in a vacuum. Bulk MEMS devices such as accelerometers can be designed to have a large proof mass and therefore low mechanical noise. However, as the bulk MEMS devices often include separate dies for the electronics and the mechanical devices, the necessary interconnecting wires, bonding pads, and especially, any existing protection against electrostatic discharge (ESD) between the IC and the sensor element can considerably increase the amount of parasitic capacitance and noise.

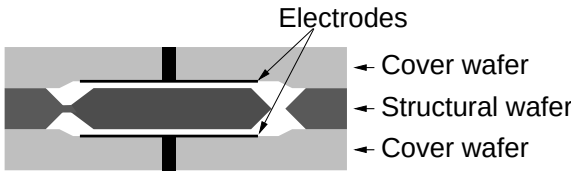

Figure 2.15: Illustration of a bulk micromachined structure, an accelerometer, that is encapsulated using two cover wafers.

2.6 Discussion

Micromachined accelerometers measure acceleration in the direction of up to six axes and, because of their overall dimensions, which are typically less than a few millimeters, these sensors have quickly found their way into consumer applications, where they are used to detect, for example, free fall or orientation. Clearly in these example applications the lowest performance suffices. On the other hand, compact MEMS accelerometers have already met or even exceeded the performance of, for example, geophones, which are precise measuring instruments used as seismometers.

The properties of accelerometers are different, depending on the type of accelerometer. Thermal and optical accelerometers are more robust against electromagnetic interference, and piezoresistive ones are small and easy to manufacture but are fairly noisy, whereas tunneling accelerometers can reach an extremely good noise performance. In capacitive microaccelerometers the power consumption and often also the performance are limited

Table 2.1: Examples of published state of the art capacitive microaccelerometers.

Reference	[43]	[15]	[16]	[44]	**[II]**
Published	2004	2009	2004	2005	2009
Sensor element	surface MEMS	bulk MEMS	bulk MEMS	-	bulk MEMS
Interface type	analog open-loop readout	open-loop direct $\Delta\Sigma$ readout	closed-loop digital or analog interface	closed-loop mixed-signal $\Delta\Sigma$ interface	analog closed-loop interface
Supply (V)	5	1.2	± 6	3.3	5 / 12
current (mA)	6	0.021	12	0.8	15 / 0.9
power (mW)	30	0.025	144	2.6	86
Noise floor ($\mathrm{mg}/\sqrt{\mathrm{Hz}}$)	0.05	1.1 (x), 1.1 (y), 0.9 (z)	0.0003 (analog)	0.09 (estimated)	≈ 0.0003 (average)
Signal band (Hz)	2000	1	5000	50	300
Full-scale signal $\pm(\mathrm{g})$	6	4	3	10	1.5

by the electronic interface so they can be designed to be either very low-power or, on the other hand, very high-performance devices. The requirements for the sensor, therefore, translate not just to the specifications for the element but also to those for the electronic interface, which forms the main topic of this thesis.

As the interface electronics often reflects the performance of the sensor, a few state-of-the-art accelerometer designs with integrated interface electronics are included in Table 2.1. It can be noticed that most of the low-noise accelerometers utilize bulk micromachined sensor elements as a result of the fact that surface-micromachined structures typically do not generate an equally high capacitive signal. The power consumption and supply voltage are also tied to the noise performance and, as can be seen from [15], they can be traded for lower speed and accuracy. The accelerometer design that is part of this thesis, [II], is capable of nearly the same performance as even [16], while details of the topology, which has not been previously used to attain an equal performance, are presented in [I-IV].

Gyroscopes, on the other hand, are used to measure rotation about up to three axes. A single-axis gyroscope comprises a driven resonator which is set into motion about one axis and a sense resonator that is coupled to the drive resonator, which is sensitive in the direction of an axis orthogonal to the driven axis. The Coriolis force, caused by rotation about the axis orthogonal to both axes of the resonators, couples vibration between the two axes. Inherently low-noise capacitive interfaces are utilized both to enforce precise oscillation of the drive resonator and to detect the minute motion of the sense resonator in order to resolve the angular rate. Other methods also exist to attain the proper functionality of a vibratory gyroscope, for example, piezoelectric readout and actuation, piezoresistive readout, which, however, is usually too noisy, and tunneling-based readout. As the

Table 2.2: Examples of published state of the art capacitive microgyroscopes.

Reference	[47]	[23]	[46]	[45]	**[V]**
Published	2002	2008	2009	2009	2009
Sensor element	surface MEMS	-	-	SOI MEMS	bulk MEMS
Active mode matching	No	Yes	No	Yes	No
Sense interface type	analog open-loop readout	closed-loop mixed-signal $\Delta\Sigma$ interface	closed-loop $\Delta\Sigma$ interface	analog open-loop readout	pseudo-continuous-time analog readout
Supply (V) current (mA) power (mW)	5 6 30	3.3 / 12 - / - 1	5 / 18 0.25 / 0.1 3	3 / 40 2 / - -	3 1.8 5.4
Noise floor ($^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$)	0.05	0.004	0.025	0.00006	0.015 (x) / 0.041 (y)
Signal band (Hz)	1000	50	>100	1	300
Full-scale signal $\pm(^\circ/\mathrm{s})$	150	-	>1100	-	300

electronics also plays an important role in gyroscopes, a few state-of-the-art gyroscope designs with integrated interface electronics are included in Table 2.2. As can be seen in the table, matching the resonance frequencies in the gyroscope effectively increases the noise performance. Active mode matching typically allows a higher capacitive signal from the sense resonator, which is because even a slight mismatch in the resonance frequencies will reduce the gain attained by taking advantage of the high Q-value of the sense resonator. Increased bandwidth and dynamic range can be attained by utilizing a closed-loop interface for the sense resonator with active mode matching. For [V], however, the design goal was not just the good noise performance and low power consumption as in, for example, [45]. Instead, the interface was optimized for performance and low power, but most of all for compact design with, ideally, no external components. In this case, a gyroscope that operates in low-pass mode and allows compact open-loop readout techniques to be used was utilized for the design. The minimized chip area was achieved by introducing a new low-noise readout technique, while at the same time fully integrating the PLL and the high-voltage circuits, which, as indicated by the voltage requirements, are missing in [23], [46], and [45]. All the circuit blocks of the implementation are presented in [V-IX]. In fact, the two-axis gyroscope with the complete updated and redesigned interface chip with an area of 4.3 mm^2 is presented by the author et al. in [13].

3 Interface Circuits for Capacitive Sensors

When the functionality of a microaccelerometer is compared with a microgyroscope from the signal detection viewpoint, the accelerometer outputs the capacitive signal at the same frequency as the input acceleration. On the other hand, in a vibratory microgyroscope the capacitive signal corresponds to the amplitude-modulated angular velocity information. Hence, in accelerometers, a dc input acceleration brings forth a dc shift in the sensor capacitances, which cannot be detected using dc voltage for the readout. Unlike in accelerometers, in vibratory gyroscopes a constant input angular rate generates a capacitive signal at the carrier frequency, which allows a finite signal current even with a mere dc voltage across the sensor capacitors. This feature, and the considerably smaller capacitive signal of a microgyroscope form the main differences between the readouts of the two types of capacitive sensors. As the Coriolis acceleration in a vibratory gyroscope and linear acceleration in an accelerometer are detected using a common structure, which is basically a microresonator, the typical signal bands of interest can also be examined in the frequency domain. The transfer function (TF) of gain of a low-Q resonator is shown in Fig. 3.1 and represents the gain from the input force, induced by either linear acceleration or Coriolis acceleration, to the output capacitance. The signal band of the gyroscope is modulated at the carrier frequency and hence is shifted away from the very low frequencies.

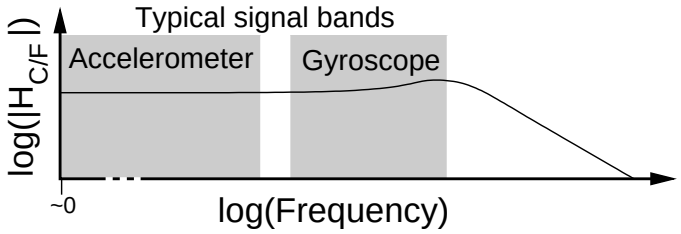

Figure 3.1: A transfer function of gain from force to capacitance ($H_{C/F}$) and typical signal bands of interest.

The front-end electronics are often alike for accelerometers and gyroscopes. Both sensor types can be operated either in open- or closed-loop configuration using the same structures, but with distinctive features related to the type of sensor being interfaced with. The different types of interface circuits for capacitive accelerometers and gyroscopes will be studied in this section.

3.1 Capacitive Open-Loop Readout

A block diagram of a capacitive open-loop sensor is shown in Fig. 3.2. The external observed signal, e.g. acceleration, is converted to force with gain G_T, which is equal to the inertial mass of the sensor, i.e. $G_T = m$. The force domain signal traverses the resonator (the TF of the resonator is H_{RES}), and is transformed into position. The position is converted to capacitance with gain G_{T2} (see Section 2.3 for details), and the capacitance is detected by the electronic interface (the TF of the readout is H_R) and transformed to an easily accessible format such as a voltage or digital word. The total transfer function from the external signal of interest to the sensor output can thus be written as

$$H_S = G_T H_R G_{T2} H_{RES}. \tag{3.1}$$

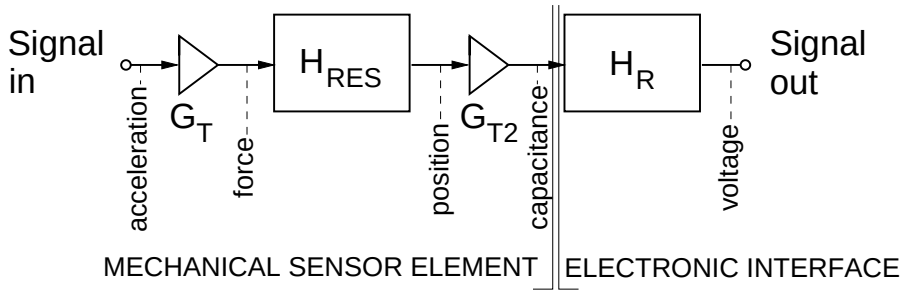

Figure 3.2: Block diagram of an open-loop sensor also depicting the main signal domains.

An open-loop system can only be designed to be as good as the worst element of the system, if it is assumed that complex calibration and correction methods are not utilized. Hence, for example, improving the design of the electronics will only help up to the level that is reached by the sensor element with fixed design. In this case, for example, the bandwidth of the element will limit the signal bandwidth of the open-loop readout. Additional element-related parameters, such as linearity, the full-scale signal range, or high Q resonances, cannot be controlled in an open-loop configuration either. On the other hand, a simple and often low-noise readout circuit is the significant benefit of an open-loop sensor.

Open-loop readouts can be performed using either continuous-time (CT) or discrete-time techniques (DT) with either analog or direct digital output. The circuit techniques for the readout will be introduced next.

3.1.1 Continuous-Time Detection of Capacitive Signals

Before the sensor output can be transformed into voltage mode, or digital information, the signal capacitance is converted into a charge. To be more precise the actual quantity of interest is the moving charge, i.e. the current, which is further converted into voltage by the front-end electronics attached to the sensing element. The procedure for creating the signal current is depicted in Fig. 3.3, where the sensor element is modeled using a single variable capacitor C_s. In the case of Fig. 3.3 (a) the detection voltage V_{det} is assumed to

Figure 3.3: The use of (a) dc and (b) ac detection voltage for transforming the capacitive signal into charge/current.

be constant, or time-independent, which allows a non-zero signal current

$$I_s = \frac{dQ}{dt} = V_{det}\frac{dC_s}{dt}, \tag{3.2}$$

only if C_s is time-dependent. This assumption is valid in vibratory gyroscopes, where the constant V_{det} can be used for detection. The detection using the constant (dc) V_{det} can also be referred to as *rate-of-change* or *velocity measurement*. In accelerometers C_s settles to a new constant value when dc acceleration is applied, and hence (3.2) would give zero current for Fig. 3.3 (a). If V_{det} is replaced with an ac detection voltage V_{det_ac} as in Fig. 3.3 (b), the signal current can be written as

$$I_s = \frac{dQ}{dt} = \frac{d(V_{det\_ac}C_s)}{dt}. \tag{3.3}$$

The spectral components of the original capacitive signal and the charge mode signal are depicted in Fig. 3.4. The only case where the detected signal does not require demodulation before the final sensor output is created corresponds to an unmodulated capacitive signal and dc detection voltage (V_{det}). Unfortunately, when the signal frequency f_s is zero (dc signal), the signal current is also zero. A constant capacitive signal can be detected properly using an ac detection voltage, which is equivalent to amplitude modulation and corresponds to the product term $V_{det\_ac}C_s$ in (3.3). The detection using the ac voltage V_{det_ac} can also be referred to as *displacement measurement*. In the case of a gyroscope, where the original capacitive signal is already amplitude-modulated, the charge (current) mode signal becomes modulated twice, as can be seen in Fig. 3.4.

The frequency of the carrier or ac detection voltage is a design parameter which is determined by factors such as power consumption, noise, and chip area-related specifications

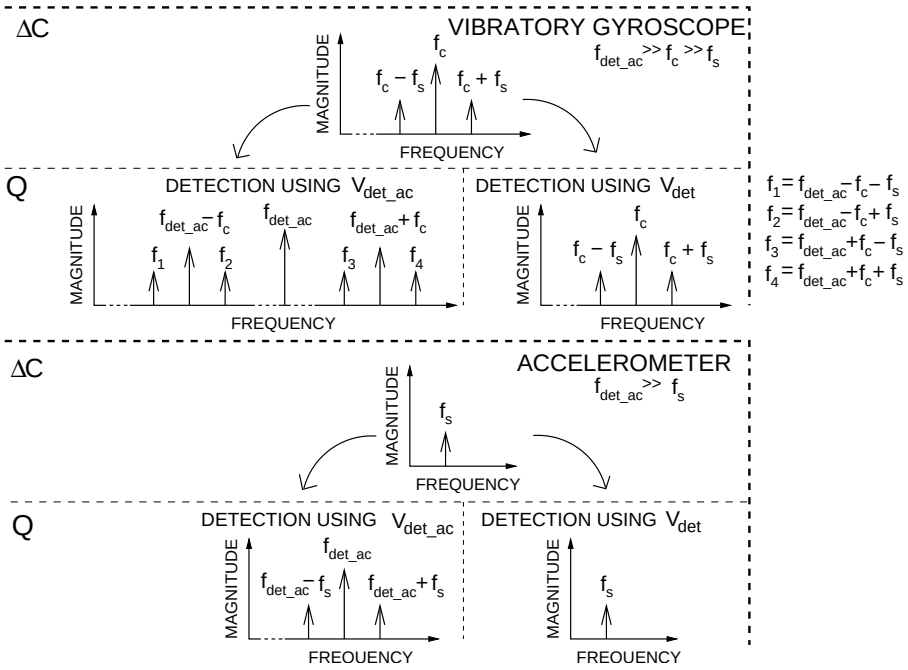

Figure 3.4: Typical spectral components of the capacitive signal ΔC and the signal charge Q after detection using both ac and dc detection voltages in a gyroscope and an accelerometer. The signal frequency is f_s and the frequency of V_{det_ac} is equal to f_{det_ac}. The capacitive signal in a gyroscope is modulated at f_c.

that apply to the readout circuitry. For example, the effect of flicker noise ($1/f$-noise) [48] is typically sufficiently low at roughly 100 kHz. A further increase in the frequency would allow smaller and more compact RC-time constants to be implemented for the CT readout circuits. Smaller integrated resistors and capacitors can reduce the chip area required. On the other hand, ac detection voltage is typically used, instead of dc, at the expense of higher power consumption and the increased complexity of the readout.

3.1.2 Voltage Buffer

The signal current from the sensor can be transformed into voltage using a simple CT voltage buffer. An example buffer is shown in Fig. 3.5 (a). In the figure, C_p depicts the parasitic capacitance formed, for example, by the interconnections and the buffer amplifier. The resistor R_{bias} is added to maintain a proper dc bias V_{bias} at the amplifier input, and A_V is the voltage gain of the buffer amplifier.

When a voltage buffer is combined with the dc detection voltage in order to detect the capacitance of a microgyroscope, noise requirements, potential issues with the stability of the resistance value over temperature, and frequency-dependent gain necessitate the

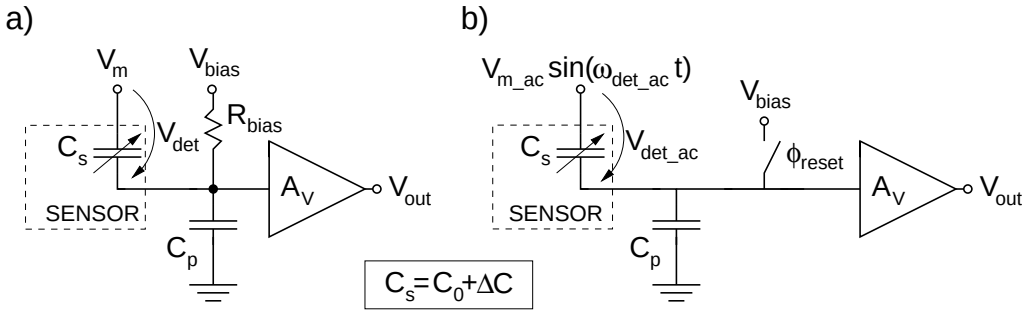

Figure 3.5: Voltage buffers used for the detection of capacitive signals; (a) for combined dc detection voltage V_{det} and a large resistor for implementing the dc bias at the amplifier input, and (b) for ac detection voltage V_{det_ac} and periodically refreshed dc bias.

condition $R_{bias} \gg 1/[2\pi f_c(C_s + C_p)]$. This requirement typically sets the resistance to be as high as a few gigaohms, which makes the resistor unsuitable for integration as a polysilicon resistor [49]. In order to avoid the high parasitic capacitance inflicted by a very large polysilicon resistor, the resistor can be replaced with a reverse-biased diode or a MOSFET operating in the subthreshold region. Example implementations can be found in [50] for a diode and in [51, 52, 53, 54] for a MOSFET-based dc biasing. In fact, if a PMOS transistor is used in the subthreshold region and connected in diode configuration (gate- and source-terminal shorted) in such a way that the source terminal is connected to the bulk terminal, the single transistor allows two back-to-back diodes to be realized. In this case the two diodes are formed by the MOSFET and the pn junction between the bulk and drain terminals.

When the voltage buffer is combined with the ac detection voltage V_{det_ac} and the frequency f_{det_ac} is selected to be sufficiently high, R_{bias} can be designed to be smaller and realized as a polysilicon resistor. Example interfaces using an ac detection voltage and a linear resistor for dc biasing can be found in [55, 56, 57] for the readout of an accelerometer. Another solution for maintaining the proper bias voltage is to reset the voltage at the amplifier input periodically, as in Fig. 3.5 (b). This approach is applied to the readout of a capacitive full-bridge accelerometer element in [43], where a detailed analysis of the buffer is also presented.

In order to review the general dynamic features of a voltage buffer, the sensor capacitance C_s can be divided into a static part C_0 and signal-dependent part ΔC. The voltage at the amplifier input will become distorted if the value of ΔC approaches that of C_0. Distortion is generated as the voltage across the sensor capacitor is essentially dependent on the signal itself. However, when $C_0 \gg \Delta C$, the detection voltage is approximately constant and the linear small signal gain from the signal capacitance to the output voltage can be evaluated. For Fig. 3.5 (a), with a dc detection voltage and frequency f_s (of ΔC) higher than the corner frequency $1/[2\pi R_{bias}(C_s + C_p)]$, the s-domain transfer function can be

written as

$$\frac{V_{out}(s)}{\Delta C(s)} \approx A_V \frac{V_m - V_{bias}}{C_0 + C_p}. \tag{3.4}$$

The ac detection in Fig. 3.5 (b) results in an amplitude-modulated output signal, when the reset switch is not conducting. The output voltage V_{out} in Fig. 3.5 (b) can be calculated in the time domain as

$$V_{out}(t) \approx A_V \frac{C_p}{(C_0 + C_p)^2} V_{m\_ac} \sin(\omega_{det\_ac} t) \Delta C(t), \tag{3.5}$$

for a sinusoidal detection voltage.

It can be noticed from (3.4) that $V_{det} = V_m - V_{bias}$ and hence, both bias voltages, V_m and V_{bias}, affect the gain. In (3.5) the gain is independent of V_{bias}, the purpose of which is simply to maintain the proper bias point of the amplifier. Additionally, in both (3.4) and (3.5), the gain is proportional to the parasitic capacitance, which is seldom a precisely defined parameter. It is also interesting to notice that the ratiometric readout of ac signals is achieved its simplest form using the voltage buffers. Especially if a differential sensor is used in Fig. 3.5, in such a way that $C_0 - \Delta C$ is substituted for the parasitic capacitor C_p, the output voltage can be calculated to be directly proportional to ΔC without any small signal approximations being made.

3.1.3 Transimpedance Amplifier

A well-defined gain can be achieved using a *transimpedance amplifier* (TIA), of which an example configuration is shown in Fig. 3.6 for a half-bridge sensor element. The signal current I_s of the sensor element is converted into voltage in the feedback impedance Z_{fb}, which is typically a resistor R_{fb} and a capacitor C_{fb} connected in parallel. TIA can be used together with either ac or dc detection voltage, which will have distinctive features. These characteristics will be studied next.

When the TIA is combined with a dc detection voltage ($V_{m\_ac} = 0$), and the operational amplifier is assumed to be ideal, and the leakage currents I_{leak1} and I_{leak2} are zero, the gain from the signal capacitance to the output voltage can be written as

$$\frac{V_{out}(s)}{\Delta C(s)} = -\frac{2R_{fb}s}{1 + sR_{fb}C_{fb}}(V_m - V_{incm}), \tag{3.6}$$

where V_{incm} is the common-mode level at the operational amplifier input. The equation exhibits total independence of parasitic capacitance at the amplifier input. It also suggests that the common-mode voltage at the amplifier input partly defines the detection voltage $V_{det} = V_m - V_{incm}$, and hence is an important design parameter. Any non-zero I_{leak} drawn from the input of the amplifier will affect the gain unless V_{incm} is actively controlled.

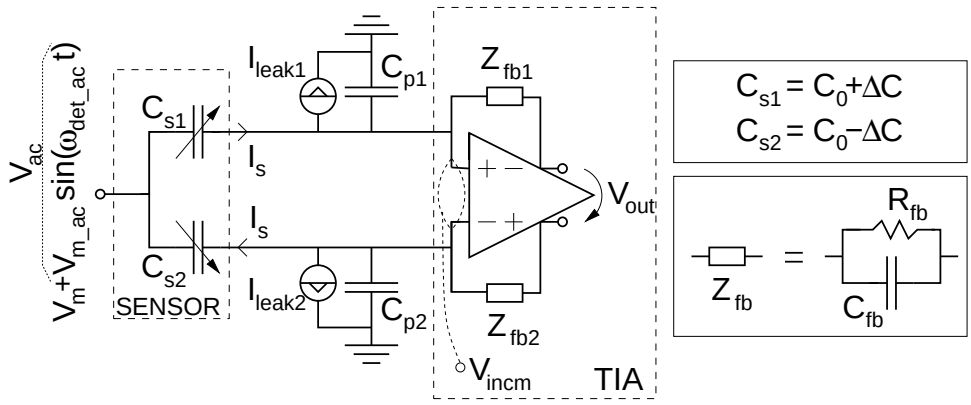

Figure 3.6: The detection of a capacitive half-bridge sensor using TIA. It is assumed that $C_p = C_{p1} = C_{p2}$ and $Z_{fb} = Z_{fb1} = Z_{fb2}$.

Stabilization of gain is the typical reason for controlling the common-mode level at the *input* of the amplifier (V_{incm}), instead of the output. This was the selected configuration in, for example, [VI] and [58].

When the TIA is combined with an ac detection voltage ($V_m = 0$), the method for controlling only the input common-mode voltage can rarely be applied. This is because with a constant V_{incm} the amplitude V_{m_ac} will be transferred to the common-mode output of the amplifier with gain $\omega_{det\_ac} C_0 Z_{fb}$ and hence would impede any further utilization of the TIA output voltage. On the other hand, a low-impedance common-mode node at the amplifier output inevitably causes V_{incm} to have a signal component at the detection frequency ω_{det_ac}. This signal will affect the output voltage, which can first be calculated in the s-domain as a function of the carrier $V_{ac}(s)$. By assuming that the signal capacitance ΔC is frequency-independent, and that the differential signal at the input and the common-mode signal at the output of the operational amplifier are both zero, the transfer function can be written as

$$\frac{V_{out}(s)}{V_{ac}(s)} = -\frac{1 + sC_p Z_{fb}(s)}{1 + s(C_p + C_0) Z_{fb}(s)} 2s\Delta C Z_{fb}(s). \tag{3.7}$$

Assuming that the carrier is now sinusoidal $V_{ac} = V_{m\_ac} \sin(\omega_{det\_ac} t)$ as shown in Fig. 3.6 and that the capacitive signal $\Delta C(t)$ varies slowly when compared with the detection frequency, $V_{out}(t)$ can be written in the time domain approximately as

$$\begin{aligned} V_{out}(t) \approx & -\frac{2\Delta C(t) R_{fb} \omega_{det\_ac}}{\sqrt{1 + [\omega_{det\_ac} R_{fb} C_{fb}]^2}} \sin(\omega_{det\_ac} t + \phi_d) \cdot \\ & \sqrt{\frac{1 + (R_{fb}(C_{fb} + C_p)\omega_{det\_ac})^2}{1 + [R_{fb}(C_{fb} + C_p + C_0)\omega_{det\_ac}]^2}} V_{m\_ac}, \end{aligned} \tag{3.8}$$

where ϕ_d is the component value and ω_{det_ac}-dependent phase shift from the sinusoidal detection voltage to the output of the TIA. In (3.8) Z_{fb} has been replaced by the parallel

connection of R_{fb} and C_{fb}. The effect of V_{incm} can now be seen in (3.8), where the second row of the two-row equation describes the detection voltage across the sensor capacitors. The higher the C_0 is compared to C_p and C_{fb}, the smaller the ac detection voltage V_{det_ac} and the gain are. One way to remove the ac component of V_{incm} is to actively drive it to zero using an additional amplifier. This approach is described in [59] for a switched-capacitor interface. It is also noteworthy that if there were mismatch between any of the two differential capacitances, offset would be created to the amplifier output at ω_{det_ac}.

TIA is typically used in such a way that either the feedback resistance R_{fb} or the feedback capacitance C_{fb} dominates the feedback impedance at the detection frequency. In the former case the TIA is then referred to as a *transresistance amplifier* (TRA), and in the latter as a *transcapacitance amplifier* or as a *charge-sensitive amplifier* (CSA). Additionally, (3.6) and (3.8) can be approximated for TRA by substituting $C_{fb} = 0$, and for CSA by substituting $R_{fb} = \infty$. It is interesting to notice that when $C_{fb} = C_p = 0$, (3.8) becomes zero as the detection voltage across the sensor capacitances (V_{det_ac}) approaches zero with an increasing detection frequency.

When the design target is to implement a CSA, the value of the feedback resistance should be maximized for minimized noise [58], and hence the design issues are similar to those related to the dc biasing of the voltage buffer. In most cases, implementing the resistor as a polysilicon resistor is not an option. Typical integrated realizations of the feedback resistor include MOSFETs biased in the linear region (see Fig. 3.7). Example implementations can be found in, for example, [46, 47, 58]. In [46] the voltage swing across the MOSFETs is reduced by applying a low-pass (LP) filter in the feedback path. In this way the MOSFET will not leave the linear (triode) region even in the presence of a large output signal. In [47] the impedance of the MOSFET feedback is increased by disconnecting the MOSFET periodically.

MOSFETs also offer an important alternative for the realization of dc feedback in integrated high-pass filters (HPF, see Fig. 3.7), where the signal level is typically even higher compared to CSAs. In these cases the strong second-order non-linearity can become an is-

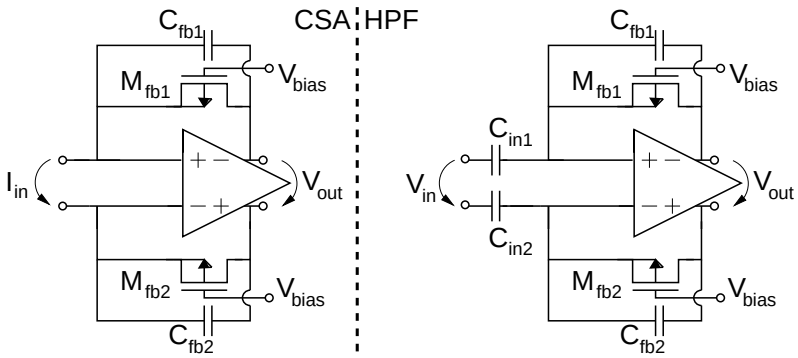

Figure 3.7: A CSA and an HPF utilizing MOSFETs for the realization of the dc feedback.

sue, even though a differential configuration would be used. This occurs especially when V_{bias} is a very high-impedance voltage source, such as the MOSFET diode-based biasing in [47, 58], and becomes signal-dependent. The bias shift resulting from the non-linearity is addressed in [VII].

The implementation of CSAs for the CT readout of a gyroscope using a dc detection voltage can be found, for example, in [46, 47, 58, 60], and for a CT readout of an accelerometer in [61, 62] and in [I, II]. Both accelerometer interfaces utilize an ac detection voltage, whereas the CT readout of a gyroscope is done using an ac detection voltage in [63, 64]. The noise analysis of the CSA can be found, for example, in [65, 66]. As integrated capacitors tend to be more linear and more stable over temperature when compared with large integrated resistors, CSAs, rather than TRAs, are more commonly applied for low-noise capacitive readout. A TRA where a resistive T-network realizes the high-impedance feedback is, however, used together with a very high dc detection voltage in [67] for the secondary (sense) readout of a gyroscope. Compared to a single resistor implementation, a T-network always results in increased noise and offset of the TIA, and hence is typically not used for interfaces where the feedback impedance is a significant noise contributor. TRAs are commonly used for the detection of the primary (drive) resonator in a gyroscope [47, 60, 67], mostly because the output of the TRA is in the correct phase for the electrostatic excitation of the primary resonator. The topic is discussed in more detail in [VII] and in Section 3.2.5.

3.1.4 Demodulation

In practically all capacitive inertial sensors that utilize continuous-time open-loop readout, the voltage at the output of the front-end circuit is in the form of amplitude modulation. Before the final signal can be output, the signal must be demodulated. When considering only the continuous-time techniques, there are basically two topologies for downconverting the amplitude-modulated signal back to the signal frequency; a multiplier (coherent or synchronous detection) or an envelope detector (incoherent detection). In coherent detection a sample of the carrier component, the ac detection voltage, at the correct phase is multiplied by the signal and the resulting low-frequency signal component represents the output of the demodulator. An envelope detector, typically a diode rectifier, on the other hand, extracts the envelope of the amplitude-modulated input signal and does not require a sample of the carrier component for the demodulation.

When an ac voltage is used for the detection of the signal capacitance, the same carrier is naturally also available for demodulation. This makes the application of coherent demodulation straightforward. In vibratory gyroscopes too the voltage mode signal, which is directly proportional to the primary resonator motion of a gyroscope, is typically accessible. The component is obtained from the primary loop of the gyroscope, which essentially

forms an oscillator at the carrier frequency ω_c.

The carrier can be used for demodulation in, for example, a Gilbert multiplier [68], shown in Fig. 3.8. The differential output current of the multiplier can be written as [69]

$$I_{out} = I_1 - I_2 = I_0 \tanh \frac{V_1}{2V_T} \tanh \frac{V_2}{2V_T} \approx I_0 \frac{V_1 V_2}{4V_T^2}, \tag{3.9}$$

where the approximation is valid if $V_1, V_2 \ll V_T$. V_T is the thermal voltage, 25.9 mV at 300 K, defined as $k_B T/q$, where k_B is the Boltzmann constant, T the absolute temperature, and q the elementary charge. Although the circuit is clearly capable of implementing the product of the two signals, the linear input range is very limited, and the temperature sensitivity is high as a result of the temperature-dependent V_T. A significant improvement of the functionality in the multiplier can be achieved by utilizing proper predistortion of the input voltage [68, 69]. The linear Gilbert multiplier is used, for example, for the read-out of an accelerometer in [62], and in a gyroscope in [63], where a folded CMOS Gilbert multiplier is used.

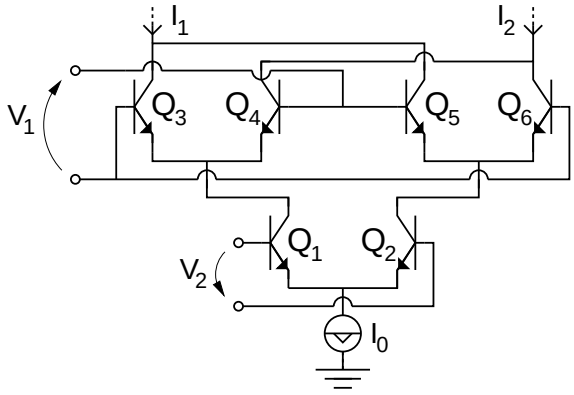

Figure 3.8: Gilbert multiplier, excluding the predistortion circuit.

The multiplier in Fig. 3.8 can also be used with a large signal carrier, V_1. Now the transistors $Q_3 - Q_6$ function as switches, in this way passing the signal current to the output with changing polarity. The operation is equivalent to that of a full-wave rectifier, which can also be implemented using switches.

A switching demodulator, a chopper, realizes full-wave rectification coherently using four switches, as shown in Fig. 3.9. Clearly, in this case the carrier must be a square wave signal, which is why it can be referred to as a clock. In addition, if the chopper is used as a full-wave rectifier, the signal and the square wave carrier must be in phase, as depicted in the example waveform shown in Fig. 3.9. The requirement is also the same for the linear multiplier i.e. the Gilbert cell.

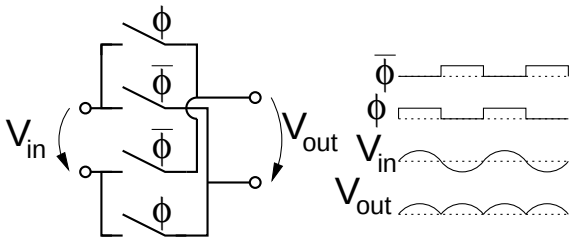

Figure 3.9: Switching demodulator.

The functionality of the chopper is mathematically equivalent to the product of the signal and a square wave carrier with unity amplitude,

$$V_{out}(t) = V_{in}(t) \sum_{n=1}^{\infty} \left[\frac{4}{\pi n} \sin\left(\omega_{det\_ac} n t\right) \right], \tag{3.10}$$

where the sum-term represents the Fourier series of the square wave carrier and $V_{in}(t)$ is the amplitude-modulated input signal. After the demodulation, the signal components of interest are located at dc, whereas the signal components at the harmonics of the carrier frequency are typically LP filtered. Let us consider an example case. Let the input signal frequency, f_s, be zero, so that $V_{in}(t) = V_s \sin\left(\omega_{det\_ac} t + \phi_e\right)$. The phase error ϕ_e represents the phase inaccuracy during demodulation and V_s the amplitude of the dc signal. After $V_{in}(t)$ has been substituted into (3.10), the resulting *dc term* can be written as

$$V_{out\_filt} = V_s \frac{2}{\pi} \cos \phi_e. \tag{3.11}$$

The equation indicates that minimizing ϕ_e is important for the maximization of the gain. On the other hand, if a signal is fully in quadrature, or $\phi_e = \pi/2$, it results in a zero dc output voltage, a feature which is especially significant in a gyroscope, where large quadrature signal components often need to be rejected [17]. A chopper, together with a square wave ac detection voltage, is used, for example, in [43] for the open-loop readout of an accelerometer. In the closed-loop accelerometer in [I, II] the detection ac voltage used is sinusoidal and the demodulation is performed via synchronous full-wave rectification. The demodulation within a closed-loop accelerometer is also discussed in more detail from the system point of view in [I, II].

Incoherent demodulation can be performed using an envelope detector, which is depicted in its simplest form in Fig. 3.10. The example waveforms in the figure show the approximate functionality of the detector. The time constant, formed by R_e and C_e, is selected in such a way that $f_{s\_max} \ll 1/(R_e C_e) \ll f_{det\_ac}$ [70]. In this way the output signal droops only slightly between the consecutive input signal peak values, but is able to follow the fastest envelope (signal) at the frequency f_{s_max} without inflicting distortion.

At first glance an envelope detector and a multiplier would both appear to fulfill the same task – demodulation. Even in the presence of additive noise $V_n(t)$, in which case the

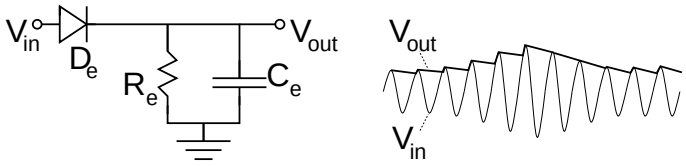

Figure 3.10: Envelope detector.

signal of the previous example can be expressed as $V_{in}(t) = V_s \sin(\omega_{det\_ac}t + \phi_e) + V_n(t)$, the performance of the two types of demodulators remains similar as long as $|V_n(t)| \ll |V_s|$. The other important limit case that must be taken into account, however, occurs when $|V_n(t)| \gg |V_s|$, which can be due to, for example, a high carrier frequency and the resulting wide noise bandwidth at the detector input and a very small signal. When the noise dominates over the signal power, the envelope detector deforms the signal, and the desired information can no longer be detected at the demodulator output. Unlike if the signal passes a coherent demodulator, the noise remains additive [70]. For this reason it is straightforward to limit the use of envelope detection to applications where the condition $|V_n(t)| \ll |V_s|$ is always met. In terms of sensor interfaces, a typical application where a rectifier-based solution is viable is the drive loop automatic gain control in gyroscopes [67].

3.1.5 Discrete-Time Detection

The original signal of interest in the case of inertial sensors is always a continuous-time analog signal, such as acceleration or angular rate. The measurable quantity, capacitance, which is proportional to the original signal of interest, is also a continuous-time analog signal. When the capacitive signal is transformed into voltage using a sampling readout circuit, the signal no longer contains the original theoretically unlimited band of information. Instead, when the signal is sampled and processed in a discrete-time readout circuit, the information is mapped in a band ranging from 0 up to $1/(T_{sa}2)$, or the Nyquist frequency [71, 72]. Hence, the sample rate $1/T_{sa} = f_{sa}$ sets the theoretical maximum signal bandwidth of a discrete-time readout.

A set of typical waveforms of an analog DT system is sketched in Fig. 3.11. The continuous-time input signal in the example is a sine, which is sampled at the rate f_{sa}, which is eleven times higher than the frequency of the sine f_{ct}. The discrete-time spectrum in Fig. 3.11 is usually plotted in such a way that $N_{sa} = f_{sa}$. It is interesting to notice that if the input signal were at the frequency $f_{sa}r + f_{ct}$, where r is an integer, the resulting spectral components of both the continuous-time sampled signals and the discrete-time signal would lie at the same frequencies as in the example. It should also be noted that a continous-time sampled signal cannot be realized in practice, and is shown just to depict the effect of sampling. Likewise, the periodic impulses that represent the continous-time

sampled signal are scaled to have a magnitude that corresponds to the input signal.

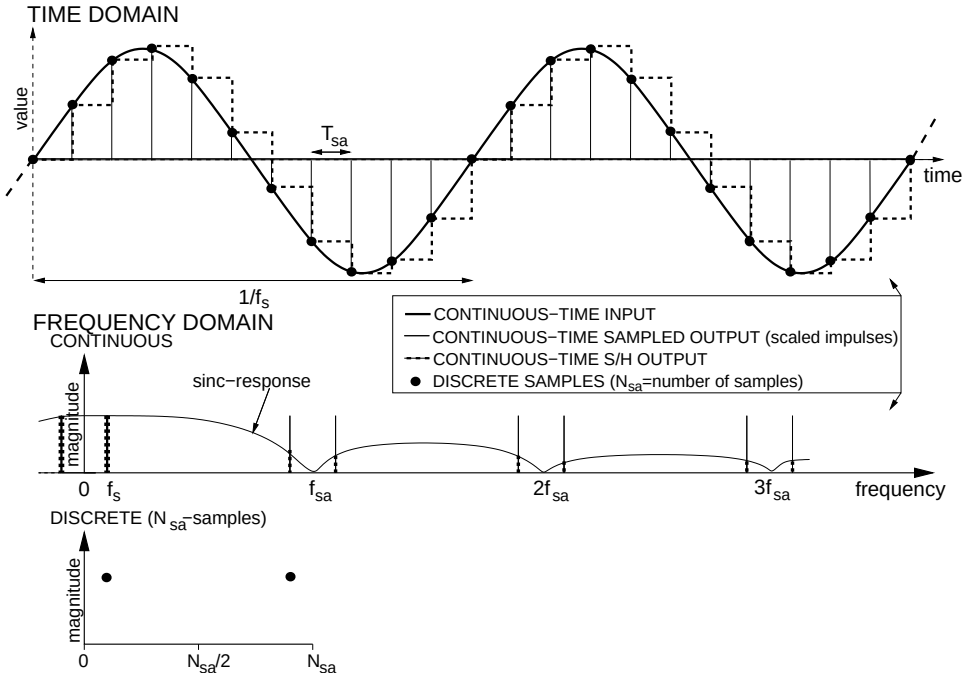

Figure 3.11: Sketched examples of both the continuous-time sampled signal, where a scaled inpulse represents the value of a sample within each clock cycle, and the corresponding S/H signal, both in the time and frequency domains. The discrete-time samples that correspond to the input signal are also shown.

A mathematical representation of the sampling [73] can be written as a product of a periodic impulse train,

$$s_{pt}(t) = \sum_{n=-\infty}^{\infty} \delta(t - nT_{sa}), \tag{3.12}$$

where impulses exist at an interval that is the same as the sampling period T_{sa}, and the continuous-time input signal $s_{ct}(t)$. The Fourier transformation of the impulse train is another impulse train in the frequency domain,

$$S_{pt}(j\omega) = \frac{1}{T_{sa}} \sum_{n=-\infty}^{\infty} \delta(\omega - n\omega_{sa}), \tag{3.13}$$

where $\omega_{sa} = 2\pi/T_{sa}$. The frequency domain representation of the sampled signal (see Fig. 3.11) corresponds to the convolution of the impulse train (3.13) and the frequency domain signal $S_{ct}(j\omega)$,

$$\begin{aligned} S_{sa}(j\omega) &= S_{ct}(j\omega) \otimes S_{pt}(j\omega) \\ &= \frac{1}{T_{sa}} \sum_{n=-\infty}^{\infty} S_{ct}(j\omega - jn\omega_{sa}). \end{aligned} \tag{3.14}$$

Now the continuous-time sampled signal in the frequency domain $S_{sa}(j\omega)$ is equivalent to the sum of the original signal spectra each shifted by $n\omega_{sa}$. If the frequency of the CT input signal is higher than $\omega_{sa}/2$, folding will occur. The high-frequency signal components that are susceptible to folding are typically removed by antialias filtering before the sampling is performed. In the readout of a sensor element care must be taken not to allow noise or other high-frequency components, for example, in the detection voltage or supply, to fold to the signal band.

If the output of a sampling system is to be used as a continuous-time signal, the sampled output is typically fed through a zero-order hold. An example of the resulting output, typically referred to as a *sample-and-hold-* (S/H)-response, is shown in Fig. 3.11. The frequency domain representation of the S/H signal can be derived from the time domain waveform of the same signal.

A single value of the continuous-time input signal is expressed as $s_{ct}(nT_{sa})$, which is equal to the value of $s_{ct}(t)$ at $t = nT_{sa}$. The discrete-time signal can be turned into a continuous-time signal by using the samples of the discrete-time input signal. When each sample is represented as a pulse, the complete set of pulses that forms the continuous-time signal can be written as

$$s_{sah}(t) = \sum_{n=-\infty}^{\infty} s_{ct}(nT_{sa})[u(t - nT_{sa}) - u(t - nT_{sa} - \tau)], \tag{3.15}$$

where $u(t) = 1$ for $t \geq 0$ and $u(t) = 0$ for $t < 0$. Now (3.15) can be written in the Laplace domain as

$$S_{sah}(s) = H_{sinc\_\tau}(s) \sum_{n=-\infty}^{\infty} s_{ct}(nT_{sa})e^{-snT_{sa}} = H_{sinc\_\tau}(s)S_{sa}(s), \tag{3.16}$$

where

$$H_{sinc\_\tau}(s) = \frac{1 - e^{-s\tau}}{s} \tag{3.17}$$

forms the *sinc* response in the S/H output, when the pulse length τ is equal to T_{sa}. Hence, the corresponding gain transfer function of (3.17) can be written as

$$G_{sinc}(\omega) = T_{sa}\frac{\sin \omega T_{sa}/2}{\omega T_{sa}/2}, \tag{3.18}$$

where $G_{sinc}(\omega) = |H_{sinc\_\tau}(j\omega)|$ for τ equal to T_{sa}. The significance of the term $S_{sa}(s)$ can be explained by calculating (3.16) when τ is equal to zero.

The value of $H_{sinc\_\tau}(s) = \tau$ when τ approaches zero. In this case (3.16) can be written as

$$S_{sa}(s) = \sum_{n=-\infty}^{\infty} s_{ct}(nT_{sa})e^{-snT_{sa}} = \frac{S_{sah}(s)}{\tau} \; |_{\tau \to 0} \; . \tag{3.19}$$

Now that $S_{sah}(s)$ is normalized by the duration (τ) of the pulses which approaches zero, (3.19) represents, in fact, an impulse train. The result is equivalent to (3.14), where a product of the impulse train and the input signal was used to form the frequency domain representation of the sampled spectrum. Hence, the sinc term can be seen to attenuate the high-frequency signal components, as is also depicted in the spectrum in Fig. 3.11.

The infinite sum (3.19) can also be used to calculate the z-transformation of the input signal by substituting $e^{sT_{sa}} = z$. On the other hand, transfer functions can be constructed in the z-domain using the shifting property; $v(n - n_0) \leftrightarrow z^{-n_0}V(z)$. For example, for the simple integrator in Fig. 3.12 [73], the current output voltage can be written as the difference between the previous output value and the delayed input value, $v_{out}(n) = v_{out}(n-1) - v_{in}(n-1)$. The same can be written in the z-domain as $V_{out} = V_{out}z^{-1} - V_{in}z^{-1}$. In this case the transfer function $H(z) = V_{out}(z)/V_{in}(z) = -z^{-1}/(1-z^{-1})$. The

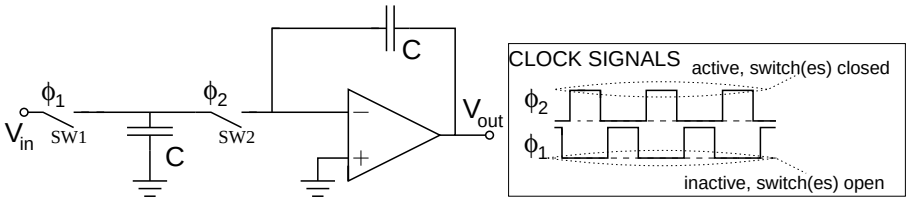

Figure 3.12: A simple integrator with equally-sized capacitors. The clock signals are drawn as non-overlapping to emphasize the fact that the switches do not conduct simultaneously.

frequency response $H(j\omega)$ of a z-domain transfer function can be obtained by substituting $z = e^{-j\omega T_{sa}}$ into the z-domain transfer function. The frequency $z = -1$ corresponds to the Nyquist frequency, and hence, the frequency response for a discrete-time circuit is usually plotted up to the frequency $\omega = \pi/T_{sa}$. A more detailed introduction to the topic can be found in, for example, [73] or [74].

Another significant factor in defining the sample rate, in addition to the folding of undesired spurious tones, is the noise. The *voltage density* of the white thermal noise, or Johnson-Nyquist noise [75, 76], of a resistor can be written as

$$V_n^2 = 4k_BTR, \tag{3.20}$$

where k_B is the Boltzmann constant, T the absolute temperature, and R the resistance. When the resistor, in a switched-capacitor (SC) circuit typically represented by a conducting switch, is placed in series with a capacitor, the rms noise voltage of the capacitor is equal to

$$V_{n\_rms}^2 = kT/C, \tag{3.21}$$

where C is the capacitance and is independent of the resistance. When the switch is opened the noise will fold. The resulting rms noise, (3.21), is therefore often called *switch noise* or *kT/C noise*. The total rms noise power in the discrete-time signal will

concentrate at a frequency band ranging from 0 to the Nyquist frequency, $1/(2T_{sa})$, and the rms noise voltage can be written back to the rms noise density as

$$V_{n\_sa}^2 = 2T_{sa}kT/C. \tag{3.22}$$

The condition for the noise density being flat, i.e. frequency independent, and (3.22) being valid is that $T_{sa} \gg RC$. Clearly, the higher the sample rate, the lower the noise density of the discrete-time signal. The folding of noise is typically also a reason to avoid the use of discrete-time readout in cases where extremely low noise levels are required. For example, in [I, II] the continuous-time loop was chosen over a discrete-time one in order not to allow the folding of noise to degrade the performance. Similarly, in [VI] the sampling is not performed until the noise bandwidth is properly limited.

Now the sampling operation and resulting folding can also be taken advantage of. *Sub-sampling* is performed when high-frequency signals are deliberately converted to lower frequencies, i.e. the frequency of the input signal is allowed to be higher than the sampling frequency. When considering sensor interfaces, this can be utilized in, for example, resonating sensors [26] such as gyroscopes by taking only one sample per period of the carrier f_c. If the sampling is set correctly to occur at the maximum value of the signal, the resulting sampled output corresponds directly to the amplitude of the input signal. This feature is applied, for example, for the amplitude control of the drive loop of the gyroscope in [VII] and also for the pseudo-continuous-time secondary readout in [VI].

The following sections introduce different structures for the open-loop discrete-time readout of capacitance, including mostly conventional SC circuits but briefly also a few switched-current (SI) methods.

3.1.6 SC Amplifiers with CDS and Chopper Stabilization for the Detection of Capacitances

SC buffers are easy to adapt for the readout of capacitive sensors. The technique allows the signal capacitances to be detected by first biasing them to a known voltage and then moving the charge from the sensor to a reference capacitor, the value of which is known. This procedure allows the value of the unknown sensor capacitor to be converted to voltage with a well-determined gain. The operation of a typical SC circuit is examined next through example circuits.

A basic SC amplifier for the detection of a capacitive half-bridge element is shown in 3.13. The switches $SW1$ and $SW2$ bias the sensor capacitor C_{s1} to the dc voltage V_m and C_{s2} to the dc voltage $-V_m$ in the clock phase ϕ_1. At the same time the feedback capacitor C_{fb} is reset or zeroed. When the phase ϕ_2 begins, the amplifier moves the charge from the

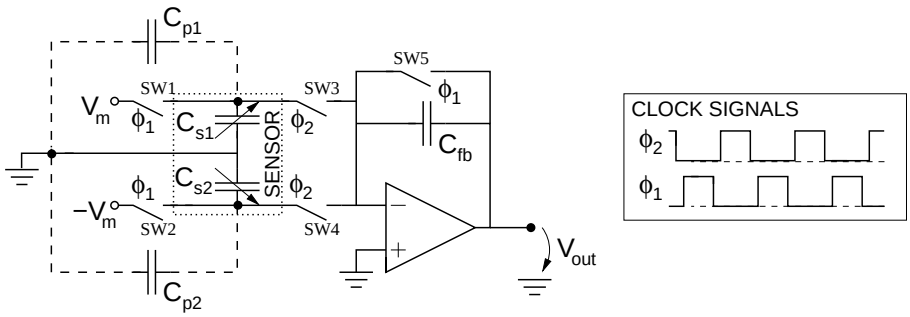

Figure 3.13: The detection of a half-bridge sensor using an SC voltage buffer.

sensor capacitors in such a way that the voltage across C_{s1} and C_{s2} becomes zero. The total charge moved from the sensor capacitors is equal to

$$Q = V_m C_{s1} - V_m C_{s2}. \tag{3.23}$$

The charge is moved via C_{fb}, which will receive the charge $-Q$. Now the output voltage at the end of ϕ_2 is equal to

$$V_{out} = V_m \frac{C_{s2} - C_{s1}}{C_{fb}}. \tag{3.24}$$

The gain from the capacitive information $C_{s2} - C_{s1}$ to the output voltage V_{out} is, hence, V_m/C_{fb}. It is important to notice that the circuit in Fig. 3.13 is also sensitive to parasitic capacitance at the switched nodes of the sensor capacitors. As these potentially existing parasitics, C_{p1} and C_{p2}, are taken into account, (3.24) can be written as

$$V_{out} = V_m \frac{C_{s2} + C_{p2} - (C_{s1} + C_{p1})}{C_{fb}}. \tag{3.25}$$

The circuit in 3.13 can be improved, regarding the flicker noise and offset of the operational amplifier or unbalanced references V_m and $-V_m$, by applying the *chopper stabilization* technique. The resulting circuit [77] is shown in Fig. 3.14. Now the detection of the capacitance is performed by periodically inverting the voltage V_m, which defines the detection voltage. In this example the chopping rate is half of the sampling frequency, which is a typical design choice and simple to implement. Now the voltage at the amplifier output in the phase ϕ_2 is modulated at the chopping frequency and needs to be down-converted. In [77] the demodulation is performed by sampling the amplifier output using two S/H circuits, one sampling at ϕ_{2a} and the other one sampling at ϕ_{2b}. The two S/H blocks thus allow a differential continuous-time S/H output. The rising edges in the clock phases ϕ_{2a} and ϕ_{2b} are delayed so that the amplifier has settled before the signal is transferred to the S/H blocks. In this way the S/H output could be used as a continuous-time one with improved linearity. The differential output voltage of the amplifier in Fig. 3.14 is

$$V_{out} = 2V_m \frac{C_{s2} - C_{s1}}{C_{fb}}. \tag{3.26}$$

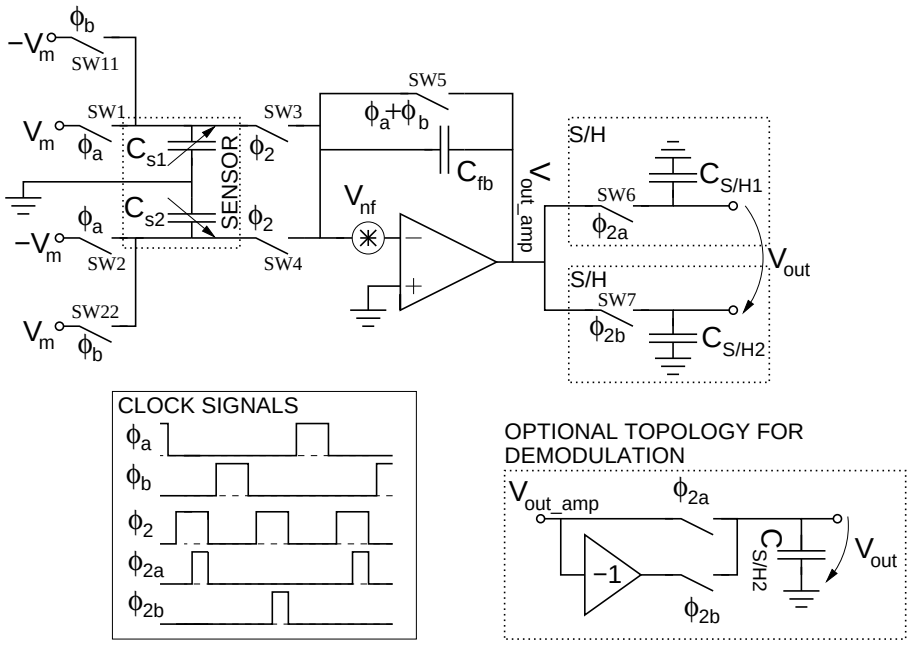

Figure 3.14: A chopper-stabilized SC voltage buffer in [77], together with an optional topology for the realization of the demodulation.

The low frequency noise source V_{nf} in Fig. 3.14, which illustrates the input-referred flicker noise and offset of the operational amplifier, will not appear modulated at the output of the amplifier V_{out_amp}. Instead, when the S/H circuits sample the voltage to both negative and positive branches consecutively, the error will appear as common-mode error at the final differential output. Transforming the noise into common-mode error is possible as the frequency of the error is low compared with the chopping frequency, and the change in V_{nf} from ϕ_{2a} to the next ϕ_{2b} is negligible. A detailed analysis of the circuit, including the noise analysis, is given in [77].

The circuit in Fig. 3.14 is in fact an unconventional chopper-stabilized circuit in the sense that the single-ended output is converted into differential form. A more common approach, especially in differential circuits, is to change the polarity of the output in order to demodulate the chopped signal. This way the signal that is upconverted as a result of the chopping, returns to the original signal frequency, while the low-frequency noise V_{nf} that appears directly at the amplifier output becomes upconverted and is therefore removed from the signal band. The approach is also depicted in Fig. 3.14, where an inverting unity gain buffer makes possible the demodulation of the single-ended amplifier output signal. Now it is important to notice that the upconverted noise and offset will remain, unlike in the original demodulator in Fig. 3.14, as part of the output signal, unless an LP filter is applied to remove the carrier frequency components.

Chopper stabilization can be applied in SC circuits with very little or no additional noise, which is because additional noisy switched capacitors are not required for the implementation. The same technique for the reduction of non-idealities in operational amplifiers is also available for continuous-time circuits. In fact, the use of an ac detection voltage, together with demodulation, is equivalent to chopper stabilization. The non-idealities associated with chopper stabilization are introduced in detail in [78] and also discussed in [II] in relation to continuous-time demodulation in a closed-loop accelerometer.

Another SC amplifier utilized as a front-end for the open-loop readout of an accelerometer is shown in Fig. 3.15 [79]. Here the half-bridge element is read differentially, in such a way that the common node of the capacitors $C_{s1}+C_{s2}$ is switched. In order for this configuration to be practical, a set of reference capacitors C_r is required. If these capacitors are omitted, the detection voltage, and the resulting signal charge, become dependent on the value of the feedback capacitances C_{fb} and the sensor capacitances. The behavior of the gain could therefore be compared to the continuous-time front-end using ac detection voltage in Section 3.1.3.

When the capacitors C_r are properly sized, $C_{r1} = C_{r2} = (C_{s1}+C_{s2})/2$ and the common-mode voltage at the nodes $N1$ and $N2$ will remain at $V_{DD}/2$. The differential output voltage will be equal to

$$V_{out} = V_{DD}\frac{C_{s1} - C_{s2}}{C_{fb}}. \tag{3.27}$$

Sensitivity to parasitic capacitances C_p exists only if the value of C_r is incorrect and a common-mode signal exists in the nodes $N1$ and $N2$. The accelerometer in [79] was further improved in [80] by the redesign of the sensor element. The single differential pair of capacitors was replaced by two differential pairs, because of which the reference capaci-

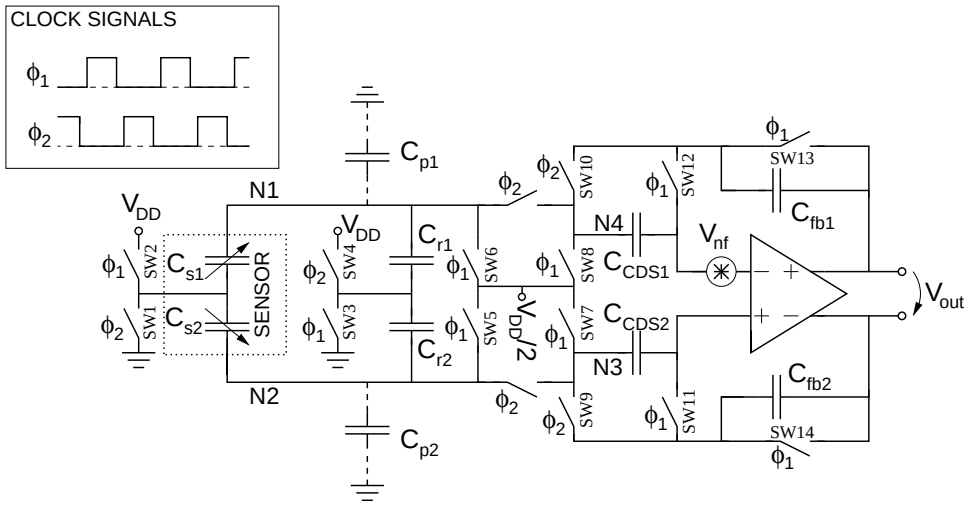

Figure 3.15: A simplified differential SC voltage buffer, the original version of which is presented in [79].

tors C_r can be replaced by the additional pair of sensor capacitors. Hence, two integrated capacitors less are required for the interface, which is significant as the reference capacitors had to be well matched with the sensor capacitors and required calibration. However, as all the capacitors will have one common node (seismic mass) and the original topology in Fig. 3.15 cannot be used, the switching of the element in [80] is equivalent to that in Fig. 3.13.

In Fig. 3.15 the additional capacitors C_{CDS} are included in order to implement the *correlated double sampling* (CDS) -technique. The functionality of CDS in this example can be depicted with the help of the low-frequency noise source V_{nf}. In the phase ϕ_1 the switches $SW7$, $SW8$, $SW11$, and $SW12$ are conducting and allow the current value of V_{nf} to be stored into the capacitors C_{CDS}. The noise can be assumed to be constant between two adjacent clock phases. Hence, in the next clock phase ϕ_2 the voltage between the nodes $N3$ and $N4$ is free of V_{nf}, the value of which was stored into the capacitors C_{CDS} with different polarity. By the end of ϕ_2 the capacitors C_{CDS} function as floating voltage sources and allow the nodes $N3$ and $N4$ to form a virtual ground, and consequently V_{out}, free of V_{nf}.

The CDS technique does not allow the perfect attenuation of low-frequency noise sources, such as flicker noise. Instead the transfer function from the low-frequency noise source to the output voltage can be approximated as a first-order high-pass transfer function, where the zero is at dc. In modern MOSFETs the flicker noise corner, referring to the frequency where the powers of white and flicker noise are equal, can be several MHz. Although in typical analog circuits the corner is below 100 kHz, the efficient realization of CDS or chopper stabilization still sets moderately high requirements for the clock or carrier frequency. Additional non-idealities and a more detailed introduction to the error reduction techniques can be found in [78], together with several example circuits.

The pseudo-CT interface in [VI] is designed to realize both the implementation of the CDS and chopper stabilization. However, as the interface operates close to the resonance frequency of the primary resonator, the frequency is insufficient for the efficient removal of the flicker noise. Instead, the closed-loop accelerometer in [I, II] utilizes a 3 MHz carrier frequency, much higher than the flicker noise corner of the readout circuits. At the same time, high gain preceding the demodulation will reduce the effect of the flicker noise after the demodulation.

3.1.7 Self-Balancing Capacitor Bridge

All the front-end circuits for capacitive parallel-plate interfaces introduced so far necessitate the condition $x \ll x_0$, in order not to have the sensor output distorted by the electrostatic forces. This is due to the fact that the capacitive signal is detected using a *constant*,

either dc or ac, detection voltage. It is important to notice that as a result of the squared voltage dependency, a non-zero average electrostatic force is also created by the mere ac detection voltage. The electrostatic forces can be made constant in the parallel-plate interfaces by utilizing an SC circuit that is capable of performing charge-balanced operation. An example of a circuit that realizes both a ratiometric readout and charge-balanced operation is shown in Fig. 3.16 and was originally published in [81]. The circuit shown in the figure omits the measures taken in [81] to reduce clock feedthrough and offset, but still allows proper functionality.

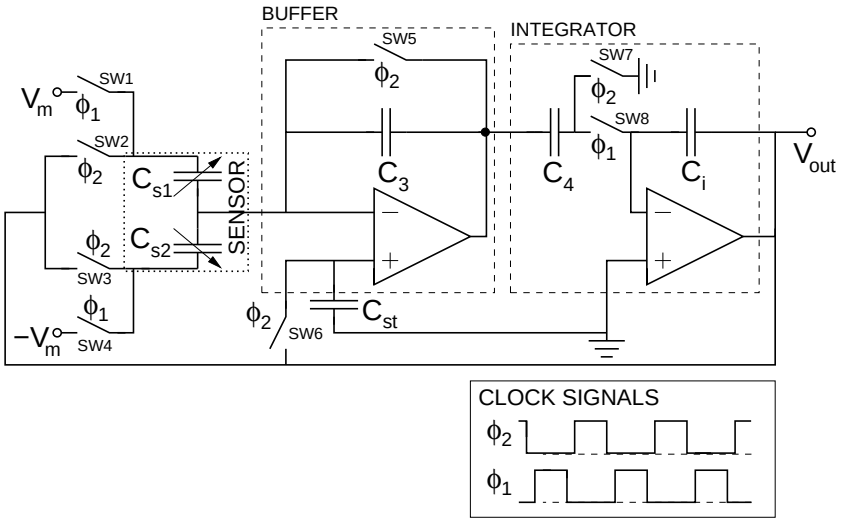

Figure 3.16: A self-balancing capacitor bridge.

The circuit operates in the two clock phases ϕ_1 and ϕ_2. In the phase ϕ_2 all three nodes of the half-bridge sensor element are biased to the output voltage V_{out}, which is held constant by the integrator. The capacitors C_4 and C_{st} are also biased to the voltage V_{out}. When the clock phase ϕ_2 ends, the voltage stored in the capacitor C_{st} is sampled to the value provided by the integrator. As the phase ϕ_1 begins, the buffer stage feeds the voltage sampled in C_{st} to the sensor capacitors in such a way that the capacitors C_{s1} and C_{s2} are biased to the voltages $V_m - V_{out}$ and $V_{out} + V_m$, respectively. The charge that is required to bias the sensor capacitors flows through C_3 and changes the output of the buffer. The voltage shift at the buffer output is converted to a charge in C_4. The charge is integrated in C_i, the value of which now becomes updated, and transferred to C_{st} when the next ϕ_2 begins. After several clock cycles, and assuming that the feedback in the loop is negative, the integrator output V_{out} has settled to a finite value and the input to the integrator is zero. This denotes the fact that the charge from the sensor element, transferred during the phase ϕ_1, also approaches zero. Hence, after the settling of the loop, the charges in the two sensor capacitors C_{s1} and C_{s2} have been balanced and in the phase ϕ_1

$$(V_m - V_{out})C_{s1} = (V_m + V_{out})C_{s2}. \tag{3.28}$$

The circuit also allows a ratiometric readout, which can be seen when (3.28) is rewritten

as

$$V_{out} = V_m \frac{C_{s1} - C_{s2}}{C_{s1} + C_{s2}}. \tag{3.29}$$

Clearly, the charge balance is not achieved instantaneously. Instead V_{out} can be written in the z-domain as

$$V_{out}(z) = \frac{[(C_{s1} - C_{s2})(z)]V_m z}{(z-1)C_3 C_i/C_4 + C_{s1} + C_{s2}}, \tag{3.30}$$

which is equal to (3.29) at dc, i.e. when $z = 1$ and all the parameters correspond to those in Fig. 3.16. Only the differential signal capacitance $(C_{s1} - C_{s2})(z)$ is approximated to be time-dependent. V_{out} is an LP function of the signal, which can be seen in (3.30), where the single pole is at $z_p = 1 - C_4(C_{s1} + C_{s2})/(C_3 C_i)$.

The properties of the circuit can also be examined by means of an example. Now the following parameters are set for the example case: $C_3 = C_4 = C_i/10 = C_{s1}/1.1 = C_{s2}/0.9 = 1$ pF and $V_m = 1$ V. The output dc voltage can be calculated using (3.29) as being equal to 0.1 V, and the pole is located at $z_p = 0.8$. If it is assumed that the clock frequency $1/T_{sa}$ is equal to 10 kHz, the $-3dB$-frequency of (3.30) is 355 Hz. An increase of an order of magnitude in the clock frequency increases the $-3dB$-frequency by the same amount and, hence, the signal bandwidth of the bridge can easily be increased to cover the frequency band of interest in, for example, an accelerometer.

A self-balancing bridge allows charge-balanced operation of the sensor element, together with a ratiometric readout, which is why it offers the biggest benefits when applied in, for example, an accelerometer, where the signal capacitance can be substantial compared to the static capacitances of the sensor element. Both the original interface in [81] and the electronics presented in [82] are applied for the readout of an accelerometer. In the latter reference the single bridge is multiplexed for four half-bridge sensors and implemented as a differential circuit.

3.1.8 $\Delta\Sigma$ ADCs for Sensor Open-Loop Readout

The interconnection between the analog world surrounding us and the increasingly digital computerized world requires data to be converted between the two realms. Analog information is converted into digital with the help of analog-to-digital converters (ADC), and digital-to-analog converters (DAC) are utilized for the inverse process. While ADCs and DACs have been and continue to be, under active global research, the topic is reviewed here only to provide the reader with an idea of how a single category of ADCs, $\Delta\Sigma$ ADCs, adapts well to the readout of capacitive sensors.

In discrete-time circuits the signal is discretized in time, whereas the amplitude of the signal is still continuous, i.e. it can attain all real values within the signal range. The ADC will perform both the sampling, if this has not already been performed in discrete-time analog circuits, and the *quantization*, the mapping of the continuous values of the signal to 2^{N_B} discrete levels represented by N_B bits. In a $\Delta\Sigma$ ADC the number of levels can be as small as two, i.e. the ADC has a 1-bit output.

$\Delta\Sigma$ ADCs belong to the group of *oversampling* converters. Oversampling refers to the output data rate, which is deliberately set to be considerably higher than the signal bandwidth of interest. Quantization, especially using a 1-bit quantizer, introduces significant error to the digital signal. This error, which behaves usually as a random signal, is referred to as *quantization noise*. In a $\Delta\Sigma$ ADC an analog loop filter is utilized to shape the quantization noise away from the signal band of interest. Digital filtering that follows the $\Delta\Sigma$ ADC then allows the quantization noise to be removed, the digital word length (unity for a 1-bit output) increased, and the sample rate reduced.

The efficiency of the noise shaping in a $\Delta\Sigma$ ADC varies, depending on the design of the loop filter. Two example block diagrams of $\Delta\Sigma$ ADCs, or in fact one ADC with two different loop filter structures, are shown in Fig. 3.17. The loop filter of the modulator has two inputs, the signal S_{in} and the feedback. The feedback carries, in addition to the actual feedback signal, an undesired component, the quantization noise N_Q, which is injected into the loop when the signal is quantized. The transfer of the noise to the digital output D_{out}/N_Q is described by the *noise transfer function* (NTF), which is defined by the loop filter. The *oversampling ratio* (OSR), the ratio of half the sample rate and the signal bandwidth $f_{sa}/(2f_{sbw})$, together with the signal-to-quantization noise ratio (SQNR), sets the requirements for the NTF. In oversampling converters OSR is typically much higher than unity.

A single-bit quantizer, a comparator, allows high linearity of the ADC together with a

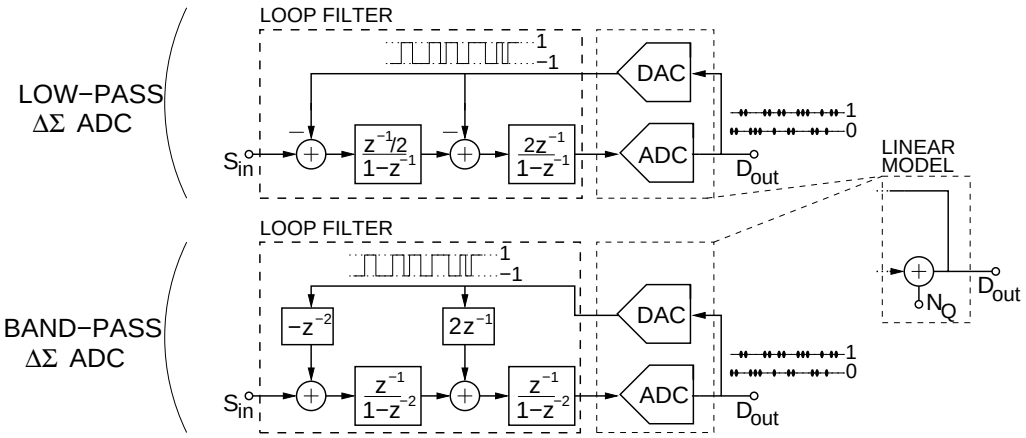

Figure 3.17: Two examples of $\Delta\Sigma$ ADCs, a low-pass and a band-pass $\Delta\Sigma$ ADC.

simple design, at the expense of more unpredictable dynamic properties of the loop and higher quantization noise [83]. Compared to multi-bit quantizers, the linearity of 1-bit feedback DACs is independent of the matching of components. In eletromechanical $\Delta\Sigma$ modulators (see Section 3.2.3) the importance of the inherently linear single-bit DAC is further emphasized.

In the example modulators in Fig. 3.17 a single-bit quantizer is used. The low-pass characteristics of the example modulator are realized by the two integrators in the loop. By using the coefficients and the linear model of the combined ADC and DAC shown in Fig. 3.17, the NTF can be written in the z-domain as

$$NTF(z) = D_{out}/N_Q = (1 - z^{-1})^2. \tag{3.31}$$

According to the result, the quantization noise is transferred to the output through a cascade of two derivators. The same result can also be observed from the spectrum shown in Fig. 3.18, where the quantization noise increases by 40 dB per decade of increase in frequency. The signal, on the other hand, is only delayed, and the *signal transfer function* (STF) can be written as

$$STF(z) = D_{out}/S_{in} = z^{-2} \tag{3.32}$$

for the LP $\Delta\Sigma$ ADC in Fig. 3.17.

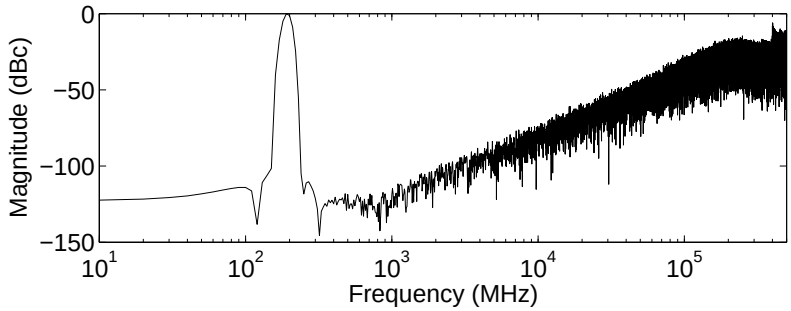

Figure 3.18: An example spectrum for the ideal second-order LP $\Delta\Sigma$ ADC with a 1-bit quantizer. (10^5-point FFT, Kaiser window ($\beta = 13$), 1-MHz sample rate (f_{sa}), -14 dB full-scale sine at 193 Hz)

The LP characteristics of the modulator can be transformed to band-pass (BP) by replacing the integrators of the loop filter with resonators. An example of a fourth-order BP $\Delta\Sigma$ ADC is also shown in Fig. 3.17, for which an example spectrum is shown in Fig. 3.19. Now the input sine is moved to the notch frequency, where the quantization noise is minimized.

For a typical ADC the input signal S_{in} is a voltage-mode signal and the ADC is realized as an SC circuit. An LP $\Delta\Sigma$ ADC, with a voltage-mode input, can for example, be utilized for the digitization of an analog output of an accelerometer, as is done, for example, in

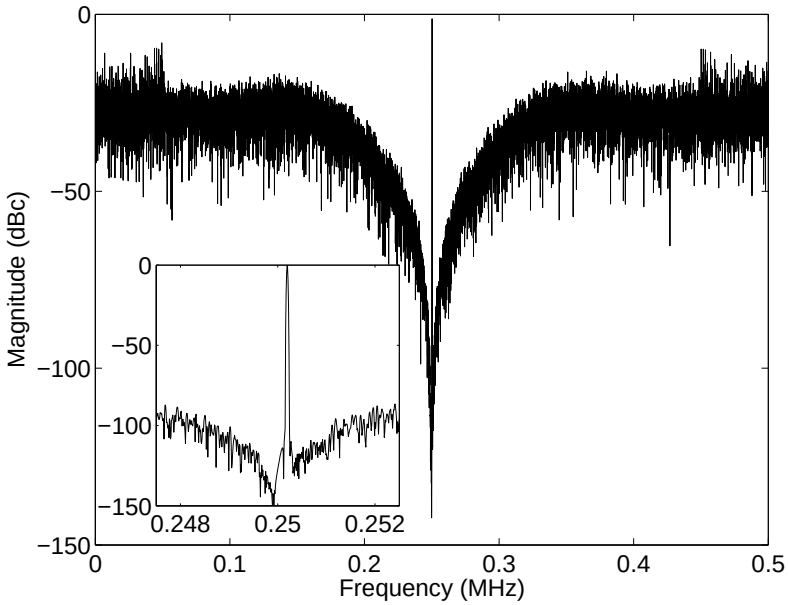

Figure 3.19: An example spectrum for the ideal fourth-order band-pass $\Delta\Sigma$ ADC with 1-bit quantizer. The inset figure shows a 4-kHz region around the notch frequency. (10^5-point FFT, Kaiser window ($\beta = 13$), 1-MHz sample rate (f_{sa}), -14 dB full-scale sine at 193+f_{sa}/4 Hz)

[79, 84] for a discrete-time signal and in [III] for a continuous-time high-resolution analog signal. In [III] the design of the buffer that drives the sampling capacitors of the ADC is also reported.

The BP $\Delta\Sigma$ ADC is suitable for digitizing a narrow signal band located off the dc, and, for such signals, reduces the necessary sample rate compared to an LP $\Delta\Sigma$. Signals of the aforementioned type can be found, for example, in vibratory gyroscopes, where the narrow signal band is located, before demodulation, at the carrier frequency f_c, provided that a dc detection voltage is applied. In this case the use of a single BP $\Delta\Sigma$ ADC allows the demodulation of both in-phase and quadrature signal to be performed digitally, assuming the sampling clock is properly synchronized with the input signal [58]. A thorough introduction to $\Delta\Sigma$ ADCs and DACs can be found in [83].

Although a typical ADC samples a voltage, or current mode information, the $\Delta\Sigma$ ADC can also be used to directly digitize the value of a capacitor, or capacitors. This approach is depicted in the schematic shown in Fig. 3.20, which was originally published in [85]. In the first-order LP $\Delta\Sigma$ ADC shown in the figure, the sampling capacitor and the reference capacitor are replaced by a capacitive half-bridge element. The operation of the interface requires two clock phases, which are shown in Fig. 3.20. Depending on the value of the output bit, either C_{s1} or C_{s2} is biased to the reference voltage in such a way that C_{s1} creates a positive and C_{s2} a negative shift in the integrator output voltage. The clocked comparator, COMP, creates a new output value at the rising edge of ϕ_2 and keeps that

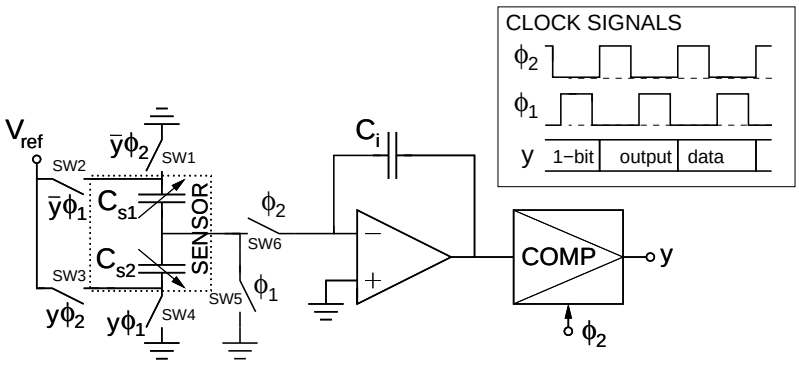

Figure 3.20: A $\Delta\Sigma$ ADC for direct capacitance-to-digital conversion.

value until the next rising edge. When the operation is considered for a long period of time, the average current to the ideal integrator must be zero. Hence, for a continuous operation with constant capacitors, the charge transferred from both sensor capacitors must be equal in order for the integrator output to be finite. Therefore

$$V_{ref}C_{s1}(1 - B_{ave}) = V_{ref}C_{s2}B_{ave}, \tag{3.33}$$

which can be rewritten as

$$B_{ave} = \frac{C_1 - C_2}{2(C_1 + C_2)} + \frac{1}{2}, \tag{3.34}$$

where B_{ave} corresponds to the average value of the output bit stream y and the single bit output (1 and 0 for logic high and low) has an offset equal to 1/2. As (3.34) indicates, the average bit stream allows ratiometric capacitive detection of the signal capacitances and, in addition, is completely independent of the dc reference voltage V_{ref}. If the settling time in both clock phases is very small compared to the whole clock period, the charge balance of the capacitive half-bridge is also maintained. Hence, the $\Delta\Sigma$ ADC in Fig. 3.20 can be used to realize a low-complexity and low-power charge-balancing capacitive readout with a one-bit digital output.

Althought the first-order $\Delta\Sigma$ interface in Fig. 3.20 allows dc capacitance difference to be detected correctly, the dynamic operation, including the quantization noise shaping, can be considerably improved by increasing the order of the loop filter. For example, a second-order filter is proposed both in [85] and in [15] to realize a $\Delta\Sigma$ interface for a single- and three-axis accelerometer, respectively.

3.1.9 Current-Mode Readout of Capacitive Signals

Maintaining the charge of the detection capacitors constant would also allow constant electrostatic forces in a parallel plate capacitor, and thus reduced non-linearity and an increased operating range. In addition to SC circuits, current-mode readout can also offer

charge-balanced operation. However, it is problematic to create a constant charge using continuous-time methods and hence the charge is periodically refreshed, first by resetting the capacitor and second by feeding a new charge packet.

The approach of periodically refreshing the charge has been applied in, for example, [86], where the circuit shown in Fig. 3.21 is applied for the readout of a capacitive pressure sensor. The circuit operates in three phases: first, the switch $SW1$ conducts and feeds a fixed amount of charge to the sensor; second, both switches are open and the buffer detects the voltage across the sensor, and third, the switch $SW2$ zeroes the charge of the capacitor. The operating cycle is repeated at the rate determined by the leakage current through the switches, which causes the voltage to drift in the hold phase. The constant charge operation allows the sensor to be biased to the region where the position-to-capacitance sensitivity is higher compared to the voltage mode readout. In [86] discussion on other performance parameters, such as noise and linearity, is omitted.

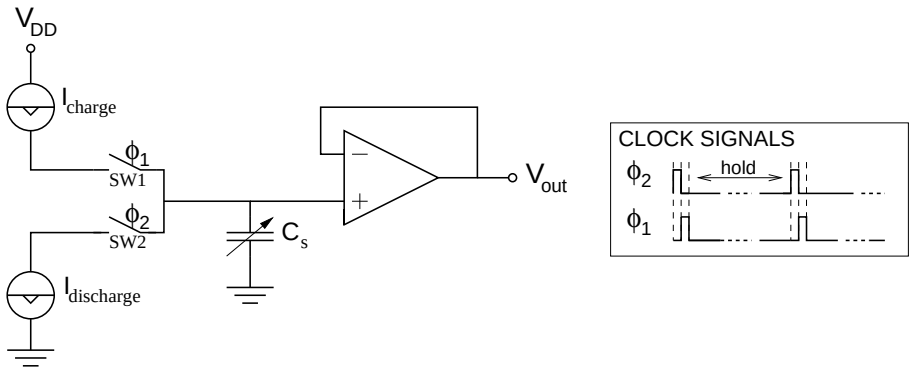

Figure 3.21: A block diagram of the readout circuit in [86].

The readout circuit in [87], where a constant current source is used to detect the signal capacitance, is shown in Fig. 3.22. Unlike in the previous example, here the clock frequency is considerably higher than the signal bandwidth. The circuit operates in two phases, reset and measure. In the measuring phase a constant current I_{charge} is fed through the reference capacitor C_r and the sensor C_s. The current resulting from the difference between the capacitors is transformed to voltage in the feedback components Z_{fb}. The voltage at the amplifier output can be sampled as soon as the voltage is settled. The capacitance-to-voltage response of the readout is non-linear for a single-ended capacitive signal, but will be linearized for a differential sensor. The effect of various non-idealities is analyzed in [87], but the discussion of the effect of electrostatic forces is omitted.

The detection of capacitive accelerometers and gyroscopes using switched-current (SI) techniques, for which the driving factor is mainly the possibility of using low-cost CMOS technologies with no passive analog components, is uncommon. However, an accelerometer has been interfaced using an SI front-end and an SI $\Delta\Sigma$ ADC in [88]. The actual

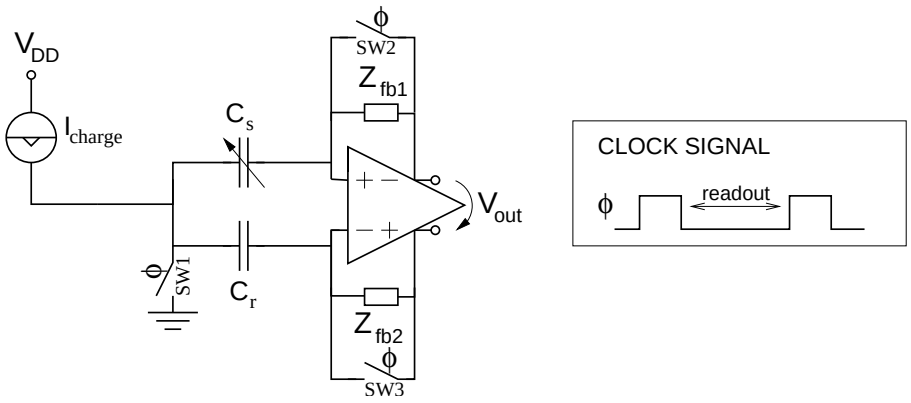

Figure 3.22: A block diagram of the readout circuit in [87].

capacitance-to-current conversion is performed using voltage-mode biasing and the linearity of the implementation is limited to below 40 dB.

3.1.10 Pseudo-CT Open-Loop Readout

In Sections 3.1.2 and 3.1.3 it became clear that the dc biasing in the amplifying stages of CT interfaces forces finite but very high resistances to be used in order to properly dc bias the active structures in the presence of leakage currents. Large resistors can result in an increased silicon area, parasitic capacitances, and non-linearity. In addition, after the detection of the capacitive signal, the voltage mode information must be demodulated.

Switched-capacitor interfaces, on the other hand, are prone to increased noise as a result of folding, but do not require demodulation at all or allow it to be performed by applying subsampling. The effect of the folding of the noise can also be decreased, for example, by increasing the signal level. However, if the magnitude of the signal charge needs to be increased by resorting to on-chip high-voltage generation, the active switching of the high-voltage node, which is necessary in SC circuits, requires a fairly low-impedance high-voltage source. The implementation of a low-impedance local high-voltage source typically increases power consumption or forces external components to be used. High-voltage generation is discussed in more detail in Section 5.

Especially in gyroscopes, where only a tiny signal results from the Coriolis force, the electrostatic forces are not likely to inflict distortion and the use of dc a detection voltage is efficient. The pseudo-CT readout allows a constant bias voltage to be maintained across the sensor capacitors while performing the signal detection by periodically integrating the current obtained from the element. The sampling is performed after the signal has been amplified to its final magnitude and the noise bandwidth has been limited. Periodic integration makes possible inherent demodulation, chopper stabilization and CDS. In its

simplest form, the pseudo-CT readout could be realized using just a single active gain stage followed by an SC stage to sample the output of the pseudo-CT stage. An example of this type of very simple front-end is shown in Fig. 3.23.

In the figure a continuous sinusoidal current is fed to the amplifier. The amplifier is designed to be very fast and low-noise and therefore also has a wide noise bandwidth. The amplifier is also capable of transforming the current to its final magnitude using a very small feedback capacitor C_1. Now, in order for the signal amplitude to be capable of being extracted without folding all the noise of the amplifier, the noise bandwidth should be limited before sampling. The resistor R_1 is added for this purpose. The extraction of the signal amplitude or, in fact, the peak-to-peak value starts by resetting the sampling capacitor C_3 in phase ϕ_2. The reset phase ends at the time when the minimum value at the amplifier output is reached (zero value of the input current), and the current flowing through R_1 is directed to C_3. As the current, which is now band-limited in R_1, is integrated for half a period, i.e., the whole negative half-period of the input current, a peak-to-peak value of the signal is extracted by the end of ϕ_3, assuming that the capacitive voltage division between C_2 and C_3 is small enough. The sampled value is available in ϕ_1 and free of the amplifier offset and switch noise, which were stored in C_2 in phase ϕ_2. The periodic reset ϕ_1 allows proper dc feedback to be maintained in the amplifier and no linear resistors are required for this purpose. A detailed analysis of the readout technique is presented in [VI], and a complete gyroscope utilizing the pseudo-CT technique is introduced in [V].

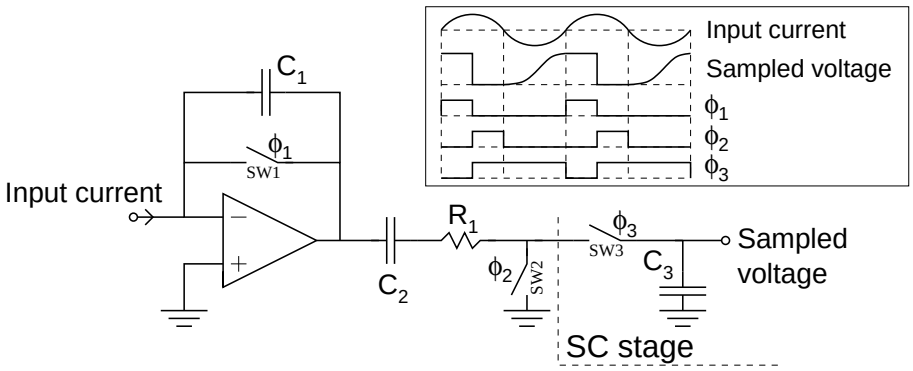

Figure 3.23: An example readout circuit which utilizes the pseudo-CT readout technique.

3.2 Closed-Loop Operation of Capacitive Sensors

The open-loop interfaces that are introduced can basically all be used to detect the capacitive signal in closed-loop sensors too. The essential difference when compared to an open-loop interface is that the closed-loop sensor applies feedback to the mechanical sensor element. In accelerometers and gyroscopes the feedback is used in order to attain control over the proof mass position within the element. The position is controlled by applying a force, in capacitive sensors an electrostatic force, to the proof mass of the element. As the feedback is in the form of a force it is often referred to as *force feedback*.

An example closed-loop sensor is depicted in Fig. 3.24, where only the feedback is added when compared to the open-loop example shown in Fig. 3.2. The gain G_{T3} of the feedback is defined by the voltage-to-force transducer and is discussed in the next section. The feedback in the example is negative, depicting the fact that the feedback aims to reduce, or nullify, the total force affecting the proof mass within the reference system. The dynamic characteristics of the system depend on H_{RES} and H_R and the three constant gains G_T, G_{T2}, and G_{T3}. The transfer function from the external signal to the sensor output can be written as

$$H_S = \frac{G_T H_R G_{T2} H_{RES}}{1 + G_{T3} H_R G_{T2} H_{RES}}, \tag{3.35}$$

which, it can be noticed, approaches (3.1) when the feedback is weak or totally removed ($G_{T3} = 0$). On the other hand, with sufficient open-loop gain, (3.35) is equal to G_T/G_{T3} and is determined purely by the gains from the acceleration to the force G_T and from the voltage to the force G_{T3}, i.e. the feedback. Now, if the sensor H_{RES} limited the bandwidth in an open loop, or if the position-to-capacitance conversion limited the linearity, the closed-loop gain could theoretically be designed to be equal to G_T/G_{T3}. The constant gain denotes the fact that the force entering the resonator is zero and therefore the open-loop limiting factors become insignificant in a closed loop. In practice, however, (3.35) is

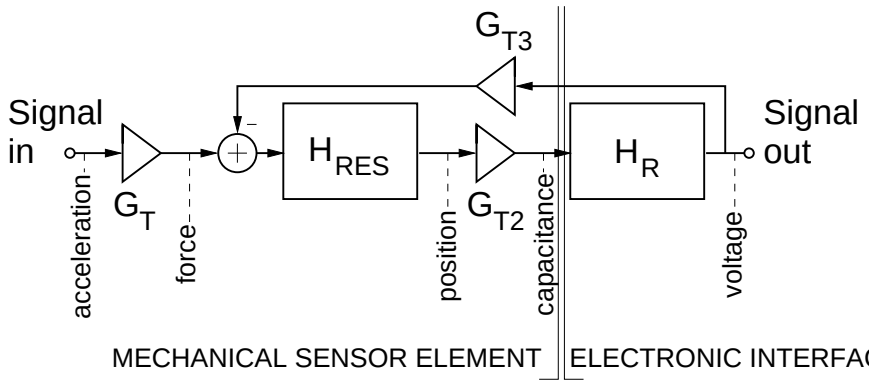

Figure 3.24: Block diagram of a closed-loop sensor, also depicting the main signal domains.

never constant over an infinite frequency band, and instead, the approximation G_T/G_{T3} can be designed to be roughly valid in the frequency band of interest, e.g. from 0 to 50 Hz.

The challenge in realizing capacitive microelectromechanical closed-loop systems is both in linearizing the feedback where the electrostatic force depends on the voltage squared (see Section 2.3 for details) and on ensuring the stability of the system, especially if the mechanical element is strongly underdamped (quality factor $\gg 0.5$). The magnitude of the force that can be applied to the element is also limited in the case of electrostatic excitation. Whether this limits the usable dynamic region of the sensor, e.g. the full-scale acceleration of a closed-loop accelerometer, depends on the mechanical design, gain G_{T3}, and the mass of the seismic element. If the nominal supply is insufficient to create a sufficient electrostatic force, the electronics need to adapt to the use of either a local or external high-voltage source.

The circuits and characteristics related to capacitive closed-loop accelerometers and gyroscopes are studied in the following sections.

3.2.1 Linearizing the Electrostatic Feedback

The problem related to electrostatic feedback relates to its inherent non-linearity. The electrostatic force, which is dependent on the voltage squared, allows only an attractive force to be generated in a single capacitor. In a differential sensor, an example of which is depicted in Fig. 3.25, the two actuation capacitors allow the feedback force to change its polarity. The actuation capacitors can also be the same ones that are used for the detection, if the readout and actuation are separated either in the frequency domain (CT interface) or time domain (DT interface).

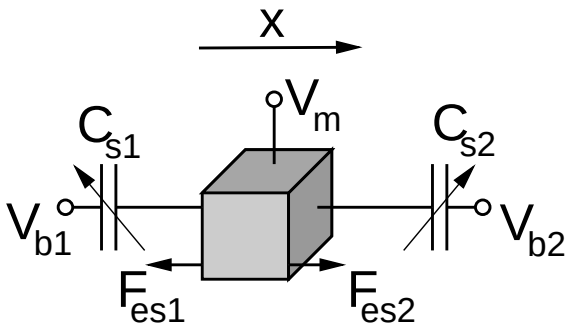

Figure 3.25: Sketch of a differential voltage-to-force transducer. Only the electrostatic forces are shown. The cube depicts the proof mass of the sensor element.

The differential configuration also allows the force feedback to be linearized. The feedback force affecting the proof mass in Fig. 3.25 can be written as

$$F_{es} = F_{es2} - F_{es1}. \tag{3.36}$$

When the sensor element is placed within a closed loop, the electrostatic feedback can be designed to minimize the motion of the proof mass. If plate capacitors (2.24) are used in the sensor that operates in a closed loop, and the area A and the spacing between the plates x_0 are equal for the two capacitors, the force can be rewritten as

$$F_{es} = \frac{e_0 A}{2x_0^2}[(V_{b2} - V_m)^2 - (V_m - V_{b1})^2] = \frac{e_0 A}{2x_0^2}[(V_{b2}^2 - V_{b1}^2) + 2V_m(V_{b1} - V_{b2})]. \tag{3.37}$$

Now the proper closed-loop functionality allows to keep the spacing between the capacitor plates constant ($x \approx 0$) even in the presence of, for example, external acceleration. When also the bias voltages fulfill the condition $V_{b2} = -V_{b1} = V_b$, and the V_m is controlled by the feedback of the system, the electrostatic force becomes a linear function of V_m,

$$\frac{F_{es}}{V_m} = G_{T3} = \frac{e_0 A}{x_0^2} 2V_b, \tag{3.38}$$

where G_{T3} can be found in Fig. 3.24. If only a single capacitor C_{s1} were available, the second-order terms in (3.37) could not be canceled and the gain G_{T3} would be half that of a differential sensor.

Similarly, if comb actuators, (2.29), are used for the interface, and the height h of the fingers and the spacing between them, x_0, are equal for the two capacitors, the force can be rewritten as

$$F_{es} = \frac{e_0 h}{2x_0}[(V_{b2}^2 - V_{b1}^2) + 2V_m(V_{b1} - V_{b2})]. \tag{3.39}$$

When $V_{b2} = -V_{b1} = V_b$,

$$\frac{F_{es}}{V_m} = G_{T3} = \frac{e_0 h}{x_0} 2V_b. \tag{3.40}$$

It should again be noticed that no small signal approximation of x was made.

In practice perfect matching between the two capacitors is not possible and mismatch will cause the second-order non-linearity to become visible. However, the voltage-to-force transducers can be balanced in a fairly simple manner, as explained in [I] and measured in [II], which allows a system linearity much better than 60 dB to be achieved. On the other hand detecting the point of optimal linearity is challenging without actually measuring the linearity.

Another, more popular means to linearize the force feedback is to apply *pulse-width modulation* (PWM) or *pulse-density modulation* (PDM); both methods are well applicable for digital feedback [89]. The difference between the two modulation techniques is depicted

in Fig. 3.26, where six samples of a single-bit PWM and PDM feedback are shown. The electrostatic force in the figure can be compared to Fig. 3.25, and attained, for example, by setting $V_m = 0$ and allowing V_{b2} to be active when $B = 1$, and V_{b1} to be active when $B = 0$. It should also be assumed that $V_{b1} = V_{b2} \neq 0$ in the active state and that $V_{b1} = V_{b2} = 0$ otherwise. When the pulse rate is much faster than the bandwidth of the mechanical element, the electrostatic force will be averaged. If B_{ave} corresponds to the fraction of the time F_{es2} is active, then the fraction of time F_{es1} is active is equal to $1 - B_{ave}$. The corresponding average force

$$F_{es} = F_{es2}B_{ave} - F_{es1}(1 - B_{ave}) = -F_{es1} + (F_{es2} + F_{es1})B_{ave} \tag{3.41}$$

is linearly dependent on B_{ave}. In order for the linear relationship between B_{ave} and F_{es} to hold, the pulses are assumed to have zero rise and fall times. Fig. 3.27 illustrates an example of a PWM feedback, where the feedback pulses pass a first-order linear low-pass filter (LPF) with the time constant τ_p before arriving at the voltage-to-force transducer. The average force, calculated for the nominal duration of the input pulse, shows a clear dependency on the pulse width. If the rise and fall times were considerably shorter than the shortest pulse applied, the average force would become independent of the pulse width. This can also be observed in the figure – the longer the pulse is compared to τ_p, the lower the sensitivity of the average force to the pulse length. In practice it is difficult to realize a sufficiently short rise time, which imposes stringent slew rate requirements on the source that creates the bias voltages. A more viable approach is offered by a return-to-zero (RTZ) PDM, similar to the 1-bit PDM in Fig. 3.26, where each feedback sample

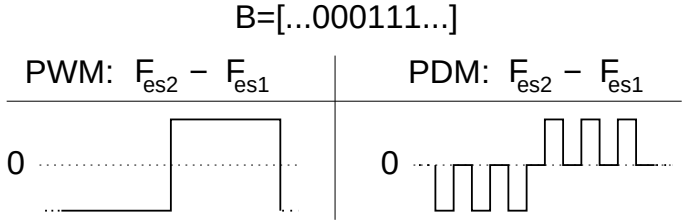

Figure 3.26: An example to depict the difference between PWM and PDM (RTZ).

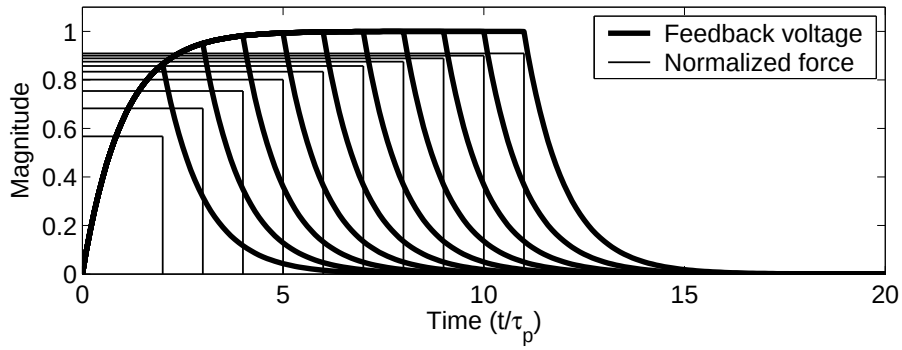

Figure 3.27: Effect of finite rise and fall times on the average feedback force. If $\tau_p = 0$ the normalized feedback force is always unity and independent of the pulse width.

creates a pulse. Rise and fall times, appearing similarly on each pulse, will just affect the gain from the average feedback voltage to force, and not the linearity.

It should be taken into account that if signal-dependent or, in fact, any non-zero position x exists in the parallel plate actuator in a closed loop, it will introduce non-linearity within the sensor, regardless of the method used to apply the feedback. The minimization of x can be accomplished by realizing efficient feedback, i.e. by increasing the loop gain of the closed-loop system. The design of the feedback can also be modified in such a way that the force is nearly independent of x, as described in [90].

3.2.2 Parasitic Resonance Modes of the Sensor Element

The reduction of noise in accelerometers and gyroscopes requires not just the maximization of the proof mass, but also the reduction of the mechanical damping within the element. Hence the very low noise performance makes it necessary to operate the sensor elements in a vacuum. Although the beneficial effect of lower noise can be reached by a considerable reduction in damping, it also results in a high Q-value of the element, which inflicts ringing and consequently a long settling time of the sensor. In order to reduce the Q-value and to damp the element operating in a vacuum, a proper closed-loop control can be built.

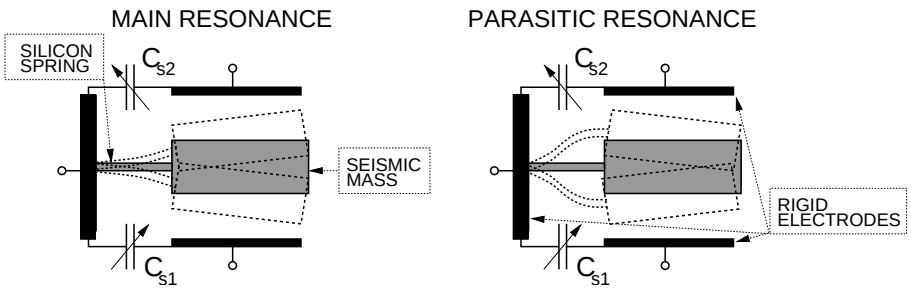

Figure 3.28: Sketch of two resonance modes of the same sensor element.

In a practical resonator the number of resonance modes is never limited to unity [23, 91]. When the sensor is operated in a vacuum all the modes will exhibit an increased Q-value. Two resonance modes of the same silicon resonator are sketched in Fig. 3.28. When considering the capacitive signal, which is detected using the plate capacitors, both resonance modes contribute to the response from the excitation force to the capacitive signal.

The detection and actuation can be done using the same capacitive interface or separate ones; the former method can be referred as a *collocated* control and the latter to as a *non-collocated* control [92]. One motivation for using dedicated actuation capacitors is

that the feedback and readout can be electrically isolated from each other, whereas when common electrodes and a common signal path are used, the isolation takes place either in the time domain or in the frequency domain. It is, however, important to notice that the additional electrodes do not guarantee perfect isolation between the actuation and the readout. Finite impedance of the proof mass can cause the potential of the proof mass to vary in the event of rapid voltage transitions that result from, for example, square wave actuation. Variation of the proof mass potential will couple to the detection capacitors. Another unwanted signal path can exist because of parasitic capacitances, which can couple the signal between actuation and detection.

When non-collocated control is utilized, the mechanical system between the actuation and detection will introduce an additional phase lag of up to -180° compared to collocated control. An example of such an open-loop system is shown in Fig. 3.29. In the closed-loop gyroscope in [91] the difference between the two detection methods is analyzed. If the proof mass in the sense resonator in [91] is directly actuated but the sensing is done using separate sensing capacitors, which will realize an additional parasitic resonance, the resulting system would correspond to Fig. 3.29.

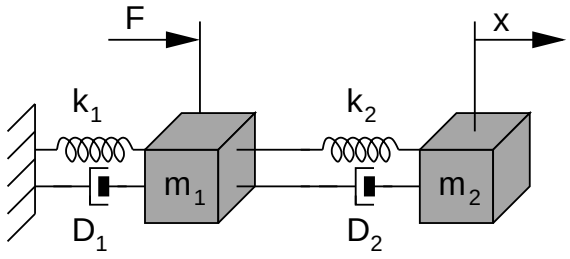

Figure 3.29: Example of an open-loop system (x/F) resulting in non-collocated control in a closed loop. (The collocated system would require the position information to be extracted from the first resonator.)

Additional phase shift can also result from a sensor element where the feedback is capable of exciting two independent resonances, which both contribute to the signal capacitance. In a non-collocated system it is possible that the sign of the gain of the resonances is different. The effect of sign change can be seen in the Bode diagram of a simple CT example system shown in Fig. 3.30. In the system two resonators, fundamental at 1 $\mathrm{rad/s}$ and parasitic at 20 $\mathrm{rad/s}$, a parasitic pole at 1000 $\mathrm{rad/s}$, and a lead compensator, form the loop transfer function

$$H_{loop}(s) = \left[\frac{1}{s^2 + \frac{2s}{10^3} + 1} + \frac{g_{par}}{s^2 + \frac{40s}{10^3} + 20^2}\right] \frac{1}{\frac{s}{10^3} + 1} \frac{10s + 20}{\frac{s}{10} + 1}. \tag{3.42}$$

The Bode diagram is plotted for three values of g_{par}, which defines the gain of the parasitic resonance. The negative sign of g_{par} in this case incidates the use of non-collocated control, which has led to an additional phase shift of -180° and a negative phase margin.

The corresponding closed-loop step responses are shown in Fig. 3.31. The negative phase margin causes growing oscillations approximately at the frequency of the parasitic mode. The only way to stabilize the system in the presence of phase uncertainty up to 360° is to ensure that the loop gain remains below unity at frequencies where parasitic resonances exist [92].

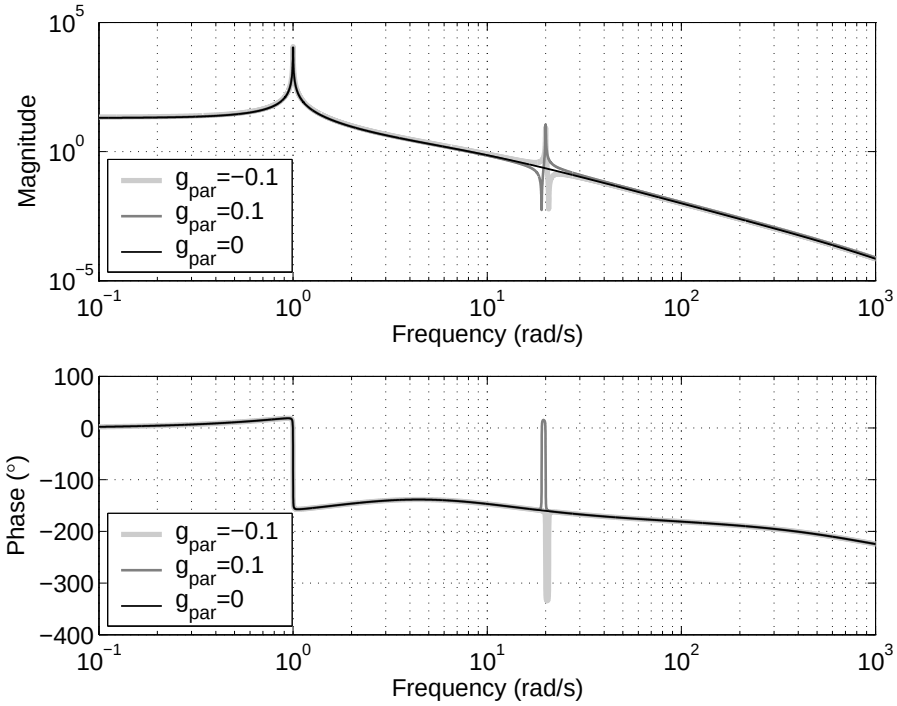

Figure 3.30: Bode diagram for the loop response of the example system, including the lower frequency resonance only, two modes with $g_{par} = 0.1$, and two modes with $g_{par} = -0.1$.

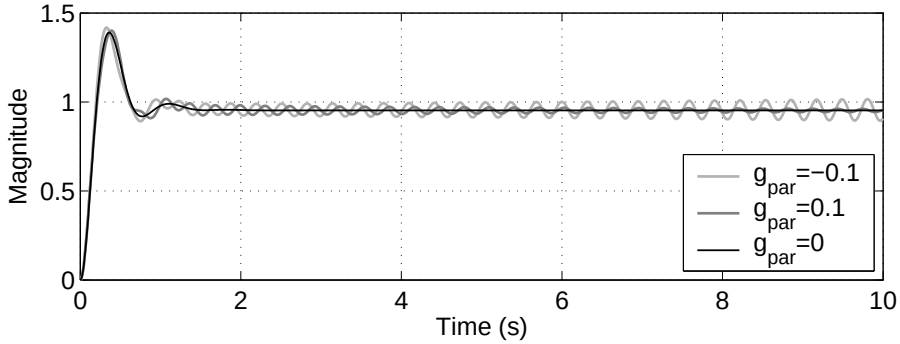

Figure 3.31: Step response of the example system (feedback factor unity), including the lower frequency resonance only, two modes with $g_{par} = 0.1$, and two modes with $g_{par} = -0.1$.

Even if collocated control were utilized, always ensuring a pair of imaginary left-half-plane zeroes between the resonance peaks to compensate for the phase lag caused by the parasitic resonance, the modes are still very challenging to control in closed-loop systems. In CT loops the separation of the readout and feedback in the frequency domain obliges filtering to be used. The filtering causes delay in the loop before the gain decreases, which exposes the loop to the parasitic resonances [I, II]. Similarly, in a DT loop separating the feedback and readout in time always inflicts some delay. The phase in the loop will start to turn negative as a result of the delay when the sampling frequency is approached. In DT systems the folding, which will bring high-frequency resonances into the Nyquist band, must also be taken into account [93]. One approach used to alleviate the problem, introduced for a closed-loop gyroscope in [23, 93], is to use positive feedback to permit a sufficient phase margin at the parasitic resonances. In vibratory gyroscopes, where the loop dc gain can be set to be zero, positive feedback can be used to realize a stable system.

3.2.3 Electromechanical $\Delta\Sigma$ Interfaces

The use of a $\Sigma\Delta$ ADC for the open-loop detection of capacitance was reviewed in Section 3.1.8, but with some small changes a $\Sigma\Delta$ loop can be applied to build a closed-loop sensor interface. The conversion from a purely electrical $\Sigma\Delta$ loop into an *eletromechanical* (EM) $\Sigma\Delta$ loop, or EM-$\Delta\Sigma$ modulator as it is often called, can be done by replacing two integrators in the loop with the sensor element. This results in a closed-loop system, where the feedback to the element is an electrostatic force attempting to minimize the total force entering the sensor. Ideally, the average value of the PDM feedback, which is typically also the output of the loop, is a linear function of the external force affecting the sensor. In its simpliest form the EM-$\Delta\Sigma$ loop is a second-order system, a linear model of which is shown in Fig. 3.32. The model comprises the sensor (TF $H_{RES}(s)$), a constant gain from the position to the voltage G_R, an electrical lead filter to compensate for delay in the loop (TF $H_{LF}(z)$), and a quantizer with equivalent gain G_q. The feedback is realized by the voltage-to-force transducer (gain G_{T3}).

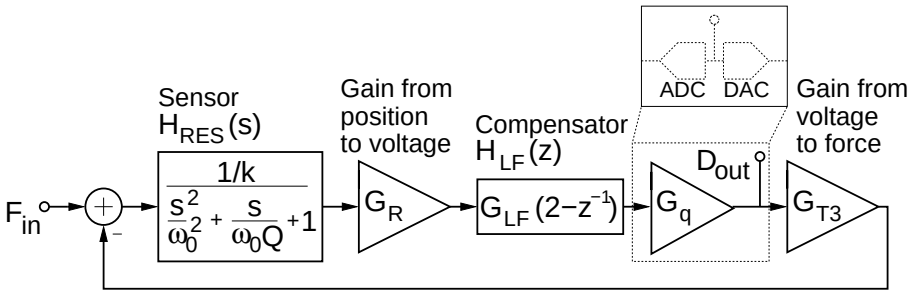

Figure 3.32: A block diagram of a second-order electromechanical $\Delta\Sigma$ modulator, including the linear models of the subblocks.

A loop filter which allows a positive phase shift, such as a lead filter, is necessary in order to attain a positive phase margin in the loop. It is also possible to use a strongly overdamped element as in [94] to make the resonator appear as a single-pole device. However, the heavy damping compromises the noise performance of the element. The lead filter-based approach to the second-order EM-$\Delta\Sigma$-loop was first utilized in [95] to realize a low-noise accelerometer. The sensor element used in the design is a high-Q bulk micromachined element, and the system is reported to achieve a noise floor of 10 $\mu\mathrm{g}/\sqrt{\mathrm{Hz}}$.

A number of second-order EM-$\Delta\Sigma$ sensors, accelerometers, such as [59, 96, 97], and gyroscopes, such as [91, 98, 99], have been published since the first one in [95]. For example, in [59] an overdamped surface-micromachined element is used to implement a three-axis closed-loop accelerometer. The element and the differential SC interface implementing the input common-mode feedback (see Section 3.1.3) and CDS are analyzed for the noise performance and offset. At a sufficiently high sampling frequency, 0.3 MHz, the noise is dominated by the element and a noise floor of roughly 100-1000 $\mu\mathrm{g}/\sqrt{\mathrm{Hz}}$, depending on the axis, is reached.

The sampling frequency in a second-order EM-$\Delta\Sigma$ loop inevitably becomes moderately high, even higher than in [59], as the analysis in [100] indicates. This is because the mechanical element does not provide filtering as efficient as that provided by the integrators in a purely electrical $\Delta\Sigma$-loop, and the most straightforward way to reduce the quantization noise is by increasing the sampling frequency. Similarly the effect of the non-zero periodic motion of the sensor element, *residual motion*, present with a dc input signal especially in a second-order EM-$\Delta\Sigma$ modulator, can be reduced by increasing the sampling frequency [100].

A factor which significantly affects the quantization noise properties, is that the second-order EM-$\Delta\Sigma$ loop provides no filtering for the noise of the front-end electronic interface [100]. In fact the lead filter even amplifies the noise to the quantizer input. The noise inflicted by the electronics causes the effective quantizer gain to decrease and the quantization noise to increase at the modulator output [101]. The phenomenon can be seen in Fig. 3.33 for the 0.1FS (full-scale) input signal F_{in} for the modulator in Fig. 3.32. The loop gain is plotted in Fig. 3.34. The other curve in Fig. 3.33 is attained as a strong 0.5FS sine at a normalized frequency of 0.16 is fed to the input of the electronic interface in order to demonstrate how a strong high-frequency disturbance, e.g., noise, affects the operation of the modulator. The quantization noise can be clearly seen to increase as a result of the reduced quantizer gain. More details of the simulation can be found in Appendix A.

More efficient quantization noise shaping and less interaction between the electronic noise and quantization noise can be attained by increasing the order of the EM-$\Delta\Sigma$ modulator. This has clearly been the latest direction of research and higher-order inter-

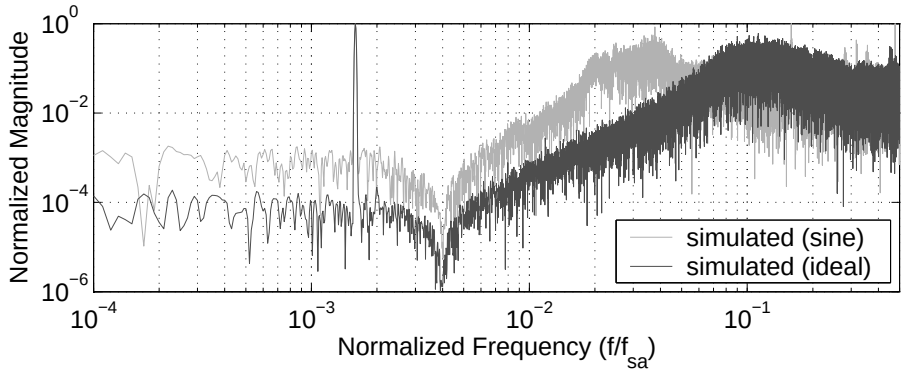

Figure 3.33: Two simulated output spectra of a second-order EM-$\Delta\Sigma$ loop with a single-bit quantizer referred to the maximum value of the output signal. The frequency is referred to the sample rate. The effect of out-of-band disturbance is studied by adding a 0.5FS sine at a frequency 0.16 to the input of the electronic interface.

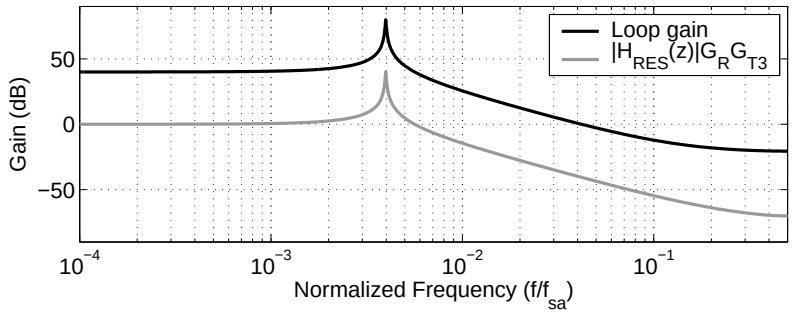

Figure 3.34: The loop gain with $G_q = 1$ and $G_{LF} = 100$ for Fig. 3.33, and the gain from the feedback voltage to the voltage-mode output of the sensor.

faces have been introduced for gyroscopes [23, 46, 102, 103, 104] and for accelerometers [89, 104, 105, 44]. The accelerometers are, without exception, low-pass-type modulators where the filtering in the electronic interface is typically achieved by adding two or more integrators. In gyroscopes, where the signal band is modulated off the dc, electrical resonators can be used to form the additional noise shaping so that the sampling frequency does not have to be increased excessively. The accelerometer in [44] cannot be considered a typical higher-order $\Delta\Sigma$ loop as here an electrical second-order $\Delta\Sigma$ ADC is used to convert the capacitance to digital word and a complex compensator is implemented in the digital part of the interface to realize the feedback and the final output. As all the cited higher-order $\Delta\Sigma$ interfaces are SC circuits, they are prone to the folding of noise. In [46] the noise is reduced by using a CT front-end for detecting the capacitive signal, whereas in [23] a *boxcar* integrator is utilized for the front-end in order to efficiently reduce the noise bandwidth before sampling.

An example fourth-order LP EM-$\Delta\Sigma$ modulator is shown in Fig. 3.35. The original circuit including an additional local feedback for the realization of a resonator, is presented

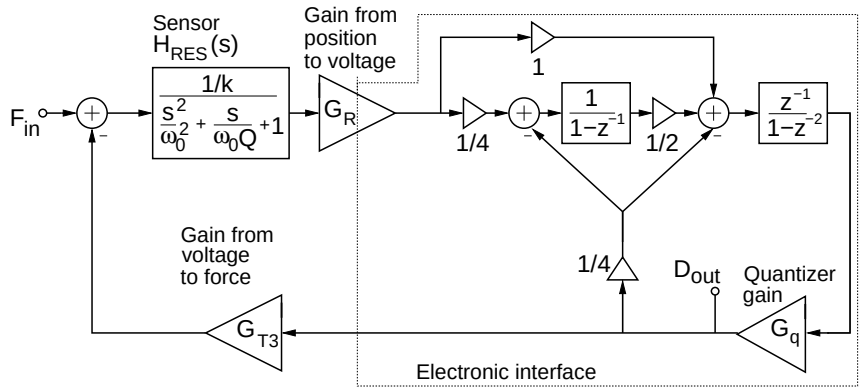

Figure 3.35: A block diagram of a fourth-order electromechanical $\Delta\Sigma$ modulator, including the linear models of the subblocks.

in [46]. The figure can be compared to an electrical modulator, where only feedback paths are utilized. In the example, the feedback that is missing as a result of the mechanical element is replaced by a local feedforward path. The feedforward is added as the internal properties (velocity) of the mechanical sensor cannot be accessed. This modification allows the EM-$\Delta\Sigma$ modulator to be designed without limiting the properties of the loop filter in comparison with an electrical modulator. The technique is presented in [106] and is referred to as *unconstrained sigma-delta force feedback*.

The block diagram in Fig. 3.35 is simulated (see Appendix A for the Simulink model) using the same sensor, sample rate and input signals as for the previous example concerning the second-order EM-$\Delta\Sigma$ loop. When comparing the spectrum in Fig. 3.33 for a second-order loop with the one in Fig. 3.36 for a fourth-order loop, the quantization noise shaping is considerably improved in the higher-order modulator. It is important to take

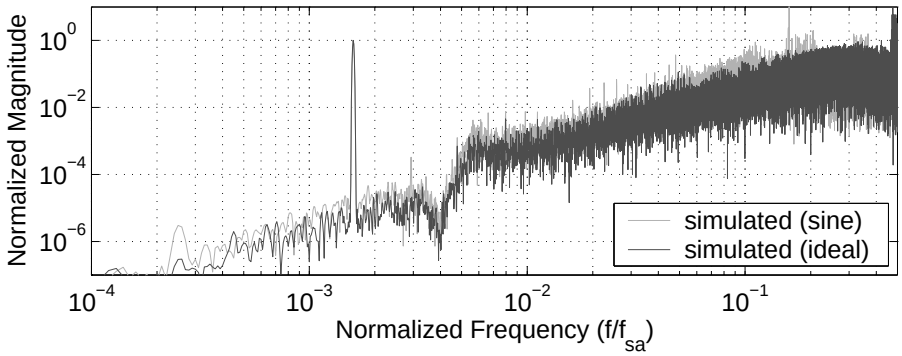

Figure 3.36: Two simulated output spectra of a fourth-order EM-$\Delta\Sigma$ loop with a single-bit quantizer referred to the maximum value of the output signal. The frequency is referred to the sample rate. The effect of out-of-band disturbance is studied by adding a 0.5FS sine at a frequency 0.16 to the input of the electronic interface. The gain TF of the sensor is the same as that shown in Fig. 3.34.

note that the example simulations are run for a linear model of the sensor. For a proper system design the non-linearity of the electrostatic feedback and parasitic modes should be included in the simulations (see Sections 3.2.1 and 3.2.2) and the stability should be confirmed in the presence of process and parameter variations.

3.2.4 Closed-Loop Analog Interfaces

Although EM-$\Delta\Sigma$ modulators with digital feedback have been proven to achieve good performance and inherent digitization of the signal, the analog closed loop can still show potential, for example, when folding prevents a sufficient performance of the sensor from being attained. A typical design of a CT analog closed-loop accelerometer is shown in Fig. 3.37, where a single pair of capacitors is shared between the readout and feedback. Unlike in a discrete-time system, where a single clock period can be split into separate readout and clock phases, in a CT system the separation must be done in the frequency domain. The approach is also depicted in the example interface; the ac detection voltage generates a signal proportional to the mismatch between the capacitors, whereas the dc bias defined by V_{b1} and V_{b2} is required to generate a linear electrostatic force. The feedback is generated by amplifying the detected signal, downconverting and filtering it, and finally by using a controller to define the dynamics of the loop. The two frequency regions, readout and feedback, are ideally perfectly isolated from each other. The essential component allowing proper isolation is the mixer, but the filters, especially the LPF, also play an important role in separating the frequency bands. Imperfect isolation between the frequency band compromises the stability of the loop and is discussed in detail in [I].

The feedback signal can be brought to the element through, for example, the biasing resistor as in Fig. 3.37 if a voltage buffer is used for the signal detection [55, 56, 107], or through the virtual ground if a TIA is utilized for detection [I, II]. In both cases the front-end must tolerate the full-scale voltage range of the feedback. The linear model for the system shown in Fig. 3.37 is easy to construct. The whole readout can be modeled as a constant gain G_R, providing that the delay in this part of the interface is insignificant. Similarly, the conversion gain of the demodulator (mixer) G_{demod} is constant and at its maximum when the two signals being mixed are in phase. After the signal is demodulated, the frequency behavior of all the following blocks, such as the LPF $H_{lpf}(s)$ and the controller $H_{ctrl}(s)$, is straightforward to include into the linear model of the loop. The output of the system is taken at the controller output and hence the feedback factor is determined by the voltage-to-force transducer G_{T3} and the parasitic poles, which in this case are formed by the bias resistors R_{bias} and the sensor. With a loop gain much larger than unity, and $H_{par}(s)$ equal to unity in the frequency band of interest, the closed-loop gain V_{out}/F_{in} is defined as $1/G_{T3}$, the inverse of (3.38). The loop gain is clearly inversely proportional to the bias voltage V_b. It is interesting to notice that when the signal is digitized using V_b as a reference for the ADC, the ADC, where the digital output is typically inversely proportional to the reference, increases the bias sensitivity of gain in the com-

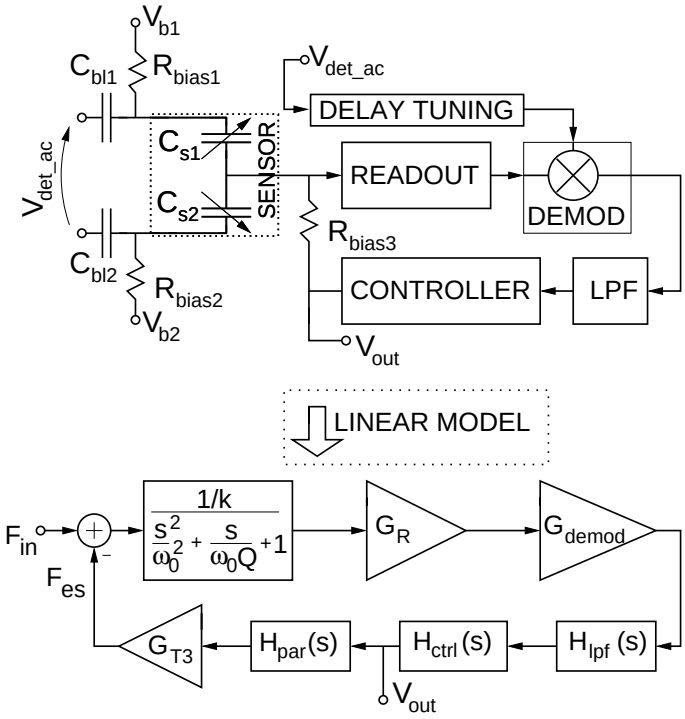

Figure 3.37: An example block diagram of a continuous-time analog closed-loop interface typically used for accelerometers. The linear model of the loop is also shown.

plete sensor to $1/V_b^2$. The bias sensitivity of gain is similar in the closed-loop EM-$\Delta\Sigma$ modulators. When compared with the open-loop readout techniques, where the effect of absolute V_b can be completely eliminated, as in (3.34) [15], the closed-loop sensor imposes considerably more stringent requirements on the stability of the bias voltage V_b. A detailed analysis of a very high-accuracy closed-loop CT accelerometer is given in [I] and the design is upgraded in [II]. The ADC and the controller in [II] are presented in [III] and [IV], respectively.

As extremely low noise levels also require an element with low thermal noise and typically a consequent high quality factor, the high-Q parasitic modes must also be considered. The direct consequence of filtering, which enables the readout and feedback to be separated, is that the LPF and any parasitic poles ($H_{par}(s)$) in the loop inflict a negative phase shift. At sufficiently high frequencies the total phase in the loop turns negative and exposes the loop to instability as a result of high-Q parasitic modes that potentially exist. The phase can be compared to delay in a DT loop with the help of a simple example. Assuming that a CT loop utilizes a detection frequency of 1 MHz, the LPF is designed to have a corner frequency of 100 kHz, which allows sufficient attenuation at and above the carrier. The negative phase shift resulting from the LPF is 10° at 10 kHz. When the phase shift is converted to an equivalent delay in a DT system with a sample rate equal to 1 MHz, the delay is roughly equal to 3 clock periods. As a DT loop can easily be designed to inflict a delay of less than a single clock period, the negative phase shift in a CT loop

can become more significant when compared with a DT loop. The region where instability resulting from the high-Q parasitic modes can occur is moderately easy to identify (see Fig. 13 in [I]), and should be taken into account in the design of both the element and the interface.

Isolation between the readout and actuation can also be attained if a second pair of signal capacitors is available. This approach is shown in Fig. 3.38, where a dc detection voltage and a TRA are combined to implement a very simple closed-loop system. The absence of a dc signal current will prohibit any control of the dc position in the sensor, but the interface could be applied, for example, in a gyroscope, where the signal is close to or at the resonance frequency. The capacitors drawn using dashed lines simply depict the small capacitors that can be included to stabilize the TRA.

The analog closed loop can also be realized in discrete-time form [84, 108], which allows a simpler time-domain separation of the feedback and readout. An example of a DT

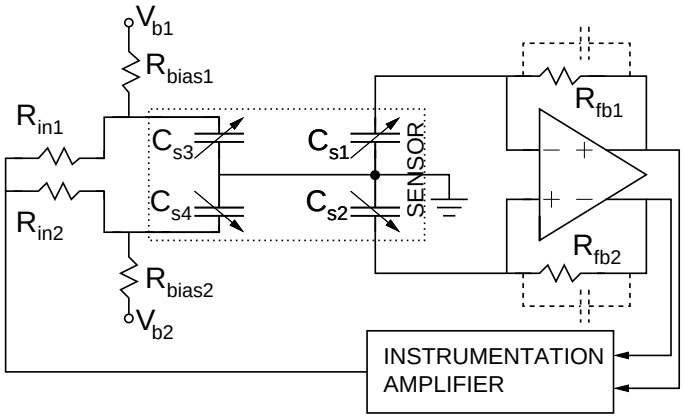

Figure 3.38: A simple continuous-time analog-closed loop interface where the front-end TRA also implements the controller in the loop. The second pair of sensor capacitors subtitutes for the frequency division that is otherwise necessary.

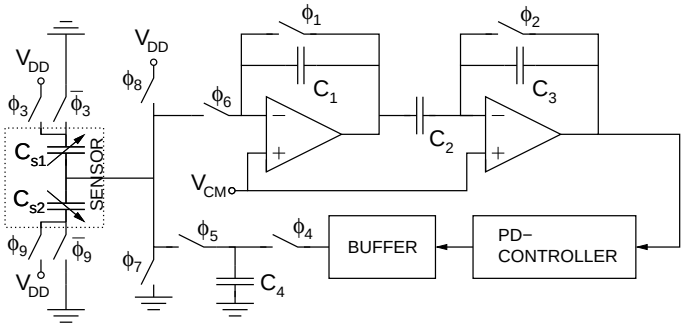

Figure 3.39: A block diagram of a discrete-time analog closed-loop accelerometer in [84].

analog interface is shown in Fig. 3.39 [84]. Here the two SC gain stages allow the implementation of CDS, whereas the SC proportional-derivative (PD) controller realizes the sufficient dc gain and damping of the high-Q resonances of the element. The capacitor C_4 allows the minimization of the settling time of the feedback voltage in order to minimize the non-linearity resulting from the electrostatic forces (see Section 3.2.1). Detailed clock phases can be found in [84].

3.2.5 Capacitive Gyroscope: Drive Loop

In a typical MEMS gyroscope the angular velocity signal that is sensed originates from the Coriolis acceleration. The Coriolis acceleration $\overline{a_{cor}}$, on the other hand, is directly proportional not just to the angular rate $\overline{\Omega}$, but also to the velocity $\partial\overline{r_{mr}}/\partial t$ of the drive resonator (see Section 2)

$$\overline{a_{cor}} = 2\overline{\Omega} \times \frac{\partial\overline{r_{mr}}}{\partial t}. \tag{3.43}$$

Hence, providing a maximum and constant velocity oscillation is essential in a MEMS gyroscope. In capacitive gyroscopes the magnitude of the electrostatic force is fairly limited and it can best be taken advantange of by exciting the high-Q drive resonator at its resonance frequency.

The magnitude of the electrostatic force, in e.g. a parallel plate or comb drive, depends on the squared excitation voltage. Hence, if the excitation voltage contains both a dc component V_{dc} and an ac component $V_{ac}\sin(\omega t)$ at the frequency ω, the force

$$\begin{aligned} F_{es} &= K_{F/V^2}[V_{dc} + V_{ac}\sin(\omega t)]^2 \\ &= K_{F/V^2}[(V_{dc}^2 + \frac{V_{ac}^2}{2} + 2V_{dc}V_{ac}\sin(\omega t) + \frac{V_{ac}^2}{2}\cos(2\omega t)]. \end{aligned} \tag{3.44}$$

can be seen as having an effect at dc, ω, and 2ω. The coefficient K_{F/V^2} can be found by comparing (3.44) with (2.24) and (2.29), where $V = V_{dc} + V_{ac}\sin(\omega t)$, for plate and comb capacitors, respectively. The proof mass motion within the resonator can be significant, which can affect the magnitude of the excitation force, especially in parallel plate actuators.

Generating the excitation force by operating the resonator in a closed loop with positive feedback is straightforward. The linear force term at ω allows the resonator to be excited at the same frequency as the one at which the position signal is detected. The force that has an effect at 2ω enables the resonance frequency force to be generated using an ac voltage at half the resonance frequency with no dc component. Though the magnitude of the excitation force is lower in comparison to the linear force, the sensor element is theoretically free of a strong voltage component at the resonance frequency, thus reducing problematic cross-coupling. It should be noticed that if the electrostatic actuator is

differential, the squared voltage terms in (3.44) will disappear and excitation at half the resonance is not possible. This feature was taken advantage of for linearizing the force feedback in (3.37).

The electronic interface for the drive resonator must compensate for the 90° phase lag caused by the drive resonator at the resonance frequency in order to create an oscillator. Hence, an ideal phase shift in the loop at the resonance frequency is either 90° or -90°, depending on the sign of the feedback, when the linear force component is utilized for the excitation. For a half-frequency excitation no phase shift is required in the loop, but it should be noticed that a square wave drive cannot be utilized. This is due to the fact that the electrostatic force in this case is, in practice, constant and no energy can be transmitted to the resonator.

As [VII] provides a thorough introduction and analysis of the implementation of an analog drive loop, an example implementation of the digital drive loop is taken from [46] and shown in Fig. 3.40. Here the transfer function $G_{T3}H_{RES}(s)G_R$ models the linear response from the electrostatic force to the voltage-mode position of the sensor element. The readout voltage is converted into the digital domain using a $\Delta\Sigma$ ADC and the rest of the system is implemented as digital. Now the digital phase-locked-loop (DPLL) is locked at the resonance frequency. The DPLL creates a signal that is 90° phase-shifted compared to the input of the DPLL. This signal is set to drive the resonator after the level control in a variable gain amplifier (VGA) and the digital-analog conversion in a $\Delta\Sigma$ DAC. In order to control the level of oscillation of the drive resonator, the amplitude of the oscillation is extracted in the mixer and fed to a controller, which then sets the gain of the VGA. The $\Delta\Sigma$ DAC shapes the quantization noise of the two-level electrostatic feedback away from the resonance frequency. The use of the $\Delta\Sigma$ DAC allows the digital interface to be realized without the need for a multibit DAC for the feedback.

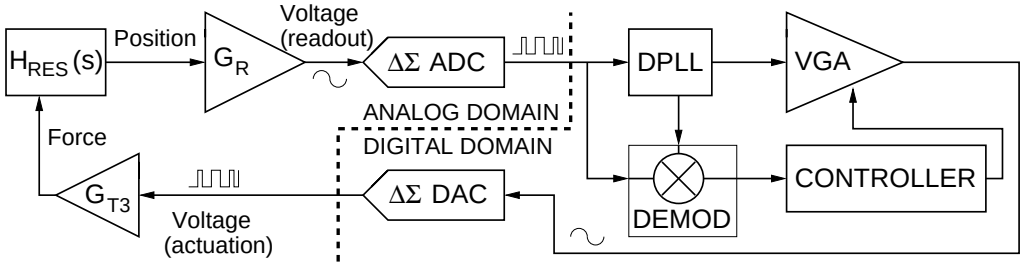

Figure 3.40: A block diagram of the drive loop in [46].

Although the example is implemented mainly digitally, it gives a good description of the typical main features of the drive loop. The PLL is commonly used to create a feedback signal in the correct phase, but it can also provide precise clock signals for other blocks of the interface for the gyroscope. The controller is necessary for precise regulation over the oscillation amplitude (velocity) of the resonator, and the VGA provides the means

to change the gain in the loop. Other example implementations of the drive loop can be found in, for example, [47], where a TRA is used to detect the capacitance and to create the proper phase shift in the loop, and in [58], where an analog interface including a PLL is utilized.

As in all closed-loop interfaces where a high-Q mechanical resonator in included in the loop, the behavior of the parasitic resonance modes must be taken into account also in the drive loop. The probability of oscillation at any parasitic mode can be reduced, for example by ensuring that the gain of the interface is at its highest at the fundamental and lowest resonance mode, as in [VII], where an integrator is used as the phase-shifting element. It is, however, imperative to confirm that the cross-coupling between the excitation and readout is small enough not to cause the electronic interface to oscillate.

3.3 Discussion

The purpose of a readout circuit of a capacitive sensor is to extract the absolute or relative value of the signal capacitance. The detection process is never ideal and is typically corrupted by noise, distortion, and spurious tones. CT techniques can be used efficiently to realize a low-noise readout with a typically somewhat more complex readout circuit when compared with the simplest types of SC, or in general DT circuits. SC circuits provide a simple way to convert the capacitive information into voltage, allow the use of noise reduction techniques such as chopper stabilization and CDS, and offer the possibility of relieving the non-linearity resulting from electrostatic forces. However, it is imperative to take the effect of folding in DT circuits into account during the design, especially if it is known in advance that, for example, the supply is likely to contain significant disturbances.

It is common that the final output of the sensor is digital, in which case it is also inevitable that the signal is converted to the DT domain, i.e., sampled, usually before the quantizer. SC circuits allow the quantization to be performed very close to the sensor element using $\Delta\Sigma$ modulation [85], making possible a small supply current and low complexity [15]. On the other hand, in gyroscopes, where the capacitive signal is very small, low-noise CT circuits have been used [46, 58] to amplify the signal before transforming it to the DT domain, and further, to the digital domain. Similarly, in [II] the ultra-low-noise accelerometer has an analog closed-loop core and a separate ADC.

As a part of the research work the pseudo-CT open-loop readout technique is presented in [V,VI] and applied to create a two-axis gyroscope with analog outputs and minimized chip area. Unlike in a typical example, where the front-end is the dominant noise source of a sensor, in this gyroscope the on-chip generation of references and detection voltages

Table 3.1: Summary of the properties of the gyroscope in [VI].

Process technology	0.35 μm HV CMOS
Chip area (mm^2)	7.9 (active area 2.5)
Supply voltage (V)/current (mA)	2.5-3.6/1.8
Detection voltage, dc (V)	9.1
Equivalent noise capacitance for x/y ($\mathrm{aF}/\sqrt{\mathrm{Hz}}$)	0.19/0.51
Full-scale signal ($^\circ/\mathrm{s}$)	$\pm$300
Signal bandwidth max. (Hz)	300
Spot noise for x/y ($^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$)	0.015/0.041
Gain shift from -10 to 90 $^\circ\mathrm{C}$ for x/y (%)	1/7
Max. dc non-linearity for x/y (% of full-scale)	0.1/1.5
Bias stability for x/y ($^\circ/\mathrm{hr}$)	25/33
ZRO shift from -10 to 90 $^\circ\mathrm{C}$ ($^\circ/\mathrm{s}$)	50/6

in the presence of sensor element non-idealities, especially as external filtering is not an option, has inevitably also evoked other noise sources than the front-end. A summary of the properties of the sensor is shown in Table 3.1. The noise levels of the two channels differ significantly. This is mainly due to the absence of mechanical quadrature compensation, which is replaced by the very compact purely electrical quadrature cancellation. The cancellation method, however, adds to the noise in the y-channel, where the quadrature signal is high. Considerable cross-coupling between readout and actuation, and the noise of the structural wafer (proof mass) bias, which exists as no external filtering capacitors are added, are the reasons why the overall noise levels are higher than those caused by the readout circuits only. In fact, in [V] only the references and supply bypass capacitance are external to the ASIC, which is made possible by the careful design of the interface. With smaller cross-coupling caused by the less-than-optimal bonding of the sensor element and a smaller quadrature signal in the y-channel, the ZRO stability in the x-channel and the linearity and noise performance in the y-channel would improve. The circuits and theory presented in [VII-IX] cover high-voltage, drive-loop, and clock generation circuitry, which all have a significant effect on the performance, supply current, and chip area of the complete sensor.

In capacitive closed-loop sensors an electrostatic force feedback is added in order to balance the forces affecting the proof mass of the sensor element. Thus, in a closed-loop sensor the feedback voltage, which is usually the output of the sensor, represents the external force. In this way a closed-loop sensor is linear, provided that the ratio of the feedback voltage and the feedback force is constant and the loop gain in the signal band is sufficient. Similarly, the full-scale range and the dynamic behavior become determined by the range of the feedback force and the parameters of the complete loop, respectively. Another significant benefit is that low damping can be used to reduce the noise of the element, while the feedback is used to flatten the gain peak resulting from the high Q sensor element. However, compared with an open-loop sensor, the closed-loop operation in-

Table 3.2: Summary of the properties of the accelerometer in [II].

Process technology	0.7 μm HV CMOS
Chip area (mm^2)	22
Supply current (mA)	15 (5 V) and 0.9 (12 V)
Bandwidth (Hz)	300
SNR, analog/digital output (dB)	111/105 (@ full-scale dc of 1.5 g)
Maximum dc non-linearity ($\%$)	0.014
Detection frequency (MHz)	3
Detection amplitude, single-ended (V)	1
Input referred noise in open-loop from the CSA input (detection voltage) to the LPF output ($\mathrm{aF}/\sqrt{\mathrm{Hz}}$)	0.2

creases both the complexity resulting from the non-linearity of the electrostatic feedback force and the sensitivity of the sensor gain to the references or supply.

In the closed-loop CT accelerometer implemented in [II], a summary of the parameters of which is shown in Table 3.2, the signal band was limited as a result of the parasitic resonance modes of the sensor element, suggesting that careful parallel design of the interface and the sensor element would be beneficial. The noise performance, although very good, was still inferior to that in the simulations, which is probably due to modeling problems regarding flicker noise. The noise performance of the readout is at the expected level and does not limit the sensor noise performance because of the modeling inaccuracy. In [I-IV] theoretical analysis, circuit design, and several solutions are presented in order to realize the analog closed loop, reduce the noise, improve the linearity and the stability of the closed-loop accelerometer, and digitize the high-voltage analog output signal. It is clear that the calibration of linearity, proper identification of dominating noise sources, and the use of a CT closed loop have made possible the design of the very high-performance accelerometer in [II].

4 Clock Generation within Sensor Interfaces

The necessity of transforming a sine into a square wave, or clock, is common in sensor systems that require any coherent discrete time signal processing. Within interface electronics for inertial sensors this often denotes some type of demodulation or coherent sampling. Examples that include the micro-gyroscope readout in [V], the amplitude demodulation in the accelerometer interface of [II], and the phase-coherent analog-to-digital conversion in the gyroscope interface of [58] take advantage of sine-to-square-conversion. The actual conversion is very simple, and can, in the simplest case, be done using a single inverter. However, if the conversion process is improperly designed, a faulty clock can result in a complete failure of the sensor system.

In sensor applications, especially with fully integrated frequency references, the frequencies required are fairly low, well below the GHz region that would allow a reasonable use of LC oscillators. If the sinusoidal signal is generated on-chip using an RC or GmC oscillator, the sine-to-square-conversion that is potentially required is not likely to limit the accuracy of the clock. This is because the available signal in electrical oscillators is high, which allows the effect of sine-to-square conversion to be lowered. On the other hand, a clock generated on-chip easily suffers from originally higher phase noise. If the mechanical sensor is capable of providing the frequency reference, as in, for example, gyroscopes [VII], the available signal magnitude might be low, whereas the quality of the signal can be excellent. In these cases the noise properties of the signal processing required to finally convert the sinusoidal current into a square wave clock are emphasized.

Phase-locked loops (PLL) offer the possibility of creating clock frequencies higher than the reference, shaping the phase noise of the output clocks, and maintaining accurate phase coherency between the reference and the output clock signals. In this way PLLs have become an indispensable tool for signal processing, including within sensor interfaces. The design of a PLL for clock generation offers the possibility of trading off silicon area and power consumption for noise performance, hence making efficient cost and power optimization possible. The essential issues related to phase noise, jitter, and clock generation are introduced in this chapter.

4.1 Introduction to Phase Noise and Jitter

In an ideal case a sinusoidal signal with an amplitude V_a and random constant phase ϕ carries power at a single frequency f_0 only;

$$V_{osc}(t) = V_a \sin(2\pi f_0 t + \phi). \tag{4.1}$$

However, any real oscillator that is used to generate the frequency reference introduces error. The source of the error can be, for example, losses within the oscillator and the resulting thermal noise, flicker noise, or power supply noise. After travelling through the oscillator, the error will partly express itself as a random phase component. Hence, the real output signal of an oscillator has a random time-dependent phase component $\phi_n(t)$ that accounts for the phase noise;

$$V_{osc}(t) = V_a \sin(2\pi f_0 t + \phi_n(t)). \tag{4.2}$$

When this sinusoidal component traverses linear circuits, such as buffers, some additive noise $V_n(t)$ will accompany the sine, but the phase noise remains unaltered:

$$V_{osc}(t) = V_a \sin(2\pi f_0 t + \phi_n(t)) + V_n(t). \tag{4.3}$$

If digital or SC circuits necessitate the use of a square wave clock, the very nonlinear process of sine-to-square conversion will cause $V_n(t)$ to be converted into additional $\phi_n(t)$.

As the phase in a real oscillator is a random time-variant factor, it also causes power to appear around the average carrier frequency. The frequency domain measure of the phase uncertainty is *phase noise*. The phase noise is defined using the frequency domain representation $S_\phi(f)$ of the phase fluctuations $\phi_n(t)$ [109]. Another commonly used expression for the phase noise is the ratio between the rms power spectral density (1 Hz spectral resolution) and the total power of the carrier, which is plotted as a function of the offset frequency from the average carrier frequency. This definition, also used in this section, is referred to using the symbol $\mathcal{L}(\Delta f)$, where Δf is the frequency offset from the carrier. The relative phase noise power is usually expressed in decibels and, hence, the unit for $\mathcal{L}(\Delta f)$ is accordingly $[\mathrm{dBc/Hz}]$. According to [110], $\mathcal{L}(\Delta f) \approx S_\phi(f)$ when $\Delta f = f$ is sufficiently large.

It should be taken into account that when the phase noise is measured by measuring the power spectral density, the amplitude noise, i.e. the time-dependent V_a will add to the noise power [111]. However, as the amplitude in oscillators, unlike the phase, is practically always a controlled parameter, the effect of amplitude noise is typically insignificant at low offsets Δf. Furthermore, for square wave signals the amplitude information is ideally completely discarded.

A typical example power spectrum of the fundamental frequency component of a noisy clock is sketched in Fig. 4.1, together with the corresponding single-sideband (SSB) phase noise plot. f_0 denotes the average frequency of the frequency reference and Δf is the frequency offset of interest. Now that the x-axis of the phase noise plot is a logarithmic function of the frequency offset, the two frequency-dependent regions where the reduction in the noise magnitude is either 30 dB or 20 dB per decade of frequency increase can be identified. These two regions correspond to the phase noise inflicted by the respective flicker and white noise sources of the oscillator. In the same way as flicker

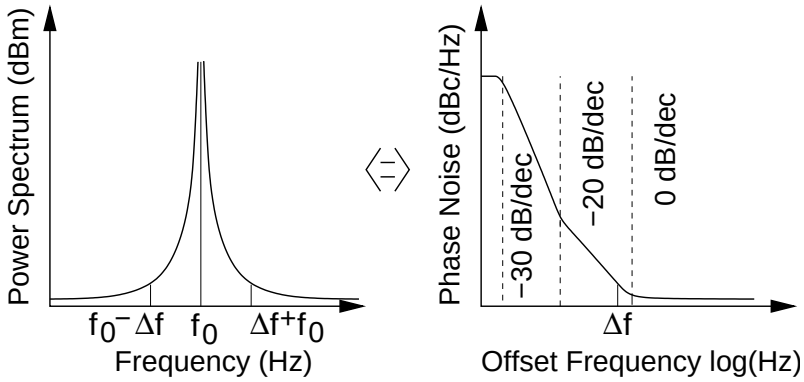

Figure 4.1: A sketched example of the power spectrum of the fundamental component of the frequency reference and the corresponding phase noise plot.

noise, other dominant colored noise sources can also alter the shape of the phase noise curve. Clearly, as the frequency dependency of the flicker noise power is of the form $1/f$ whereas white noise is frequency-independent, the oscillator reshapes the spectral density of the noise sources. It is generally agreed [111, 112, 113, 114] that this process results in the approximate equation

$$\mathcal{L}(\Delta f) \approx 10 \log \left(\frac{f_0^2}{\Delta f^2} c \right) \tag{4.4}$$

for the phase noise of a free-running oscillator when the noise sources are white. In the equation the constant c describes the combined contribution of all white noise sources to the phase noise. In the corresponding case of flicker noise, the approximate equation for the phase noise can be written as [110]

$$\mathcal{L}(\Delta f) \approx 10 \log \left(\frac{f_0^2}{\Delta f^3} c_f \right), \tag{4.5}$$

where c_f is defined as the effective contribution of flicker noise sources at 1 Hz. A typical shape of the frequency-dependent phase noise, which is formed when the phase noise power is contributed by both flicker and white noise sources, is sketched in Fig. 4.1.

Equations (4.4) and (4.5) are valid at sufficiently high offset frequencies, but still serve as approximations. At very low offset frequencies, as also shown by the sketched phase noise in Fig. 4.1, the approximation is not valid. An exact expression for the phase noise exists only in the case of white noise, and the more accurate form of (4.4) can be written as [114]

$$\mathcal{L}(\Delta f) = 10 \log \left(\frac{f_0^2 c}{\Delta f^2 + c^2 f_0^4 \pi^2} \right). \tag{4.6}$$

Clearly the phase noise plot is flat at very low offsets. The effect of low-frequency noise fluctuations has been analyzed in, for example, [113].

The phase noise equation (4.4) is also not valid in the flat region at high offset frequencies. The noise floor is exposed when the spectral density of the phase noise of the oscillator decreases below the floor. The noise floor can be due to the additive white noise that results from each buffer stage that follows the oscillator core. However, the flat noise floor can be actual phase noise as well. If the frequency component, "the sine", already exists and traverses some very non-linear circuitry, the frequency dependency of the original noise source will not change when it is being transformed to phase noise. This type of phase noise is typically inflicted by clock buffers for square wave signals, or by sine-to-square conversion [XI]. The two different cases, the noise shaping of an oscillator and the sine-to-square conversion, are depicted in Fig. 4.2. The difference in noise-shaping properties can be explained by the fact that in an oscillator, any disturbance that deflects the output phase causes the phase error to persist, whereas in sine-to-square conversion the momentary disturbance affects only the current zero crossing point. Mathematical analysis of the sources and development of phase noise in oscillators is presented in [111, 112, 114], to mention but a few different approaches. In [112] the linear time invariant (LTI) analysis is based on average effect of different noise sources and the definition of new Q-value for the noise shaping function of different oscillators. In [111, 115] a linear time-variant analysis is developed to allow phase noise prediction with the help of an impulse sensitivity function (ISF), which describes the time-variant sensitivity to different noise sources. In [114] complex non-linear analysis is presented for the evaluation of the phase noise generation process.

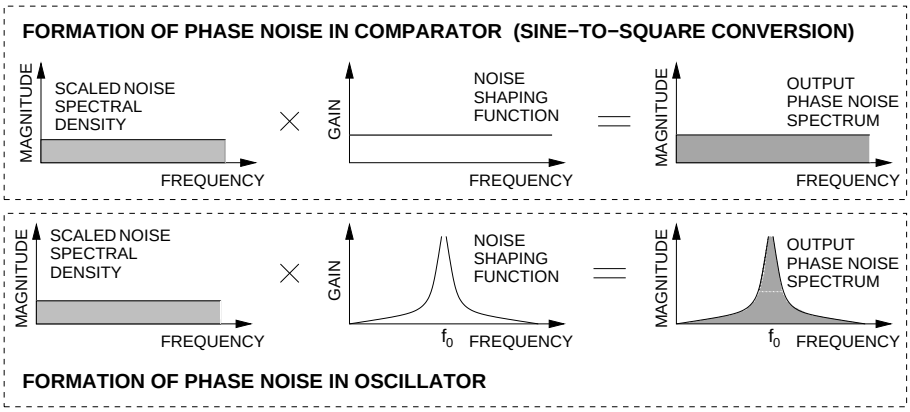

Figure 4.2: A sketch of the process by which the white noise within an oscillator, or the white noise added to a sine reference before sine-to-square conversion, is converted to phase noise.

If the oscillator output is considered a square wave signal, a clock, then ideally the zero crossings of the clock occur at a constant rate. In practice, however, the clock edges deflect from the ideal ones. The magnitude of the deflection is quantified using different definitions of *jitter*. In the same way as the phase noise allows us to analyze the non-ideal properties of the oscillator in the frequency domain, jitter represents the same non-idealities in the time domain. Here the jitter is expressed in [s].

The accumulated timing error, the jitter σ_{abs}, is measured over a time period of ΔT. According to [110], the absolute jitter can be written as

$$\sigma_{abs}^2(\Delta T) = \frac{1}{(2\pi f_0)^2} \int_{-\infty}^{\infty} S_{\phi\_srn}(f) df, \tag{4.7}$$

where S_{ϕ_srn} is the frequency domain representation of the increment phase error $\phi_{snr}(t) = \phi_n(t) - \phi_n(t - \Delta T)$. Hence, S_{ϕ_srn} can be treated as the phase error accumulated over the time interval ΔT. If the phase noise is inflicted by white noise, i.e. $\mathcal{L}$ corresponds to (4.4),

$$\sigma_{abs}^2(\Delta T) = \int_{-\infty}^{\infty} c \frac{\sin^2(\pi f \Delta T)}{\pi^2 f^2} df = c\Delta T. \tag{4.8}$$

The absolute jitter depends on the measurement (accumulation) time ΔT.

The rms jitter for a single period can be obtained by setting the ΔT to be equal to $1/f_0$ in (4.8). The resulting equation for the jitter can be written as

$$\sigma_{jper}^2 = c/f_0. \tag{4.9}$$

An alternative expression for the *period jitter* for the phase noise shape equal to (4.4) or (4.6) can be written as [116]

$$\sigma_{jper}^2 = \mathcal{L}(\Delta f) \frac{\Delta f^2}{f_0^3}, \tag{4.10}$$

where $\mathcal{L}(\Delta f)$[1] denotes the magnitude of the phase noise at Δf.

The period jitter, also known as the cycle-to-cycle jitter, is different from the *cycle jitter*, which is defined, according to [117], as the rms difference between the oscillation period and the mean oscillation period. The cycle jitter is, hence, also capable of modeling slow frequency drift, unlike the period jitter.

In most cases it is not possible to obtain the expression for the jitter in closed form, when the dominant noise sources are colored. Hence, the jitter can be calculated by performing the integral of (4.7) numerically. Further information can be found in, for example, [110, 116, 118].

Many different types of analysis have been proposed to solve the magnitude of the phase noise and jitter in CMOS oscillators [112, 119, 120]. The most common types of oscillators, GmC and ring oscillators, which are needed for sensor applications, exhibit moderately high phase noise as a result of their low Q-value and wide-band nature. The non-linear behavior of the oscillators inflicts folding, which increases the level of phase noise by, for example, downconverting white noise and upconverting flicker noise. Examples of both a relaxation oscillator and a ring oscillator are shown in Fig. 4.3. Although

[1]The single-sideband power to the carrier power ratio is used here in linear scale (unit $[1/\mathrm{Hz}]$).

the circuits represent very simple versions of oscillators, they can be examined in order to coarsely identify the common factors affecting the phase noise in the two oscillator topologies.

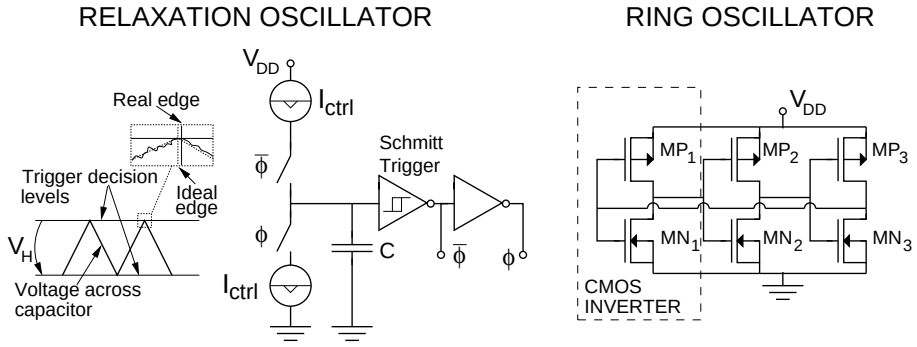

Figure 4.3: Simple example circuit diagrams of both a relaxation oscillator and a ring oscillator for identification of the sources of the phase noise.

In the relaxation oscillator shown in Fig. 4.3 [120], the oscillation frequency depends on the hysteresis of the Schmitt trigger V_H, control current I_{ctrl}, and capacitor C as

$$f_0 \sim \frac{I_{ctrl}}{V_H C}. \tag{4.11}$$

The current I_{ctrl} will be integrated to the capacitor C and, hence, will be low-pass filtered. However, low-frequency noise can have a significant effect on the phase noise and can be evaluated through narrow-band frequency modulation [112]. The noise in V_H, which corresponds to the input-referred noise of the Schmitt trigger and also affects the frequency, will not be filtered in the same way as the noise in the control current. The effect of this noise source can be minimized by maximizing the derivative of the capacitor voltage at the trigger point, i.e. by maximizing the swing across the capacitor C. The actual source of noise, the Schmitt trigger, should be a low-noise device. The noise should be evaluated in the Schmitt trigger at the moment of state change.

In the same way as in the relaxation oscillator, the ring oscillator phase noise is also approximately inversely proportional to the signal derivative at the input/output node of each inverter. Thus, with an increasing number of stages (in Fig. 4.3 three stages), the signal transitions become faster when the frequency is kept constant. However, with an increasing number of stages, the number of noise sources also increases [119]. This makes the phase noise in single-ended ring oscillators almost independent of the number of stages when the frequency is assumed to be constant. On the other hand, the larger the current through the inverters, the lower the phase noise. This relation enables a trade-off to be made between the phase noise power and the oscillator power consumption. The flicker noise effect is minimized by the symmetry of the rising and falling edges [119]. This requirement also holds true for the half-circuits of the differential ring oscillators, while the mere differentiality does not reduce the effect of internal noise sources.

The phase noise resulting from power supply noise can be an additional factor limiting the accuracy of oscillators. Better supply insensitivity usually favors differential oscillators, even though the internal noise would not be improved. This is analyzed in detail in, for example, [117]. Generally speaking, power supply noise can be minimized by making the factors that define the oscillation frequency as supply-insensitive as possible. For example, the capacitors can be isolated from a noisy substrate by placing them on an isolated well that is connected to local clean potential, the bias for the oscillator transistors can be made supply-insensitive, and the supply noise can be made to appear as a common-mode error by using differential circuits.

4.1.1 The Effect of Phase Noise and Jitter

In order to define the allowed limits for the jitter or phase noise, the effect of this type of noise within the sensor interface should be identified. In digital signal processing, if the required clock frequencies are moderately low, below a few tens of MHz, timing errors can quite easily be avoided. However, the circuits that are critical are typically either continuous-time analog circuits or, when transforming the signal between discrete and continuous time regions, switched-capacitor devices, such as data converters.

The effect of phase noise in data converters or mixers can be identified either in the frequency or the time domain. In a mixer, demodulator or modulator, the time-domain product of the clock and the signal can be written as

$$V_{mix}(t) = V_s(t)V_{osc}(t), \tag{4.12}$$

where V_s represents the signal and V_{osc} the noisy frequency reference from the local oscillator. In order to consider an example case, let V_s be an ideal sinusoidal signal with an amplitude V_{as} and frequency f_s, and V_{osc} the signal in (4.2);

$$\begin{aligned} V_{mix}(t) =& V_{as}\sin(2\pi f_s t)V_a\sin(2\pi f_0 t + \phi_n(t)) \\ =& \frac{V_{as}V_a}{2}[\cos(2\pi t(f_0 - f_s) + \phi_n(t)) - \cos(2\pi t(f_0 + f_s) + \phi_n(t))]. \end{aligned} \tag{4.13}$$

The phase noise term ϕ_n, and the corresponding phase noise spectrum, are transferred unaltered to both the new center frequencies.

In sampling systems, e.g. data converters, the effect of phase noise is somewhat different and has been considered in, for example, [116]. In [116] the effect of phase noise is derived in the case of the sampling of an ideal sine at the frequency f_s. The signal-to-spectral noise ratio (S/N_L) as a function of the frequency offset can be written as [116]

$$S/N_L(\Delta f) = \frac{f_s^2}{f_0^2}\mathcal{L}(\Delta f), \tag{4.14}$$

where $\mathcal{L}(\Delta f)$[1] is the phase noise power of the sampling clock. According to (4.14), if it is assumed that the frequency offset is sufficient, the shape of the phase noise is directly transferred to the spectrum of the sampled signal, while the magnitude is scaled by the frequency ratio between the clock at f_0 and the signal at f_s.

When considering (4.6), the phase noise is frequency-independent at very low offset frequencies, whereas the corner frequency ($cf_0^2\pi$) is dependent on the square of the clock (or the sampled signal) frequency. This can be illustrated by a simple simulation where strong white noise is fed to the voltage-controlled oscillator (VCO) input and the resulting VCO output clock is divided by factors of two and four. The resulting phase noise for all three different frequencies is shown in Fig. 4.4. As indicated by (4.14), halving the input frequency of the sampler should reduce the spectral power of the sampled signal at the same offset by 6 dB. The division of the clock frequency has the same effect on the phase noise. This behavior is observed in the phase noise plot shown in Fig. 4.4 at sufficiently large offsets. However, the corner frequency in the spectrum is dependent on the square of the clock frequency, as predicted by (4.6), and at very low offset frequencies the spectral noise power increases with decreasing f_s.

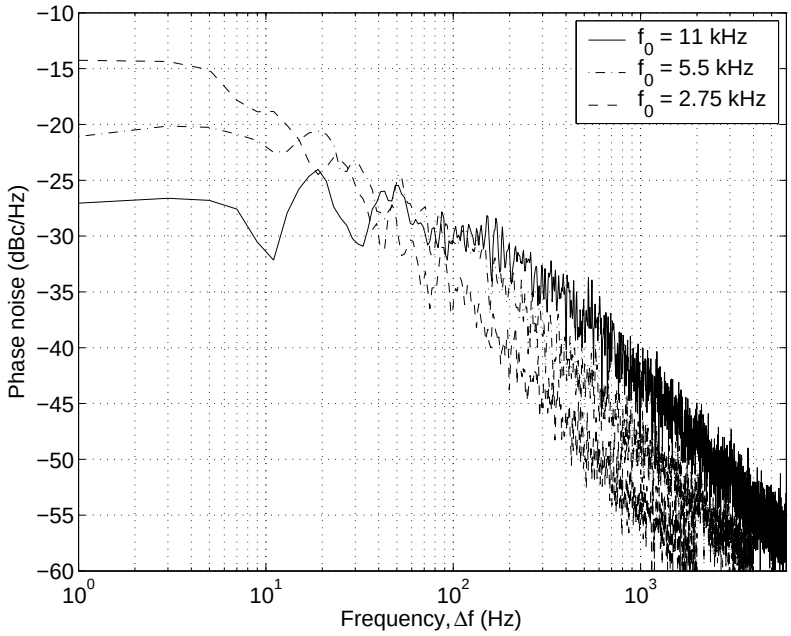

Figure 4.4: Phase noise inflicted by white noise at VCO input and the effect of frequency division.

An important special case of sampling which often occurs in sensor interfaces is the processing of a signal when the carrier is at the same frequency as the signal being processed or at a proper fraction of it. This can be the case, for example, during full-wave rectification, which is used to extract the amplitude information without sampling the signal, or

[1]The single-sideband power to the carrier power ratio is used here in linear scale (unit $[1/\mathrm{Hz}]$).

during the sampling of the amplitude information. These two cases are considered in Fig. 4.5.

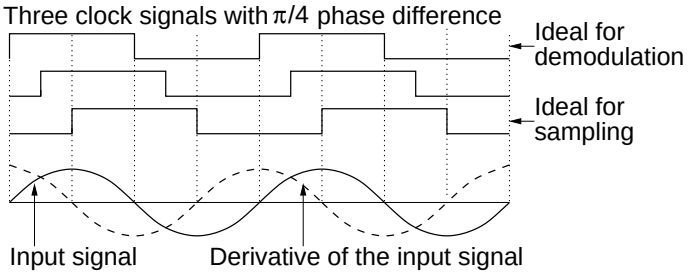

Figure 4.5: The processing of a sinusoidal signal using a synchronized clock.

The demodulation, performed using either a square wave or sinusoidal carrier, has minimum sensitivity to jitter when the carrier and the signal are in phase. For example, (4.13) can be modified in such a way that f_s is equal to f_0. When the phase error is also divided into dc and time-dependent errors, $\phi_n(t) = \phi_{dc} + \phi_{nx}(t)$, the result of the demodulation can be written as

$$V_{mix}(t) \approx \frac{V_{as}V_a}{2}[1 - \phi_{dc}\phi_{xn}(t)], \tag{4.15}$$

where the unwanted signal component at $2f_0$ has been removed. The sensitivity of $V_{mix}(t)$ to the noise $\phi_{nx}(t)$ clearly is minimized when $\phi_{dc} = 0$.

When the amplitude is being sampled and either clock edge defines the sampling instant, the derivative is minimized and the signal value is maximized when the sampling is performed at either peak value of the input signal. This is thus the desired sampling instant. If the phase between the clock and the signal is not the ideal one, $\pi/2$, the sampling instant will not coincide with the zero crossing of the derivative and the sensitivity to jitter increases. At the sampling instant, the derivative of the input signal, together with the rms jitter, defines the magnitude of the resulting voltage error. The rms voltage error can be calculated simply as

$$V_{n\_rms\_out} = \sigma_{abs}\frac{dV_{in}(t)}{dt}_{t=sampling\ instant}. \tag{4.16}$$

The rms, or absolute, phase jitter σ_{ϕ_abs} in $[\mathrm{rad}]$, or rms jitter σ_{abs} in $[\mathrm{s}]$, can be approximately calculated from the phase noise spectrum as[1] [121]

$$\sigma_{\phi\_abs} = \sigma_{abs}2\pi f_0 \approx \sqrt{\int_0^\infty 2\mathcal{L}(\Delta f)df}, \tag{4.17}$$

which is not practicable in the case of open-loop oscillators. The exact absolute jitter, which was given in (4.7), will not converge for infinite measurement time. Likewise,

[1]The single-sideband power to the carrier power ratio is used here in linear scale (unit $[1/\mathrm{Hz}]$).

(4.17) gives more useful results when the phase noise is limited at low offset frequencies or this region could be considered irrelevant. This is typically the case when the oscillator operates inside a PLL which utilizes an "ideal" reference [121]. For example, in gyroscopes, the good-quality signal from the mechanical element functions as the frequency reference for the PLL and can be considered phase-noiseless compared to the sine-to-square conversion and the PLL. Detailed analysis of the jitter and phase noise for PLLs is also given in [110].

For square wave signals the noise bandwidth is limited by the rate at which zero crossings, or edges, occur. The white noise floor in the phase noise spectrum, formed, for example, during the sine-to-square conversion, can dominate the jitter. The computation of the rms jitter can be done in the time domain, if the rms noise voltage V_{n_rms} before the sine-to-square conversion, and the amplitude V_{as} and frequency f_0 of the sinusoidal reference, are known. Now the error can be written as

$$\sigma_{\phi\_abs} = \sigma_{abs} 2\pi f_0 = \frac{V_{n\_rms}}{V_{as}}. \tag{4.18}$$

The same parameters can be calculated in the frequency domain using (4.17), with the upper integral bound changed to be equal to f_0. The two methods are illustrated in Fig. 4.6.

It is most straightforward to accomplish the minimization of the effect of the noise during sine-to-square conversion by increasing the signal-to-noise ratio of the input sine, i.e.

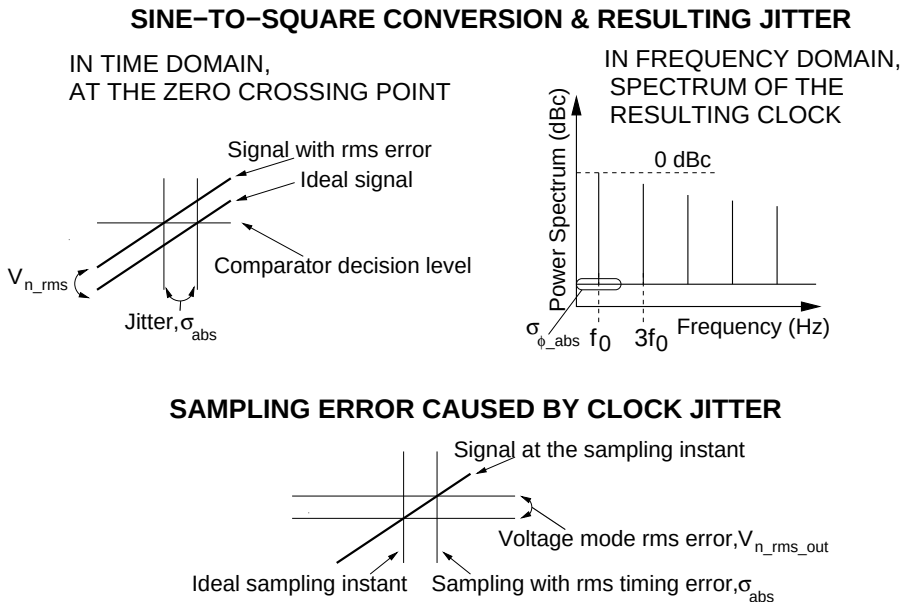

Figure 4.6: Evaluation of the jitter of a square wave signal and the resulting sampling error caused by the jitter.

by increasing the amplitude of the sine and by minimizing the total noise at the comparator input. A faulty conversion process, where the reference sine is contaminated by excess noise or cross-coupled signals, can cause extra pulses in the clock signal that is created. These extra switchings cause incorrect charge transfer in discrete-time circuits and the incorrect operation of digital circuits. The sine-to-square conversion process is especially prone to extra switching when the frequency and the amplitude of the sine are low compared to the noise bandwidth and the speed of the comparator.

4.2 Phase-Locked Loop for the Sensor Interface

The basic functionality of a PLL (see Fig. 4.7) is, generally, to take either a square wave or sine as a reference input and to extract the phase information from this signal. This information is then filtered and employed to control an oscillator that produces a frequency which is typically higher than the reference frequency. The feedback is created by comparing the phase of the divided oscillator output to the input reference. Proper design of the loop ensures that the reference and the divided oscillator output remain synchronized and the PLL locked. The PLLs are generally a well-documented topic covered by many books, for example [122]. Hence the purpose of this section, instead of repeating the detailed analysis, is to provide a short overview of the topic from the sensor interface design point of view.

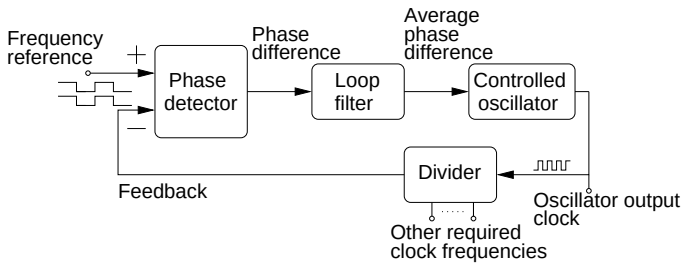

Figure 4.7: The basic architecture of a PLL.

Compared to the design of a radio frequency PLL, used for example in telecommunications, somewhat different design issues rise when clock generation is required for a sensor interface with an audio frequency reference signal. As the purpose of the PLL within a sensor interface is, in most cases, simply to produce synchronized clock signals with a constant reference frequency, the focus of the design can be set to achieve the goal with minimum resources. The resources, such as the supply current, chip area, and external components, can be traded for higher phase noise. On the other hand, the sensitivity of the system to the phase noise can also be reduced, for example by minimizing the phase errors, such as ϕ_{dc} in (4.15), that increase the jitter-inflicted noise.

The available architectures for PLLs include both analog PLLs and digital PLLs. The analog PLLs consist of charge pump PLLs, PLLs with a switched-capacitor (SC) loop filter, switched-current (SI) PLLs, and PLLs with a multiplier as the phase detector and a continuous time loop filter.

Using a multiplier, especially a full-wave rectifier, as the phase detector, is a feasible optional topology for a PLL that is operated as a part of the sensor interface. This is due to the potentially reduced sensitivity to the noise of the sinusoidal frequency reference. The absence of frequency detection and necessity for heavier filtering required after the phase detection, however, complicate the design compared to a basic charge pump PLL. This type of approach is also reviewed in [VII]. Another optional analog PLL topology is a switched-current (SI) PLL, which allows the PLL to be implemented with transistors only. One example of this type of PLL, which requires no explicit phase detector, is given in [123].

If the sensor interface sets the requirements for the semiconductor technology that is used, often denoting higher voltages or thicker oxide and high-quality analog components and the clock generation does not require a fractional division ratio, a traditional second-order charge pump PLL becomes a feasible alternative. Both the implementations [IX] and [X] use this type of PLL, because of its applicability for integration, simple structure, and the possibility of easily evaluating and minimizing the chip area required. In fact the two components of the simplest loop filter, a single resistor and capacitor, can be selected to allow minimum chip area as reported in [X]. In [IX] the large resistor in the loop filter is replaced by a simple SC equivalent in order to avoid using very high resistances and to reduce the variation of the voltage across the loop filter resistor. The most severe limiting factor for all PLL topologies that include discrete time operation is the leakage currents at the loop filter, which start to increase the jitter at the PLL output. Hence, avoiding this limitation also favors the use of transistors with thick gate oxide and a large threshold voltage, and a resulting smaller leakage.

Many of the analog PLLs utilize digital logic, whereas an all-digital PLL (ADPLL) performs all the signal processing (phase comparison, filtering, division, frequency control etc.) in the digital domain. ADPLLs have emerged together with the evolving CMOS technology and decreasing linewidths, which have enabled large numbers of digital cells to be integrated within a continuously decreasing area. At the same time, increasing leakage and decreasing supply have complicated the implementation of analog circuits, such as varactors, and increased the overall sensitivity to noise. While ADPLLs have been developed to serve application areas such as wireless communication, microprocessors, and digital signal processing and to allow all the circuitry to benefit from the state-of-the-art semiconductor technologies, sensor interface electronics can still rely on technologies far from deep sub-micron linewidths. This fact also makes it more difficult to know whether ADPLLs offer any advances over analog PLLs when speaking of sensor interfaces.

The traditional asset of ADPLLs is their use of hardware description languages (HDL), which allows the PLL to be transferred to new technologies more easily, even though the digitally controlled oscillator (DCO) often still requires careful SPICE-level simulations. Another new degree of freedom is the freer design of algorithms for frequency locking. Probably the most significant assets of ADPLLs are their reduced chip area with modern technologies, and also the power savings they offer because some of the dc current consuming blocks, such as charge pumps, can be left out. However, the actual difficulty is to evaluate which of these benefits can be considered important for the sensor system being designed, especially when the linewidth of the technology used is just below one micron and frequencies required are in the order of few MHz. Issues such as the increased supply noise resulting from the heavy digital signal processing and increased complexity due to for example the dithering required to produce an accurate DCO output frequency with no spurious tones can make the ADPLLs less attractive. Detailed information about the topic can be found for example in [124].

As the charge pump PLL is the topology chosen for the implementation, a short introduction to the dynamics of these PLLs is presented in the following section.

4.2.1 Dynamics and Noise-Shaping Properties of the Charge Pump PLL

As already briefly discussed in connection with phase noise, the PLL can have a significant effect, either beneficial or detrimental, on phase noise. In order to make possible the identification of the factors affecting the phase noise of the PLL output, the dynamic properties of charge pump PLLs are introduced in this section.

The block diagram of a second-order charge pump PLL is shown in Fig. 4.8. The phase-frequency detector (PFD) extracts either the phase difference, when the PLL is in lock, or the frequency difference, when the PLL is acquiring the lock, between the input reference and the feedback signal. This asynchronous digital block creates the control signals for the charge pump, which converts the phase difference into a current pulse. The gain from the PFD input to the charge pump output is denoted by K_{CP}, the magnitude of which is determined by the current sources so that $K_{CP} = I_{CP}/(2\pi)$. The current pulse is fed to the loop filter, which in a charge pump PLL is formed by the impedance $Z(s)$. The capacitor C of the loop filter integrates the current, allowing infinite dc gain in the loop, while the resistor R is required for stabilization. Often a small capacitor C_2 is added in parallel with the series-connected C and R in order to filter out the large voltage spikes occuring when the charge pump current surges through R. The size of this additional capacitor is selected to be such that it does not essentially affect the stability of the loop. The SC loop filter in [IX] automatically levels the voltage across the whole clock period and hence does not require additional filtering. The effect of C_2 is ignored during this analysis, because the current pulses during the steady-state operation of the PLL with a

low reference frequency are very short compared to the reference period, and hence can be filtered without affecting the dynamics of the PLL.

The voltage mode output of the loop filter controls the voltage-controlled oscillator (VCO). The gain of the VCO, from the control voltage to the output frequency must be integrated, i.e. multiplied by the $1/s$-term in the Laplace domain, in order to get the gain from the voltage to the output phase ϕ_{out}. After division by N, the VCO output phase is compared with the phase of the input reference. The resulting negative feedback and infinite loop gain cause the rising edges of the reference ϕ_{in} and the feedback signal to coincide and the dc output current of the charge pump to become zero. The linear model in Fig. 4.8 can be used to derive the TFs from the input nodes to the output phase ϕ_{out}. The TFs in the Laplace domain are given in Table 4.1.

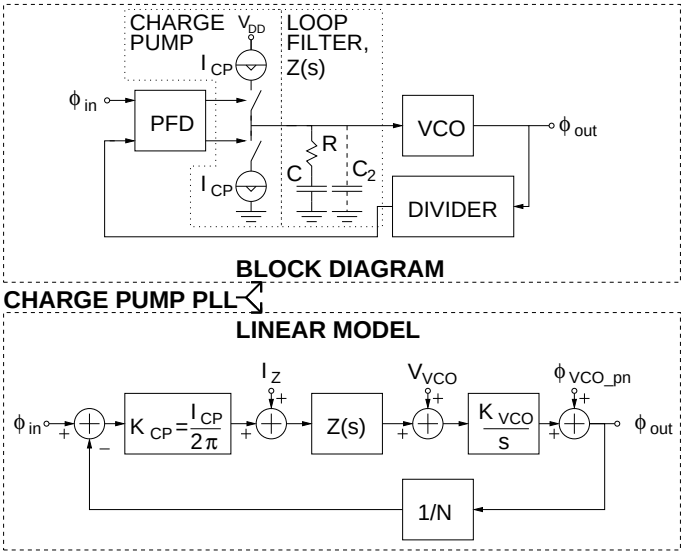

Figure 4.8: The block diagram and the linear model of a second-order charge pump PLL.

Table 4.1: Transfer functions of the charge pump PLL.

$\frac{\phi_{out}}{\phi_{in}}(s)$	$\frac{sNRC+N}{s^2CN/(K_{VCO}K_{CP})+sRC+1}$
$\frac{\phi_{out}}{I_Z}(s)$	$\frac{(sRC+1)N/K_{CP}}{s^2CN/(K_{VCO}K_{CP})+sRC+1}$
$\frac{\phi_{out}}{V_{VCO}}(s)$	$\frac{sNC/K_{CP}}{s^2CN/(K_{VCO}K_{CP})+sRC+1}$
$\frac{\phi_{out}}{\phi_{VCO\_pn}}(s)$	$\frac{s^2NC/(K_{CP}K_{VCO})}{s^2CN/(K_{VCO}K_{CP})+sRC+1}$

The phase noise in the input reference ϕ_{in} has a low-pass TF to the PLL output. Now that the gain at low frequency offsets is defined by N, it also emphasizes the fact that the phase noise of the frequency reference must be low enough not to dominate the PLL phase noise. This can also be noticed in Fig. 4.9, which depicts the sensitivity of the PLL to the phase noise of both the reference and the VCO. On the other hand, the PLL offers an opportunity to filter the phase noise of the reference by reducing the speed of the loop. This could be done to some extent on-chip by decreasing the charge pump current, redesigning the loop filter, and reoptimizing the area of the filter components. However, this results in a somewhat increased chip area, but also increased phase noise as a result of the bigger filter resistor. The effect of the loop filter noise can be seen from $\phi_{out}/V_{VCO}(s)$, which is a band-pass TF. In the example case of Fig. 4.9, the phase noise resulting from the 7 $\mathrm{M}\Omega$ filter resistor would be -65 $\mathrm{dBc/Hz}$ at a maximum (offset of 500 Hz). The effect of the noise of the charge pump is more than 20 dB below the noise of the loop filter and can therefore be neglected. This is mostly thanks to the very low ratio between the conduction time of the charge pump and the reference period when the PLL is in lock [121].

The VCO phase noise becomes high-pass-filtered in the PLL, as can be seen in Fig. 4.9. Hence, with a low phase noise reference, the wide bandwidth of the PLL allows the phase noise of the VCO to be filtered, and vice versa; with a good-quality VCO the low bandwidth of the PLL allows the noise of the reference to be cleaned up. The divider can be considered noiseless when no fractional division ratio is required.

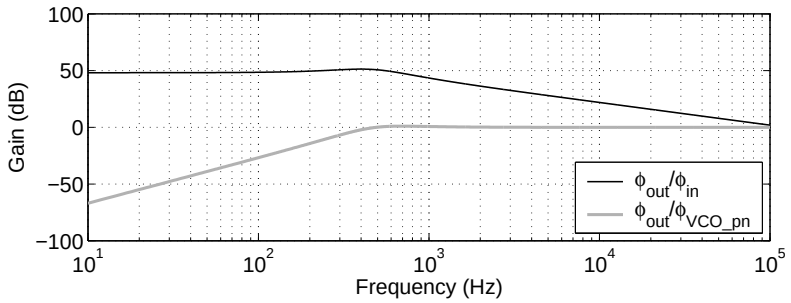

Figure 4.9: The gain TFs from the phase noise of both the reference and the open-loop VCO to the PLL output. The TFs are valid for the PLL with the properties shown in Table 4.2, for which N is 256 and K_{VCO} 4.7 $\mathrm{Mrad/(sV)}$. When considering the phase noise shaping, the x-axis corresponds to the frequency offset Δf from the average carrier frequency.

4.3 Implemented PLL of [X] and the Measured Characteristics Including the Effect of Sine-to-Square Conversion

The phase noise properties of the PLL that was implemented were optimized according to the theory described in [X]. The structure of the PLL is similar to the one that was simulated in [X]. The chip micrograph is shown in Fig. 4.10. The area of the PLL core is 0.4 mm^2 and the supply current roughly 1.5 mA. The PLL was measured to have lock ranges of 3-11 and 8-15 kHz with free running frequencies of 0 and 8 kHz, respectively.

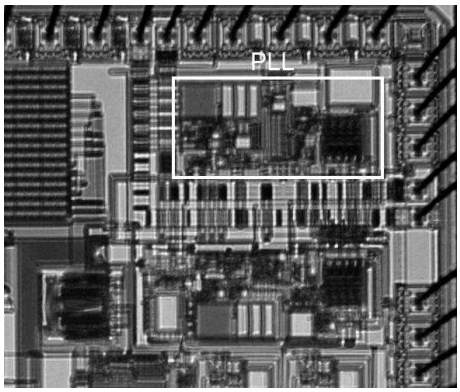

Figure 4.10: A microphotograph of the PLL that was implemented.

The PLL was first measured using a low-phase-noise square wave reference signal. This enables the PLL only to be characterized, without the phase noise resulting from the sine-to-square conversion. After the measurements using a low-noise external reference, a sinusoidal wave was fed into the on-chip comparator and the resulting square wave signal was used as a reference for the PLL. The phase noise of the PLL output was measured and compared to the properties of the PLL with an "ideal" reference.

4.3.1 PLL with an External Square Wave Reference

In order to be able to compare the measured phase noise with the theory in [X], both the phase noise-shaping effect of the PLL (see Fig. 4.9) and simulated noise of the noise sources internal to the PLL are taken into account. The phase noise of the open-loop VCO can be calculated using (9) and (11) in [X]. The white noise inflicted by the 7-$\mathrm{M}\Omega$ resistor in the loop filter is calculated using (9), in such a way that $I_{nf}/\Delta f^{0.5}$ is replaced by I_{nw} in (9). Furthermore, the flicker noise in the bias current of the VCO comparator (see Fig. 4 in [X]) can be taken into account by writing (11) in [X] into the form

$$\mathcal{L}(\Delta\omega) \approx 10\log\left(\frac{1}{4}\frac{f_0^2}{\Delta f^3}\frac{I_{nf\_COMP}^2}{I_{BCOMP}^2}\right), \tag{4.19}$$

Table 4.2: Simulated parameters for evaluation of phase noise

f_0	2.56 MHz
V_H	1.67 V
V_n	36 nV/$\sqrt{\text{Hz}}$
I_{nf}	64 pA/$\sqrt{\text{Hz}}$
I_{nw}	3.4 pA/$\sqrt{\text{Hz}}$
I_{nf_COMP}	180 pA/$\sqrt{\text{Hz}}$
I_{BCOMP}	0.1 mA
m	15
K_{CCO}	0.47 Trad/(sA)
ω_N	2.5 krad/s
ζ	0.45

where I_{nf_COMP} is the flicker noise current of the comparator bias current I_{BCOMP} at 1 Hz. The effect of white noise in I_{BCOMP} is included in the comparator input-referred noise. The simulated parameters for (9) and (11) in [X], for (4.19) and for the transfer function

$$\frac{\phi_{out}}{V_{VCO\_pn}}(s) = \frac{s^2 NC/(K_{CP}K_{VCO})}{s^2 CN/(K_{VCO}K_{CP}) + sRC + 1} = \frac{s^2}{s^2 + 2\zeta\omega_N s + \omega_N^2}, \tag{4.20}$$

are given in Table 4.2 and are used to evaluate the theoretical magnitude of the phase noise. The theoretical phase noise, together with the measured phase noise, which matches well with the theory, are shown in Fig. 4.11 at offset frequencies ranging from 60 Hz to 30 kHz.

In the VCO that was implemented, external current can be used to increase the free running frequency of the VCO. Increasing the external bias current decreases the required level of the control current, which can have a noticeable effect when, for example, the charge pump operates close to either supply rail. The phase noise (gray line) in Fig. 4.11 is measured with an external current, which allows the charge pump voltage to be balanced roughly half-way between the supply rails. Compared to the other measured curve (black line), the spike at a 10-kHz offset is reduced by about 20 dB. The zero bias forces the VCO control close to the upper supply rail, which further breaks the balance between the negative and positive currents of the charge pump. The imbalance between the currents, when combined with a delay in the PFD and charge pump, results in a spurious component at the PLL output [125]. The resulting distortion can be lowered by balancing the currents with a lower VCO control voltage, as was observed with the increased VCO free-running frequency, i.e. with an increased external bias current.

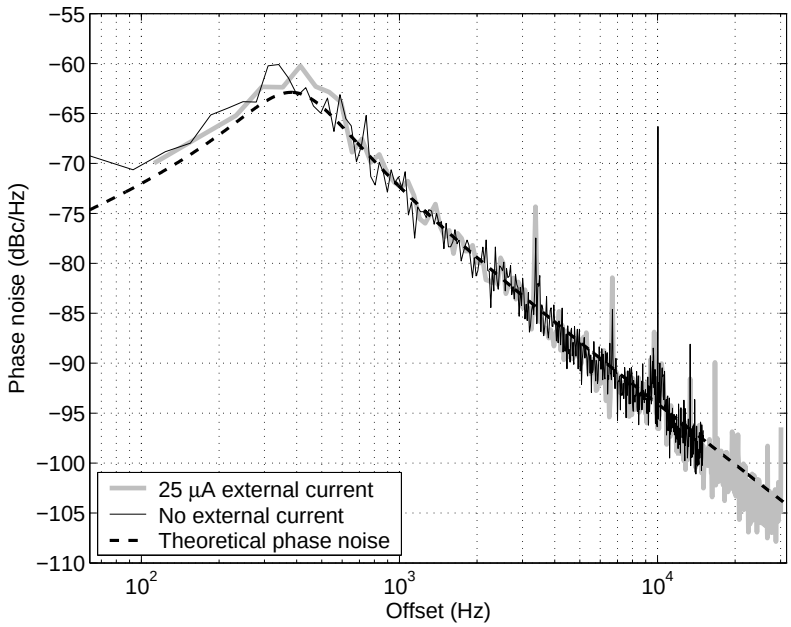

Figure 4.11: Measured and theoretical PLL phase noise with a low-noise reference signal.

4.3.2 Effect of Sine-to-Square Conversion on Phase Noise

The comparator used for creating the square wave reference is a traditional two-stage comparator with a differential input and single-ended output. The propagation delay is approximately 43 ns with a supply current of 240 $\mu\mathrm{A}$. The comparator is preceded by several active gain and filter stages which dominate the noise at the input of the comparator. A sinusoidal 10 kHz reference was fed to the system in such a way that the amplitude at the comparator input was measured to be 0.33 V. The noise density at the input of the comparator, referred to the input signal, is shown in Fig. 4.12. Both noise components will have a significant effect on the output noise, the low-frequency noise because of its high level and the high-frequency noise because of the high noise bandwidth. The input-referred noise of the comparator is considerably smaller than the noise magnitude in Fig. 4.12 and is therefore neglected.

As the noise spectra in Fig. 4.12 now represent $N(\omega_n)$ in [XI], the clock spectrum can be evaluated in a similar way as in the example in the paper. Now the PLL output is used for evaluating the spectrum, and hence the study is limited to the low-frequency offset region only, where the gain ϕ_{in}/ϕ_{out} is constant, 48 dB (see Fig. 4.9). The resulting clock spectra, with different levels of input amplitude, are shown in Fig. 4.13, while the theoretical lines of Fig. 4.13 are calculated on the basis of the input-referred noise. The reference level $-0\ \mathrm{dB}$ corresponds to the noise in Fig. 4.12. The measured phase noise is inversely proportional to the reference amplitude, as expected.

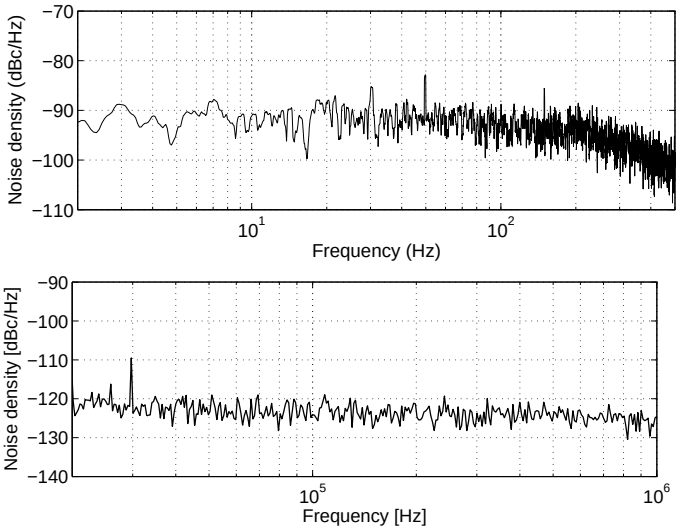

Figure 4.12: Low-frequency noise (top) and wide-band noise (bottom) at the input of the comparator referred to the 10-kHz reference signal.

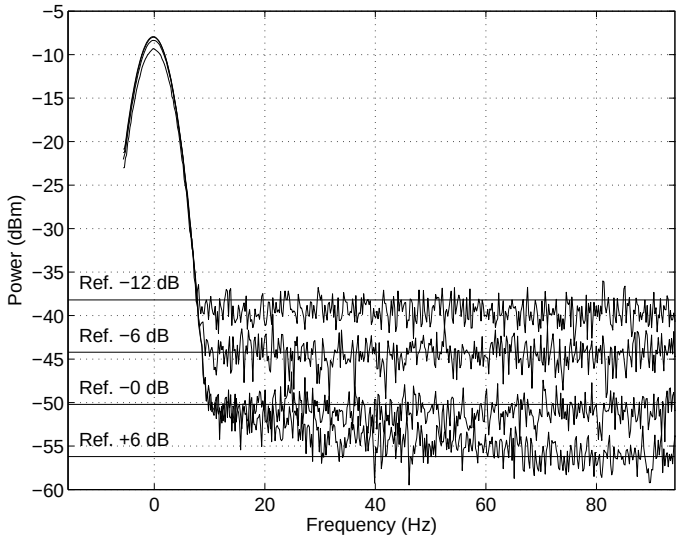

Figure 4.13: Measured and theoretical output clock spectra of the PLL when the square wave reference is created using comparator and sine input.

The resolution bandwidth in the spectra of Fig. 4.13 is 5 Hz, and hence, the phase noise magnitude can be evaluated to be roughly 20 to 40 dB worse than for a PLL with a low-noise reference. This indicates that the noise at the comparator input strongly dominates the phase noise. The situation could be improved by more than 10 dB by simply band-limiting the noise. The results also indicate that the phase noise of the PLL in this case is overdesigned and a significant amount of supply current could be saved without significantly affecting the noise at the output of the PLL.

4.4 Discussion

PLLs are also important tools within capacitive inertial sensors and allow the precise generation and synchronization of clock signals. A compact PLL, for example for the interface of a gyroscope, can be designed with no external components. It is, however, essential to identify the effect of the clock inaccuracies in order to make possible a PLL design that is efficient in terms of power and area. In general, the clock quality requirements are relieved if the derivative of the signal is minimized at the sampling instant and the absolute value of the signal is minimized during the clock transition in the case of CT full-wave rectification. This is also a general reason why the existence of a heavy quadrature signal in gyroscopes sets very stringent requirements on the clock signals in order not to increase the noise or the ZRO.

Both the PLLs that were implemented and are part of the research work in this thesis, [IX] and [X], are traditional charge pump PLLs, optimized for use within sensor interfaces. The sine, which was obtained from the mechanical element, was converted into a square-wave frequency reference for these PLLs. It was seen in Section 4.3, which covered the actual characterization of the PLL in [X], that a poorly designed sine-to-square conversion caused the phase noise of the reference to exceed that of the PLL by tens of decibels. On the other hand the later design reported in [IX] and used in the gyroscope of [V] had the noise band properly limited before the sine-to-square conversion in the comparator. The filtering comprised an integrator, which was used as a phase-shifting element in the drive loop, and a passive high-pass filter. The resulting spectra of the output clock of the PLL both with an external reference and during the normal operation of the gyroscope are shown in Fig. 4.14. The two spectra indicate only a small difference in the phase noise at the frequency where the filtering of the reference sine adds most noise. A current consumption that is smaller than 10 μA and a chip area of 0.13 mm^2, while the DT loop filter offers the possibility of reducing the chip area further, indicate that the PLL in [IX] is both low-power and compact and is easily fitted within the sensor interface.

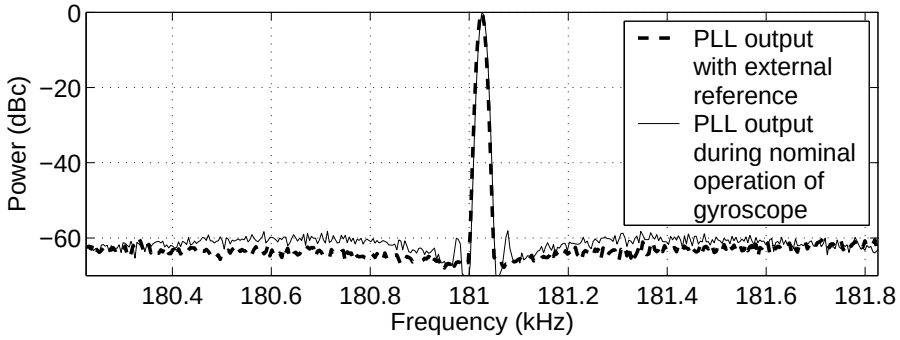

Figure 4.14: Comparison between the PLL output clock spectra both during normal operation of the gyroscope and with external square wave reference.

5 High-Voltage Generation within Sensor Interfaces

In inertial sensors the capacitive signal originating from a sensor element is first converted to signal current, and further to voltage by the interface electronics. As the magnitude of the signal current, especially in gyroscopes, is very small, the front-end of the readout circuit commonly limits the noise performance of the sensor. One means to accomplish a lower noise of the readout is to increase the transconductance of the signal-detecting amplifier. At best the decrease in the noise voltage that is gained is proportional to the square root of the current increase. Another way to improve the resolution is to increase the value of the detection voltage, in which case the effect of the noise decreases linearly with the increasing detection voltage.

Charge pumps provide a way to increase the voltage above the nominal supply. As the sensor inflicts only a capacitive load, the charge pump can be used for increasing the detection voltage, ac or dc, with a moderately small additional chip area. The benefits of charge-pumping become emphasized when control is required over the mechanical element using electrostatic forces and the nominal supply is not high enough to achieve a sufficient control force. In such a case, increasing the available voltage range is the sole alternative if a functional system is to be realized, and it is straightforward to implement using a charge pump.

Depending on the application, the charge pump design can focus on optimizing either efficiency, silicon area, or output ripple separately, or simultaneously. These issues will be discussed in the following sections.

5.1 Operation and Properties of a Charge Pump

The key component in charge pump circuits is the non-linear *charge transfer element*, a switch or a diode, which allows an ac input voltage to be rectified and increased. The operation of a charge pump can be seen by studying the circuit shown in Fig. 5.1, which represents the first stages of a Dickson charge pump [126] with ideal diodes. During the start-up of the pump, in the phase ϕ_1 the capacitor C_1 is charged to V_{DD} through the forward-biased D_1. At the same time the voltage at the cathode of D_2 increases above V_{DD}, creating a reverse bias across the diode. Some charge from C_2 is moved through D_3 to the next pump stage. When ϕ_2 becomes active the voltage at the bottom plate of C_1 is increased by V_{DD}, while the voltage at the cathode of D_1 attempts to rise to $2V_{DD}$. However, if the voltage of C_2 is lower than $2V_{DD}$, D_2 becomes forward-biased

and balances the voltages of C_1 and C_2. In a steady state, with zero load current and parasitic capacitances, no charge transfer occurs, while the voltages across C_1 and C_2 are V_{DD} and $2V_{DD}$, respectively, also indicating the ideal voltage gain per stage in the Dickson charge pump.

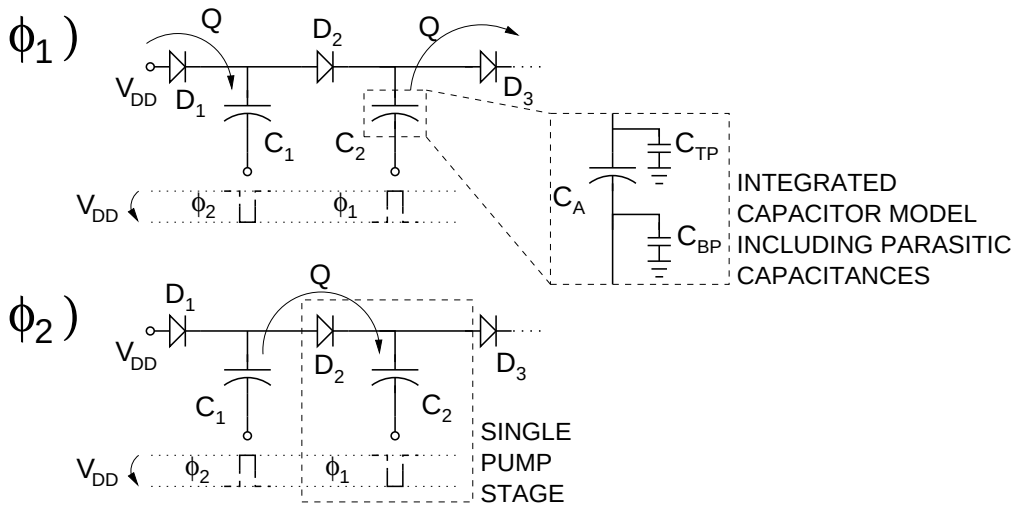

Figure 5.1: The operation of a charge pump through the example of a Dickson charge pump circuit.

For a charge pump which is utilized as a part of the sensor interface circuit, the required load current levels are typically low, in the order of a few tens of μA, because of which the full integration of the pump is feasible. Especially in fully integrated charge pumps several different non-idealities reduce the output voltage and efficiency of the pump. One of the most significant sources of losses is the parasitic capacitance associated with different nodes. In an integrated capacitor the top plate parasitic capacitance C_{TP} is typically considerably smaller than the bottom plate parasitic capacitor C_{BP}, which is formed between the bottom plate and the substrate. This is depicted in the simple cross-sectional view of an integrated capacitor in Fig. 5.2. When the capacitors are driven as in Fig. 5.1, by applying the clock to the bottom plate of the capacitor, the output voltage of the pump V_{HH} is affected by C_{TP}[2] only [126],

$$V_{HH} = V_{DD} - V_D + N\left(\frac{C_A}{C_A + C_{TP}}V_{DD} - V_D\right) - \frac{NI_{HH}}{(C_A + C_{TP})f_{CP}}. \qquad (5.1)$$

Additionally, a non-zero drop V_D across a forward-biased diode reduces the attainable output voltage. In the equation, N denotes the number of stages, I_{HH} the current drawn from the high-voltage output, f_{CP} the clock (pumping) frequency, and C_A the pumping capacitance per one stage (equal for all stages).

[2]In a practical charge pump the charge transfer elements and wirings also contribute to C_{TP}. Here the charge transfer elements are assumed to be free of any parasitic capacitance.

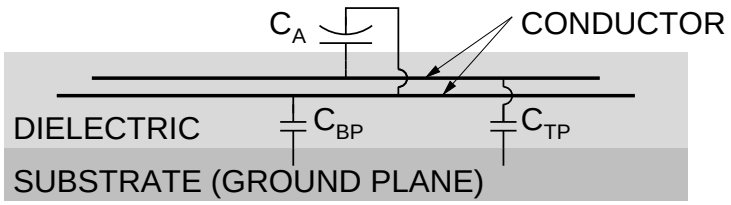

Figure 5.2: A cross-section of an integrated capacitor.

The efficiency, defined as the ratio between the input and output power of the charge pump, is impaired by both C_{TP} and C_{BP}. From the efficiency point of view, how the pump capacitors are connected is of only minor significance. As (5.1) indicates, V_{HH} will decrease if C_{TP} is changed to C_{BT}, but on the other hand the output impedance $N/(C_A + C_{TP})/f_{CP}$ of the charge pump is reduced. If only a low output current is required, the efficiency can be slightly improved when connecting the clock signals to the bottom plates of the capacitors [127]. For a case where the bottom plate is clocked, and C_{TP} and V_D are assumed negligible, the efficiency can be written as [127]

$$\eta = \frac{V_{HH}}{V_{DD}[(N+1) + N f_{CP} C_{BP} V_{DD}/I_{HH}]}. \tag{5.2}$$

For a more accurate prediction of efficiency more non-idealities should be considered [127]. These include the effect of the charge transfer elements, in this case diodes, which will both contribute to C_{TP} and cause a non-zero forward voltage drop V_D, the total power consumed by the clock generator and buffers, and any leakage within the charge pump [128].

A simple example can be provided to describe how the number of stages affects the properties of the pump. Let us assume that the pump is required to supply a current I_{HH} of 30 μA and that the clock frequency is 10 MHz. The higher the frequency, the smaller the pump capacitors required, as can be noticed from (5.1). However, dynamic losses, for example in the clock generation circuitry, can start to dominate at high clock frequencies. The supply voltage for the example case is set to 2.5 V and the diode drop is assumed to be zero. The total amount of capacitance (NC_A), which is solved using (5.1), and the efficiency (5.2) are plotted in Fig. 5.3. The only non-ideality considered is the bottom plate parasitic capacitance, C_{BP}, which, with the thick field oxide as the only available insulator in the capacitors, is assumed to be equal to $0.35C_A$ [129]. The figure indicates that for an integrated charge pump the optimization of both the efficiency and the area, which is usually dominated by the capacitors, calls for a larger number of stages than the lowest number necessary in order to reach the desired output voltage [XII].

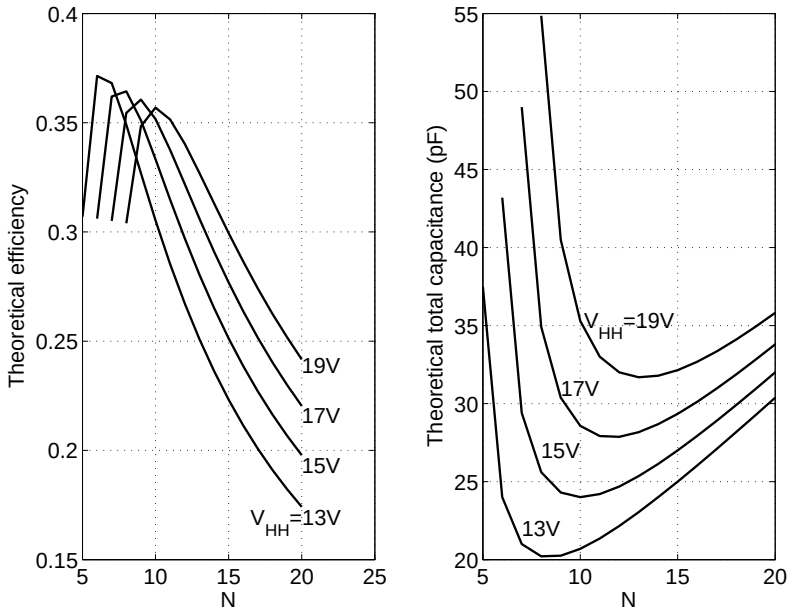

Figure 5.3: The efficiency and total capacitance of an example charge pump. The only non-ideality considered is the bottom plate parasitic capacitance.

5.2 Charge Pump Circuits

A number of different types of charge pumps have been published since the Cockcroft-Walton charge pump was introduced in 1932 [130]. This voltage multiplier was implemented using discrete components with very small parasitic capacitances. The multiplier was not optimal for full integration because of its rapidly increasing output impedance when the number of stages is increased, and also because of a decreasing voltage gain with non-zero parasitic capacitances [126]. A charge pump circuit especially intended for complete integration was first introduced by Dickson in [126], where the charge pump was realized using p-channel MNOS transistors. Two examples of the Dickson charge pump, where the ideal diodes in Fig. 5.1 are replaced using transistors, are shown in Fig. 5.4. In (a) p-channel transistors are used to replace the ideal diodes in order to create a high negative voltage compared to the ground potential. In a similar pump, where n-channel devices are utilized, as shown in Fig. 5.4 (b), the high voltage produced is positive compared to the ground potential.

Since the publishing of the Dickson charge pump, improved charge pump circuits have been developed to meet the demands of modern semiconductor technologies. The clear problem when connecting the bulk of the diode-connected transistors which function as charge transfer elements to the ground is the body effect [133]. As the number of stages increases, the source-bulk voltage and, consequently, the threshold voltage, also increases. This reduces the pump output voltage; the larger the threshold compared to the supply voltage, the more significant the effect. In order to reduce the effect of threshold

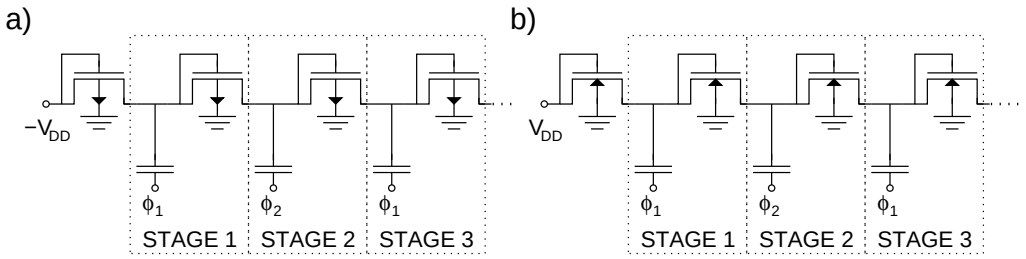

Figure 5.4: a) Three stages of the Dickson [126] charge pump for generating a high negative voltage using PMOS transistors, and b) the same circuit with NMOS transistors for producing a positive high voltage.

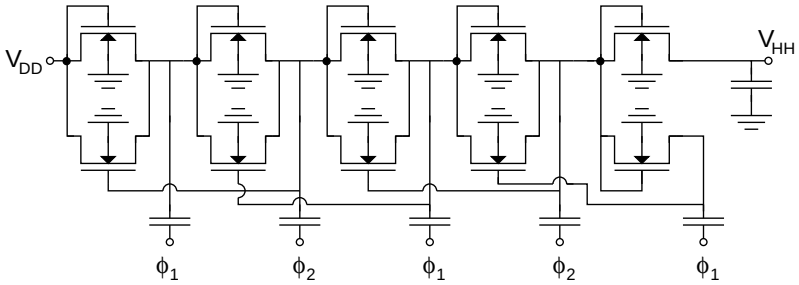

Figure 5.5: A charge pump circuit introduced in [131].

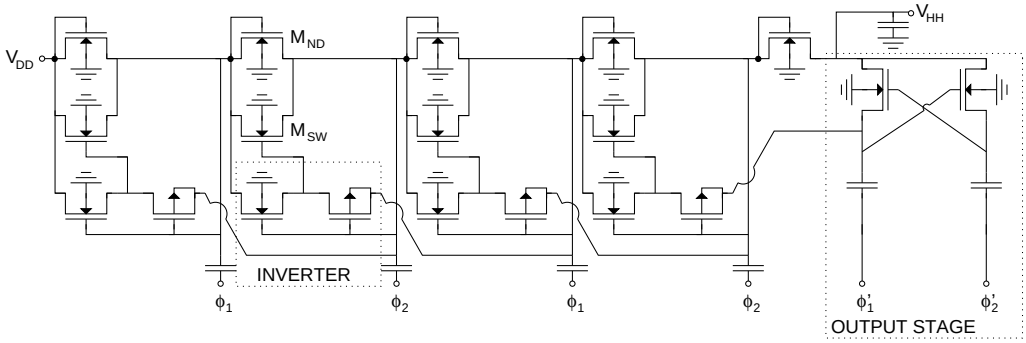

Figure 5.6: A charge pump circuit presented in [132].

voltage, the charge pump shown in Fig. 5.5 [131] was introduced. Here, the charge transfer element is a combination of a diode-connected transistor in parallel with a switch transistor. Although the additional transistor considerably reduces the required input voltage and clock swing, reverse currents can degrade the efficiency, because the charge transfer elements cannot be fully turned off during reverse bias operation. Further progress in enhancing the Dickson charge pump finally led to the implementation shown in Fig. 5.6 [132]. In this circuit the additional switch transistors can be effectively turned off with the help of the floating inverters, while the bootstrapped output stage enables the last stage of the pump to be operated properly. A similar functionality, i.e. a smaller voltage drop in the charge transfer elements, can also be achieved using auxiliary capacitors and a four-phase clock scheme to provide improved switch control signals. Examples of this approach are given in [127, 134, 135, 136].

When the required pump output voltage is too high to meet the voltage tolerance requirements of the pump charge transfer elements, floating PMOS transistors, or, if a triple-well technology is accessible, floating NMOS transistors can be used[3]. In this case the well-to-substrate voltage tolerance must be higher than the desired output voltage. Further, the n-wells can be biased to a local maximum voltage, and the p-wells to a local minimum voltage, as described for example in [137], in order to reduce the body effect.

The use of actual diodes as charge transfer elements provides an additional simple method to eliminate the body effect. For example, the SOI (silicon-on-insulator) technology offers a means to implement diodes which, compared to bulk CMOS, have fewer parasitic devices, which can reduce the efficiency of the pump or even prevent the proper functionality of it [138, 139].

Voltage doublers can also be used to generate a high dc voltage. An ideal voltage doubler for creating a V_{out} equal to $2V_{in}$ is shown in Fig. 5.7. In the phase ϕ_1 the capacitor is charged to the input voltage V_{in}. In the next phase the capacitor node at the lower potential is connected to V_{in}, and simultaneously the capacitor node with a positive charge rises to the voltage V_{out}. In theory, when cascaded, doublers can offer a voltage gain equal to 2^N, where N is the number of stages, hence offering a very area efficient way to generate a high-voltage dc. The example implementation given in [140] is redrawn in Fig. 5.8. This circuit generates equal positive V_+ and negative V_- high-voltage outputs with a maximum magnitude of $2V_{DD}$. In practice, using several doublers to generate a high dc voltage sets stringent requirements for the oxide voltage tolerance in the switch transistors. This is because the switch control signals, at least for the last stage, need to have a swing equal to the high-voltage output in order to fully open or close the switches.

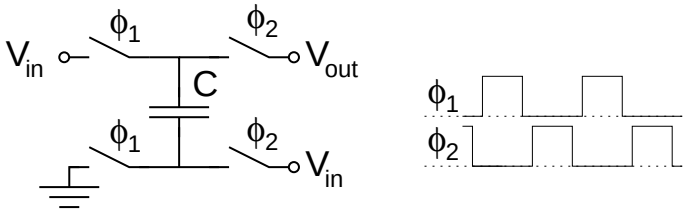

Figure 5.7: An ideal voltage doubler.

Even the traditional Dickson charge pump circuit can suffer from increased oxide voltage stress, which is because the reverse bias voltage can be as high as twice the clock swing. The reason behind the increased voltage stress can be depicted using the ideal Dickson charge pump shown in Fig. 5.1. In a steady state, if the voltage lost from a pump capacitor during the charge transfer is minimal, in ϕ_2 the voltage across the diode D_2 is zero, and the voltages across the pump capacitors C_2 and C_1 are equal to $2V_{DD}$, and V_{DD}, respectively. When arriving at the phase ϕ_1, the capacitor voltage at the cathode of D_2 is increased by V_{DD}, while the voltage at the anode is reduced by the same amount. Hence, the reverse

[3]p-type substrate assumed

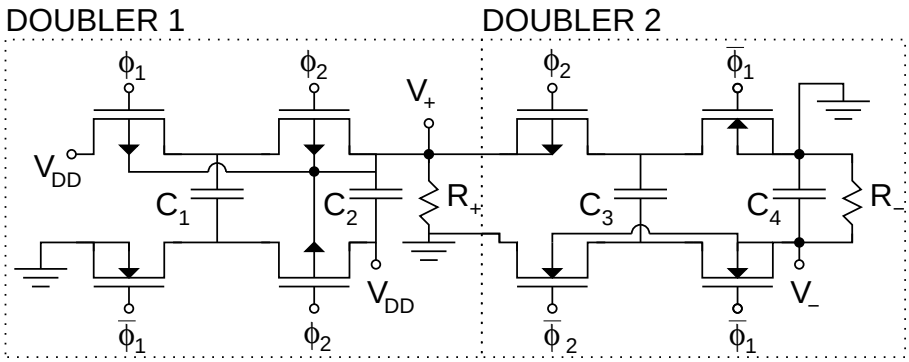

Figure 5.8: A doubler charge pump redrawn from [140].

bias becomes equal to $2V_{DD}$. This can prevent the use of standard floating low-voltage MOSFET transistors as charge transfer elements in a Dickson charge pump.

Lower requirements for the voltage stress tolerance can be achieved using the charge pump shown in Fig. 5.9, which in some cases is also called a doubler or a cross-coupled doubler, and can even be used as one [141]. In this circuit the clock swing determines both the voltage tolerance required from the switch transistors and the gain of a single pump stage shown in Fig. 5.9. If the clock swing is assumed to be equal to the input voltage and the same for all the stages, the gain of a pump using the cascaded doubler units shown in Fig. 5.9 is equal to $N + 1$, the same as for the Dickson charge pump with ideal charge transfer elements. Hence, this topology is suitable for low-voltage floating transistors, which can allow the efficiency of the pump to be improved, being smaller devices with consequent smaller parasitics. A circuit similar to Fig. 5.9 is used, for example, in [142, 143]. Examples of different well-biasing techniques for reducing the effect of parasitic devices are introduced in [129], and other variations of the circuit in Fig. 5.9 are presented in [144, 145].

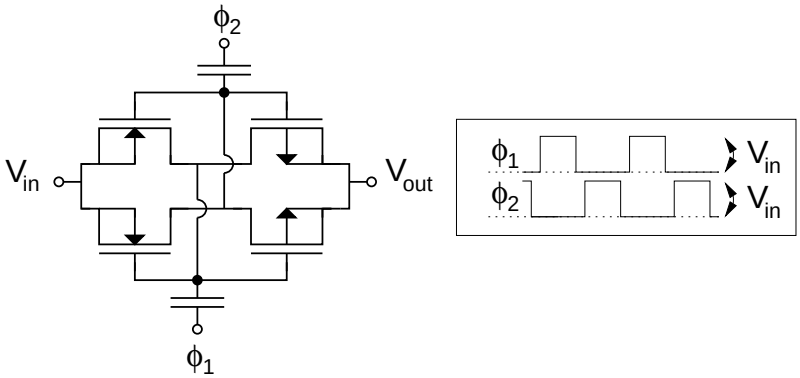

Figure 5.9: A floating charge pump unit for increasing the voltage by an amount equal to the clock swing.

5.3 Inertial Sensors and High-Voltage Signal Generation

When the charge pump is being designed, the focus in optimization can be set on the minimization of the losses, or the chip area, or the ripple of the pump output voltage. For a fully integrated charge pump the efficiency is likely not to be optimal [129] because of the significant parasitic content of the integrated capacitors. On the other hand, the chip area and output ripple are both inversely proportional to the clock frequency of the pump. Hence, when the chip area is being optimized, which is a significant cost issue in an integrated circuit, the output ripple is also reduced. As the capacitive load of a sensor element typically requires only low output current levels for capacitive detection or actuation, the implementation of a very compact charge pump becomes possible. When the total supply current of the pump forms only a fraction of the supply current of the sensor interface, the implementation of a fully integrated charge pump also becomes feasible as a result of the reduced importance of the less-than-optimal efficiency.

5.3.1 Closed-Loop Charge Pumps and High-Voltage Signals with Wide Voltage Range

An important matter when creating high-voltage signals is not to compromise the lifetime of the components. This implies the limitation of the voltage across the capacitors and any active device below the maximum tolerated value. Furthermore, it is not feasible to allow the output voltage to increase unnecessarily with the input voltage, which will potentially vary significantly, depending on, for example, the voltage of a battery that supplies the chip. In an on-chip charge pump the process variation in pump capacitors, clock source, or charge transfer elements can lead to additional severe output variation. The variation can be limited using a suitable regulation method.

A typical regulation method for a charge pump is shown in Fig. 5.10. The output voltage of the pump V_{HH} is divided, according to the two impedances Z_1 and Z_2, to make possible the use of a low-voltage reference V_{ref}. The division can be performed using either capacitors with reset switches or resistors, or, if the phase shift in the resistive divider becomes problematic, both resistors and capacitors. During start-up the divided value of V_{HH} remains below V_{ref}, which makes the comparator output stay high. Now that the clock Clk is fed to the charge pump, V_{HH} increases until the comparator reaches the trip point and the clock is blocked from entering the pump. In steady-state operation the average output voltage stays at the value defined as $V_{ref}(Z_1 + Z_2)/Z_2$. However, any delay in the sensing path will cause the voltage to oscillate around the average output value [134]. The frequency of this oscillation will decrease with increasing load capacitance and decreasing load current [146], which can be problematic as the low-frequency spurious components, especially for sensor applications, should be minimal.

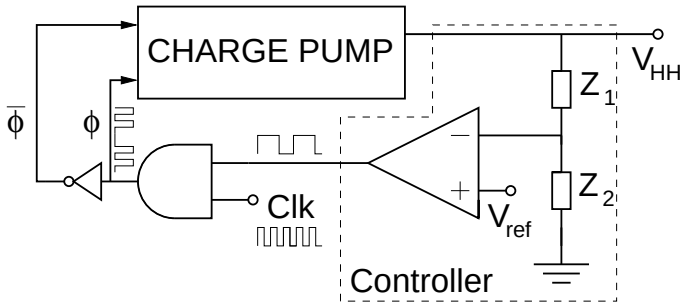

Figure 5.10: Typical configuration for regulating the charge pump output voltage.

Several different types of control methods have been published. The traditional topology in Fig. 5.10 with resistive Z_1 and Z_2, is used, for example, in [147], whereas in [140] similar operation is achieved by replacing the voltage divider and the comparator by a voltage-sensitive level shifter for the clock. The same controller structure is also utilized for a current-mode charge pump in [148]. Reducing the ripple at the charge pump output by adding a capacitive path from V_{HH} to the comparator input is proposed in [134]. The ripple can also be transformed into pseudo-random noise by applying a delta-sigma modulator to control the gain of the pump. In this way the regulation-inflicted discrete tones can be removed from the charge pump output. This approach is reported in [149]. In [150], another different approach to the regulation is presented. Here the focus of the implementation of the pseudo-continuous regulation scheme is on maximizing the efficiency and minimizing the ripple of the single doubler stage. This is made possible by using a very fast control loop, which can respond to a droop in the output voltage within the clock cycle by continuously controlling the output current of the pump.

The charge pump dc output voltage always depends on the clock frequency when a finite load current is present. However, common charge pumps do not allow bidirectional charge-pumping. Hence, attempting to create a clean high-voltage signal with a wide voltage range directly using a frequency-regulated charge pump can turn out to be very impractical. This is because at low voltages the required clock frequency would be very low, resulting in heavily increased ripple at the pump output. Additionally, only the rate of increase of the output voltage is defined by the pump, whereas the speed of the voltage decrease will depend on the load current. The related variation of the large signal dynamic properties would most probably be a major impediment to designing a charge pump able to meet all the dynamic requirements.

A solution for increasing the continuous attainable high-voltage range is provided in [143], which reports a charge pump design, which can pump the voltage to both directions. The pump consists of stages, shown in Fig. 5.11, which allow the voltage to be either increased or decreased in a controlled fashion. In [VIII] and [XII] the continuous high signal range is attained using separate two-stage high-voltage operational amplifiers to generate the desired high-voltage output. Now the charge pumps are used simply to supply the amplifiers. In this way the noise, dynamic properties, and the accuracy of the

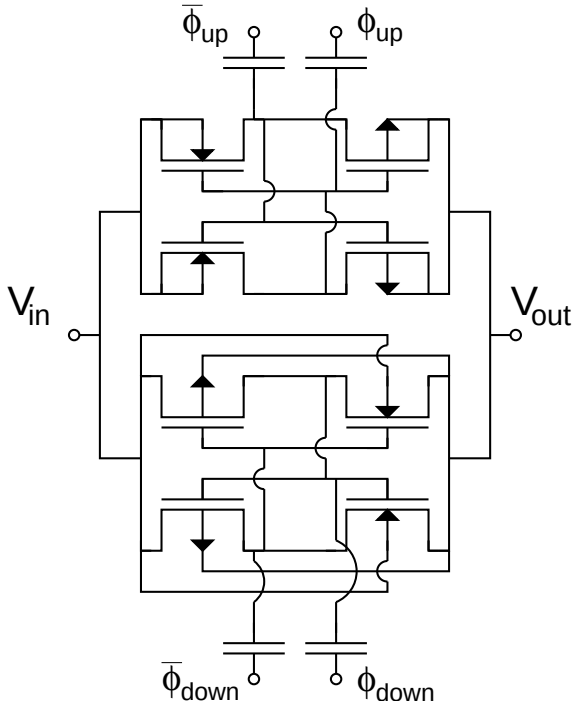

Figure 5.11: A single charge pump stage, redrawn from [143], for pumping the voltage either up or down.

amplifier output can be set very accurately and deterministically. Unfortunately, large resistors are required to implement the feedback in the amplifiers. The resistors partially determine the bias current of the operational amplifier, which further sets the load current of the charge pump. These resistors also define the noise level of the closed-loop amplifier. Hence, although the noise of the operational amplifier could be reduced by using single-stage amplifiers in [VIII] and [XII] with a folded high-voltage output stage, the total noise will not necessarily improve. Two-stage amplifiers with a high-voltage second stage and a loop gain in excess of 100 dB become the most feasible alternative for the precise scaling of low-voltage input signals.

Now that the high dc PSRR (power supply rejection ratio) of the high-voltage amplifiers provides the precision dc regulation, the charge pump output should be regulated only to meet the voltage tolerance requirements and to improve the efficiency of the charge pump. The continuous control of the frequency enables a very simple output voltage control method to be used and makes possible the efficient filtering of the output voltage. A charge pump with a proportional controller for continuous frequency control is presented in [VIII]. Another version of this regulation method is presented in [151], where the feedback, which is achieved by controlling the drive capability of the charge pump clock, is completed using frequency control.

High voltages can be problematic, even for logic signals, if, for example, the gate oxide

cannot tolerate the full voltage swing. In [XIII] the charge pump is applied for the high-voltage excitation of the drive resonator in a gyroscope. Here a high-amplitude square wave signal is created by periodically shorting the charge pump output to ground, when the actual pump is disabled and the resetting does not consume dc power. In this way high-voltage signals do not have to be applied to the gate electrodes of the switches.

5.3.2 Reduction of Ripple and Area

The actual tolerance of the charge pump output ripple depends on how the ripple can couple to the system output. Fully continuous-time systems are fairly insensitive to the out-of-band spurious frequency components, especially when the circuit contains no frequency conversions. This, however, is rarely the case. Traditionally SC-circuits, multipliers, or comparators, which are prone to folding, must be used in at least some parts of the sensor interface. Even if all the paths to the critical circuitry were filtered properly, the high-frequency ripple can cross-couple on-chip. As it is complicated to accurately predict how much supply ripple is tolerated, it becomes feasible to simply minimize it.

The analysis presented in [VIII] of the dynamic properties of the frequency-controlled charge pump indicate that the closed-loop stability increases with the load capacitance. This indicated that the ripple can be reduced to any desired level by increasing the load capacitance without changing the steady-state clock frequency. Limiting the ripple is important in order not to compromise the purity of the final high-voltage output. This is because the PSRR of the high-voltage amplifiers can be low at the clock frequency.

If the filtering of the charge pump output ripple is required to be done on-chip, the amount of filtering capacitance that is required should be minimized. The evaluation of the magnitude of the ripple can be performed using the circuit in Fig. 5.12, which models the last stage of an ideal Dickson charge pump, the filtering capacitance C_F, and the potentially required additional filter components R_F and C_{F2}. When the update rate of the charge pump output voltage is determined by the clock frequency f_{CP} of the pump, the voltage of the filtering capacitance appears as in Fig. 5.13. In the figure, the sawtooth wave is assumed to result from the instantaneous updating of the charge at the rising edge of ϕ. With C_F as the only filtering component, the peak-to-peak amplitude of the ripple V_{ppr} is given as

$$V_{ppr} \approx \frac{I_{HH}}{f_{CP}C_F}, \tag{5.3}$$

where I_{HH} is the magnitude of the load current drawn from the pump output. The ripple voltage is dominated by the fundamental component of the sawtooth wave (dashed line), the amplitude of which, V_{afr}, can be written as

$$V_{afr} = \frac{I_{HH}}{\pi f_{CP}C_F}. \tag{5.4}$$

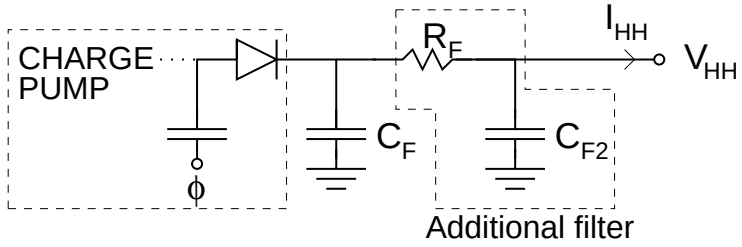

Figure 5.12: A simplified circuit for the modeling of the charge pump output ripple voltage.

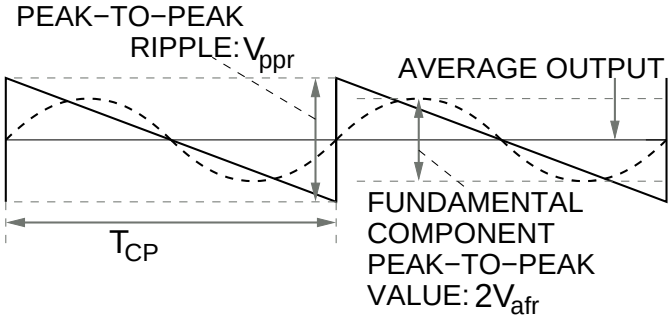

Figure 5.13: charge pump output waveform (solid) when ideal charge transfer is assumed. The dashed line represents the fundamental frequency component of the sawtooth wave. The period of the ripple T_{CP} is determined as an inverse of the clock frequency f_{CP} of the clock signal ϕ.

In order to attain minimun ripple without affecting the output impedance, the clock frequency should be maximized and the pump capacitors minimized. However, the determination of the optimum frequency using a theoretical approach is troublesome, as the frequency also affects the efficiency of the pump and the optimal operating point varies as a result of processing uncertainties and with temperature. Hence, selecting the frequency can be done with the help of simulations.

If mere C_F is not enough to provide sufficient attenuation of the ripple, an additional RC filter (R_F and C_{F2}) can be used at the expense of lower high-voltage output. In this case the value for R_F is determined by the maximum voltage drop allowed across the resistor. Provided that $R_F \gg 1/(2\pi f_{CP} C_F)$, and that $f_{CP} \gg 1/(2\pi C_{F2} R_F)$, the fundamental component amplitude at the filter output can be approximated as

$$V_{afr} \approx \frac{2I_{HH}}{(2\pi f_{CP})^2 C_F C_{F2} R_F}. \tag{5.5}$$

When the chip area limits the available filtering capacitance to $C = C_F + C_{F2}$, the optimal filtering result is obtained when $C_{F2} = C_F = C/2$.

Exactly in the same way as the minimization of the pump output ripple, the optimization of the chip area of a charge pump also requires maximum clock frequency. But the total

amount of capacitance can be further optimized (minimized) as was seen in Fig. 5.3. By minimizing the capacitance, which dominates the area, the losses resulting from the bottom plate parasitics are also minimized and the efficiency improved. The minimization of the total capacitance of a Dickson charge pump has been analyzed in [147] and [152], while [XII] introduces the optimization for a modified Dickson charge pump. Here the pump is split into two sections, which allows advantage to be taken of the higher density of the low-voltage capacitors and the area to be reduced further.

5.4 Discussion

Charge pumps allow the generation of a local high-voltage source. In capacitive sensors voltages higher than the nominal supply can predominantly be used to increase the detection voltage and electrostatic actuation force. When the load is capacitive, as in the case of capacitive sensors, and no rapid voltage transients need to be created by the pump, the load current remains small and no off-chip components are necessary. Fully integrated charge pumps can be created with the focus on minimizing the chip area and the output ripple, both properties that are important for precision and low-cost capacitive sensors.

The charge pumps implemented in [VIII], [XII], and [XIII] all utilize diodes as charge transfer elements. The diode-connected floating bipolar transistors are simple and have low parasitic capacitance and a constant voltage drop, and are therefore good alternatives for the realization of area-optimized charge pumps. The efficiency, however, can be further improved, as is done in [13] for the pump in [VIII] using, for example, the voltage doubler stages in Fig. 5.9, where the voltage drop is zero in an ideal case. In [VIII] and [XII] the greatest emphasis, in addition to area optimization, is put on the development of efficient voltage-limiting techniques in order to create a nearly ripple-free and constant high voltage. Hard limiting in [XII] is an effective and precise but power-consuming method for setting the desired pump output, whereas the continuous frequency regulation presented in [VIII] even allows good efficiency to be maintained. It should, however, be taken into account that the efficiency in [VIII] of 0.18 and about 0.24 with improved pump design in [13] is rather limited, which is typical in low-power fully integrated charge pumps and a result of high bottom plate parasitics and dynamic losses resulting from the high-frequency operation. The rms ac voltage of 0.8 mV at the charge pump output in [VIII], on the other hand, implies that the ripple and the noise reduction are effective. In [XIII] the charge pump with a rise time of a few tens of microseconds was directly used to generate a 40-V differential excitation signal for the drive loop of a gyroscope. Unlike the other two pumps, this one shows that a charge pump can well be used to directly generate rail-to-rail high-voltage ac signals, while at the same time limiting the voltage stress of the gate oxide. All the charge pumps that were implemented have been successfully used as part of the interface electronics and demonstrate the feasibility of on-chip high-voltage generation in capacitive sensors.

6 Summary of Publications

In this section a brief overview of the publications is given.

[I] High-resolution continuous-time interface for micromachined capacitive accelerometer

In this paper the design and analysis of the continuous-time accelerometer interface for a capacitive sensor element are presented. The interface design is focused on attaining resolutions up to 120 dB, together with a signal bandwidth of 300 Hz. The circuit structures for which the design will be presented include a charge-sensitive amplifier-based readout, demodulator, low-pass filter, and the controller. Details of the design of the GmC oscillator can be found in [153]. Important sources of instabilities in the continuous-time system, where common electrodes are used for readout and actuation, are presented, and the theoretical basis for the calibration of linearity is introduced. The accelerometer is measured to achieve a minimum noise floor of 500 $\mathrm{ng}/\sqrt{\mathrm{Hz}}$.

[II] Continuous-time interface for a micromachined capacitive accelerometer with NEA of 4 μg and bandwidth of 300 Hz

An upgraded version of the accelerometer in [I] is presented in this paper. Several modifications are made in order to reduce the noise and the supply current of the interface. Completely new blocks included in the system are the digitizer [III] and the high-voltage controller [IV]. The interface is measured to attain a noise-equivalent acceleration (NEA) density of 500 $\mathrm{ng}/\sqrt{\mathrm{Hz}}$ at 30 Hz for the on-chip digitized output and 300 $\mathrm{ng}/\sqrt{\mathrm{Hz}}$ at 30 Hz for the analog output using a capacitive half-bridge sensor element with a single pair of electrodes. The different sources of noise in the sensor are analyzed in detail.

[III] High resolution analog-to-digital converter for low-frequency high-voltage signals

In this paper, the design and measurements of a high-resolution analog-to-digital converter (ADC) are presented. The $\Sigma\Delta$-ADC that was implemented is combined with a low-noise buffer which enables a single-ended input signal with a maximum value of twice the nominal supply to be used. The system that was designed was measured to

achieve an input-referred noise voltage density of 220 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and a bandwidth up to 1 kHz.

[IV] Integrated high-voltage PID controller

An integrated PID controller is presented in this paper. Only two operational amplifiers are used for the controller in order to minimize the power consumption and area, but also to enable two complex zeros to be realized. The amplifier that was designed tolerates a supply voltage of 12 V. Measured transfer functions of the controller are presented.

[V] An interface for a 300°/s capacitive 2-axis micro-gyroscope with pseudo-CT readout

In this paper the design of an interface for a capacitive 2-axis micro-gyroscope, implemented in a 0.35-$\mu\mathrm{m}$ high-voltage CMOS with an active area of 2.5 mm^2, is presented. The sensor start-up time is 0.4 s and the x- and y-axis noise floors are 0.015 $^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$ and 0.041 $^\circ/\mathrm{s}/\sqrt{\mathrm{Hz}}$. The supply current for the on-chip charge pump and drive and sense interfaces is 1.8 mA. Area reduction is made possible by the proposed pseudo-continuous-time (CT) readout technique, without the noise performance of the readout being compromised. More detailed discussion of the sense readout, drive loop, high-voltage circuits, and PLL is presented in [VI], [VII], [VIII] and [IX], respectively.

[VI] Pseudo-continuous-time readout circuit for a 300°/s capacitive 2-axis micro-gyroscope

In this paper the pseudo-continuous-time readout circuit utilized for the readout of a capacitive micro-gyroscope is presented in detail. Compared to a regular continuous-time interface with large on-chip RC time constants, the reduction of the chip area is made possible by the technique that is proposed, which allows a dc biasing voltage to be used for the detection and requires no large RC time constants to be implemented. The supply current of a sense readout channel is approximately 0.4 mA, and the dominant noise sources are identified as the middle-electrode biasing voltage, front-end, and the quadrature nulling voltage.

[VII] An analog drive loop for a capacitive MEMS gyroscope

The linear model and the design of an analog drive loop for the drive (primary) resonator in a capacitive gyroscope are presented in this paper. Four different types of gain control topologies are compared and analyzed with both P- and PI-type controllers, and clock generation using a phase-locked loop and the drive loop signal as the reference is discussed in the paper. A proportional amplitude controller, together with the rest of the drive loop, is implemented using a high-voltage 0.35-μm CMOS technology and a nominal supply of 3 V. The loop that is implemented allows the start-up of the drive resonator in less than 0.4 s.

[VIII] On-chip charge pump with continuous frequency regulation for precision high-voltage generation

A fully integrated charge pump, which utilizes continuous frequency control for the closed-loop operation, is presented in this paper. This means of control allows the charge pump clock to settle to the correct frequency according to the current load while maintaining the 50-% duty ratio of the clock. The final high-voltage signal is generated by using a closed-loop amplifier, for which the pump creates the supply, and which then amplifies the desired low-voltage signal to the correct level. The pump that was implemented with the regulator has an active chip area of 0.14 mm^2 and creates a nominal output of 10 V with a 29-μA load current and 2.5-V minimum supply.

[IX] Integrated charge-pump PLL with SC-loop filter for capacitive microsensor readout

In this paper, simulated and measured phase noise characteristics for a charge pump PLL with a switched-capacitor loop filter are presented. The PLL is fabricated using a 0.35-μm high-voltage CMOS technology. The PLL is designed for a reference frequency range from 3 kHz to 10 kHz, for a divider value of 32, and to operate with a supply voltage ranging from 2.5 to 3.6 V. The supply current of the PLL, excluding the external references, is 7.3 μA. The gyroscope in [V] and [VI] was measured using the RC loop filter in the PLL. Compared with the SC filter, the RC filter allowed a larger locking range without the phase noise impairment resulting from cross-coupling.

[X] Design of clock generating fully integrated PLL using low frequency reference signal

This paper describes a design procedure for a fully integrated charge pump PLL, which can utilize low reference frequencies. Noise is taken into account in the design process and a simulated example of a PLL is presented. The theory presented here allows a fully integrated PLL to be design with either noise or power consumption being favored. The measured results for a PLL similar to the one presented in this paper are given in Section 4.3.

[XI] Noise analysis of comparator performed sine-to-square conversion

This paper describes a theoretical analysis of sine-to-square conversion when noise is included in the conversion process. The analysis is done for conversion that is performed by a comparator. As a result of the analysis, a simple method for calculating the spectrum of the clock resulting from the noisy conversion process is obtained. To support the theory derived here, simulation results will be presented. The measured results and a comparison to the theory are given in Section 4.3. These result indicate that noisy sine-to-square conversion impairs the phase noise of the PLL by as much as 40 dB.

[XII] On-chip digitally tunable high voltage generator for electrostatic control of micromechanical devices

This paper presents circuit structures for on-chip high voltage generation in order to allow digital electrostatic control. The required load current levels for this application are basically due to transients only and are thus very small. A high-voltage amplifier with digitally controllable output, i.e. a high-voltage DAC, is implemented and, as an example application, the DAC is used for quadrature compensation in a microelectromechanical gyroscope in [58]. The high-voltage generator that was implemented achieves output voltages between zero and 27 V in 29 mV steps with a supply current of less than 3 mA.

[XIII] Fully integrated charge pump for high voltage excitation of a bulk micromachined gyroscope

This paper describes a fully integrated charge pump for the electrostatic excitation of a gyroscope in [58]. The high-voltage drive signal that is attained makes possible the

quick start-up of the drive resonator. The charge pump circuit converts the low-voltage signal at the resonant frequency to a 40-V (peak-to-peak) differential square wave. The functionality is verified by forming a positive feedback loop and measuring the start-up time of a bulk micromechanical gyroscope. The measured charge pump is implemented in a 0.7-$\mu\mathrm{m}$ high-voltage CMOS with a chip area of 0.46 mm^2 and draws 0.9 mA from a 5-V supply.

7 Conclusions and Future Work

The development of the MEMS technology has made it increasingly possible for sensor applications to emerge. Masses of accelerometers and gyroscopes are applied in consumer electronics, for devices such as game controllers, digital cameras, and mobile phones, which necessitate both low cost and minimal size per sensor unit. As the whole field of applications for inertial sensors varies from inertial navigation, where typically the highest performance is required, to the detection of orientation, for which a more modest performance is sufficient, it is clear that the design of the electronics is also dependent on the end application. This is especially relevant as the electronics are the only power-consuming section in a capacitive sensor. In order for the system or electronics designer to reach a more optimal interface and complete sensor, a broad knowledge of the technologies and techniques that are available is beneficial. In this thesis several alternative topologies and circuits for sensor readout are introduced in order to give an impression of how it is possible to detect the information in a capacitive sensor. Important auxiliary circuits are also discussed. The implementation examples show that, for example, a realization of a fully integrated PLL is straightforward and power-efficient. Similarly, compact and low-power charge pumps can be realized completely on-chip in order to generate sufficient electrostatic forces.

Although the electromechanical $\Delta\Sigma$-loops have reduced the difference, one of the most important design issues is still whether the mechanical element should be operated in a closed loop or open loop. The latter is practically always simpler to realize, and allows the significant noise sources to be identified more easily, but on the other hand it lacks the several additional degrees of freedom available for closed-loop systems. The sensors that were implemented, the closed-loop accelerometer and the gyroscope, provide examples of the two different design foci. The accelerometer was designed with the clear aim of maximizing the resolution and dynamic range, and the implementation enabled accelerations well below one micro-g to be detected. On the other hand, the design focus for the gyroscope was not just on the resolution, but also the chip area and current consumption. The design led to the realization of a new readout topology, which resulted in a simple open-loop interface with a good performance. Hence, even though a single-axis accelerometer should be a considerably simpler device compared to a complete gyroscope system, the complexity of the closed-loop accelerometer clearly approaches that of the gyroscope.

When considering the accelerometer that was implemented, with the readout and actuation separated in the frequency domain, the stability is mostly compromised as a result of the spurious resonance modes of the element. The accelerometer was measured to achieve noise-equivalent acceleration of 4 $\mu\mathrm{g}$ at a signal band of 300 Hz. The main challenges left for further research include the linearity, dc offset, and on-chip generated biases. The methods of calibration for linearity were demonstrated to function properly. However,

it is most probably not enough to calibrate the linearity at one temperature only, as the parasitics that inflict the non-linearity change with temperature. In order for the linearity to be calibrated continuously, a method should be found to detect and balance the differential electrostatic transducer so that the operation of the accelerometer is not affected. In some applications the dc offset, measured to be equal to 0.2 $\mathrm{mg}/^{\circ}\mathrm{C}$, is also an important parameter, and it is also affected by non-linearity and calibration. The last significant issue outside the scope of this thesis, the references, is an important part of the system and can become a significant source of noise if improperly designed. Although the references can be realized on-chip, the filtering of the references for sufficent noise performance will most probably require external capacitors in order to maintain the high noise performance of the accelerometer.

The interface that was implemented for the micro-gyroscope using pseudo-CT sense readout was demonstrated to achieve a spot noise of 0.015 $^{\circ}/\mathrm{s}/\sqrt{\mathrm{Hz}}$, or an equivalent noise capacitance of about 0.2 $\mathrm{aF}/\sqrt{\mathrm{Hz}}$, with very compact realization. The recently published results in [13] indicate that the whole interface, with integrated references, bonding pads, and calibration memory, fits within 4.3 mm^2 in the 0.35-μm technology and has a supply current of 2.2 mA. The sensor element and the ASIC are still separately packaged in [13], which increases unwanted cross-coupling considerably. It is expected that as a result of bonding the two chips directly together the performance of the sensor will be improved in the future.

It is a clear fact that the design of microelectronics for interfacing micromechanical sensors, not to mention microelectronics in general, is an extensively researched topic. Yet the research in the field is still actively continuing. This is mostly thanks to the very broad scale of the different electronics needed for sensors, ranging from sensor front-ends to PLLs and high-voltage circuits. Each of the sub-blocks of the sensor interface can be optimized not just separately but also together, and hence, improving and developing the interface electronics is to continue. The research is further driven by the fact that new types of sensors and applications of sensors are appearing continuously and are also changing the design focus of the electronics. Digital electronics, an area that is basically completely outside the scope of this thesis, continues to serve up new possibilities for reducing the chip area and current consumption and for improving the tolerance to variations. Furthermore, algorithms and intelligence can be embedded into the digital part of the interface in order to improve the sensors and widen the range of potential applications.

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Appendix A

Simulation of the EM-$\Delta\Sigma$ modulator

A top-level Simulink model of the modulator is shown in Fig. A.1. The model consists of the continuous-time transfer function of the resonator and a discrete-time model of the electronic interface. The resonator model is the same for both the second- and the fourth-order modulators. The parameters of the model do not relate to any practical system but instead are simplified for example purposes. The electronic interface for the second-order EM-$\Delta\Sigma$ modulator is shown in Fig. A.2 and that for the fourth-order EM-$\Delta\Sigma$ modulator in Fig. A.3. An additional simulation result is shown in Fig. A.4 to demonstrate how the use of out-of-band sine relates to the actual noise. In the figure the two simulations that were run for the second-order modulator are exactly the same, with the exception that in the case of noise the out-of-band sine is replaced by a white noise source with the same power as the sine. It can be seen that in both cases the level of the in-band noise floor is roughly the same.

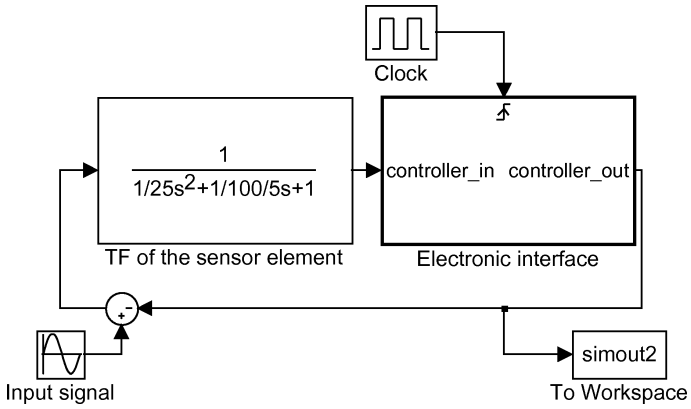

Figure A.1: Top level Simulink model of the simulated EM-$\Delta\Sigma$ modulators.

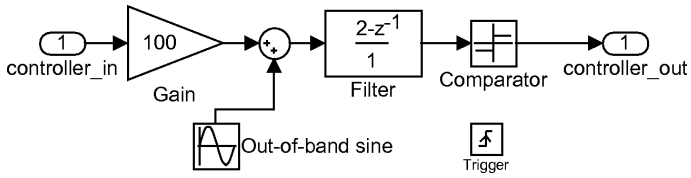

Figure A.2: Electronic interface of the second-order EM-$\Delta\Sigma$ modulator.

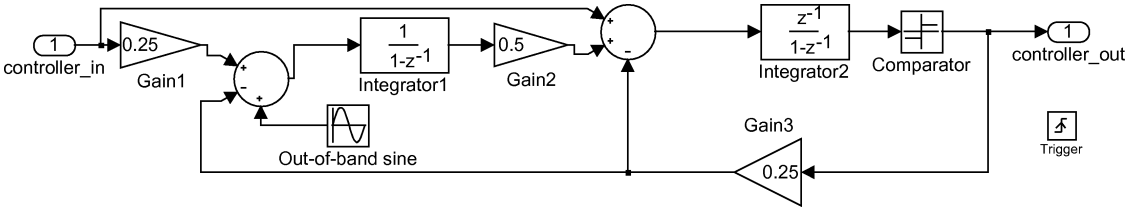

Figure A.3: Electronic interface of the fourth-order EM-$\Delta\Sigma$ modulator.

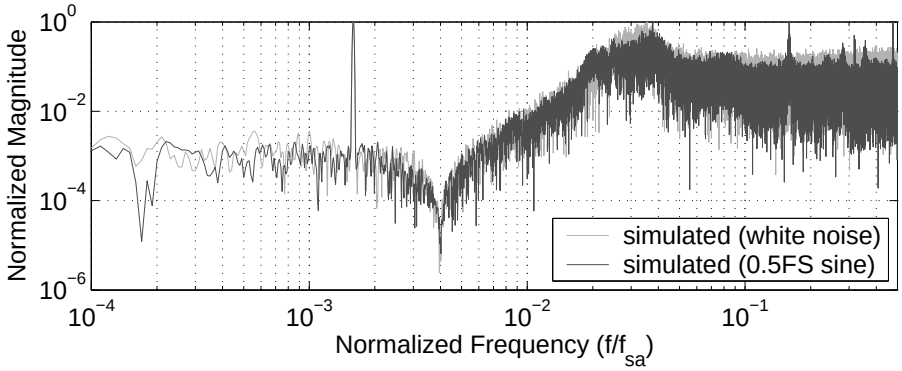

Figure A.4: Comparison of the effect of high-frequency sine and white noise in the second-order EM-$\Delta\Sigma$ modulator. In both simulations the 0.1FS input signal is at frequency 0.0016.

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