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CRYOGENIC DEEP REACTIVE ION ETCHING OF SILICON MICRO AND NANOSTRUCTURES

Doctoral Dissertation

Lauri Sainiemi

Helsinki University of Technology
Faculty of Electronics, Communications and Automation
Department of Micro and Nanosciences

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Doctoral Dissertation

Lauri Sainiemi

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Faculty of Electronics, Communications and Automation
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Abstract

This thesis focuses on cryogenic deep reactive ion etching (DRIE) and presents how it can be applied to the fabrication of silicon micro- and nanostructures that have applications in microfluidics and micromechanics. The cryogenic DRIE process relies on inductively coupled SF_6/O_2 plasma at temperatures below -100 °C. Low etching temperatures can cause some photoresist materials to crack, but Al_2O_3 has been shown to be a very well-suited masking material for cryogenic etching. The anisotropy of the etching process is enhanced by a thin passivation layer on sidewalls that prevents lateral etching. The main parameters that are used to adjust the thickness of the passivation layer are the process temperature and the O_2 flow. Under adequate conditions vertical sidewalls are obtained, whereas passivation layers that are too thin result in negatively tapered sidewall slopes. Under conditions where a passivation layer is not formed, at higher temperatures and/or without oxygen flow, the etching profiles are isotropic. On the other hand, too high oxygen flow results in over passivation. Under conditions where the sidewall is slightly over passivated, its slopes are positively tapered, while more pronounced over passivation results in the formation of black silicon (or silicon nanograss, silicon nanoturf or columnar microstructures).

Typically, vertical sidewall profiles are desirable. However, this thesis shall also demonstrate the usefulness of under and over passivation regimes. Here, highly anisotropic etching conditions are utilized to create trenches with vertical sidewalls, fluidic channels with regular micropillar arrays, and high aspect ratio silicon nanopillars. An isotropic etching process is utilized during the release of aluminum heaters fabricated on top of perforated free-standing Al_2O_3 membranes and silicon dioxide coated thermal silicon actuators. The fabrication process of three-dimensional sharp electrospray ionization (ESI) tips takes advantage of etching conditions that result in negatively tapered sidewalls. A self-feeding ESI interface for mass spectrometry (MS) is fabricated by combining a lidless micropillar filled channel with a sharp tip. Two approaches to the fabrication of silicon nanopillars are presented, both of which are suitable for wafer-scale manufacturing. One method combines silica nanoparticles with a highly anisotropic DRIE step, while the other method relies on highly over passivating conditions in a maskless DRIE process. Due to a large surface area and efficient light absorption in UV-range, silicon nanopillar structured surfaces are utilized as sample plates in laser desorption/ionization (LDI) MS. The wetting of nanopillar structured silicon surfaces is also studied. Fluoropolymer coated nanopillar structured surfaces have a contact angle of more than 170° and are ultrahydrophobic, whereas oxidized nanostructured surfaces are completely wetting. The accurate patterning of both completely wetting and ultrahydrophobic areas side by side allows complex droplet shapes and droplet splitters to be tailored.

Keywords Cryogenic deep reactive ion etching; microfabrication; nanofabrication; silicon

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Tiivistelmä

Väitöskirja käsittelee kryogeenistä lämpötilaa hyödyntävää reaktiivista ionietsausmenetelmää ja sen soveltamista piistä tehtyjen mikro- ja nanorakenteiden valmistukseen. Rakenteita hyödynnetään mikrofluidistisissa ja mikromekaanisissa komponenteissa. Etsausprosessi perustuu SF_6/O_2-plasman käyttöön alle -100 °C lämpötilassa. Osa fotoresisteistä ei ole yhteensopivia matalan lämpötilan kanssa, vaan ne halkeilevat, kun taas Al_2O_3 soveltuu hyvin kryogeenisen etsausprosessin etsausmaskimateriaaliksi. Ohut passivointikerros rakenteen sivuseinämillä parantaa etsausprosessin anisotropiaa estämällä sivusuuntaisen etsaantumisen. Tärkeimmät parametrit, joilla passivointikerroksen paksuutta voidaan säätää, ovat prosessin lämpötila ja O_2-virtaus. Sopivissa olosuhteissa on mahdollista saavuttaa täysin pystysuorat sivuseinät, kun taas liian ohut passivointikerros aiheuttaa levenevän (negatiivisen) sivuseinäkulman. Olosuhteissa, joissa passivointikerrosta ei muodostu (esim. korkeammissa lämpötiloissa tai ilman happivirtausta), etsausprofiilista tulee isotrooppinen. Toisaalta liian korkea happivirtaus johtaa ylipassivointiin. Hieman ylipassivoivissa olosuhteissa sivuseinän kulma on kapeneva (positiivinen), ja voimakas ylipassivointi johtaa mustan piin syntymiseen. Musta pii tunnetaan myös nimellä piinanoruoho.

Tyypillisesti rakenteisiin halutaan pystysuorat sivuseinät. Tässä väitöskirjassa osoitetaan myös yli- ja alipassivointi-olosuhteiden hyödyllisyys. Anisotrooppisia etsausolosuhteita hyödynnetään syvänteiden, mikrofluidististen pilarikanavien ja korkean aspektisuhteen nanopilareiden valmistuksessa. Isotrooppista prosessia hyödynnetään itsekantavan reititetyn aluminakalvon päälle valmistettujen alumiinihehkulankojen ja piidioksidilla pinnoitettujen piiaktuaattoreiden vapautuksessa. Terävän sähkösumutusionisaatiokärjen valmistus hyödyntää negatiivia sivuseinäprofiileja tuottavia etsausolosuhteita. Kun kanneton pilarikanava ja terävä kärki yhdistetään, voidaan valmistaa itsesyöttävä sähkösumutus-ionisaatiolähde massaspektrometriaan. Työssä esitellään myös kaksi tapaa valmistaa piistä tehtyjä nanopilareita. Valmistustavat soveltuvat suurien pinta-alojen prosessointiin. Ensimmäisessä tavassa piioksidisia nanopartikkeleita käytetään etsausmaskeina kryogeenisessä etsausprosessissa. Toinen tapa hyödyntää kryogeenistä etsausprosessia ylipassivoivissa olosuhteissa ilman maskia. Suuren pinta-alansa sekä UV-valon voimakkaan absorption takia nanopilaripinnat sopivat näytealustoiksi LDI-massaspektrometriaan. Myös nanopilaripintojen vettymistä tutkittiin. Kontaktikulma veden ja fluoropolymeerillä pinnoitettujen nanopilareiden välillä on yli 170° ja pilarit ovat ultrahydrofobisia. Oksidoidut nanopilaripinnat ovat puolestaan täysin vettyviä. Täysin vettyvien ja ultrahydrofobisten pintojen kuviointi tarkasti vierekkäin mahdollistaa vesipisaroiden muodon manipuloinnin ja pisarajakajan valmistuksen.

Asiasanat Reaktiivinen ionietsaus kryogeenisissä lämpötiloissa; mikrovalmistus; nanovalmistus; pii

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Preface

The work presented in this thesis was carried out at the Microfabrication group at the Helsinki University of Technology during the years 2006-2008. There are so many people who have helped and supported me along the way that this page is not big enough to mention everyone, but below I have listed some of the many people and organizations whom I am grateful to.

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Espoo, April 2009

Lauri Sainiemi

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4 Conclusions and future outlook ... 51

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List of publications included in the thesis:

The following peer-reviewed publications form the basis for this thesis. The publications are hereafter referred to by their Roman numerals:

I Handbook of Silicon Based MEMS Materials and Technologies, editors Veikko Lindroos, Markku Tilli, Ari Lehto and Teruaki Motooka:

Franz Lärmer, Sami Franssila, Lauri Sainiemi, Kai Kolari: parts of the chapter "Deep reactive ion etching", Elsevier (to be published autumn 2009)

II Lauri Sainiemi, Sami Franssila, Mask material effects in cryogenic deep reactive ion etching, *Journal of Vacuum Science and Technology B,* **25**, 801-807, 2007, DOI:10.1116/1.2734157

III Lauri Sainiemi, Teemu Nissilä, Ville Jokinen, Tiina Sikanen, Tapio Kotiaho, Risto Kostiainen, Raimo A. Ketola, Sami Franssila, Fabrication and fluidic characterization of micropillar array electrospray ionization chip, *Sensors and Actuators B, Chemical*, **132**, 380-387, 2008, DOI:10.1016/j.snb.2007.09.077

IV Lauri Sainiemi, Kestas Grigoras, Sami Franssila, Suspended nanostructured alumina membranes, *Nanotechnology*, **20**, 2009, 075305, DOI: 10.1088/0957-4484/20/7/075306

V Lauri Sainiemi, Kestas Grigoras, Ivan Kassamakov, Kalle Hanhijärvi, Juha Aaltonen, Ji Fan, Ville Saarela, Edward Hæggström, Sami Franssila, Fabrication of thermal microbridge actuators and characterization of their electrical and mechanical responses, *Sensors and Actuators: A Physical,* **149**, 305-314, 2009 DOI:10.1016/j.sna.2008.11.031

VI Lauri Sainiemi, Helmi Keskinen, Mikko Aromaa, Laura Luosujärvi, Kestas Grigoras, Tapio Kotiaho, Jyrki M. Mäkelä, Sami Franssila, Rapid fabrication of high aspect ratio silicon nanopillars for chemical analysis, *Nanotechnology*, **18**, 505303, 2007, DOI:10.1088/0957-4484/18/50/505303

VII Ville Jokinen, Lauri Sainiemi, Sami Franssila, Complex droplets on chemically modified silicon nanograss, *Advanced Materials*, **20**, 3453-3456, 2008 DOI:10.1002/adma.200800160

Author’s contribution to the publications included in the thesis

Publication I:
One of the authors of the book chapter. Author’s contributed especially to chapters 23.3, DRIE processes and 23.5, DRIE applications.

Publication II:
Planning the experiments, all the experimental work and writing the article.

Publication III:
Planning the experiments, experimental work with the exception of mass spectrometry, and writing the article.

Publication IV:
Planning the experiments, experimental work with the exception of the nanobead processes and atomic layer deposition, and writing the article.

Publication V:
Planning the experiments, experimental work with the exception of the white light interferometry part, and writing the article.

Publication VI:
Planning the experiments, micro- and nanofabrication work with the exception of the porous silicon fabrication, and writing the article.

Publication VII:
The planning of the experiments, experimental work and the writing of the article were all done together with Ville Jokinen. Equal contribution with the first author.

Abbreviations

μPESI	micropillar array electrospray ionization
μTAS	micro total analysis systems
ADRE	aspect ratio dependent etching
ALD	atomic layer deposition
Al_2O_3	aluminum oxide / alumina
APCI	atmospheric pressure chemical ionization
APPI	atmospheric pressure photo ionization
BOX	buried oxide layer
CHF_3	carbon hydro trifluoride
CF_4	carbon tetrafluoride
$C_2H_2F_3NO$	trifluoroacetamide
C_4F_8	octofluoro cyclobutane
CTE	coefficient of thermal expansion
CVD	chemical vapor deposition
DIOS	desorption/ionization on silicon
DRIE	deep reactive ion etching
EBL	electron beam lithography
EDP	ethylene diamine-pyrocatechol
ESI	electrospray ionization
FIB	focused ionbeam etching
H_2	hydrogen
HF	hydrofluoric acid
IC	integrated circuits
KOH	potassium hydroxide
LDI	laser desorption ionization
LFS	liquid flame spray
MALDI	matrix assisted laser desorption ionization
MEMS	microelectromechanical systems
MOSFET	metal oxide semiconductor field effective transistor
MS	mass spectrometry
NIL	nanoimprint lithography
HNO_3	nitric acid
NSL	nanosphere lithography
O_2	oxygen
PECVD	plasma enhanced chemical vapor deposition
RF	radio frequency
RIE	reactive ion etching
SALDI	surface activated laser desorption/ionization
SEM	scanning electron microscopy
SF_6	sulfur hexafluoride
SOI	silicon on insulator
S-FIL	step & flash imprint lithography
SiO_2	silicon dioxide / silica
SiO_xF_y	silicon oxyfluoride
TEOS	nanoparticles tetra–ethyl–ortho–silicate
TMAH	tetramethyl ammonium hydroxide
UV	ultraviolet

1 Introduction

Historical perspective

The first transistor was fabricated in 1947 by Bardeen, Brattain, and Shockley and the first patent application concerning integrated circuits (IC) was filed over ten years later in 1959 by Jack Kilby [1]. The first transistors were made out of polycrystalline germanium, but soon the superiority of single crystalline materials was noticed. The single crystalline materials offered reproducible and uniform device properties with longer carrier lifetimes and higher carrier mobility [2]. Point contact transistors were already commercially available by the mid 1950s. Germanium was still the dominant material, despite the fact that the fabrication of silicon transistors was demonstrated very soon after the first germanium transistor. The dominant fabrication techniques of point contact transistors were grown junction and alloy junction technologies. At this stage, there were no means for integrating multiple transistors on a single chip [3].

The next big leaps towards modern IC technology were the inventions of the gas phase diffusion process and the planar transistor fabrication process. At this point, silicon quickly replaced germanium as the main transistor material. The silicon transistor enabled higher output powers and operating temperatures than germanium. Also the good availability of silicon, the possibility to fabricate single crystalline silicon wafers and tailor the resistivity of the material made its use feasible. Furthermore, the single most important factor that made silicon the transcendent material for electronic applications was possibility of growing a silicon dioxide layer on top of the wafer in a controllable manner [2]. Chemically, silicon dioxide is a fairly inert material and therefore often utilized as a passivating coating to protect silicon from reacting with environmental impurities. Patterned silicon dioxide layers also work as a diffusion and an etch mask. Silicon dioxide is an insulating material which, even today, is used as a gate oxide material in metal oxide semiconductor field effective transistors (MOSFET).

After these developments, the first integrated circuits were demonstrated. The first IC was fabricated by Kilby, again based on germanium transistors. Less than a year later, Robert Noyce demonstrated the first silicon based IC. The design presented by Noyce took advantage of the planar process. The emitters and the collectors were diffused into the substrate. The individual components fabricated on a single substrate were interconnected using evaporated aluminum [1]. The circuit presented by Noyce was, in principle, very similar to modern integrated circuits. The usefulness of integrated circuits was soon realized and they completely revolutionized the world of electronics to such an extent that today all electronic devices (computers, cellular phones etc.) rely on integrated circuits. The scientific community also realized the value of these inventions. Bardeen, Brattain and Shockley were awarded the Nobel Prize in Physics in 1956 for their researches in semiconductors and their discovery of the transistor effect. Kilby received the same honor in the year 2000 for his part in the invention of integrated circuits.

Since the 1960s, basic technology has advanced steadily and the demand for higher numbers of components on smaller chips has made it necessary to develop more accurate silicon micro- and nanofabrication techniques. Gradually, the benefits of miniaturization in other fields of engineering became apparent, and the miniaturization of, for example, mechanical, optical and fluidic devices was begun

[4-12]. Silicon was also the most obvious choice of material for non-electronic applications, due to its good mechanical properties and the fact that fabrication techniques had already been developed for the needs of IC industry. The first resonator based on silicon surface micromachining techniques was published already 1967 [4]. Later, a similar but more sophisticated device was fabricated and utilized in radio frequency switching applications [7]. The device fabrication utilized methods such as bulk micromachining and epitaxial growth of silicon. Today, there are many research groups that devote their efforts entirely to the development of radio frequency microelectromechanical systems (RF-MEMS). Similar membrane structures and small moving parts that are important in RF-MEMS have also played a key role in the development of miniaturized sensors and transducers [8, 9, 11]. Pressure sensors and accelerometers were among the first sensors that were miniaturized, and today both of these devices have been commercialized [13]. Lately, the feasibility of MEMS technology has also been applied to the field of optics [12]. The polished silicon surface is a good substrate for a micromirror, and the mechanical properties of silicon offer the possibility of fabricating fatigue free components. These are key elements in optical switches.

The first microfluidic devices emerged in 1970's [5, 6, 9]. A microfluidic nozzle, used for ink jet printing, was one of the first fluidic applications that took advantage of silicon micromachining [6]. The first nozzles were simply through-wafer anisotropically wet etched holes. Since their initial release, ink jet nozzles have developed substantially and they still are probably the most widespread and most successfully commercialized miniaturized fluidic devices. In addition, much more complex fluidic devices have been created by means of silicon microfabrication. Terry et al. fabricated a gas chromatograph on a silicon wafer [5, 9]. This miniaturized chromatograph, just as a conventional one, consisted of inlets for the sample and carrier gases, a capillary column for the sample separation, and a thermal conductivity detector. A glass cover was anodically bonded onto silicon wafer to enclose the channels. Anodic bonding is still frequently used to seal the fabricated silicon micro channels. This miniaturized gas chromatograph was around the size of a matchbox. A new boost was given to the development of miniaturized fluidic systems capable of chemical analysis in the early 1990`s, when Manz et al. introduced the concept of miniaturized total analysis systems (μTAS) [10]. Since then, the goal of many research groups has been to integrate several functions such as sample concentration, separation and analysis on a single fluidic chip.

Etching of silicon

When creating desired structures into a silicon wafer, some parts of the wafer must be protected while the unprotected parts are etched. The protective material is known as an etch mask, and a common substance used for this purpose is silicon dioxide. Silicon etching is typically divided to two main categories: wet etching and dry etching according to the type of etchant. In wet etching, the partially protected silicon wafer is immersed in an aqueous solution such as potassium hydroxide, which etches silicon from unprotected areas. In dry etching gaseous etchants etch the silicon substrate. Reactive ion etching (RIE) and plasma etching are, on some occasions, used somewhat incorrectly as synonyms for dry etching. Reactive ion etching is the most common dry etching method, which combines the effects of chemically active gaseous radicals and physical ion bombardment. Other dry etching methods include spontaneous chemical etching (E.g. XeF_2 etching) and ion beam etching.

Deep reactive ion etching (DRIE) is considered an extension of RIE. They both rely on the same etching mechanisms (ion bombardment and chemical etching), but DRIE enables the fabrication of deeper and narrower structures with a higher etch rate than conventional RIE. DRIE reactors are also equipped with two power sources and, unlike traditional RIE systems, they employ sidewall passivation to enhance process anisotropy. DRIE is nowadays a commonly used technique in the fabrication of MEMS and microfluidic devices. There are two main deep reactive ion etching processes. The most common one is the Bosch process, which is also known as "switched process" or "time multiplexed process". The other one is known as a "cryogenic process" due to its low process temperature. This thesis presents how cryogenic DRIE processes can be applied to the fabrication of silicon micro- and nanostructures of microfluidic and MEMS components.

Thesis outline

This thesis consists of this review and seven articles published elsewhere. Publication I contains parts of a chapter of a book which briefly reviews available DRIE chemistries and DRIE equipment requirements. The cryogenic DRIE technique and processes are discussed in detail, along with advanced issues and challenges common to all DRIE processes. The reasons why and how DRIE is applied to the fabrication of fluidic and MEMS components are also reviewed in Publication I.

Publications II-VII are peer reviewed journal articles that form the basis for this thesis. Publication II examines the mask material issues related to cryogenic DRIE processes. Not all mask materials tolerate the low temperatures required for the cryogenic DRIE process. Publication III presents a new kind of silicon based electrospray ionization chip. The fabrication of this device utilizes nested mask and through-wafer etching. The capability for tailoring the sidewall angles during the cryogenic DRIE process is utilized to create truly three dimensional structures. Publication IV demonstrates a method for the fabrication of smooth and corrugated suspended alumina membranes. Smooth membranes can be used as supporting layers for metallic devices and corrugated ones could have applications in fluidics. Publication V describes a fabrication process for free-standing single crystalline silicon microbridges. These devices are fabricated on silicon-on-insulator (SOI) wafers and the capability to switch between anisotropic and isotropic etching is exploited. In publications VI and VII, silicon nanopillars are fabricated and utilized. Publication VI demonstrates a novel method for silicon nanopillar fabrication which combines liquid flame spray deposited silica nanoparticles and the cryogenic DRIE process. The nanostructured surfaces are exploited in laser desorption/ionization on silicon mass spectrometry. In publication VII, nanopillar structured silicon surfaces are selectively chemically modified and areas of complete wetting are created alongside ultrahydrophobic surfaces. Extremely high wettability contrast makes it possible to tailor droplet shapes and to design passive droplet splitters.

Chapter 2 of this thesis describes the fundamentals of silicon micro- and nanofabrication. The most common lithographic techniques are briefly introduced before a discussion about the etching of silicon is presented. This chapter places an emphasis on fluorine based deep reactive ion etching, but the basics of chlorine and bromine plasma chemistries and wet etching are also covered. The most common applications and limitations of DRIE (such as loading and aspect ratio dependent

etching) are presented in Publication I and therefore they are not discussed here. In addition, film deposition techniques, bonding and packaging issues are excluded from the thesis. Chapter 3 provides a perspective on Publications II-VII.

2 Fundamentals of silicon micro- and nanofabrication

The transfer of micro- and nanopatterns into a silicon wafer typically requires two processes: a lithography step for masking, followed by an etching step that copies the mask pattern into the underlying silicon. Some direct etching methods, such as focused ion beam etching, are capable of producing accurate patterns without masking, but their use is mainly limited to niche processes and research purposes due to their slow speed. Section 2.1 presents the most common lithography techniques. Section 2.2 discusses how the mask pattern is transferred onto the silicon wafer. The focus is on silicon fabrication but, to some extent, other materials such as glasses, metals, and metal oxides can be processed in a similar manner.

2.1 Lithography

2.1.1 Optical lithography

Optical lithography is by far the most common way to create patterns in the field of microfabrication. A photoresist layer, which is sensitive to selected UV-wavelengths, is applied on the silicon substrate, typically by spin coating. Subsequently, the photoresist layer is UV-exposed through a partly opaque photomask. This photomask is typically made of quartz, and opaque patterns are made of chromium. The contact printing mask aligners typically utilize mercury lamps to produce a wide band UV spectrum that has a maximum peak at 365 nm (i-line) or at 436 nm (g-line). Modern stepper and scanner tools take advantage of magnification and utilize wavelengths of 193 nm generated by an ArF excimer laser [3]. The use of shorter wavelengths makes it possible to create smaller linewidths, but the use of deep UV-wavelengths also introduces new problems, such as the transparency of optical components. The UV-light initiates chemical reactions in the photoresist material. After exposure, the photoresist is developed. In the case of positive photoresist, the exposed photoresist areas are dissolved during the development and the opaque pattern on the photomask is copied to the photoresist layer as depicted in Figure 1. Negative photoresist chemistry results in a negative photomask pattern image [14, 15]. Positive photoresist chemistry is often utilized in pattern transfer because positive resists can be easily stripped away. In contrast, highly cross-linked negative resists are typically mechanically stronger, and more difficult to remove. Therefore, negative resists are often used for structural materials rather than pattern transfer [14]. Easy-to-remove negative photoresists are well suited for lift-off processes due to their negative sidewall slopes. Factors such as thermal stability, etch resistance, photosensitivity, resolution requirement and exposure wavelength all play a role in photoresist selection.

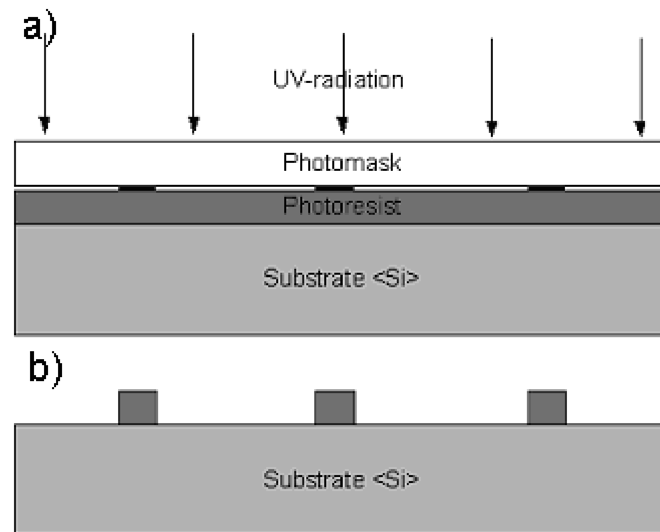

Figure 1. UV-lithography. a) Photoresist is applied on the silicon substrate, after which it is exposed to UV-light through the partly opaque photomask. b) In the case of positive photoresist, the areas exposed to UV-light become soluble in alkaline developer solution. After development, the opaque image of the photomask has been copied onto the photoresist.

Diffraction sets fundamental limits to the resolution of optical lithography. Still, today's integrated circuit manufacturers already routinely produce 45 nm linewidths using deep UV-lithography, and extreme UV-lithography systems are already on trial. The major drawback of a modern stepper and scanner system capable of producing such small structures is its price of tens of millions of dollars. The minimum linewidth of contact printing UV-exposure tools is around 500 nm, depending on the wavelength of the exposing light, exposure mode and clean room conditions. It should also be pointed out that the thickness of the photoresist layer has an effect on the minimum linewidth. A thick photoresist layer increases the minimum feature size as a result of Fresnel diffraction [16].

2.1.2 Electron beam lithography (EBL)

The most common way to produce nanostructures (excluding deep UV-lithography) is to use electron beam lithography [17]. An electron sensitive photoresist is exposed using a well-confined beam of electrons. The movement of the electron beam can be controlled accurately and the desired pattern is directly written onto the photoresist. No photomask is required. EBL makes it possible to produce linewidths below 10 nm in a repeatable manner, but at the expense of throughput. Due to the serial nature of the EBL technique, it is mainly used for the prototyping of silicon nanostructures and the manufacturing of photomasks and imprint masters. Commercial silicon fabrication processes are very limited.

2.1.3 Nanoimprint lithography (NIL)

The limitations of UV and electron beam lithography techniques have led to the development of novel, rapid, and inexpensive nanofabrication schemes. Replication techniques have become very popular because of their simplicity. Nanoimprint lithography in particular has already challenged optical lithography in some industrial applications because of the low price and good performance of the tools [18]. The technique was originally introduced by Chou et al. in 1995 [19, 20].

The thermal nanoimprint lithography process starts with a silicon substrate. The polymer to be imprinted is applied on the substrate. The master (or mould) and the substrate are heated to imprinting temperature, which is dependent on the glass transition temperature (T_g) of the polymer that is being used. When the imprinting temperature is reached, which is typically around 80 °C above the T_g of the polymer, the mould is compressed against the polymer layer. When the pressure is applied on the master and the substrate, the protrusions on the master displace the polymer and the cavities of the master are filled. After the imprinting process, the temperature of the master and the substrate is lowered below T_g and the master is released. A thin residual polymer layer remains between the patterns on the substrate. The residual layer is removed using a short oxygen plasma etching step. The entire NIL process is depicted in Figure 2. Many modified NIL processes, such as UV-NIL [21] and step & flash imprint lithography (S-FIL^{TM}) [22, 23], which utilize UV-light instead of temperature to cure the resist, have also been developed. This makes the process faster but requires a transparent master or substrate.

The biggest advantages of imprinting techniques lie in the fact that, unlike optical methods, they are not diffraction limited and tools are inexpensive because they do not require complex optical lens systems to create sub-micron linewidths. The throughput and linewidth capabilities of imprinting techniques are similar to those of optical stepper tools, but alignment accuracy is poorer. Modern NIL tools are capable of precise alignment, but some of the price benefit is lost. The overlay accuracy of modern NIL tools is around 10 nm. Residual layer uniformity is another big challenge for NIL, as non-uniform residual layers result in the distortion of patterns that are created during the final oxygen plasma etching step. A recent article reviews the current status of thermal NIL and its variants [24].

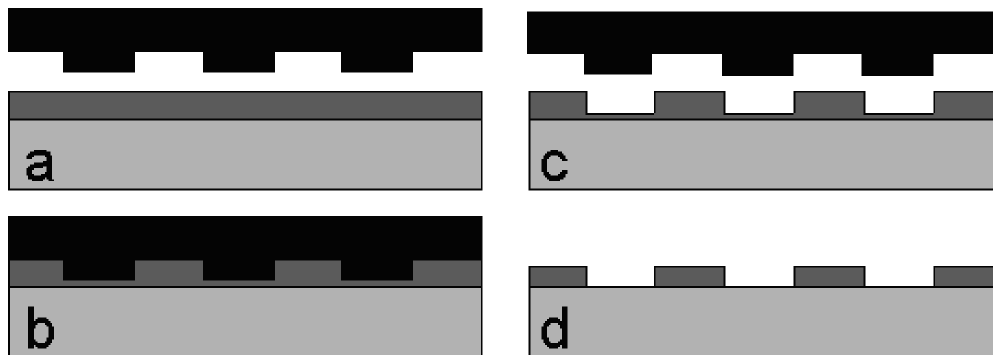

Figure 2. Thermal nanoimprint lithography process. a-b) The hard, heated mould is pressed against the heated thermoplastic polymer on the substrate. c) After cooling below T_g, the mould is released. d) Oxygen plasma is used to remove the residual polymer layer on the substrate.

2.1.4 Other masking techniques

Nanosphere lithography

The idea of using nanospheres as etch or deposition masks had already been introduced by the beginning of 1980’s [25]. A self-assembled monolayer of polystyrene spheres was applied to the wafer, and the spheres served as a mask during the subsequent etching or deposition process. This process was initially known as "natural lithography" [25]. The term "nanosphere lithography" (NSL) was introduced

over a decade later, when the development of double layer sphere masks was added to the technique and defect-free areas up to 100 μm^2 were demonstrated [26]. The biggest limitations of NSL are the inability to control the pattern shape freely and its small defect-free areas [27]. Sometimes the term "colloidal lithography" is used as a synonym for NSL.

Block copolymer lithography
The application of block copolymers to nanofabrication is based on their tendency to self-assemble into a thermodynamically stable morphology with feature sizes in the 10 nm – 200 nm scale [28, 29]. Block copolymer thin films are especially interesting, because they can be applied on flat surfaces and utilized as an etch mask for nanolithography or as a template for further structure deposition [30]. Depending on their film morphology, block copolymers are capable of producing pillars, holes, trenches, and lines. Controlling the morphology of the block copolymer thin film can be problematic. Still, the main problem of self-assembled block copolymers is that even if the self-assembly gives a very good short-range order, their long-range order is typically poor. The self-assembly also requires heat treatments lasting many hours, which limits the use of block copolymers in commercial applications [31].

Particle masks
In addition to polymeric nanospheres, other nanoparticles deposited on the substrate can also be used as etch masks for creating nanopillar structured surfaces [Publication VI, 32]. Silica [Publication VI] and metal nanoparticles [32], combined with anisotropic plasma etching have been utilized in the fabrication process of silicon nanopillars. Nanoparticle methods are typically well-suited for rapidly masking large areas, but they do not have similar self-assembling qualities to nanospheres and block copolymer films. In addition, nanoparticle deposition and anneal process temperatures are typically high. Nanoparticle masks are especially well-suited to applications such as chemical reactors and optical absorbers where random or quasi-regular arrays suffice and large surface areas and optical absorption are desirable.

2.2 Etching

The mask pattern, created using some of the techniques described above, is used as an etch mask in a subsequent etching step. The mask material should be stable under the etching conditions. During deep reactive ion etching of silicon, the photoresist is slowly consumed. Therefore the use of a thin photoresist mask (1 μm) is limited only to shallow etching (< 100μm). Thicker photoresist masks make it possible to create deeper structures, but the use of thick photoresist is typically not desirable due to linewidth limitations and possible cracking problems. Photoresists are also unable to tolerate harsh wet etching conditions such as heated potassium hydroxide solutions. The photoresist masks also have a quite limited temperature range and high and low temperatures are known to harm the resist [Publication II, 33, 34].

If photoresist cannot be used during the silicon etching step, a hard mask is needed. The most common hard mask material is silicon dioxide, which can be either grown thermally on top of the silicon substrate or deposited by chemical vapor deposition (CVD). After the lithography, the SiO_2 layer is etched and the photoresist is removed. The patterned SiO_2 layer now acts as an etch mask. The etch rate of SiO_2 during DRIE of silicon is very low, which makes the creation of deep structures possible. The temperature range allowed by the SiO_2 mask is superior to that of resists. The stability

of SiO_2 during the wet etching of silicon is also reasonable. Other common hard mask materials used during DRIE include metals, such as aluminum and nickel [Publication II, 35], metal oxides, such as aluminum and titanium oxides [Publication II, 36], and silicon nitride. Aluminum oxide in particular is an interesting masking material because of its extreme selectivity in cryogenic DRIE. Atomic layer deposition allows low-temperature deposition of conformal Al_2O_3 layers [Publication II]. Silicon nitride is an excellent masking material in KOH etching, but it is consumed quite rapidly during DRIE of silicon. Nevertheless, silicon nitride is also sometimes utilized as an etch mask for DRIE due to its low built-in stresses. Therefore, nitride is well suited for membrane applications [37, 38].

2.2.1 Wet etching

In wet etching, a masked silicon wafer is immersed in an aqueous solution that etches the unprotected silicon areas. Isotropic etching proceeds as spherical wave in all directions at a constant etch rate, while the anisotropic etching process causes some directions to be etched faster than others. For wet etching, the isotropic etching profile is most common, especially when etching amorphous or polycrystalline materials. Different etching profiles are introduced in Figure 3.

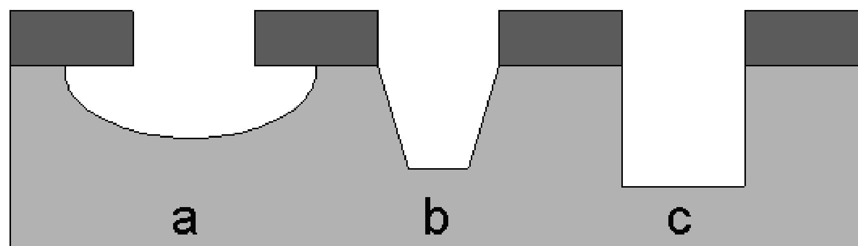

Figure 3. Trench profiles etched into (100) silicon substrate. a) Isotropic etching profile. b) An anisotropically wet etched trench. The sidewall angles are 54.7° because of the slow etch rate of <111> planes. c) In anisotropic dry etching, the sidewall angle is approximately 90° because of the directional ion bombardment and sidewall passivation.

Silicon is a crystalline material with a diamond lattice structure. Nowadays practically all silicon wafers used in microfabrication, with the exception of the photovoltaic industry, are single crystalline. Because of its crystalline structure, many common silicon wet etchants, such as potassium hydroxide (KOH), tetra methyl ammonium hydroxide (TMAH), and ethylene diamine-pyrocatechol (EDP), etch silicon anisotropically. In the anisotropic wet etching of silicon, the (100) atomic planes are the fast etching planes while the (111) planes etch substantially slower. Therefore, the sidewall angel of anisotropically wet etched trenches is 54.7°, which is the angle between the (100) and (111) atomic planes. The etch rate ratio between different planes is strongly dependent on the etchant, the solution concentration and the etching temperature. Also, additives such as isopropyl alcohol change the etch rate ratios of different atomic planes drastically [39, 40]. Isotropic wet etching of silicon is also possible, but it has limited applications. The most frequently utilized isotropic wet etchant is the mixture of nitric acid (HNO_3) and hydrofluoric acid (HF). Nitric acid oxidizes the silicon surface, which is simultaneously etched by HF. The etch rate of isotropic etchants can be two orders of magnitude higher than anisotropic ones, but they are also hard on resists [39].

Anisotropic wet etching of silicon is used in many industrial processes, such as the fabrication of ink jet nozzles, because of its well-known process characteristics, its

capability for batch processing and its low price. Isotropic etching is mainly utilized in applications where undercutting is desirable. For example, the release of free-standing perforated membranes, bridges and cantilevers can be achieved by selective and isotropic etching of the sacrificial layer beneath the structural material [Publication IV, Publication V, 41]. Free-standing alumina structures, released by the isotropic etching of underlying sacrificial silicon, are shown in Figure 4.

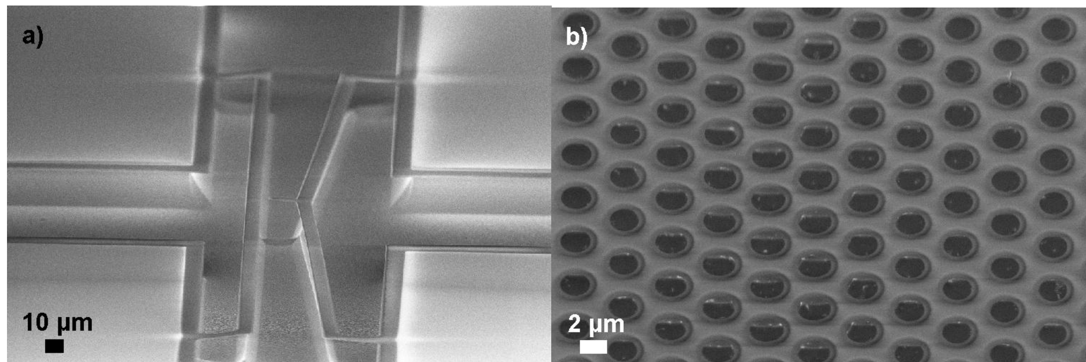

Figure 4. Free-standing alumina structures released by the isotropic plasma etching of underlying silicon [Publication IV]. a) Alumina bridges. b) Perforated alumina membrane.

2.2.2 Dry etching

There is a wide range of dry etching methods. Spontaneous chemical etching without ion bombardment can be employed for the isotropic etching of silicon [42]. On the other hand, ions without reactive radicals can also be used to etch materials. Focused ion beam etching is one example of an ion beam etching method and it will be discussed in more detail at the end of this chapter. Techniques such as laser ablation [43] and powder blasting [44] are sometimes categorized as dry etching methods [39], although they are quite different from traditional etching methods. Laser ablation is typically used for polymer microfabrication and powder blasting is especially useful when processing chemically inert materials such as glass. Still, reactive ion etching and the closely related process of deep RIE are the most commonly used dry etching methods in the field of microfabrication, and they shall be the main focus of this thesis. Publication I provides an in-depth review of the current status of deep reactive ion etching, with the exception of the Bosch process. Here, general reactive ion etching mechanisms are discussed, and both the Bosch and the cryo processes are introduced and compared with each other.

Etching process

There are a large number of review articles concerning reactive ion etching [39, 45 - 48]. Many processes take place simultaneously in the process chamber. The etching event can be divided up into seven processes, all of which are essential [45, 46, 49]. The processes are:

1. The generation of active species. Electron-impact dissociation/ionization creates a glow discharge from feed gases. The most typical feed gas in silicon etching is sulphur hexafluoride (SF_6), which forms neutral fluorine radicals (F^*) and positive and negative ions (SF_5^+, F^-).

2. DC bias generation. The silicon wafer is placed on the capacitively coupled bottom electrode, which is typically driven by the frequency of 13.56 MHz. The generated ions cannot follow the applied field, but electrons have higher

mobility and therefore the bottom electrode charges negatively. Due to this so-called self-bias voltage, the substrate is exposed to positive ion bombardment. In modern DRIE reactors the plasma is generated using an inductively coupled plasma source, which results in a plasma density that is 1-2 orders of magnitude higher (ca. 10^{12} ions/cm^3). The bias voltage between the plasma and the wafer can be adjusted with a separate capacitively coupled source.

3. The transport of reactive species from the plasma glow to the wafer by diffusion.

4. The adsorption of reactive species. Generated active fluorine radicals are adsorbed by the silicon surface. The bombarding ions remove the fluorinated surface layer (SiF_x) and produce so-called active sites where fluorine radicals are adsorbed.

5. Reaction. The adsorbed fluorine radicals react with silicon forming SiF_x ($x \leq 4$) species. The reaction rate between the fluorine and silicon is greatly increased by ion bombardment.

6. The desorption of reaction products. The SiF_x species that are formed must desorb from the surface. Otherwise the reaction products can form an etch inhibitor layer on the surface. SiF_x molecules have a high vapor pressure and, therefore, they are typically volatile. Ion bombardment enhances the removal of non-volatile reaction products from horizontal surfaces by sputtering.

7. Exhaust. Desorbed reaction products diffuse back to the plasma glow and they are exhausted. Otherwise, dissociation of the reaction products and redepositon may occur.

Reactive ion etching chemistries

Reactive ion etching is an anisotropic process but, unlike wet etching, the etch rate is not dependent on the crystalline structure of silicon as depicted in Figure 3. RIE creates trenches that have, in principle, vertical sidewalls due to directional ion bombardment. Still, the RIE processes that rely on pure SF_6 or CF_4 chemistry are not capable of producing high aspect ratio structures because the sidewalls are also exposed to highly reactive fluorine radicals. Anisotropy can be enhanced by using less reactive etchants, or by protecting the sidewalls with a passivation layer.

Chlorine and bromine plasmas can also be used to etch silicon, even though their reactivity with silicon is considerably lower than the reactivity of fluorine [35, 50, 51]. Due to their low reactivity, Cl and Br radicals do not etch silicon spontaneously, or the spontaneous etching that does occur is insignificant. Silicon is etched only when ion bombardment is present. Because of the directionality of the ions, the etch profiles are anisotropic. The drawback of using less reactive etchants is a considerably lower etch rate [35]. The selectivity of photoresist, silicon dioxide and metal masks is also lower with Cl-based plasmas than with fluorine plasmas due to a low silicon etch rate and the greater ion bombardment required for the desorption of non-volatile etch products. Low selectivity typically requires the use of metal masks if deep structures are desired [35]. Integrated circuit manufacturers still rely on Cl- or Br-based plasmas because the required etch depths are shallow, and tolerances for undercutting and

roughness are strict. Additionally, the aspect ratio dependent etching (ARDE) effect [Publication I] with Cl-based plasmas is typically less pronounced than with fluorine plasmas because of the lower process pressure, which results in a longer mean free path and more directional ion bombardment [35]. The ARDE effect can be seen again with extremely low pressures as a result of the starvation of neutral radicals [51]. In the MEMS industry, fluorine based plasma is a de facto standard because high etch rates and selectivity are frequently needed.

Formation of a non-volatile passivation layer on the substrate surface during the RIE process has been reported, especially when exploiting CHF_3 (or CF_4/H_2) plasma or plasma composed of molecules that contain fluorine (e.g. SF_6 or CF_4) and oxygen [46]. In the case of CHF_3 plasma, the passivation layer is composed of carbon and fluorine. The role of hydrogen is to catalyze the formation of polymeric precursors such as CF. Hydrogen also reduces the density of free fluorine radicals by forming HF. Chemistries relying on SF_6/O_2 and CF_4/O_2 gas mixtures result in a silicon oxyfluoride (SiO_xF_y) passivation layer [46]. The quality of the passivation layer is heavily dependent on the process temperature. At cryogenic temperatures the passivation layer is more stable and less oxygen is required for its formation [48]. The passivation layer improves the directionality of the etching. The layer is removed from horizontal surfaces by sputtering, but sidewalls remain protected. A low amount of oxygen in CF_4 or SF_6 plasma also increases the etch rate of silicon, because the recombination of fluorine radicals with CF_3^+ or SF_5^+ ions is reduced, which increases the amount of free fluorine [52]. Too high oxygen concentration in the plasma results in a thick passivation layer, which leads to a reduced etch rate and formation of silicon nanograss (or black silicon, silicon nanoturf and columnar microstructures) [53].

Deep reactive ion etching

Both the Bosch [54] and cryo [55, 56] DRIE processes rely on inductively coupled fluorine based plasmas, and directionality is enhanced by sidewall passivation. The Bosch process utilizes a separate passivation step followed by an etching step, while in the cryo process the passivation occurs simultaneously with the etching. Recently, cryogenic processes that exploit separate etching and passivation cycles have also been published [57, 58], but the main advantage of the cryogenic process over the Bosch process, smooth sidewalls, is lost. A cycled process, which resembles the Bosch process, has also been developed for a traditional capacitively coupled RIE tool [59]. The down side of this process is its low etch rate and poor uniformity.

The Bosch process is the most widely used DRIE technique. The processing of masked silicon wafer starts with a short etching step that utilizes SF_6 plasma. After this etching step, a thin fluorocarbon film is deposited on the wafer. The fluorocarbon film passivates the surface and prevents etching. Octofluoro cyclobutane (C_4F_8) is commonly used in the passivation step. It generates $(CF_2)_n$ radicals and results in a Teflon-like soft polymer film. At the beginning of the next short etching step, the fluorocarbon film is removed from horizontal surfaces. The SF_6 etching step is not anisotropic, but the polymer still etches preferentially from the horizontal surfaces due to directional ion bombardment, while the vertical sidewalls remain protected. The repetition of etching and passivation cycles results in almost vertical sidewalls [60]. The drawback of the process is the scalloping of the sidewalls due to the alternating etching and passivation steps [61]. The sidewall roughness can be reduced by

shortening the duration of the etching and passivation steps [Publication I] or by post processing: thermal oxidation followed by oxide etching [62], or annealing in a hydrogen atmosphere at high temperature [63] reduces the size of the scallops. This scalloping is discussed in a more detailed manner in Publication I. The Bosch process is presented schematically in Figure 5.

A continuous SF_6/C_4F_8 gas mixture does not produce scallops. The controllability of this kind of continuous mixed process is poor and the etch rate of the silicon is considerably lower than in normal Bosch process. Due to controllability problems, the etch depths are limited to ca. 10 μm [Publication I].

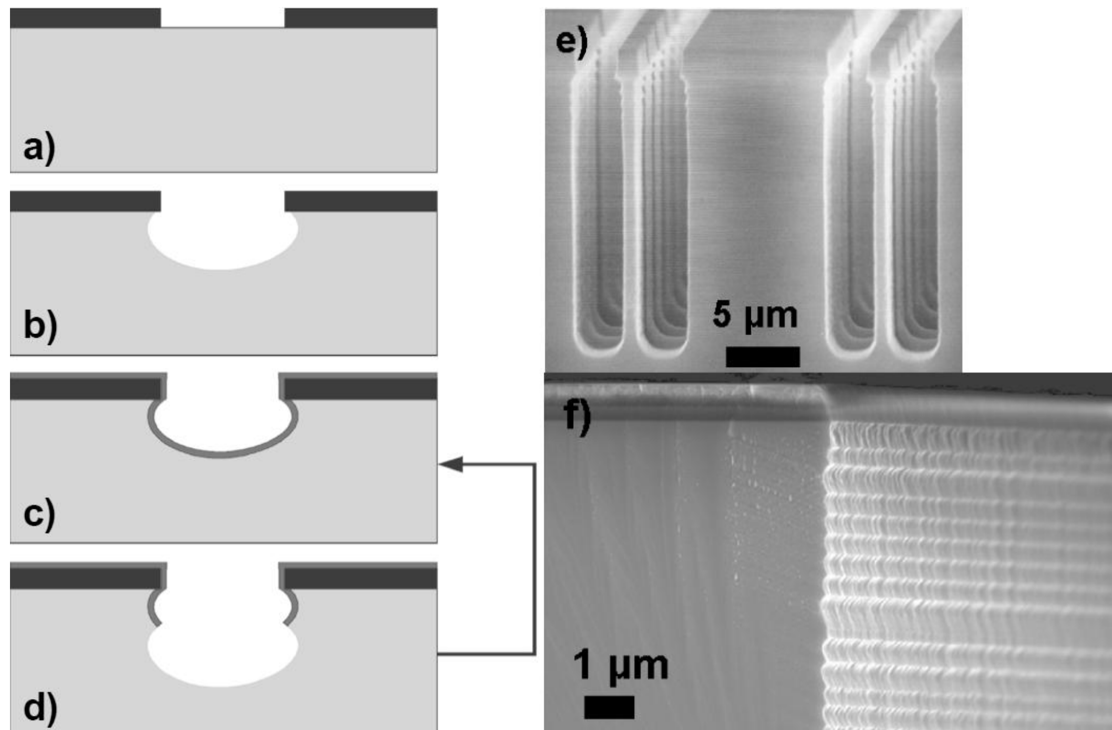

Figure 5. The Bosch process [47]. a) Patterning of etch mask. b) Etching step. c) Deposition of passivation layer. d) Next etching step. e) SEM image of trenches fabricated using the Bosch process. f) The close-up view reveals the scallops on the sidewalls.

The cryogenic DRIE process does not have separate etching and passivation steps, as they both occur simultaneously. The etching is performed in SF_6/O_2 plasma. At cryogenic temperatures (T < -100 °C), a passivating SiO_xF_y layer forms on top of the silicon surface [64, 65], which again is sputtered away from horizontal surfaces by directional ion bombardment. When the temperature is fixed, the thickness of the passivation layer is mainly determined by the O_2 flow rate. Too low oxygen flow results in the failing of the passivation layer and isotropic etching profiles, whereas too high oxygen content in the plasma leads to over passivation, a reduction to the silicon etch rate and the creation of black silicon [Publication VI, Publication VII, 56, 66]. Changing the SF_6/O_2 ratio is the most convenient way to optimize passivation layer thickness and, ultimately, the sidewall angles. The etch rate of silicon is mainly dependent on SF_6 flow rate and the power of the ICP source. Higher SF_6 flow and ICP power increase the quantity of free fluorine radicals that result in the higher etch rate of silicon. The etch rate of the masking material is mainly dependent on the ion energies that are determined by CCP source. The ions have to have sufficient energy to remove the passivation layer from horizontal surfaces, but when a certain threshold

is reached, an increase in CCP power only increases the etch rate of masking material and undercutting. The effect that the process parameters have on the conditions of the process and, ultimately, on the etch rate, selectivity and anisotropy of the process are summarized in Figure 6. The sidewall quality of structures etched using cryogenic DRIE is superior to Bosch process. Scanning electron microscope (SEM) images of cryo-etched structures are shown in Figure 7.

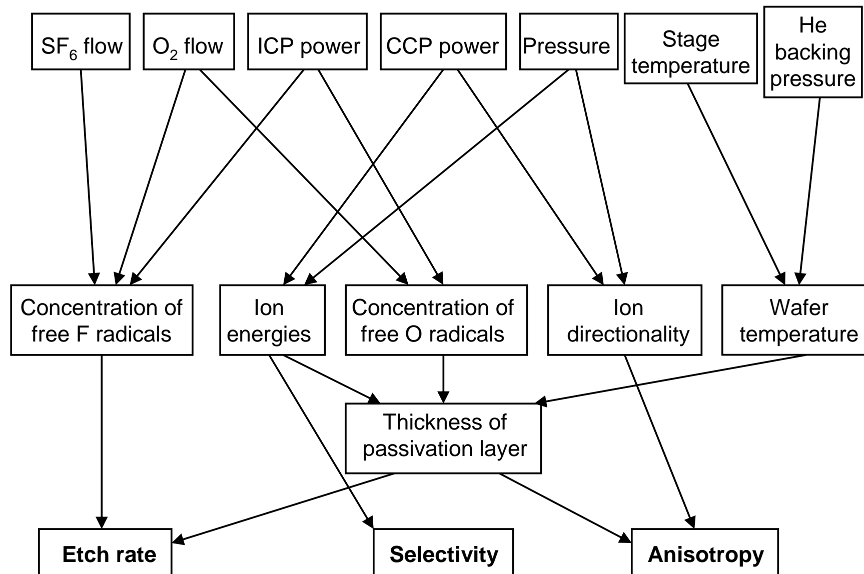

Figure 6. Guidelines for adjusting cryogenic DRIE process. Seven parameters that can be directly controlled using the equipment are shown at the top row. Their influences on process conditions and, ultimately, on the silicon etch rate, selectivity and anisotropy are indicated by the arrows.

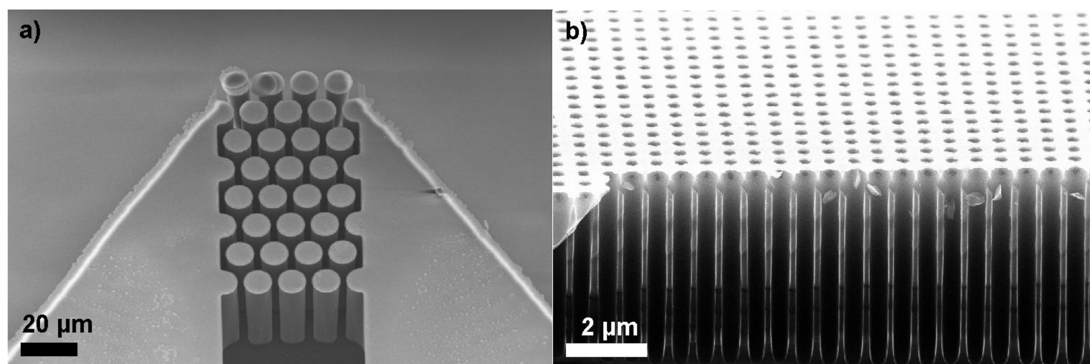

Figure 7. SEM images of structures etched using anisotropic cryogenic DRIE process. a) Micropillars at the end of a microfluidic channel. b) Nanoholes patterned using nanoimprint lithography.

Both Bosch and cryo processes typically utilize reactors which are equipped with two plasma sources: an ICP source for high density plasma generation and a CCP source for controlling the ion energies. Still, both processes also have their own special equipment requirements. The substrate temperature plays a key role in cryo processes. The possibility of controlling the substrate temperature accurately at very low temperatures is crucial. In Bosch processes, the temperature control is also important, but the temperatures used are considerably higher. The Bosch process uses etching and passivation steps that last only a few seconds. Therefore extremely high speed mass flow controllers, with sub-second settling times are required. Alternatively, fast-acting valves can be used to open and close gas lines to the process chamber at high

switching speeds [Publication I]. In the Bosch process it is also important to have an adequate ratio between ions and radicals. A relative ion concentration that is too high degrades the sidewall profiles. The reactor issues are discussed in a more detailed manner in ref. [34]. The highest etch rates (50 μm/min) have been demonstrated using the Bosch process. Generally, high etch rates are always achieved at the expense of undercutting and profile control and the etchable area must be small. Cryo processes typically have higher selectivity than Bosch processes, because ions that are at a low-energy are already enough to sputter the thin passivation layer.

Even though DRIE techniques are typically utilized to create sidewalls that are as vertical as possible, DRIE can be used to produce tilted sidewalls as well. By controlling the amount of passivation during the process, both positively and negatively tapered sidewalls are attainable. If passivation is not used, DRIE is capable of producing completely isotropic etch profiles, which is especially beneficial for the release of free-standing structures. The structures shown in Figure 4 have been released using isotropic plasma etching. Crystallographic dependent etching is also possible with cryogenic etching, when extremely low temperatures and low ion energies are used [56].

Focused ion beam etching

Focused ion beam (FIB) etching is a technique capable of producing accurately defined nanostructures without any masking [67]. It is also capable of sample imaging, ion implantation and, in a suitable gas atmosphere, thin film deposition [67]. FIB milling is a purely physical process which relies on a focused beam of gallium ions that sputter the surface. Redeposition of sputtered material can cause problems. FIB milling has an even lower throughput than electron beam lithography systems, which mainly limits its use to the prototyping of nanostructures. The rate of the milling process can be increased by introducing a reactive etching gas such as XeF_2, trifluoroacetamide ($C_2H_2F_3NO$) or Cl into the chamber. In this case, the nature of the process is not purely physical, but a combination of chemical etching and physical ion bombardment as seen with RIE. The advantages of FIB milling are its capacity for modifying complex devices fabricated using conventional microfabrication, along with the fact that no masking is required. At low ion doses, instead of etching the ions are implanted into the substrate and the ions dope the substrate with gallium [67, 68]. The gallium doped silicon has low etch rate when wet etching or cryogenic DRIE techniques are used on silicon. Therefore FIB can be used as direct masking method instead of etching. Using FIB masking combined with cryogenic DRIE, the process time is 1:30000 of the time that FIB etching requires [69]. The world's smallest Aalto Vase, fabricated using the doping method is shown in Figure 8.

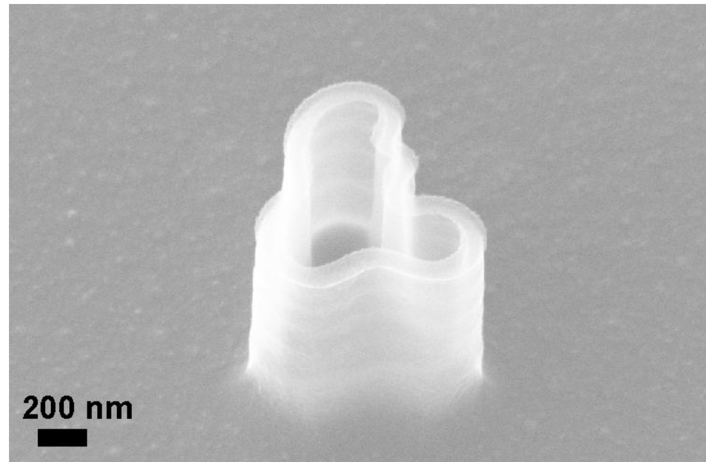

Figure 8. A SEM image of the world's smallest Aalto Vase. The vase was masked by FIB doping and etched using cryogenic DRIE. Picture courtesy of Nikolai Chekurov, Helsinki University of Technology.

3 Cryogenic deep reactive ion etching processes

3.1 Mask material effects and issues

3.1.1 Introduction

Photoresist is a good mask material for the DRIE of silicon, if only shallow features are required and the etching is performed at room temperature. The low temperatures involved in the cryogenic DRIE process set new requirements for masking materials. The use of photoresist masks is limited by their restricted selectivity [70], and the cracking of the photoresist also becomes a problem. Especially thick photoresists (> 1.5 µm) have been reported to be vulnerable to cracking [Publication II , 34]. Also temperatures above the glass transition temperature of the resist inflict problems [33].

Due to their better selectivity, hard masks are utilized when deep structures are required. The temperature range permitted by hard masks is also much greater than in the case of photoresist. Silicon dioxide is the most common hard mask material and it is also well-suited for cryogenic DRIE. The obvious drawback of all hard masks is the increased amount of complexity in the process, because extra deposition and etching steps are required. The isotopic etching of hard mask material also results in poor dimensional control [71]. Deposition of a hard mask, such as thermal silicon dioxide, may also require the inclusion of high-temperature steps in the process.

Metal masks are even more selective than SiO_2, but some metals have been reported to affect etch rate [72, 73], undercutting [74, 75], and the surface quality of the etched features [Publication II, 72, 76]. Similar effects can also be expected when using metal oxide masks. Fedynyshyn et al. [72, 73] noted that the etch rate of silicon increased in fluorine containing plasmas when aluminum was used as an etch mask. According to these studies, aluminum catalyzes the generation of free fluorine radicals and thus increases the etch rate. Aluminum masks are also known to create micro or nanograss on the etched silicon surfaces due to sputtering and redeposition of the aluminum on the etch field [Publication II, 50, 72, 76]. The redeposited aluminum micromasks protect underlying silicon from etching and micro- or nanopillars form under highly anisotropic etching conditions. This phenomenon is often referred to as “micromasking” and it is typically observed when using soft metal masks that have high etch selectivity.

3.1.2 Photoresist cracking

The cracking of five different types of photoresist was studied by dividing the cryogenic DRIE process to four distinct thermal phases:

1. Loading. The wafer is loaded onto the cryogenically cooled stage. Cooling of the wafer starts spontaneously.
2. Wafer cooling. The wafer is mechanically or electrostatically clamped onto the cryogenically cooled stage and helium pressure (ca. 10 Torr) is applied between the stage and the backside of the wafer to enhance the heat exchange.

3. Etching. Etching gases (SF_6/O_2) are fed into the chamber and power is turned on. The wafer is heated by the bombarding ions and exothermal reactions, and simultaneously cooled down.
4. Unloading. The etched wafer is unloaded from chamber and it heats up to room temperature spontaneously.

The etching process itself (phase 3) is never responsible for photoresist cracking. Photoresist cracking usually occurs already if only the phases 1 and 4 are run, as a result of the evolution of thermal stresses during thermal ramping [77-79]. The thermal stresses are caused by a thermal expansion mismatch between the silicon wafer and the photoresist film. Tensile stress in the thin film is known to create pinholes and cracks [80]. The stresses are released when the film cracks. In some cases, the photoresist can tolerate thermal ramping (phases 1 and 4), but cracking occurs when helium backside cooling is applied. During phase 2, the edges of the wafer are mechanically clamped against the stage and the pressure is applied to its backside. The pressure difference between the front and backsides of the wafer causes it to deform [Publication II, 81], thereby increasing the stresses in the photoresist. Increased stress may result in cracking. The wafer could also be cooled down to cryogenic temperatures without helium backside cooling, but this is required during the etching process because the bombarding ions and exothermal reactions on the wafer heat up the substrate and spontaneous heat exchange between the wafer and the etching stage is not enough to maintain cryogenic temperatures.

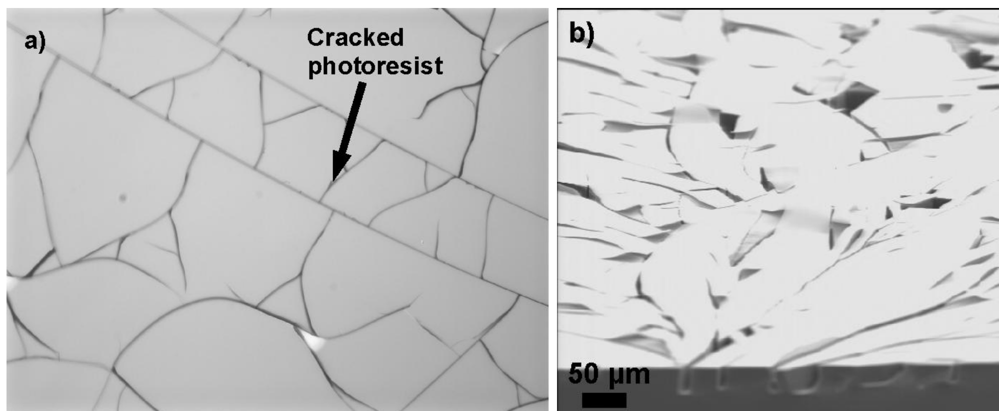

Figure 9. Photoresist cracking [Publication II]. a) An optical microscopy image and b) a SEM image of a cracked photoresist layer. Because the resist cracks during the wafer cooling, the crack patterns are also transferred onto the silicon during the etching phase, as seen in the SEM image.

The trend, which can be seen on Table 1 and has also been reported earlier [34], is that thin photoresists are generally more stable at cryogenic temperatures than thick ones. However, thickness is not the only factor that plays a role in photoresist cracking. SU-8 50 is a clear exception to this trend. Even very thick SU-8 50 layers do not have any cracking problems, because of the high cross-linking density of the negative EPON SU-8 resin based photoresists [Publication II]. If the photoresist has a high cross-linking density, this results in exceptionally good mechanical strength [82]. SU-8 50 is typically used as a structural material, as it has limited use as a masking material due to the fact that it is troublesome to remove.

Table 1. Cracking of different photoresist during cryogenic DRIE processes [Publication II].

Photoresist	Tone of resist	Layer thicknesses	Cracking problems
AZ 1505	Positive	0.5 μm	Not observed
AZ 5214 E	Positive	1.5 μm	Sometimes when He-backside cooling is turned on
AZ 4562	Positive	6.0 μm	Always at low temperatures
ma-N 415	Negative	2.6 μm	Always at low temperatures
SU-8 50	Negative	7; 20; 60 μm	Not observed

3.1.3 Hard masks

Hard mask materials do not suffer from cracking because their coefficients of thermal expansion (CTE) are better matched to the CTE of silicon [Publication II]. Hard mask materials also have better mechanical properties than photoresists. For example, the Young's moduli of SiO_2 and Al are around 56 GPa and 70 GPa respectively, while the Young's modulus of SU-8 is only 4 GPa.

The selectivity of hard mask materials is typically at least one order of magnitude higher than the selectivity of photoresists. The popularity of silicon dioxide is based on its well-explored material properties and growth, deposition and etching techniques. The thermal growth of SiO_2 requires temperatures around 1000 °C, which limits its use. Plasma enhanced chemical vapor deposition (PECVD) can be done at considerably lower temperatures (ca. 300 °C), but at the expense of the quality and the conformality of the film. In plasma etching, the etch rate of PECVD oxide is comparable with thermal oxide, whereas PECVD oxide is typically etched very rapidly with wet etching [83]. Silicon dioxide has not been reported to inflict surface roughening, changes in etch rate or pronounced undercutting like some of the metal masks.

Many metal masks such as aluminum have an exceptionally high selectivity and offer easy deposition at room temperature by sputtering or evaporation. Copying the photoresist pattern accurately to a metal film can be difficult because the plasma etching of some metals, such as nickel, is cumbersome. Aluminum is commonly utilized as an etch mask because of its wide availability, reasonable price and the fact that it can fairly easily be etched anisotropically in chlorine-based plasmas. The major tradeoff of an aluminum mask is the compromised surface quality of the etched features caused by micromasking. The effect that aluminum etch masks have on the etch rate of silicon in cryogenic DRIE processes has not been unambiguously observed. Two groups that have studied cryogenic DRIE reported pronounced undercutting when using an aluminum mask [74, 75], but mask material dependent etch rates have not been reported. In our experiments, mask material selection did not have a clear effect on the etch rate of silicon or undercutting [Publication II]. If aluminum actually catalyzes the generation of fluorine radicals, as speculated in [72, 73], the influence on the quantity of fluorine radicals in modern ICP equipped reactors is insignificant. Fluorine concentration in an old RIE reactor equipped only with a CCP source is very low compared to an up-to-date ICP reactor. This could explain why references [72, 73] found a connection between the mask material and the silicon etch rate, which can no longer be seen. It has been suggested that, instead of being caused by catalytic reactions, an instable etch rate could be caused by the uncontrollable process temperature in old RIE reactors [46].

Atomic layer deposited (ALD) amorphous alumina (Al_2O_3) combines the good properties of aluminum and silicon dioxide. This material has extreme selectivity (66 000:1), a fully conformal deposition profile, a deposition temperature of 85 °C, and it does not inflict micromasking [Publication II, 84, 85].The pattern transfer to the Al_2O_3 layer can be done accurately, even when isotropic wet etchants such as phosphoric acid or hydrofluoric acid are used, because an alumina layer that is just a few nanometers thick is enough for through-wafer etching. Thin alumina layers (< 10 nm) can also be etched using RIE or DRIE processes that utilize high bias voltage [86]. Due to the highly chemical nature of silicon etching, the bias voltages used in cryogenic DRIE are ca. 20-40 V. A bias voltage that is one order of magnitude higher is required for the etching of alumina.

3.1.4 Peeling mask

In the fabrication process of devices that require structures with different depths, a peeling mask (or nested mask) approach is often utilized in order to avoid applying photoresist over severe topography [Publication I, Publication III, 87]. Two (or more) mask materials are deposited and patterned on the substrate prior to any silicon etching. The mask material must be selected to allow selective patterning and the removal of the upper mask layer at the same time when other process requirements, such as sufficient selectivity, are being fulfilled. After the first DRIE step, the upper mask is removed to reveal the second mask layer and more silicon. The second DRIE step etches newly opened areas and continues etching the earlier opened areas to make them deeper. The use of a nested mask for the fabrication of a device is illustrated in Figure 15 and described in section 3.2.2.

The obvious combination of mask materials is a photoresist mask on top of a patterned silicon dioxide mask. The depth and the process temperature range of the first DRIE step is limited by the photoresist. Therefore, if deeper structures are required or cryogenic DRIE is utilized, a good mask pair is formed by silicon dioxide and alumina. Alumina is atomic layer deposited on a patterned silicon dioxide mask. The etching of alumina can be performed in phosphoric acid without harming the underlying silicon dioxide and silicon.

3.2 Miniaturized devices for analytical applications

3.2.1 Ionization methods for mass spectrometry

The concept of micro total analysis systems (µTAS) was presented in 1990 [6]. The basic idea was to integrate many fluidic components on a single microchip and utilize it in chemical analysis. Thereby, several functions that have traditionally been performed separately such as sample introduction, concentration, separation, and detection, could be integrated into a single lab-on-a-chip device. This would allow fast and cheap chemical analyses to be carried out on small sample amounts without laborious manual work. Another advantage of such miniaturized devices is that diffusion limited reactions occur substantially faster on a microscale. At the moment, only few true lab-on-a-chip devices exist [88, 89]. Most of the miniaturized devices perform only one or two functions.

Coupling a microfluidic chip to a mass spectrometer is a very common method for performing chemical analysis, due to the sensitivity and specificity of an MS measurement [90]. The most common coupling methods are laser desorption/ionization (LDI), electrospray ionization (ESI), and atmospheric pressure chemical ionization (APCI). The working principles of these methods are schematically illustrated in Figure 10. A recent tutorial, which reviews all atmospheric pressure surface ionization methods for mass spectrometry, can be found in [91].

In LDI methods, the sample is applied to the surface of a sample plate. The sample is desorbed from the surface and ionized by shooting it with a UV or IR-laser pulse for a few nanoseconds. The desorbed and ionized sample molecules are subsequently analyzed using an MS. Desorption and ionization processes are typically assisted by an organic matrix, which is crystallized with the sample molecules [92]. The drawbacks of matrix assisted LDI (MALDI) include increased background in the mass spectrum and the difficulty of integrating it with continuous detection systems. The background can be reduced by using a similar technique called lased desorption/ionization on silicon (DIOS) [93], or more generally by using surface assisted desorption/ionization (SALDI) that does not require a matrix. In SALDI the sample plate material, structure and surface chemistry play important roles [94]. The surface has to absorb the energy from the laser, protonate the sample molecules and desorb them. Typically, matrix-free SALDI techniques are only suited to the analysis of small molecules. Large molecules cannot be detected because desorption and protonation are not enhanced by a matrix.

Electrospray ionization is a widely applied technique in the field of analytical chemistry, especially proteomics, even though it is not well suited to the analysis of neutral compounds. Fenn et al. [95], who demonstrated the analysis of large biomolecules using ESI-MS, was awarded the Noble Prize in Chemistry in 2002. The flow rates used in ESI (ca. μl/min) are ideal for microfluidic devices. Therefore ESI is the most common method for coupling a microfluidic chip with mass spectrometry. In ESI, high potential difference (kVs) is applied between the ESI tip and the MS. The strong electric field at the tip creates a Taylor cone and an electrospray, which transport the ionized molecules to the MS. The voltage needed to create an electric field that is sufficiently strong for formation of an electrospray is dependent on the sample composition and the sharpness of the ESI tip [96]. Microfabricated ESI tips have already been combined with separation systems such as chromatography [97] and electrophoresis [98].

The APCI technique is better suited to the ionization of neutral compounds than ESI. A miniaturized APCI source is a nebulizer chip in which a liquid sample is evaporated, mixed with nebulizer gas and sprayed out. The ionization is done in the gas phase with an external coronal needle [99, 100]. The ionization of the sample that is sprayed out of the chip can also be achieved using UV-light instead of a corona needle [101]. This technique is called atmospheric pressure photoionization (APPI).

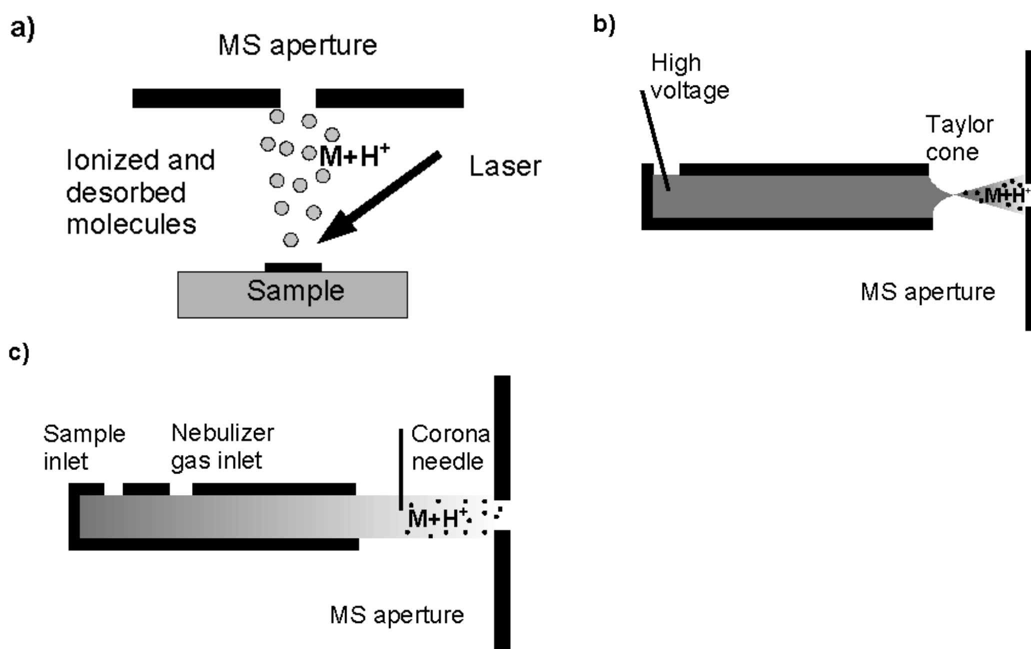

Figure 10. The most common ionization methods for mass spectrometry. A) Laser desorption ionization, b) electrospray ionization c) atmospheric pressure chemical ionization.

3.2.2 Miniaturized electrospray ionization source

Material issues

Again, the first choice of material for the fabrication of lab-on-a-chip devices was silicon because of its well explored fabrication techniques [5]. Silicon based ESI chips have been created [102-104], but more popular fabrication materials are glass [105] and polymers, such as parylene [106], poly(dimethylsiloxane) (PDMS) [107], and SU-8 [108].

Mechanically, glass is a fairly strong and chemically inert material that can tolerate high process temperatures. Its exact mechanical and thermal properties are heavily dependent on the type of glass that is used. For borosilicate glass, the maximum process temperature is ca. 500 °C, while quartz glass tolerates temperatures in excess of 1000 °C. In practice, the maximum operating temperature of a glass device is typically lower than the process temperature because glass cannot tolerate high temperature differentials. The transparency of glass is often beneficial, because it allows, for example, fluorescent detection. Glass is also a thermal and electrical insulator, which is often beneficial. Glass microfabrication techniques have developed rapidly during last two decades, but they are still slow and cumbersome compared to silicon micromachining [109-111].

Polymer microfabrication has become popular due to its simplicity [14] and low price of materials. The temperature range allowed for polymers is heavily dependent on the polymer that is used, but it is generally much more limited than for glass and silicon. Also their mechanical properties are inferior. The poor solvent tolerance of polymers is limiting their use in analytical applications. At the moment, most polymer microfabrication techniques cannot compete with silicon micromachining for the

fabrication of complex three dimensional features and high aspect ratio structures, as shown in Figure 11.

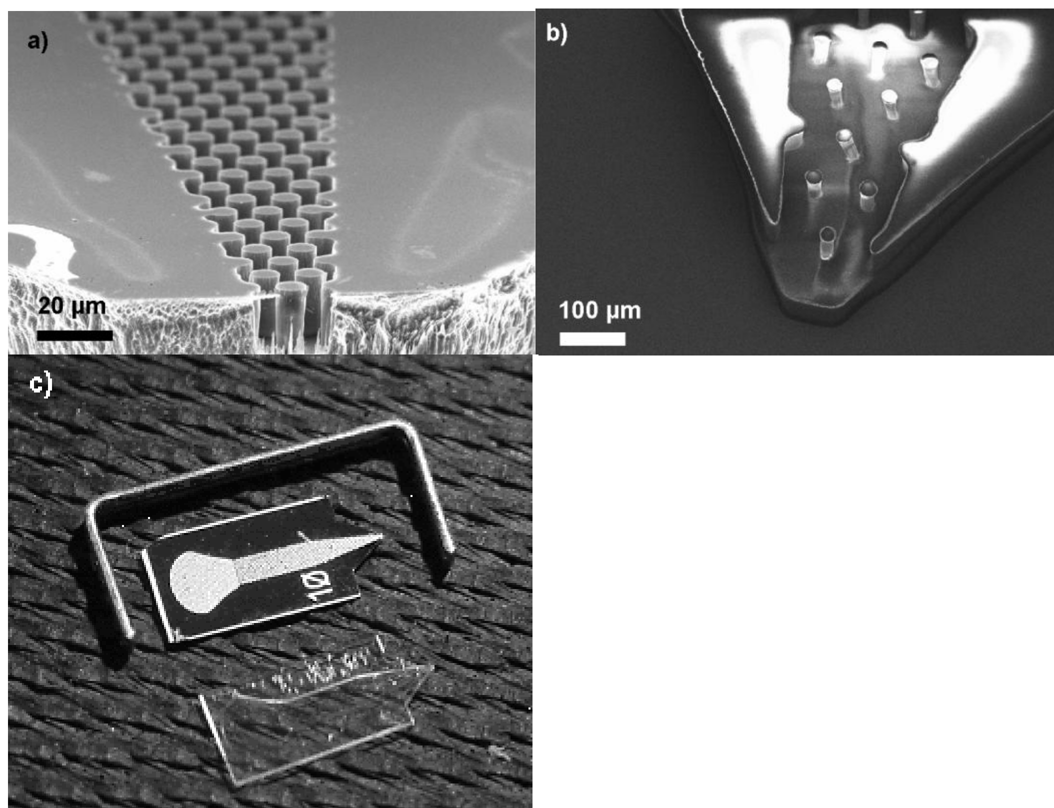

Figure 11. Micropillar array electrospray ionization chips. SEM images of similar pillar chips fabricated of a) silicon b) SU-8 polymer. c) A photograph of both chips. The chips are 8.5 mm long and 4 mm wide.

Capillary filling of a lidless channel

Electroosmotic flow is a common sample transportation method in miniaturized electrospray sources, because it enables electrophoretic separations before ESI [98]. In silicon based ESI sources, electroosmotic flow cannot be utilized due to the conductivity of silicon. An alternative to electroosmotic sample transport is pressure driven flows actuated by pumps [108]. The third option is to utilize capillary forces to transport the sample [104]. This circumvents the need for external actuators. A drawback of systems that rely on capillary forces is that narrow, enclosed channels are typically required in order to achieve adequate capillarity.

Basically, the surface energetics of the channel determine the capillary filling. If filling leads to the reduction of free surface energy, the channel fills spontaneously. The surface energy of the system and the contact angles are connected by the Young-Dupré equation.

$$\gamma_{sv} - \gamma_{sl} = \gamma_{lv}\cos\theta, \quad (1)$$

where θ is the contact angle, γ_{lv}, γ_{sl}, and γ_{sv} are the surface energies of the liquid-vapor, solid-liquid and the solid-vapor phases respectively. For a microchannel that has a rectangular cross-section, the pressure inside the liquid can be written as [112]:

$$P = \gamma_{lv}(\frac{\cos\theta_t + \cos\theta_b}{d} + \frac{\cos\theta_l + \cos\theta_r}{w}), \quad (2)$$

where θ_t, θ_b, θ_l, and θ_r are the contact angles at the top, bottom, left, and right channel walls respectively, d is the depth and w the width of the channel. Positive capillary pressure indicates that filling of the channel is energetically favorable and will happen spontaneously if there are no other forces present. From the latter equation it can be concluded that low contact angles and small channel dimensions result in high capillary pressure. Filling is more favorable in enclosed channels than in open systems, because the contact angle between the sample and air is 180° and all other surfaces provide smaller contact angles and thus higher capillary pressure.

The other way to increase the capillary pressure is to increase the amount of hydrophilic material inside the channel. This can be done by micromachining an array of micropillars inside the flow channel. Qualitatively, the difference in the capillary filling properties of a channel with and without a micropillar array is that the channel with the micropillar array has more hydrophilic surface area per unit length, which makes the pillar channels more conducive to capillary flow. The filling of lidless silicon channels without pillars and with a pillar array is compared in Figures 12 and 13. Otherwise, the channels are identical. It is remarkable that even a 1 mm wide channel that has a micropillar array inside fills spontaneously. The filling rate of the channels can be tuned by changing the packing density of pillars or by tuning the contact angles of the channel walls.

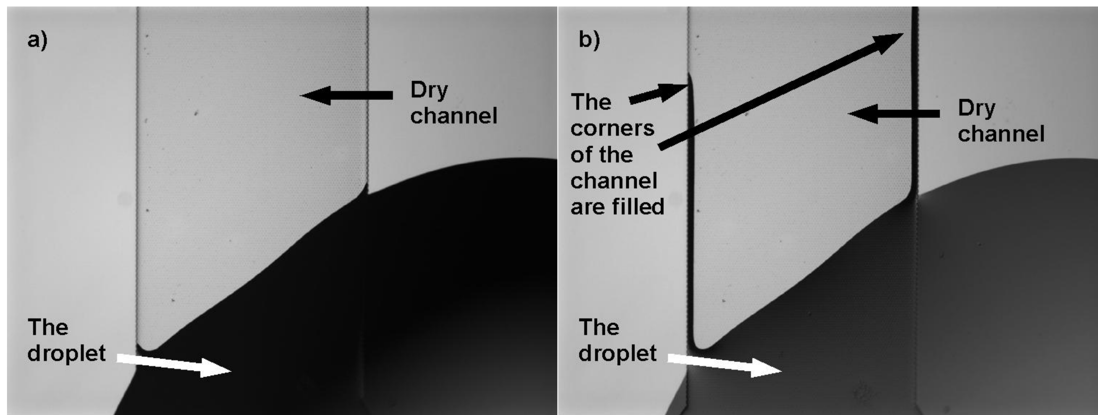

Figure 12. Capillary filling of a lidless silicon channel [Publication III]. a) Application of a water droplet. b) The water only fills the intersections of the bottom and side walls. The horizontal surface contact angle was measured to be 47° +- 2°. The channel width was 1 mm and depth 22.5 µm.

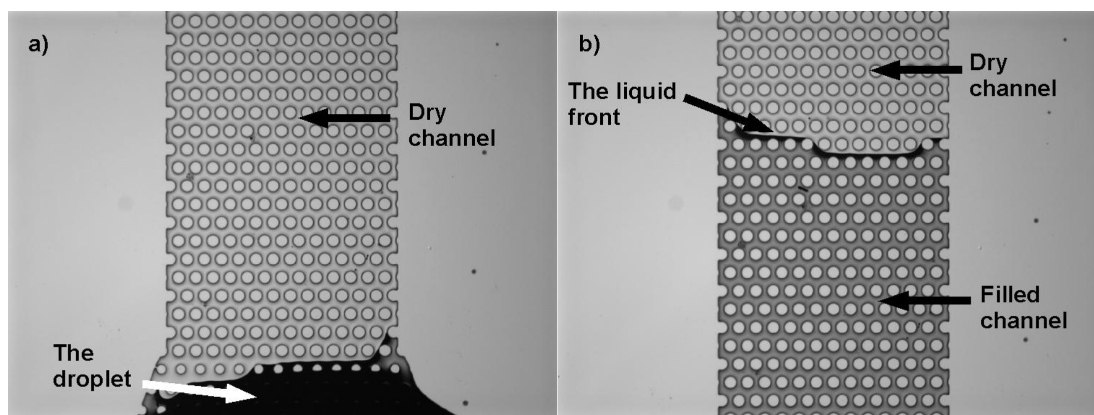

Figure 13. Capillary filling of a lidless silicon pillar channel [Publication III]. a) Application of a water droplet. b) The whole channel is filled because the channel has a greater hydrophilic surface area. The horizontal surface contact angle was measured to be 47° +- 2°. The channel width was 1 mm and depth 22.5 μm.

Silicon micropillar array electrospray ionization (μPESI) chip

Capillary filling is a convenient way to transport the sample in silicon microchannels because electroosmotic sample transport cannot be utilized and the use of pumps also necessitates the use of cumbersome fluidic connectors. This is especially the case for micropillar filled channels that provide sufficient capillary pressure even without a coverlid. In addition, the fabrication of a lidless device is easier, because bonding is not required. A lidless channel which is filled with micropillars and ends in a sharp tip can be utilized as an ESI interface for mass spectrometry. Figure 14 presents the measurement setup of the system.

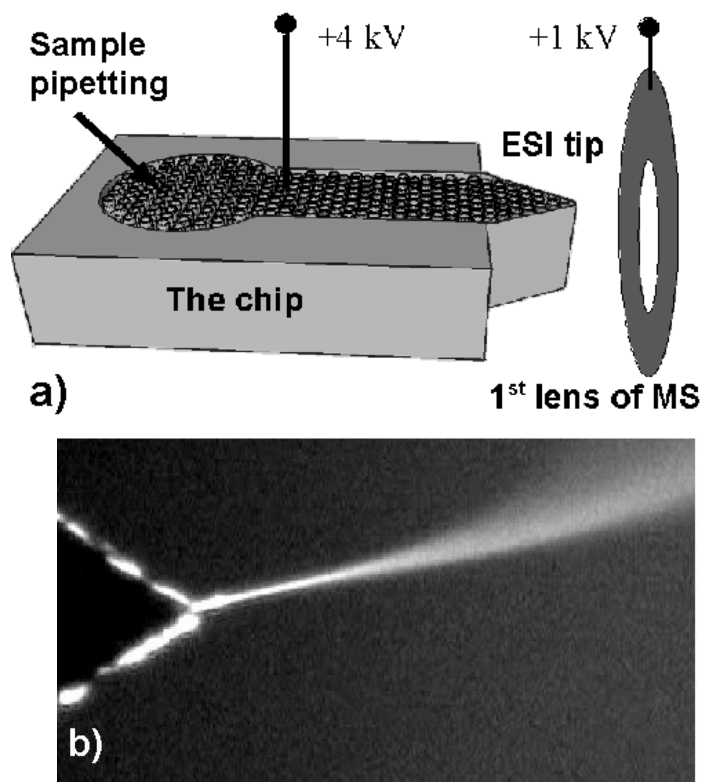

Figure 14. μPESI chip in operation. a) Schematic illustration of the measurement setup. b) A photograph of the electrospray generated from the silicon chip.

The fabrication of μPESI chips requires two separate DRIE steps: one for the sharp ESI tip and another for creating the micropillar channel. Patterning the second mask level after the first DRIE step is impossible because the photoresist cannot be spun on a through etched wafer. Therefore, a peeling mask technique was used. A thermal silicon dioxide (SiO_2) layer was grown on the wafer and subsequently patterned in the shape of pillar channels (Figure 15a). An aluminum oxide (Al_2O_3) layer was atomic layer deposited on the patterned SiO_2 layer. The second lithography step defined the ESI tips at the ends of the channels. Both the Al_2O_3 and SiO_2 were etched to expose the silicon for through-wafer etching (Figure 15b and c). Because aluminum oxide tolerates fluorine based plasmas extremely well, it was used as an etch mask during the through-wafer DRIE step, which defined the ESI tip.

As discussed earlier, the sharpness of the ESI tip is crucial for the performance of the chip [96]. By performing the through-wafer DRIE step in two parts, it is possible to create a three-dimensionally sharp ESI tip. First, an anisotropic, fairly shallow silicon DRIE was performed (Figure 15d). Then silicon dioxide was deposited on the wafer by plasma enhanced chemical vapor deposition (PECVD) (Figure 15e). Even though the SiO_2 layer thickness on the vertical sidewalls was thinner than on the horizontal surfaces, it was possible to selectively remove the deposited PECVD oxide from horizontal surfaces using anisotropic RIE of silicon dioxide (Figure 15f). Similar sidewall passivation schemes have also been used elsewhere [Publication V, 113]. Afterwards, the through-wafer DRIE step was continued using a smaller proportion of oxygen in feed gas, which resulted in negatively sloped sidewall profiles (Figure 15g). Because of the oxide on the sidewall, the protected part of the ESI tip was undercut and a three-dimensionally sharp tip was formed.

After through-wafer etching, the alumina mask was removed to expose more silicon and an underlying, patterned silicon dioxide mask (Figure 15h). The alumina was etched away using phosphoric acid without harming the silicon or silicon dioxide. The second DRIE process created the micropillar filled channels, after which the SiO_2 mask was removed. The hydrophilicity of the chips can be tuned by oxidizing the silicon surface, e.g., in an oxygen plasma or RCA-1 solution. Different chemical treatments result in slightly different contact angles. The analytical power of the fabricated μPESI chips is shown in refs. [Publication III, 114].

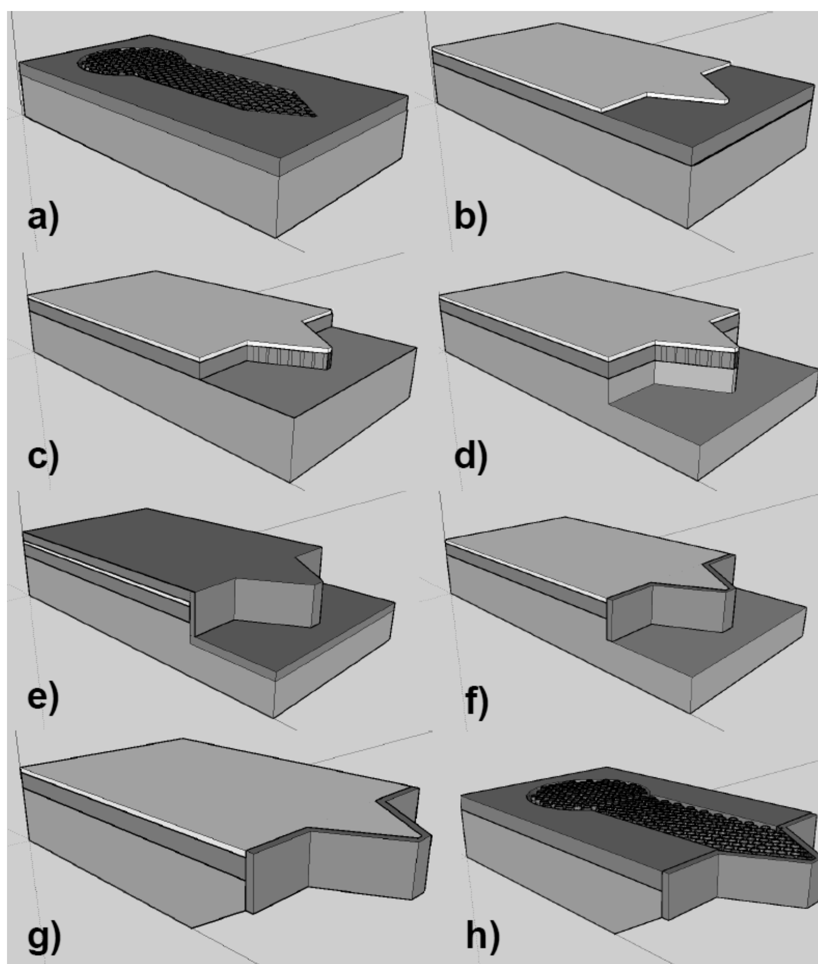

Figure 15. The fabrication of a μPESI chip with 3D sharp tip. The gray bottom layer is silicon substrate; the dark gray middle layer SiO_2 and light gray top layer Al_2O_3. Photoresist layers are excluded from the figure. See text for details [Publication III]. a) Patterning of SiO_2 mask. b) Deposition and patterning of Al_2O_3 on top of SiO_2 mask. c) Etching of SiO_2 from the tip of the chip. d) Shallow anisotropic DRIE of silicon step. e) Deposition of thin PECVD oxide layer. f) Removal of the oxide from horizontal surfaces using anisotropic RIE process. g) Second DRIE of silicon under more isotropic conditions. h) Removal of Al_2O_3 mask. The oxide mask that is revealed is utilized in a final DRIE step to create the pillar channel.

SU-8 micropillar array electrospray ionization chip

Similar μPESI chips can also be fabricated from SU-8. The fabrication starts with an oxidized silicon wafer that serves only as a mechanical support. The first layer of SU-8, which created a 70 μm thick floor, was spun onto the substrate and exposed to form the bottom part of the sharp electrospray tip. Before the non-cross linked SU-8 was developed, another 70-μm thick SU-8 layer was spun on top of the first one. The second layer was exposed in order to create the channel with micropillars and the ESI tip. Then both SU-8 layers were simultaneously developed. The SU-8 chips were released from the substrate in 50 % hydrofluoric acid. Finally, the chips were treated in oxygen plasma in order to decrease the water contact angle of the SU-8 surface to below 45°. A photograph of the fabricated chip and the scanning electron microscope (SEM) image of the electrospray tip of the chip are shown in Figure 11. Different kinds of SU-8 ESI chips have been fabricated in a similar manner in ref. [108]. The advantage of SU-8 μPESI chips over silicon μPESI chips lies in their cheaper, faster and simpler fabrication process. Particularly, etching through the silicon wafer to create a sharp electrospray ionization tip at the end of the micropillar channel is a

cumbersome process and the SU-8 process avoids this step [115]. The disadvantages of SU-8 chips include higher background in mass spectra, worse limit of detection, and a more constricted temperature range.

3.3 Dry fabrication of suspended microstructures

3.3.1 Alumina membranes

Suspended membranes [Publication IV, 37, 116] and micro- and nanodevices [Publication V, 41, 117-128] have been extensively studied due to their unique thermal properties. The air surrounding the suspended membrane or device thermally isolates it from the substrate. Thin membranes have been utilized as thermally insulating platforms for devices working either at high [116] or low [37] temperatures. Silicon rich SiN_x is the most common membrane material due to its sufficient mechanical strength, low residual stresses and low thermal conductivity. The nitride membranes are released by etching through the silicon wafer from the backside. The component is fabricated on top of the membrane before or after the release etch [Publication IV, 37, 116,]. Good thermal isolation decreases the device's power consumption [116] and enables fast thermal ramping [Publication V].

Smooth, continuous membranes are fabricated by depositing the membrane material on the topside of the polished silicon wafer and releasing it by etching through the wafer from the backside [Publication IV, 37, 116,129]. The fabrication of smooth, patterned membranes does not require through-wafer etching if the membrane material is inert during the sacrificial etching of the underlying silicon substrate. In this case, the patterned membrane can be released by the isotropic etching of silicon from the front side of the wafer [Publication IV, 129]. Obtaining good selectivity between silicon nitride and silicon is difficult in cryogenic DRIE. However, atomic layer deposited alumina has extremely high selectivity [Publication II, 84, 85], and it is well suited to membrane applications due to its good mechanical properties and low residual stresses [Publication IV, 129]. Patterned alumina structures released in isotropic SF_6 plasma are shown in Figure 4. The perforated alumina membranes can be used to support metallic devices as shown in Figure 16. The metallic device was patterned onto the perforated alumina film before the isotropic plasma release. The electrical characteristics of an aluminum heater on top of a released and non-released alumina membrane are compared in Figure 17. The heater on top of the non-released membrane shows Ohmic behavior until the current limit sets in. The current density increases in a linear fashion with the voltage and the heat that is generated is conducted to the silicon substrate. The aluminum heater on the released membrane shows a similar behavior at low voltages. After 300 mV, the slope of the released heater starts to decrease because the resistance of the heater increases with temperature. The released heaters were thermally destroyed at 950 mV, which indicates a bridge temperature of 650°C. Similar suspended aluminum heaters cannot be fabricated without the alumina support due to residual stresses in the sputtered aluminum film.

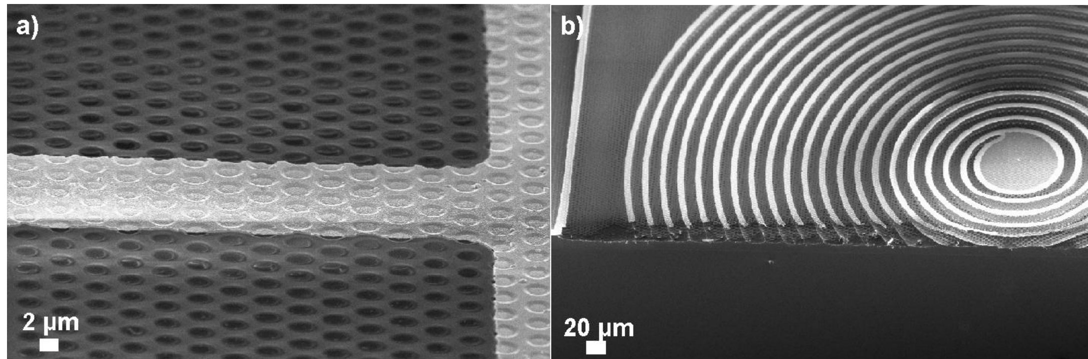

Figure 16. Aluminum structures on a released alumina membrane [Publication IV]. a) A thermally insulated aluminum heater. b) An aluminum spiral, demonstrating that large structures can be fabricated on free-standing membranes.

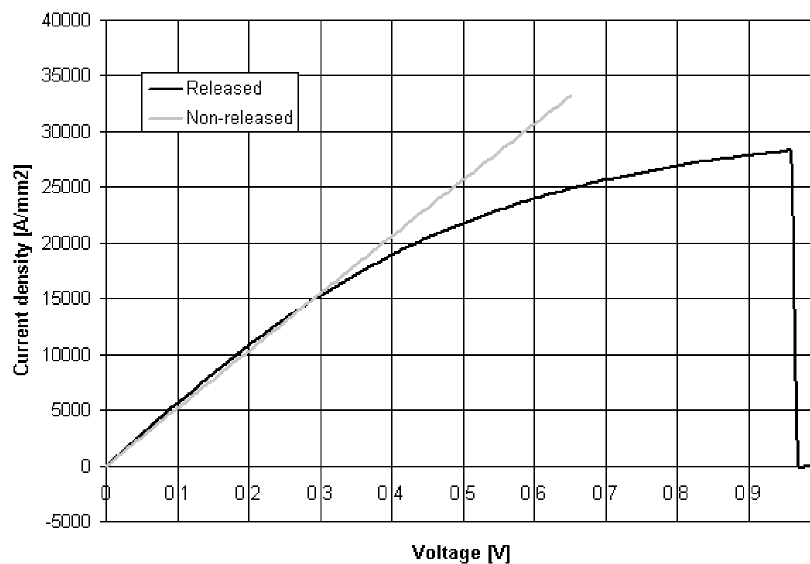

Figure 17. Current density-voltage curves for aluminum heaters on top of released and non-released alumina films [Publication IV]. The curves show that the heater on top of the released alumina membrane is thermally well-isolated from the substrate.

The fabrication of nanocorrugated alumina membranes is also possible due to fully conformal deposition profiles enabled by ALD [Publication IV]. The main fabrication steps for nanocorrugated membranes are presented in Figure 18. The fabrication was begun with the creation of nanostructures on a double side polished silicon substrate. Two different nanocorrugations were used: black silicon nanospikes and polymeric nanobeads. The low deposition temperature of alumina (80 °C) also permits the use of materials with low melting points, such as polymers. The nanostructured surfaces were coated with an atomic layer deposited alumina film, which was then protected by a photoresist layer. An aluminum layer was sputtered onto the backside of the wafer and it was patterned using lithography and wet etching. After the removal of the photoresist layers, the patterned aluminum film on the backside of the wafer acted as an etch mask during the through-wafer etch process, which released the nanocorrugated membranes.

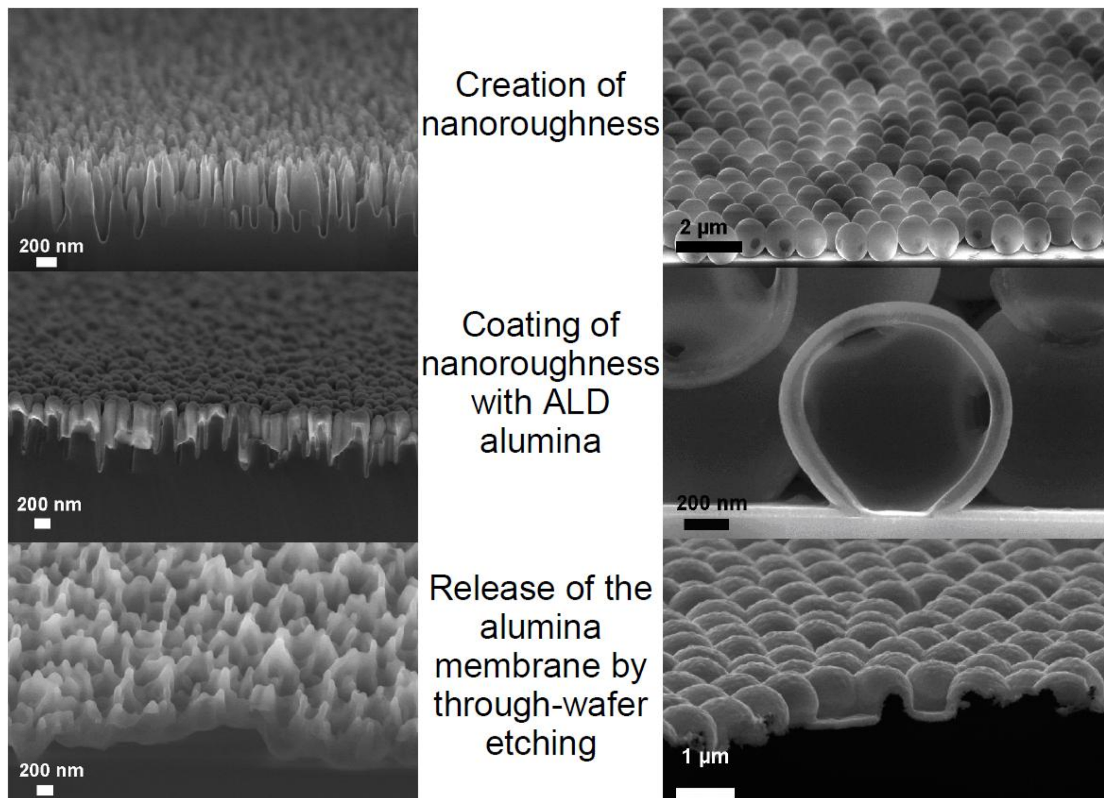

Figure 18. Fabrication of nanocorrugated suspended alumina membranes [Publication IV]. The use of two different nanocorrugations is demonstrated.

3.3.2 Thermal silicon actuators

Suspended silicon devices do not require supporting membranes because single crystalline silicon is free from residual stresses and it has adequate mechanical properties [Publication V, 41, 122, 125]. Various process flows have been used to create suspended silicon microdevices. The first devices were made of poly-silicon and covered by silicon nitride, which allowed KOH to be used for the wet release of the devices from the front side [119, 121]. The properties of poly-silicon are inferior to those of single crystalline silicon, and they change drastically when heated due to grain growth and oxidization. Crystalline silicon also oxidizes when it is heated, but otherwise it is much more stable material. Silicon nitride coating protects silicon from oxidation. To be able to fabricate suspended silicon devices that have reproducible properties, single crystalline silicon must be used. The etch rate difference between highly doped p-type silicon and intrinsic silicon in KOH and EDP has been exploited with the fabrication of free-standing highly doped silicon devices [41, 122]. This fabrication method is limited to highly doped devices. Furthermore, the dimensional control of devices is difficult because also highly doped silicon is slowly consumed during release etching. Therefore, the dimensions of the devices cannot be very accurately defined and the surfaces of released structures are rough. The use of SOI wafers opens up new possibilities. Structures can be released by the sacrificial etching of a buried oxide layer (BOX) [41, 126] or by through-wafer etching from the backside of the wafer that automatically stops at the BOX [125]. The sacrificial etching of the BOX introduces new problems for the release. The gap between the device and the substrate is defined by the thickness of the BOX, which is limited to a few micrometers. This small gap can cause stiction, and the actuated device consumes more power because of the conduction of heat from the device to the substrate

through the small air gap [Publication V, 121]. On the other hand, using through-wafer etching to release the device is cumbersome, as it requires double sided lithography and etching through the handle wafer, which is time consuming.

A novel way to produce suspended single crystalline silicon devices with accurate dimension control is presented in Figure 19 and described in detail in Publication V. The fabrication process uses a similar sidewall passivation scheme as in refs. [Publication III, 113]. After defining the bridge and the anchor areas on the silicon device layer (Figure 19d), a thin PECVD oxide layer was deposited on the wafer (Figure 19e). Due to the PECVD technique's poor conformality, the layer thickness on the sidewall was much thinner than on the horizontal surfaces. However, by using a highly anisotropic RIE process, it was possible to selectively remove the oxide from horizontal surfaces and the device sidewalls remained passivated (Figure 19f). After passivation, all sides of the bridge were covered by silicon dioxide and the device could be released by the isotropic plasma etching of the handle wafer. The release did not change the bridge's dimensions and the gap between the device and the substrate could be chosen freely. This process flow also circumvented the use of double-sided lithography, through wafer-etching and stiction. The fabricated free-standing thermally actuated silicon devices are shown in Figure 20.

Due to the low thermal mass of the suspended silicon microdevices, a short and low-voltage pulse is all that is needed to raise the temperature of the device to close the melting point of silicon (1414°C). At high temperatures, silicon emits light at visible wavelengths, although most of the light is emitted at the infrared wavelengths. Thermal expansion also substantially deflects the suspended beams [Publication V, 127]. On the other hand, the device cools fairly quickly. The main heat loss mechanism is conduction through the anchoring points of the device [127]. Rapid heating and cooling allow for fast thermal cycling. Due to these intriguing thermal properties of suspended silicon microdevices, they have a wide range of applications. They have been used, for example, as infrared emitters or microlamps [119-121], large stroke actuators [124], RF-MEMS switches [123], and micro reactors [126].

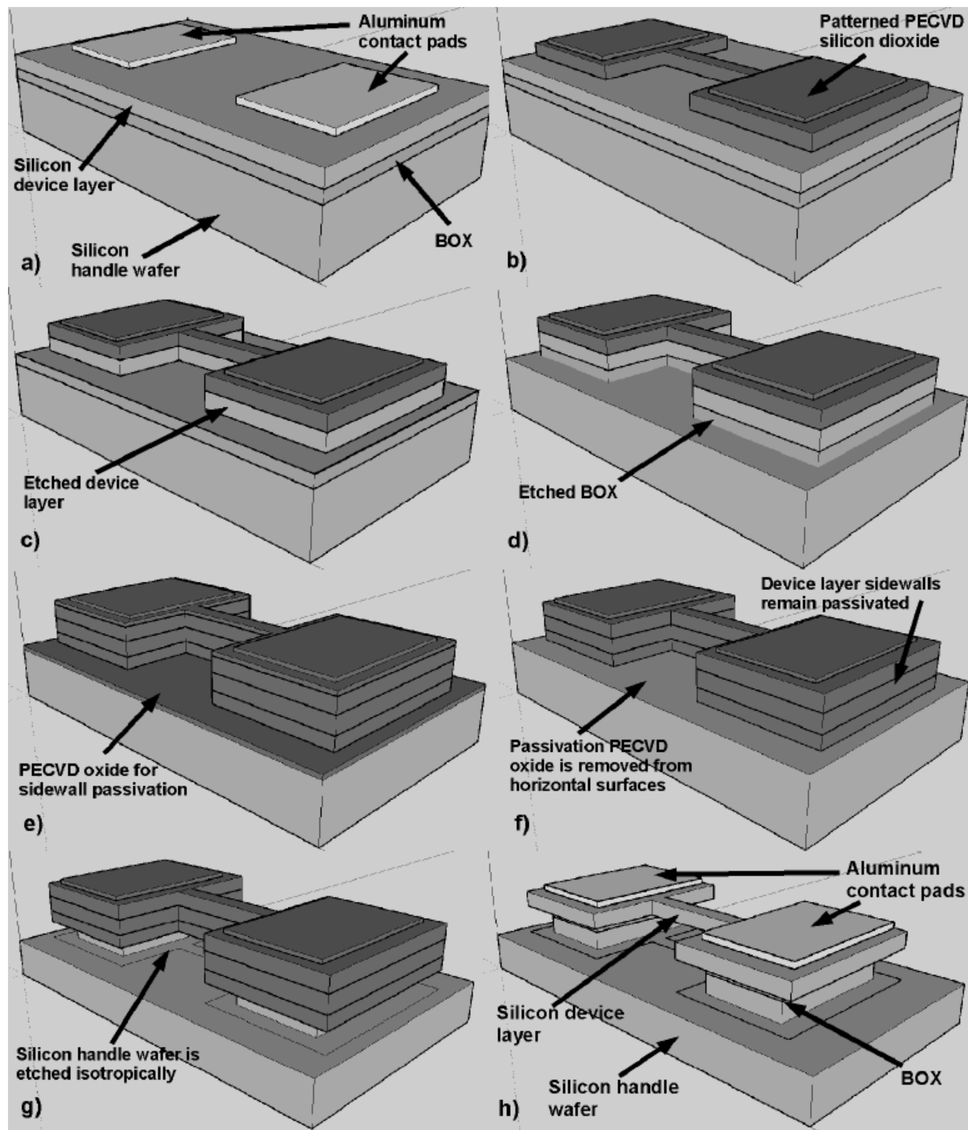

Figure 19. The fabrication process of a suspended crystalline silicon microbridge [Publication V]. a) Electrical contacts on an SOI wafer. b) PECVD oxide deposition and patterning. c) DRIE of the silicon device layer. d) RIE of the BOX layer. e) PECVD of oxide for the bridge sidewall protection. f) Anisotropic RIE of the protective oxide layer from the horizontal surfaces. g) Isotropic dry release of the bridge. h) Optional removal of the protective oxide layers. Photoresist layers excluded from the figure.

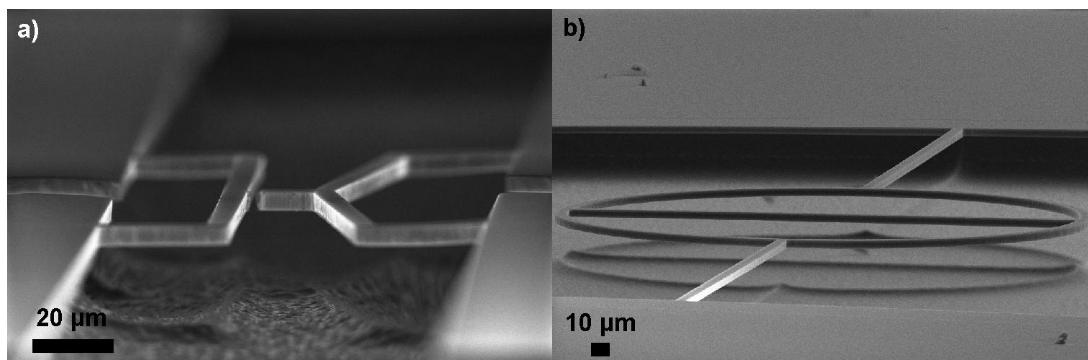

Figure 20. Suspended silicon microdevices fabricated using the process flow described in Figure 19 and Publication V. a) A thermally actuated silicon lateral stroke actuator. b) A ring-shaped stress test bridge.

3.4 Fabrication of silicon nanopillars

3.4.1 Silicon nanopores and pillars

Nanostructured surfaces have an enormous surface area when compared to smooth ones. A large amount of light at visible wavelengths is also absorbed by nanostructured silicon and, therefore, it typically appears as a black surface to the naked eye. A large surface area is advantageous in fluidic applications where strong surface-fluid interactions are desirable. Two of the most obvious nanostructures used to increase the surface area are pillars and pores. It has been proposed that a micro- or nanopillar array machined inside the separation channel of a miniaturized liquid chromatography chip could replace bead based separation columns, due to the huge surface area of the pillar array [130]. On the other hand, porous silicon was the first material utilized in desorption/ionization with silicon mass spectrometry because its exceptionally high surface area can be used to trap the analyte molecules. Porous silicon also efficiently absorbs the UV wavelengths of light [93]. It has subsequently been demonstrated that surfaces with nanopillar structures are even better suited to DIOS-MS [131].

Nanoporous silicon is commonly fabricated by electrochemical etching [132, 133]. Pore positioning is typically random, but the size distribution is fairly narrow. By using pre-structured wafers, it is possible to attain ordered pore arrays. Pore diameters can be fine tuned by changing the etchant, applied voltage, illumination intensity and the type and doping level of the substrate [132]. Extremely high aspect ratio nanopores can be economically produced by using electrochemical etching. Nanoporous silicon can also be fabricated with the help of lithography and DRIE. The nanopores shown in Figure 7b were fabricated using nanoimprint lithography combined with cryogenic deep reactive ion etching. Furthermore, block copolymer and nanosphere masks combined with DRIE have been used to produce nanoporous silicon. Porous silicon is utilized in solar cells, low temperature oxidation, fabrication of SOI wafers, wafer thinning, and chemical analysis.

Fabrication of nanopillars typically requires DRIE of silicon. Using nanoimprint lithography or electron beam lithography combined with DRIE, it is possible to create accurately defined high aspect ratio pillars [134, 135]. The use of block copolymers [136] and nanosphere lithography [137] with DRIE also gives some control over the placing of the pillars. If the only functions of nanopillars are to increase the surface area and light absorption, a random nanopillar array functions as well as an ordered one and emphasis should be on throughput instead of regularity. The next two sections present two extremely rapid fabrication methods for random silicon nanopillar arrays. Both methods are suitable of for wafer-scale manufacturing.

3.4.2 Black silicon

The most straightforward method for fabricating a random silicon nanopillar array is to etch silicon under overpassivating conditions without a mask [Publication VI, Publication VII, 53, 66, 138]. In cryogenic etching, the growth rate of the passivation layer is determined by the wafer temperature and the oxygen content in the SF_6/O_2 plasma. The removal rate is mainly dependent on the ion energies and ion flux, because sputtering is used as the main mechanism for removing the passivation layer. Therefore, overpassivation is achieved by using low temperature, high oxygen flow

and a low bias voltage [138]. The pulsed Bosch process also results a in similar nanopillar structure when it is utilized in overpassivation regimes [139, 140].

The exact mechanism that initiates the formation of a random silicon nanopillar array during cryogenic etching is not known. This kind of nanopillar array can be known as black silicon [53], columnar microstructures [138], silicon nanoturf [141] and silicon nanograss [Publication VII]. Characteristically, some silicon is always etched before the nanopillars start to form. Evidently, the etching stops in small areas at some point of the process while it continues elsewhere. It has been suggested that redeposition etch products (SiF_x) could create a more etch resistant passivation layer [138]. This could result in a non-uniform passivation layer removal rate on horizontal surfaces, and the formation of nanopillars. Nanopillars are typically around 100-300 nm wide, and have aspect ratios up to 5:1. Sidewalls slopes are slightly positively tapered as seen in Figure 21. The nanopillar dimensions can be tuned to some extent by changing the process parameters [138].

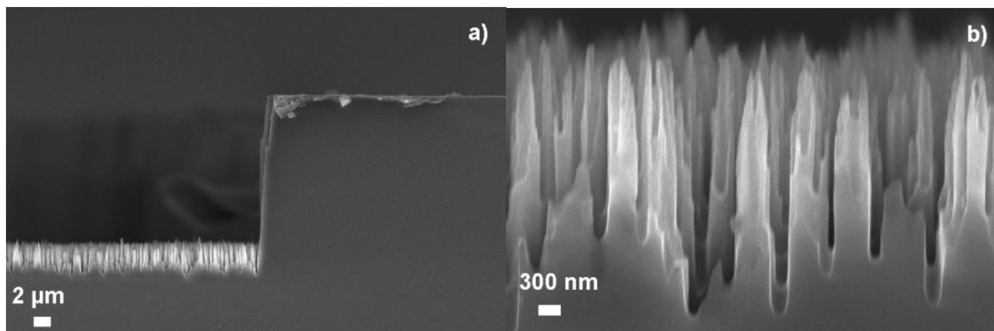

Figure 21. Black silicon formed using a cryogenic DRIE process in an over-passivation regime [Publication VI]. a) Some of the silicon is always etched before nanopillars start to form. b) Close-up view of nanopillars.

Smooth trench bottoms and vertical sidewalls are normally desirable and black silicon is considered to be an unwanted result. Optimal etch conditions for vertical sidewalls lie very close to an overpassivation regime. Therefore, black silicon was originally used for determining optimal etch parameters [53]. The large surface area and good light adsorption properties of black silicon, have subsequently been exploited. Some examples are solar cells [142], the geometric enhancement of hydrophobic effects [Publication VII, 141], increasing bonding strength [139] and chemical analysis [Publication VI, 66]. Furthermore, all the products produced by a certain company are based on black silicon [143].

The creation of black silicon is easy and fast, because the process is maskless and the required etch time is only a few minutes. Using lithography to protect some parts of the wafer, black silicon can be formed only in the desired locations. Some drawbacks of black silicon nanopillars include positive sidewall tapers and the fact that some of the silicon is etched before the black silicon forms. Therefore, the top surface of larger structures that are fabricated at the same time as black silicon nanopillars will be at a higher level, as seen in Figure 21.

3.4.3 Silicon nanopillars defined by liquid flame spray deposited silica nanoparticle agglomerates

As discussed in section 2.1.4 nanoparticles can be used as etch masks for the DRIE of silicon if the particle material is stable under etching conditions. Silicon dioxide is a commonly used mask material with a low etch rate. Therefore, silica nanoparticles can be used to define silicon nanopillars if the particles can be conveniently introduced onto the substrate.

Flame spray based methods are widely used in the production of nanoparticles. With the liquid flame spray (LFS) technique [144], a liquid precursor is sprayed into a turbulent flame where nanoparticles are formed. When silica nanoparticles are formed, tetra–ethyl–ortho–silicate (TEOS) in a 2-propanol solution is used as a precursor, which is sprayed into a turbulent H_2/O_2 flame [145]. With LFS, the higher mass feed rate of the precursor solution typically results in a larger particle size. However, high melting point ceramic compounds such as silica form nanoparticle agglomerates instead of individual particles. The sizes of the agglomerates are greater than the primary particle size of 10 nm [145]. The resulting silica particle agglomerates can be deposited onto the wafer by moving the substrate through the turbulent flame. The particle agglomerates deposit onto the wafer due to thermophoresis and Brownian diffusion, and van der Waals forces cause them to adhere to the surface. The concentration of the nanoparticle agglomerates is not uniform throughout the wafer; it is highest in the sector where the flame touches the substrate and it decreases as the distance from the point where the flame touched the substrate increases [Publication VI].

After the nanoparticle agglomerate deposition, cryogenic deep reactive ion etching of silicon is performed. The silica agglomerates act as etch masks and pillars are created. It is possible to combine microstructures defined by optical lithography with nanopillars defined by LFS deposited nanoparticle agglomerates. Firstly, a silicon dioxide layer is deposited onto the substrate and patterned with the help of optical lithography and RIE. Then, silica agglomerates are deposited and the wafer is etched. The wafer and the flame are in contact with each other during the LFS deposition. Therefore, the mask material used to create micro patterns must be able to tolerate high temperatures. The whole nanopillar fabrication process is schematically illustrated in Figure 22.

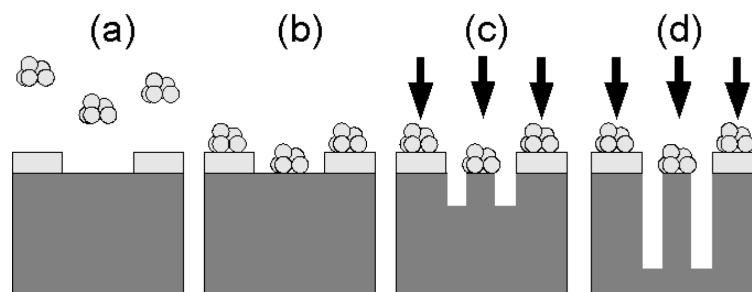

Figure 22. Fabrication of LFS silica nanoparticle agglomerate masked silicon nanopillars [Publication VI]. a) LFS production of the agglomerates. b) The agglomerates adhere to the SiO_2 masked silicon substrate. c) Cryogenic DRIE of silicon and the formation of nanopillars. d) The heights of the nanopillars are dependent on etching time. Other nanopillar dimensions are dependent on the agglomerate projection area.

The small size of a nanoagglomerate sets high requirements for the anisotropy and selectivity of the DRIE process. SEM images of simultaneously created micro- and nanopillars and close-up view of nanopillars are shown in Figure 23. The aspect ratios of pillars are around 20:1 and their sidewalls are vertical.

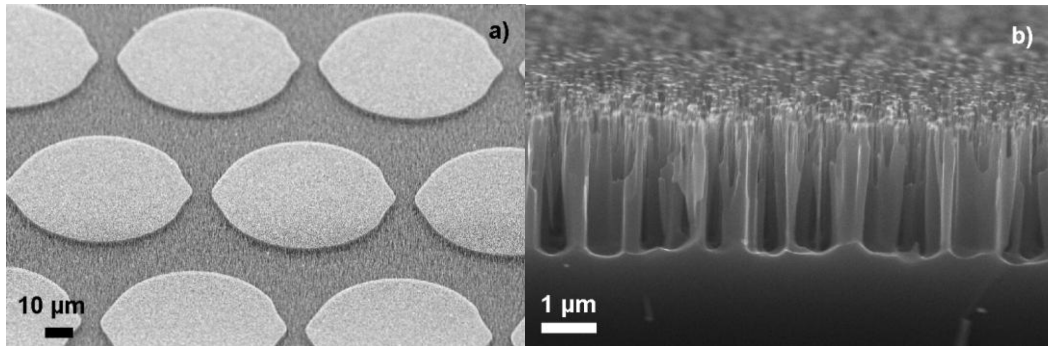

Figure 23. SEM images of LFS masked silicon nanopillars. a) An overview image of 60 μm diameter micropillars defined by optical lithography, surrounded by LFS masked nanopillars. b) Close-up view of LFS masked nanopillars.

3.5 The chemical modification of nanostructured silicon surfaces

3.5.1 Wetting of surfaces

A liquid droplet placed on a solid surface forms an angle of contact which is independent of the size of the droplet. This angle is known as the contact angle θ and it is defined by the surface energies of the solid-vapor, solid-liquid and liquid-vapor interfaces when vapor and liquid phases are in thermodynamic equilibrium. This can also be seen from the equation (1). The thorough review of the wetting of solids with liquids can be found in ref. [146].

If the contact angle of a water droplet is less than 90°, the surface is termed hydrophilic, whereas surfaces that exhibit contact angles greater than 90° are said to be hydrophobic. Surfaces that have angles close to zero are sometimes called ultra hydrophilic or completely wetting. Water droplets spread and form a thin aqueous film over these types of surfaces. Conversely, surfaces with contact angles close to 180° are referred to as super- or ultrahydrophobic. Typically, a low contact angle hysteresis and low sliding angles are also conditions that the surface has to meet before it can be considered as ultrahydrophobic [147]. Contact angle hysteresis is defined as the difference between advancing and receding contact angles. Sliding angle is the term used for the tilting angle required for a droplet to slide on a surface as a result of gravity.

The contact angle between a water droplet and the solid surface can be tuned by changing the chemical and physical composition of the surface. A flat, clean silicon surface has a contact angle of around 65°. One way of making the surface more hydrophilic is by oxidizing it. Conversely, more hydrophobic surface properties can be attained by depositing a Teflon-like fluoropolymer film on top of the silicon surface. Physical micro- or nanoroughness changes the wetting behavior by enhancing the intrinsic properties of the flat surface. A nanostructured hydrophilic surface, such as oxidized black silicon, is even more hydrophilic than a flat oxidized silicon surface. The water droplet fills the cavities between the pillars and wets the entire surface.

This kind of wetting is also known as Wenzel type behavior. On the other hand, if a nanotextured surface is intrinsically hydrophobic, the water droplet is pinned on the nanostructures. The air trapped between the droplet and the nanostructures acts as 180° contact angle material, making the surface more hydrophobic. The droplet assumes the so-called Cassie state. This kind of method is repeatedly exploited in the fabrication of super- and ultrahydrophobic surfaces [Publication VII, 66, 141, 147-149]. Oxidized black silicon is completely wetting, whereas fluoropolymer coated black silicon has a contact angle of around 170° and is ultrahydrophobic [Publication VII].

3.5.2 The fabrication of accurately defined completely wetting domains on ultrahydrophobic surfaces

The fabrication of super- and ultrahydrophobic surfaces has attracted a considerable amount of attention lately because of their applications in self-cleaning surfaces [150], analytical devices [66] and the reduction of friction in microfluidic channels [141]. Completely wetting surfaces have not attracted similar levels of interest, even though they are well known. Still, surprisingly few studies exist where completely wetting and ultrahydrophobic domains have been fabricated on the same surfaces [Publication VII, 151]. The fabrication of such a surface with lithographic accuracy, using only standard clean room processes, is outlined in Figure 24. The process was started with the creation of black silicon by the maskless deep reactive ion etching of silicon under overpassivating conditions. This black silicon was then coated with a hydrophobic fluoropolymer layer. The fluoropolymer deposition was performed in CHF_3 plasma using a RIE. The completely wetting areas were defined on the wafer by lithography. Spinning photoresist onto rough ultrahydrophobic surface may be problematic and the use of thin photoresists should be avoided. After the lithography, the fluoropolymer layer is etched in O_2 plasma, which also oxidizes the underlying silicon surface to make it completely wetting.

Spinning the photoresist onto the hydrophobic surface can be avoided by using the lift-off patterning of the fluoropolymer layer. After creating the black silicon, the surface was oxidized and the negative of the original photoresist image was patterned on the completely wetting black silicon. Subsequently the fluoropolymer was deposited. When the photoresist was removed, the fluoropolymer on top of the photoresist was also lifted-off to reveal the underlying completely wetting surface. Both the lift-off and the etching processes produced identical surface properties. Therefore, the lift-off process is more reliable, but the etching process worked as well in the case of the fairly thick photoresists (> 5μm).

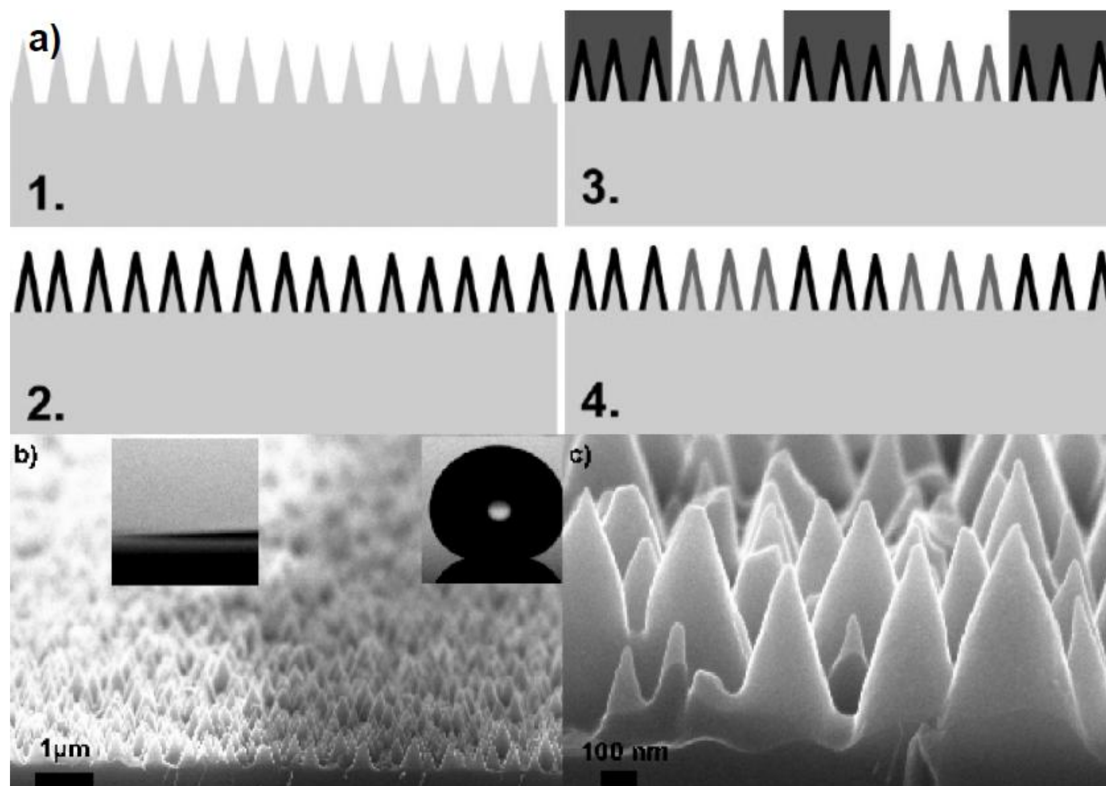

Figure 24. Chemical surface modification of a nanostructured silicon surface [Publication VII]. a) Fabrication of surfaces with a high wettability gradient. 1. Creation of black silicon. 2. Deposition of fluoropolymer. 3. Lithography, removal of fluoropolymer and the oxidation of underlying black silicon in oxygen plasma. 4. Removal of the photoresist in acetone. b) The edge of oxidized and fluoropolymer coated silicon nanograss. The contact angles of differently coated materials are also shown. c) Close-up view of oxidized black silicon.

The fabrication of completely wetting and ultrahydrophobic areas side by side makes it possible to passively manipulate droplet behavior. A high wettability gradient allows droplet shapes to be tailored freely. When a droplet is applied onto a completely wetting domain, which is surrounded by an ultrahydrophobic surface, the droplet copies the shape of the hydrophilic area accurately as demonstrated in Figure 25a.

High wettability gradients also allow droplets to be passively split. A typical droplet splitter has a round hydrophilic source which is surrounded by a very narrow ultrahydrophobic barrier. A hydrophilic target, where another droplet is created, surrounds the barrier. The first droplet is applied on the source. The size of the droplet is increased until it must also occupy the barrier's space. The droplet splits if its size is increased further until its edge touches the target. Finally, one droplet sits on the source and the other one on the target. The splitter design is shown in Figure 25b.

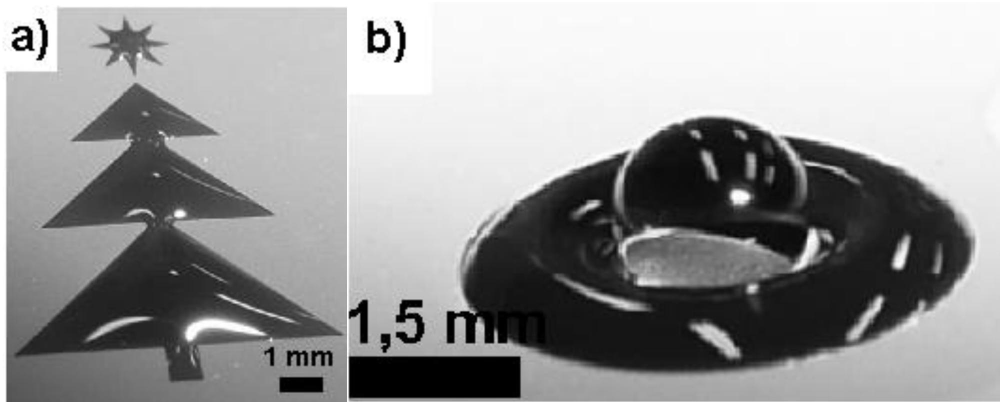

Figure 25. Complex droplets on chemically modified silicon nanograss. a) Dyed droplets creating a holiday tree shaped droplet, demonstrating obtuse and acute angled droplet shapes. a) A dyed water droplet surrounded by a ring shaped droplet. A narrow hydrophobic barrier isolates the droplets. This same geometry can be utilized as a droplet splitter [Publication VII].

3.6 Etching parameters for different processes

Previous sections have given several examples how cryogenic DRIE can be utilized in the fabrication of devices. Each of the anisotropic, isotropic, and overpassivation regimes have their own applications. Table 2 summarizes the most important etch processes utilized in Publications II-VII.

Table 2. Process parameters for different kinds of cryogenic DRIE processes. The temperature used by all processes, with the exception of release, is -110°C.

Process name	ICP power [W]	CCP power [W]	O_2 flow (sccm)	SF_6 flow (sccm)	Pressure [mTorr]	Etch rate [µm/min]*
Baseline [Publication II]	1000	2	6	40	10	4.3
Nanostructures [Publication VI]	700	3	6	38	9	1
Through wafer [Publication II]	2000	3	15	100	19.5	7.6
Release [Publication V]	2000	3	-	100	50	7
Black silicon [Publication VI]	500	3	18	38	9	Not measured

*Etch rate values are only indicative. The actual etch rate of the process is heavily dependent on the loading of the wafer, aspect ratio of the structure and structure size.

The *Baseline* process is typically utilized when anisotropic etch profiles are required [Publication II, Publication III, Publication V, Publication VI]. At the temperature of -110°C, the process parameters result in a SiO_xF_y layer thickness that ensures anisotropic etch profiles. At higher temperatures, sidewall passivation is not as efficient and sidewall profiles turn isotropic [Publication II]. Therefore, all anisotropic processes must be run at cryogenic temperatures.

In order to create high aspect ratio nanostructures, undercutting must be further minimized. The *Nanostructures* process utilizes a lower ICP power and SF_6 flow rate than the *Baseline* process in order to reduce the densities of ions and radicals

[Publication VI]. Therefore, the passivation layer is etched at lower rate. The process pressure is also slightly lower than that of the *Baseline* process, thus reducing the angular distribution of the ions and improving the anisotropy of the process. The disadvantage of the *Nanostructures* process is the low etch rate.

High etch rate and selectivity are typically required when deep or through wafer structures are etched. The *Through wafer* process maximizes the etch rate of silicon at the expense of sidewall quality [Publication II, Publication III, Publication IV]. The densities of free radicals and ions are maximized by using ICP powers and SF_6 flow rates that are as high as possible. Oxygen flow is also increased to maintain the same SF_6/O_2 ratio as used in *Baseline* process. Due to the increased total gas flow into the process chamber, the vacuum pump cannot maintain a process pressure of 10 mTorr. Because of the high densities of free radicals and ions, the etch rates of the silicon and passivation layers increase. Due to a higher process pressure, the angular distribution of ions also increases, thereby increasing the number of collisions between the ions and the trench sidewalls. Therefore, the sidewall quality of features etched using the *Through wafer* process is inferior. Masking materials are typically chemically inert and the main etching mechanism is sputtering. Therefore, the etch rate of the masking material is not substantially higher in the case of the *Through wafer* process.

The *Release* process is utilized to release suspended structures and, therefore, the lateral etch rate is maximized [Publication IV, Publication V]. Unlike the other processes, the *Release* process is not temperature sensitive and it is typically performed at room temperature. The second big difference is that the *Release* process utilizes pure SF_6 plasma instead of an SF_6/O_2 mixture. The passivating SiO_xF_y layer cannot form without oxygen. Otherwise the process is quite similar to the *Through wafer* process. A high ICP power and SF_6 flow are used to attain a high plasma density and etch rate. The lateral etch rate is further increased by increasing the angular distribution of ions through the use of a higher process pressure.

The *Black silicon* process is a maskless process that is used to create silicon nanograss [Publication IV, Publication VI, Publication VII]. This process utilizes the overpassivation regime of the cryogenic DRIE process. Therefore, O_2 flow is increased considerably. Otherwise the process parameters are similar to the *Nanostructures* process, to ensure a low etch rate of the passivation layer and the formation of black silicon.

4 Conclusions and future outlook

This thesis presents the most important results obtained by the author during the 2006 – 2008 period. The aim of the work was to create practical silicon etching processes using the cryogenic DRIE tool acquired for our clean room. The capabilities of the new tool were soon realized and the etching processes that were developed were applied to the fabrication of novel silicon based devices.

In conclusion, this thesis gives an overview of the possibilities offered by cryogenic DRIE. Etch processes, which utilize all three process regimes of the cryogenic DRIE process were studied and applied to the fabrication of silicon micro- and nanostructures that have applications in microfluidics and MEMS. The most commonly used process regime, the anisotropic regime, was utilized to create high aspect ratio silicon nanopillars, fluidic channels filled with an array of ordered micropillars and through-wafer structures. The isotropic process regime was successfully utilized for the release of suspended silicon microbridges and alumina membranes. The overpassivation regime is also very useful as it was used to create silicon nanograss, which was utilized for the fabrication of nanocorrugated membranes, laser desorption ionization sample plates and droplet microfluidics.

This thesis presents the parameters of five etching process in detail and describes how these parameters affect the etching conditions and results. Still, the emphasis of the thesis and its attached articles is not on process optimization, but on the fabrication of novel miniaturized devices and structures that have applications in microfluidics and MEMS.

The only publication that concentrates purely on process characterization is Publication II, which studies the effects of mask material at cryogenic temperatures. It shows that thick photoresists that are mechanically strong, such as SU-8, can also be utilized at cryogenic temperatures. Before this, all photoresist films thicker than 1.5 µm were thought to suffer from cracking problems. Another important result is the discovery of the extremely low etch rate of atomic layer deposited alumina films. An alumina film of just 6 nm of thickness was enough to etch through a 400 µm thick wafer. The use of very thin mask layers that have extremely high selectivity allows the fabrication of nanostructures with a high aspect ratio.

Publication III presents a micropillar array electrospray ionization chip. The chip has a microchannel which is filled with an ordered array of micropillars and ends in a three-dimensional sharp tip. The sample transfer in the lidless pillar channel is based purely on capillary forces. Besides easy sample transfer, the chip provides an extremely sensitive analysis of drugs and biomolecules when it is coupled with mass spectrometry. The fabrication process takes advantage of three slightly different cryogenic DRIE processes. The next step in the development of the chip is the integration of an on-chip microreactor before the MS analysis. This would allow the reaction products to be directly analyzed.

Publications IV and V concentrate on the fabrication of suspended devices and structures. The fabrication of the microbridge actuator presented in Publication V takes advantage of an SOI wafer and the capability to switch between highly anisotropic and fully isotropic etching profiles by simply changing the process

parameters. The alumina membranes shown in Publication IV utilize fully conformal deposition profiles, which are enabled by ALD and the good mechanical properties of alumina. In the future, we will characterize the properties of free standing alumina membranes in detail and use them as platforms for devices that require good thermal isolation.

The fabrication and use of nanostructures have become extremely hot topics. A novel method for the fabrication of silicon nanopillars is demonstrated in Publication VI. The fabrication process combines liquid flame spray produced silica nanoparticles and a highly anisotropic cryogenic DRIE process. The method is suitable for nanostructuring large areas rapidly and nanopillars can be easily combined with microstructures defined by optical lithography. Due to the large surface area of nanostructured surfaces and their effective light absorbance, the surface can be utilized as a sample plate in laser desorption ionization mass spectrometry. In Publication VII, a nanopillar structured silicon surface was chemically modified to change its wetting properties. A fluorocarbon coated nanostructured surface is ultrahydrophobic, whereas an oxidized nanostructured surface is completely wetting. The process developed in Publication VII allowed completely wetting areas to be patterned alongside ultrahydrophobic areas with lithographic accuracy. A water droplet on this kind of surface exhibits extraordinary behavior due to an extreme wettability gradient. By designing the completely wetting areas appropriately, passive droplet splitters can be constructed. Appropriately designed surfaces could also be used to concentrate non-volatile substances in a droplet. Nanopillar structured surfaces also allow the direct mass spectrometric analysis of concentrated substances.

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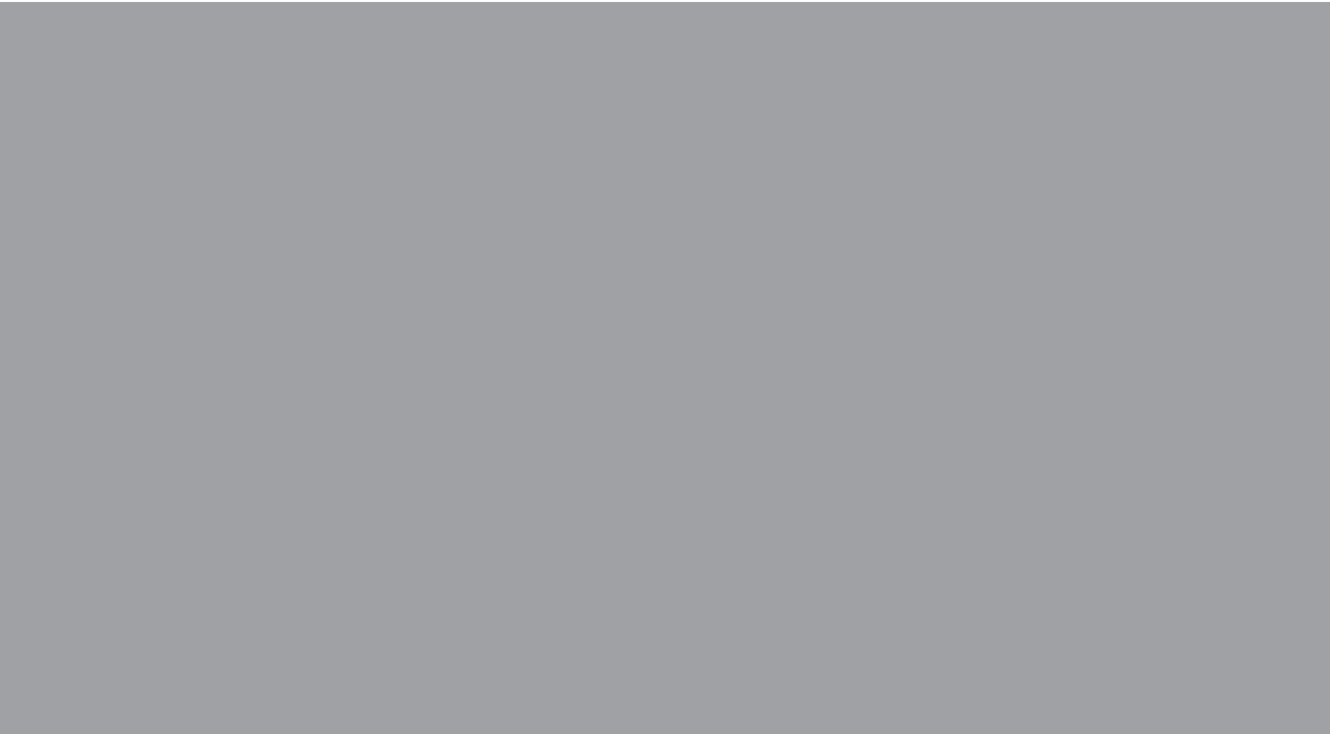

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