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DYNAMIC ANALYSIS AND QFT-BASED ROBUST CONTROL DESIGN OF SWITCHED-MODE POWER CONVERTERS

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Abstract

The use of switched-mode power converters is continuously growing both in power electronics products and systems, e.g. in Telecom applications, commercial grid systems etc.

The switching converters are required to provide robust behavior and to operate without instability under a variety of operation conditions. Hence the converter system may be subject to disturbances due to load, input voltage, and system parameter variations. In the thesis a robust control design procedure based on the QFT method (Quantitative Feedback Theory) is applied successfully for switching-mode DC-DC converters in order to achieve robust output in spite of different uncertainties. Simulation results are presented to demonstrate and validate the control design, showing good dynamic performance of the QFT controller.

When designing large-scale systems it is often impractical to analyze and design the system as a whole. Instead, it is desirable to divide the system into manageable subsystems which can then be designed independently. The subsystems may then be connected together to form a complete integrated system. One of the major difficulties in integrated subsystems is the stability performance degradation due to the interaction between the subsystems.

A formalism to analyze the interaction between subsystems using the unterminated two-port small-signal representation is derived. Two-port models are first defined as unterminated models, where the effect of load is excluded but may be easily included using the developed reflection rules. The use of the impedance ratio as a minor loop gain, which can be used to check system stability, is outlined.

Recently, there has been increasing interest in the parallel operation of DC-DC converters for reasons of increasing system reliability, facilitating system maintenance, allowing for future expansion, and reducing system design cost. However, paralleled DC-DC converters require a systematic modeling methodology and a categorical current-sharing mechanism to improve a performance of the overall system.

In order to achieve desirable characteristics when operating converter modules in parallel, a unified systematic approached for modeling of parallel DC-DC converter with current-sharing control, is proposed, developed, and analyzed.

Keywords Switched-mode converters, QFT-based robust control, subsystem interaction, current-sharing control.

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Preface

This research work has been carried out at the Department of Automation and Systems Technology of Helsinki University of Technology.

First of all I would like to thank my God for blessing me with the ability to complete this work successfully.

I am indebted to my supervisor *Professor Heikki Koivo* for giving me the opportunity to work in his laboratory and providing me with an excellent atmosphere for doing research. I am deeply grateful to my instructor, *Professor Teuvo Suntio* from Tampere University of Technology for his invaluable guidance and patience during the process. I wish to express my sincere appreciation to *D.Sc. Kai Zenger* for his support and all the time he spent with me discussing this work. I am grateful to the pre-examiners Prof. Pertti Silventoinen and Dr. Mikko Hankaniemi for their valuable comments and recommendations.

I would also like to thank all the people in the Control Engineering Group for creating an enjoyable atmosphere to work. The Academy of Finland and the Research Foundation of Helsinki University of Technology through different technology programs have supported this research financially, which are gratefully acknowledged. In addition, the grants received from Finnish Society of Automation, Elektroniikkainsinöörien Säätiö, Finnish Cultural Foundation and Alfred Kordelin Säätiö are gratefully acknowledged.

Deepest gratitude to my family and relatives for their continuous support. Finally, my dearest thanks go to my wife Salha, my daughters Fatma and Arwa for providing me with their everlasting love and confidence. Great thanks to all friends here in Finland and in Libya or elsewhere for their care and commitment.

Espoo, September, 2008

Ali Al.Towati

"This work is dedicated to the memory of my father, Mohammed, who has always been very supportive, patient, understanding, and encouraging. To the memories of my dearest brother, Elmuntaser and my beloved sister, Nafeesa, who have both passed away a few months ago, you will always have a place in my heart. It is also dedicated to my mother Fatma, for her continuous love, support, and encouragement"

List of Symbols

$(\boldsymbol{A},\boldsymbol{B},\boldsymbol{C},\boldsymbol{D})$	State-space realization of a linear system
$B(\omega)$	QFT bound
c	Control variable
C	Capacitor or capacitance
C_f	Filter capacitance
d	Duty cycle
D	Steady state duty cycle
D_i	Diode
d_s	Output disturbance signal
e_o	Voltage-source in current-output converter
F	Prefilter
f_o	Filter resonance frequency
f_c	Crossover frequency
f_f	The resonant frequency of output averaging filter
f_g	Feedforward gain from the input voltage
f_s	Switching frequency
F_m	Duty cycle gain
f_v	Feedback gain from the output voltage
G_c	Controller transfer function
G_{ci}	Control-to-input transfer function
G_{cid}	Cross-coupling transfer function
G_{cL}	Transfer function from control-to-inductor current
G_{co}	Control-to-output transfer function
G_{csc}	Current-sharing controller transfer function
G_D	Output disturbance model
G_{io-o}	Open-loop line-to-output transfer function
G_{ic-o}	Transfer function from line-to-capacitor voltage
G_{iL-o}	Transfer function from line-to-inductor current
G_{io-c}	Closed-loop line-to-output transfer function
G_{io-f}	Filter forward-voltage transfer function
G_{jc-o}	Transfer function from output current-to-capacitor voltage
G_{jL-o}	Transfer function from output-to-inductor current
G_a	Gain factor matching the voltage control signal to the internal control signal
H_{se}	Sensor gain
H_∞	Hardy space of transfer functions with bounded ∞-norm
H_v	Voltage-sensing gain

i_C	Capacitor current
i_{co}	Control command
i_{in}	Input current
i_{inc}	Bus current
i_L	Inductor current
i_p	Peak of inductor current
i_o	Output current
I_{in}	DC-value of input current
I_L	DC-value of inductor current
I_o	DC-value of output current
$j(s)$	Gain of controlled current source in canonical equivalent circuit
j_N	Norton current sink
j_o	Load current sink
J_o	DC-value of load current sink
K	Controller gain
L	Inductor or inductance
$L_g(s)$	Loop gain
$L_{g_{nom}}(s)$	Nominal loop gain
$L_c(s)$	Current loop gain
$L_{co}(s)$	Current-output loop gain
$L_{csc}(s)$	Current-sharing loop gain
$L_m(s)$	Minor loop gain
$L_v(s)$	Voltage loop gain
m_1	Inductor current slope when the switch is ON
m_2	Inductor current slope when the switch is OFF
$M(D)$	Voltage conversion ratio
M_c	Compensating ramp slope
M_s	Maximum peak magnitude
n	measured noise
N	Number of dc-dc converters in parallel
Q_c	Charge received by capacitor
Q_f	Quality Factor
P	Plant model
P_{in}	Converter input power
P_o	Converter output power
r_C	Equivalent series resistance of capacitor of the converter
r_{CF}	Equivalent series resistance of capacitor of the filter
r_d	The dynamic resistance associated to diode
r_{rds}	The MOSFET on-time channel resistance
r_L	Equivalent series resistance of inductor of the converter
r_{LF}	Equivalent series resistance of inductor of the filter
R	Resistance or resistor
R_{eq}	Equivalent resistance
R_{in}	Converter input resistance
R_L	Resistive load
R_s	Current-sensing resistor
S	Switch
S_P^T	Sensitivity function
t	Time in seconds

t_{on}	ON-time of the switch
t_{of}	OF-time of the switch
T	Complementary sensitivity function
T_{ji-o}	Open-loop input susceptibility to load changes
T_{ji-c}	Closed-loop input susceptibility to load changes
T_{ji-f}	Filter reverse-current transfer function
T_L	Lower tracking bound
T_s	Switching time interval
T_U	Upper tracking bound
u_c	Output of voltage controller
u_C	Output capacitor voltage
u_{CF}	Filter output capacitor voltage
u_d	Plant input
u_L	Inductor voltage
u_{in}	Input voltage
u_{inc}	Filter output voltage
u_o	Output voltage
u_r	Reference signal
$\boldsymbol{U}$	Input vector
U_C	DC-value of capacitor voltage
U_D	Voltage loss of the diode
U_{in}	DC-value of input voltage
U_o	DC-value of output voltage
V_{st}	Sawtooth waveform amplitude, i.e. PWM gain
$W_s(s)$	Weighting function
$\boldsymbol{X}$	State-variable vector
y	Plant output
$\boldsymbol{Y}$	Output vector
$Y_{in-\infty}$	Input admittance of ideally controlled converter
Y_{in-o}	Open-loop input admittance
Y_{in-c}	Closed-loop input admittance
Y_{in-f}	Filter input admittance
Y_{in-sc}	Input admittance of nulled output voltage
Y_{o-csc}	Current-sharing output admittance of slave module
Z_{in}	Input impedance
Z_{in-o}	Open-loop input impedance
Z_{in-c}	Closed-loop input impedance
Z_L	Load impedance
Z_{L_v}	Impedance of parallel-connected output capacitor and load impedance
Z_o	Output impedance
Z_{o-o}	Open-loop output impedance
Z_{o-c}	Closed-loop output impedance
Z_{o-f}	Filter output impedance
Z_s	Source impedance
Δi_L	The difference between a peak inductor current and its averaged
γ	Robust stability bound
ω_B	Bandwidth frequency

List of Abbreviations

AC	Alternating current
AC/DC	AC to DC rectifier
BW	Bandwidth
CCM	Continuous conduction mode
CS	Current sharing
DC	Direct current
DC−DC	DC to DC converter
DCM	Discontinuous-conduction mode
DPA	Distributed power architecture
DPS	Distributed power supply
DSP	Digital signal processor
EET	Extra-element-theorem
EMI	Electromagnetic interference
ESR	Equivalent series resistance
GM	Gain margin
GMPM	Gain margin and phase margin criterion
GUI	Graphical user interface
KCL	Kirchhoff's Current Law
KVL	Kirchhoff's Voltage Law
LC	Inductance-capacitance
LCR	Inductance-capacitance-resistance
LFT	Linear fractional transformation
LTI	Linear time invariant
LHP	Left-hand plane
LQG	Linear Quadratic Gaussian
MIMO	Multi input/multi output
MOSFET	Metal-oxide-semiconductor field-effect transistor
MSC	Master-Slave Control
NRO	Negative-resistance-oscillator
PCMC	Peak current-mode control
PI	Proportional-integral control
PFC	Power factor correction
PM	Phase margin
PWM	Pulse-width modulator
QFT	Quantitative feedback theory
RHPZ	Right-hand plane zero

SISO	Single input/single output
SMPS	Switching-mode power supply
SSA	State-space averaging
TODF	Two degree of freedom
VMC	Voltage-mode control

Contents

Chapter 1

Introduction

1.1 Background

The electric power is not normally used in the form in which it was produced or distributed. Practically all electronic systems require some form of power conversion. A device which transfers electric energy from the source to the load using electronic circuits is called a Power Supply, although power converter would be a more accurate term for such a device. A typical application of a power supply is to convert utility AC voltage into regulated DC voltages required for electronic equipment. Nowadays in most power supplies providing more than a few watts the energy flow is controlled with power semiconductors that are continuously switching on and off with high frequency. Such devices are called Switch Mode Power Supplies or SMPS. In general, SMPS can be classified into four types according to the form of input and output voltages: AC to DC (off-line power supply or a rectifier); DC to DC (voltage converter); AC to AC (frequency changer or cycloconverter); DC to AC (inverter). In this thesis, the modeling, control design challenges and subsystems interaction issues will be treated only for DC-DC converters.

Switching-mode power-electronic converters are nonlinear dynamical systems. The nonlinearities arise primarily due to switching, power devices, and passive components such as inductors, capacitors and parasitics. SMPS's represent different circuit topologies or configurations within each switching cycle. For the continuous conduction mode, there are two topologies. For the discontinuous conduction mode of operation, a third configuration has to be added to yield a total of three topologies. In each configuration, the system can be described by linear state equations. Switching between the different topologies will vary from cycle to cycle depending on the output of the system, and this complicates the analysis further.

The static conservation properties of the elementary switching converters (buck, boost, and buck-boost) have been thoroughly understood since the early 1970s. This is one of the main reasons of their ever-increasing number of applications in electrical energy conversion. However, the complete dynamics behavior of switching power converters still has to be further understood and improved. This is not possible without an in-depth understanding of the operation of such circuits and without easy-to-use and accurate models.

1.2 Modeling of Switching DC-DC Converters

Modeling and analysis of switching DC-DC converters can be either numerical or analytical. In numerical techniques, several algorithms or circuit simulators are used to produce quan-

titative results. These methods are easy to use. They posses accuracy and universality and they are applicable when no equivalent model is available. However, they are fail to provide the design insight needed to understand the behavior of switching converters. In contrast to numerical techniques, analytic techniques provide analytic expressions representing the operation and performance of the converters.

The most popular continuous-time technique is the small-signal analysis, which uses either circuit averaging [1], state-space averaging [2], or PWM switch modeling [3, 4]. In [1] analytical techniques were developed to represent buck, boost and buck-boost converters by approximate continuous models. Simple analytical expressions in terms of the circuit components were derived to characterize the low-frequency response of such systems. In [2] the above technique was generalized by introducing the state-space averaging method. The state-space descriptions of each switching mode were replaced by a single state-space description, hence eliminating the switching process from consideration and representing the average effect of the switched networks during operation cycle. The system was further simplified by perturbing the averaged system and then linearizing the resulting perturbed equations around the steady-state values. After a considerable amount of matrix manipulations, the system characteristics such as input impedance, output impedance, line-to-output transfer function, and control to-output characteristics, were obtained.

1.3 Control Design of Switching DC-DC Converters

The converters are required to provide robust behavior and to operate without instability under a variety of operation conditions. Hence the converter system may be subject to the disturbances of load, input voltage, and system configuration variations.

To improve the dynamic performances of converters, closed-loop control is indispensable. Generally, the linear small-signal model obtained using state-averaging and linearization techniques around an operating point is adopted for the controller design. However, since the model is dependent on the operating conditions and system configuration, the controller with fixed parameters (e.g., the PI and optimal controllers) which are adequate under the designed condition may not be so for other operating conditions. It is well known that robust control technic is one of the most effective techniques for dealing with parameter variations.

Several attempts have been made to apply robust control theory for DC-DC power converters. The linear quadratic Gaussian/loop transfer recovery methodology was used in [5] to design a controller for a series parallel resonant converter. In [6], a controller for a buck-boost converter with peak current control was designed using the μ-synthesis procedure. In [7, 8], H_∞ approach was applied to design controllers for boost and buck-boost converters. Nonlinear H_∞-control theory has been applied to regulate a PWM Cuk converter under parameter uncertainties and exogenous inputs which generate the reference trajectories [9]. In [10], H_∞ and μ-synthesis control methods have been applied to Telecom power supplies. But most of the existing robust control techniques are too complex theoretically for practical engineers to understand. It follows that optimal performance is generally not achieved, because traditional control methods design are used in practice.

This thesis proposes the use of robust control techniques to derive a controller for dc-dc converters, which are able to cope with the parameter variations in the converter's power stage. In particular, this thesis proposes the use of "Quantitative Feedback Theory" or QFT approach [11] which operates on the frequency domain to design a robust output voltage controller for switching-mode power converters. It was introduced by Isaac Horowitz in 1960s. This technique takes into account the uncertainty that may be present in the process and its environment, and establishes a balance between the complexity of controller and

complexity of design. It also differs in the way in which uncertainty is characterized as gain-phase variations or templates in the Nichols chart.

1.4 Stability and Subsystems Interactions

Stability is the most important requirement for switching-mode power supply systems. The issue of stability is closely related to the EMI filter design for subsystems powered through switching power converters. Improper designs of the input filter for such subsystems may result in undesirable interactions [12, 13].

Considerable interest is focused on evaluating the stability of subsystem interactions in distributed power systems. Usually, the impedance ratio stability criterion suggested in [12] is used to analyze the stability of interactions between two interconnecting subsystems. For example, the stability of a spacecraft DC distributed power system is addressed in [14]. Stability analysis for a system with a source converter and one or more load converters is given in [15, 16]. The design rules are usually based on the separation of the impedance levels at the interface of the subsystems. After [12, 17], many efforts have been taken in defining less conservative rules, see e.g. [18].

All these examples covered relatively simple system configurations, with an ideal voltage source, one source converter, and one or more load converters with resistive loads. The examples represented particular case studies rather than universal analysis tools. The results were obtained by tedious analytical developments for a particular system configuration rather than applying computer-aided analysis techniques to easily reconfigurable global system model.

1.5 Modeling and Dynamics Analysis of Multimodule DC-DC Converters

As a viable solution to demanding power requirements, power supplies for distributed power applications employ several converter modules in parallel. The resulting multimodule converters offer efficient processing of high current and built-in redundancy [19, 20, 21, 22]. However, standard converter modules may not have identical characteristic, which causes unbalance of current sharing. Modules delivering large currents will have their life-time shortened and the system reliability degraded [21]. Many factors contribute to the fact that modules not being identical, such as component tolerances, non-identical electrical conductors connected from the converters to current distribution and so on. Therefore, a unified consistent modeling approach is necessary to understand the dynamic behavior of the power supply and also to design a controller that regulates the output voltage and achieves balanced current distribution of the converter.

With current-sharing control, the output current of a multimodule converter is equally distributed among parallel modules, thereby improving reliability and reducing current stress on switching devices. Furthermore, the parallel processing of the load current provides fault tolerance to the system against the failure of a single module.

1.6 Research Objectives

Objectives of this thesis can roughly be divided into the following main categories:

- To give clear physical insight into the concept of switching-mode power converters, and to present a unified modeling methodology of the buck, boost and buck-boost convert-

ers operating in continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM).

- To implement a robust control approaches (i.e. QFT) in synthesizing robust controllers for DC-DC switching power converters in order to improve their dynamic performance by minimizing the effects of load disturbances over the specified region of plant uncertainties.

- To study the interaction of the subsystems in a distributed power supply system to ensure proper overall operation. The aim is to analyze the effect of the input filter and load on the dynamics of the converter. The main purpose is to develop design guidelines which prevent instabilities and performance degradations of the converter.

- To improve the performance characteristics of multimodule parallel DC-DC converter system through modeling, control design and simulation.

1.7 Outline of the Thesis

The thesis is organized as follows: In Chapter 2, an overview of a switched-mode supply system is given, and the modeling methodology of the system is discussed. In Chapter 3, the Quantitative Feedback Theory (QFT) is applied successfully to design a robust controller for DC-DC buck, boost and buck-boost converters operating in continuous conduction mode (CCM) and discontinuous conduction mode (DCM). In Chapter 4, the use of two-port unterminated network representation is demonstrated. Subsystem impedance interactions and stability analysis for distributed power supply systems are analyzed. The guidelines for how to design an optimal input filter for a switching power supply application, which prevents instabilities and performance degradations of the converter, are presented.

In Chapter 5, the small-signal model of DC-DC paralleled converters with individual voltage loop and Master-Slave Control (MSC) circuit is developed using small-signal equivalent two-port model. The dynamic characteristics of the current-sharing loop is derived. A robust current-sharing controller which takes into account the stability and ensures distribution of currents among the modules is designed.

Conclusions are drawn and some further work considerations are presented in Chapter 6. Appendix A.1 gives some Simulink/SimPower Systems™ models which have been used to generate the results presented in the thesis.

The following notation is adopted: The capital letters denote the DC values of associated quantities, the "hatted" small letters the ac or perturbed value excluding the switching ripple, and the small letters denote the total values. In equations the notation for the time variable t is suppressed, when no confusion is possible, e.g. i instead of $i(t)$ etc. The calculus is usually done in Laplace domain, which is not expressed explicitly except in the special cases when there is a chance of confusion.

1.8 Thesis's Contribution

The main contributions of this thesis can be summarized as follows:

- A new application of QFT to the control design of DC-DC switching-mode power converters is presented and examined for all basic converters operating in CCM and DCM in VMC and PCMC configurations.

- The analysis and simulation results show the practical applicability and performance of QFT in power converters.
- Subsystem interaction and stability problems for switching-mode power converter systems are illustrated and analyzed. In general, the interaction problem can be defined as the interaction between an unterminated component and its terminating subsystem.
- General formulations to determine the necessary conditions for system stability based on the impedance ratio inequality are derived.
- A unified systematic approach for modeling parallel DC-DC converters is proposed.
- A robust current-sharing controller, which ensures distribution of currents among the modules and grantees system stability, is designed using the QFT method.

Chapter 2

DC-DC Switching Converters

Modern electronic systems require high-quality, small, lightweight, reliable, and efficient power supplies. Linear power converters, whose principle of operation is based on a voltage or current divider, are inefficient. This is because they are limited to output voltages smaller than the input voltage, and also because their power density is low due to the low frequency (50 or 60 Hz) line transformers and filters needed. Linear converters can, however, provide a very high-quality output voltage. Their main area of application is at low power levels. Electronic devices in linear converters operate in their active (linear) modes, but at higher power levels switching converters are used. Switching converters use power electronic semiconductor switches in on and off states. Because there is a small power loss in those states (low voltage across a switch in the on state, zero current through a switch in the off state), switching converters can achieve high energy conversion efficiencies[23, 24] .

The functions of dc-dc converters are:

- to convert a dc input voltage into a dc output voltage ;
- to regulate the dc output voltage against load and line variations; and
- to provide isolation between the input source and the load (isolation is not always required);

To power the new information technology equipment, the distributed power architecture (DPA) has been widely adopted in the industry [25, 26, 27]. In DPA, the load converters are placed near the loads. Therefore, the conversion from the high or medium voltage to low voltage is done locally in front of each load. This allows the use of very high switching frequency and guarantees a fast response to load current transients. Furthermore, the current ratings in the entire power supply system are not so high. An example of a typical distributed power system (DPS) telecom power system is shown in Fig. 2.1, [25]. There are two power processing stages. In the figure, the first stage is the AC-to-DC rectifier that converts the AC line voltage into a 48V DC bus. This stage consists of two parts. One part is the AC-to-DC converter that converts the AC line voltage into an intermediate DC voltage (usually 400V). Also the power factor correction (PFC) is often included in this stage. However, Boost converter is usually used for this stage, because it is easier for input current shaping and it is suitable for high DC output voltage.

The other part is the DC-to-DC converter that converts the 400V DC to 48V DC. Electrical isolation is provided at this stage. Then the 48V bus is feeding the entire telecom load system. There is often a battery backup in the dc line, which powers the dc bus when the mains fails. In this case, the AC-to-DC rectifier should also be able to charge the battery

when needed. The second level consists of DC-to-DC power converters that convert the 48V DC into tightly regulated logic voltage such as 12V, 5V, 3.3V or 2.5V.

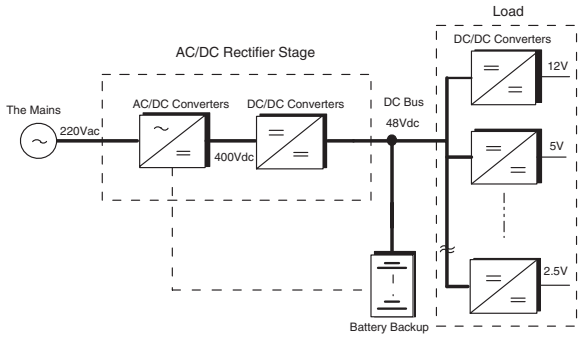


Figure 2.1: Distributed power system architecture in a telecom application.

In this chapter, the fundamentals and earliest topologies - the buck, boost and buck-boost converters are analyzed. Their basic operation is described and the modeling methodology of the system is discussed and explained.

2.1 The Buck DC-DC Converter

The buck converter is one of the simplest and mostly used among power converters: a chopper circuit that converts a dc input to a lower dc output voltage. Many switched-mode power supplies employ circuits closely related to the buck converter [28, 29].

The basic open-loop buck converter connected to the load is shown in Fig. 2.2. The impedance Z_L with constant-current j_o represents the non-ideal load system. In practice, the switch circuit is realized using power semiconductor devices, such as MOSFET S and diode D_i. The switch S opens and closes periodically at the switching frequency f_s, with a duty ratio d (the fraction of time that the switch is *on* during the whole switching cycle T_s, $d = t_{on}/T_s$). When S is closed, the input voltage u_{in} is transferred to the LC low-pass filter. When S is open, the inductor maintains its current flow, forcing the diode D_i to conduct and grounding the input of the LC filter. Thus the filter sees a square wave between 0 and u_{in}. The cutoff frequency of the filter is much lower than f_s, removing most of the switching ripple and delivering a relatively smooth output voltage u_o to the load. The output voltage can be varied by changing the duty ratio d (by pulse-width modulation (PWM)).

2.2 The Boost DC-DC Converter

A boost converter is shown in Fig. 2.3. When the switch S is on, the diode is reverse biased, and the input supplies energy to the inductor. The load receives energy from the capacitor. When the switch S is off, the output stage receives energy from the inductor as well as from the input. The output voltage is always larger than the input voltage. Ideally it can be infinite, but in practice it is constrained to some maximum value. The input current is triangular waved, which means that the harmonic content of it is not so high as that of a buck converter.

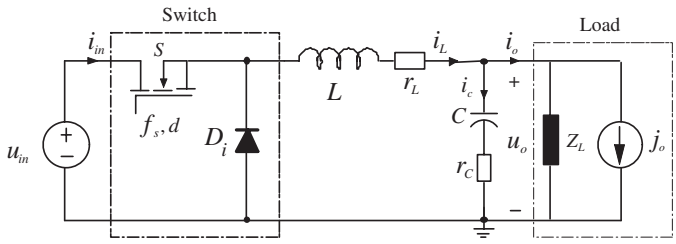


Figure 2.2: The open-loop buck converter.

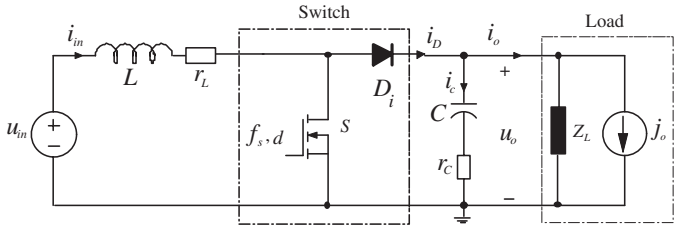


Figure 2.3: The open-loop boost converter.

2.3 The Buck-Boost DC-DC Converter

A buck-boost is mainly used in regulated DC power supplies, where a negative-polarity output may be desired with respect to the common terminal of the input voltage, and the output voltage can be either higher or lower than the input voltage, depending on the duty ratio [29]. A buck-boost converter is constructed by the cascade connection of the two basic converters: the buck converter and the boost converter as shown in Fig. 2.4. When the switch is on, the input provides energy to the inductor and the diode is reverse biased. When the switch is off, the load receives energy from the inductor. No energy is supplied by the input in this interval.

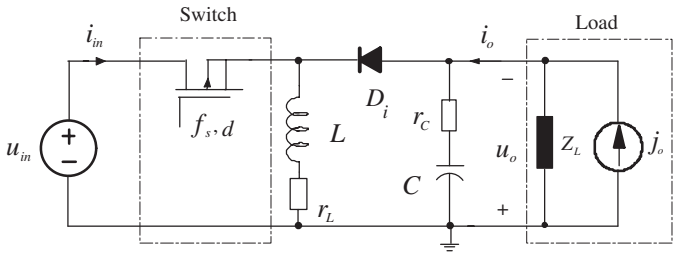


Figure 2.4: The open-loop buck-boost converter.

2.4 Modes of Operation of the DC-DC Converter

The dc-dc converters can have two distinct modes of operation: (1) continuous conduction mode (CCM) and (2) discontinuous conduction mode. In practice, a converter may operate

in both modes, which have significantly different characteristics. Therefor, a converter and its control should be designed based on both modes of operation.

2.4.1 Continuous Conduction Mode CCM

If the current through the inductor L never falls to zero during a commutation cycle, the converter is said to operate in continuous conduction mode (CCM). The inductor current waveforms in a converter can be seen in Fig. 2.5.

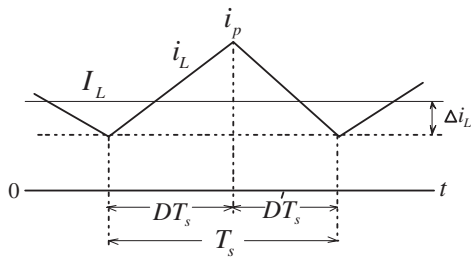


Figure 2.5: Inductor current waveform in CCM.

2.4.2 Discontinuous Conduction Mode DCM

If the inductor current stays at zero level during a part of the off time, the converter is said to operate in discontinuous conduction mode (DCM).

The discontinuous conduction mode (DCM) of operation is often associated with light loads. In order to avoid the reverse recovery problem of the diode for low power applications, the designers usually prefer to operate the converter in DCM even for all loads. The inductor current waveforms of a converter is shown in Fig. 2.6.

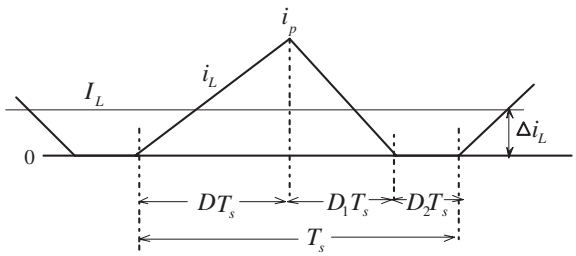


Figure 2.6: Inductor current waveform in DCM.

2.5 Control Structures of DC-DC Converter

In a dc-dc converter application, it is desired to obtain a constant output voltage despite of changes and disturbances in the input voltage or the load current. It is desired that essentially all of this variation fall within a specified range; however, this is not possible to achieve without the use of negative feedback. Given an input voltage, the average output

voltage is controlled by controlling the switch on and off durations. One of the methods for controlling the output voltage employs switching at a constant frequency and adjusting the on duration of the switch to control the average output voltage. In this method, called the pulse-width modulation (PWM) switching, the switch duty ratio d is varied.
The two main control schemes used in practice are the voltage mode control (VMC) and peak-current mode control (PCMC).

2.5.1 Voltage-Mode Control VMC

The VMC scheme is the most popular and simple PWM control scheme. The basic voltage mode configuration is shown in Fig. 2.7. In voltage-mode control VMC, the output-voltage feedback loop tracks the output voltage variations and adjusts the duty cycle accordingly. The control voltage signal u_c is generated by amplifying the error between the output voltage and the reference voltage. The control voltage is then compared to the sawtooth waveform, having frequency f_s and peak voltage V_{st}. When the amplified error signal is larger than the sawtooth waveform, the switch control signal becomes high, causing the switch to turn ON. Otherwise, the switch is OFF.

The main drawback of voltage-mode control is the fact that, any change in the line or load must first be sensed as an output change and then compensated by the feedback loop. There is then an unavoidable delay in the compensation of these disturbances.

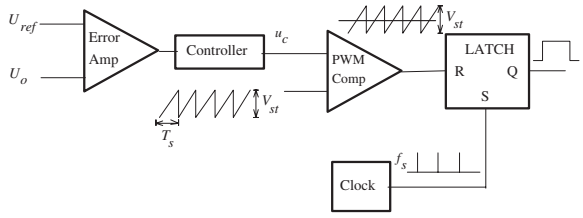


Figure 2.7: Voltage-mode control structure.

2.5.2 Peak Current-Mode Control PCMC

Peak current-mode control is a direct extension of voltage-mode control. In PCMC, an inner inductor-current feedback loop is added to improve the system dynamics. The inner loop forces the maximum value of the inductor current to track the control current, while the outer loop regulates the output voltage. The duty cycle is generated by comparing the inductor current and control current i_{co}.

The main problem in current-mode control is the instability for duty cycles above 50%. The problem is well known and discussed in the literature, e.g. in [28]. This limitation can be removed by adding a compensation ramp M_c, to the control current signal, as shown in Fig. 2.8.

2.6 Modeling of DC-DC Switching Power Converters

The inherent switching operation of power converters results in the circuit components being connected together in periodically changing configurations, in which each configuration is described by a separate set of equations. The transient analysis and control design for converters are therefore difficult since a number of equations must be solved in sequence.

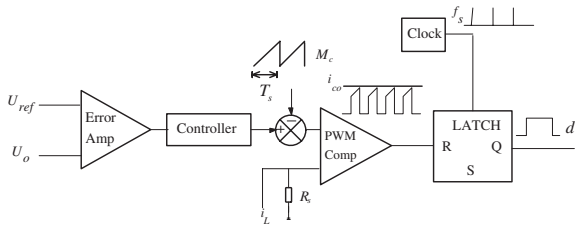


Figure 2.8: Peak-current-mode control structure.

The technique of averaging provides a solution to this problem. A single equation may be formed to describe the converter approximately over a number of switching cycles by simply taking a linearly weighted average of the separate equations for each switched configuration of the converter. State space averaging [29, 23, 2, 24] is the most common averaging technique, and is used here to model the switching dc-dc converter.

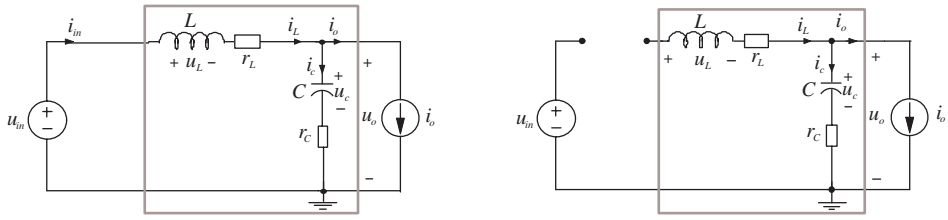
2.6.1 Continuous Conduction Mode CCM

The state-space averaging technique will be reviewed next to model all basic dc-dc converters (i.e., Buck, Boost and Buck-Boost converters) operating in continuous conduction mode CCM.

State-Space Averaging Technique

In state-space averaging (SSA), the switching circuit is divided into two (CCM) different structures. The derivatives of inductor currents and capacitor voltages are defined based on circuit theory for every substructure. These currents and voltages are averaged over one switching cycle. Consider the state space representation for a buck converter shown in Fig. 2.2. The voltage loss of the free-wheeling diode is assumed to be U_D.

During the on time, the switch is on, and the diode is off. Therefore, the corresponding subcircuit is as shown in Fig. 2.9(a). Applying Kirchhoff's Voltage Law (KVL) and Kirchhoff's Current Law (KCL) we obtain



(a) On-time. (b) Off-time.

Figure 2.9: On and Off time subcircuits of buck converter.

$$\frac{di_L}{dt} = -\frac{r_C + r_L}{L} \cdot i_L - \frac{1}{L} \cdot u_C + \frac{1}{L} \cdot u_{in} + \frac{r_C}{L} \cdot i_o \tag{2.1a}$$

$$\frac{du_C}{dt} = \frac{1}{C} \cdot i_L - \frac{1}{C} \cdot i_o \tag{2.1b}$$

$$u_o = r_C \cdot i_L + u_C - r_C \cdot i_o \tag{2.1c}$$

$$i_{in} = i_L \tag{2.1d}$$

During the off time, the switch is off, and the diode is conducting. Therefore, the corresponding subcircuit is as shown in Fig. 2.9(b), Applying (KVL) and (KCL) we get, correspondingly

$$\frac{di_L}{dt} = -\frac{r_C + r_L}{L} \cdot i_L - \frac{1}{L} \cdot u_C - \frac{1}{L} \cdot U_D + \frac{r_C}{L} \cdot i_o \tag{2.2a}$$

$$\frac{du_C}{dt} = \frac{1}{C} \cdot i_L - \frac{1}{C} \cdot i_o \tag{2.2b}$$

$$u_o = r_C \cdot i_L + u_C - r_C \cdot i_o \tag{2.2c}$$

$$i_{in} = 0 \tag{2.2d}$$

The averaged state equations can be obtained by weighting the equations in (2.1) and (2.2) by their proportional time d, and $d' = 1 - d$ respectively, and the resulting equations are added together

$$\frac{d\langle i_L \rangle}{dt} = -\frac{r_C + r_L}{L} \cdot \langle i_L \rangle - \frac{1}{L} \cdot \langle u_C \rangle + \frac{\langle d \rangle}{L} \cdot \langle u_{in} \rangle - \frac{\langle d' \rangle}{L} \cdot U_D + \frac{r_C}{L} \cdot \langle i_o \rangle \tag{2.3a}$$

$$\frac{d\langle u_C \rangle}{dt} = \frac{1}{C} \cdot \langle i_L \rangle - \frac{1}{C} \cdot \langle i_o \rangle \tag{2.3b}$$

$$\langle u_o \rangle = r_C \langle i_L \rangle + \langle u_C \rangle - r_C \cdot \langle i_o \rangle \tag{2.3c}$$

$$\langle i_{in} \rangle = \langle d \rangle \langle i_L \rangle \tag{2.3d}$$

where the symbol "$\langle\ \rangle$" denote the averaging over an entire switching cycle.

Small Signal Model

The problem with the state equations (2.3) is that they are nonlinear. The nonlinearity is due to the multiplication of two time-varying components (i.e. $d(t)u_{in}(t)$). This problem can be solved by linearizing the model in the vicinity of the steady-state operating point. The small-signal representation can be obtained from (2.3) by applying the linearization procedure presented in [31]. This procedure gives the linearized state-space representation as follows

$$\dot{\hat{\mathbf{x}}} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{\mathbf{u}} \tag{2.4a}$$

$$\hat{\mathbf{y}} = \mathbf{C}\hat{\mathbf{x}} + \mathbf{D}\hat{\mathbf{u}} \tag{2.4b}$$

where the symbol ($\hat{}$) over the variables means small perturbation around the corresponding steady-state value. The inductor current i_L and the capacitor voltage u_C are selected as the state variables, the input voltage u_{in}, the output current i_o and duty cycle d as the input variables, and the input current i_{in} and the output voltage u_o as the output variables,

$$\hat{\mathbf{x}} = \begin{bmatrix} \hat{i}_L & \hat{u}_C \end{bmatrix}^T, \hat{\mathbf{u}} = \begin{bmatrix} \hat{u}_{in} & \hat{i}_o & \hat{d} \end{bmatrix}^T, \hat{\mathbf{y}} = \begin{bmatrix} \hat{i}_{in} & \hat{u}_o \end{bmatrix}^T$$

After linearization the SSA matrices for a buck converter become

$$\mathbf{A} = \begin{bmatrix} -\frac{r_L+r_C}{L} & -\frac{1}{L} \\ \frac{1}{C} & 0 \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} \frac{D}{L} & \frac{r_C}{L} & \frac{U_{in}+U_D}{L} \\ 0 & -\frac{1}{C} & 0 \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} D & 0 \\ r_C & 1 \end{bmatrix}, \quad \mathbf{D} = \begin{bmatrix} 0 & 0 & I_L \\ 0 & -r_C & 0 \end{bmatrix}$$

Likewise, the SSA matrices for a boost converter are represented by

$$\mathbf{A} = \begin{bmatrix} -\frac{D'r_C+r_L}{L} & -\frac{D'}{L} \\ \frac{D'}{C} & 0 \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} \frac{1}{L} & \frac{D'r_C}{L} & \frac{U_o+U_D+r_C(I_L-I_o)}{L} \\ 0 & -\frac{1}{C} & -\frac{I_L}{C} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} 1 & 0 \\ D'r_C & 1 \end{bmatrix}, \quad \mathbf{D} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -r_C & -r_C I_L \end{bmatrix}$$

and for a buck-boost converter

$$\mathbf{A} = \begin{bmatrix} -\frac{D'r_C+r_L}{L} & -\frac{D'}{L} \\ \frac{D'}{C} & 0 \end{bmatrix}, \mathbf{B} = \begin{bmatrix} \frac{D}{L} & \frac{D'r_C}{L} & \frac{U_{in}+U_D+r_C(I_L-I_o)}{L} \\ 0 & -\frac{1}{C} & -\frac{I_L}{C} \end{bmatrix}$$

$$\mathbf{C} = \begin{bmatrix} D & 0 \\ D'r_C & 1 \end{bmatrix}, \mathbf{D} = \begin{bmatrix} 0 & 0 & I_L \\ 0 & -r_C & -r_C I_L \end{bmatrix}$$

The steady-state operating point

The steady-state operating point of a buck converter can be obtained from (2.3) letting the average derivative to be equal to zero and replacing the values of variables with their steady-state values. The expressions for the state and output variables of all basic converters are summarized in Table (2.1).

Table 2.1: Steady-state operating point for all basic ideal converters in CCM.

Type	I_L	I_{in}	D	U_o
Buck	I_o	DI_o	$\frac{U_D+r_L I_o+U_o}{U_{in}+U_D}$	U_C
Boost	$\frac{I_o}{D'}$	$\frac{I_o}{D'}$	$1-\frac{\left(1+\sqrt{1+4\frac{r_L I_o(U_o+U_D-r_C I_o)}{(U_{in}-r_C I_o)^2}}\right)}{\frac{2(U_o+U_D-r_C I_o)}{(U_{in}-r_C I_o)}}$	U_C
Buck-Boost	$\frac{I_o}{D'}$	$\frac{DI_o}{D'}$	$1-\frac{\left(1+\sqrt{1+4\frac{r_L I_o(U_o+Uin+U_D-r_C I_o)}{(U_{in}-r_C I_o)^2}}\right)}{\frac{2(U_o+Uin+U_D-r_C I_o)}{(U_{in}-r_C I_o)}}$	U_C

2.6.2 Discontinuous Conduction Mode DCM

The DCM operation of switching converters differs from CCM operation by an additional third time interval in each switching cycle during which an inductor current is clamped to zero. In DCM operation the inductor current rises in the first interval when the switch is turned on, reaches a peak when the switch is to be turned off, and resets to zero at the end of the second interval. However, we use d and d_1 to denote the duty ratio of the first and the second interval, respectively (see Fig. 2.10).

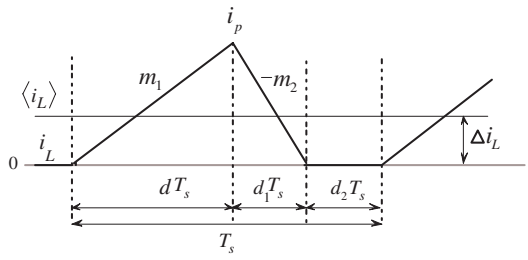


Figure 2.10: Inductor current waveforms within a switching cycle in DCM.

A basic idea in forming the state-space equations for a continuous linear time-invariant system (LTI) is to describe the derivatives of the state variables as a function of state, input, and control variables. In the conventional SSA method [32, 28] applied to switching converters, the derivatives are derived using circuit theory and averaged over one switching cycle. This approach has proved to be efficient in CCM, because the instantaneous inductor current is continuous, and therefore, the average currents within ON and OFF times are related directly to the duty ratio and its complement. The situation is different in DCM, and therefore, the SSA method does not give correct formulation [33, 34]. Alternatively, those derivatives will be derived based on the physical phenomena associated to the inductor current (i.e., average slope) and the capacitor voltage (i.e., average charge), resulting in a consistent formulation in DCM for all basic converters.

Based on inductor current waveform shown in Fig. (2.10), the average inductor current $\langle i_L \rangle$ and its derivative for all basic converters (i.e., buck, boost and buck-boost) can be expressed as

$$\langle i_L \rangle = \frac{i_p}{2}(d + d_1) \tag{2.5}$$

$$\frac{d\langle i_L \rangle}{dt} = dm_1 - d_1 m_2 - \frac{r_L}{L}\langle i_L \rangle \tag{2.6}$$

where i_p is the peak of the inductor current i_L, m_1 and m_2 are the up and down slopes of instantaneous inductor current expressed as positive quantities. Their expressions of buck, boost and buck-boost converters are defined in Table 2.2, [33, 34].

The output circuitry (Fig. 2.11) is the same for all the basic converters with respect to the formulation for the derivative of average capacitor voltage $\langle u_C \rangle$, and therefore, the derivative of average capacitor voltage can be approximated by computing the average charge delivered into the capacitor as an average change of charge as following

Table 2.2: Up and down slopes of basic converters.

Type	m_1	m_2
Buck	$\frac{u_{in}-u_o}{L}$	$\frac{u_o+U_D}{L}$
Boost	$\frac{u_{in}}{L}$	$\frac{-u_{in}+u_o+U_D}{L}$
Buck-Boost	$\frac{u_{in}}{L}$	$\frac{u_o+U_D}{L}$

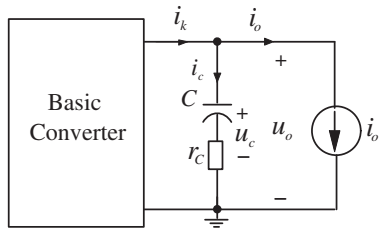


Figure 2.11: Basic converter.

$$\frac{d\langle u_C\rangle}{dt} = \frac{\Delta Q_c}{T_s} = \frac{\langle i_k\rangle}{C} - \frac{\langle i_o\rangle}{C} \tag{2.7}$$

where i_k denotes the current coming through the inductor, for a buck converter

$$\langle i_k\rangle = \langle i_L\rangle \tag{2.8}$$

and for boot and buck-boost converters

$$\langle i_k\rangle = \frac{d_1}{d+d_1}\langle i_L\rangle \tag{2.9}$$

Therefore, the derivative of $\langle u_c\rangle$ in (2.7) is for a buck converter as (2.10) and for boost and buck-boost converters as (2.11),

$$\frac{d\langle u_C\rangle}{dt} = \frac{\langle i_L\rangle}{C} - \frac{\langle i_o\rangle}{C} \tag{2.10}$$

$$\frac{d\langle u_C\rangle}{dt} = \frac{d_1}{d+d_1}\frac{\langle i_L\rangle}{C} - \frac{\langle i_o\rangle}{C} \tag{2.11}$$

In order to include the effect of parasitic elements in a converter average model, formulas for the average output voltage have to be derived. By applying KVL to the circuit shown in Fig. 2.11 and using the expressions of the current coming from the inductor i_k given in (2.8) and (2.9), the average output voltage $\langle u_o\rangle$ for a buck converter can be expressed as (2.12) and for boost and buck-boost converters as (2.13)

$$\langle u_o\rangle = r_C\langle i_L\rangle + \langle u_C\rangle - r_C\langle i_o\rangle \tag{2.12}$$

$$\langle u_o \rangle = \frac{d_1}{d+d_1} \cdot r_C \langle i_L \rangle + \langle u_C \rangle - r_C \langle i_o \rangle \tag{2.13}$$

For boost and buck-boost converters, only the average and OFF time values are of interest [34], therefore (2.13) can be rewritten as

$$\langle u_o \rangle = r_C \langle i_L \rangle + \langle u_C \rangle - r_C \langle i_o \rangle \tag{2.14}$$

To complete the averaged state-space models, the average input current of the converter $\langle i_{in} \rangle$ has to be introduced. The input current of buck and buck-boost converters is equal to the inductor during the ON time. Therefore, the average input current can be expressed as

$$\langle i_{in} \rangle = \frac{d}{d+d_1} \langle i_L \rangle \tag{2.15}$$

The input current of a boost converter equals the inductor current, and therefore, its average value can be presented as

$$\langle i_{in} \rangle = \langle i_L \rangle \tag{2.16}$$

We consider again a buck converter shown in Fig. 2.2 and derive the state-space representation model.

$$\begin{aligned}
&\tfrac{d\langle i_L \rangle}{dt} = dm_1 - d_1 m_2 - \tfrac{r_L}{L} \langle i_L \rangle \\
&\tfrac{d\langle u_C \rangle}{dt} = \tfrac{1}{C} \langle i_L \rangle - \tfrac{1}{C} \langle i_o \rangle \\
&\langle u_o \rangle = r_C \langle i_L \rangle + \langle u_C \rangle - r_C \langle i_o \rangle \\
&\langle i_{in} \rangle = \tfrac{d}{d+d_1} \langle i_L \rangle
\end{aligned} \tag{2.17}$$

It can be seen that the second duty ratio, d_1, in (2.17) is not independent, rather algebraically dependent on state and control variables. For the purposes of an averaged model, it is convenient to reflect this dependency in terms of the average values of voltage and current. In this way, d_1 can be eliminated, and a model expressed in the averaged state variables can be obtained. The algebraic function defining this dependency is called the duty-ratio constraint.

Unlike the conventional state-space averaging method [32] where a volt-second balance relation of inductor current is used to define d_1, a different duty-ration constraint which includes the effect of parasitic elements will be derived here. For this purpose equation (2.5) is recalled

$$\langle i_L \rangle = \frac{i_p}{2} (d + d_1)$$

When the switch is ON, the inductor peak current i_p can be expressed as

$$i_p = \frac{u_L}{L} \cdot dT_s \tag{2.18}$$

where u_L is the voltage across the inductor. The relation (2.18) can be written in terms of

the up slope m_1 as following

$$i_p = \left(m_1 - \frac{r_L}{L}\langle i_L\rangle\right)\cdot dT_s \tag{2.19}$$

Substituting (2.19) into (2.5) and solving the resulting equation for d_1 yields

$$d_1 = \frac{2\langle i_L\rangle}{\left(m_1 - \frac{r_L}{L}\langle i_L\rangle\right)\cdot dT_s} - d \tag{2.20}$$

When d_1 is substituted into (2.17), we get

$$\begin{aligned}
&\frac{d\langle i_L\rangle}{dt} = d(m_1+m_2) - \frac{2\langle i_L\rangle m_2}{dT_s\left(m_1-\frac{r_L}{L}\langle i_L\rangle\right)} - \frac{r_L}{L}\langle i_L\rangle \\
&\frac{d\langle u_C\rangle}{dt} = \frac{1}{C}\langle i_L\rangle - \frac{1}{C}\langle i_o\rangle \\
&\langle u_o\rangle = r_C\langle i_L\rangle + \langle u_C\rangle - r_C\langle i_o\rangle \\
&\langle i_{in}\rangle = \frac{d^2T_s}{2}\left(m_1 - \frac{r_L}{L}\langle i_L\rangle\right)
\end{aligned} \tag{2.21}$$

When the up and down slopes (i.e., m_1 and m_2 in Table 2.2) as well as the output voltage in (2.12) are substituted into (2.21), the corresponding nonlinear state-space representation for a buck converter can be written as

$$\frac{d\langle i_L\rangle}{dt} = \frac{d(\langle u_{in}\rangle + U_D)}{L} - \frac{2\langle i_L\rangle(r_C\langle i_L\rangle + \langle u_C\rangle - r_C\langle i_o\rangle + U_D)}{dT_s(\langle u_{in}\rangle - (r_C+r_L)\langle i_L\rangle - \langle u_C\rangle + r_C\langle i_o\rangle)} - \frac{r_L}{L}\langle i_L\rangle \tag{2.22a}$$

$$\frac{d\langle u_C\rangle}{dt} = \frac{1}{C}\langle i_L\rangle - \frac{1}{C}\langle i_o\rangle \tag{2.22b}$$

$$\langle u_o\rangle = r_C\langle i_L\rangle + \langle u_C\rangle - r_C\langle i_o\rangle \tag{2.22c}$$

$$\langle i_{in}\rangle = \frac{d^2T_s}{2L}(\langle u_{in}\rangle - (r_C+r_L)\langle i_L\rangle - \langle u_C\rangle + r_c\langle i_o\rangle) \tag{2.22d}$$

Small Signal Model

The small-signal state-space representation for a buck converter can be obtained from (2.22) by applying the linearizing procedure presented in [31], yielding

$$\begin{aligned}
\frac{d\hat{i}_L}{dt} = &-\left(\frac{r_L}{L} + \frac{2((U_{in}-U_o-r_LI_o)+I_o(r_L+r_C))(U_o+U_D)}{DT_s(U_{in}-U_o-r_LI_o)^2}\right)\cdot\hat{i}_L \\
&-\frac{2I_o((U_{in}-U_o-r_LI_o)+(U_o+U_D))}{DT_s(U_{in}-U_o-r_LI_o)^2}\cdot\hat{u}_C + \left(\frac{D}{L} + \frac{2I_o(U_o+U_D)}{DT_s(U_{in}-U_o-r_LI_o)^2}\right)\cdot\hat{u}_{in} \\
&+\left(\frac{U_{in}+U_D}{L} + \frac{2I_o(U_o+U_D)}{D^2T_s(U_{in}-U_o-r_LI_o)}\right)\cdot\hat{d}
\end{aligned} \tag{2.23a}$$

$$\frac{d\hat{u}_C}{dt} = \frac{1}{C}\cdot\hat{i}_L - \frac{1}{C}\cdot\hat{i}_o \tag{2.23b}$$

$$\hat{i}_{in} = -\frac{D^2T_s\left(r_C + r_L\right)}{2L}\cdot\hat{i}_L - \frac{D^2T_s}{2L}\cdot\hat{u}_C + \frac{D^2T_s}{2L}\cdot\hat{u}_{in} + \frac{r_C D^2T_s}{2L}\cdot\hat{i}_o + \frac{2DT_s\left(U_{in} - U_o - r_L I_o\right)}{2L}\cdot\hat{d} \tag{2.23c}$$

$$\hat{u}_o = r_C\hat{i}_L + u_C - r_C\hat{i}_o \tag{2.23d}$$

The states-space representation in (2.23) would be most convenient to be solved when the numerical values of the corresponding operating points are utilized. The effect of the parasitic elements on the converter dynamics is minimal as stated in [33]. Therefore, they may omitted in (2.23), except the effect of the equivalent series resistor of the output capacitor r_C in(2.23d), and the small-signal stat-space representation can be accordingly expressed in state-space representation

$$\hat{\dot{\mathbf{x}}} = \mathbf{A_{dcm}}\hat{\mathbf{x}} + \mathbf{B_{dcm}}\hat{\mathbf{u}} \tag{2.24a}$$

$$\hat{\mathbf{y}} = \mathbf{C_{dcm}}\hat{\mathbf{x}} + \mathbf{D_{dcm}}\hat{\mathbf{u}} \tag{2.24b}$$

where $\mathbf{x} = \begin{bmatrix} i_L & u_C \end{bmatrix}^T$, $\mathbf{u} = \begin{bmatrix} u_{in} & i_o & d \end{bmatrix}^T$, $\mathbf{y} = \begin{bmatrix} i_{in} & u_o \end{bmatrix}^T$, the subscript "$_{dcm}$" denotes the discontinuous-conduction-mode of operation.

It is convenient to present the SSA matrices in terms of voltage conversion ratio $M = U_o/U_{in}$ and K, where $K = 2L/R_{eq}T_s$ and $R_{eq} = U_o/I_o$. As a result the SSA matrices for a buck converter can be obtained as follows

$$\mathbf{A_{dcm}} = \begin{bmatrix} -\frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} & -\frac{1}{L(1-M)}\sqrt{\frac{K}{1-M}} \\ \frac{1}{C} & 0 \end{bmatrix} \quad \mathbf{B_{dcm}} = \begin{bmatrix} \frac{(2-M)M}{L(1-M)}\sqrt{\frac{K}{1-M}} & 0 & \frac{2U_{in}}{L} \\ 0 & -\frac{1}{C} & 0 \end{bmatrix}$$

$$\mathbf{C_{dcm}} = \begin{bmatrix} 0 & -\frac{M^2}{R_{eq}(1-M)} \\ r_C & 1 \end{bmatrix} \quad \mathbf{D_{dcm}} = \begin{bmatrix} \frac{(2-M)M}{L(1-M)}\sqrt{\frac{K}{1-M}} & 0 & \frac{U_o}{R_{eq}}\sqrt{\frac{1-M}{K}} \\ 0 & -\frac{1}{C} & 0 \end{bmatrix}$$

Likewise, the SSA matrices for a boost converter are

$$\mathbf{A_{dcm}} = \begin{bmatrix} -\frac{R_{eq}}{L}\sqrt{\frac{K(1-M)}{M}} & -\frac{1}{L}\sqrt{\frac{KM}{M-1}} \\ \frac{1}{C} & 0 \end{bmatrix} \quad \mathbf{B_{dcm}} = \begin{bmatrix} \frac{M^2}{L}\sqrt{\frac{MK}{M-1}} & 0 & \frac{2U_o}{L} \\ 0 & -\frac{1}{C} & -\frac{2U_o}{R_{eq}C}\sqrt{\frac{M-1}{MK}} \end{bmatrix}$$

$$\mathbf{C_{dcm}} = \begin{bmatrix} 1 & 0 \\ r_C & 1 \end{bmatrix} \quad \mathbf{D_{dcm}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix}$$

Correspondingly, the SSA matrices for a buck-boost converter are given as follows

$$\mathbf{A_{dcm}} = \begin{bmatrix} -\frac{R_{eq}}{L}\sqrt{K} & -\sqrt{\frac{K}{L}} \\ \frac{1}{C} & 0 \end{bmatrix} \quad \mathbf{B_{dcm}} = \begin{bmatrix} \frac{M(M+2)\sqrt{K}}{L} & 0 & \frac{2(U_o+U_{in})}{L} \\ -\frac{M^2}{R_{eq}C} & -\frac{2U_o}{R_{eq}C\sqrt{K}} & \end{bmatrix}$$

$$\mathbf{C_{dcm}} = \begin{bmatrix} 1 & 0 \\ r_C & 1 \end{bmatrix} \quad \mathbf{D_{dcm}} = \begin{bmatrix} \frac{M^2}{R_{eq}} & 0 & \frac{2U_o}{R_{eq}\sqrt{K}} \\ 0 & 1 & 0 \end{bmatrix}$$

The expressions for the state and output variables are of all basic converters are summarized in Table 2.3

Table 2.3: Steady-state operating point for all basic converters in DCM.

Type	I_L	I_{in}	D	D_1	U_o
Buck	I_o	MI_o	$M\sqrt{\frac{K}{1-M}}$	$\sqrt{K(1-M)}$	U_C
Boost	MI_o	MI_o	$\sqrt{KM(M-1)}$	$\frac{1}{M-1}$	U_C
Buck-Boost	MI_o	$(1+M)I_o$	$M\sqrt{K}$	$\frac{K(M+1)}{M} - M\sqrt{K}$	U_C

2.7 Modeling of Pulse-Width Modulator

While there are no substantial differences in the modeling of the power stage for all converters, there are differences in the modeling of converter's PWM stage, particularly in PCMC. In voltage-mode control the switching operation is done by comparing the control voltage to the sawtooth waveform. In PCMC, the inductor current is connected directly to the pulse-width modulator. It then follows that the duty cycle is not generated independently by the control current, but also other variables affect the duty cycle. The inductor current may depend on the input and output voltages. Hence, perturbations in the input and output voltages propagate to the pulse-width modulator also via the inductor-current feedback loop, and thus affect the duty cycle directly. A small-signal model of the PWM stage is needed.

2.7.1 Voltage-Mode PWM

A voltage-controlled buck converter is shown in Fig. 2.12. Normally, the duty ratio is obtained by comparing the error or control signal u_c with the sawtooth voltage V_{st}. When u_c is larger than V_{st} the switch is turned on and, consequently the diode turns off. When u_c is less than V_{st}, the switch is turned off, and as a result the diode turns on. In this case the following expression for the duty cycle can be derived

$$d = \frac{1}{V_{st}} u_c \tag{2.25}$$

where u_c is the control signal. Note that, in the frequency domain, modulator equation is simply given

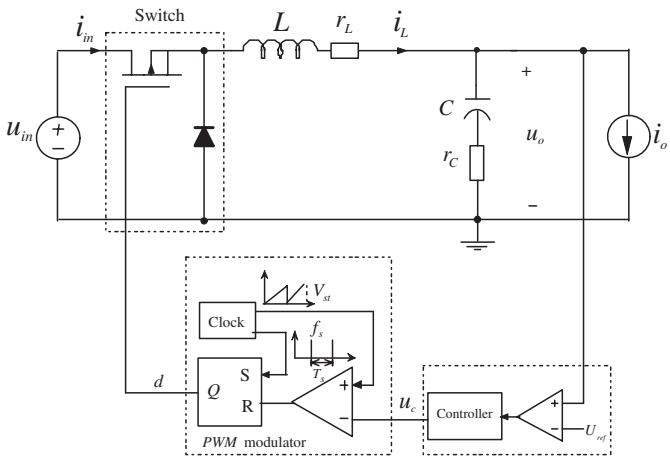


Figure 2.12: VMC buck converter.

$$d(s) = \frac{1}{V_{st}} u_c(s) \tag{2.26}$$

Open-loop transfer functions of voltage-mode-controlled converter

The open-loop small-signal transfer functions of voltage-mode-controlled converter, which describing the input and output dynamics at open loop in CCM and DCM will be considered next.

Continuous conduction mode CCM

The state space equations in (2.4) can be expressed in frequency domain using Laplace transformation as shown in (2.27).

$$s\hat{\mathbf{x}}(s) = \mathbf{A}\hat{\mathbf{x}}(s) + \mathbf{B}\hat{\mathbf{u}}(s) \tag{2.27a}$$

$$\hat{\mathbf{y}}(s) = \mathbf{C}\hat{\mathbf{x}}(s) + \mathbf{D}\hat{\mathbf{u}}(s) \tag{2.27b}$$

where $\hat{\mathbf{x}}(s) = \begin{bmatrix} \hat{i_L}(s) & \hat{u_C}(s) \end{bmatrix}^T$, $\hat{\mathbf{u}}(s) = \begin{bmatrix} \hat{u_{in}}(s) & \hat{i_o}(s) & \hat{d}(s) \end{bmatrix}^T$, $\hat{\mathbf{y}}(s) = \begin{bmatrix} \hat{i_{in}}(s) & \hat{u_o}(s) \end{bmatrix}^T$. Note that the initial conditions have been assumed to be zero.

It is convenient to express the control variable explicitly. For VMC, if the control variable is denoted with $c(s)$, then the open-loop transfer function model of the buck, boost and buck-boost converters can be obtained by inserting the modulator equation (2.26) into the power stage (2.27), yields

$$s\hat{\mathbf{x}}(s) = \mathbf{A}'\hat{\mathbf{x}}(s) + \mathbf{B}'\hat{\mathbf{u}}(s) \tag{2.28a}$$

$$\hat{\mathbf{y}}(s) = \mathbf{C}'\hat{\mathbf{x}}(s) + \mathbf{D}'\hat{\mathbf{u}}(s) \tag{2.28b}$$

where a prime is used to denote altered matrices. According to the matrix algebra, we can solve the system in (2.29) as follows

$$\hat{\mathbf{x}}(s) = \left(s\mathbf{I} - \mathbf{A}'\right)^{-1}\mathbf{B}' \cdot \hat{\mathbf{u}}(s) \tag{2.29a}$$

$$\hat{\mathbf{y}}(s) = \left(\mathbf{C}'(s\mathbf{I} - \mathbf{A}')^{-1}\mathbf{B}' + \mathbf{D}'\right) \cdot \hat{\mathbf{u}}(s) \tag{2.29b}$$

As a result, six unterminated transfer functions (denoted using a superscript '*') of voltage-mode controlled converter are obtained, which characterize the input and output open-loop operation of a switched-mode power converter in CCM, and shown in (2.30) and (2.31) respectively.

$$\begin{bmatrix} \hat{i}_L \\ \hat{u}_C \end{bmatrix} = \begin{bmatrix} G^*_{iL-o} & G^*_{jL-o} & G^*_{cL} \\ G^*_{ic-o} & G^*_{jc-o} & G^*_{cc} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{c} \end{bmatrix} \tag{2.30}$$

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y^*_{in-o} & T^*_{ji-o} & G^*_{ci} \\ G^*_{io-o} & -Z^*_{o-o} & G^*_{co} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{c} \end{bmatrix} \tag{2.31}$$

Here $\hat{c}$ is the control signal and the subscript "-o" denotes open-loop operation.

$Y^*_{in-o} = \frac{\hat{i}_{in}}{\hat{u}_{in}}\Big\vert_{\hat{i}_o,c=0}$	input admittance
$T^*_{ji-o} = \frac{\hat{i}_{in}}{\hat{i}_o}\Big\vert_{\hat{u}_{in},\hat{c}=0}$	reverse (output-to-input) transfer function
$G^*_{ci} = \frac{\hat{i}_{in}}{\hat{c}}\Big\vert_{\hat{u}_{in},\hat{i}_o=0}$	control-to-input transfer function
$G^*_{io-o} = \frac{\hat{u}_o}{\hat{u}_{in}}\Big\vert_{\hat{i}_o,\hat{c}=0}$	forward (line-to-output) transfer function
$Z^*_{o-o} = -\frac{\hat{u}_o}{\hat{i}_o}\Big\vert_{\hat{u}_{in},\hat{c}=0}$	output impedance
$G^*_{co} = \frac{\hat{u}_o}{\hat{c}}\vert_{\hat{u}_{in},\hat{i}_o=0}$	control-to-output transfer function

Consequently, the open-loop output dynamics of a converter (i.e.,$\hat{u}_o$) can be defined as (2.32) and the open loop input dynamics (i.e., $\hat{i}_{in}$) as (2.33), respectively.

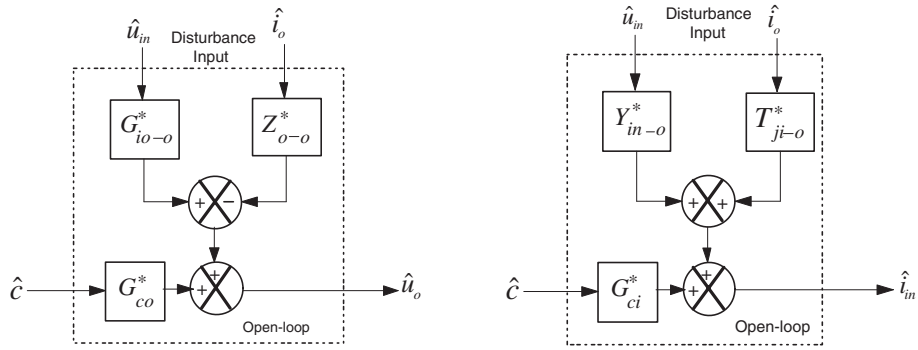
$$\hat{u}_o = G^*_{io-o} \cdot \hat{u}_{in} - Z^*_{o-o} \cdot \hat{i}_o + G^*_{co} \cdot \hat{c} \tag{2.32}$$

$$\hat{i}_{in} = Y^*_{in-o} \cdot \hat{u}_{in} + T^*_{ji-o} \cdot \hat{i}_o + G^*_{ci} \cdot \hat{c} \tag{2.33}$$

The output and input dynamics presented in (2.32) and (2.33), respectively, can be presented also using the control block diagrams shown in Fig. 2.13(a) and 2.13(b). The input variables $\hat{u}_{in}$ and $\hat{i}_o$ are typically known also as *disturbance inputs*.

Discontinuous conduction mode DCM

Similarly, the open-loop transfer functions of voltage-mode-controlled converter in DCM can be obtained by expressing the state-space representation in (2.24) in frequency domain, and then inserting the modulator equation (2.26) into the resulting power stage model.



(a) Output dynamics. (b) Input dynamics.

Figure 2.13: Open-loop voltage-mode control block diagrams.

Closed-loop transfer functions of voltage-mode-controlled converter

The closed loop model of the converter is obtained by combining the open-loop transfer function model with the output voltage feedback. A controller is designed, and a feedback from the output voltage is formed. The corresponding closed-loop control block diagrams are shown in Figs. 2.14(a) and 2.14(b), where G_c is the transfer function of the control circuit, H_v is the sensor gain u_r is the reference voltage, and G_a the gain factor matching the voltage control signal to the internal control signal [35].

The closed-loop transfer functions can be derived directly from Fig. 2.14, or by substituting the control law (2.34) to (2.32) and (2.33) as follows:

$$\hat{c} = -H_v(s)G_cG_a \cdot \hat{u}_o + G_cG_a \cdot \hat{u}_r \tag{2.34}$$

$$\hat{u}_o = G^*_{io-o} \cdot \hat{u}_{in} - Z^*_{o-o} \cdot \hat{i}_o + G_cG_aG^*_{co} \cdot \hat{u}_r - H_v(s)G_cG_aG^*_{co} \cdot \hat{u}_o \tag{2.35}$$

$$\hat{u}_o = \frac{G^*_{io-o}}{1 + H_v(s)G_cG_aG^*_{co}} \cdot \hat{u}_{in} - \frac{Z^*_{o-o}}{1 + H_v(s)G_cG_aG^*_{co}} \cdot \hat{i}_o + \frac{G_cG_aG^*_{co}}{1 + H_v(s)G_cG_aG^*_{co}} \cdot \hat{u}_r \tag{2.36}$$

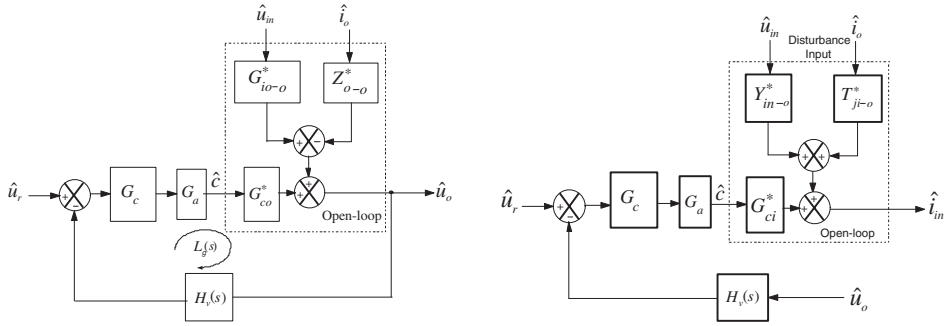
The product of the gains along the path starting from the output voltage and ending at it (i.e., $H_v(s)G_cG_aG^*_{co}$) is known as *loop gain* and denoted as $L^*_g(s)$, where the superscript '*' denotes the unterminated nature of the loop gain. When using the loop gain, the output dynamics may be expressed as (2.37)

$$\hat{u}_o = \frac{G^*_{io-o}}{1 + L^*_g(s)} \cdot \hat{u}_{in} - \frac{Z^*_{o-o}}{1 + L^*_g(s)} \cdot \hat{i}_o + \frac{L^*_g(s)}{1 + L^*_g(s)} \cdot \frac{\hat{u}_r}{H_v(s)} \tag{2.37}$$

where

$$L^*_g(s) = H_v(s)G_cG_aG^*_{co} \tag{2.38}$$

The closed-loop input dynamics can be solved from (2.33) and (2.34) as follows:



(a) Output dynamics. (b) Input dynamics.

Figure 2.14: Closed-loop control block diagrams.

$$\hat{i}_{in} = \left(Y^*_{in-o} - \frac{G^*_{io-o}G^*_{ci}}{G^*_{co}} \cdot \frac{L^*_g(s)}{1+L^*_g(s)} \right) \cdot \hat{u}_{in} + \left(T^*_{ji-o} + \frac{Z^*_{o-o}G^*_{ci}}{G^*_{co}} \cdot \frac{L^*_g(s)}{1+L^*_g(s)} \right) \cdot \hat{i}_o + \frac{G^*_{ci}}{H_v(s)G^*_{co}} \cdot \frac{L^*_g(s)}{1+L^*_g(s)} \cdot \hat{u}_r \tag{2.39}$$

If the reference signal $\hat{u}_r = 0$, then, the closed-loop transfer function matrix is

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y^*_{in-o} - \frac{G^*_{io-o}G^*_{ci}}{G^*_{co}} \cdot \frac{L^*_g(s)}{1+L^*_g(s)} & T^*_{ji-o} + \frac{Z^*_{o-o}G^*_{ci}}{G^*_{co}} \cdot \frac{L^*_g(s)}{1+L^*_g(s)} \\ \frac{G^*_{io-o}}{1+L^*_g(s)} & -\frac{Z^*_{o-o}}{1+L^*_g(s)} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \end{bmatrix} \tag{2.40}$$

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y^*_{in-c} & T^*_{ji-c} \\ G^*_{io-c} & -Z^*_{o-c} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \end{bmatrix} \tag{2.41}$$

The closed-loop input admittance can be rewritten in terms of feedback as follows:

$$Y^*_{in-c} = Y^*_{in-o} \cdot \frac{1}{1+L^*_g(s)} + Y^*_{in-\infty} \cdot \frac{L^*_g(s)}{1+L^*_g(s)} \tag{2.42}$$

where

$$Y^*_{in-\infty} = Y^*_{in-o} - \frac{G^*_{ci}G^*_{io-o}}{G^*_{co}} \tag{2.43}$$

is equal to closed-loop input admittance under the condition that the feedback controller operates ideally [28], and it has a negative value.

$Y^*_{in-\infty}$ may be given as (2.44), (2.45), and (2.46) for the basic converters (i.e., buck, boost, and buck-boost) in CCM without considering the effect of the circuit parasitic elements, respectively.

$$Y^*_{in-\infty} = -\frac{DI_L}{U_{in}} \tag{2.44}$$

$$Y^*_{in-\infty} = -\frac{I_L}{U_{in}} \cdot \frac{1}{1 - s \cdot \frac{LI_L}{U_{in}}} \tag{2.45}$$

$$Y^*_{in-\infty} = -\frac{DI_L}{U_{in}} \cdot \frac{1}{1 - s \cdot \frac{LI_L}{U_{in}}} \tag{2.46}$$

Expression (2.42) shows that typically the closed-loop input admittance varies from negative at low frequencies (i.e. high loop gain) to positive at high frequencies as the loop gain falls below unity [12].

2.7.2 Peak Current-Mode PWM

The resulting expression of the duty cycle of a PCMC converter shows how the perturbations in the input voltage, output voltage, inductor current and control current affect the duty cycle. The expression leads to concept called the duty cycle constraints. The derivation of these is thoroughly explained in [36].

Continuous Conduction Mode CCM

The principles of the duty-ratio generation under PCM control are shown in Fig. 2.15 using a buck converter as an example. In CCM, the time-averaged inductor current lies always in the middle of the inductor current ripple band as shown in Fig. 2.16. The duty ratio under PCM control is established, when the on-time inductor current reaches the compensated control current i_{co}. The state variable is the average inductor current $\langle i_L \rangle$ and the sampling of inductor current takes place when $t = (k + d)T_s$ and the duty-cycle constraints can, therefore be written as in (2.47), where Δi_L is the dynamic distance between the peak inductor current and the average inductor current as shown in Fig. 2.16

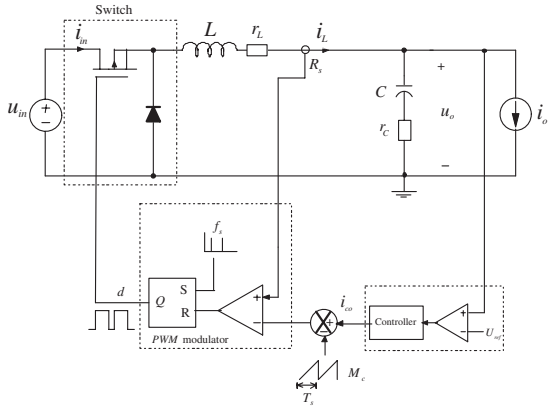


Figure 2.15: PCMC buck converter.

$$i_{co} - M_c d T_s = \langle i_L \rangle + \Delta i_L \tag{2.47}$$

From Fig. 2.16, Δi_L can be derived by solving the following governing equations:

$$\Delta i_L = i_p - \Delta i'_L \tag{2.48}$$

We know that the derivative of the average inductor current $\langle i_L \rangle$ can be approximated as

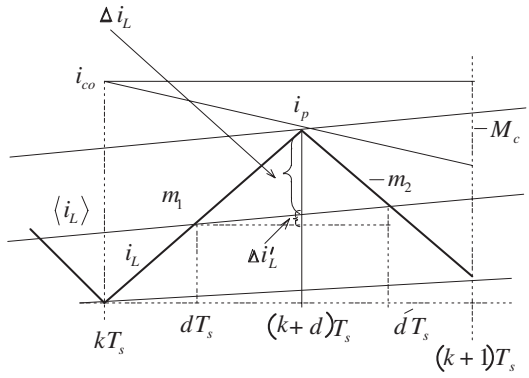


Figure 2.16: The inductor current waveform.

$$\langle i_L \rangle' = dm_1 - (1-d)m_2 \tag{2.49}$$

It follows that

$$\Delta i_L = \frac{1}{2} m_1 dT_s - \frac{1}{2} dT_s \left(dm_1 - d'm_2 \right) = \frac{dd'T_s}{2} \left(m_1 + m_2 \right) \tag{2.50}$$

where m_1 and m_2 are topology-dependent rising and falling slopes of the inductor current. Their expressions for buck, boost and buck-boost converters after neglecting the parasitic elements are shown in Table (2.4).

When (2.50) is inserted into (2.47), we obtain the averaged duty-ratio constraints (2.51) from which the small-signal constraints may be derived by replacing the topology-based up and down slopes and developing the proper partial derivatives:

$$i_{co} - M_c dT_s = \langle i_L \rangle + \frac{dd'T_s}{2} \left(m_1 + m_2 \right) \tag{2.51}$$

which is the same conclusion that has been reached in [37, 36, 38].

To derive the ac-small signal model, equation (2.51) must be linearized. Then general expressions of the small signal of duty-cycle both in time and frequency domain can be obtained

$$\hat{d}(t) = F_m \left[\hat{i}_{co}(t) - \hat{i}_L(t) - f_g \cdot \hat{u}_{in}(t) - f_v \cdot \hat{u}_o(t) \right] \tag{2.52}$$

$$\hat{d}(s) = F_m \left[\hat{i}_{co}(s) - \hat{i}_L(s) - f_g \cdot \hat{u}_{in}(s) - f_v \cdot \hat{u}_o(s) \right] \tag{2.53}$$

where F_m is the duty-cycle gain, f_g is the feedforward gain and f_v is the feedback gain The coefficients are shown in Table (2.4) [36].

It can be noted that the PCMC transfer functions depend strongly on the duty-cycle gain F_m. Therefore, F_m would tend to infinity when there is no compensation (i.e., $M_c = 0$) and

Table 2.4: Duty-cycle constraints coefficients for CCM.

Type	m_1	m_2	F_m	f_g	f_v
Buck	$\frac{u_{in}(t)-u_o(t)}{L}$	$\frac{u_o(t)}{L}$	$\frac{1}{T_s\left[M_c+\frac{(U_{in}+U_D)(1-2D)}{2L}\right]}$	$\frac{T_s}{2L}DD'$	0
Boost	$\frac{u_{in}(t)}{L}$	$-\frac{u_{in}(t)-u_o(t)}{L}$	$\frac{1}{T_s\left[M_c+\frac{(U_o+U_D)(1-2D)}{2L}\right]}$	0	$\frac{T_s}{2L}DD'$
Buck-Boost	$\frac{u_{in}(t)}{L}$	$\frac{u_o(t)}{L}$	$\frac{1}{T_s\left[M_c+\frac{(U_o+U_{in}+U_D)(1-2D)}{2L}\right]}$	$\frac{T_s}{2L}DD'$	$\frac{T_s}{2L}DD'$

the duty cycle D approaches 50% [36]. In order to obtain the maximum duty-cycle limit D_{max} at which F_m would become infinite, the duty-cycle gain can be expressed in a unified form as follows

$$F_m = \frac{1}{T_s\left[M_c + \frac{(D'-D)(M_1+M_2)}{2}\right]} \tag{2.54}$$

Equation (2.54) predicts that the duty-cycle gain F_m will tend to infinity at the vicinity of D_{max} defined by

$$D_{\max} = \frac{1}{2} + \frac{M_c}{M_1 + M_2} \tag{2.55}$$

It can be obviously noted that, the active operation up to $D = 1$ may be ensured if the compensation ramp slope M_c is selected as follows

$$M_c = \frac{M_1 + M_2}{2} \tag{2.56}$$

Discontinuous Conduction Mode DCM

The small-signal modeling of PCM controlled converter in DCM is a similar process as in CCM [39, 36]. The comparator equation (2.47) defined for CCM applies but the dynamic description of Δi_L differs from the corresponding CCM description of (2.50). The inductor-current waveform in DCM is shown in Fig. 2.17.

From Fig. 2.17, Δi_L can be presented using the difference between the peak inductor current and average inductor at $t = (k + d)\, T_s$ as follows [39]

$$\Delta i_L = m_1 d T_s - \frac{m_1 d\,(d + d_1)\, T_s}{2} \tag{2.57}$$

The portion of duty ratio d_1 may be estimated using the relation (2.58) given in [28, 39],

$$d_1 = \frac{m_1}{m_2}.d \tag{2.58}$$

Inserting (2.58) into (2.57), yields

$$\Delta i_L = m_1 d T_s - \frac{m_1\,(m_1 + m_2)\, d^2 T_s}{2m_2} \tag{2.59}$$

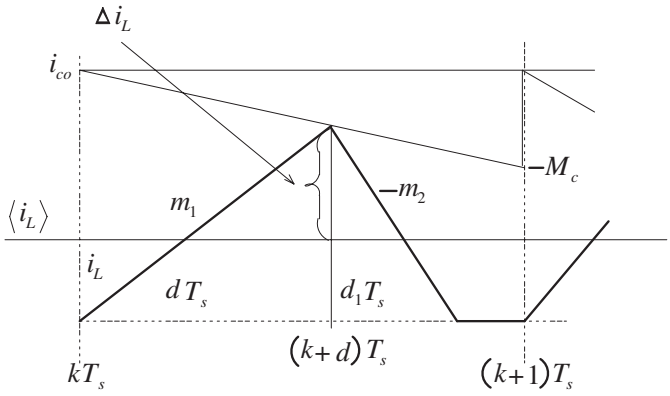


Figure 2.17: The inductor current waveform in DCM.

Substituting (2.59) into the comparator equation (2.47), yields (2.60) from which the coefficients of the duty-cycle constraints of (2.61) can be defined by replacing the inductor-current up and down slopes with their topology-based values and applying the standard linearizing approach. These procedures result in the coefficients of small-signal duty-cycle constraints for a buck, boost and buck-boost converter as given in Table 2.5.

$$i_{co} - M_c d T_s = \langle i_L \rangle + m_1 d T_s - \frac{m_1 \left(m_1 + m_2\right) d^2 T_s}{2 m_2} \tag{2.60}$$

$$\hat{d}(t) = F_m \left[\hat{i}_{co}(t) - \hat{i}_L(t) - f_g \cdot \hat{u}_{in}(t) - f_v \cdot \hat{u}_o(t) \right] \tag{2.61}$$

The general expression of the duty-cycle in frequency domain can be obtained as

$$\hat{d}(s) = F_m \left[\hat{i}_{co}(s) - \hat{i}_L(s) - f_g \cdot \hat{u}_{in}(s) - f_v \cdot \hat{u}_o(s) \right] \tag{2.62}$$

Table 2.5: Duty-cycle constraints coefficients for DCM.

Type	F_m	f_g	f_v
Buck	$\frac{1}{T_s\left[M_c+\frac{U_{in}(1-M)(M-D)}{LM}\right]}$	$\frac{T_s}{L} D \left(\frac{D}{2M^2} - 1\right)$	$\frac{T_s}{L} D \left(1 - \frac{2-M}{2M} D\right)$
Boost	$\frac{1}{T_s\left[M_c+\frac{D' U_{in}\left(M-\frac{1}{D'}\right)}{L(M-1)}\right]}$	$\frac{T_s}{2L} \frac{D^2}{(M-1)^2}$	$\frac{T_s}{L} D \left(1 - \frac{M^2}{2(M-1)^2} D\right)$
Buck-Boost	$\frac{1}{T_s\left[M_c+\frac{D' U_{in}\left(M-\frac{D}{D'}\right)}{LM}\right]}$	$\frac{T_s}{2L} \frac{D^2}{M^2}$	$\frac{T_s}{L} D \left(1 - \frac{2+M}{2M} D\right)$

From the values of the duty-ratio gains F_m given in Table 2.5, it is evident that the duty-ratio gain tends to infinity without compensation (i.e., $M_c = 0$), when M approaches CCM

at the mode limit [28]. Hence, in DCM operation compensation is not necessarily needed.

Open-loop transfer functions of peak-mode-current-controlled converter

The open-loop small-signal transfer functions of peak-current-mode-controlled converter, describing the input and output dynamics at open-loop in CCM and DCM will be shortly discussed in the following.

Continuous conduction mode CCM

For PCMC, the duty-cycle constraints (2.53) must be substituted to (2.27), and then the equations must be manipulated in such a way that the control current is explicitly shown. If the control variable is denoted with $c(s)$, then it follows that six transfer functions are obtained, which characterize the open-loop operation of a current-controlled converter.

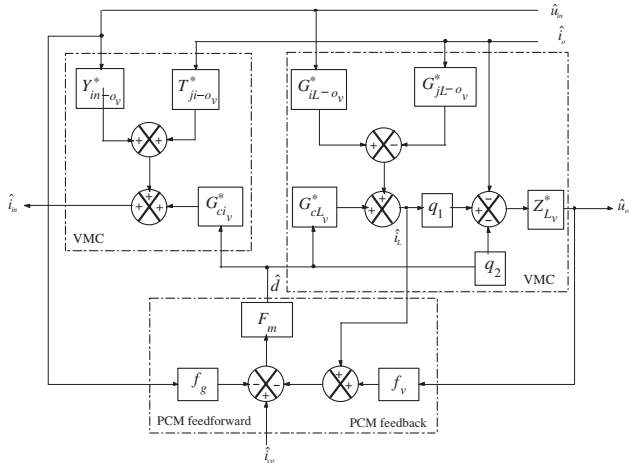


Figure 2.18: Unified small-signal peak-current-mode-controlled converter diagram in CCM.

Peak-current-mode control in CCM is a direct extension of voltage-mode control. Therefore, it is possible to express the PCMC transfer functions as functions of VMC transfer functions and duty-cycle constraints (2.53). The unified small-signal block diagram for basic switching converters is shown in Fig. 2.18, [38].

The coefficients q_1 and q_2 for basic converters are shown in Table 2.6. The VMC basic transfer functions (denoted by subscript extension "v") are as follows

$$G^*_{co_v} = (q_1 G^*_{cL_v} - q_2) Z^*_{L_v} \tag{2.63}$$

$$G^*_{io-o_v} = q_1 G^*_{iL-o_v} Z^*_{L_v} \tag{2.64}$$

$$Z^*_{o-o_v} = (q_1 G^*_{jL-o_v} + 1) Z^*_{L_v} \tag{2.65}$$

where $Z^*_{L_v}$ is the parallel connected output capacitor and load impedance. In the case of unterminated load, we get

$$Z^*_{L_v} = \frac{1 + sr_eC}{sC} \tag{2.66}$$

The feedback loop created by current-mode control is referred to as the *current loop* and is denoted by $L^*_c(s)$. The *voltage loop*, created by the output-voltage feedback path, is denoted by $L^*_v(s)$.

The current and voltage loops can be defined as follows

$$L^*_c(s) = F_m G^*_{ci_v} \tag{2.67}$$

$$L^*_v(s) = F_m f_v G^*_{co_v} \tag{2.68}$$

The PCMC transfer functions (2.69) - (2.74) can be derived from VMC transfer functions and in terms of the loops gains as shown in Fig. 2.18 by solving inductor current and output voltage from the corresponding block diagram.

$$Y^*_{in-o_c} = Y^*_{in-o_v} - \frac{F_m\left(\left(f_v + \frac{1}{q_1 Z^*_{L_v}}\right) G^*_{io-o_v} + f_g\right) G^*_{ci_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.69}$$

$$T^*_{ji-o_c} = T^*_{ji-o_v} + \frac{F_m\left(\left(f_v + \frac{1}{q_1 Z^*_{L_v}}\right) Z^*_{o-o_v} - \frac{1}{q_1}\right) G^*_{ci_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.70}$$

$$G^*_{ci_c} = \frac{F_m G^*_{ci_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.71}$$

$$G^*_{io-o_c} = \frac{\left(1 + \frac{q_2 F_m}{q_1}\right) G^*_{io-o_v} - F_m f_g G^*_{co_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.72}$$

$$Z^*_{o-o_c} = \frac{\left(1 + \frac{q_2 F_m}{q_1}\right) Z^*_{o-o_v} + \frac{F_m}{q_1} G^*_{co_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.73}$$

$$G^*_{co_c} = \frac{F_m G^*_{co_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.74}$$

Discontinuous conduction mode DCM

For DCM, the open-loop transfer functions of peak-current-mode-controlled converter can be obtained by expressing the state-space replantation in (2.24) in frequency domain, and then inserting the modulator equation (2.62) into the resulting power stage model.

Peak-current-mode control in DCM is a direct extension of voltage-mode control. However, it is possible to express the PCMC transfer functions in terms of VMC transfer functions. The corresponding unified small-signal block diagram of switching converter is shown in Fig. 2.19. The coefficients q_3 and q_4 for basic converters are shown in Table 2.6.

The VMC basic transfer functions (denoted by subscript extension "v") are as follows

$$G^*_{co_v} = (G^*_{cL_v} - q_3) Z^*_{L_v} \tag{2.75}$$

$$G^*_{io-o_v} = (G^*_{iL-o_v} - q_4) Z^*_{L_v} \tag{2.76}$$

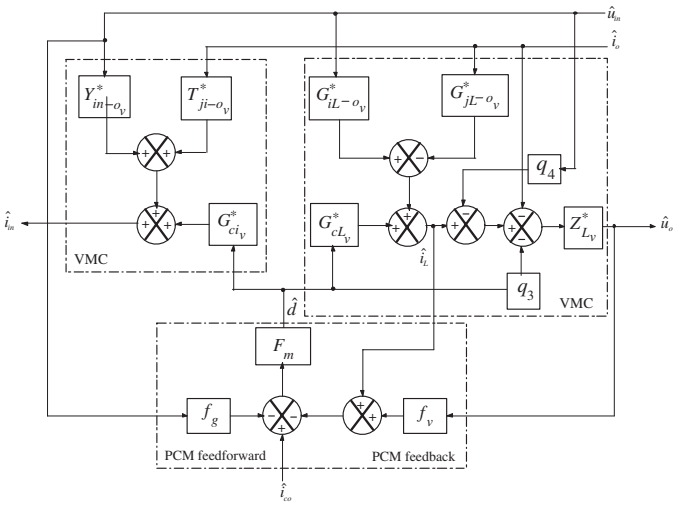


Figure 2.19: Unified small-signal peak-current-mode-controlled converter diagram in DCM.

Table 2.6: The coefficients for basic converters in CCM and DCM.

Type	q_1	q_2	q_3	q_4
Buck	1	0	0	0
Boost	D	I_L	$\frac{2U_o}{R_{eq}}\sqrt{\frac{M-1}{KM}}$	$\frac{M(M-1)}{R_{eq}}$
Buck-Boost	D	I_L	$\frac{2U_o}{R_{eq}\sqrt{K}}$	$\frac{M^2}{R_{eq}}$

$$Z^*_{o-o_v} = (G^*_{jL-o_v} + 1)Z^*_{L_v} \tag{2.77}$$

Similarly, the PCMC transfer functions in DCM (2.80) - (2.83) can be derived from VMC transfer functions and in terms of the loops gains as shown in Fig. 2.19 by solving inductor current and output voltage from the corresponding block diagram.

$$Y^*_{in-o_c} = Y^*_{in-o_v} - \frac{F_m\left(\left(f_v + \frac{1}{Z^*_{Lv}}\right)G^*_{io-o_v} + f_g + q_4\right)G^*_{ci_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.78}$$

$$T^*_{ji-o_c} = T^*_{ji-o_v} + \frac{F_m\left(\left(f_v + \frac{1}{Z^*_{Lv}}\right)Z^*_{o-o_v} - 1\right)G^*_{ci_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.79}$$

$$G^*_{ci_c} = \frac{F_m G^*_{ci_v}}{1 + L^*_c(s) + L^*_v(s)} \tag{2.80}$$

$$G^*_{io-o_c} = \frac{(1+q_3F_m)\,G^*_{io-o_v} - F_m\,(q_4+f_g)\,G^*_{co_v}}{1+L^*_c(s)+L^*_v(s)} \tag{2.81}$$

$$Z^*_{o-o_c} = \frac{(1+q_3F_m)\,Z^*_{o-o_v} + F_m G^*_{co_v}}{1+L^*_c(s)+L^*_v(s)} \tag{2.82}$$

$$G^*_{co_c} = \frac{F_m G^*_{co_v}}{1+L^*_c(s)+L^*_v(s)} \tag{2.83}$$

Chapter 3

Robust Control Design for Switching-Mode Power Converters

Numerous control strategies for designing robust controllers for switching converters have been proposed to find a successful and practical feedback control method. Many of the proposed control strategies are based on optimal control theory. The linear quadratic Gaussian (LQG)/loop transfer recovery methodology was used in [5] to design a controller for a series-parallel resonant converter. In [6], a controller for a buck-boost converter with peak current control was designed using the μ-synthesis procedure. In [7, 8], H_∞ approach was applied to design controllers for boost and buck-boost converters. Nonlinear H_∞-control theory has been applied to regulate a PWM Cuk converter under parameter uncertainties [9]. In [10], H_∞ and μ-synthesis control methods have been applied to Telecom power supplies. But such techniques usually need tedious work to find appropriate weighting functions, and they often result in high order controllers, which are difficult to implement.

Among the robust control techniques that are being currently investigated in power electronics is the quantitative feedback theory (QFT) approach. It was introduced by Horowitz [11] in 1960's. QFT is a frequency domain-based design technique where the controllers can be designed to achieve a set of performance and stability objectives over a specific range of plant parameter uncertainty.

Unlike H_∞ an LQG control, the QFT approach is based on classical ideas of frequency domain shaping of the open-loop transfer function. It also differs in the way that uncertainty is usually characterized, by using gain-phase variations or templates in the Nichols chart. The QFT method has already been applied in the design of different types of control systems, for example in flight control [40, 41] and in robot control systems [42, 43].

In this chapter, QFT approach and associated design for Linear-Time-Invariant systems are presented. A controller adopted to design a robust controller for switching-mode power converters, maximizing the bandwidth of the control loop with a perfect tracking of the desired output voltage, and minimizing the effects of load disturbances over the specified region of plant uncertainties and load disturbances is developed. Consequently, the main contribution of this chapter is to show how the QFT controller methodology can be successfully employed for robust control design of SMPS's subject to system uncertainties due to parameter variations. Different design examples are discussed in this chapter to verify the control design procedures. The effectiveness and robustness of the proposed control system is confirmed by simulation results, where the Matlab^{TM} QFT Frequency Domain Control Design Toolbox [44] and Matlab^{TM}/Simulink SimPowerSystems blockset [45] are used as a setup platform for design and validation.

3.1 Quantitative Feedback Theory (QFT)

QFT is a robust control design framework that offers a transparent design procedure to the engineers in order to generate a good response of the system in spite of disturbance signals and plant uncertainty. Specifically, it employs a two degrees-of-freedom control structure which uses output feedback, a controller, and a prefilter to reduce the variations of the plant output due to plant parameter variations and disturbances.

The QFT method takes into account quantitative information on plant's variability, robust performance requirements, tracking performance specifications, and expected disturbance amplitudes with their attenuation requirements. The controller is designed to ensure that stability, robustness and disturbance rejection requirements are met. The prefilter is then used to tailor the reference step response to meet the other control specifications.

The QFT designs are usually performed using the Nichols chart, a plot of phase as abscissa and log magnitude as ordinate, both parameterized by frequency. Because a whole set of plants, rather than a single plant is considered, the magnitude and phase of the plants (at each selected frequency) yields a set of points on the Nichols chart, which form a connected region, or so-called template. Larger templates indicate larger uncertainty. These templates are then used to define regions (or so-called bounds) in the frequency domain where the system open-loop frequency response must lie. The stability bounds are calculated using these templates. The performance bounds are derived using the templates and the upper and lower limits on the frequency-domain responses. The upper limit of the disturbance bounds is derived based on the disturbance rejection specifications. The controller is determined through the loop shaping process, using a Nichols chart that displays the stability, performance, and disturbance rejection bounds. The disturbance rejection and tracking action of the controller are based on keeping the loop gain above the disturbance and tracking performance within the bounds on the Nichols chart. The stability performance is achieved by keeping the loop transfer function outside the corresponding stability bounds at appropriate frequencies [46, 40]. During the loop shaping process, modifying the poles and zeros of the controller produces immediately visible results, enabling the designer to examine the tradeoffs between controller complexity and system performance [47]. Finally, the prefilter design is conducted using a Bode diagram to shape the closed-loop frequency response, so as to satisfy the tracking performance requirement.

QFT was originally introduced to design robust controllers for highly uncertain, linear time invariant (LTI), single-input/single-output (SISO) systems. Recent research has extended the technique to handle multi input/multi output (MIMO) [40], nonlinear and time varying plants [48]. MIMO systems are mathematically decomposed into their multi input/single-output (MISO) counterparts, where the coupling between the channels is treated as a disturbance that needs to be rejected. A beneficial byproduct of MIMO QFT design is the approximate decoupling of the resulted closed-loop robust control system [40].

3.1.1 Closed-Loop Formulation

The typical two degree of freedom (TDOF) feedback system configuration in QFT is shown in Fig. 3.1. $P(s)$ is the plant transfer function, $H_v(s)$ is feedback sensor transfer function and the transfer functions $G_c(s)$ and $F(s)$ denote the controller and prefilter to be synthesized. The general closed loop specifications of the system in Fig. 3.1 are typically described in terms inequalities on the systems transfer functions from some inputs to some outputs , as follows:

(i) Disturbance rejection at plant output: for a given uncertain set of linear time-invariant

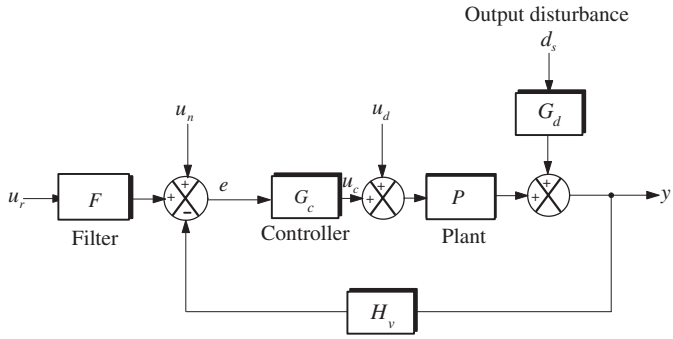


Figure 3.1: Two degree-of-freedom control system.

plants $\forall P \in \{P\}$ the transfer function from the disturbance at the plant output d_s to the plant output y is bounded by

$$\left|\frac{y}{d_s}\right| = |T_D(j\omega)| \leq \gamma_s(\omega) \tag{3.1}$$

where

$$T_D(j\omega) = \frac{G_d(j\omega)}{1 + L_g(j\omega)}$$

$G_d(j\omega)$ is the disturbance frequency response and $L_g(j\omega) = PH_vG_c(j\omega)$ is the loop frequency response.

(*ii*) Disturbance rejection at plant input: for $\forall P \in \{P\}$ the transfer function from the disturbance at the plant input u_d to the plant output y is bounded by

$$\left|\frac{y}{u_d}\right| = \left|\frac{P(j\omega)}{1 + L_g(j\omega)}\right| \leq \gamma_p(\omega) \tag{3.2}$$

(*iii*) Noise rejection: for $\forall P \in \{P\}$ the transfer function from the sensor output u_n to the plant output y is bounded by

$$\left|\frac{y}{u_n}\right| = \left|\frac{PG_c(j\omega)}{1 + L_g(j\omega)}\right| \leq \gamma_n(\omega) \tag{3.3}$$

(*v*) Tracking specification: The tracking specification defines the acceptable range of variations in the closed loop tracking responses of the system due to uncertainty and disturbances. It is generally defined in the time-domain, but normally transformed into the frequency domain. For $\forall P \in \{P\}$ the transfer function from the reference u_r to the plant output y is bounded by

$$T_L(j\omega) \leq |FT(j\omega)| \leq T_U(j\omega) \tag{3.4}$$

where

$$T(j\omega) = \frac{P(j\omega)G_c(j\omega)}{1 + L_g(j\omega)}$$

denotes the closed-loop frequency response without the prefilter, $T_L(j\omega)$ and $T_U(j\omega)$ are the equivalent frequency responses of the lower and upper tracking bounds. These transfer functions are systematically derived from the desired step response of the system.

3.1.2 Robust Performance

Due to parametric uncertainty in frequency responses P, and G_d , there exist corresponding families of transfer functions T, and T_D denoted by $\mathbf{T} = \left[\begin{array}{cccc} T_1 & T_2 & \cdots & T_k \end{array}\right]$, and $\mathbf{T_D} = \left[\begin{array}{cccc} T_{D_1} & T_{D_2} & \cdots & T_{D_k} \end{array}\right]$, where k is the number of plants under uncertainty $\forall P \in \{P\}$.

To proceed with the QFT design, it is necessary to specify the required tolerances on the acceptable closed loop responses in the frequency domain. The performance specifications of interest here are:

Robust Stability

To ensure robust stability of the closed-loop system for a unity feedback sensor (i.e., $H_v = 1$), the following constraint on the peak magnitude of the closed loop frequency responses is set:

$$\left|\frac{\mathbf{L}_g}{1+\mathbf{L}_g}\right| \leq \gamma, \qquad \forall P \in \{P\} \tag{3.5}$$

It corresponds to a minimum gain margin (GM) and phase (PM), [46] as follows:

$$\mathrm{GM} \geq 20\log\left\{\frac{\gamma+1}{\gamma}\right\} \quad [\mathrm{dB}] \tag{3.6}$$

$$\mathrm{PM} \geq 2\sin^{-1}\left\{\frac{1}{2\gamma}\right\} \quad [\mathrm{deg}] \tag{3.7}$$

where $\mathbf{L}_g(j\omega)$ denotes the set of the loop gains frequency responses.

Disturbance Rejection

The general problem is how to design the controller G_c and prefilter F in Fig. 3.1 such that the variation in system output caused by uncertainty and disturbances are reduced. In other words, it is required to reduce the sensitivity [11],

$$S_P^T = \frac{\partial T/T}{\partial P/P} = \frac{1}{1+L_g} \tag{3.8}$$

If controller G_c can be designed such that over a sufficiently wide frequency range $|L_g| \gg 1$ then it is possible to make S_P^T as small as desired so that $\mathbf{T} \approx F$ despite the parametric uncertainty. The response due to the output disturbances $T_D = G_d S_P^T$, will also be improved by decreasing S_P^T. However, there exists a fundamental constraint on the nature of S_P^T in the context of linear time invariant (LTI) feedback control systems: Bode's integral theorem for minimum phase plants [49] states that

$$\int_0^\infty \log\left|S_P^T(j\omega)\right| d\omega = 0 \tag{3.9}$$

Equation (3.9) asserts that if $\left|S_P^T\right| < 1$ over some frequency range then there must exist another frequency range where $\left|S_P^T\right| > 1$ to satisfy the integral. In most practical feedback

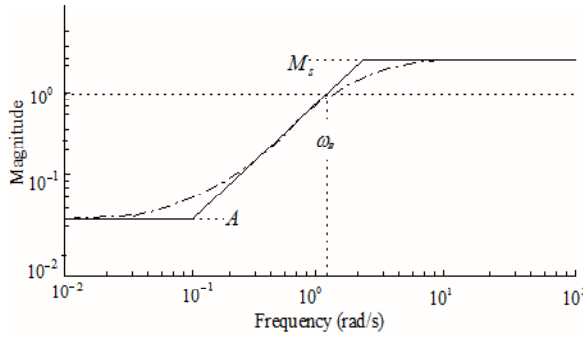


Figure 3.2: Inverse of performance weight function $1/|W_s(j\omega)|$, [50].

control systems, $\left|S_P^T\right| < 1$ up to the crossover frequency, ω_c , where $|L_g(j\omega_c)| = 1$. So, in order to satisfy (3.9), the sensitivity must be larger than unity for some $\omega > \omega_c$. In other words, closing the feedback loop around the plant simply shifts the region of high loop sensitivity from the low frequencies where $|L_g| > 1$ to the high frequencies above ω_c where $|L_g| < 1$ [50].

In general, to fulfill a design specification, such as disturbance attenuation in equation (3.1), the sensitivity function S_P^T is constrained to satisfy

$$\left|\frac{1}{1+\mathbf{L}_g(j\omega)}\right| \leq |1/W_s(j\omega)|\,, \qquad \forall P \in \{P\} \tag{3.10}$$

where $W_s(s)$ is a weighting function related to the desired sensitivity function such that it must hold

$$|\mathbf{T_D}(j\omega)| < 1 \tag{3.11}$$

for all frequencies [50].

The sensitivity function S_P^T is a very good indicator of closed-loop performance. Typical specifications of performance in terms of S_P^T are

(i) the minimum bandwidth frequency ω_B.

(ii) the maximum steady-state tracking error A.

(ii) the maximum peak magnitude M_s of S_P^T.

Mathematically, these specifications are captured by an upper bound (performance weight, $1/|W_s|$), which can be represented e.g. by

$$W(s) = \frac{s/M_s + \omega_B}{s + \omega_B A} \tag{3.12}$$

An asymptotic plot of a typical upper bound $1/|W_s|$ is shown in Fig. 3.2, [50].
In some cases, if faster rolloff is desired, then a higher-order weight may be selected as follows

$$W(s) = \frac{\left(s/\sqrt[k]{M_s} + \omega_B\right)^k}{\left(s + \omega_B \sqrt[k]{A}\right)^k} \tag{3.13}$$

for some integer $k \geq 1$, [49, 50].

Reference Tracking

The reference tracking specification due to plant uncertainty is then formulated as follows

$$T_L(j\omega) \leq |\mathbf{T}(j\omega)| \leq T_U(j\omega) \tag{3.14}$$

Note that the constraints set limits on the time domain transient performance [40].

3.1.3 Uncertainty Model and Plant Templates

A control system is said to be robust if it is insensitive to differences or errors between the actual system and the model of system. These differences or errors are referred to the model uncertainty. That may have several sources such as the variation in parameters of the linear model due to nonlinearities or changes in the operating conditions, measurement errors and high frequency modeling [50].

The various origins of model uncertainty mentioned may be divided into the following main groups:

(A) - Parametric uncertainty

Parametric uncertainty implies specific knowledge of variations in parameters of the transfer function. A general procedure to represent the parametric uncertainty is given e.g. in [50, 51]. The parametric uncertainty can be quantified by assuming that each uncertain parameter a is bounded within region $[a_{min}, a_{max}]$. That is, we have parameter sets which may be expressed as in (3.15). The corresponding plant uncertainty, however, will commonly have the properties illustrated in Fig. 3.3

$$a_p = a_o\left(1 + \sigma\Delta\right), \qquad -1 \leq \Delta \leq 1 \tag{3.15}$$

where a_o is the nominal parameter value, σ is the relative magnitude of the gain uncertainty and Δ is a real scalar.

(B) - Unparametric uncertainty

The main source of unparametric uncertainty is error in the model because of missing dynamics, usually at high frequencies, due to a lack of understanding of the physical process [50]. Only the case of parametric uncertainty is considered in this thesis.

The essential first step in QFT design process is to represent the uncertainty of the system as accurately as possible. When the system is not defined by a single model, but rather has several due to the parametric uncertainty, the frequency responses of the system for a given frequency are represented by a set of points (most often obtained by forming a grid in the uncertain parameter space), as many as there are different models. All of these points define a region of uncertainty on Nichols chart known as *template*. The resulting plant response set should be carefully studied. A generic illustration of "good" and "bad" grid choices are

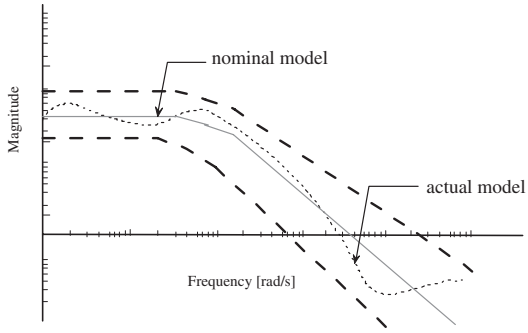


Figure 3.3: Typical behavior of plant uncertainty .

depicted in Fig. 3.4. In general, there are no rules for obtaining a reasonable approximation of the boundary from the structure of the parametric uncertain plant. However, for specific cases, such as transfer functions with coefficients belonging to known intervals or with coefficients related to the uncertain parameters in a linear or multi-linear fashion, some useful results can be found in e.g., [52, 53]. These templates are then used to define regions (or so-called *bounds*) in the frequency domain where the system open-loop frequency response must lie.

In QFT design procedure, the algorithms used for computing bounds require input data in terms of frequency responses (templates) rather than in terms of numerator/denominator transfer functions. For simply connected templates, it is necessary and sufficient to work only with the boundary of these templates [44].

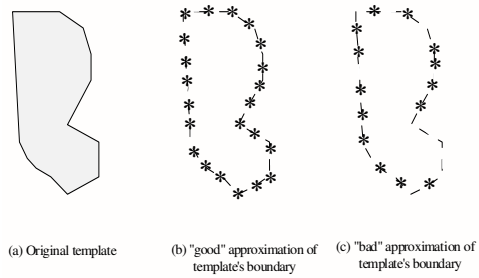


Figure 3.4: "good" and "bad" approximations of a plant template, [44].

3.1.4 QFT Design Procedure

Choice of Frequency Array

In QFT design process, an appropriate frequency band for a computing templates and bounds has to be selected. An important question arises, for which there is no definite

global answer, is how to select this array from the possible range between zero and infinity. Fortunately, for engineering design we need only a small set that can be found with, at the most, a few repetitions. The basic rule is that for the same specification, the bounds will change only with changes in the shape of the template. Therefore, a guideline for selecting the frequency range are to search frequencies where the shape of the template shows significant variations compared to those at other frequencies [44].

Choice of Nominal Plant

In order to compute bounds, it is necessary to choose a plant from the uncertainty set as the nominal plant. If there is no uncertainty the fixed plant is the nominal one. This is required in order to perform QFT design with a single nominal loop. In parametric uncertainty model any plant in P can be chosen as the nominal plant. It is common practice to select a nominal plant which we think is most convenient for design. However, the selected nominal plant must be the same for the rest of the frequencies for which templates are to be obtained.

QFT Bounds Computations

Given the plant templates, QFT converts closed-loop magnitude specifications into magnitude and phase constraints on a nominal open-loop function. These constraints are called QFT bounds. The preferred bound calculation algorithm proposed in [46] (also used by the QFT Matlab$^{\mathrm{TM}}$ toolbox, [44]).

QFT Loop-shaping

The final step in a QFT design involves the design (loop shaping) of a nominal loop function that meets its bounds. The controller design then proceeds using the Nichols chart and classical loop-shaping ideas. The objective is to synthesize a controller, $G_c(s)$, which meets the design specifications and maximizes the controller bandwidth.

QFT Algorithm:

The main steps involved in the QFT design technique can be summarized as

1. Formulating of the closed-loop control performance specifications, i.e., stability margins, tracking and disturbance rejection

2. Generating templates. For a given uncertain plant $P(s) \in \{P\}$, select a series of frequency points ω_i, $i = 1, 2, \cdots, m$ according to the plant characteristics and the specifications. Calculate the value sets of the plant in the complex plane $P(j\omega_i)$, i.e., the so called plant templates at all frequency point ω_i;

3. Computation of QFT bounds. An arbitrary member in the plant set is chosen as the nominal case. At each selected frequency point, combining the stability and performance specifications with the plant template yields stability margin and performance bounds in term of the nominal case. Intersection of all such bounds, i.e., the worst case bound, at the same frequency point yields a single QFT bound. Compute such a QFT bound for all frequency points ω_i, $i = 1, 2, \cdots, m$. Hence the specifications of the closed-loop systems for all $P(s) \in \{P\}$ are translated into that of the open loop nominal case;

4. Loop shaping for QFT controllers. The design of the QFT controller, $G_c(s)$ is accomplished on the Nichols Chart. The phase gain loop shaping technique is employed to design of the controllers, $G_c(s)$, until the QFT bounds at all frequencies are satisfied and the closed-loop nominal system is stable;

5. Design of prefilters $F(s)$. The Final step in QFT is to design the prefilter, $F(s)$, such that the performance specifications are satisfied.

3.1.5 QFT Design for Uncertain Non-minimum Phase Systems

In addition, an underlying requirement of the controller design is to minimize sensitivity to load changes and attenuate input-output transmission over as large a bandwidth as possible. A major problem is encountered, however, when the transfer function of the power stage (i.e. control-to-output transfer function) has a right-half-plane zero (RHPZ). In such cases (e.g., boost or buck-boost converters), the presence of the RHPZ contributes additional phase lag to the system restricting severely the closed-loop bandwidth .

The key idea behind the method used in [54, 55, 40] is to convert a loop-shaping problem of a non-minimum phase nominal plant to that for a stable minimum phase nominal plant by shifting robust stability and performance bounds. The reason is that in numerical design it is more convenient to work with a minimum phase function because the optimal loop shaping procedures then can be derived [55].

The formulation of the QFT design for non-minimum phase systems used in this Section is identical to the detailed formulation in [54] and [55].

Consider a non-minimum phase uncertain plant

$$P(s) = \frac{N(s)\hat{N}(-s)}{D(s)} \tag{3.16}$$

where $\hat{N}(-s)$ denotes the part with right half plane zeros explicitly.

The QFT design problem is to find a controller $G_c(s)$ and a prefilter $F(s)$ such that conditions (3.5), (3.10) and (3.14) are satisfied and the nominal plant is stabilized. An arbitrarily chosen nominal plant $P_o(s)$ within the plant family is given by

$$P_o(s) = \frac{N_o(s)\hat{N}_o(-s)}{D_o(s)} \tag{3.17}$$

Now let

$$A(s) = \frac{\hat{N}_o(-s)}{\hat{N}_o(s)} \tag{3.18}$$

where $A(s)$ is all-passing with property

$$|A(j\omega)| = 1, \qquad \text{for all } \omega \in [0, \infty) \tag{3.19}$$

The new nominal plant is defined as

$$P'_o(s) = P_o(s)A(s)^{-1} = \frac{N_o(s)\hat{N}_o(s)}{D_o(s)} \tag{3.20}$$

Obviously $P'_o(s)$ is a stable minimum phase plant. Furthermore we have

$$L_g(s) = P(s)G_c(s) = P'(s)G_c(s)A(s) = L'_g(s)A(s) \tag{3.21}$$

with

$$P'(s) = \frac{N(s)\hat{N}(-s)\hat{N}_o(s)}{D(s)\hat{N}_o(-s)} \tag{3.22}$$

and

$$L'_g(s) = P'(s)G_c(s) \tag{3.23}$$

Since $A(s)$ defined in (3.19) is all-passing, this implies

$$|1 + L_g(s)| = \left|1 + L'_g(s)A(s)\right| = \left|A(s)^{-1} + L'_g(s)\right| \tag{3.24}$$

The robust stability margin in (3.5) becomes

$$\left|\frac{L_g(j\omega)}{1 + L_g(j\omega)}\right| = \left|\frac{L'_g(j\omega)}{A(j\omega)^{-1} + L'_g(j\omega)}\right| \leq \gamma \tag{3.25}$$

$L'_g(j\omega)$ under the allowable uncertainties must satisfy condition (3.25).

Similar conditions can be found for the bounds of tracking performance and disturbance rejection, respectively in (3.26) and (3.27).

$$T_L(j\omega) \leq \left|\frac{L'_g(j\omega)}{A(j\omega)^{-1} + L'_g(j\omega)}\right| \leq T_U(j\omega) \tag{3.26}$$

$$\left|\frac{1}{A(j\omega)^{-1} + L'_g(j\omega)}\right| \leq |1/W_s(j\omega)| \tag{3.27}$$

It has been proved in [55] that, the bounds imposing on $L'_g(j\omega)$ by (3.25), (3.26) and (3.27) are the same as the bounds imposing on $L_g(j\omega)$ by (3.5), (3.10) and (3.14) but with horizontal shift of $-\arg A(j\omega)$. In other words, the bounds for robust stability margin, tracking and disturbance specifications for the stable minimum phase nominal plant $P'_o(j\omega)$ are therefore the same as that for the non-minimum phase nominal plant $P_o(j\omega)$ but with a horizontal (in the Nichols plane) shift of phase $-\arg A(j\omega)$ at frequency ω_i. That is, the bounds for the new nominal plant $P'_o(j\omega)$ are obtained by shifting the bounds for the nominal plant $P_o(j\omega)$ by $-\arg A(j\omega)$, [54, 55].

3.2 QFT-Based Robust Controller Design for Switching-Mode Power Converters

Use of regulated high-frequency DC/DC converters is increasing rapidly in powering all kind of electronic equipment and systems in industrial and consumer applications. However, the dc-dc switching converters require a high degree of dynamic regulation. In such cases, switching regulators have to provide robust behavior in spite of load variations or input voltage perturbations.

In this section, the problem of designing a QFT controller for switching-mode power converters that maximizes the bandwidth control loop with a perfect tracking of the desired output voltage and minimizing the effects of load disturbances will be analyzed. The Matlab QFT Frequency Domain Control Design Toolbox [44] is used for the design and validation, since it includes a convenient graphical user interface (GUI) to be used in the interactive loop-shaping process needed in applying the control method based on QFT.

3.2.1 Voltage-Mode-Controlled Converter

In the following a typical low-power buck converter, shown in Fig. 3.5, is considered, where u_o is the output voltage and u_{in} is the input voltage. The converter load is represented by impedance Z_L with the current source j_o, while C and L represent the capacitor and inductor, whose equivalent series resistances are r_C and r_L. The MOSFET on-time channel resistance r_{ds} and the dynamic resistance r_d associated to the fly-wheeling diode are also taken into account.

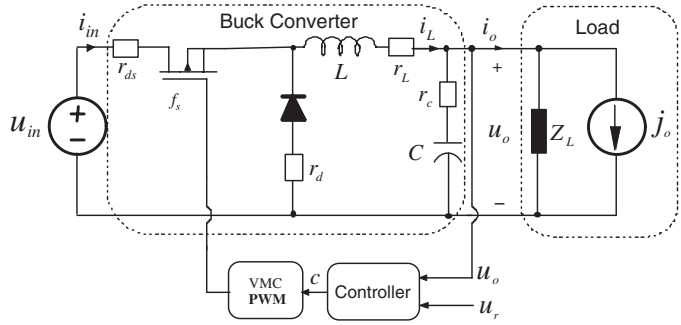


Figure 3.5: Voltage-mode-controlled buck converter.

The control-to-output $G^*_{co}(s)$, output impedance $Z^*_{o-o}(s)$ and line-to-output (audio susceptibility) $G^*_{io-o}(s)$ are of interest, and these transfer functions are given as follows:
When the converter is operating in CCM, we get

$$G^*_{co} = \frac{\frac{V_{st}(U_{in}+U_D+(r_d-r_{ds}))I_o(1+sr_CC)}{LC}}{s^2+\frac{(r_L+r_c+Dr_{ds}+(1-D)r_d)}{L}+\frac{1}{LC}} \tag{3.28}$$

$$Z^*_{o-o} = -\frac{\frac{(r_L+Dr_{ds}+(1-D)r_d+sL)(1+sr_CC)}{LC}}{s^2+\frac{(r_L+r_c+Dr_{ds}+(1-D)r_d)}{L}+\frac{1}{LC}} \tag{3.29}$$

$$G_{io-o} = \frac{\frac{D(1+sr_CC)}{LC}}{s^2+\frac{(r_L+r_c+Dr_{ds}+(1-D)r_d)}{L}+\frac{1}{LC}} \tag{3.30}$$

And when the converter is operating in DCM, the corresponding transfer functions are as follows

$$G_{co} = \frac{\frac{2V_{st}U_{in}(1+sr_CC)}{LC}}{s^2 + s \cdot \frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{1}{LC}\sqrt{\frac{K}{1-M}} \cdot \frac{1}{1-M}} \tag{3.31}$$

$$Z_{o-o} = \frac{\frac{(sL+R_{eq}\sqrt{\frac{K}{1-M}})(1+sr_CC)}{LC}}{s^2 + s \cdot \frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{1}{LC}\sqrt{\frac{K}{1-M}} \cdot \frac{1}{1-M}} \tag{3.32}$$

$$G_{io-o} = \frac{\frac{\frac{M(2-M)}{LC(1-M)}\sqrt{\frac{K}{1-M}}\cdot(1+sr_CC)}{LC}}{s^2 + s \cdot \frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{1}{LC}\sqrt{\frac{K}{1-M}} \cdot \frac{1}{1-M}} \tag{3.33}$$

Table 3.1 defines the buck converter model parameters and summarizes the nominal values of all model parameters and their variations used in controller design ($L = 5\mu$F in DCM) [56]. The modulator gain is $V_{st} = 3$ V.

Table 3.1: Nominal model parameters and their ranges

Uncertain parameter	Nominal Value	Variations
U_o	10V	...
U_{in}	50V	20-70V
P_{out}	30W	$10\% \sim 90\%$
L	105μH	$\pm 50\%$
C	316μF	$\pm 20\%$
r_C	33mΩ	+90%
r_L	0.06mΩ	+90%
U_D	0.3V	$\pm 20\%$
r_{ds}	400mΩ	+90%
r_d	55mΩ	+90%
f_s	100kHz	...

Closed-Loop Analysis

The proposed two degree-of-freedom (TDOF) feedback voltage-mode control structure is shown in Fig. 3.6. The closed-loop responses due to changes in the reference voltage $\hat{u}_r$, and disturbance input voltage $\hat{u}_{in}$, and output current $\hat{i}_o$ are given by

$$T = \frac{\hat{u}_o}{\hat{u}_r} = \frac{FL_g^*}{1 + L_g^*} \tag{3.34}$$

$$T_{D1} = \frac{\hat{u}_o}{\hat{u}_{in}} = \frac{G_{io-o}^*}{1 + L_g^*} \tag{3.35}$$

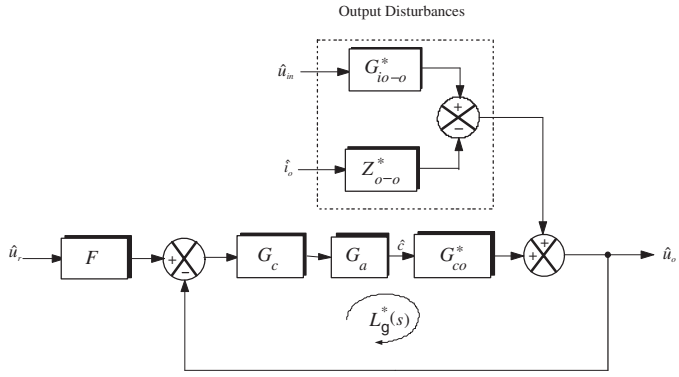


Figure 3.6: TDOF control-block diagram for converter output dynamics.

$$T_{D2} = \frac{\hat{u}_o}{\hat{i}_o} = -\frac{Z^*_{o-o}}{1 + L^*_g} \tag{3.36}$$

where function $L^*_g = G_c G_a G^*_{co}$ is the output-voltage-loop gain, G_c is the controller and G_a is the modulator gain (i.e., in VMC, $G_a = 1/V_{st}$ and in PCMC, $G_a = 1/R_s$).

Due to parametric uncertainty in transfer functions G^*_{co}, G^*_{io-o} and Z^*_{o-o}, there exist corresponding families of transfer functions T, T_{D1} and T_{D2} denoted by $\mathbf{T} = [\, T_1 \;\; T_2 \;\; \cdots \;\; T_k \,]$, $\mathbf{T_{D1}} = [\, T_{D1_1} \;\; T_{D1_2} \;\; \cdots \;\; T_{D1_k} \,]$ and $\mathbf{T_{D2}} = [\, T_{D2_1} \;\; T_{D2_2} \;\; \cdots \;\; T_{D2_k} \,]$, where k is the number of plants under uncertainty. The general problem is how to design the controller G_c and prefilter F in Fig. 3.6 such that the variation in system output caused by uncertainty and disturbances are reduced and the closed-loop nominal system is stable.

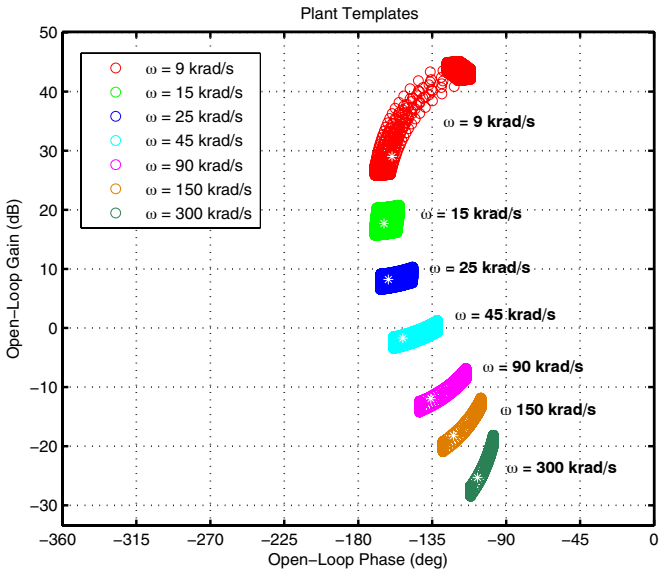
Template Generation

The creation of templates for uncertain plants is an essential first step in QFT design process. The most common method of generating the plant template is to grid the parameter set and calculate the transfer function values on the discrete parameter points.

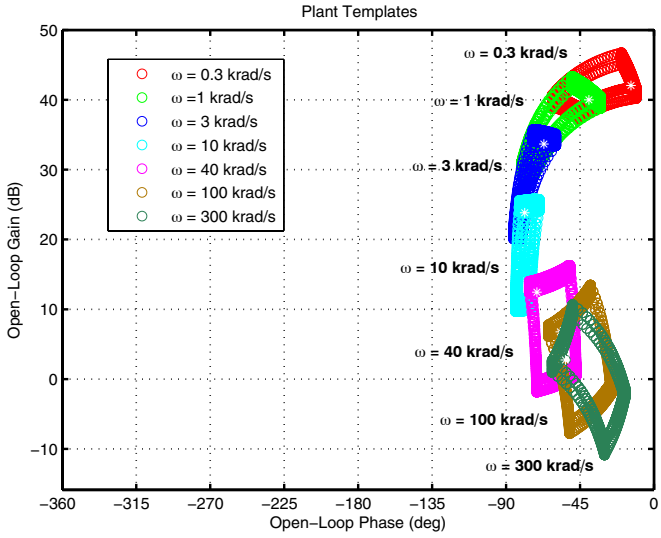
The plant templates are plotted on the Nichols chart at useful selected frequency array $\omega = \{9,\ 15,\ 25,\ 45,\ 90,\ 150,\ 300$ krad/s$\}$ for the CCM and $\omega = \{0.3,\ 1,\ 3,\ 10,\ 40,\ 100,\ 300$ krad/s$\}$ for the DCM, (i.e. frequency range up to half the switching frequency $f_s = 100$ kHz), by computing $G_{co}(j\omega)$ over the set of plants. It is very important that the plant templates are carefully inspected before proceeding with the design. Viewing templates verifies that the template boundary approximation is reasonable and that an appropriate frequency array has been selected. The templates obtained for the family of plants $\mathbf{G_{co}} = \{\, G_{co_1}, \ldots, G_{co_k} \}$ and for the set of frequencies for the CCM and DCM are illustrated in Fig. 3.7, where the nominal plant is indicated by a star in the templates.

Closed-Loop Performance Specifications

To proceed with the QFT design, it is necessary to specify the required tolerances on the acceptable closed-loop responses $\mathbf{T}$, $\mathbf{T_{D1}}$ and $\mathbf{T_{D2}}$ in the frequency domain. The performance specifications of interest here are:



(a) CCM.



(b) DCM.

Figure 3.7: Plant templates.

i. Robust Stability

ii. Reference Tracking

iii. Disturbance Rejection.

These specifications are used to compute the frequency dependent QFT bounds, $B(\omega)$, that guide the shaping of the nominal loop transmission $L^*_{g_{nom}} = G_c G^*_{co_{nom}}$.

i. Robust Stability

To ensure robust stability of the closed-loop system, the following constraint on the peak magnitude of the closed loop frequency responses is set:

$$\left| \frac{\mathbf{L}_g(j\omega)}{1 + \mathbf{L}_g(j\omega)} \right| \leq \gamma, \qquad \forall\, G_{co} \in \mathbf{G_{co}} \tag{3.37}$$

With specifications $\gamma_{(CCM)} = 1.2$ and $\gamma_{(DCM)} = 1.15$, the corresponding minimum gain and phase margins are obtained using equations (3.6) and (3.7), which give 5.26 dB, 5.43 dB, 49° and 51.5°, respectively.

ii. Reference Tracking

An acceptable range of variations in the closed loop tracking responses of the system due to uncertainty and disturbances is expressed as

$$|T_L(j\omega)| \leq |\mathbf{T}(j\omega)| \leq |T_U(j\omega)|\,, \qquad \forall\, G_{co} \in \mathbf{G_{co}} \tag{3.38}$$

where $\mathbf{T}(s)$ denotes the set of the closed-loop transfer functions, and $T_L(s)$ and $T_U(s)$ are the equivalent transfer functions of the lower and upper tracking bounds. These transfer functions are systematically derived from the desired step response of the system with a settling time of less than 0.1 ms, an overshoot of less 2% and a steady state error of less than 0.1% in step response. The equivalent bound transfer functions for the CCM are derived [40] as follows

$$T_U(s) = \frac{3.1 \times 10^4 \left(s + 1.5 \times 10^5\right)}{\left(s^2 + 10.66 \times 10^4 s + 4.66 \times 10^9\right)}, \tag{3.39a}$$

$$T_L(s) = \frac{2.57 \times 10^{19}}{\left(s + 11 \times 10^4\right)\left(s + 6.83 \times 10^4\right)\left(s + 5 \times 10^4\right)} \tag{3.39b}$$

iii. Disturbance Rejection

In general, to fulfill a design specification, such as disturbance attenuation in equations (3.35) and (3.36), the sensitivity function $S^T_{G_{co}}$ is constrained to satisfy

$$\left|S^T_{G_{co}}\right| = \left| \frac{1}{1 + \mathbf{L}_g(j\omega)} \right| \leq \left|1/W s(j\omega)\right|, \qquad \forall\, G_{co} \in \mathbf{G_{co}} \tag{3.40}$$

where $W_s(s)$ is a weighting function related to the desired sensitivity function such that it must hold

$$|\mathbf{T_{D1}}(j\omega)| < 1, \quad \text{and} \quad |\mathbf{T_{D2}}(j\omega)| < 1 \tag{3.41}$$

at all frequencies.

The weighting function $W_s(s)$ in (3.42) is constructed based on the expression shown in (3.13). The design specifications for the performance of the buck converter is a minimum bandwidth frequency of 4.5×10^4 rad/s (with a minimum cross-over frequency $f_c = 10$ kHz),

a maximum steady-state tracking error of 0.035 and a maximum peak magnitude of the sensitivity function of 1.6.

$$W_s(s) = \frac{0.625\left(s^2 + 11.38 \times 10^3 s + 3.24 \times 10^9\right)}{\left(s^2 + 1.684 \times 10^4 s + 7.088 \times 10^7\right)} \tag{3.42}$$

All performance specifications involved in the QFT controller design for voltage-mode-controlled buck converter operating in CCM and DCM are summarized in Table 3.2.

Table 3.2: Robust Performance Specifications

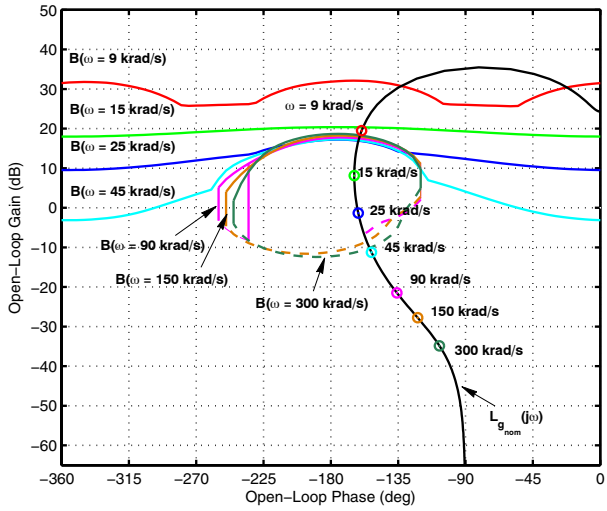
Performance specifications		CCM	DCM
Robust stability	γ	1.2	1.15
Upper bound	$T_U(s)$	$\frac{3.1\times10^4\left(s+1.5\times10^5\right)}{(s^2+10.66\times10^4 s+4.66\times10^9)}$	$\frac{2.91\times10^3\left(s+0.22\times10^5\right)}{(s^2+10.4\times10^3 s+6.4\times10^7)}$
Lower bound	$T_L(s)$	$\frac{2.57\times10^{19}}{(s+11\times10^4)(s+6.83\times10^4)(s+5\times10^4)}$	$\frac{7.9\times10^{15}}{(s+0.65\times10^4)(s+0.8\times10^4)^2(s+1.9\times10^4)}$
Weighting function	$W_s(s)$	$\frac{0.625\left(s^2+11.38\times10^3 s+3.24\times10^9\right)}{(s^2+1.684\times10^4 s+7.088\times10^7)}$	$\frac{0.769\left(s^2+12.1\times10^3 s+36.53\times10^6\right)}{(s^2+250.8s+1.573\times10^4)}$

The intersection of the important QFT bounds, $B(\omega)$, for each inequality (3.5), (3.38) and (3.10) was computed on the Nichols chart at a number of design frequencies based on plant templates and the performance specifications of voltage-mode-controlled buck converter operating in CCM and DCM , as depicted in Fig. 3.8(a) and 3.8(b). The vertical curve line represents the frequency response of the nominal open-loop transfer function $L_{g_{nom}}(s)$ with the controller $G_c = 1$ at several points marked in different colors. These points correspond to the response of the loop for the various frequencies, following the same color code as in the bounds. The wavy lines in the upper area represent the worst case of the tracking and sensitivity reduction bounds at different selected frequencies and the closed round lines in the central area represent the worst case of the robust stability bounds. The bound plotted with a *solid line* implies that $L_{g_{nom}}(s)$ must lie above or on it in order to meet the performance specifications. On the other hand, the bound plotted with a *dashed line* implies that $L_{g_{nom}}(s)$ must lie below or on it in order to meet the performance specifications, [46].

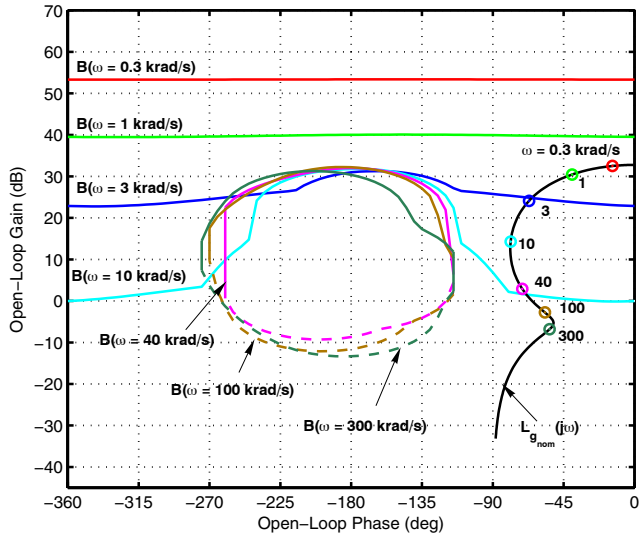
QFT Loop-shaping controller

The controller design then proceeds using the Nichols chart and classical loop-shaping ideas. The objective is to synthesize a controller, G_c, which satisfies the design specifications so that the converter is stable and quickly regulates the output voltage against changes in input voltage or load conditions. Fast response requires that the loop gain cross-over frequency f_c be as high as possible. In general, the controller is designed such that $(f_s/10) < f_c < (f_s/5)$; where f_s is the switching frequency of the converter [58].

This part of the design process is not automatic but depends on the skill of the designer. Generally speaking, loop shaping involves adding poles and zeros until the nominal loop lies near its bounds and results in nominal closed-loop stability. Fig. 3.8(a) shows the frequency



(a) CCM.



(b) DCM.

Figure 3.8: Open-loop frequency response and QFT bounds $B(\omega)$.

response of the nominal open-loop transfer function, which violates the stability bounds. The design objective is to apply dynamic compensation to the nominal open-loop transfer function, so that the performance bounds are satisfied at each frequency. From Fig. 3.8(a), it is seen that the open-loop frequency response is located below the appropriate tracking performance bounds at each trial frequency. Thus an appropriate control gain should be

introduced to push the open-loop frequency response upwards. Moreover, the open-loop frequency response has also crossed the stability bounds. Hence a dynamic compensator is required to change the shape of the open-loop frequency response. Analysis then shows that a pole at the origin in addition to two pole-zero pairs should be added.

The pole at the origin provides a very high gain at low frequencies as an integral control and the pole-zero pairs result in a reduced phase shift between the frequency of the two zeros and the frequency of two poles as a lead controller.

In this way, once the loop is adjusted, it is simple to obtain the transfer function of the controller as follows

$$\begin{aligned} G_c(s) &= \frac{5928\,(s/1617+1)\left(s/1.7\times10^4+1\right)}{s\left(s/1.766\times10^5+1\right)\left(s/1.369\times10^5+1\right)} \\ &= \frac{5928\left(879.5s+14.22\times10^5\right)\left(s+1.7\times10^4\right)}{s\,(s+1.766\times10^5)\,(s+1.369\times10^5)} \end{aligned} \tag{3.43}$$

The resulting open-loop frequency response with this controller is illustrated in Fig. 3.9(a). It is obvious that the open-loop frequency response does not violate the stability performance requirements. Also the loop gain has a cross-over frequency of 17 kHz and a phase margin of nearly 60° with an infinite gain margin when the converter is operating in CCM.

A similar loop-shaping analysis can be performed when a converter operates in DCM. From Fig. 3.8(b), analysis shows that a pole at the origin in addition to two pole-zero pairs are enough to design a controller which meets all the performance requirements. The transfer function of the controller can be then obtained as follows

$$\begin{aligned} G_c(s) &= \frac{3608\,(s/3141+1)\left(s/6.814\times10^5+1\right)}{s\left(s/2.834\times10^5+1\right)\left(s/9.059\times10^4+1\right)} \\ &= \frac{3608\left(12s+37.69\times10^4\right)\left(s+6.81\times10^5\right)}{s\,(s+2.834\times10^5)\,(s+9.059\times10^4)} \end{aligned} \tag{3.44}$$

The resulting open-loop frequency response with this controller is illustrated in Fig. 3.9(b). It's obvious that the open-loop frequency response does not violate the stability performance requirements. Also the loop gain has a cross-over frequency of f_c= 9.9 kHz and a phase margin of 72°. However the tradeoff between system response and system stability prevails.

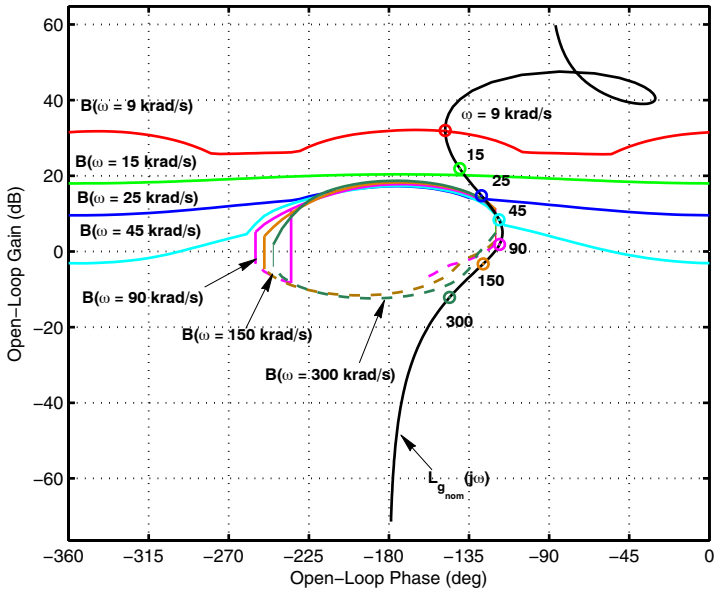
The controllers obtained are robust, that is, they provide good results for all of the family of plants defined under uncertainty, not only for the nominal plant used in the loop-shaping stage. The stability performance analysis of the closed-loop system in the next section also supports this observation, which will later be seen in Fig. 3.14.

Fig. 3.10 shows the Bode magnitude plot of the closed-loop frequency response without a prefilter, together with the tracking frequency response specifications plotted with dashed lines. Obviously dynamic prefilter are required to shape the frequency response to be within the required envelope and attenuate high frequency peaking. They were designed for the CCM and DCM, respectively as follows

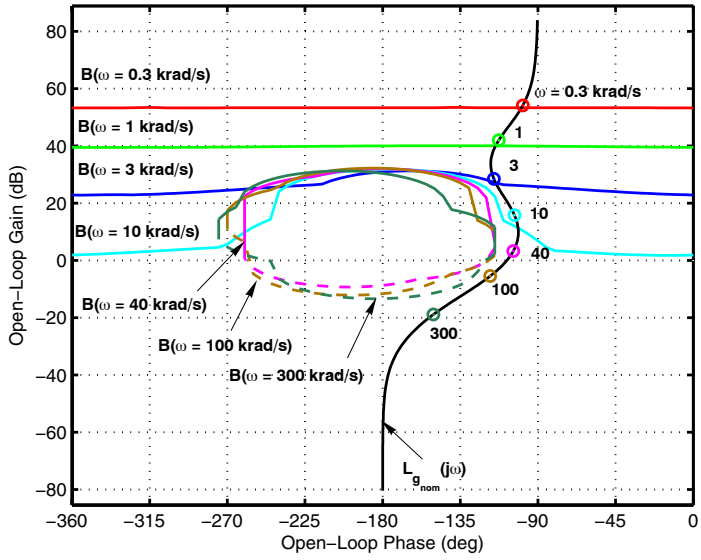
$$F(s) = \frac{5.514\times10^4}{\mathrm{s}+5.514\times10^4}, \tag{3.45}$$

$$F(s) = \frac{3.742\times10^3}{s+3.742\times10^3} \tag{3.46}$$

The resulting closed-loop frequency response with these prefilters are shown in Fig. 3.11.

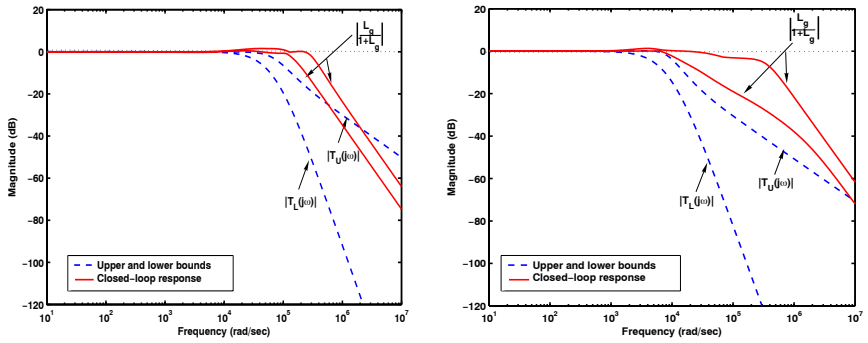


(a) CCM.



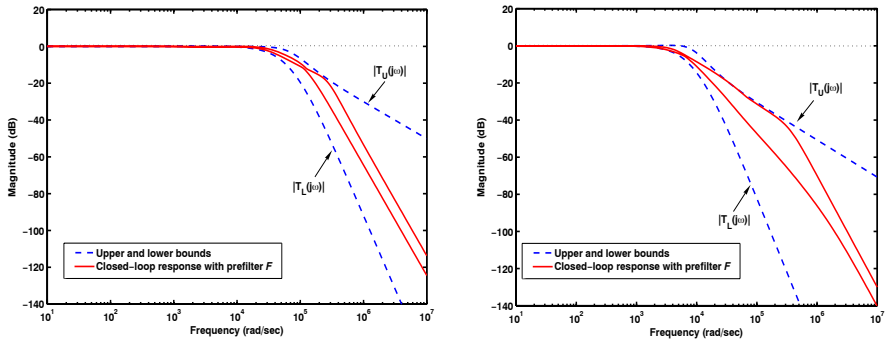
(b) DCM.

Figure 3.9: Open-loop frequency response with controller



(a) CCM. (b) DCM.

Figure 3.10: Closed-loop frequency response without prefilter



(a) CCM. (b) DCM.

Figure 3.11: Closed-loop frequency response with prefilter

Performance Validation and Simulation

To verify the design of QFT controller (3.43)-(3.44), a validation of the obtained results should be made, graphically checking the specifications in the frequency and time domains. Moreover, this validation is essential, since the design has been made only for a finite set of frequencies and hence it cannot be ensured, a priori, that it will be fulfilled for any other frequency, inside or outside this range.

Analyzes of the closed-loop system performance in the frequency domain show that the worst closed-loop response magnitude (covering all uncertainty cases) is well below the specified value ($\gamma = 1.2 = 1.58$ dB, dashed line) (refer to (3.37), as illustrated in Fig. 3.14(a). The maximum variation of the closed-loop system frequency response is well within the specified range (refer to (3.38)-(3.39b)), as illustrated in Fig. 3.12(a). Thus the closed-loop control system has met all the design specifications in the voltage-mode control. The time-domain simulation results, illustrated in Fig. 3.12(b) together with the specified tracking bounds plotted with dashed lines, further support the above conclusion.

A similar analysis in DCM reveals that the worst closed-loop response magnitude (cover-

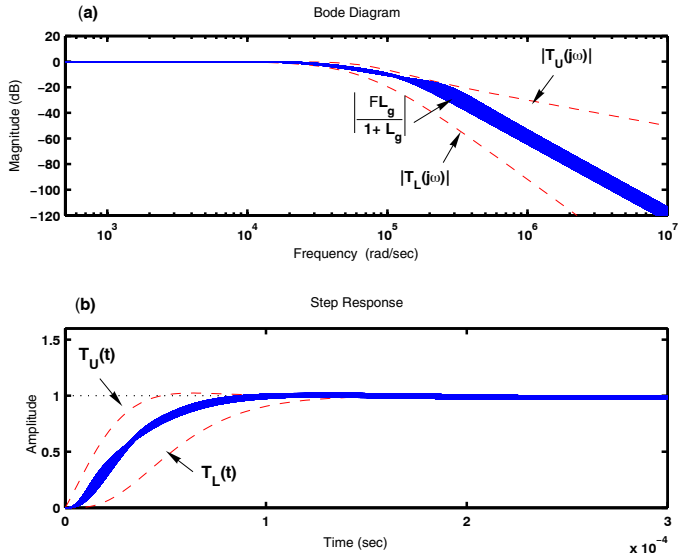


Figure 3.12: Closed-loop responses in CCM: (a) frequency response; (b) unit step response.

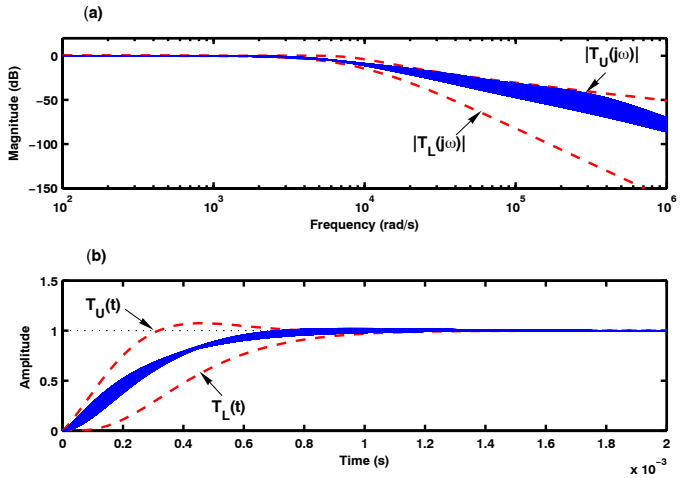
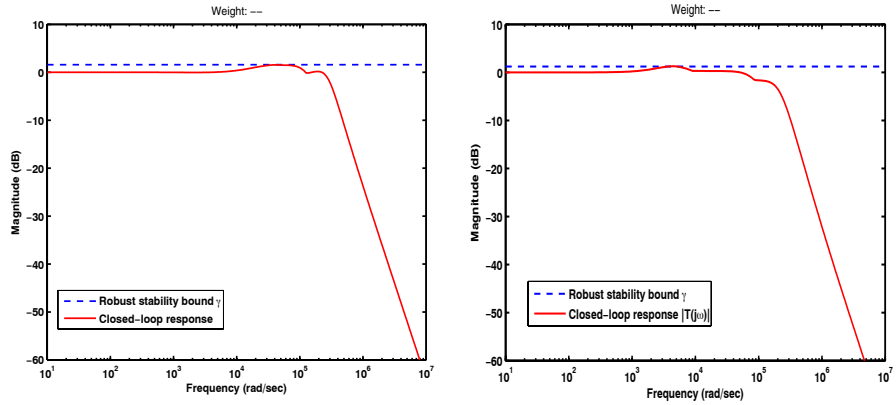


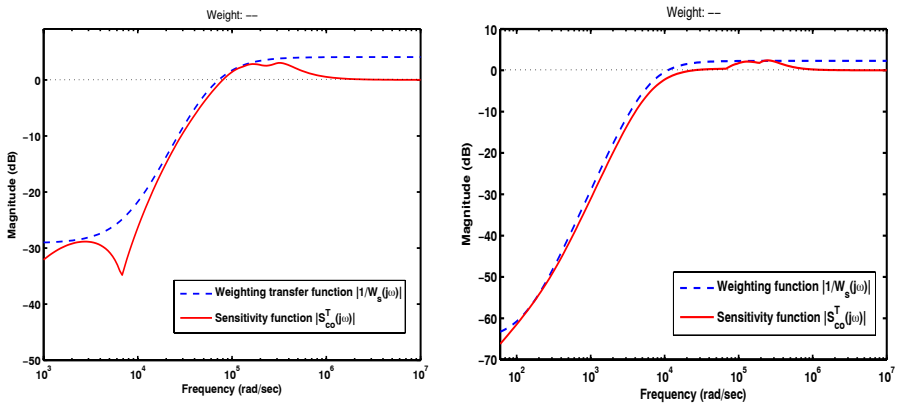
Figure 3.13: Closed-loop responses in DCM: (a) frequency response; (b) unit step response.

ing all uncertainty cases) is well below the specified value ($\gamma = 1.15 = 1.21$ dB, dashed line) as depicted in Fig. 3.14(b). The maximum variation of the closed-loop system frequency and time responses are well within the specified range as illustrated in Fig. 3.13(a) and 3.13(b), respectively.



(a) CCM. (b) DCM.

Figure 3.14: Closed-loop robust stability margins



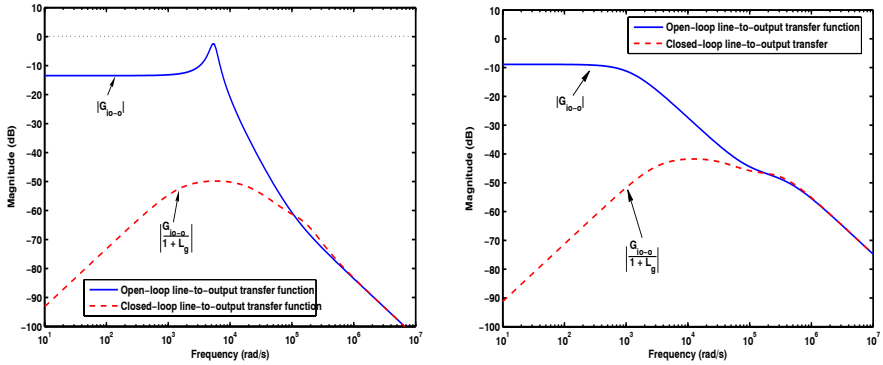
(a) CCM. (b) DCM.

Figure 3.15: The nominal sensitivity function $\left|S^T_{G_{co}}\right|$ versus the weighting function

The closed-loop frequency responses to disturbances, $\mathbf{T_{D1}}$ and $\mathbf{T_{D2}}$ will now be analyzed. As evidenced by Fig. 3.15, the control loop adequately meets the specified disturbance attenuation tolerance despite the obtained $\left|S^T_{G_{co}}(j\omega)\right|$ does not follow exactly the weighting function.

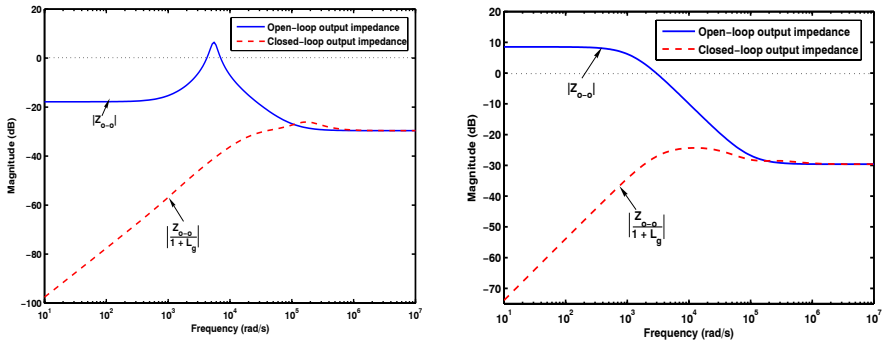
In Figs. 3.16 and 3.17, the voltage-disturbance attenuation and output impedance of the closed-loop systems are shown, together with their open-loop frequency responses. It can be seen that the QFT-controller provides a good disturbance rejection performance, and the disturbance rejection constraints in (3.41) are adequately fulfilled.

To be consistent, the voltage-mode controlled buck converter shown in Fig. 3.5 has been examined by simulation using Matlab™/Simulink SimPowerSystems Toolbox [45]. Figs. 3.18−3.19, show the corresponding simulated time responses of the converter for different perturbations. Fig. 3.18 shows zero steady-state error in the output-voltage response after introducing step-changes in output power 10% $\sim$ 90% at 0.02 s and at 0.05 s. A step



(a) CCM. (b) DCM.

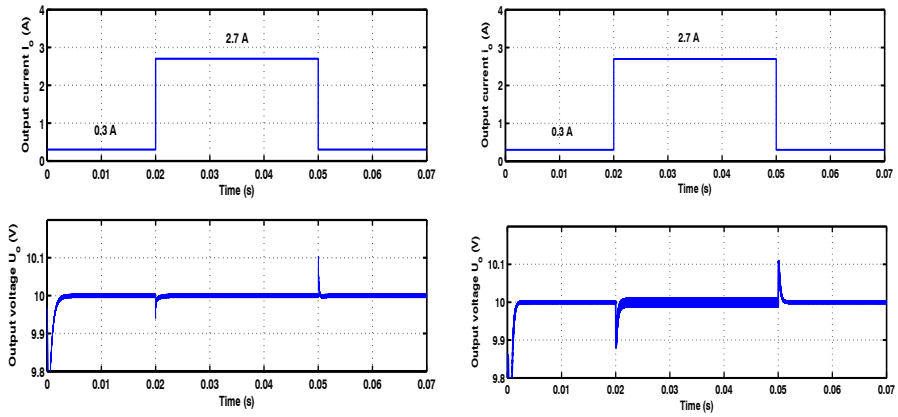
Figure 3.16: The input-output voltage-disturbance attenuation



(a) CCM. (b) DCM.

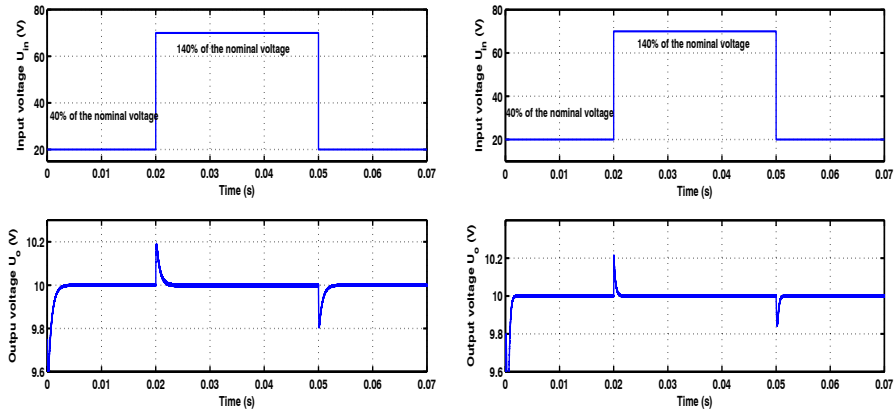
Figure 3.17: The output impedance

perturbation of 2.4 A is introduced at 0.02 s, and a negative step of -2.4 A at 0.05 s over 10% of an average load current 3 A. Similarly, output voltage u_o response for step-changes in input voltage from 20 V to 70 V is illustrated in Fig. 3.19. In this case, a step perturbation of 50 V is introduced at 0.02 s, and a negative step of -50 V at 0.05 s over 40% of an averaged nominal input voltage of 50 V.



(a) CCM. (b) DCM.

Figure 3.18: The output voltage response u_o for load perturbations



(a) CCM. (b) DCM.

Figure 3.19: The output voltage behavior u_o for input voltage perturbations.

3.2.2 Peak-Current-Mode-Controlled Converter

A similar QFT controller design procedure will be now implemented to synthesize a controller for a peak-current-mode-controlled buck converter operating in CCM and DCM. A typical low-power peak-current-mode controlled buck converter is shown in Fig. 3.20. Table 3.1 defines the converter model parameters and summarizes the nominal values of all model parameters and their variations used in controller design. The current-sensing resistor $R_s = 0.15\ \Omega$.

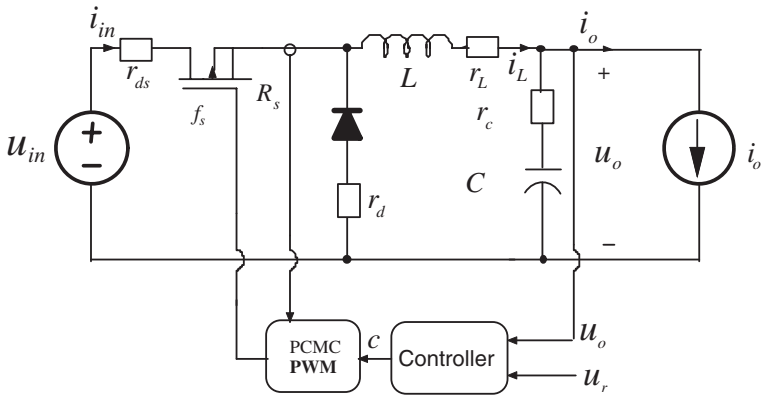


Figure 3.20: Peak-current-mode-controlled-buck converter.

The control-to-output $G^*_{co}(s)$, output impedance $Z^*_{o-o}(s)$ and line-to-output (audio susceptibility) $G^*_{io-o}(s)$ are of interest, and these transfer functions are given as follows: When the converter is operating in CCM,

$$G^*_{co} = \frac{\frac{F_m(U_{in}+U_D+(r_d-r_{rds})I_o)(1+sr_cC)}{LC}}{s^2 + s\cdot\frac{r_L+r_C+Dr_{ds}+(1-D)r_d+F_m(U_{in}+U_D)}{L} + \frac{1}{LC}} \tag{3.47}$$

$$Z^*_{o-o} = -\frac{\frac{(r_L+Dr_{rds}+(1-D)r_{rd}+F_m(U_{in}+U_D)+sL)(1+sr_cC)}{LC}}{s^2 + s\cdot\frac{r_L+r_C+Dr_{ds}+(1-D)r_d+F_m(U_{in}+U_D)}{L} + \frac{1}{LC}} \tag{3.48}$$

$$G^*_{io-o} = \frac{\frac{(D-F_mf_g(U_{in}+U_D))(1+sr_cC)}{LC}}{s^2 + s\cdot\frac{r_L+r_C+Dr_{ds}+(1-D)r_d+F_m(U_{in}+U_D)}{L} + \frac{1}{LC}} \tag{3.49}$$

where the duty-cycle gain F_m, the feedforward gain f_g and the compensation ramp M_c are as follows

$$F_m = \frac{2L}{T_s\left(2LM_c + (U_{in}+U_D)\left(1-2D\right)\right)} \tag{3.50}$$

$$f_g = \frac{D(1-D)T_s}{2L} \tag{3.51}$$

$$M_c = \frac{\left(U_o + U_D + (r_L + (1-D)r_d + Dr_{ds})\, I_o\right)}{2L} \tag{3.52}$$

When the converter is operating in DCM, the corresponding transfer functions become

$$G_{co}^{*} = \frac{\frac{2F_m U_{in}(1+sr_cC)}{LC}}{s^2 + s\cdot\frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{2F_m U_{in}}{L} + \frac{1}{LC}(\frac{1}{1-M}\sqrt{\frac{K}{1-M}} + 2F_m U_{in} f_v)} \tag{3.53}$$

$$Z_{o-o}^{*} = \frac{-\frac{1}{C}(s + \frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{2F_m U_{in}}{L})(1+sr_cC)}{s^2 + s\cdot\frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{2F_m U_{in}}{L} + \frac{1}{LC}(\frac{1}{1-M}\sqrt{\frac{K}{1-M}} + 2F_m U_{in} f_v)} \tag{3.54}$$

$$G_{io-o}^{*} = \frac{\frac{1}{LC}(\frac{M(2-M)}{1-M}\sqrt{\frac{K}{1-M}} - 2F_m U_{in} f_g)}{s^2 + s\cdot\frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{2F_m U_{in}}{L} + \frac{1}{LC}(\frac{1}{1-M}\sqrt{\frac{K}{1-M}} + 2F_m U_{in} f_v)} \tag{3.55}$$

Template Generation

The plant templates are plotted on the Nichols chart in Fig. 3.21 at the useful desired frequency $\omega = \{0.08,\ 0.4,\ 1,\ 3,\ 10,\ 40,\ 300$ krad/s$\}$ for the CCM, and $\omega = \{0.08,\ 0.3,\ 1,\ 3,\ 10,\ 35,\ 100,\ 300$ krad/s$\}$ for the DCM, by computing $G_{co}(j\omega)$ over the set of plants.

Closed-Loop Performance Specifications

All performance specifications involved in the QFT controller design for peak-current-mode-controlled buck converter operating in CCM and DCM are summarized in Table 3.3.

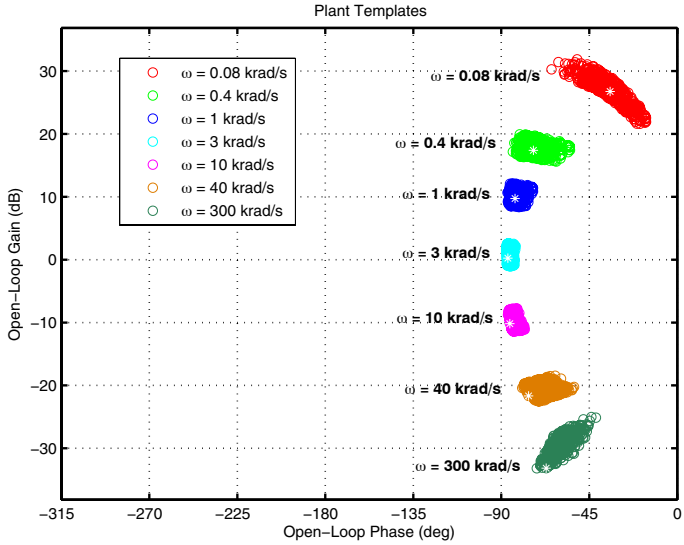
Table 3.3: Robust Performance Specifications

Performance specifications		CCM	DCM
Robust stability	γ	1.05	1.08
Upper bound	$T_U(s)$	$\frac{3.1\times10^4(s+1.5\times10^5)}{(s^2+10.66\times10^4 s+4.66\times10^9)}$	$\frac{9.11\times10^3(s+0.2\times10^5)}{(s^2+1.75\times10^4 s+1.82\times10^8)}$
Lower bound	$T_L(s)$	$\frac{2.56\times10^{19}}{(s+11\times10^4)(s+6.83\times10^4)^2(s+5\times10^4)}$	$\frac{7.9\times10^{15}}{(s+0.65\times10^4)(s+0.8\times10^4)^2(s+1.9\times10^4)}$
Weighting function	$W_s(s)$	$\frac{0.625(s^2+11.38\times10^3 s+3.24\times10^9)}{(s^2+1.684\times10^4 s+7.088\times10^7)}$	$\frac{0.77(s^2+1.78\times10^4 s+6.91\times10^7)}{(s^2+120.8s+3.65\times10^2)}$

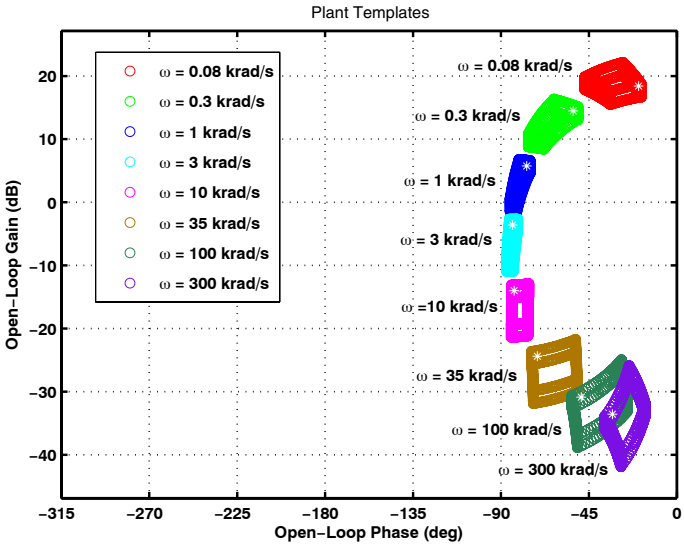
The union of the performance QFT bounds, $B(\omega)$, for each inequality (3.5), (3.38) are then computed based on the performance specifications and the plant templates in the CCM and DCM, as depicted in Fig. 3.22(a) and Fig. 3.22(b), respectively.

QFT Loop-shaping controller

Fig. 3.23(a) shows that the frequency response of the nominal open-loop transfer function $L_{g_{nom}}(s)$ is located below the appropriate tracking performance bounds at each trial frequency. Thus an appropriate control gain should be introduced to push the open-loop frequency response upwards. Moreover, a dynamic compensator is required to change the shape of the open-loop frequency response.

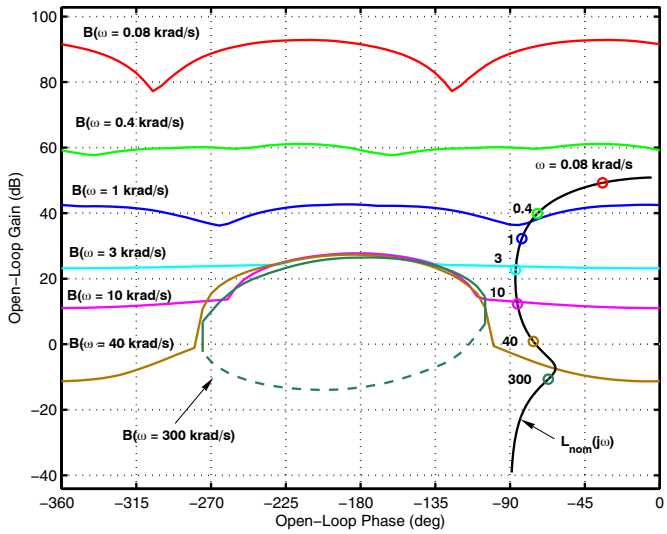


(a) CCM.

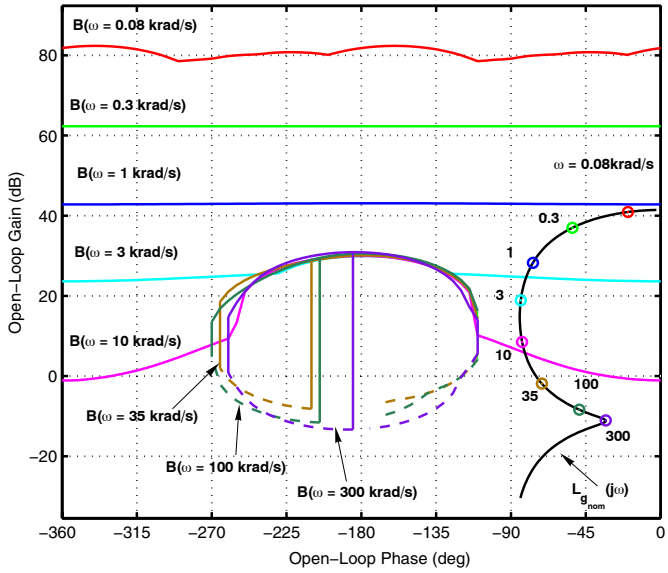


(b) DCM.

Figure 3.21: Plant templates



(a) CCM.



(b) DCM.

Figure 3.22: Open-loop frequency response and QFT bounds $B(\omega)$

Analysis then shows that a pole at the origin in addition to pole-zero pair should be added. In this way, once the loop is adjusted, it is simple to obtain the transfer function of the controller (3.56)

$$G_c(s) = \frac{4515\left(s/3.152\times10^3+1\right)}{s\left(s/1.108\times10^5+1\right)}$$

$$= \frac{4515\left(35.15s+1.108\times10^5\right)}{s\left(s+1.108\times10^5\right)} \tag{3.56}$$

From Fig. 3.22(b), it is obviously seen that the open-loop frequency response violates the tracking bounds. Thus an appropriate control gain should be introduced to push the open-loop frequency response upwards. Analysis then shows that a pole at the origin in addition to two pole-zero pairs should be added. The pole at the origin provides a very high gain at low frequencies as an integral control and the pole-zero pairs result in a reduced phase shift between the frequency of the two zeros and the frequency of two poles as a lead controller.

$$G_c(s) = \frac{6145\left(s/2496+1\right)\left(s/1.115\times10^6+1\right)}{s\left(s/2.033\times10^5+1\right)\left(s/7.93\times10^4+1\right)}$$

$$= \frac{5928\left(5.792s+14.45\times10^5\right)\left(s+1.115\times10^6\right)}{s\left(s+2.033\times10^5\right)\left(s+7.93\times10^4\right)} \tag{3.57}$$

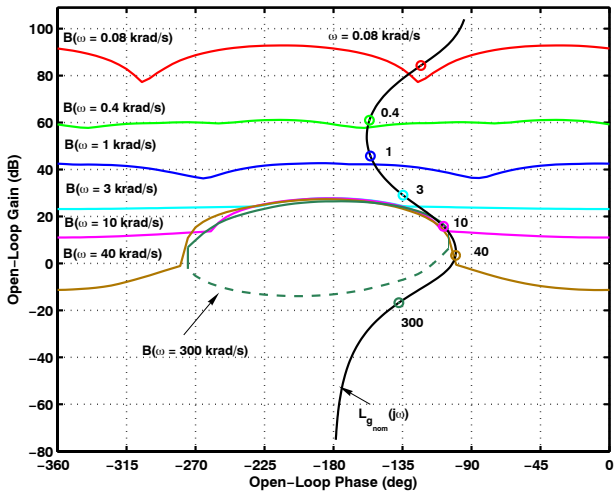
The resulting open-loop frequency responses with these controllers are illustrated in Fig. 3.23. It is clearly seen that the open-loop frequency response does not violate the stability and performance requirements. Also the loop gain has a cross-over frequency $fc \approx 10$ kHz and a phase margin of nearly 78° with an infinite gain margin. However the tradeoff between system response and system stability prevails. The obtained controllers are robust, that is, they provide good results for all of the family of plants defined under uncertainty, not only for the nominal plant used in the loop-shaping stage. The stability performance analysis of the closed-loop system in the next subsection also supports this observation, as seen in Fig. 3.28.

To place the closed-loop tracking responses within the required envelope and attenuate high frequency peaking, prefilter F is then designed to achieve the required shape of the closed-loop frequency response. Fig. 3.24 shows the Bode magnitude plot of the closed-loop frequency response without a prefilter, together with the tracking frequency response specifications plotted with dashed lines. Obviously a dynamic prefilter is required to shape the frequency response to be within the desired range. They were designed for the CCM and DCM, respectively as follows

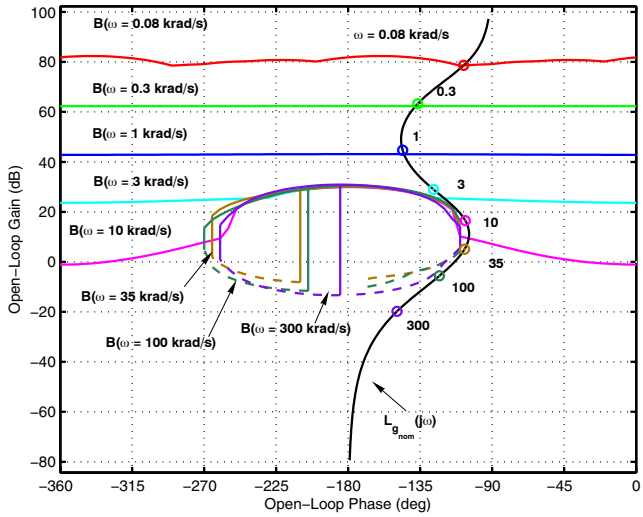
$$F(s) = \frac{1.389\times10^4}{s+1.389\times10^4}, \tag{3.58}$$

$$F(s) = \frac{7.262\times10^3}{s+7.262\times10^3} \tag{3.59}$$

The resulting closed-loop frequency responses with these prefilters are shown in Fig. 3.25.

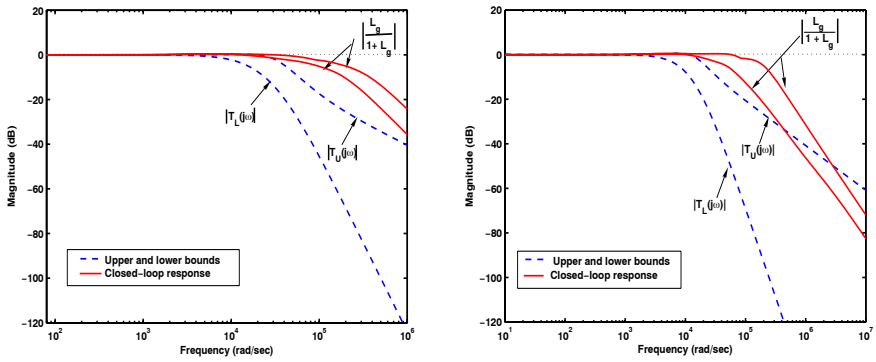


(a) CCM.



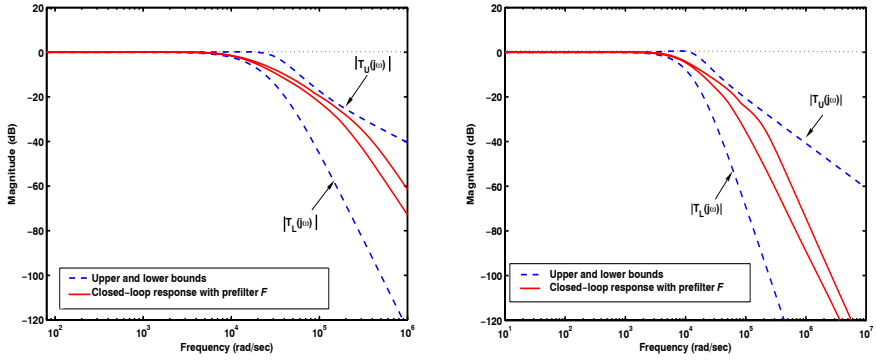
(b) DCM.

Figure 3.23: Open-loop frequency response with controller



(a) CCM. (b) DCM.

Figure 3.24: Closed-loop frequency response without prefilter



(a) CCM. (b) DCM.

Figure 3.25: Closed-loop frequency response with prefilter

Performance Validation and Simulation

In order to verify the design of QFT controllers (3.56)-(3.57), a validation of the obtained results should be made, graphically checking the specifications in the frequency and time domains. Analyzes of the closed-loop system performance in the frequency domain show that the worst closed-loop response magnitude (covering all uncertainty cases) is well below the specified values (γ =1.05 = 0.42 dB, dashed line) (refer to (3.37)), as illustrated in Fig. 3.28(a). The maximum variation of the closed-loop system frequency response is well within the specified range (refer to (3.38)-(3.39b)), as illustrated in Fig. 3.26(a). Thus the closed-loop control system has met all the design specifications in the peak-current-mode control. The time-domain simulation results, illustrated in Fig. 3.26(b) together with the specified tracking bounds plotted with dashed lines, further support the above conclusion.

A similar analysis in DCM reveals that the worst closed-loop response magnitude (covering all uncertainty cases) is well below the specified value (γ = 1.08 = 0.67 dB, dashed line)

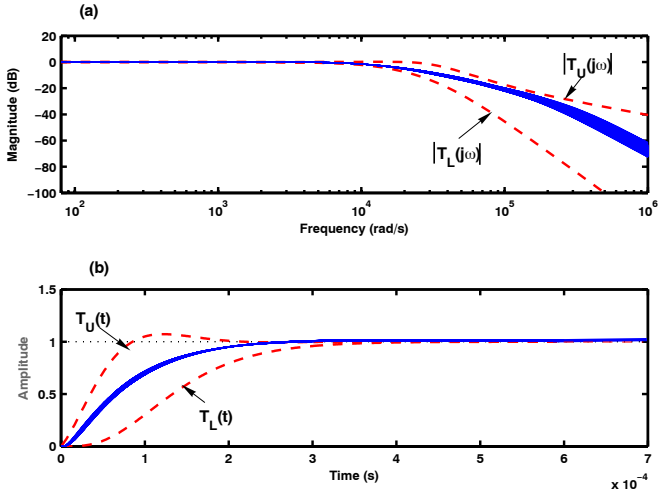


Figure 3.26: Closed-loop responses in CCM: (a) frequency response; (b) unit step response.

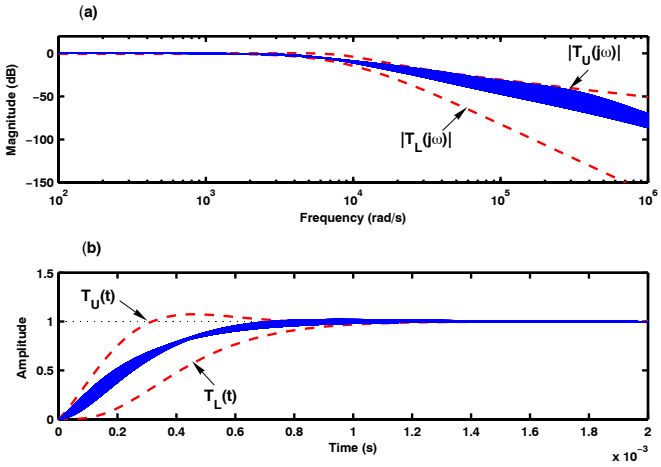
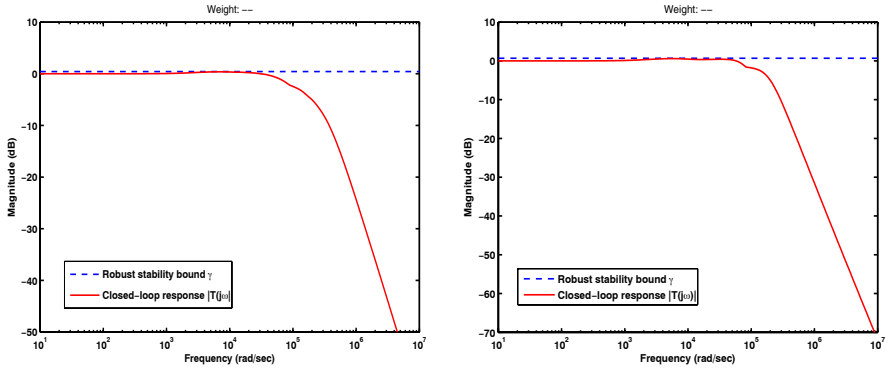


Figure 3.27: Closed-loop responses in DCM: (a) frequency response; (b) unit step response.

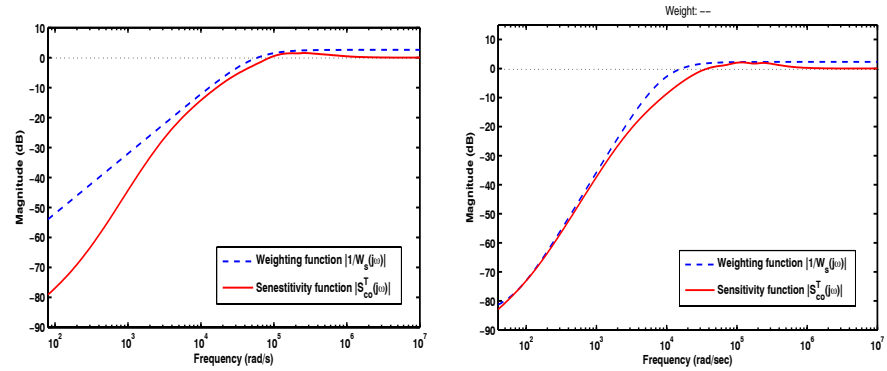
as depicted in Fig. 3.28(b). The maximum variation of the closed-loop system frequency and time responses are well within the specified range as depicted in Fig. 3.27(a) and 3.27(b), respectively.

The closed-loop frequency responses to disturbances, TD_1 and TD_2 is analyzed next. As shown in Fig. 3.29, the control loop adequately meets the specified disturbance attenuation tolerance despite that the obtained $\left|S^T_{G_{co}}(j\omega)\right|$ does not follow exactly the weighting function. In Figs. 3.30 and 3.31, the voltage-disturbance attenuation and output impedance of the closed-loop systems are shown, together with their open-loop frequency responses. It can be



(a) CCM. (b) DCM.

Figure 3.28: Closed-loop robust stability margins



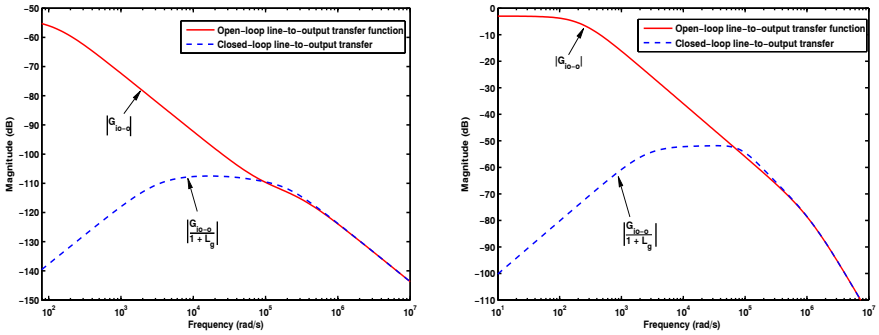
(a) CCM. (b) DCM.

Figure 3.29: The nominal sensitivity function $\left|S^T_{G_{co}}\right|$ versus the weighting function

seen that the QFT-controller provides a good disturbance rejection performance, and the disturbance rejection constraints in (3.41) are adequately fulfilled.

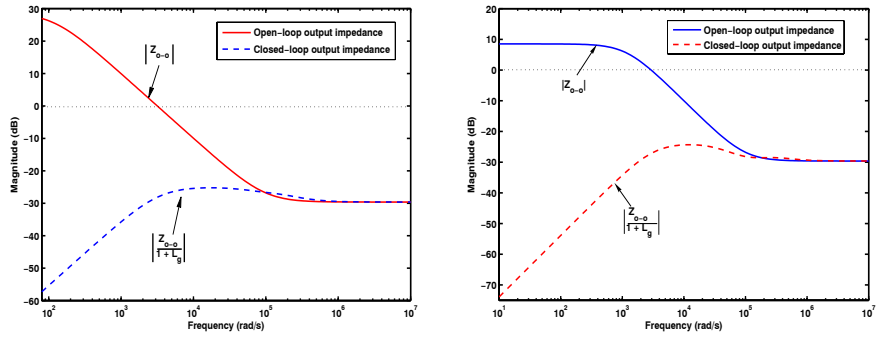
To be coherent, the peak-current-mode-controlled buck converter shown in Fig. 3.20 has been evaluated by simulation. Figs. 3.32-3.33, show the corresponding simulated time responses of the converter for different perturbations for each operating mode. Fig. 3.32 shows zero steady-state error in the output-voltage response after introducing step-changes in output power 10% $\sim$ 90% at 0.02 s and at 0.045 s. A step perturbation of 2.4 A is introduced at 0.02 s, and a negative step of -2.4 A at 0.045 s over 10% of an average load current 3 A.

Similarly, output voltage u_o response for step-changes in input voltage from 20 V to 70 V is illustrated in Fig. 3.33. In this case, a step perturbation of 50 V is introduced at 0.025 s, and a negative step of -50 V at 0.045 s over 40% of an averaged nominal input voltage of 50 V.



(a) CCM. (b) DCM.

Figure 3.30: The input-output voltage-disturbance attenuation



(a) CCM. (b) DCM.

Figure 3.31: The output impedance

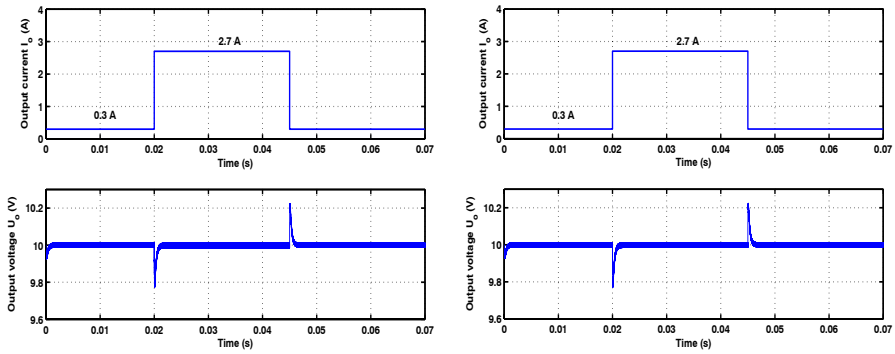
In all cases, the output response exhibits a fast recovery with zero steady-state error and is in good agreement with the frequency responses results.

3.3 QFT-Based Robust Controller Design for Non-minimum Phase Converters

The application of the QFT theory to control non-minimum phase dc-to-dc switching converters is investigated in this section based on the design methodology presented in Section 3.1.5. The problem of designing a QFT controller for boost and buck-boost converters that improves the bandwidth control loop in spite of practical limitations on the achievable closed-loop performance (i.e., right-half-plane zero) and in the presence of other design constraints including closed-loop tracking and robust stability is analyzed.

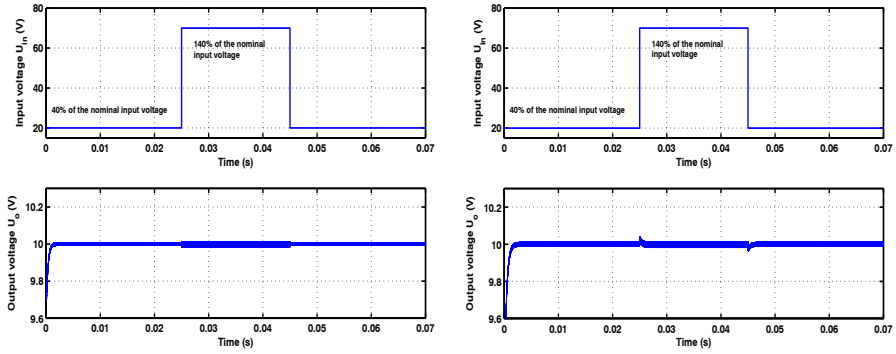
3.3.1 QFT-Based Robust Controller Design for a Boost Converter

The design procedure proposed in Section 3.1.5 will be now implemented to synthesize controllers for voltage and peak-current-mode-controlled boost converter operating in CCM



(a) CCM. (b) DCM.

Figure 3.32: The output voltage response u_o for load perturbations



(a) CCM. (b) DCM.

Figure 3.33: The output voltage behavior u_o for input voltage perturbations.

shown in Fig. 3.34.
The converter control-to-output transfer $G^*_{co}(s)$ in VMC can be presented as follows

$$G^*_{co} = \frac{\left(D'(U_o+U_D)-(D'r_c+\frac{r_L}{D'})I_o-s\frac{LI_o}{D'}\right)(1+sr_C)}{LC} \Big/ \left(s^2 + s\frac{r_L+D'r_C}{L} + \frac{D'^2}{LC}\right} \tag{3.60}$$

An arbitrarily chosen nominal plant $G^*_{co_{nom}}$ within the plant family is given by

$$G^*_{co_{nom}} = \frac{\left(D'_o(U_o+U_{D_o})-(D'_or_{c_o}+\frac{r_{L_o}}{D'_o})I_o-s\frac{L_oI_o}{D'_o}\right)(1+sr_{C_o})}{L_oC_o} \Big/ \left(s^2 + s\frac{r_{L_o}+D'_or_{C_o}}{L_o} + \frac{D'^2_o}{L_oC_o}\right} \tag{3.61}$$

If

$$A(s) = \frac{\left(D'_o(U_o+U_{D_o})-(D'_or_{c_o}+\frac{r_{L_o}}{D'_o})I_o\right)-s\frac{L_oI_o}{D'_o}}{\left(D'_o(U_o+U_{D_o})-(D'_or_{c_o}+\frac{r_{L_o}}{D'_o})I_o\right)+s\frac{L_oI_o}{D'_o}} \tag{3.62}$$

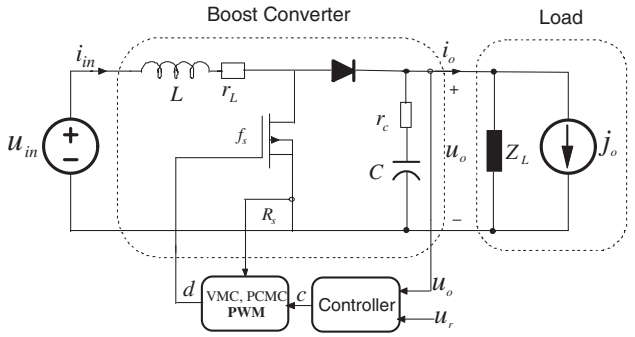


Figure 3.34: Voltage and peak-mode-controlled-boost converter.

Then the new nominal plant is defined as

$$G'_{co_{nom}} = G^*_{co_{nom}}(s)A(s)^{-1} = \frac{\frac{\left(D'_o(U_o+U_{D_o})-(D'_o r_{c_o}+\frac{r_{L_o}}{D'_o})I_o+s\frac{L_o I_o}{D'_o}\right)(1+sr_{C_o})}{L_o C_o}}{s^2+s\frac{r_{L_o}+D'_o r_{C_o}}{L_o}+\frac{D'^2_o}{L_o C_o}} \tag{3.63}$$

Obviously $G'_{co_{nom}}$ is a stable minimum phase plant and the new nominal loop gain $L'_{g_{nom}}(s)$ is defined as

$$L'_{g_{nom}}(s) = G'_{co_{nom}}(s)G_a G_c(s) \tag{3.64}$$

Furthermore we have

$$L^*_g(s) = G^*_{co}(s)G_a G_c(s) = G^*_{co}{}'(s)G_a G_c(s)A(s) \tag{3.65}$$

where

$$G^*_{co}{}'(s) = \frac{\frac{\left(D'(U_o+U_D)-(D'r_c+\frac{r_L}{D'})I_o-s\frac{LI_o}{D'}\right)(1+sr_C)}{LC}}{s^2+s\frac{r_L+D'r_C}{L}+\frac{D'^2}{LC}} \cdot \frac{\left(D'_o(U_o+U_{D_o})-(D'_o r_{c_o}+\frac{r_{L_o}}{D'_o})I_o\right)+s\frac{L_o I_o}{D'_o}}{\left(D'_o(U_o+U_{D_o})-(D'_o r_{c_o}+\frac{r_{L_o}}{D'_o})I_o\right)-s\frac{L_o I_o}{D'_o}} \tag{3.66}$$

and the new loop gain transfer function $L^{*\prime}_g(s)$ is defined as

$$L^{*\prime}_g(s) = G^*_{co}{}'(s)G_a G_c(s) \tag{3.67}$$

Similarly, the converter control-to-output transfer function $G^*_{co}(s)$ in PCMC can be presented as follows

$$G^*_{co} = \frac{\frac{D'F_m(U_o+U_D)\left(1-s\cdot\frac{LI_o}{D'^2(U_o+U_D)}\right)(1+sr_C C)}{LC}}{s^2+s\frac{F_m(U_o+U_D)}{L}-\frac{F_m f_v I_o}{D'C}+\frac{D'^2}{LC}\left(1+\frac{F_m f_v(U_o+U_D)}{D'}+\frac{F_m I_o}{D'^2}\right)} \tag{3.68}$$

However $A(s)$ is chosen accordingly as follows

$$A(s) = \frac{\left(1 - s \cdot \frac{L_o I_o}{{D'_o}^2 (U_o + U_{D_o})}\right)}{\left(1 + s \cdot \frac{L_o I_o}{{D'_o}^2 (U_o + U_{D_o})}\right)} \tag{3.69}$$

Template Generation

Table 3.4 defines the boost converter model parameters and the nominal values of all model parameters and their variations used in controller design. The original and new plant templates for VMC are plotted on the Nichols chart in Fig. 3.35 at the selected frequency $\omega = \{1.9, 3, 5, 9, 20, 60, 300$ krad/s$\}$, by computing $G_{co}(j\omega)$ over the set of plants.

Table 3.4: Nominal model parameters and their ranges

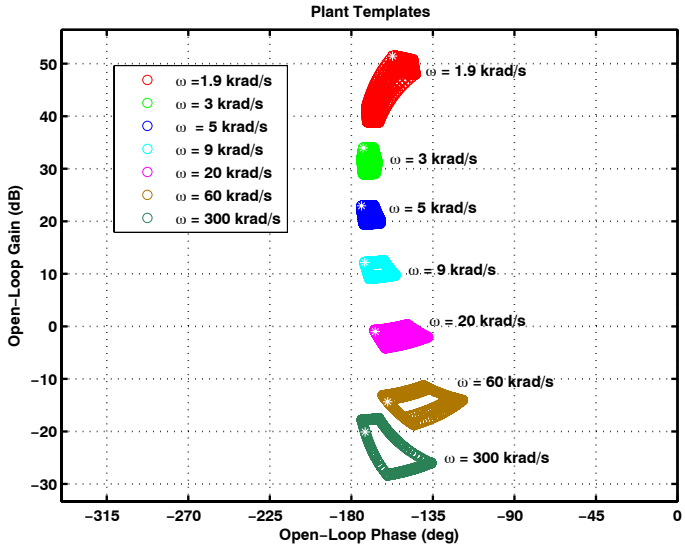
Uncertain parameter	Nominal Value	Variations
U_o	75V	...
U_{in}	50V	20-70V
P_{out}	100W	$10\% \sim 90\%$
L	350μH	$\pm 50\%$
C	500μF	$\pm 20\%$
r_C	50mΩ	$+90\%$
r_L	20mΩ	$+90\%$
U_D	1.5V	$\pm 20\%$
f_s	100kHz	...

Closed-Loop Performance Specifications

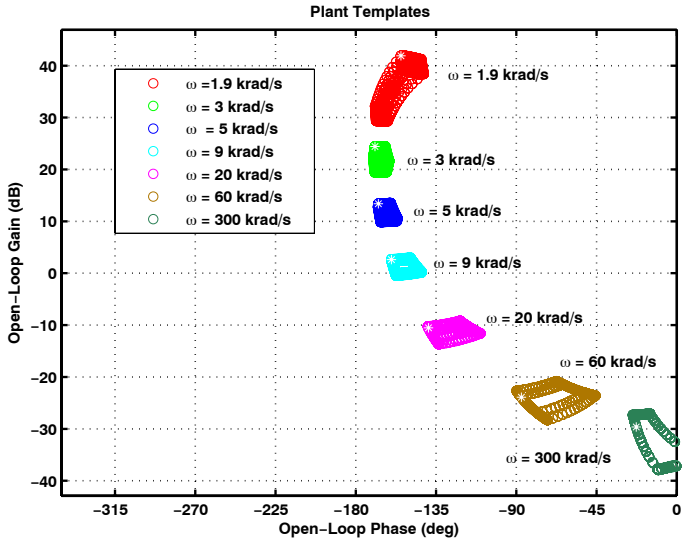
All performance specifications involved in the QFT controller design for a boost converter in VMC and PCMC are summarized in Table 3.5.

Table 3.5: Robust Performance Specifications

Performance specifications		VMC	PCMC
Robust stability	γ	1.18	1.05
Upper bound	$T_U(s)$	$\frac{2.812\times10^3\left(s+2\times10^4\right)}{\left(s^2+8.850\times10^3 s+5.625\times10^7\right)}$	$\frac{504.3\left(s+0.3\times10^4\right)}{\left(s^2+1599s+1.512900\times10^6\right)}$
Lower bound	$T_L(s)$	$\frac{2.448\times10^{16}}{(s+2\times10^4)(s+1.2\times10^4)^2(s+0.85\times10^4)}$	$\frac{1.15\times10^{13}}{(s+1.9\times10^3)(s+1.23\times10^3)^2(s+4\times10^3)}$
Weighting function	$W_s(s)$	$\frac{0.833\left(s^2+9.422\times10^3 s+2.22\times10^7\right)}{\left(s^2+2.58\times10^3 s+1.664\times10^6\right)}$	$\frac{0.8\left(s^2+2.9075\times10^3 s+2.1125\times10^6\right)}{\left(s^2+48.64s+591.5\right)}$



(a) Original templates.



(b) New templates.

Figure 3.35: Plant templates.

The intersection of the performance QFT bounds, $B(\omega)$, for each inequality (3.25)-(3.27) are then computed based on the performance specifications and the plant templates in the VMC and PCMC, as depicted in Fig. 3.36 and Fig. 3.37, respectively.

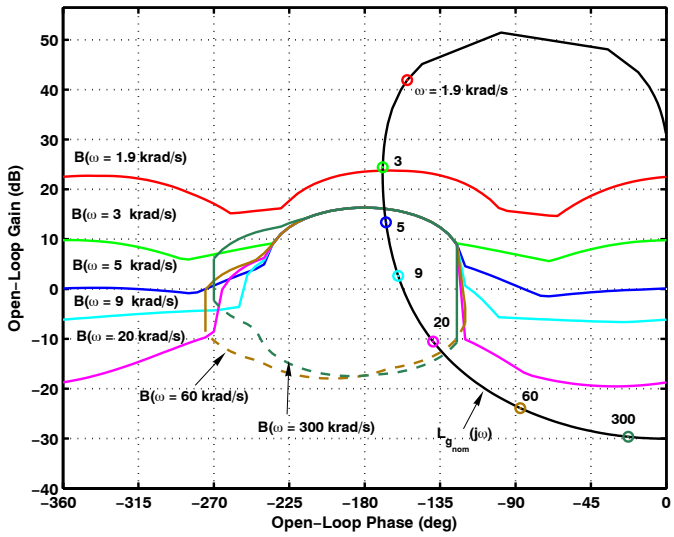


Figure 3.36: Open-loop frequency response and QFT bounds $B(\omega)$, (VMC).

QFT Loop-Shaping Controller

The loop-shaping is performed with the experience of the designer as usual. Fig. 3.36 shows the frequency response of the new nominal open-loop transfer function $L'_{g_{nom}}(s)$ according to (3.64) , which violates the stability bounds. The design objective is to apply dynamic compensation to the nominal open-loop transfer function, so that the performance bounds are satisfied at each frequency. It can be seen also that, the open-loop frequency response is located below the appropriate tracking performance bounds at each frequency. Thus an appropriate control gain should be introduced to push the open-loop frequency response upwards. Moreover, a dynamic compensator is required to change the shape of the open-loop frequency response. Analysis then shows that a pole at the origin in addition to two zeros and three poles should be added. In this way, once the loop is adjusted, it is simple to obtain the transfer function of the controller (3.70)

$$G_c(s) = \frac{100\,(\mathrm{s}/1938+1)\,(\mathrm{s}/950.4+1)}{s\,(s/3.36\times10^5+1)\,(s/4.951\times10^4+1)\,(s/1.159\times10^5+1)} \tag{3.70}$$

The resulting open-loop frequency responses with this controller shown in Fig. 3.38(a).

It is clearly seen that the open-loop frequency response does not violate the stability and performance requirements. The loop gain for the original plant is shown in Fig. 3.39(a). The stability properties have been improved where the loop gain has a cross-over frequency $f_c \approx 1.1$ kHz, a phase margin of nearly 60° and a gain margin of 21 dB. However the tradeoff between system response and system stability prevails.

From Fig. 3.37, it is obviously seen that the open-loop frequency response violates the tracking bounds. Thus an appropriate control gain should be introduced to push the open-loop frequency response upwards. Analysis then shows that a pole at the origin in addition to three poles and zero should be added.

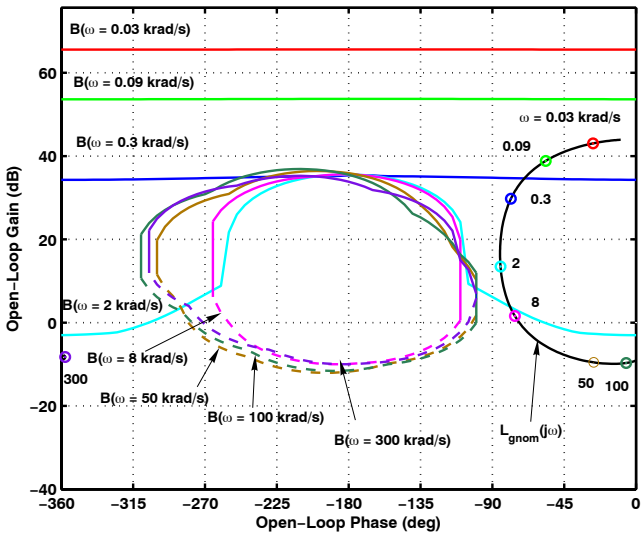


Figure 3.37: Open-loop frequency response and QFT bounds $B(\omega)$, (PCMC).

$$G_c(s) = \frac{502.4\,(s/325.4+1)}{s\,(s/7.345\times10^4+1)\,(s/3.558\times10^4+1)\,(s/5.229\times10^5+1)} \tag{3.71}$$

The resulting open-loop frequency response with this controller is shown in Fig. 3.38(b). It's seen that the open-loop frequency response does not violate the stability and performance requirements. Also there is a clear improvement in the stability properties with a cross-over frequency $f_c \approx 2.1$ kHz, a phase margin of nearly 61° and a gain margin of 12.5 dB as shown in Fig. 3.39(b).

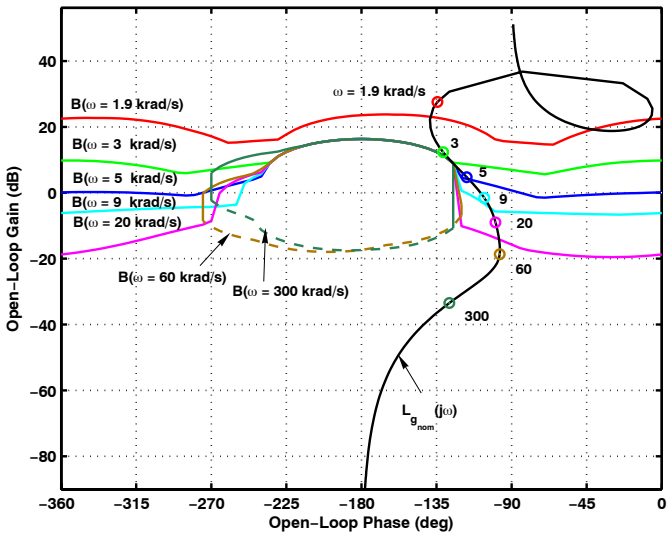
The controllers are robust, that is, they provide good results for all plants defined under uncertainty, not only for the nominal plant used in the loop-shaping stage. The stability performance analysis of the closed-loop system in the next subsection also supports this observation, as it will be seen in Fig. 3.42.

To place the closed-loop tracking responses within the required envelope and attenuate high frequency peaking, prefilter F is then designed to achieve the required shape of the closed-loop frequency response. Fig. 3.40 shows the Bode magnitude plot of the closed-loop frequency response without a prefilter, together with the tracking frequency response specifications plotted with dashed lines. Obviously a dynamic prefilter is required to shape the frequency response to be within the desired range. They were designed for the VMC and PCMC, respectively as follows

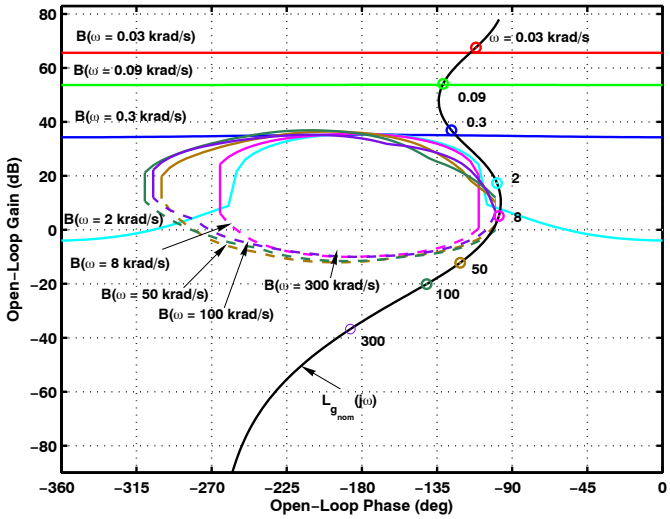
$$F(s) = \frac{5.319\times10^3}{s+5.319\times10^3} \tag{3.72}$$

$$F(s) = \frac{1}{(s/2534+1)\,(s/1039+1)} \tag{3.73}$$

The resulting closed-loop frequency responses with these prefilters are shown in Fig. 3.41.



(a) VMC.

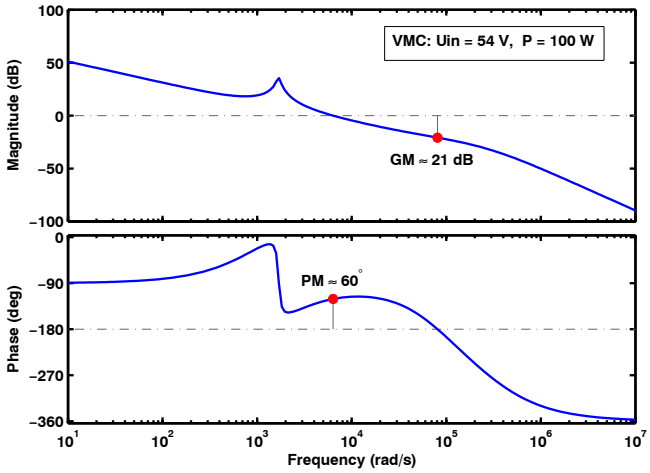


(b) PCMC.

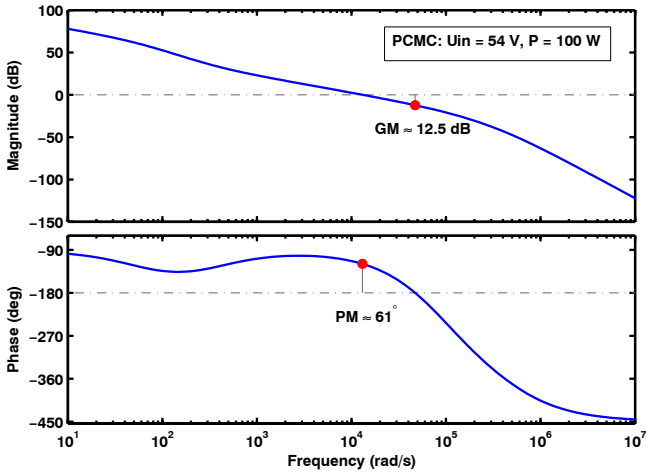
Figure 3.38: Open-loop frequency response with controller

Performance Validation and Simulation

In order to verify the design of QFT controllers (3.70)-(3.71), a validation of the obtained results should be made, graphically checking the specifications in the frequency and time domains. Analyzes of the closed-loop system performance in the frequency domain show



(a) VMC.

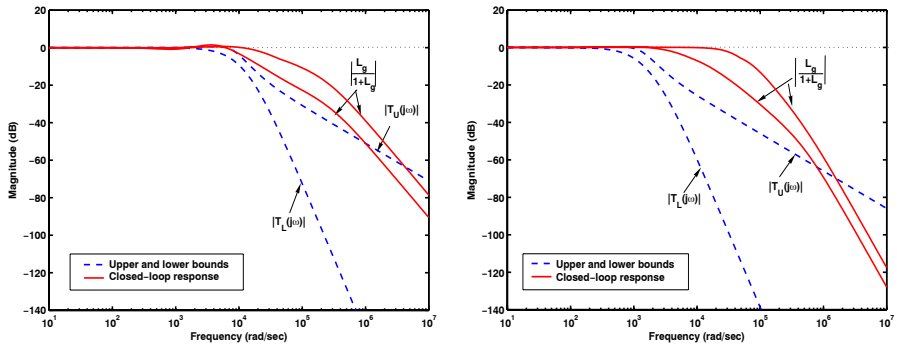


(b) PCMC.

Figure 3.39: Original loop-gain

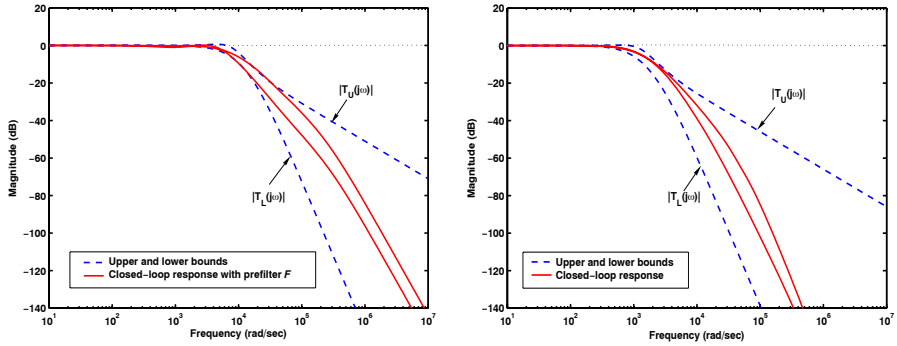
that the worst closed-loop response magnitude (covering all uncertainty cases) is well below the specified values (γ =1.18 = 1.4376 dB, dashed line) (refer to (3.25)), as illustrated in Fig. 3.42(a).

A similar analysis in PCMC reveals that the worst closed-loop response magnitude (covering all uncertainty cases) is well below the specified value ($\gamma = 1.05 = 0.4238$ dB, dashed line) as depicted in Fig. 3.42(b).



(a) VMC. (b) PCMC.

Figure 3.40: Closed-loop frequency response without prefilter

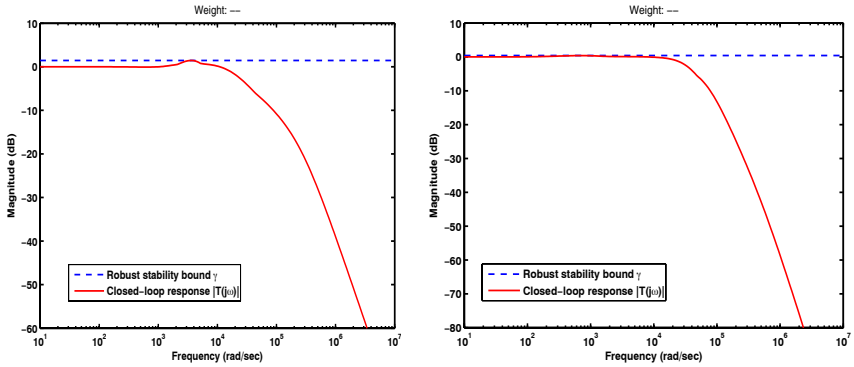


(a) VMC. (b) PCMC.

Figure 3.41: Closed-loop frequency response with prefilter

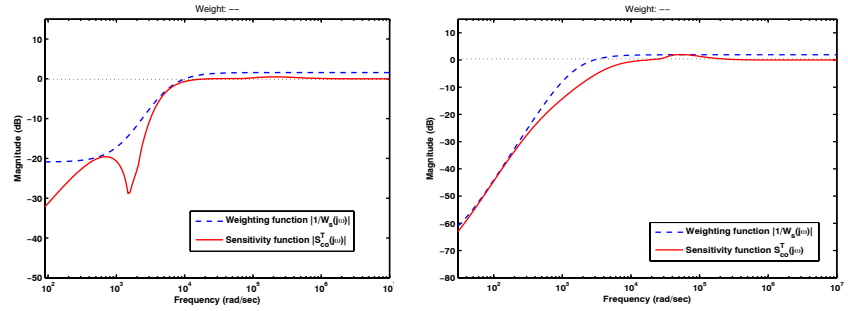
The closed-loop frequency responses to disturbances, TD_1 and TD_2 will now be analyzed. As shown in Fig. 3.43, the control loop adequately meets the specified disturbance attenuation tolerance despite that the obtained $\left|S^T_{G_{co}}(j\omega)\right|$ does not follow exactly the weighting function. In Figs. 3.44 and 3.45, the voltage-disturbance attenuation and output impedance of the closed-loop systems are shown, together with their open-loop frequency responses. It can be seen that the QFT-controller provides a good disturbance rejection performance, and the disturbance rejection constraints in (3.25) are adequately fulfilled.

To be consistent, the boost converter shown in Fig. 3.34 has been examined by simulation. Figs. 3.46−3.47, show the corresponding simulated time responses of the converter for different perturbations. Fig. 3.46 shows zero steady-state error in the output-voltage response after introducing step-changes in output power 10% $\sim$ 90% at 0.035 s and at 0.07 s. A step perturbation of 1.2 A is introduced at 0.035 s, and a negative step of -1.2 A at 0.07 s over 10% of an average load current 1.33 A. Similarly, output voltage u_o response for step-changes in input voltage from 20 V to 70 V is illustrated in Fig. 3.47. In this case, a step perturbation of 50 V is introduced at 0.04 s, and a negative step of -50 V at 0.075 s over 40% of an averaged nominal input voltage of 50 V.



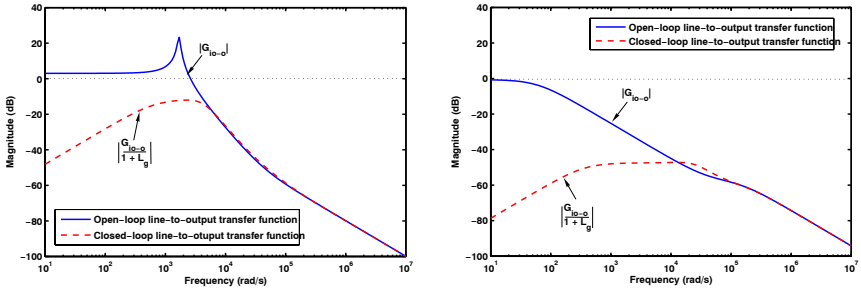
(a) VMC. (b) PCMC.

Figure 3.42: Closed-loop robust stability margins



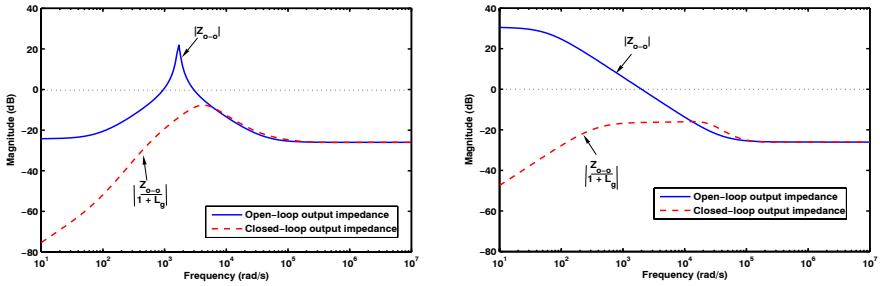
(a) VMC. (b) PCMC.

Figure 3.43: The nominal sensitivity function $\left|S^T_{G_{co}}\right|$ versus the weighting function



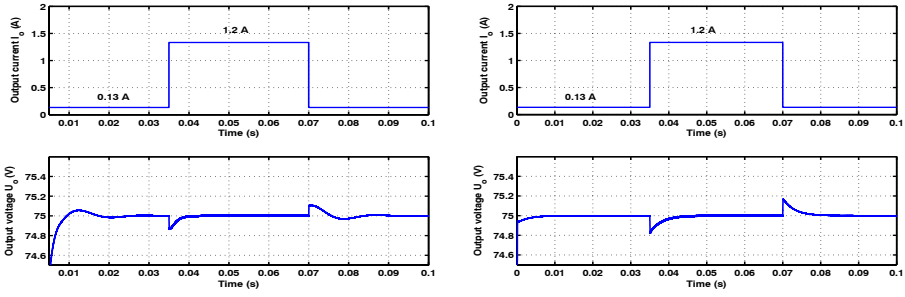
(a) VMC. (b) PCMC.

Figure 3.44: The input-output voltage-disturbance attenuation



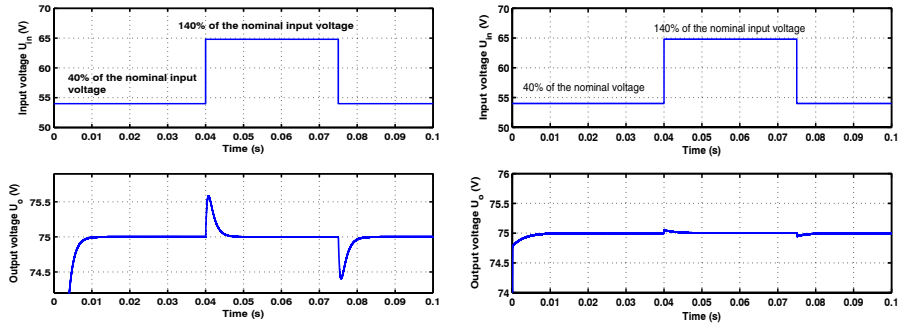
(a) VMC. (b) PCMC.

Figure 3.45: The output impedance



(a) VMC. (b) PCMC.

Figure 3.46: The output voltage response u_o for load perturbations



(a) VMC. (b) PCMC.

Figure 3.47: The output voltage behavior u_o for input voltage perturbations

3.3.2 QFT-Based Robust Controller Design for a Buck-Boost Converter

A similar design analysis can be performed to voltage-mode-controlled buck-boost converter operating in CCM shown in Fig. 3.48.

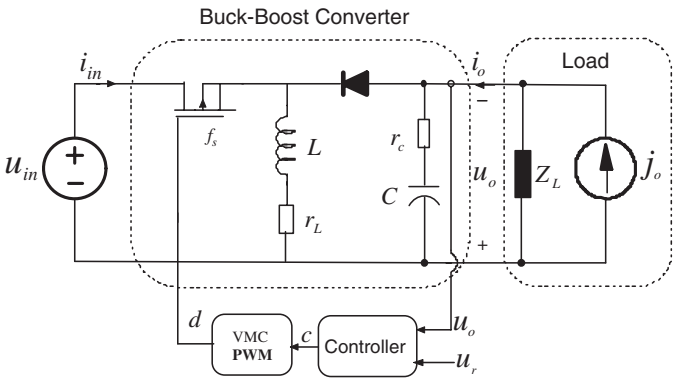


Figure 3.48: Buck-boost converter.

The converter control-to-output transfer function $G^*_{co}(s)$ in VMC can be presented as follows

$$G^*_{co} = \frac{\frac{(D'(U_{in}+U_o+U_D)-(D'r_C+\frac{r_L}{D'})I_o-s\frac{LI_o}{D'})(1+sr_CC)}{LC}}{s^2+s\frac{r_CD'+r_L}{L}+\frac{D'^2}{LC}} \tag{3.74}$$

The nominal plant $G^*_{co_{nom}}$ is chosen within the plant family as follows

$$G^*_{co_{nom}} = \frac{\frac{\left(D'_o(U_o+U_{in_o}+U_{D_o})-(D'_or_{c_o}+\frac{r_{L_o}}{D'_o})I_o-s\frac{L_oI_o}{D'_o}\right)(1+sr_{C_o})}{L_oC_o}}{s^2+s\frac{r_{L_o}+D'_or_{C_o}}{L_o}+\frac{D'^2_o}{L_oC_o}} \tag{3.75}$$

However $A(s)$ is chosen accordingly as follows

$$A(s) = \frac{(D'_o(U_{in_o}+U_o+U_{D_o})-(D'_or_{C_o}+\frac{r_{L_o}}{D'_o})I_o-s\frac{LI_o}{D'_o})}{(D'_o(U_{in_o}+U_o+U_{D_o})-(D'_or_{C_o}+\frac{r_{L_o}}{D'_o})I_o+s\frac{LI_o}{D'_o})} \tag{3.76}$$

Then the new nominal plant is defined as

$$G'_{co_{nom}} = G^*_{co_{nom}}(s)A(s)^{-1} = \frac{\frac{\left(D'_o(U_{in_o}+U_o+U_{D_o})-(D'_or_{c_o}+\frac{r_{L_o}}{D'_o})I_o+s\frac{L_oI_o}{D'_o}\right)(1+sr_{C_o})}{L_oC_o}}{s^2+s\frac{r_{L_o}+D'_or_{C_o}}{L_o}+\frac{D'^2_o}{L_oC_o}} \tag{3.77}$$

The new nominal loop gain $L'_{g_{nom}}(s)$ is defined as

$$L'_{g_{nom}}(s) = G'_{co_{nom}}(s)G_aG_c(s) \tag{3.78}$$

Furthermore the new loop gain transfer function $L^{*\prime}_g(s)$ can be obtained as follows

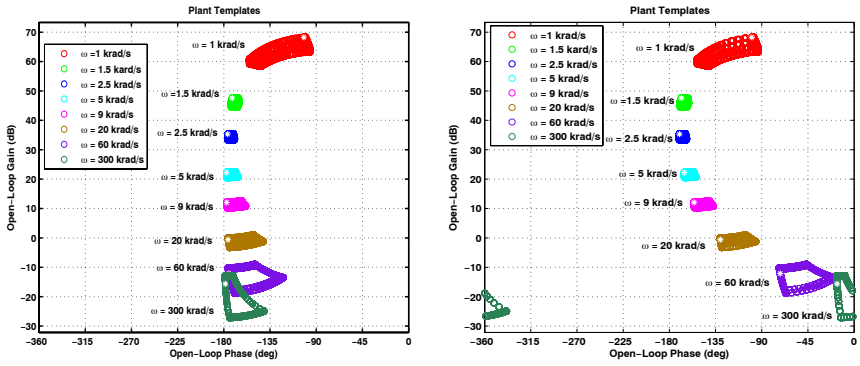
$$L_g^{*\prime}(s) = G_{co}^{*\prime}(s) G_a G_c(s) \tag{3.79}$$

where

$$G_{co}^{*\prime}(s) = G_{co}^{*}(s) A(s)^{-1} \tag{3.80}$$

Template Generation

Table 3.4 defines the buck-boost converter model parameters and summarizes the nominal values of all model parameters and their variations used in controller design. The new and old plant templates are plotted on the Nichols chart in Fig. 3.49 at the desired frequency ω = {1, 1.5, 2.5, 5, 9, 20, 60, 300 krad/s}, by computing $G_{co}(j\omega)$ as G_{co} varies over the set of plants.



(a) Before shifting. (b) After shifting.

Figure 3.49: Plant templates.

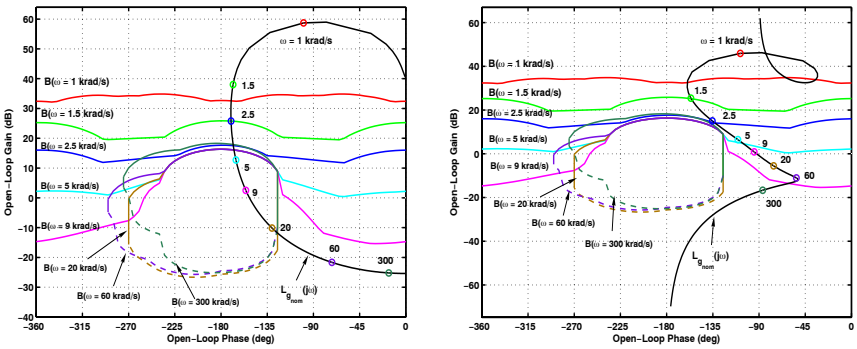
Closed-Loop Performance Specifications

All performance specifications involved in the QFT controller design for a voltage-mode-controlled-buck-boost converter operating in CMC and are summarized in Table 3.6.

Table 3.6: Robust Performance Specifications

Performance specifications		VMC
Robust stability	γ	1.18
Upper bound	$T_U(s)$	$\frac{4.114\times10^3(s+3.5\times10^4)}{(s^2+1.416\times10^4 s+1.44\times10^8)}$
Lower bound	$T_L(s)$	$\frac{3.042\times10^{16}}{(s+2\times10^4)(s+1.3\times10^4)^2(s+9\times10^3)}$
Weighting function	$W_s(s)$	$\frac{0.769(s^2+1.14\times10^4 s+3.25\times10^7)}{(s^2+1.342\times10^3 s+4.5\times10^5)}$

The intersection of the performance QFT bounds, $B(\omega)$, for each inequality (3.25)-(3.27) are then computed based on the performance specifications and the plant templates, as depicted in Fig. 3.50(a).



(a) Without controller. (b) With controller.

Figure 3.50: Open-loop frequency response and QFT bounds $B(\omega)$.

QFT Loop-shaping controller

Finally, the loop-shaping is performed. Fig. 3.50(a) shows the frequency response of the new nominal open-loop transfer function $L'_{g_{nom}}(s)$ according to (3.78), which violates the stability bounds. The design objective is to apply dynamic compensation to the nominal open-loop transfer function, so that the performance bounds are satisfied at each frequency. It can be seen also that, the open-loop frequency response is located below the appropriate tracking performance bounds at each frequency. Thus an appropriate control gain should be introduced to push the open-loop frequency response upwards. Moreover, a dynamic compensator is required to change the shape of the open-loop frequency response. Analysis then shows that a pole at the origin in addition to two zeros and three poles should be added. In this way, once the loop is adjusted, it is simple to obtain the transfer function of the controller (3.81)

$$G_c(s) = \frac{120\,(\mathrm{s}/1734 + 1)\,(\mathrm{s}/756.4 + 1)}{s\,(s/3.760 \times 10^5 + 1)\,(s/4.932 \times 10^4 + 1)\,(s/3.559 \times 10^5 + 1)} \tag{3.81}$$

The resulting open-loop frequency responses with this controller shown in Fig. 3.50(b). It can be seen that the open-loop frequency response does not violate the stability and performance requirements.

The loop gain for the original plant is shown in Fig. 3.51. As can be seen there is a clear improvement in the stability properties with a cross-over frequency $f_c \approx 1.61$ kHz, a phase margin of nearly 64° and a gain margin of 13 dB.

To place the closed-loop tracking responses within the required envelope and attenuate high frequency peaking, prefilter F is then designed to achieve the required shape of the closed-loop frequency response. Fig. 3.52(a) shows the Bode magnitude plot of the closed-loop frequency response without a prefilter, together with the tracking frequency response specifications plotted with dashed lines. Obviously a dynamic prefilter is required to shape the frequency response to be within the desired range. It was designed as follows

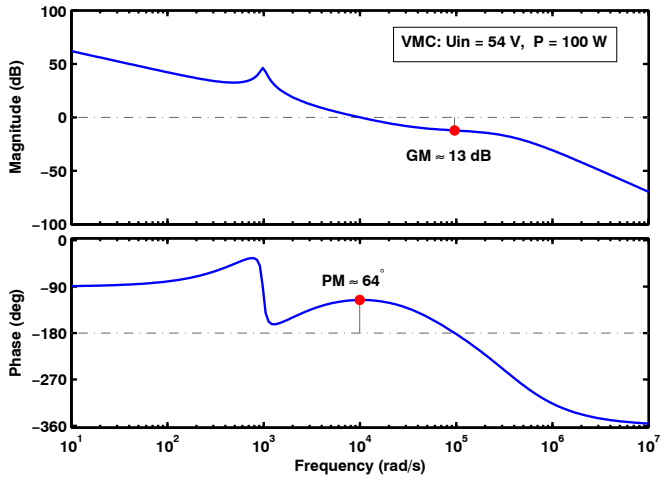
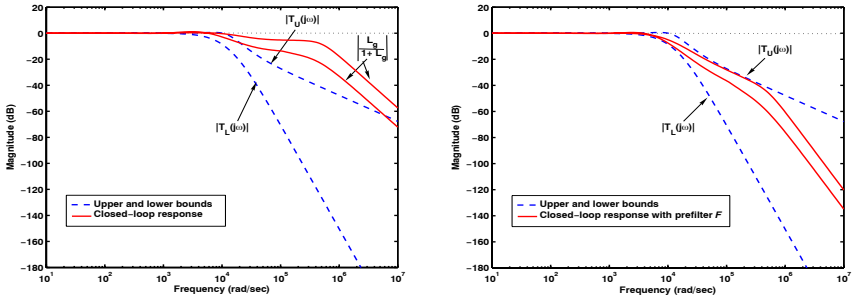


Figure 3.51: The original loop-gain



(a) Without prefilter.

(b) With prefilter.

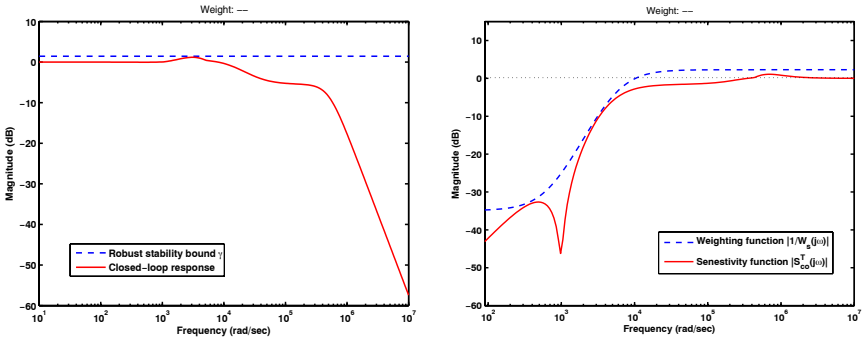
Figure 3.52: Closed-loop frequency response

$$F(s) = \frac{7.261 \times 10^3}{s + 7.261 \times 10^3} \tag{3.82}$$

The resulting closed-loop frequency responses with this prefilter is shown in Fig. 3.52(b).

In order to verify the design of QFT controller (3.81), a validation of the obtained results should be made, graphically checking the specifications in the frequency and time domains. Analyzes of the closed-loop system performance in the frequency domain show that the worst closed-loop response magnitude (covering all uncertainty cases) is well below the specified values ($\gamma = 1.18 = 1.4376$ dB, dashed line) (refer to (3.25)), as illustrated in Fig. 3.53(a).

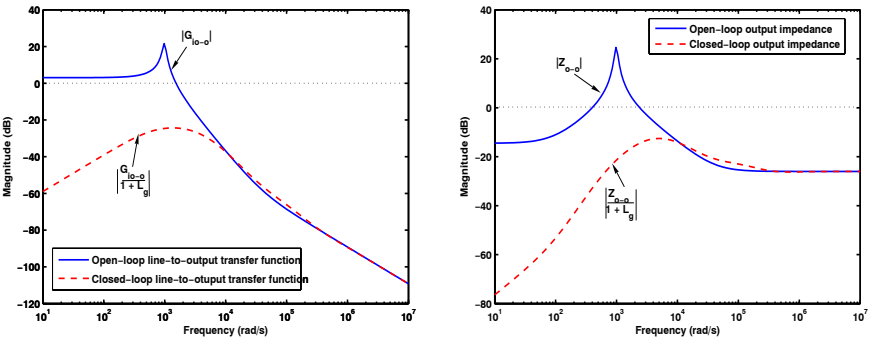
The closed-loop frequency responses to disturbances, TD_1 and TD_2 will now be analyzed. As shown in Fig. 3.53(b), the control loop adequately meets the specified disturbance atten-



(a) Closed-loop robust stability margins. (b) The nominal sensitivity function $\left|S^T_{G_{co}}\right|$ versus the weighting function.

Figure 3.53: Closed-loop frequency response

uation tolerance despite that the obtained $\left|S^T_{G_{co}}(j\omega)\right|$ does not follow exactly the weighting function. In Figs. 3.54(a) and 3.54(b), the voltage-disturbance attenuation and output impedance of the closed-loop systems are shown, together with their open-loop frequency responses. It can be seen that the QFT-controller provides a good disturbance rejection performance, and the disturbance rejection constraints in (3.25) are adequately fulfilled.



(a) The input-output voltage-disturbance attenuation. (b) The output impedance.

Figure 3.54: Input and output disturbances

The buck-boost converter shown in Fig. 3.48 has been examined by simulation. Figs. 3.55−3.56, show the corresponding simulated time responses of the converter for different perturbations. Fig. 3.55 shows the output-voltage response after introducing step-changes in output power 10% ∼ 90% at 0.035 s and 0.07 s. Similarly, output voltage u_o response for step-changes in input voltage from 20 V to 70 V is illustrated in Fig. 3.56. In this case, a step perturbation of 50 V is introduced at 0.04 s, and a negative step of -50 V at 0.075 s over 40% of an averaged nominal input voltage of 50 V.

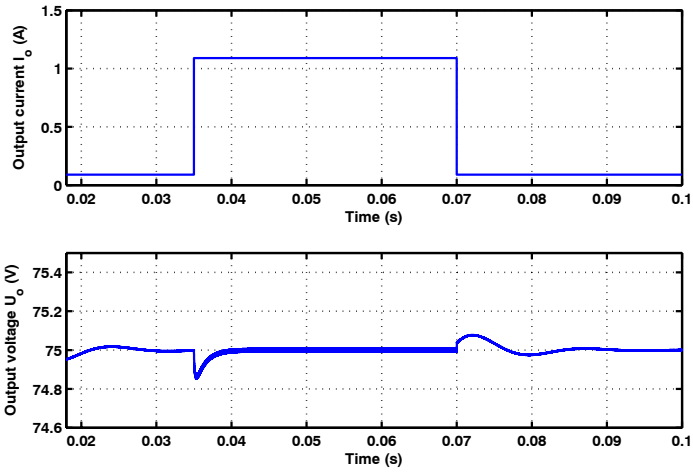


Figure 3.55: The output voltage response u_o for load perturbations

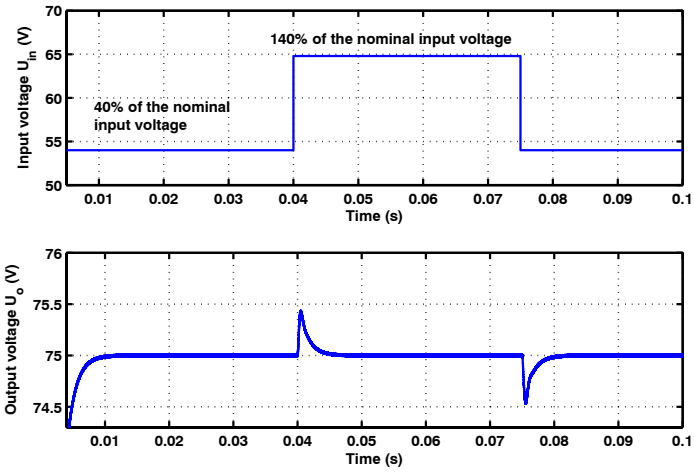


Figure 3.56: The output voltage behavior u_o for input voltage perturbations

Chapter 4

Subsystem Interaction Analysis

Analyzing complex combinations of Distributed Power Supply (DPS) systems becomes very complicated, when the system topologies get larger. A practical approach is to consider a system as an interconnection of many smaller subsystems. The unterminated modeling technique is useful especially in the analysis of large systems, such as DPS systems. Since the source and the load impedances affect the dynamics of the converter, it is important to understand how the terminal impedances of the subsystems are reflected to elsewhere in the system and how they affect the dynamics in general, [12, 17].

Some of the critical issues when integrating subsystems are stability problems, robustness of the subsystems and degradation resulting from interaction between the subsystems. Even though each subsystem may be well-designed for stand-alone operation, the interaction can lead to stability and performance problems after system integration.
The first studies on subsystem interaction in power converters addressed the interaction between an input filter and a regulated power converter [12, 17]. The methods proposed in these papers were based on linear techniques that worked on small-signal models of nonlinear systems linearized around a steady state operating point. The widely used impedance ratio criterion was generally used together with various control strategies in [61, 62, 63, 64, 65]. The design of input filters for power factor correction circuits was introduced in [66]. The factors affecting the choice of the filter topology for power factor correction circuits were outlined.

The stability analysis of distributed power systems was addressed in [67, 68, 69, 70]. In [68], the impedance ratio criterion was used to ensure the local stability of the power distribution system.

In this chapter, the concept known as unterminated two-port network representation is presented and used to develop a proper formalism for the terminated models, which may facilitate the analysis of the effect of different loads on the converter dynamics. First, several stability criterions and the forbidden region concept, which ensure the system stability, are briefly surveyed. Then, applying the unterminated technique to study the effect of load impedance on converter's dynamics is considered, resulting in the terminated model. This corresponds to the model that could have been derived initially by including the load impedance in the model. Finally, the analysis is extended to cover the effect of source impedance.

An unterminated model is derived for a single-section LC low-pass filter, and a system consisting of a converter and an input filter is analyzed. The origin of input filter instability is shown, and the input filter's influence on the dynamics of the converter is analyzed and demonstrated.

4.1 Two-Port Network

A two-port network is characterized by its terminal properties. Both ports of a two-port network can be characterized by a Thévenin or Norton equivalent circuit, depending on the choice of the input and output variables. External networks that are connected at the input and output are called terminations. To make the system modular, filters and converters must be modeled without terminating impedances. This modeling method is known as unterminated modeling technique [71, 72]. It has been applied e.g. to analyze the input filter interactions [73, 74, 65], and to design a controller for a line conditioner with unknown load [75, 76]. It is an especially useful technique for analysis of large systems, such as DPS systems. In e.g. [72, 77, 15, 67, 78] the unterminated modeling technique has been applied to modeling and analysis of distributed power systems.

In order to utilize the modular concept, each component should be modeled as an unterminated two-port network first, because the terminal characteristics of both source and load are unknown until the complete system is configured. The interconnection law should not only describe accurately the signal flows between the subsystems but it should also be presented in a standard form [71], to make a general and systematic analysis possible.

4.1.1 Unterminated Modeling Approach

A switched-mode converter can be presented as shown in Fig. 4.1 connected to supplying system and load. The supply system is characterized using its unterminated Thevenin's equivalent circuit (i.e., u_{ins} and source impedance Z_s). The load system is characterized using its terminated Norton's equivalent circuit (i.e., load impedance Z_L and current sink j_o) [73].

As it may be concluded from Fig.4.1, the practical model of a converter is its unterminated model, because the supply system and load depend on the special application, and should therefore be treated case by case. The transfer functions describing the converter dynamics are commonly given for resistive load (i.e., $Z_L = R$), as in [28]. The unterminated transfer functions may be easily derived from the resistor based transfer functions by letting $R \rightarrow \infty$, and taking the limiting value of the corresponding terminated transfer function, (4.1),

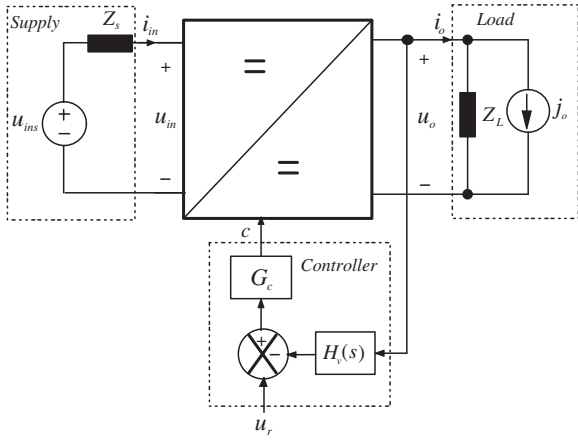


Figure 4.1: A dc-dc converter with connections to the supply system and the load system.

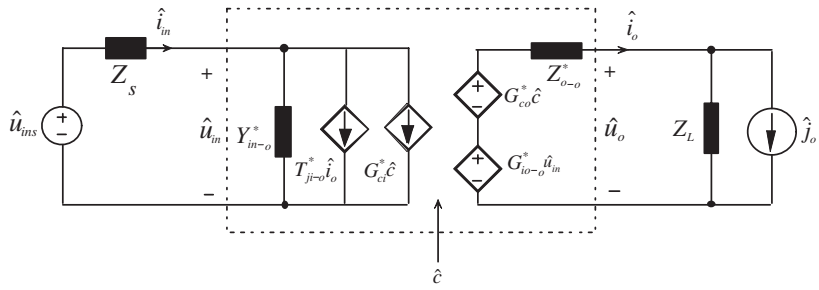


Figure 4.2: A circuit theoretical unterminated model with connections to a supply system and load.

provided that the average inductor current I_L in the model is not modified. Otherwise, the transfer functions can be derived in a normal way assuming the load composed of a constant-current sink.

$$G^*(s) = \lim_{R\to\infty} G_R(s) \tag{4.1}$$

Generally, the open-loop output dynamics of a converter may be defined as (4.2) and the open-loop input dynamics as (4.3).

$$\hat{u}_o = G^*_{io-o} \cdot \hat{u}_{in} - Z^*_{o-o} \cdot \hat{i}_o + G^*_{co} \cdot \hat{c} \tag{4.2}$$

$$\hat{i}_{in} = Y^*_{in-o} \cdot \hat{u}_{in} + T^*_{ji-o} \cdot \hat{i}_o + G^*_{ci} \cdot \hat{c} \tag{4.3}$$

The unterminated models describe the dynamics of a converter without the external effect of the supplying system and the load. It is only suitable of evaluating the dynamic performance when the source impedance of the supplying system is negligible, and the load composes of pure constant-current type load.

An unterminated circuit theoretical model of a converter connected to a supplying system and load is shown in Fig. 4.2. The output port parameters (i.e., Thevenin equivalent circuit) are defined in (4.2), and the input port parameters (i.e., Norton equivalent circuit) are defined in (4.3).

4.2 System Stability and Performance

Consider a system of two cascaded subsystems shown in Fig. 4.3, the first being the source subsystem and the second the load subsystem.

The main critical issues when integrating subsystems are usually stability problems, robustness of the subsystems and degradation of performance. Even though the subsystems may be well-designed for stand-alone operation, this interaction can lead to stability and performance problems after system integration. Therfore, the interaction of the subsystems must be considered to ensure proper operation of the integrated system.

4.2.1 Linear fractional transformations: The matrix star product

Linear fractional transformations (LFT) are a convenient tool to formulate many mathematical objects, as they are currently used in control literature for analysis and design, as

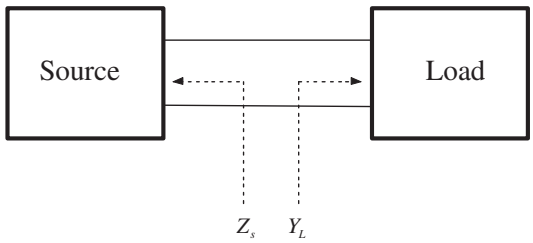
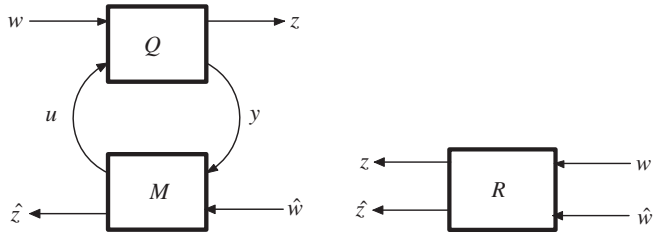


Figure 4.3: Simple source - load system

explained e.g. in [49, 50]. An important property of LFTs is that any interconnection of LFTs is again an LFT. This property is by far the most often used and is the heart of LFT machinery. A generalization of the upper and lower LFT is provided by the so-called Redheffer's star product. A system theoretic diagram of the series connection is shown in Fig. 4.4(a), where the input variables are w and $\hat{w}$, output variables z and $\hat{z}$, and internal variables u and y.

The matrices Q and M are interconnected such that the last y outputs from Q are the first y inputs of M, and the first u outputs from M are the last u inputs of the Q.



(a) Two cascaded subsystems. (b) Input-output model.

Figure 4.4: Star product of Q and M, $R = \mathcal{S}(Q, M)$.

The corresponding partitioned matrices are

$$Q = \begin{bmatrix} q_{11} & q_{12} \\ q_{21} & q_{22} \end{bmatrix}, \qquad M = \begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{bmatrix}$$

The mapping from the input to intermediate variables can be given by

$$\begin{bmatrix} y \\ u \end{bmatrix} = \begin{bmatrix} \frac{q_{21}}{1-q_{22}m_{11}} & \frac{q_{22}m_{12}}{1-q_{22}m_{11}} \\ \frac{m_{11}q_{21}}{1-q_{22}m_{11}} & \frac{m_{12}}{1-q_{22}m_{11}} \end{bmatrix} \begin{bmatrix} w \\ \hat{w} \end{bmatrix} \tag{4.4}$$

The mapping from the input to output variables can be given by

$$\begin{bmatrix} z \\ \hat{z} \end{bmatrix} = \underbrace{\begin{bmatrix} q_{11} + \frac{q_{12}m_{11}q_{21}}{1-q_{22}m_{11}} & \frac{m_{12}}{1-q_{22}m_{11}} \\ \frac{m_{21}q_{21}}{1-q_{22}m_{11}} & m_{22} + \frac{m_{21}q_{22}m_{12}}{1-q_{22}m_{11}} \end{bmatrix}}_{R} \begin{bmatrix} w \\ \hat{w} \end{bmatrix} \tag{4.5}$$

The input-output model shown in Fig. 4.4(b) and the overall matrix R with these interconnections closed is called the star product, $\mathcal{S}(Q, M)$, between Q and M,

$$R = \mathcal{S}(Q, M) = \begin{bmatrix} q_{11} + \frac{q_{12}m_{11}q_{21}}{1-q_{22}m_{11}} & \frac{m_{12}}{1-q_{22}m_{11}} \\ \frac{m_{21}q_{21}}{1-q_{22}m_{11}} & m_{22} + \frac{m_{21}q_{22}m_{12}}{1-q_{22}m_{11}} \end{bmatrix} \tag{4.6}$$

For practical calculations it is worth mentioning that the overall matrix R can be computed using the Matlab function *starp*.

4.2.2 Internal Stability

Internal stability is a fundamental requirement for a practical feedback system . It guarantees that all signals in a system are bounded provided that the injected signals (from anywhere) are bounded. Since the theorems of internal stability are well-known and understood [49, 50], it now becomes obvious that they are also equivalent to cascaded connections of canonical forms [80, 81].

Consider the system in Fig. 4.5 which is usually used to study the internal stability of system. By regrouping the external input signals into the loop as $e_1 = q_{21}w$ and $e_2 = m_{12}\hat{w}$, simple calculations show that the equations describing the system lead exactly to the intermediate equations (4.4), [80, 81].

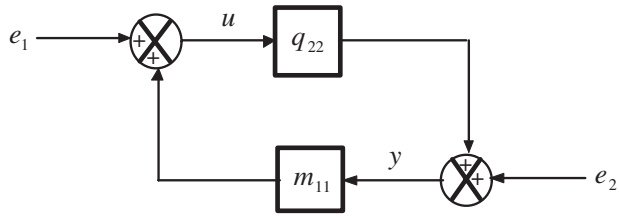


Figure 4.5: Internal stability topology.

The series connection of two subsystems represented in canonical forms is internally stable if

- the transfer functions q_{21} and m_{12} are stable (so that the signals e_2 and e_1 are bounded)
- the transfer functions $\frac{1}{1-q_{22}m_{11}}$, $\frac{q_{22}}{1-q_{22}m_{11}}$, $\frac{m_{11}}{1-q_{22}m_{11}}$ and $\frac{1}{1-q_{22}m_{11}}$ are stable

In addition, if no right half plane (RHP) pole-zero cancelations occur in the transfer functions $q_{22}m_{11}$, the stability of one the above transfer function implies stability of the others. Then, it is enough to check the stability of $1/(1 - q_{22}m_{11})$, which corresponds to application of the Nyquist criterion to the quantity -$q_{22}m_{11}$, [49, 50, 80, 81].

Note that the transfer functions q_{22} and m_{11} are the corresponding source output impedance and load input admittance of the subsystem shown in Fig. 4.3 (i.e. $q_{22} = -Z_s$ and $m_{11} = Y_L = 1/Z_L$). The quantity Z_sY_L is also known as the minor loop gain which determines, under the above assumptions, whether the system is internally stable or not.

4.2.3 Forbidden region concept

The stability analysis of distributed power supply systems is mainly based on the minor loop gain concept. The minor loop gain is calculated as the ratio of output and input impedances defined at the interface of source and load systems.

For the purposes of control design, there are numerous methods of ensuring that the Nyquist contour of $Z_s\ Y_L$ does not encircle the point $(-1, 0)$, thereby providing a guarantee of system stability [12, 82, 83, 18]. The result of the analysis is given by defining a certain forbidden region in the complex plane, out of which the minor loop gain should stay for stability. The concept of forbidden region is usually based on the use of the gain (GM) and phase (PM) margins associated to the minor loop gain. Next, two stability criteria will be briefly discussed.

Middlebrook Criterion:

This is the most straightforward of the impedance/admittance methods [12]. It consists of a circle of radius 1/GM in the s-plane, where GM denotes the gain margin associated to the minor loop gain as shown in Fig. 4.6. The shaded region is the forbidden region. Obviously, if the Nyquist plot of $Z_s\ Y_L$ is always within the circle, then encirclements of the point $(-1, 0)$ cannot occur provided that the GM is greater than 1.

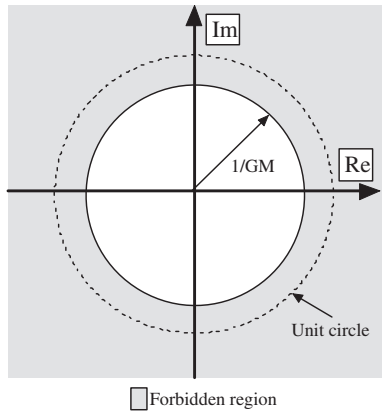


Figure 4.6: Middlebrook Stability Criterion.

Although convenient for design and easily visualized, this approach leads to artificially conservative designs. In particular, much of the region in Nyquist plane which is forbidden when using this criterion actually may have little influence on stability [18].

Gain Margin and Phase Margin (GMPM) Criterion:

In this criterion, the boundary consists of two line segments at an angle of ±PM from the negative real axis, which extend from infinity to the circle corresponding to the Middlebrook criterion; the forbidden region in this case is indicated in Fig. 4.7.

The proposed gain margin is 6 dB and phase margin 60°. It is stated that if both subsystems are stable and if the polar plot of the minor loop gain avoids the forbidden

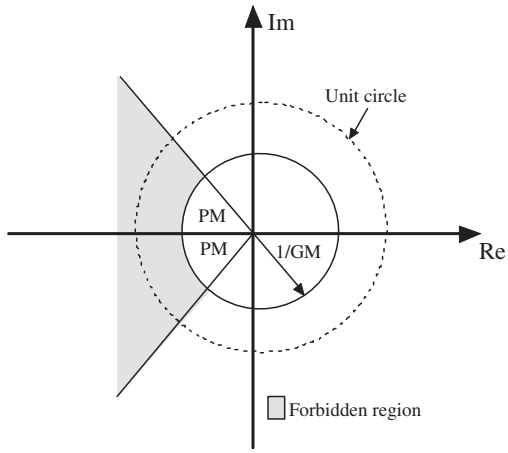


Figure 4.7: Gain Margin and Phase Margin (GMPM) Stability Criterion.

region, then it is guaranteed that the integrated system is stable and will have minimal performance degradation.

The main advantage of this method is that, both the gain and phase margins can be arbitrary specified, allowing the designer to specify the amount of conservatism in a given design. Moreover, it is also amenable to formulation of design specifications. Assuming that the source impedance is known, the range of input impedance which would cause the minor loop gain function to violate the forbidden region, if interaction were to occur at a given frequency, can be calculated. The condition for stability can then be expressed as [18]

$$|Y_L| < \frac{1}{|Z_L|\,\mathrm{GM}} \tag{4.7}$$

$$\angle Y_L(s) + \angle Z_s(s) \leq (180^\circ - \mathrm{PM}) \tag{4.8}$$

$$\angle Y_L(s) + \angle Z_s(s) \leq (-180^\circ + \mathrm{PM}). \tag{4.9}$$

The above criterion is used extensively e.g. by the power system of the space station program [82].

4.3 Load and Supply Interaction Analysis

The operation of the converter is affected by the source impedance and the load impedance, Fig. 4.3. Load impedances naturally affect all input-to-output transfer functions of the open-loop converter. It is clear that the loop gain and the closed-loop dynamics of the converter are affected as well. Source impedance affects the output-port dynamics of the open-loop converter. Since the control-to-output transfer function is affected, the loop gain is affected as well. It can be concluded that the performance of the converter can be degraded by the load or source interactions. When considering distributed power supply systems, it is therefore of interest to study the source impedance and the load impedance effects on the converters.

4.3.1 Load Interaction Analysis

The loads of switching converters are usually not simple resistive loads, but instead consist of complex and frequency dependent impedances. Furthermore, for most practical applications prior information on the ac characteristics of a load is often unavailable, therefore, a control loop design assuming a specific load may result in an undesirable performance that was not intended during the design stage, and an analytical interpretation of the results may be lost.
In order to examine the interactions between a switching converter and its load, the performance parameters of the terminated converter should be derived as a function of the load terminal characteristics. In the following a formalism to analyze the load interactions and the effect of each of its impedances on the converter transfer functions is analyzed. To that end the unterminated two-port small-signal model, Fig. 4.2, and the Linear fractional transformation (LFTs) technique are utilized. The unterminated modeling technique together with LFTs can most conveniently be used because of the transparency and easy application of circuit theory and a reflection principle. Similar formalism may be derived using the extra-element-theorem (EET) method introduced in [28, 84], but it is too theoretical for practicing engineers to apply.

We can now apply the LFT approach to the unterminated converter and load shown in Fig. 4.2. The terminated transfer matrix $\mathcal{S}\left(G_{con}, G_L\right)$ can be obtained by applying (4.6) as follows

$$G_{CL} = \mathcal{S}\left(G_{con}, G_L\right) = \begin{bmatrix} Y^*_{in-o} + \frac{1/Z_L \cdot G^*_{io-o} T^*_{ji-o}}{\frac{Z^*_{o-o}}{1+\frac{Z_L}{Z_L}}} & \frac{G^*_{ci}}{\frac{Z^*_{o-o}}{1+\frac{Z_L}{Z_L}}} & \frac{T^*_{ji-o}}{\frac{Z^*_{o-o}}{1+\frac{Z_L}{Z_L}}} \\ \frac{G^*_{io-o}}{\frac{Z^*_{o-o}}{1+\frac{Z_L}{Z_L}}} & \frac{G^*_{co}}{\frac{Z^*_{o-o}}{1+\frac{Z_L}{Z_L}}} & -\frac{Z^*_{o-o}}{\frac{Z^*_{o-o}}{1+\frac{Z_L}{Z_L}}} \end{bmatrix} \tag{4.10}$$

which can obviously be rewritten as an open-loop terminated two-port model (4.11)

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y_{in-o} & G_{ci} & T_{ji-o} \\ G_{io-o} & G_{co} & -Z_{o-o} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{c} \\ \hat{j}_o \end{bmatrix} \tag{4.11}$$

Similarly, the closed-loop terminated two-port model can be given as follows

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y_{in-c} & T_{ji-c} \\ G_{io-c} & -Z_{o-c} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{j}_o \end{bmatrix} \tag{4.12}$$

Terminated converter transfer functions

The open-loop and closed-loop terminated converter equations (4.13) and (4.15) provide an analytical closed form expression, from which the performance parameters of the converter can be expressed by well defined quantities, load impedance Z_L and closed-loop output impedance of the unterminated converter Z^*_{o-c}.

$$G_{io-o} = \frac{1}{1+\frac{Z^*_{o-o}}{Z_L}} \cdot G^*_{io-o}, \qquad G_{io-c} = \frac{1}{1+\frac{Z^*_{o-c}}{Z_L}} \cdot G^*_{io-c} \tag{4.13}$$

$$Z_{o-o} = \frac{1}{1+\frac{Z^*_{o-o}}{Z_L}} \cdot Z^*_{o-o}, \qquad Z_{o-c} = \frac{1}{1+\frac{Z^*_{o-c}}{Z_L}} \cdot Z^*_{o-c} \tag{4.14}$$

$$G_{co} = \frac{1}{1+\frac{Z^*_{o-o}}{Z_L}} \cdot G^*_{co} \tag{4.15}$$

Thus, using Z^*_{o-c} and Z_L, stability of the converter can be determined by applying the Nyquist criterion to the quantity $\frac{Z^*_{o-c}}{Z_L}$, under the assumption of both Z^*_{o-c} and Z_L being stable, which implies that $\frac{Z^*_{o-c}}{Z_L}$ does not have RHP poles. Thus, from the above assumption, the sufficient condition for the stability of the converter is simply $\left|Z^*_{o-c}\right| \ll |Z_L|$.

Loop gain analysis

The load effect on the converter dynamics can be analyzed starting from (assume $H_v(s) = 1$) according to (2.38), where $L^*_g(s)$ is the original (unterminated) loop gain, and $L_g(s)$ is the affected (terminated) loop gain.

$$L_g(s) = G_a G_c G_{co} \tag{4.16}$$

$$\begin{aligned} L_g(s) &= \frac{G^*_{co}}{1+\frac{Z^*_{o-o}}{Z_L}} \cdot G_a G_c \\ &= \frac{1}{1+\frac{Z^*_{o-o}}{Z_L}} \cdot L^*_g(s) \end{aligned} \tag{4.17}$$

It is clear that the converter loop gain $L^*_g(s)$ is not substantially affected by load impedance Z_L if the condition

$$\left|Z^*_{o-o}\right| \ll |Z_L| \tag{4.18}$$

is satisfied.

Define $\frac{Z^*_{o-c}}{Z_L}$ as the minor loop gain $L_m(s)$. It is argued that the minor-loop gain contains similar dynamic performance and stability information as the loop gain of the converter. However, the terminated loop gain may be defined in terms of minor loop by starting from (4.17) and noting that $Z^*_{o-c} = \frac{Z^*_{o-o}}{1+L^*_g(s)}$

$$L_g(s) = \frac{L^*_g(s)}{1 + L_m(s)\left(1 + L^*_g(s)\right)} \tag{4.19}$$

In order to minimize the loading effects of prospective loads, it seems that the closed output impedance $\left|Z^*_{o-c}\right|$ of the unterminated converter can only be minimized using a control loop design presented in Chapter 3. The stability and performance will be analyzed by investigating the loop gain, minor loop gain and output impedance of the converter combined with a variety of typical practical loads.

By examining the terminated system loop gain, $L_g(s)$ it can be seen that if the loading effect is negligible, meaning that $|L_m(s)| \ll 1$ at all frequencies, then $L_g(s)$ is approximately equal to $L^*_g(s)$. However, if the loading effect is not negligible, then in general there are two possible cases to consider. These involve the study of interaction below and beyond the

crossover frequency of the unterminated converter loop gain $L_g^*(s)$. All cases of interaction in an actual system will be among the combinations of these two cases.

Example 4.1

To investigate the loading effect on the performance of the converter, the VM and PCM controlled buck converter will be analyzed. Analysis of the loading effect on the converter loop gain will be carried out using the impedance-type load shown in Fig. 4.8. The corresponding load element values are shown in Table 4.1.

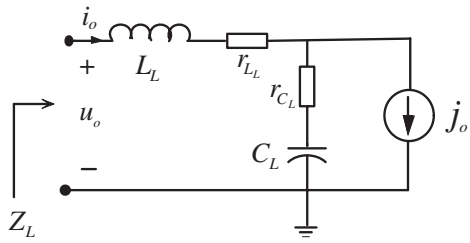


Figure 4.8: LC-type load .

Table 4.1: Load circuits parameters.

Load	L_L	C_L	r_{L_L}	r_{C_L}
A	1 mH	3 mF	50 mΩ	250 mΩ
B	105 μH	316 μF	0.05 mΩ	1 mΩ
C	2 μH	10 μF	2 mΩ	5 mΩ

The unterminated loop gain $L_g^*(s)$, terminated loop gain $L_g(s)$, and minor loop gain, $L_m(s)$ are analyzed for each of the three load cases. These gains related to VMC and PCMC control modes are shown in Fig. 4.9 and Fig. 4.10. The differences in the responses may be explained by the differences in the open-loop output impedances and control bandwidths. It can be seen from Fig. 4.9 and Fig. 4.10 that for load A which does not interact, the minor loop gain, $L_m(s)$, is always much less than 0 dB at all frequencies, so in this case the loading effect is negligible.

The first case to be analyzed is the impedance overlap occurring below the loop gain crossover frequency of the converter. The unterminated $L_g^*(s)$, terminate $L_g(s)$ loop gains and minor loop gain $L_m(s)$ of the VMC and PCMC converters, when the load resonant frequency coincides with the converter resonant frequency, as depicted in Figs. 4.11 and 4.12. In this case, the terminated loop gain $L_g(s)$ has three crossovers the 0-dB line.

From Fig. 4.11 and 4.12 it can clearly be seen that in the first two crossover frequencies the terminated (loaded) loop gain $L_g(s)$ has approximately the same phase margin as the minor loop gain $L_m(s)$. This means that if the minor loop gain $L_m(s)$ has a high stability margin at these crossover frequencies, then $L_g(s)$ does also. At the final crossover point,

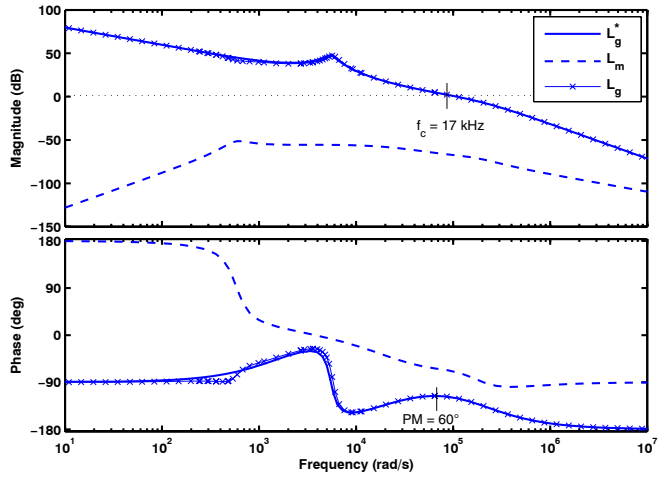


Figure 4.9: Unterminated loop gain (solid line), terminated loop gain (dotted line), and minor loop gain (dashed line) in case of load A, VMC.

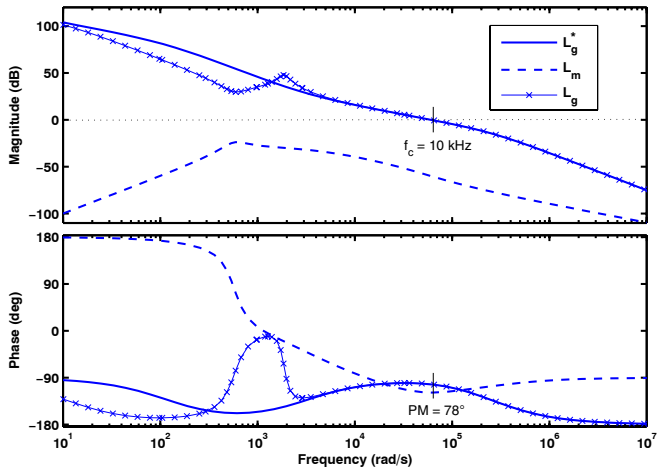


Figure 4.10: Unterminated loop gain (solid line), terminated loop gain (dotted line), and minor loop gain (dashed line) in case of load A, PCMC.

$L_m(s)$ is small, so $L_g(s)$ is approximately equal to $L_g^*(s)$, and they have the same stability margin. Consequently, if both $L_m(s)$ and $L_g^*(s)$ have high stability margins, so does $L_g(s)$. However, it can also be seen that the bandwidth of $L_g(s)$ is considerably reduced, which will have an effect on the transient response. This case corresponds to the undesirable case of low-frequency interaction, which will degrade the transient response of the system

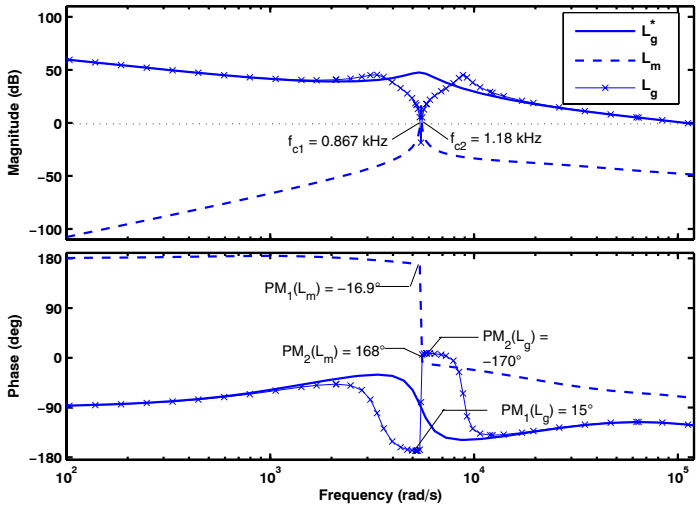


Figure 4.11: Unterminated loop gain (solid line), terminated loop gain (dotted line), and minor loop gain (dashed line) in case of load B, VMC.

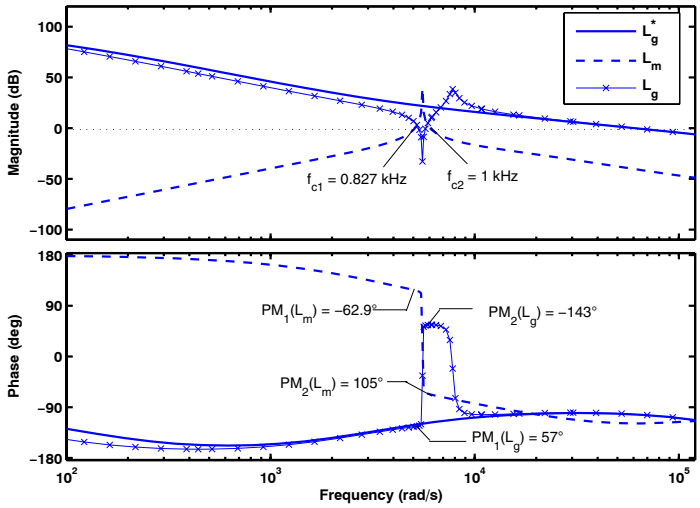


Figure 4.12: Unterminated loop gain (solid line), terminated loop gain (dotted line), and minor loop gain (dashed line) in case of load B, PCMC.

significantly.

The second case of interaction occurs beyond the loop gain crossover frequency of the

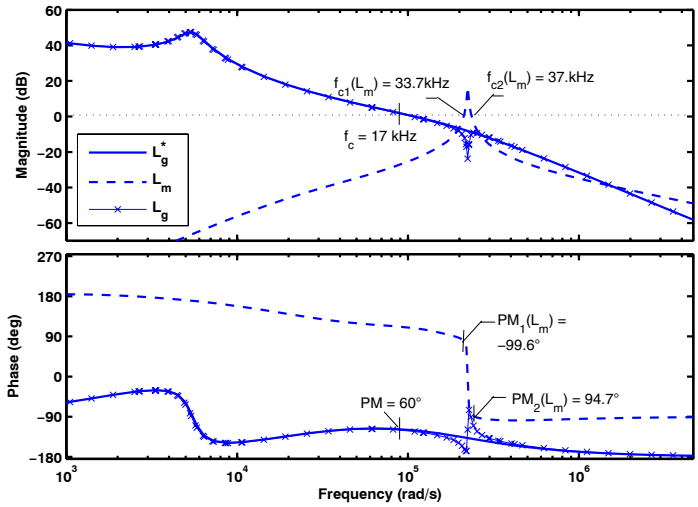


Figure 4.13: Unterminated loop gain (solid line), terminated loop gain (dotted line), and minor loop gain (dashed line) in case of load C, VMC.

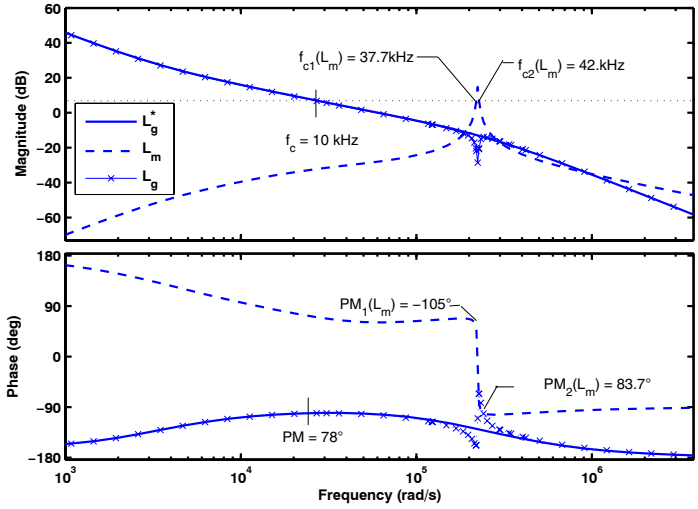


Figure 4.14: Unterminated loop gain (solid line), terminated loop gain (dotted line), and minor loop gain (dashed line) in case of load C, PCMC.

converter; this is shown in Fig. 4.13 and Fig. 4.14. In this case, it can be seen that the loading effect on the subsystem loop gain occurs in frequencies where the unterminated

(unloaded) loop gain magnitude $L_g^*(s)$, is less than 0 dB. The terminated loop gain, $L_g(s)$ differs from $L_g^*(s)$ only at high frequencies when the magnitude is small, and therefore system performance will be unaffected. The terminated loop gain, $L_g(s)$ has the same phase margin as $L_g^*(s)$ at the crossover frequency. This is because $L_m(s)$ is small, so $L_g(s)$ is approximately equal to $L_g^*(s)$ in this range.

The output impedances related to VMC and PCMC modes are shown in Fig. 4.15 and Fig. 4.16 in relation to the input impedance of three loads. By examining the phase of Z_{o-c}^* and Z_L in Fig. 4.15 and Fig. 4.16, it can be seen that a low frequencies the phase of the minor loop gain $L_m(s)$ approaches 180°, and at high frequencies, the phase of $L_m(s)$ approaches −180°. Therefore, interaction at high or low frequencies will cause minor loop gain, $L_m(s)$, to have a small phase margin. It can be clearly seen that for load A which does not interact, the minor loop gain, $L_m(s)$, is always less than 0 dB, so in this case the loading effect is negligible. However, as the degree of impedance overlap increases, the interaction moves to the low and high frequency range, thus causing the phase of $L_m(s)$ to decrease.

The stability and performance of the terminated converter in VMC can be analyzed from the Nyquist plot of the minor loop gain $L_m(s)$ as shown in Fig. 4.17. It is obvious for load A which has no impedance interaction that the minor loop function is in the acceptable region at all frequencies and the terminated converter is stable retaining the closed-loop performance of the unterminated converter. The minor loop gain of load B indicates heavy violations of the forbidden region. Therefore, the performance is clearly deteriorated, but the terminated converter is still stable. Although load C has noticeable impedance overlap, it does not violate the forbidden region. However, the terminated converter remains stable.

The minor loop of the PCMC converter is shown in Fig. 4.18. For loads A and C the minor loop gains have analogous behavior to the VMC case. Load B causes the output impedance to dip within the frequency range where the condition $\left|Z_{o-c}^*/\mathrm{Z_L}\right| \ll 1$ is violated. It is interesting to note that the minor loop gain does not heavily violate the forbidden region

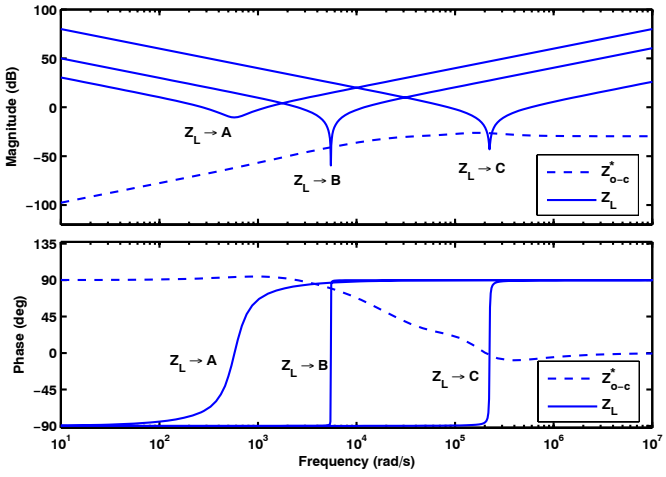


Figure 4.15: Output impedance of the converter vs. three different loads, VMC.

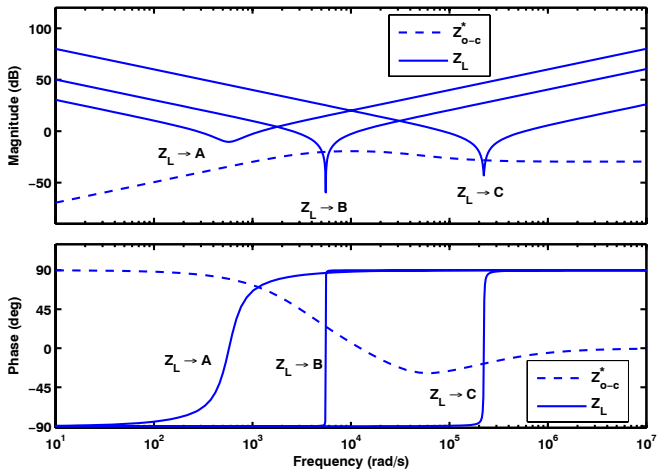


Figure 4.16: Output impedance of the converter vs. three different loads, PCMC.

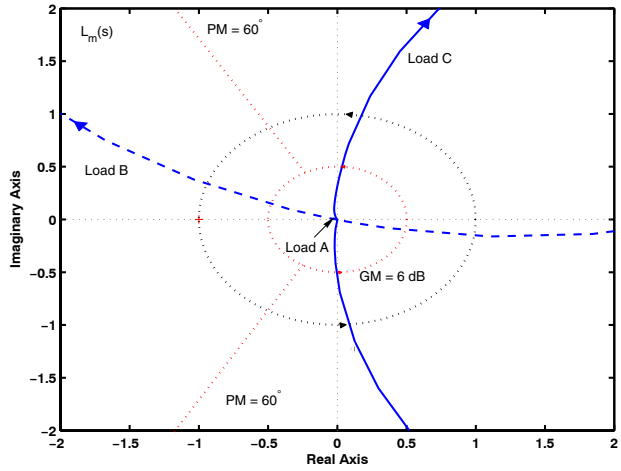


Figure 4.17: Nyquist Plots of the minor loop gains at three different loads, VMC.

and the terminated converter retains its stability.

When the transient response is examined (Fig. 4.19), it is obvious that for load A, which has no impedance interaction, there is no significant change in the output voltage. However, in the case of load B the load effect causes the terminated loop gain to crossover at a frequency slightly lower than in the unterminated loop gain. Therefore it is clear that the output voltage is slower and has a more oscillatory dynamics. In the case of load C, the loading effect causes the terminated loop gain to crossover at a frequency slightly higher

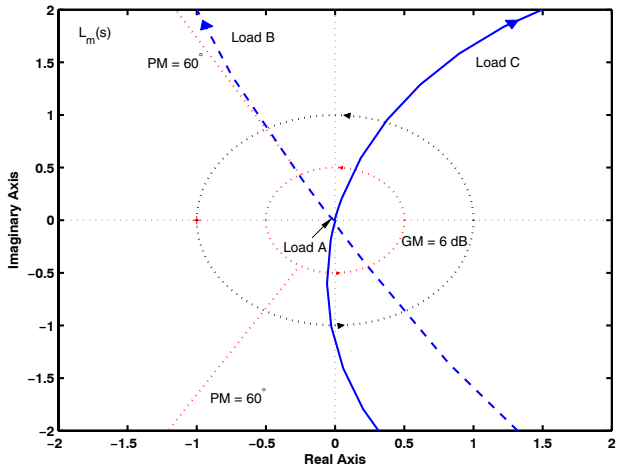


Figure 4.18: Nyquist Plots of the minor loop gains at three different loads, PCMC.

than in the case of load B. Since both of the loop gains have the same bandwidth, the system will respond more faster than in the case of load B.

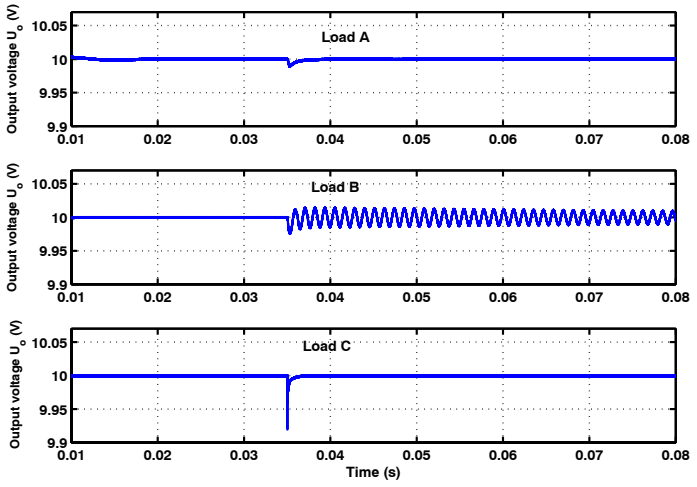


Figure 4.19: Transient response of three different loads when the load change from 10% to 90% occurs at 0.035s, VMC.

It is a tedious task to design voltage feedback compensation that provides a minimized output impedance in which the loading effects become negligible, while retaining good closed-loop performance for the unterminated converter. The above example shows that the voltage feedback compensation failed to mitigate the impedances overlap for an ill-conditioned load.

4.3.2 Source Interaction Analysis

A two-port model with a connection to the source impedance (see e.g. Fig. 4.2) is considered. It is clear that the source impedance does not affect the input port parameters of the converter. For that reason it is sufficient to study only the output dynamics. The new expressions for transfer functions can be derived by another application of the LFT approach

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_{in} \end{bmatrix} = \underbrace{\left[\begin{array}{c|c} 0 & 1 \\ \hline 1 & -Z_s \end{array}\right]}_{G_S} \begin{bmatrix} \hat{u}_{ins} \\ \hat{i}_{in} \end{bmatrix} \tag{4.20}$$

The resulting transfer matrix $\mathcal{S}(G_s, G_{con})$ can be obtained by applying (4.6) as follows

$$G_{sc} = \begin{bmatrix} \frac{Y^*_{in-o}}{1+Z_sY^*_{in-o}} & \frac{T^*_{ji-o}}{1+Z_sY^*_{in-o}} & \frac{G^*_{ci}}{1+Z_sY^*_{in-o}} \\ \frac{G^*_{io-o}}{1+Z_sY^*_{in-o}} & -Z^*_{o-o} - \frac{T^*_{ji-o}G^*_{io-o}Z_s}{1+Z_sY^*_{in-o}} & \frac{1+Z_s\cdot\left(Y^*_{in-o}-\frac{G^*_{io-o}G^*_{ci}}{G^*_{co}}\right)G^*_{co}}{1+Z_sY^*_{in-o}} \end{bmatrix} \tag{4.21}$$

which can obviously be rewritten as an open-loop terminated two-port model (4.22)

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y'_{in-o} & G'_{ci} & T'_{ji-o} \\ G'_{io-o} & -Z'_{o-o} & G'_{co} \end{bmatrix} \begin{bmatrix} \hat{u}_{ins} \\ \hat{i}_o \\ \hat{c} \end{bmatrix} \tag{4.22}$$

Similarly, the closed-loop terminated two-port model can be given as follows

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y'_{in-c} & T'_{ji-c} \\ G'_{io-c} & -Z'_{o-c} \end{bmatrix} \begin{bmatrix} \hat{u}_{ins} \\ \hat{i}_o \end{bmatrix} \tag{4.23}$$

The closed-loop terminated converter equations (4.24) and (4.25) provide an analytical closed from expression, from which the performance parameters of the converter can be expressed, as well as the defined quantities, source impedance Z_s and closed-loop input admittance of the unterminated converter Y^*_{in-c}.

$$G'_{io-c} = \frac{1}{1+Z_sY^*_{in-c}} \cdot G^*_{io-c} \tag{4.24}$$

$$Z'_{o-c} = \frac{1+Z_sY^*_{in-sc}}{1+Z_sY^*_{in-c}} \cdot Z^*_{o-c} \tag{4.25}$$

where

$$Y^*_{in-sc} = Y^*_{in-c} + \frac{T^*_{ji-c}G^*_{io-c}}{Z^*_{o-c}}$$

Thus, using the Y^*_{in-c} and Z_s, stability of the converter can be determined by applying the Nyquist criterion to the quantity $\frac{Z_s}{Z^*_{in-c}}$, where $Z^*_{in-c} = \frac{1}{Y^*_{in-c}}$. It is assumed that Z^*_{in-c} and Z_s are stable, which implies $\frac{Z_s}{Z^*_{in-c}}$ does not have RHP poles. Thus, from the above assumption, the sufficient condition for the stability of the converter is simply $|Z_s| \ll \left|Z^*_{in-c}\right|$.

Loop gain interactions $L_g^*(s)$

The effect of the source impedance on the converter dynamics can be considered according to (2.38) as (4.26), where $L_g^*(s)$ is the original loop gain, and $L_g{}'(s)$ is the affected loop gain.

$$L_g{}'(s) = \frac{1 + Z_s \cdot (Y_{in-o}^* - \frac{G_{io-o}^* G_{ci}^*}{G_{co}^*})}{1 + Z_s Y_{in-o}^*} \cdot L_g^*(s) = \frac{1 + Z_s Y_{in-\infty}^*}{1 + Z_s Y_{in-o}^*} \cdot L_g^*(s) \tag{4.26}$$

A similar analysis shows that the converter loop gain $L_g^*(s)$ is not substantially affected by source impedance Z_s if the conditions

$$|Z_s| \ll \left|Z_{in-o}^*\right| \tag{4.27}$$

$$|Z_s| \ll \left|Z_{in-\infty}^*\right| \tag{4.28}$$

are satisfied.

The problem of source impedance interaction in this thesis will be addressed and discussed, in particular, to the EMI input filter in the next section.

4.4 Input Filter Interactions in Switched-Mode Power Converters

In this section, an unterminated model is derived for a single-section LC low-pass filter, and a system consisting of a converter and an input filter is analyzed. The origin of input filter instability is shown, and the input filter's effect on the dynamics of the converter is analyzed and demonstrated. The analysis is then extended to study the interactions between two cascaded subsystems. It is assumed that the subsystems have been previously designed to meet the required specifications.

4.4.1 EMI Filters for Switching-Mode Power Converters

Any electrical or electronic device is a potential noise source to its environment. High-level electromagnetic disturbances may cause devices and systems to malfunction in a common electromagnetic environment.

Although it first emerged as a serious issue in telecommunications, electromagnetic interference (EMI) problems are also found in other applications. With the rapid growth and spread of power semiconductors and power electronics systems, interference levels on power systems have increased significantly in intensity and frequency of occurrence.

The basic operation of electronic power processing is the switching function to control the flow of electromagnetic energy through the converters. The switching function, however, is also the major mechanism of electromagnetic noise generation, which implies that a power converter is potentially a large noise source to its vicinity.

In order to prevent the input current waveform of the switching converter from interfering with the source and to maintain the integrity of the source for other equipment that may be operating from a common input power bus, the switching converter must include appropriate input electromagnetic interference (EMI) filtering. The input filter is also required to isolate the source voltage transients so as not to degrade the performance of the switching converter. Therefore, research on modeling and improving the EMI characteristics of power electronics converters by using appropriate circuit layout and input filter design is necessary [86, 28, 87].

Single-Section L-C Filter

The most common simple passive filter is the L-C passive filter shown in Fig. 4.20. The filter consists of an inductance L_f and a capacitance C_f with their equivalent internal resistances r_{LF} and r_{CF}. For simplicity, the total effective impedance of the source resistance is neglected. In general, the values of L_f and C_f are large enough to dominate the reactive impedance of the source. This will adequately attenuate the interference due to the signals at the switching frequency and its higher harmonics.

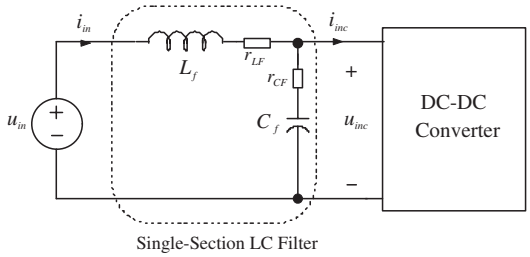


Figure 4.20: Single section LC Filter.

The transfer functions of the input filter can be derived as follows:

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_{inc} \end{bmatrix} = \left[\begin{array}{c|c} Y^*_{in-f} & T^*_{ji-f} \\ \hline G^*_{io-f} & -Z^*_{o-f} \end{array}\right] \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_{inc} \end{bmatrix} \tag{4.29}$$

$$Y^*_{in-f} = \frac{s \cdot \frac{1}{L_f}}{s^2 + s \cdot \frac{(r_{LF}+r_{CF})}{L_f} + \frac{1}{L_f C_f}} \tag{4.30}$$

$$T^*_{ji-f} = \frac{s \cdot C_f r_{CF} + 1}{s^2 + s \cdot \frac{(r_{LF}+r_{CF})}{L_f} + \frac{1}{L_f C_f}} \tag{4.31}$$

$$G^*_{io-f} = \frac{s \cdot C_f r_{CF} + 1}{s^2 + s \cdot \frac{(r_{LF}+r_{CF})}{L_f} + \frac{1}{L_f C_f}} \tag{4.32}$$

$$Z^*_{o-f} = \frac{s^2 \cdot r_{CF} + s \cdot (\frac{1}{C_f} + \frac{r_{CF} r_{LF}}{L_f}) + \frac{r_{LF}}{L_f C_f}}{s^2 + s \cdot \frac{(r_{LF}+r_{CF})}{L_f} + \frac{1}{L_f C_f}} \tag{4.33}$$

The quality factor Q_f [28] of the filter is as follows

$$Q_f = \frac{\sqrt{\frac{L_f}{C_f}}}{r_{LF} + r_{CF}} \tag{4.34}$$

The Q_f describes the resonance peaking of the filter. In practice, parasitic elements, such as inductor loss and capacitor equivalent series resistance limit the value of Q_f. If the parasitic elements are set to zero, as in the ideal filter, the Q_f tends to infinity. The peaking causes undesirable effects in switching converters, and therefore a low Q_f-value is desirable.

The single-section LC filter presents a peaking at the resonant frequency f_o. The phase of the output impedance changes rapidly in the vicinity of the resonance frequency f_o.

$$f_o = \frac{1}{2\pi\sqrt{L_f C_f}} \tag{4.35}$$

4.4.2 Nature of the Oscillation Problem

The addition of an input filter to a switching-mode converter can cause the combination to oscillate or even go unstable due to the fact that switching-mode converters usually have a negative input resistance at low frequencies. The nature of the problem can be understood by considering the buck converter with a basic single-section low-pass filter shown in Fig. 4.21.

A dc-dc converter is designed to keep its output voltage constant no matter how its input voltage varies. Given a constant load current, the power drawn from the input bus is therefore also constant. If the input voltage increases by some factor, the input current will decrease by this same factor to maintain the power level constant. In incremental terms, a positive incremental change in the input voltage results in a negative incremental change in the input current, causing the converter to look like a negative resistor R_{in} at its input terminals. The value of this negative resistance depends on the operating point of the converter according to:

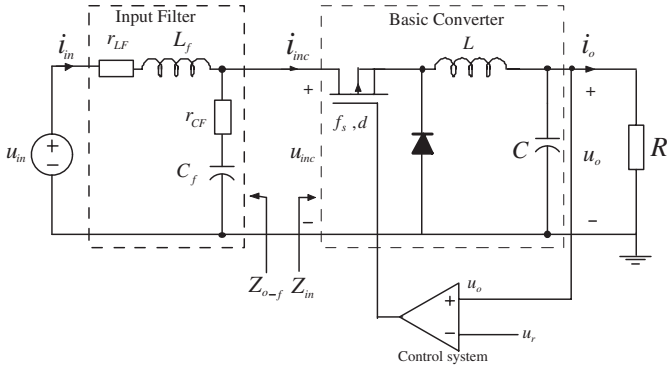


Figure 4.21: Basic Buck converter with single-section LC filter.

$$R_{in} = -\frac{U_{inc}}{I_{inc}} = -\frac{1}{M^2}\frac{U_o}{I_o} = -\frac{R}{M^2} \tag{4.36}$$

Note that the converter input impedance Z_{in}, appears as a negative resistance only at low frequencies. At higher frequencies the impedance is affected by the converter's own internal filter elements and the limited bandwidth of its feedback loop.

For the conversion ratio for the basic buck converter $M = D$ it then holds

$$R_{in} = -R/D^2 \tag{4.37}$$

The converter input resistance R_{in} with the input filter output impedance can under certain conditions constitute a *negative resistance oscillator* (NRO), which degrades the system stability and performance. The input filter output impedance Z_{o-f} is a low (positive)

resistance at low frequencies, but in the vicinity of the filter cutoff frequency it rises to a maximum $|Z_{o-f}|_{\max}$, which may be many times the associated ohmic resistances. Therefore the oscillation will take place when the net circuit resistance becomes negative [12].

4.4.3 Application of Two-Port Representation

The input filter can be also modeled using unterminated G-parameters as shown in Fig. 4.22.

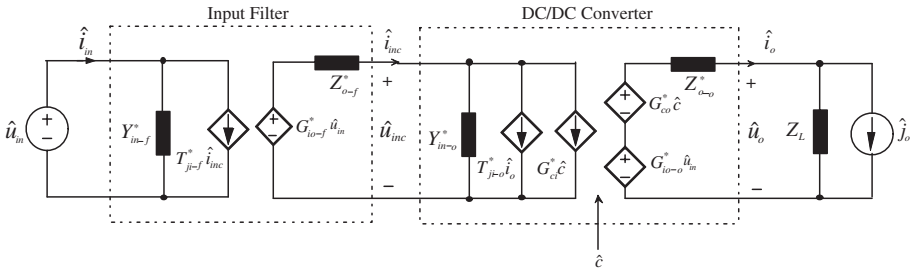


Figure 4.22: Switched-mode power converter with input filter.

To study how the input filter affects the output dynamics of a converter, new expressions for transfer functions can be derived by using LFTs. The resulting system dynamics in terms of G-parameters may be presented as shown in (4.38) in a matrix form and as a two-port model shown in Fig. (4.23).

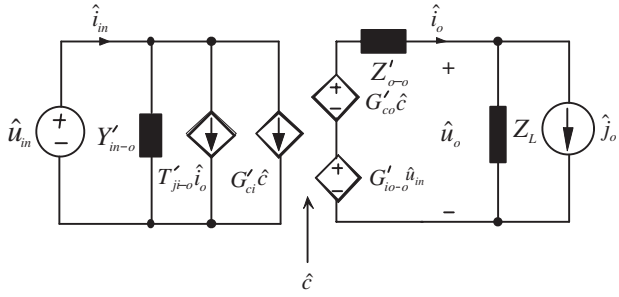


Figure 4.23: Overall two-port model.

The upper row of the matrix entries (i.e., the input dynamics) is defined in (4.39) - (4.41) and the bottom row (i.e., the output dynamics) is defined in (4.42) - (4.44), respectively.

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y'_{in-o} & T'_{ji-o} & G'_{ci} \\ G'_{io-o} & -Z'_{o-o} & G'_{co} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{c} \end{bmatrix} \tag{4.38}$$

$$Y'_{in-o} = Y^*_{in-f} + \frac{T^*_{ji-f} G^*_{io-f} Y^*_{in-o}}{1 + Z^*_{o-f} Y^*_{in-o}} \tag{4.39}$$

$$T'_{ji-o} = \frac{T^*_{ji-f} T^*_{ji-o}}{1 + Z^*_{o-f} Y^*_{in-o}} \tag{4.40}$$

$$G'_{ci} = \frac{T^*_{ji-f} G^*_{ci}}{1 + Z^*_{o-f} Y^*_{in-o}} \tag{4.41}$$

$$G'_{io-o} = \frac{G^*_{io-f} G^*_{io-o}}{1 + Z^*_{o-f} Y^*_{in-o}} \tag{4.42}$$

$$Z'_{o-o} = Z^*_{o-o} + \frac{Z^*_{o-f} T^*_{ji-o} G^*_{io-o}}{1 + Z^*_{o-f} Y^*_{in-o}} \tag{4.43}$$

$$G'_{co} = G^*_{co} - \frac{Z^*_{o-f} G^*_{io-o} G^*_{ci}}{1 + Z^*_{o-f} Y^*_{in-o}} \tag{4.44}$$

In a similar manner as described above the effect of the input filter may be deduced from the closed-loop converter transfer function as in (4.45)

$$\begin{aligned}
Y'_{in-c} &= Y^*_{in-f} + \tfrac{T^*_{ji-f} G^*_{io-f}}{1+Z^*_{o-f} Y^*_{in-c}} \cdot Y^*_{in-c} \\
T'_{ji-c} &= \tfrac{T^*_{ji-f}}{1+Z^*_{o-f} Y^*_{in-c}} \cdot T^*_{ji-c} \\
G'_{io-c} &= \tfrac{G^*_{ji-f}}{1+Z^*_{o-f} Y^*_{in-c}} \cdot G^*_{io-c} \\
Z'_{o-c} &= \tfrac{1+Z^*_{o-f}(Y^*_{in-c} + \frac{T^*_{ji-c} G^*_{io-c}}{Z^*_{o-c}})}{1+Z^*_{o-f} Y^*_{in-c}} \cdot Z^*_{o-c}
\end{aligned} \tag{4.45}$$

The output impedance Z'_{o-o} and control-to-output transfer function G'_{co} can be rewritten as

$$Z'_{o-o} = \frac{1 + Z^*_{o-f}(Y^*_{in-o} + \frac{T^*_{ji-o} G^*_{io-o}}{Z^*_{o-o}})}{1 + Z^*_{o-f} Y^*_{in-o}} \cdot Z^*_{o-o} = \frac{1 + Z^*_{o-f} Y^*_{in-sc}}{1 + Z^*_{o-f} Y^*_{in-o}} \cdot Z^*_{o-o} \tag{4.46}$$

where

$$Y^*_{in-sc} = Y^*_{in-o} + \frac{T^*_{ji-o} G^*_{io-o}}{Z^*_{o-o}}$$

is equal to open loop input admittance Y^*_{in-o} of the converter under the conditions that the converter output voltage is nulled [28]

$$G'_{co} = \frac{1 + Z^*_{o-f} Y^*_{in-\infty}}{1 + Z^*_{o-f} Y^*_{in-o}} \cdot G^*_{co} \tag{4.47}$$

Loop Gain Analysis

The unterminated output voltage loop $L_g^*(s)$ is defined in (4.48). The converter dynamics is related to the control bandwidth (i.e., the frequency range, where the magnitude of $L_g^*(s) \geq 1$), and to the phase margin (i.e. how close the phase is to -180°). Instability occurs when $\left|L_g^*(s)\right| = 1$ and $\angle L_g^*(s) = -180°$.

$$L_g^*(s) = G_a G_{cc}(s) G_{co}^*(s) \tag{4.48}$$

It is obvious according to (4.48) that the changes in the control-to-output transfer function G_{co}^* would affect directly the dynamical performance through the loop gain. The input filter effect on the converter dynamics can be considered according to (4.44) and (4.48) as shown in (4.50), where $L_g^*(s)$ is the original loop gain, and $L_g'(s)$ the affected loop gain.

$$L_g'(s) = G_a G_{cc}(s) G_{co}'(s) \tag{4.49}$$

$$L_g'(s) = \frac{1 + Z_{o-f}^* Y_{in-\infty}}{1 + Z_{o-f}^* Y_{in-o}^*} \cdot L_g^*(s) \tag{4.50}$$

It was shown that $Y_{in-\infty}^*$ would stay intact even if peak-current or average-current-mode control are applied, i.e., it may be expressed as a function of the direct-duty ratio or voltage-mode control transfer functions (4.51) giving naturally the same symbolic values as stated in [12] and [17], where the subscript "v" denotes the VM nature. These observations may be obvious due to the nature of $Y_{in-\infty}$. This also means that the observed differences in dynamical behavior of a converter under different control mode may be addressed to the behavior of the open-loop input admittance Y_{in-o} [35].

$$Y_{in-\infty}^* = Y_{in-o_v}^* - \frac{G_{ci_v}^* G_{io-o_v}^*}{G_{co_v}^*} \tag{4.51}$$

If the load is assumed to be purely resistive R and the effect of the circuit parasitic elements is ignored, then $Y_{in-\infty}$ as defined in (2.44) in Chapter 2 can be expressed as follows

$$Y_{in-\infty} = -\frac{D^2}{R} \tag{4.52}$$

which coincides with the result already obtained in (4.37), (i.e. the DC gain of $Y_{in-\infty}$ is the inverse of the negative incremental resistor).

Affected Control-to-Output Transfer Function

It has been proved earlier that the changes in the control-to-output function G_{co}^* affects directly on the dynamical performance through the loop gain. The interaction theory may be further developed in the case of the control-to-output transfer function for VMC and PCMC in order to obtain more unified results for the basic converters.

The analysis of input-filter interactions in a PCM controlled converter has proven to be difficult [28, 61]. It has been noticed that the same design rules developed to VM controlled converters may not hold in the case of a PCM controlled converter [61] but no justifications were given. This turned out later to be the consequence of the behavior of of the line-to-output transfer function G_{io-o} [65].

By studying the set of equations in (4.42) - (4.44) it is easy to conclude that the effect of input filter may be insignificant if G_{io-o} is very small as in case of PCM controlled buck converter [65]. From set of equations in (2.69)-(2.74), and Table (2.4), we can conclude that G_{io-o} of a boost converter may not be very small and cannot be either nullified by means of compensation. Therefore, the result can not be generalized.

If replacing the PCMC transfer functions in (4.42) - (4.44) with the corresponding unified transfer functions of (2.69)-(2.74), we get the affected PCMC control-to-output transfer function expressed in (4.53)

$$G^*_{co} = \frac{1 + Z^*_{o-f} \cdot (Y_{in-o_v} - \frac{G_{io-o_v} G_{ci_v}}{G_{co_v}})}{1 + \frac{Z^*_{o-f}}{Z_{in-o}}} \cdot G_{co} \tag{4.53}$$

This expression shows that the numerator of the coefficient altering the original control-to-output transfer function will remain the same as in VMC. However, the reduction the input filter interactions may be directed only to the behavior of the open-loop input impedance. It is well known that the PCMC transfer functions do not exhibit resonant like behavior because the roots of their characteristic equation are well separated [28, 73]. Therefore, the input filter designed for a VM controlled converter will have more margins, when the same filter is used for a PCM controlled converter.

Minor Loop gain

The condition for system stability in presence of the input filter can be determined by the following argument. In the absence of an input filter, the equation (2.40) shows that two system properties, G^*_{io-c} and Z^*_{o-c}, contain the factor $1/\big(1 + L^*_g(s)\big)$. For stability the term $1 + L^*_g(s)$, must not have any roots in the right half-plane. This is equivalent to saying that the loop gain $L^*_g(s)$ must satisfy the Nyquist stability criterion.

In presence of an input filter, the equation (4.45) shows that the two modified system properties, G'_{io-c} and Z'_{o-c}, contain the factor $1/\left(1 + Z^*_{o-f}/Z^*_{in-c}\right)$. By analogy, however, the ratio $\frac{Z^*_{o-f}}{Z^*_{in-c}}$ may be identified as a "minor loop gain" $L_m(s)$, and for system stability $1 + L_m(s)$ must not have any roots in the right half-plane. This is equivalent to saying that the minor loop gain $L_m(s)$ must also satisfy the Nyquist stability criterion . From (2.42) the minor loop gain can be expressed as

$$L_m(s) \equiv \frac{Z^*_{o-f}}{Z^*_{in-c}} = \frac{Z^*_{o-f}}{Z^*_{in-o}} \cdot \frac{1}{1 + L^*_g(s)} + \frac{Z^*_{o-f}}{Z^*_{in-\infty}} \cdot \frac{L^*_g(s)}{1 + L^*_g(s)} \tag{4.54}$$

Even though the formal requirement for system stability is that the minor loop gain $L_m(s)$ satisfies the Nyquist criterion, a sufficient but usually more than necessary condition is that

$$|L_m(s)| = \left| \frac{Z^*_{o-f}}{Z^*_{in-c}} \right| \ll 1 \tag{4.55}$$

We can conclude from (4.54) that if the converter closed-loop input impedance Z^*_{in-c} were always positive, as would be the case, for example, for a linear dissipative converter, the Nyquist stability criterion for minor loop gain $L_m(s)$ would automatically be satisfied, and instability could not occur as a result of the addition of an input filter. Unfortunately this is not always the case for switching-mode converters since Z^*_{in-c} can be negative as already discussed, the Nyquist stability criterion set forth in (4.55) is not trivial; because the the

requirement that $\left|Z^*_{o-f}\right| < \left|Z^*_{in-\infty}\right|$, seems to be only a partial requirement for stability since from (4.54) we can see that $|L_m(s)| < 1$ is ensured only at low frequencies (i.e. at $\left|L^*_g(s)\right| \gg 1$).

Impedance Inequalities Constraint

Inspection of loop gain in (4.50) and minor loop gain in (4.54) shows that the same factor involving Z^*_{o-f} are contained in both equations. However, if Z^*_{o-f} constrained so that

$$\left|\frac{Z^*_{o-f}}{Z^*_{in-\infty}}\right| \ll 1 \tag{4.56}$$

and

$$\left|\frac{Z^*_{o-f}}{Z^*_{in-o}}\right| \ll 1 \tag{4.57}$$

these conditions ensure that the loop gain is essentially unaffected by addition of the input filter, $L'_g(s) \approx L^*_g(s)$.

Also the same inequalities automatically implies $|L_m(s)| = \left|Z^*_{o-f}\Big/ Z^*_{in-c}\right| \ll 1$, by (4.54), which in turn ensures system stability, and also that the control-to-output transfer function is essentially unaffected, by (4.47), $G'_{co} \approx G^*_{co}$.

The line-to-output transfer function in (4.45) is naturally always affected by G^*_{io-f} but its behavior is more deterministic if also (4.55) is valid. If the input filter output impedance Z^*_{o-f} also satisfies the inequality

$$\left|\frac{Z^*_{o-f}}{Z^*_{in-sc}}\right| \ll 1 \tag{4.58}$$

then the converter closed-loop output impedance will be essentially unaffected by addition of the input filter, (i.e. $Z'_{o-c} \approx Z^*_{o-c}$).

The above statements constitute the essential theoretical results of the investigation, and lead to the formulation of a procedure for practical application of VM controlled converters.

Example 4.2

To demonstrate the input filter effect on the performance of the converter, the VM and PCM controlled buck converter will be analyzed. The circuit parameters for buck converters are given in Table 3.1. Five input filters of a single section type are considered and their parameters are shown in Table 4.2.

VM Control

The behavior of the open-loop and closed-loop input impedances under VM control is shown in Fig. 4.24 compared to the LC-filter output impedances. The design criteria presented in [12] is satisfied in case of Filter 1, i.e., $\left|Z^*_{o-f}\right| \ll \left|Z^*_{in-c}\right|$, but unfortunately it is clearly violated for the other filters. The reason is, that the resonant frequency of Filter 1 is placed below the resonant frequency of output averaging filter f_f. If the LC-filter resonant frequency f_o would be placed at the frequencies, where the closed-loop input impedance has phase -180°, NRO might take place.

Table 4.2: Filter circuits parameters.

Filter	L_F	C_F	r_{LF}	r_{CF}
F_1	600 μH	450 μF	180 mΩ	60 mΩ
F_2	540 μH	220 μF	90 mΩ	20 mΩ
F_3	500 μH	80 μF	70 mΩ	15 mΩ
F_4	440 μH	45 μF	60 mΩ	10 mΩ
F_5	200 μH	20 μF	50 mΩ	10 mΩ

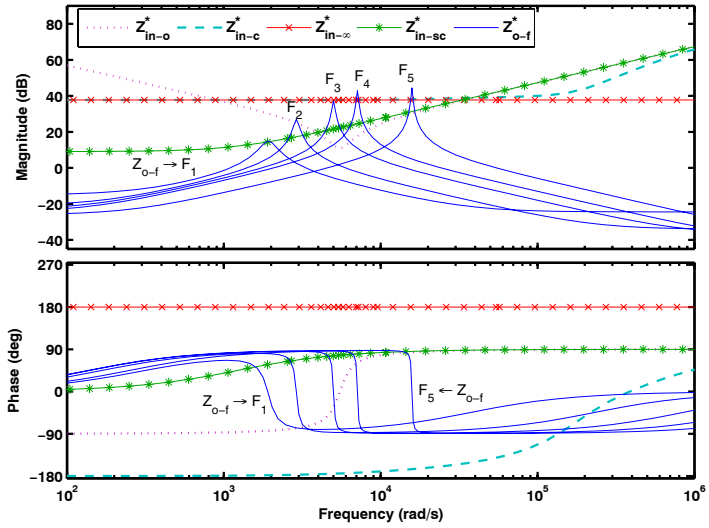


Figure 4.24: Open-loop (dotted line) and closed-loop (dashed line) input impedance under VM control vs. different LC-filter output impedances.

The practical solution is usually to place the resonant frequency of LC-filter below rather than above the resonant frequency of output averaging filter, so that the two conditions of (4.56) and (4.57) reduce simply to the single condition

$$\left|Z^*_{o-f}\right| \ll \left|Z^*_{in-o}\right| \tag{4.59}$$

since, it was noticed that $\left|Z^*_{in-o}\right|$ is always equal to or less than $\left|Z^*_{in-\infty}\right|$ for frequencies up to and beyond the chosen $f_o < f_f$.

The affected loop gains are shown in Fig. 4.25. Filter 1 alters the loop gain only slightly and is not a threat when considering the performance or stability of the converter. Although Filter 2 has noticeable effect on the loop gain, it does not degrade the bandwidth, gain margin nor the phase margin, and does not cause instability. However, the resonance peak affects

the closed-loop audio susceptibility and output impedance characteristics. Furthermore, small changes in the output impedance of the filter can cause serious effects on the loop gain, and consequently, on the performance of the converter.

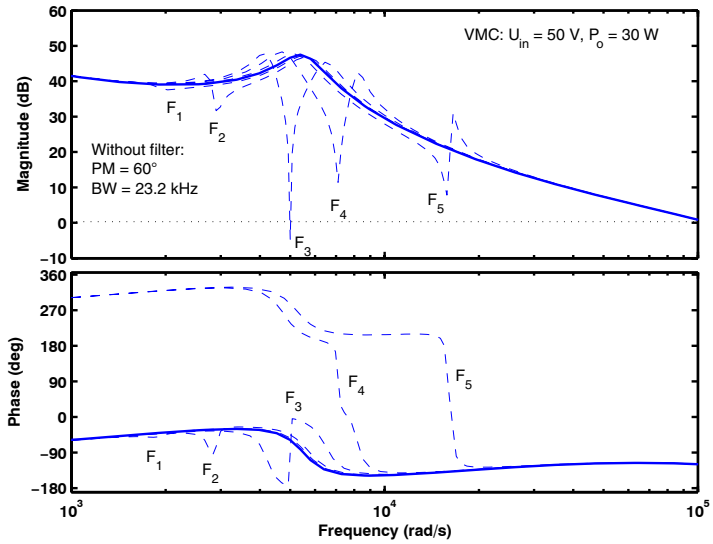


Figure 4.25: The original (solid line) and affected (dashed line) loop gain under CCM-VM control.

Filter 3 affects the loop gain severely by causing a deep and sharp peak that reduces the control bandwidth (from 23 kHz to 0.8 kHz) and phase margin (from 60° to 42.7°). The converter is still stable but its performance is severely deteriorated as shown in Fig. 4.27.

In the cases of filters 4 and 5, special care should be taken because $\left|Z^*_{o-f}\right| > \left|Z^*_{in-c}\right|$. When considering Filter 4 and 5, instability can be concluded by noticing that the peaking causes the phase curve to cross 180° at the point where the gain curve is still above 0 dB.

The instability caused by the input filter can be deduced from Nyquist plot of the minor loop gain $L_m(s)$ as shown in Fig. 4.26. It can be seen that the instability can be concluded for the case of Filter 4 and 5 by encirclement of the (-1,0) point on Nyquist plot of $L_m(s)$. In case of Filter 1 and 2, it is obvious that they meet the specification, and therefore the Nyquist plots of the minor loop gains avoid the forbidden region and the converter is stable as shown in 4.26. For the Filter 3 the converter is still stable but its performance is severely deteriorated because the minor loop violates the forbidden region.

The responses of the output voltage (Fig. 4.27; upper) and the filter-capacitor voltage (Fig. 4.27; lower) in case of Filter 3 for a load change show that the system is stable. A change of 10% to 90% of the nominal load power of 30 W at the input voltage of 50 V under VM control were used.

The filter output impedances together with the closed-loop and open-loop input impedances of VMC-DCM buck converter are also plotted in Fig. 4.28. The output impedances for filters 1,2 and 3 stay well below the closed-loop input impedance. Filter 4 and 5 are very close to cause the interaction. The original loop gain and the affected loop gains are shown in

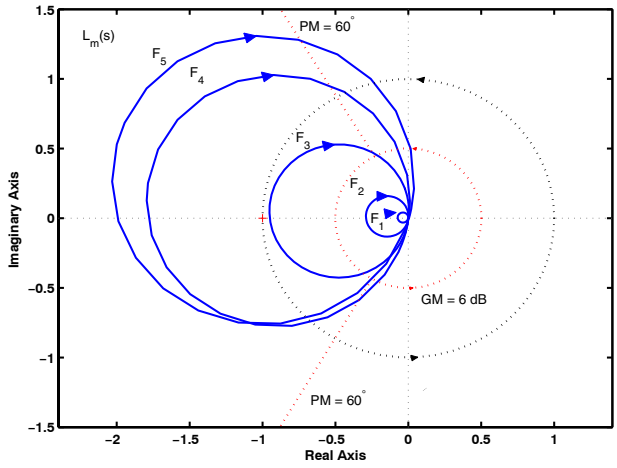


Figure 4.26: Nyquist Plots of the minor loop gains at different input filters under CCM-VM control

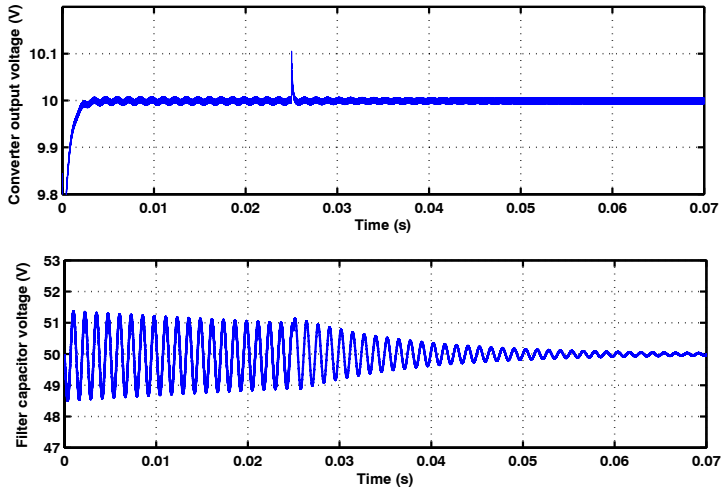


Figure 4.27: Output-voltage (upper) and LC-Filter 3 capacitor-voltage (lower) responses under CCM-VM control to a load step change.

Fig. 4.29. The loop gain reveals the converter is still stable even though the impedances are close to each other and there is some peaks.

The Nyquist plot of the minor loop gain $L_m(s)$ is shown in Fig. 4.30. The minor loop gains for all filters do not violate the forbidden region and the converter is stable.

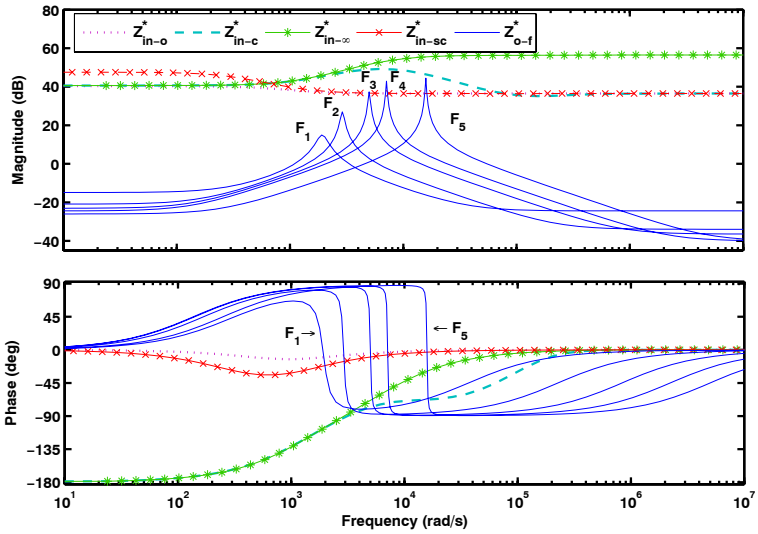


Figure 4.28: Open-loop (dotted line) and closed-loop (dashed line) input impedance under a DCM-VM control vs. different LC-filter output impedances.

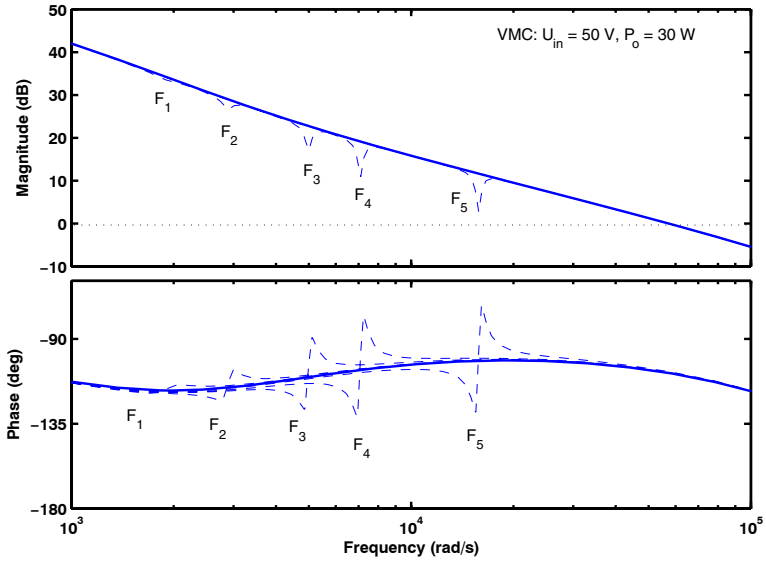


Figure 4.29: Original and affected loop gains under a DCM-VCM control.

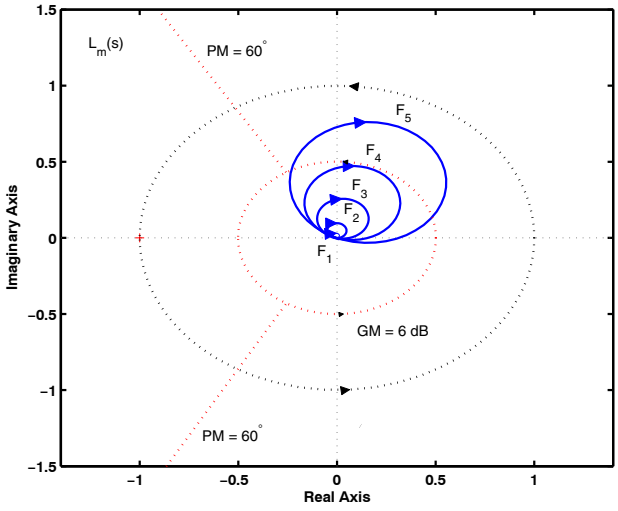


Figure 4.30: Nyquist Plots of the minor loop gains at different input filters under DCM-VM control

PCM Control

Similarly to the VMC, the input filter interaction will be investigated for the peak-current-mode-controlled buck converter, Fig. 3.20.

The open-loop and closed-loop input impedances of the converter and the output impedances of the filters are shown in Fig. 4.31, and the original loop gain and the affected loop gains are shown in Fig. 4.32, respectively.

The loop gain stays almost intact even though the impedances are close to each other and even overlap each other. However, the analysis of minor loop gains in Fig. 4.33 leads to the conclusion that filters 4 and 5 are unstable, the others are stable. The reason for unchanged the loop gain is that the line-to-output transfer function or audiosusceptibility G^*_{io-o} of a buck converter is small and can be totally nullified when using optimal compensation. According to this, it is easy to conclude that the effect of the input filter on output dynamics of the converter is negligible.

It is quite evident that the behavior of the input impedance explains the differences in the input-filter interactions between VM and PCM control.

The design criteria developed in [12, 17] are valid in both of the control modes but the lack of resonant peaking in input impedance under PCM control enables the use of somewhat 'smaller' input filter compared to VM control.

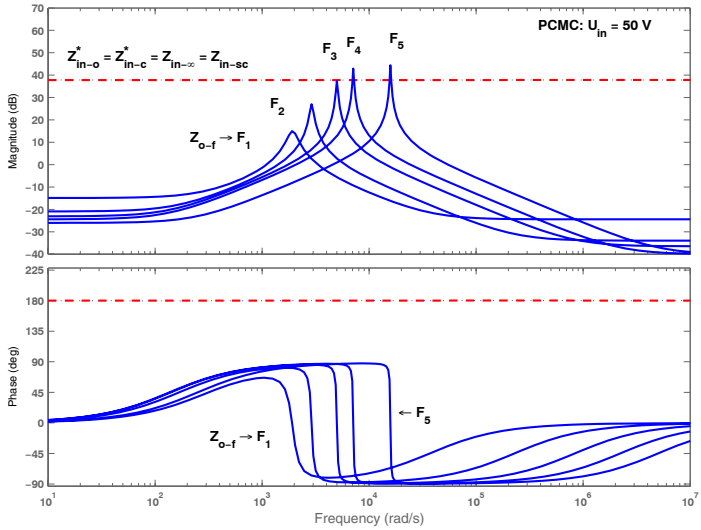


Figure 4.31: Input impedance of a PCM controlled buck converter (dashed lines) vs. LC-filter output impedances (solid lines).

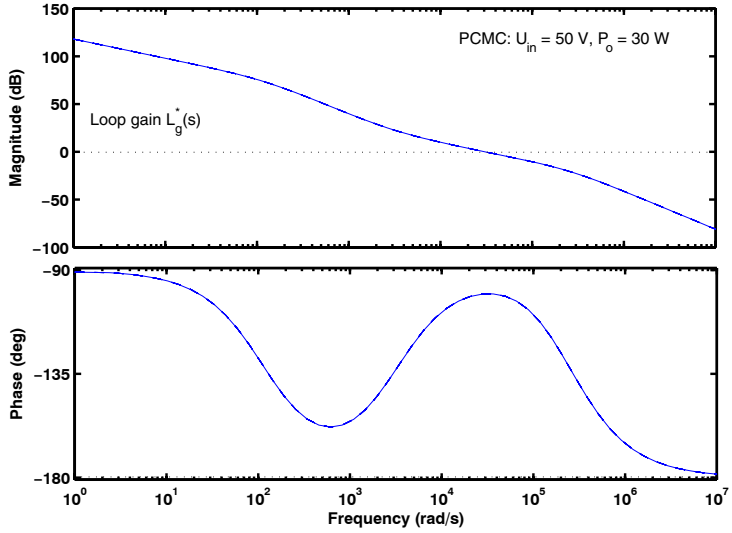


Figure 4.32: Original and affected loop gains under a PCM control.

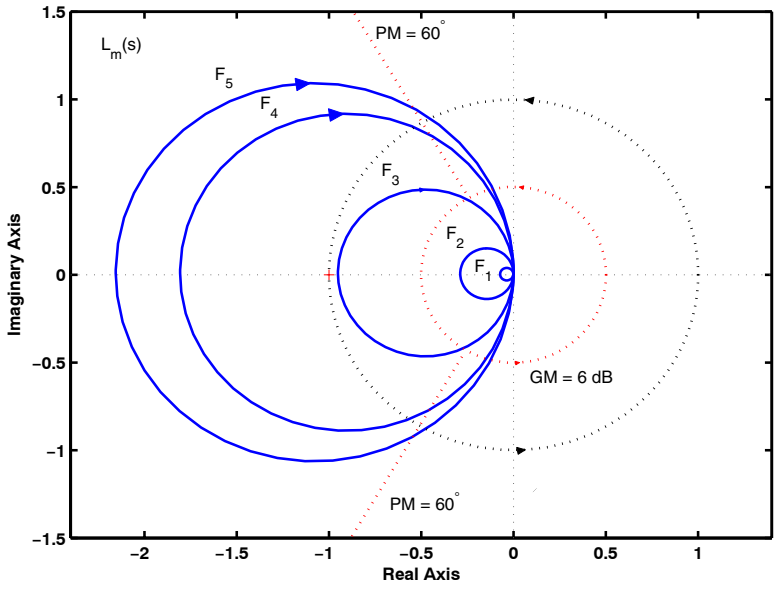


Figure 4.33: Nyquist Plots of the minor loop gains at different input filters under PCM control.

Chapter 5

Dynamics Analysis of Paralleled DC-DC Converters

Paralleling DC-DC switching converter modules (Fig. 5.1) offers several advantages over a single centralized power supply, such as expandability of output power, high reliability, design standardization, and ease of maintenance and repair. Most of the motivations stated above put more interest in the paralleled operation of DC-DC converter modules [21, 88, 89, 90].

The control objective of a single switched-mode DC-DC converter is to maintain the output voltage close to the reference. In the case of multimodule system, the control objective is enriched with the demand of keeping the power distribution between the units close to a specified pattern. However, paralleled DC-DC converters require an explicit current-sharing mechanism to ensure even distribution of current and thermal stresses among the modules and to prevent operation of one or more modules in a current-limiting mode. Without a current-sharing mechanism, even small imbalances in modules' output voltages can cause the output currents to be significantly different [19, 21, 88, 89]. Therefore, it is necessary to design a controller that can regulate the output voltage and achieve balanced current distribution.

In the past two decades, numerous approaches for paralleling DC-DC switching converters, with varying degrees complexity and current-sharing performance, have been proposed [21, 88, 89, 91]. In general, the paralleling methods are classified either based on their connection styles, current-sharing control structures or feedback functions. In [92, 93], some forms of classifications and comparisons have been given for paralleling schemes. In [92], the classification has been made based on the voltage control loop configurations. Three different paralleling schemes for multimodule converters were proposed. For each paralleling scheme, merits and limitations were addressed. In [93], a classification has been made based on the type of current-sharing method, namely, passive method, (i.e., droop method), and active current-sharing methods, i.e., the democratic scheme and master-slave scheme. The classification is thus basically a systematic collection of existing schemes.

An interesting work has been presented in [94] describing a classification of paralleling schemes for DC-DC converters from a circuit theoretic viewpoint. In the proposed classification, the converters are seen as current sources or voltage sources, and their connection possibilities, as constrained by Kirchhoff's laws, are classified systematically into three basic types.

Although the benefits and dc characteristics of multimodule DC-DC converters are well known, issues involved with a systematic derivation of current-sharing loop gain, current-sharing controller design and the system stability analysis of the paralleling scheme are not treated consistently in the existing literature.

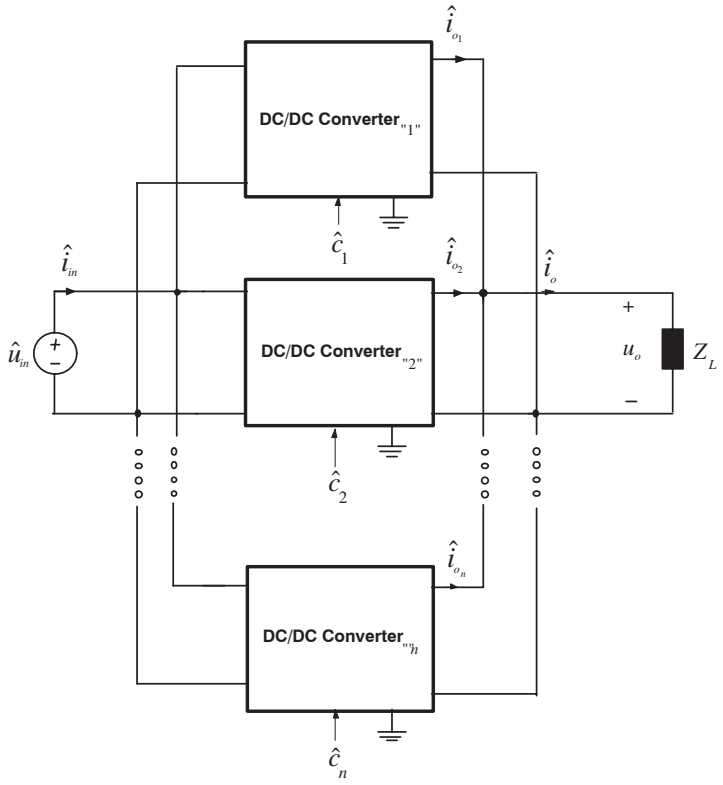


Figure 5.1: n paralleled converters.

In this chapter, a systematic modeling of parallelling DC-DC converters based on small-signal two-port network representation and circuit theory is presented. The small-signal model of paralleled converters with an individual voltage loop and current-sharing master-slave control (MSC) is developed. A robust current-sharing controller, which achieves balanced current distribution of the converters and ensures stability and performance of system, is designed using the QFT approach and verified by Matlab™/Simulink™ simulation.

5.1 General Constraints on Paralleling DC-DC Converters

In general, we may simply and generically describe the switching DC-DC converters in terms of their regulation modes. However, if the output voltage is required to be regulated, the converters are called Voltage-Output Converters, and if the output current is regulated, they are called Current-Output Converters [95]. Thus, an appropriate model for a converter which is seen at output terminals, is either a voltage source or a current source.

An appropriate modeling of paralleling scheme requires a firm understanding of fundamental circuit theory constraints which must form the basis for any parallel connection styles.

From the basic circuit theory, we know that independent sources can be connected in parallel under only two possible ways as shown in Fig. 5.2. Firstly, only one of them can

be an independent voltage source, while the others must be current sources, as shown in Fig. 5.2(a). Secondly, all parallel branches are current sources, as shown in Fig. 5.2(b). This means that two independent voltage sources are not permitted to be connected in parallel [96, 94]. Although the equivalent converters i.e., voltage and current sources are not independent in practice but are control-dependent sources, the aforementioned two basic parallel constraints still hold.

The scheme with one voltage-output converter connected in parallel with current-output converters and the associated current-sharing control problem will be the main subjects of discussion in this chapter.

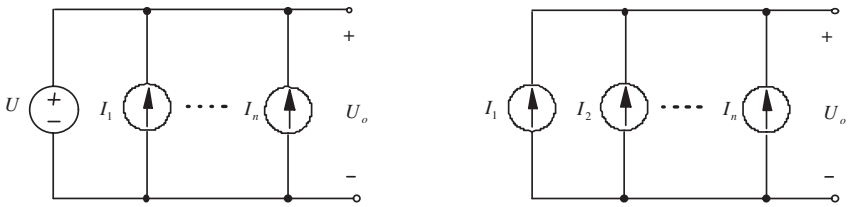


Figure 5.2: Structures for paralleling ideal independent sources.

5.1.1 Current-Output Converters

In the output-voltage converters the voltage output is regulated and, accordingly, the output current is regulated in the output-current converters. A main application of these converters is a DPA system having a back-up battery connected in parallel [95]. The basic configuration of the current-output is shown in Fig. 5.3. Unlike the voltage-output converters, the load system in the current-output converters is composed of an ideal voltage source e_o in series with the load impedance Z_L. The dynamical issues of the current-output converters have been studied in [95]. It was shown that, the dynamical profile of the current-output converters can be easily derived from the corresponding voltage-output converter profile by applying duality. This can be done by changing the Thevenin's equivalent output port to the Norton's port and replacing the current-sink load with a pure voltage source. In voltage-output converters, the modified g-parameters are used to represent the two-port model, but we use the modified y-parameters [96, 95]. The general form of y-parameters for current-output converters used to describe the input and output dynamics of the current-output converters is

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Y^*_{in-o_i} & T^*_{ji-o_i} & G^*_{ci_i} \\ G^*_{io-o_i} & -Y^*_{o-o_i} & G^*_{co_i} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_o \\ \hat{c}_i \end{bmatrix} \tag{5.1}$$

where the general control variable is denoted by c_i, and the basic open-loop transfer functions (denoted by "i") are as follows

$$Y^*_{in-o_i} = Y^*_{in-o} + \frac{G^*_{io-o}T^*_{ji-o}}{Z^*_{o-o}}, \quad T^*_{ji-o_i} = -\frac{T^*_{ji-o}}{Z^*_{o-o}}$$

$$G^*_{ci_i} = G^*_{ci} + \frac{G^*_{co}T^*_{ji-o}}{Z^*_{o-o}}, \quad G^*_{io-o_i} = \frac{G^*_{io-o}}{Z^*_{o-o}}$$

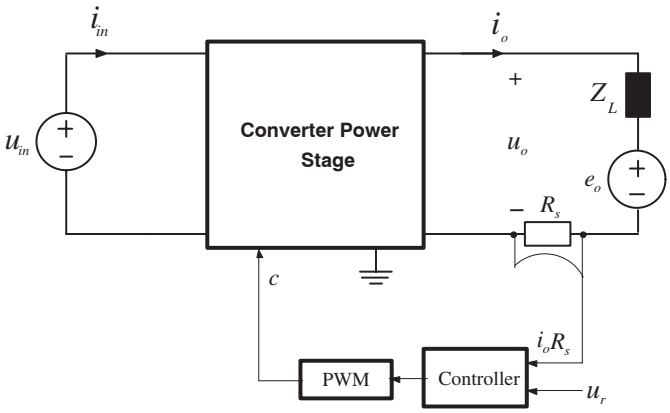


Figure 5.3: Basic configuration of current-output converter.

$$Y^*_{o-o_i} = \frac{1}{Z^*_{o-o}}, \quad G^*_{co_i} = \frac{G^*_{co}}{Z^*_{o-o}}$$

The resulting two-port model is shown in Fig. 5.4. The closed-loop transfer functions of the current-output converters can be represented as

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Y^*_{in-c_i} & T^*_{ji-c_i} \\ G^*_{io-c_i} & -Y^*_{o-c_i} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{u}_o \end{bmatrix} \tag{5.2}$$

$$Y^*_{in-c_i} = Y^*_{in-o_i} - \frac{G^*_{io-o_i}T^*_{ji-o_i}}{G^*_{co_i}} \cdot \frac{L^*_{co}}{1+L^*_{co}}, \quad T^*_{ji-c_i} = T^*_{ji-o_i} - \frac{Y^*_{o-o_i}G^*_{ci_i}}{G^*_{co_i}} \cdot \frac{L^*_{co}}{1+L^*_{co}}$$

$$G^*_{io-c_i} = \frac{G^*_{io-o_i}}{1+L^*_{co}}, \quad Y^*_{o-c_i} = \frac{Y^*_{o-o_i}}{1+L^*_{co}}$$

where the L^*_{co} is the current-output converter loop gain

$$L^*_{co} = H_{se}G^*_{co_i}G_{c_i}G_{a_i} \tag{5.3}$$

H_{se} is the sensor gain (i.e. typically the current sensing resistor R_s), G_{c_i} is the controller transfer function and G_{a_i} is the modulator gain.

5.1.2 Equivalent Circuit Models for DC-DC Switching Converters

For control design purposes, a DC-DC converter can be represented in Thévenin equivalent circuit or Norton equivalent circuit, i.e., a dependent voltage in series with a impedance Z as shown in Fig. 5.5(a) or a dependent current source in parallel with an admittance Y as shown in Fig. 5.5(b) [96, 94]. Obviously, the Thévenin equivalent circuit is more suited for voltage-output converters whose objective is to regulate the output voltage, whereas the Norton equivalent circuit is suited for current-output converters whose objective is to regulate the output current. Generally, the voltage feedback is needed for the former case, and current feedback for the latter.

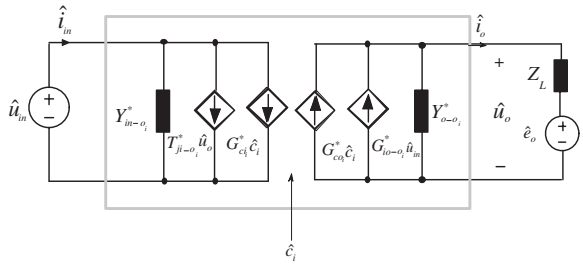
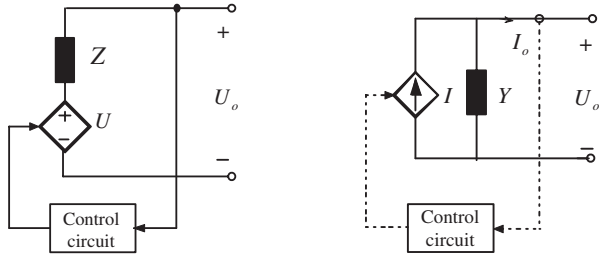


Figure 5.4: Two-port model of a current-output converter.



(a) Voltage-output converter. (b) Current-output converter.

Figure 5.5: Equivalent circuits for switching converters.

5.2 Paralleled DC-DC Converters with Master-Slave Control MSC

Due to limited tolerances in the converters' power stages and control parameters, small imbalances in modules' parameters may cause the output currents to be significantly different if special provisions are not made to distribute the load current equally among paralleled modules. This current unbalance will result in excessive thermal and device stresses on specific units and reduces the system's reliability [21]. Therefore, uniform current sharing among paralleled modules has become a primary concern.

Generally, the current sharing (CS) can be implemented using two approaches. The first one, known as a droop method [97], relies on the high output impedance of each converter to achieve load current sharing. It is simple to implement, and it doesn't require any communication between the modules. The major drawback of the droop approach is a poor load regulation, and it is not suitable for high-performance applications. The second approach, known as active current-sharing techniques [19, 98, 88, 89], is used to overcome the disadvantages of the droop method. The Master-Slave Control (MSC) technique belongs to the latter category, where one module is dedicated to be the master whose output current becomes the reference for CS loops of the remaining modules (slaves) [99].

5.2.1 Modeling of Multimodule Converters with MSC

Some performance characteristics such as system stability and transient response in the event of failure of one module are crucial for the analysis of paralleled DC-DC converter modules. As a result, to design a stable feedback control loop, one should know the exact model of the paralleled converters under study. Numerous works have been published on modeling

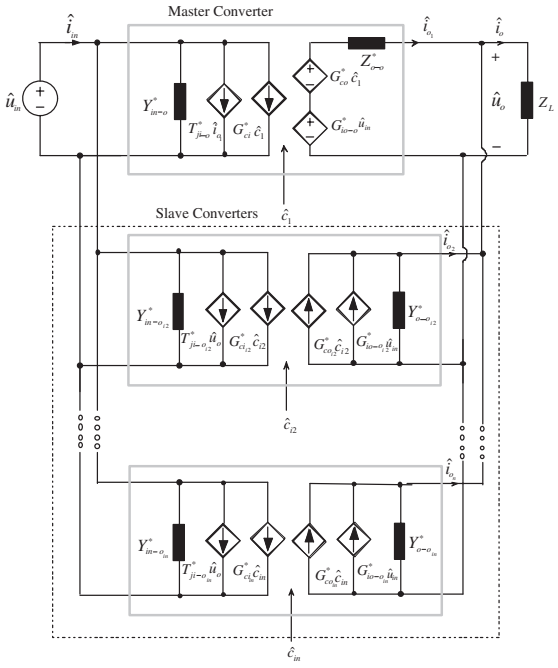


Figure 5.6: Two-port model of n parallel-buck converters.

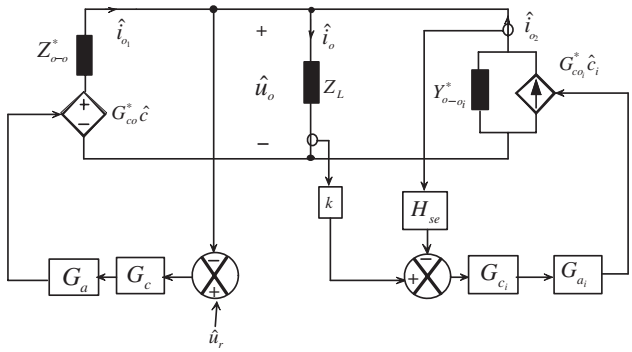
of paralleled DC-DC converters proposing a variety of methods [19, 21, 98, 88, 89, 100, 22]. A large number of these works utilized the so-called canonical equivalent circuit. However, the canonical model cannot easily be applied to other operation modes or control methods. Unlike the conventional approach, we will use the two-port network representation to model the parallel converters and to derive the current-sharing loop gain.

To illustrate the basic problem associated to modeling of parallel converters, the small-signal two-port configuration of the voltage-output converter and n current-output converters connected in parallel is shown in Fig 5.6.

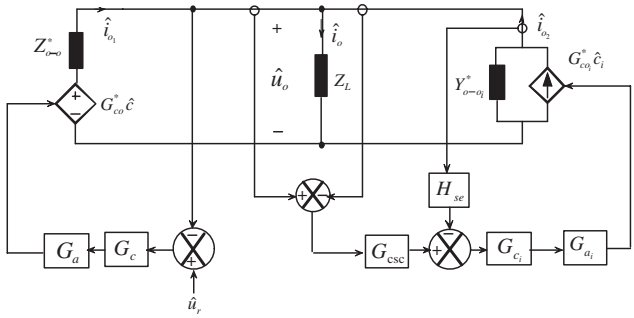
The equivalent control structure without current-sharing loop is shown in Fig. 5.7(a). There is a main voltage feedback loop, which acts on the voltage-output converter to regulate the output voltage. Other converters are current-output converters, whose purpose is to make all individual output currents share the same load current [94]. The reference current signal for each current converter is $i_o\ k$, where $k = 1/n$.

Fig. 5.7(b) shows the equivalent control structure with current-sharing loop. A main voltage feedback loop is needed to control the voltage-output converter module. The current control signal for the current-output converters modules will be derived from the voltage source branch. This control signal is then compared with the individual current of the $n-1$ converters to achieve current sharing. The current-sharing control can be done using master-slave current-sharing approach, where the voltage-output converter serves as master and the current-output converters are the slaves whose currents are adjusted to follow the master.

Note that, the above figures show only two converters, but the analysis is general and can be applied for n number of converters.



(a) Without current-sharing loop.



(b) With MS current-sharing loop.

Figure 5.7: Control structures for parallelling converters.

Current-sharing loop gain

The derivations of the module admittances and current-sharing loop gain can be essentially simplified by applying a voltage or current source excitation to the system output. First, a current source excitation is applied at the output of master module as shown in Fig. 5.8(a), and the unterminated output impedance will be derived. Then, a voltage source excitation is applied at the output of slave module as shown in Fig. 5.8(b), and the unterminated output impedance and current-sharing loop gain will be derived accordingly.

For a stable system, stability of the each individual module under source disturbance is required. The individual module stability assessment starts from the master converter. The master output voltage is

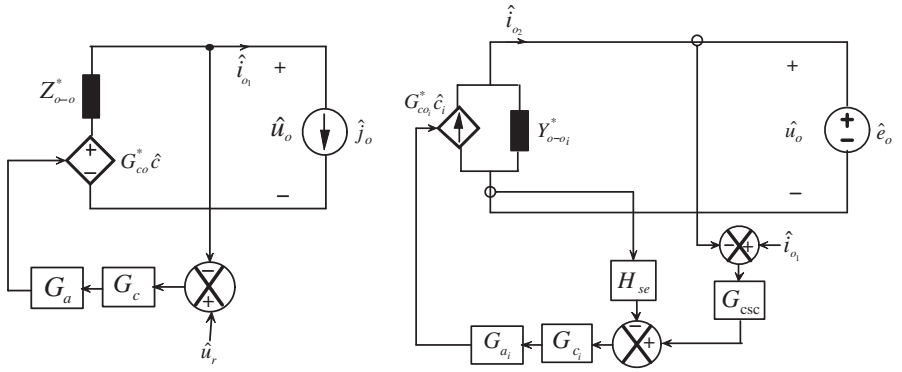
$$\hat{u}_o = \hat{i}_{o1} Z^*_{o-o} + G^*_{co}\hat{c} \tag{5.4}$$

The control signal $\hat{c}$ is given as follows

$$\hat{c} = (-\hat{u}_o + \hat{u}_r)\, G_c G_a \tag{5.5}$$

Inserting (5.5) into (5.4) yields

$$\hat{u}_o = \frac{Z^*_{o-o}}{1 + G^*_{co} G_c G_a}\hat{i}_{o1} + \frac{G^*_{co} G_c G_a}{1 + G^*_{co} G_c G_a}\hat{u}_r \tag{5.6}$$



(a) Master module. (b) Slave module.

Figure 5.8: Small-signal model with source disturbances applied.

If the reference signal $\hat{u}_r = 0$, then, the master closed-loop output impedance is

$$Z^*_{o-c} = \left.\frac{\hat{u}_o}{\hat{i}_{o1}}\right|_{\hat{u}_r=0} = \frac{Z^*_{o-o}}{1+L^*_g} \tag{5.7}$$

where $L^*_g = G^*_{co}G_cG_a$, is unterminated voltage loop gain.

The small-signal block diagram of a slave with the applied disturbance source is shown in the Fig. 5.8(b). The measured slave output current is compared with the master current which is represented as:

$$\hat{i}_{o2} = \hat{u}_o Y^*_{o-o_i} + G^*_{co_i}\hat{c}_i \tag{5.8}$$

The control signal $\hat{c}_i$ is given as

$$\hat{c}_i = \left(-\hat{i}_{o2}H_{se} + G_{\text{csc}}(\hat{i}_{o1} - \hat{i}_{o2})\right) G_{c_i}G_{a_i} \tag{5.9}$$

Inserting (5.9) into (5.8) we get

$$\hat{i}_{o2} = \hat{u}_o Y^*_{o-o_i} - \hat{i}_{o2}G^*_{co_i}G_{c_i}G_{a_i}H_{se} + G^*_{co_i}G_{c_i}G_{a_i}G_{\text{csc}}(\hat{i}_{o1} - \hat{i}_{o2}) \tag{5.10}$$

The master output current $\hat{i}_{o_1}$ is

$$\hat{i}_{o1} = Y^*_{o-c}\hat{u}_o \tag{5.11}$$

From (5.10) and (5.11), the expression for a slave output admittance can be derived as follows:

$$Y^*_{o-\text{csc}} = \frac{\hat{i}_{o2}}{\hat{u}_o} = \frac{Y^*_{o-o_i} + Y^*_{o-c}L^*_{\text{csc}}}{1 + L^*_{co} + L^*_{\text{csc}}} \tag{5.12}$$

where $L^*_{co} = G^*_{co_i}G_{c_i}G_{a_i}H_{se}$, is the unterminated current loop gain and

$$L^*_{\text{csc}} = G^*_{co_i}G_{c_i}G_{\text{csc}}G_{a_i} \tag{5.13}$$

is unterminated current-sharing loop gain.

The term L^*_{csc} is present in both nominator and denominator of (5.12). This means that if the master and slave output currents are identical and cancel each other at the CS loop summing point, then, equation (5.12) will clearly reduced to the closed-loop output admittance of current-output converter.

The dynamics of current sharing in MSC are determined by studying stability of the current-share loop gain $L_{csc}(s)$. It is obvious from (5.13) that the only transfer function with the freedom of being designed, to optimize the current share dynamics is the current-share controller transfer function G_{csc}. The controller G_{c_i} is usually designed prior to the design of the current-sharing controller.

The current share controller is designed so that the current share loop gain $L_{csc}(s)$ verifies the following requirements [88]

(1) limited bandwidth of the path from Master to Slave module;

(2) adequate high gain at low frequency;

(3) sufficient robust stability margins (e.g., GM $\geq$ 6 dB and PM $\geq 60^\circ$);

5.2.2 QFT-Based Robust Controller Design

The QFT-based robust control methodology will be applied here to design a robust controller for current-output converter G_{c_i} and also for current-sharing controller G_{csc}. For design purposes, a buck converter operating in CCM is considered and the converter circuit parameters are given in Table 3.1 (Chapter 3). The desired margins for robustness are the same as in the corresponding voltage-output converters in Chapter 3. The QFT bounds are then to be used in shaping of the nominal loop transmission $L_{co_{nom}} = G_{co_{i_{nom}}} G_{c_i} G_{a_i} H_{se}$.

After applying the QFT-loop shaping for voltage-mode control, analysis shows that a pole at the origin in addition to two pole-zero pairs are able to satisfy these requirements. The resulting controller transfer function is given in (5.14), and the open-loop frequency response with this controller is illustrated in Fig. 5.9.

$$G_{c_i}(s) = \frac{5428\,(s/1211+1)\,(s/1.85\times10^4+1)}{s\,(s/1.786\times10^5+1)\,(s/5.15\times10^4+1)} \tag{5.14}$$

Analysis of the closed-loop system performance in the frequency domain shows that the worst closed-loop response magnitude (covering all uncertainty cases) is well below the specified value as illustrated in Fig. 5.10. The $L_{co}(s)$ loop gain is stable and has a bandwidth of 12.2 kHz, the phase margin of 87° with an infinite gain margin.

The current-sharing controller $G_{csc}(s)$ will be designed to satisfy robust specifications. These specifications are used to compute the frequency dependent QFT bounds, $B(\omega)$, that guide the shaping of the nominal loop transmission $L_{csc_{nom}} = G_{co_{i_{nom}}} G_{c_i} G_{\text{csc}} G_{a_i}$. The design specifications are a minimum phase margin of 60°, a minimum gain margin of 6 dB, and a minimum bandwidth frequency of 10 kHz.

The QFT-loop shaping analysis shows that gain with a pole-zero pair (i.e., lead compensator) are able to satisfy these requirements; the zero is to cancel out the pole created by inductor and its parasitic, the pole is required to attenuate a high frequency noise and the gain gives a suitable cross-over frequency. The resulting controller transfer function is given in (5.15) and the open-loop frequency response with this controller is illustrated in Fig. 5.11.

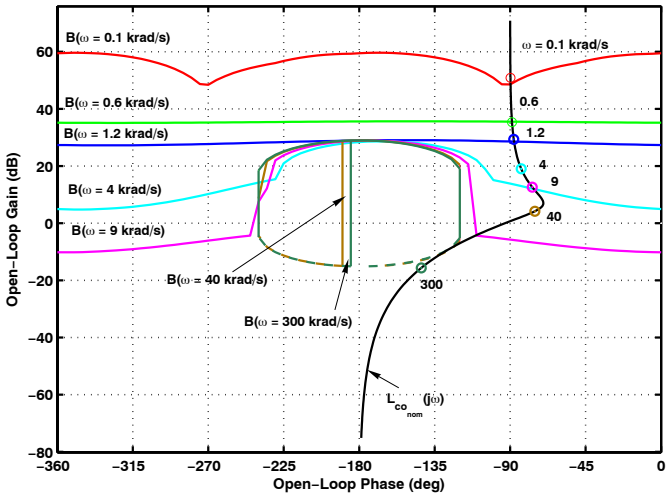


Figure 5.9: Open-loop frequency response with controller in VMC.

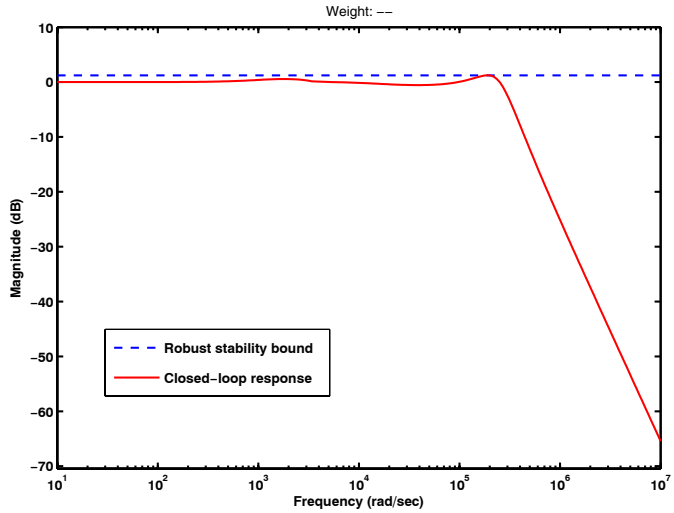


Figure 5.10: Closed-loop robust stability margins in VMC.

$$G_{\text{csc}}(s) = \frac{1181\left(s/5.856\times10^{5}+1\right)}{\left(s/1.575\times10^{8}+1\right)} \tag{5.15}$$

The closed-loop system performance analysis in the frequency domain shows that the worst closed-loop response magnitude (covering all uncertainty cases) is well below the specified value as illustrated in Fig . 5.12. The $L_{csc}(s)$ loop gain is stable and has a bandwidth of 16 kHz, the phase margin of 80° with an infinite gain margin as shown in Fig. 5.13.

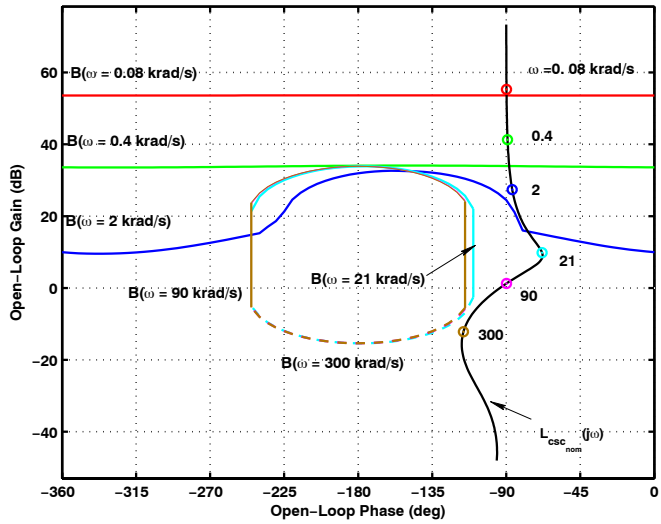


Figure 5.11: Open-loop frequency response with controller in VMC.

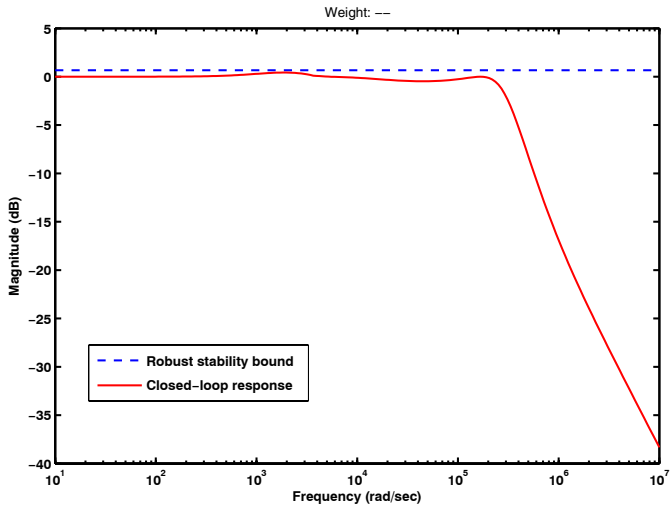


Figure 5.12: Closed-loop robust stability margins.

The Fig. 5.14 shows the plots of master and slave closed-loop output impedances. Comparison of the output impedances plots shows that the desired relationship between master and slave impedances is maintained within the CS loop bandwidth. However, the system admittance is dominated by the master admittance. This fact implies that small-signal load voltage response to the load disturbance remains approximately the same. These considerations will be confirmed by the time-domain system simulation.

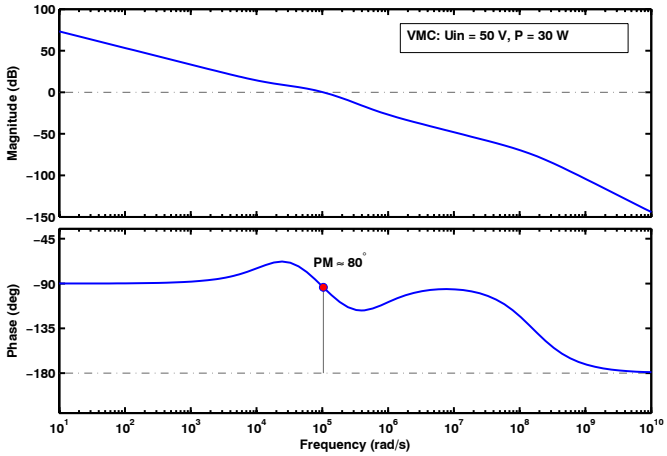


Figure 5.13: CS loop gain $L_{csc}(s)$, VMC.

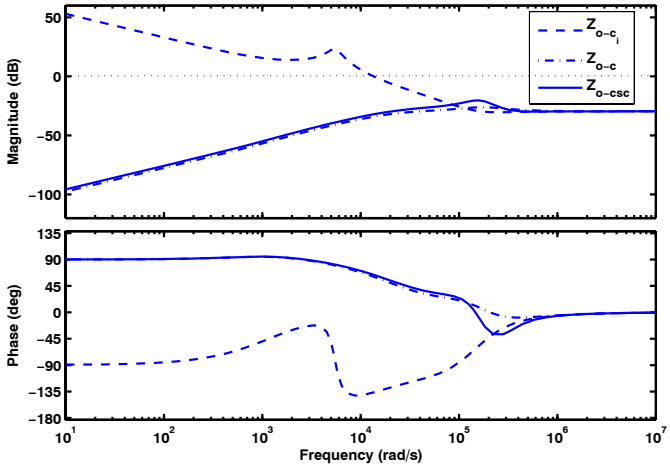


Figure 5.14: Closed-loop output impedances of VMC converter modules: slave module without current-sharing control (dashed line), master module (dash-dot line) and slave module with current-sharing control (solid line).

Since CS controller design does not depend on the number of paralleled modules, the current-sharing controller was implemented with two nonidentical buck converter modules operating in CCM. The master module has nominal parameters values which are given in Table 3.1 (Chapter 3), while the slave module deviates from the nominal design: the inductor L reduces -20% from its nominal value. In the simulations, all models are constructed using MATLAB/SIMULINK shown in Figs. A.13 - A.15 in Appendix A.1.

It is obvious from Fig 5.7(a) that the current-sharing accuracy relies on the precision of the current divider k. However, small variation of the current divider can give large current-sharing errors between the voltage-output converter and current-output converters.

To verify the proposed controllers, first the system responses (i.e., output voltage and output currents) to a load step from 90% to 10% at 0.02 s and at 0.05 s without CS control are demonstrated in Fig. 5.15. The inductor of the slave module L reduces -20% from its nominal value and the current divider k has been changed from 0.5 to 0.52. 5.15. As shown in Fig. 5.15, the output currents diverge to significantly different values while the output voltage is being regulated.

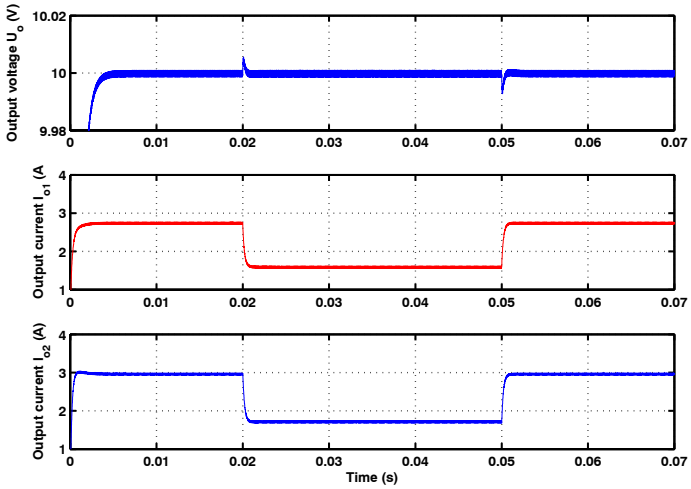


Figure 5.15: Output voltage and output current responses due to the step load change in VMC without current-sharing control; when current divider changes.

The simulation result for the system module with master-slave current-sharing control is shown in Fig. 5.16. As can be seen, satisfactory dynamic response under step load change is demonstrated. Also, the current-sharing accuracy is improved compared to the module without current-sharing control.

Similar QFT design analysis is performed in peak-current-mode control. Applying the QFT-loop shaping shows that a pole at the origin in addition to pole-zero pair should be added to satisfy the robust closed-loop specifications. The controller transfer function is given as

$$G_{c_i}(s) = \frac{4015\,(s/2152 + 1)}{s\,(s/2.5 \times 10^4 + 1)} \tag{5.16}$$

The resulting open-loop frequency response with this controller is illustrated in Fig. 5.17. It is obvious that the open-loop frequency response does not violate the stability performance requirements as depicted in Fig. 5.18.

The $L_{co}(s)$ loop gain is stable and has a bandwidth of 13.4 kHz, the phase margin of 86.4° with an infinite gain margin. However the tradeoff between system response and system stability prevails.

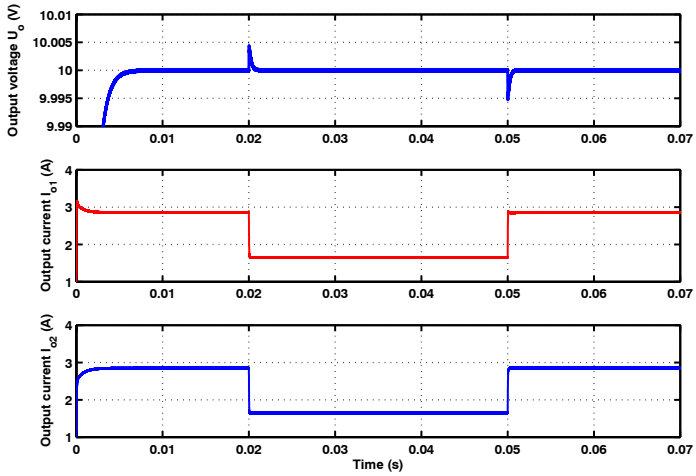


Figure 5.16: Output voltage and output current responses due to the step load change in VMC with MSC control.

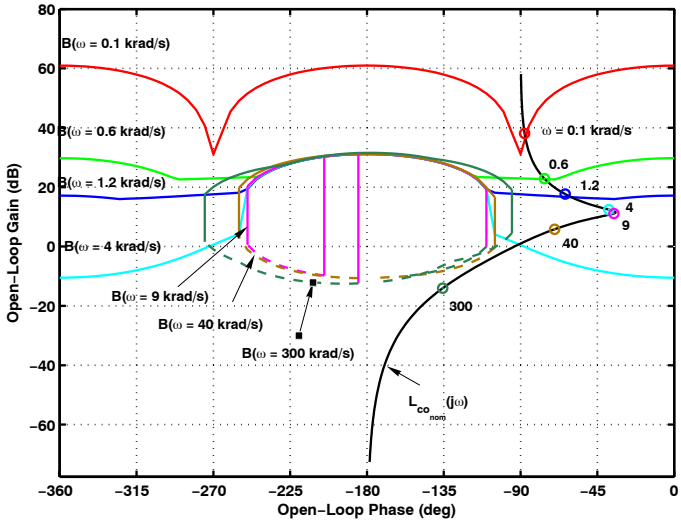


Figure 5.17: Open-loop frequency response with controller PCMC.

The QFT-based robust current-sharing controller has been deigned accordingly (Figs. 5.19 - 5.20), and the corresponding controller transfer function is

$$G_{\mathrm{csc}}(s) = \frac{1401\left(s/2.76\times10^{4}+1\right)}{(s/14.15+1)} \tag{5.17}$$

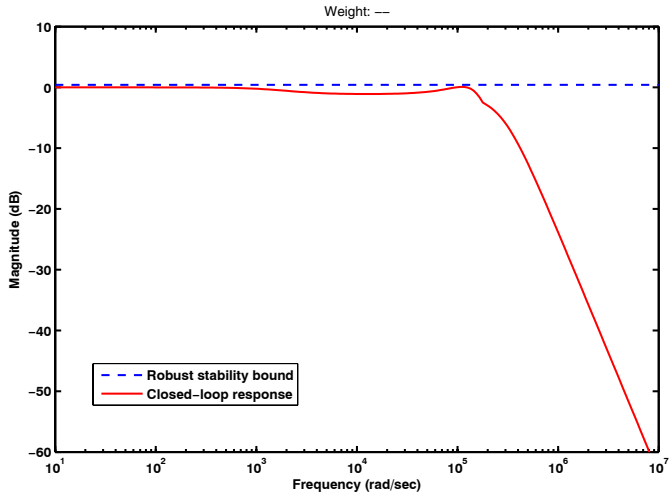


Figure 5.18: Closed-loop robust stability margins in PCMC.

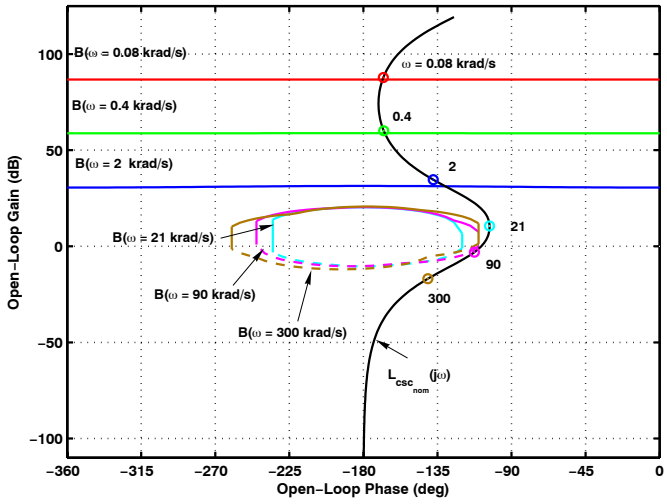


Figure 5.19: Open-loop frequency response with controller in PCMC.

Also the current-sharing loop gain $L_{csc}(s)$ is stable as shown in Fig. 5.21, and has a bandwidth of 10.4 kHz, the phase margin of 72° with an infinite gain margin.

To verify the proposed controller, the closed-loop output impedances of master and slave module with and without current-sharing control are plotted in Fig. 5.22. Comparison of the output impedances with the voltage-mode control shows that the slave module follows exactly its master at low frequency. The reason is that, as explained earlier, in VMC the controller can react only after the disturbance has propagated to the output voltage,

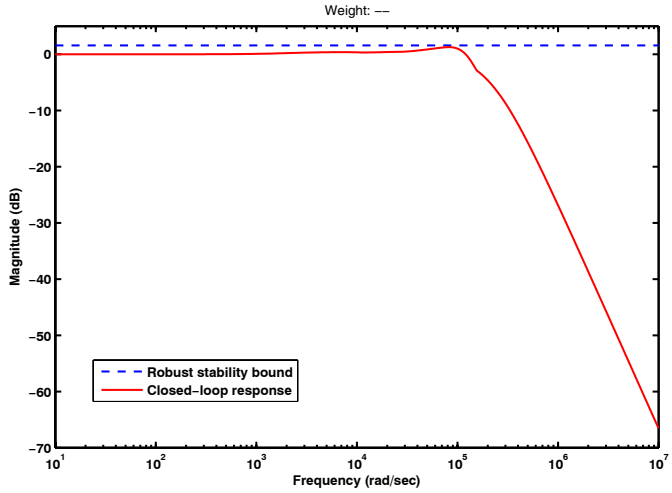


Figure 5.20: Closed-loop robust stability margins.

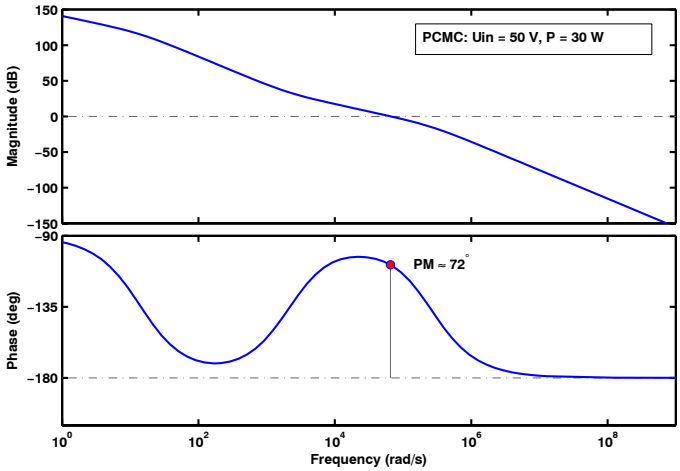


Figure 5.21: CS loop gain $L_{csc}(s)$, PCMC.

which then results in an unavoidable delay in the compensation of these disturbances. This observation will be confirmed by the time-domain system simulation.

Fig. 5.23 shows the system responses (i.e., output voltage and output currents) to a load step from 90% to 10% at 0.02 s and at 0.05 s without CS control, when the inductor of the slave module L deviates -20% from its nominal value and the current divider k deviates from 0.5 to 0.52. From Fig. 5.23, we can see that the output currents diverge to significantly different values while the output voltage is being regulated.

When master-slave current-sharing control circuit is implemented using Simulink model

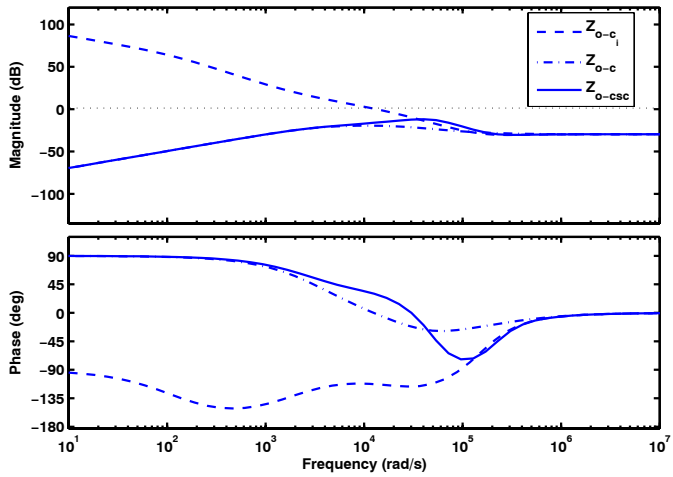


Figure 5.22: Closed-loop output impedances of PCMC converter modules: slave module without current-sharing control (dashed line), master module (dash-dot line) and slave module with current-sharing control (solid line).

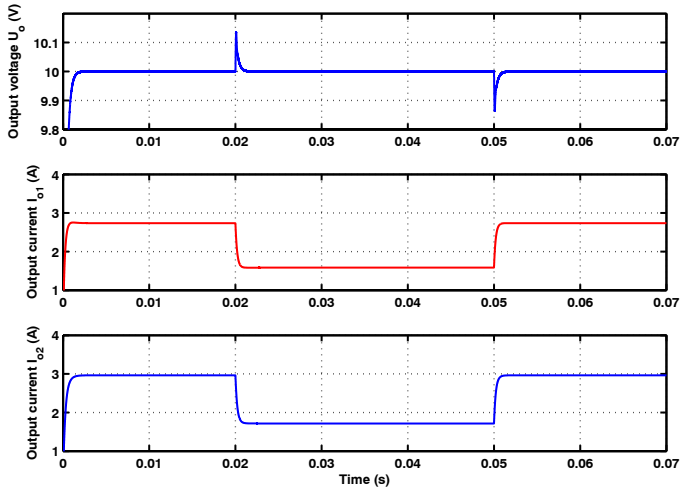


Figure 5.23: Output voltage and output current responses due to the step load change in PCMC without current-sharing control.

shown in Fig. A.15 in Appendix A.1, the difference between output currents is significantly reduced as shown in Fig. 5.24. Therefore, the time-domain behavior testifies for a proper CS loop design.

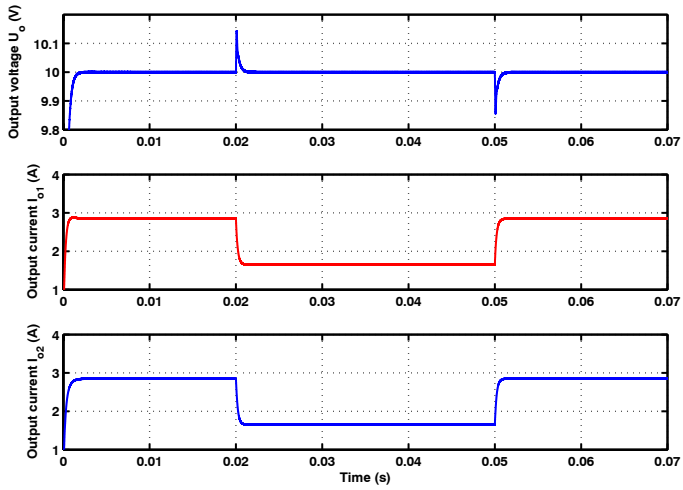


Figure 5.24: Output voltage and output current responses due to the step load change in VMC with MSC control.

From the foregoing simulation results, we may summarize the general features of the proposed parallel configuration.

The scheme is theoretically more viable as there is only one voltage-output converter paralleling with current-output converters. The dynamics of the voltage regulation thus depends on the control method being employed by the voltage regulating loop. The other current-output converters control their currents directly to achieve the desired current sharing. Thus, the current-sharing performance is generally good.

Another merit of this paralleling scheme is the insensitivity to the number of modules. Thus, once the control design is optimized for a given number of modules, the system can add or subtract an arbitrary number of modules as necessary, without compromising any performance criteria. The configuration is well suited for high-power open-ended architecture that require a flexible number of modules.

For applications where the reliability of the system is of the utmost importance, it is desirable for each module to have the full features of a complete converter. Therefore, in practice this paralleling scheme might suffer from the fault tolerance against the failure of the voltage-output converter.

Chapter 6

Conclusions

6.1 Summary

This work has addressed the issues of modeling and robust control design of DC-DC switched converters. The major accomplishments and some conclusions are given below.

The dynamic modeling of switched-mode DC-DC converters were reviewed. The fundamentals and earliest topologies-the buck, boost and buck-boost converters were analyzed and their basic operation were described. The averaged models were used to represent the dynamics of dc - dc converters. Averaged models are nonlinear and need to be linearized by using conventional linearizing methods. The model which is obtained in that way is called the small-signal model of a converter. A set of transfer functions between the inputs and outputs of the converter have been derived that characterize the dynamics of the converter in the vicinity of the operating point and up to half the switching frequency. A small-signal model of the PWM stage was obtained. The resulting expression of the duty cycle of a PCMC converter shows how the perturbations in the input voltage, output voltage, inductor current and control current affect the duty cycle. The derivation of duty-cycle constraints for VM and PCMC was thoroughly explained.

A robust control design procedure based on the QFT method has been applied successfully to design a robust controller for switching-mode dc-dc converters in order to achieve robust output in spite of different uncertainties.

The QFT approach and associated design for Linear-Time-Invariant systems were presented. The implementation of the proposed technique for switching converters was divided into subtasks according to their dynamical structures. The first for the buck converter in which the transfer function of the power stage does not have a right-half-plane zero (i.e. minimum phase converters), and the second for boost and buck-boost converters which present the right-half-plane zeros in their control-output-transfer functions (i.e. non-minimum phase converters). The presence of the RHPZ contributes additional phase lag to the system restricting severely the closed-loop bandwidth .

Different design examples for buck converter were carried out to verify the control design procedures presented in the thesis. A robust controller for each operating mode along with prefilters were designed, which met the frequency domain tracking specifications, robust stability, and disturbance rejection requirements. The effectiveness and robustness of the proposed control system was confirmed by simulation results, where the Matlab^{TM} QFT Frequency Domain Control Design Toolbox [44] and Matlab^{TM}/Simulink SimPowerSystems blockset [45] are used as a setup platform for design and validation.

It was demonstrated that this technique is suitable for application in this case, which presents uncertainties in the parameters. The bandwidth of the controller is compatible with the real limitations imposed by the existing continuous models of dc-to-dc switching converters. The redesign and tradeoffs between the system performance specifications and the controller complexity can easily be done, which provides the designer with more versatile solutions. Although QFT loop shaping technique requires design experience, the obtained QFT controller provides an appropriate and practical solution for the system.

In designing the QFT controller for boost and buck-boost converters, the loop-shaping problem of a stable non-minimum nominal plant was converted to that for a stable minimum phase nominal plant by shifting robust stability and performance bounds. The reason is that in numerical design it is more convenient to work with a minimum phase function, because the optimal loop shaping procedures can be then used. The bandwidths are restricted due to their RHPZ. The stability properties have been clearly improved in terms of PM and GM. From the simulation results, it can be seen that the use of QFT controller provides good tracking performance and disturbance rejection capability. Also it provides robust stability and robust performance in the presence of uncertainties.

The concept known as unterminated two-port network representation was introduced and used to develop a proper formalism for the terminated models, which may facilitate the analysis of the effect of different loads on the converter dynamics. The effect of input filter interactions on output dynamics of VM and PCM controlled converter were studied. The theoretical formulation was based on the use of a two-port modeling approach.

The stability criterion and forbidden region concept which ensure the system stability were briefly surveyed. Most stability analysis of DPS is based on impednacce/admittance methods. These are based on the fact that small signal stability at a given operating point can be determined by examine the Nyquist contour of $Z_s\ Y_l$. The most straightforward method is the Middelbrook criteria which states that a system will be stable provided that the Nyquist contour of $Z_s\ Y_l$ remains within the unit circle. The key feature of this method is that it is very design oriented. The primary disadvantage of the Middlebrook criteria is that it leads to artificially conservative designs. The set of transfer functions describing the internal dynamics of a regulated module and the effect of load and source on the dynamics of the module are presented. Basically the load and source impedances may change the dynamical behavior of the module drastically and lead even to instability. The associated impedances may be difficult to accurately predict and therefore, the methods, which make the module invariant to those impedances are of practical importance. It was shown that the low closed-loop output impedance would make the converter insensitive to load impedances as well as would improve also the load transient behavior.

The effect of input filter on the output dynamics of the converter was analyzed and demonstrated. It was shown that in spite of stable input filter the performance of the converter can be severely degraded, and thus it is often not sufficient to study only the input filter instability. It was shown that, if the *LC*-filter resonant frequency would be placed at the frequencies, where the closed-loop input impedance has phase -180°, NRO might take place. Voltage-mode controlled converters are susceptible to performance degradation if the input filter is designed in such a way that the magnitudes of the filter output impedance and converter input impedance are not well separated at all frequencies. In low frequencies where the closed-loop input impedance of the converter is a negative resistance, the input filter instability occurs if the magnitude of the input filter output impedance is equal to converter closed-loop input impedance. In frequencies, where the phase of the closed-loop input impedance is not anymore -180°, impedance overlapping does not necessarily cause

instability of the filter or the converter. The performance of the converter can, however, be degraded. Peak-current-mode controlled converters are not prone to performance degradation, even if the magnitudes of the input filter output impedance and converter input impedance are close to each other. The physical origin of instability is the instability of the input filter. This coincides with the minor loop gain.

Preliminary contributions to the modeling and characterizing of paralleling DC-DC converters do exist but needs more rigorous analysis and systematic control design approach for gaining wider acceptance. In this thesis, a systematic modeling of parallelling DC-DC based on small-signal two-port network representation was presented. The small-signal model of paralleled converters with an individual voltage loop and current-sharing master-slave control (MSC) was developed. A robust current share controller which achieves balanced current distribution of the converters and ensures stability and performance of system was designed and verified using the developed Simulink/SimPower Systems™ models. The proposed method provided a facility to analyze the dynamics of multimodule converter and a unified model applicable to any converter regardless of topology, and the mode of operation or control.

6.2 Future Prospects

In this thesis, the dynamical modeling, control design and interactions problems have been extensively analyzed only for the basic converters, i.e., Buck, Boost and Buck-Boost, under two different control modes. However, there are numerous topologies and control principles which are used in various applications. Therefore, other converters such as, Cuk converter and Sepic converter which are typically based on the aforemention three basic converters should be analyzed.

The QFT method has been successfully applied to design robust controller for switching-mode power converters. The essential interest must be, however, subject to make practical the use of the QFT-based controllers and promote its superiorly as a valuable tool in designing robust controller and ensuring performance and stability.

One of the latest new digital signal processor (DSP) application areas is power electronics. Therefore, the opportunities and constraints of utilizing DSP in switched-mode power converters should be investigated.

More research work should be done in modeling and control design of paralleled DC-DC converters. In practice, parallel-connected DC-DC converters may be located far apart and may require unequal lengths of cable connecting them to the load they share. The output cable resistance might have significant impact on the performance of parallel-connected converters and, therefore, should be taken into account in order to make converter design more effective. Also, the analysis problem of interactions among converters should be analyzed.

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Appendix A

Appendix

A.1 Matlab™/Simulink Simulation Setup

There are a number of commercial software packages possessing necessary capabilities for modeling and design validation of switching power DC-DC converters. MATLAB™/Simulink SimPowerSystems package was chosen as a software platform. Simulink/SimPowerSystems, a toolbox of MATLAB, is a dynamic system simulation software that provides a convenient graphical user interface for building system models based on their equations [45]. However, all basic single converters models used in thesis haven been constructed using Simulink/SimPowerSystems package are shown in Figs. A.1 - A.12 and the multimodule parallel-converters models are shown in Figs. A.13 - A.15.

A.1.1 Single Output-Voltage DC-DC Converters

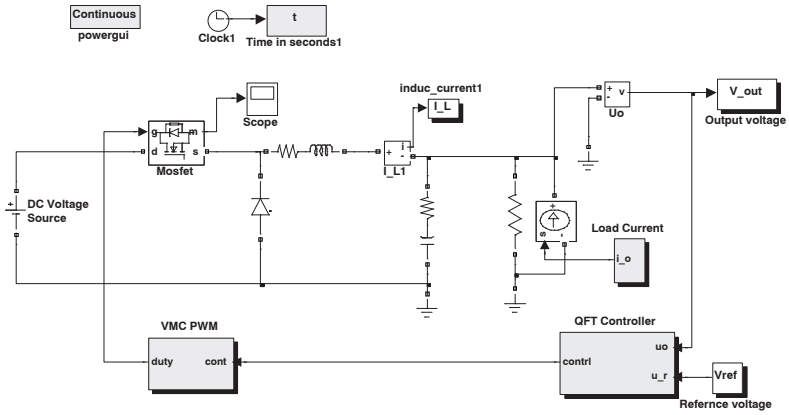

Figure A.1: VMC-Controlled-Buck Converter.

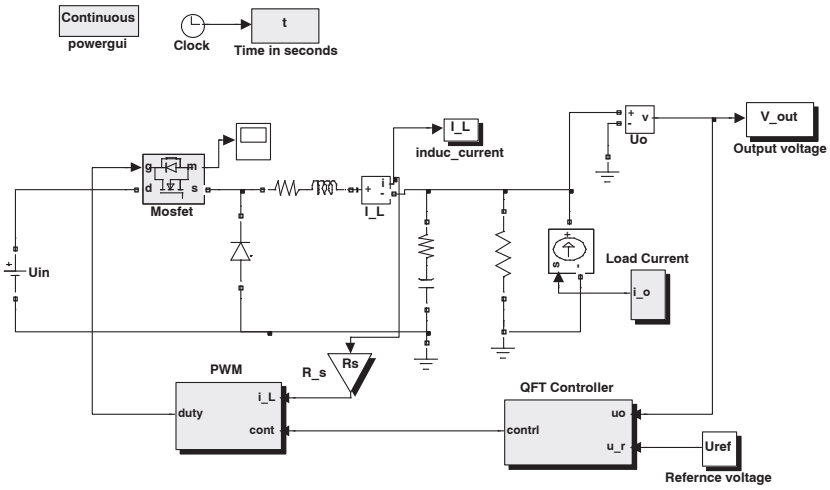

Figure A.2: PCM-Controlled Buck Converter.

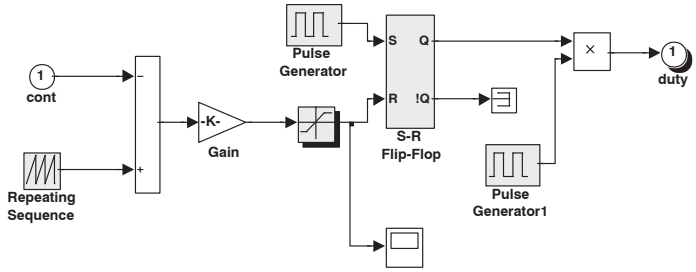

Figure A.3: PMW-VMC Control.

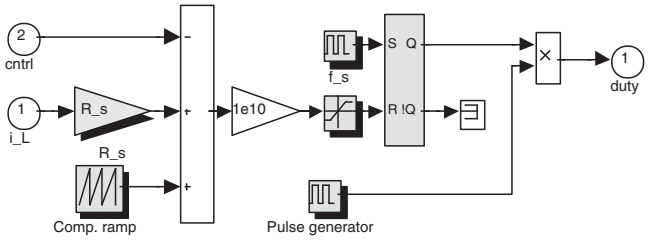

Figure A.4: PMW-PCMC Control.

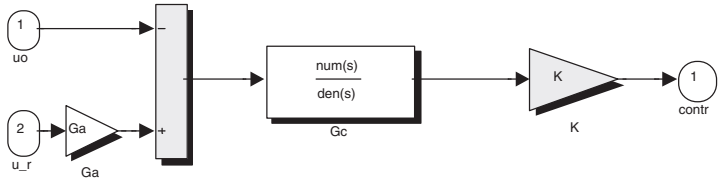

Figure A.5: QFT Controller.

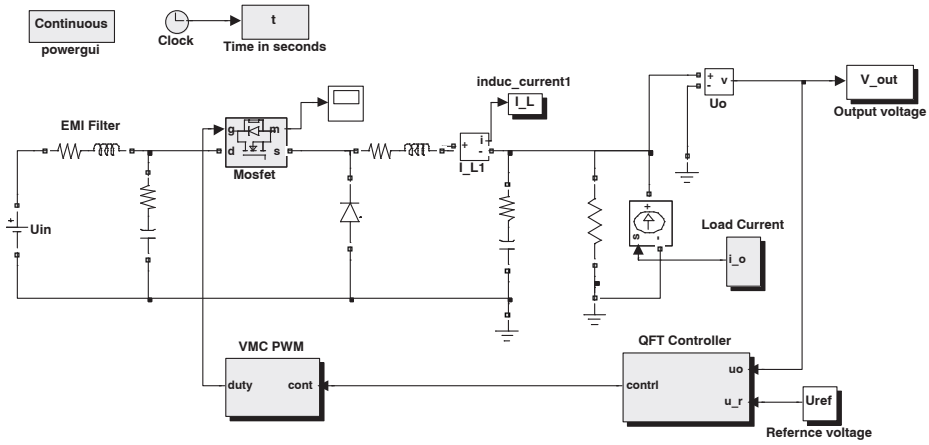

Figure A.6: Buck with EMI Filter.

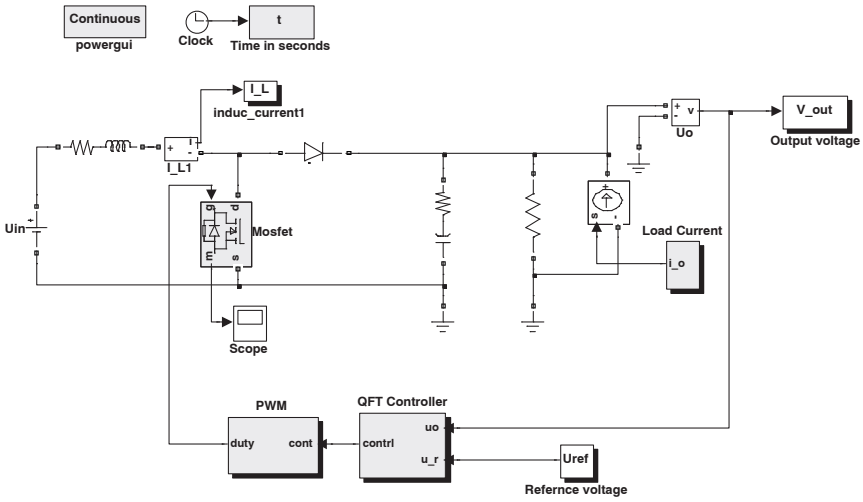

Figure A.7: VM-Controlled Boost Converter.

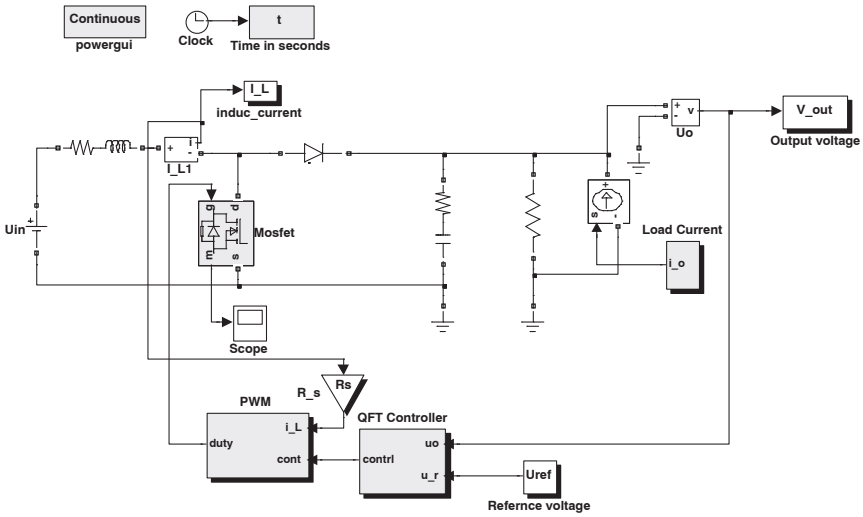

Figure A.8: PCM-Controlled Boost Converter.

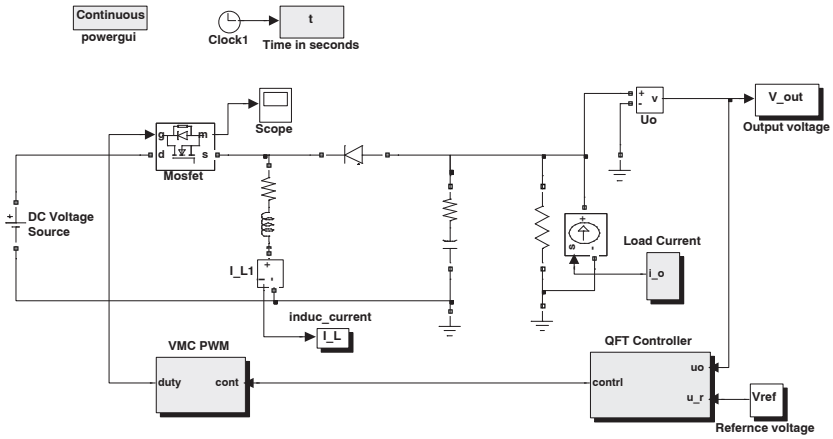

Figure A.9: VM-Controlled Buck-Boost Converter.

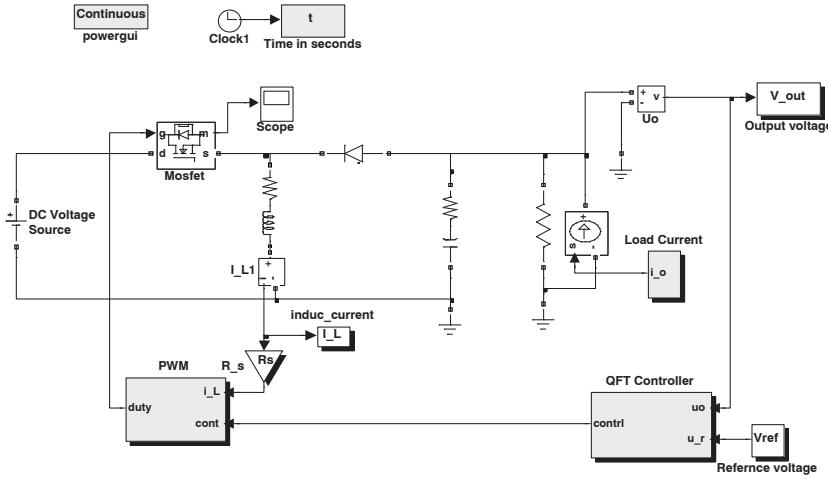

Figure A.10: PCM-Controlled Buck-Boost Converter.

A.1.2 Single Output-Current DC-DC Converters

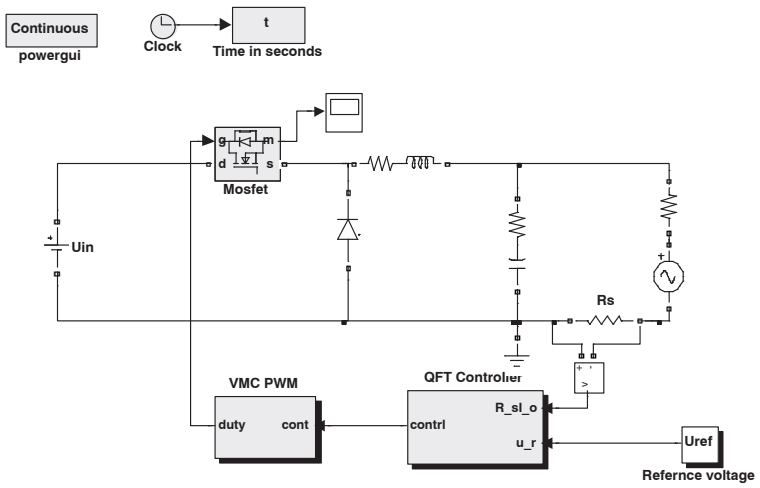

Figure A.11: VCM-Controlled Buck Converter.

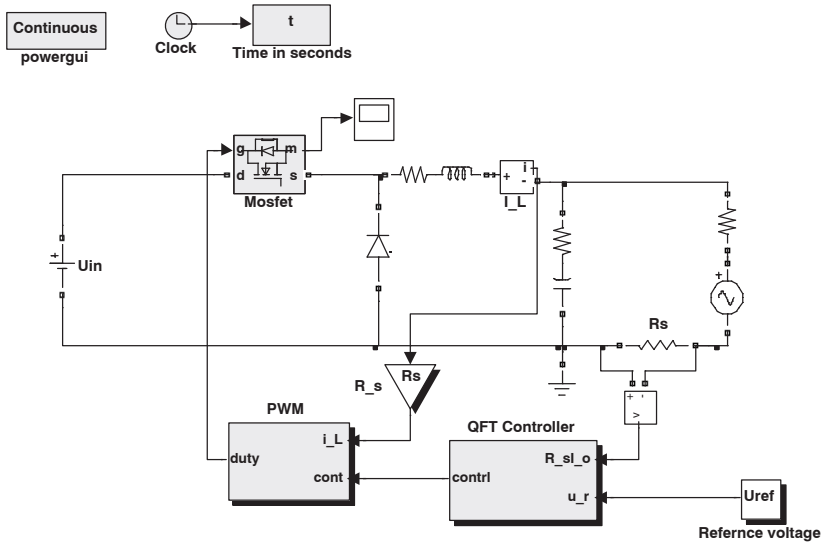

Figure A.12: PCM-Controlled Buck Converter.

A.1.3 Multimodule DC-DC Parallel Converters with MSC

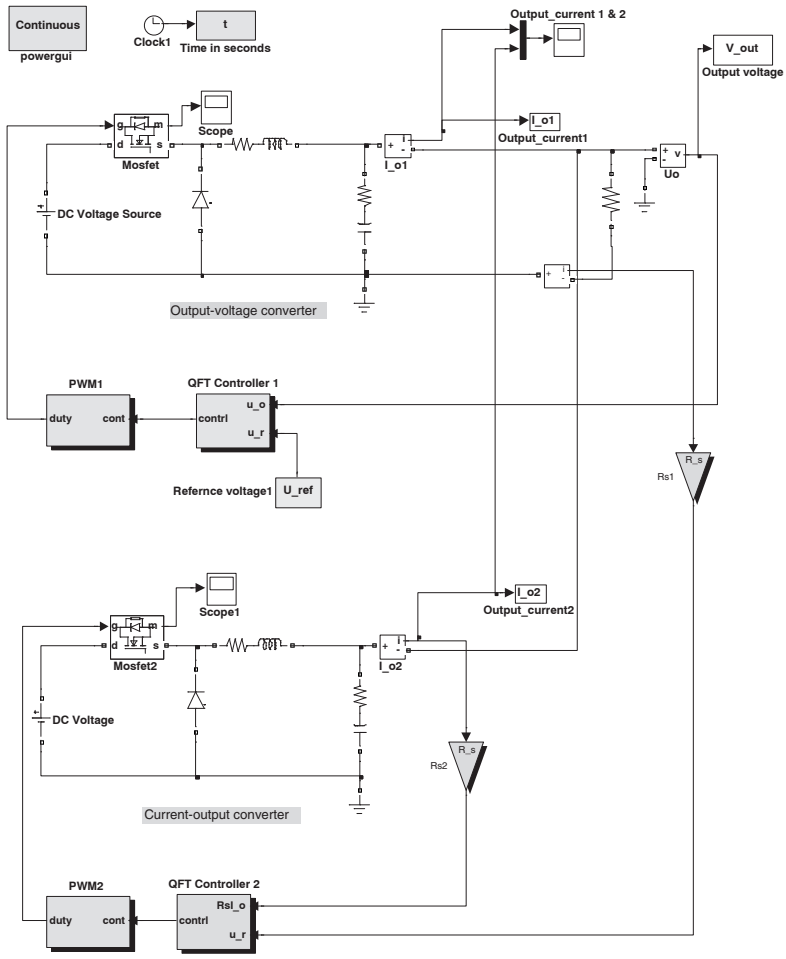

Figure A.13: Two parallel VM controlled-buck converters without current-sharing control.

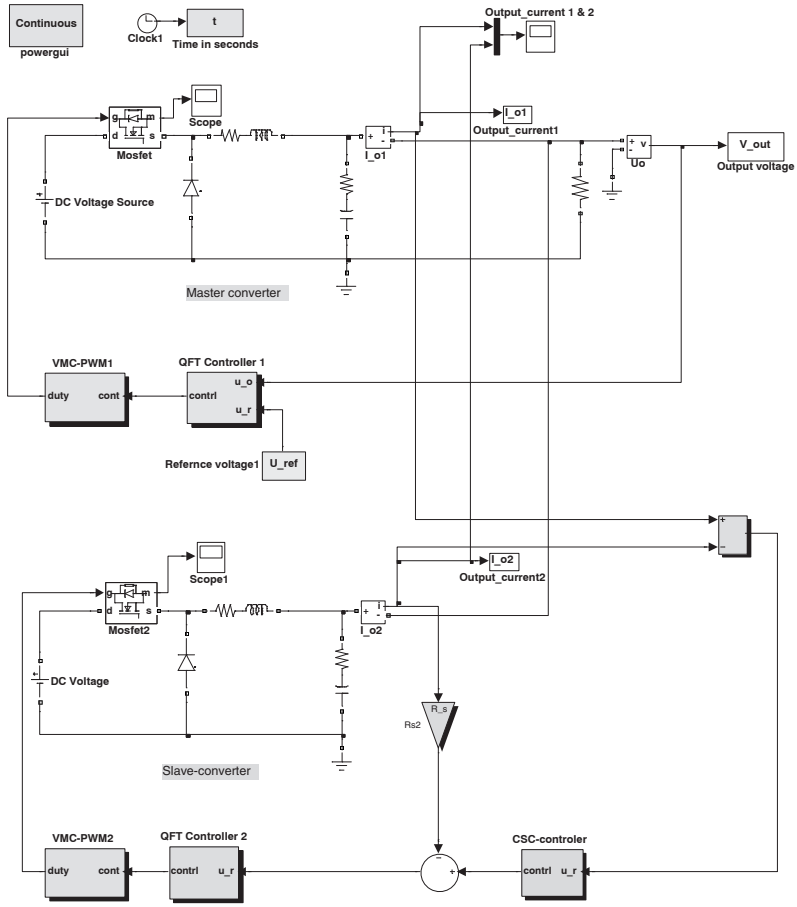

Figure A.14: Two parallel VM controlled-buck converters with MSC.

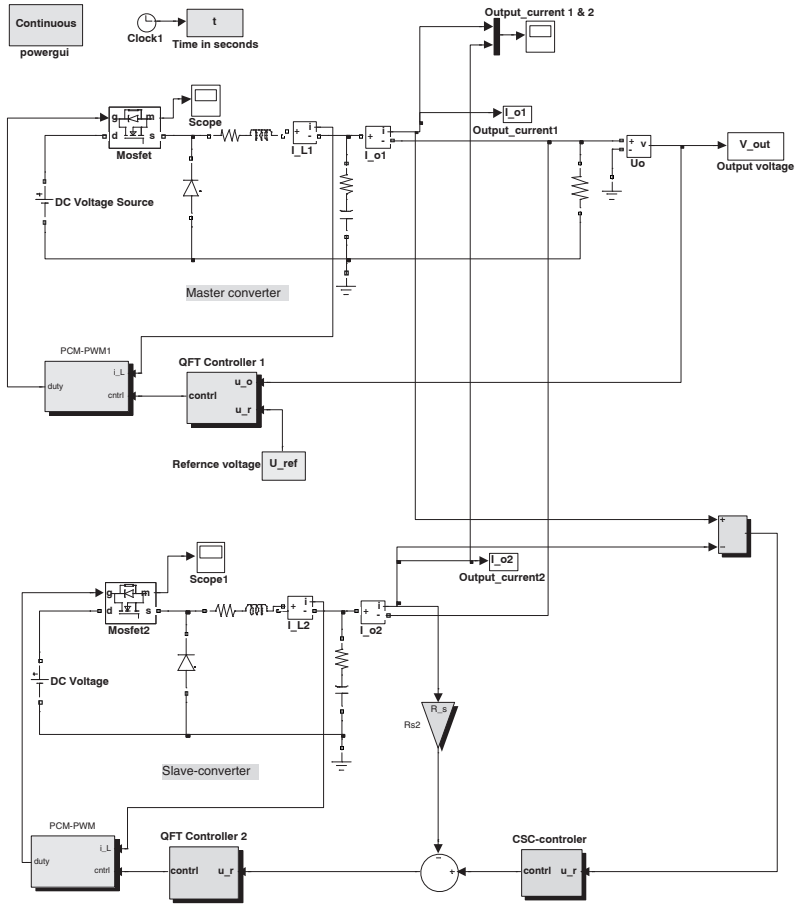

Figure A.15: Two parallel PCM controlled-buck converters with MSC.

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