Qaiser Nehal

Design of a wideband variable gain amplifier

School of Electrical Engineering

Thesis submitted for examination for the degree of Master of Science in Technology.
Espoo 11.04.2011

Thesis supervisor:

Prof. Kari Halonen

Thesis instructor:

Ville Saari

Aalto University
School of Electrical Engineering

AALTO YLIOPISTO

DIPLOMITYÖN TIIVISTELMÄ

Tekijä:	Qaiser Nehal		
Työn nimi:	Design of a wideband variable gain amplifier		
Päivämäärä:	11.04.2011	**Sivumäärä:**	59
Osasto:	Sähkötekniikan Korkeakoulu		
Professuuri:	S-87 Piiritekniikka		
Työn valvoja:	Professori Kari Halonen		
Työn ohjaaja:	Ville Saari		

Synteettisapertuurinen tutka (SAR) on hyvin tunnettu tekniikka maanpinnan kuvantamiseen. Tässä diplomityössä on suunniteltu laajakaistainen säädettävä vahvistin, jota voidaan käyttää SAR:in suorasekoitusvastaanottimessa (DCR). Ensin näytetään kuinka tärkeät muuttujat, kuten esimerkiksi VGA:n vahvistus, kaistanleveys ja kohina, saadaan määritettyä vastaanottimen kokonaisvaatimuksista. Seuraavaksi e-sitetään yleisesti suunnittelutapa VGA:lle, jossa tunnistetaan VGA:n tärkeimmät suunnittelu moduulit. Laajakaistaiset asteet, joita voidaan käyttää VGA:n suunnittelussa, esitellään lyhyesti, kuten myös tekniikoita, joilla siirrosjännite saadaan kompensoitua. Seuraavaksi esitellään yksityiskohtaisesti kuinka VGA suunnitellaan. Työssä esitetään piensignaali- ja kohina-analyysit VGA:n vahvistusasteille kuten myös simulaatiotulokset. VGA on suunniteltu ja valmistettu 0.13 μm CMOS prosessilla. Piirikuvion jälkeiset simulaatiot on myös esitetty ja ne todentavat lopullisen piirikuvion toimivuutta. Lopuksi esitetään VGA:n mittaustulokset, jotka näyttävät, että halutut vahvistus ja kaistanleveys on saavutettu. Mikropiirin digitaalisen ohjauksen epätasaisesta toimivuudesta johtuen, VGA:n taajuusvasteessa näkyi vahvistuksen piikittämistä. VGA:n tulon kohinatiheyden mittaustulokset eri vahvistusasetuksilla on myös esitetty ja ne vastaavat hyvin simuloituja arvoja. Tulon 1 dB:n kompressiopiste ja tulon kolmannen kertaluvun keskinäismodulaatiosärön leikkauspiste on myös annettu VGA:lle. Yleisesti ottaen VGA:n toimintaa voidaan pitää onnistuneena SAR:ssa käytettävälle suorasekoitusvastaanottimelle.

Avainsanat:	wideband, variable gain amplifier, low noise amplifier, low power CMOS

AALTO UNIVERSITY

ABSTRACT OF THE MASTER'S THESIS

Author:	Qaiser Nehal		
Name of the thesis:	Design of a wideband variable gain amplifier		
Date:	11.04.2011	**Number of pages:**	59
Department:	School of Electrical Engineering		
Professorship:	S-87 Electronic Circuit Design		
Supervisor:	Professor Kari Halonen		
Instructor:	Ville Saari		

Synthetic Aperture Radar (SAR) is a well known technique for imaging the earth's surface. This thesis presents a wideband variable gain amplifier which can be used in the direct conversion receiver (DCR) for SAR. The thesis first introduces how to extract the important parameters i.e. gain, bandwidth and noise of the VGA from the overall receiver requirements. Next, a general design philosophy for the VGA is presented which identifies the main design modules in the amplifier. Also, a brief introduction to wideband stages and DC-offset compensation techniques is presented. Then a detailed explanation of the VGA design is given. Small-signal and noise analyses are presented for the VGA gain stages along with their simulation results. VGA post-layout simulation results are also shown to verify the functionality of the final layout drawn using 0.13 μm CMOS. At the end, measurement results for the VGA are given which show that the VGA achieved the desired gain and bandwidth. However, due to irregular operation of the digital control for the chip, the frequency response of the VGA showed gain peaking. The measured input noise density of the VGA at different gain settings is also given and it matched well with the simulated value. Moreover, the input 1 dB compression point and the third order input intercept point results for the VGA are also given. The overall operation of VGA was deemed satisfactory for the direct conversion receiver for SAR.

Keywords: wideband, variable gain amplifier, low noise amplifier, low power CMOS

Foreword

The research for this thesis was carried out in the Electronic Circuit Design Laboratory (ECDL) of Aalto University. The work presented in this thesis was part of a reseearch project funded by the European Space Agency (ESA).

I would like to thank Professor Kari Halonen for giving me the opportunity to work in the ECDL and for his continued support and guidance during the research. I would also like to thank my instructor Ville Saari for teaching me a lot of things about the design of CMOS baseband circuits. Thanks to the members of our research team especially Tero Nieminen and Faizah Abubakar for creating a pleasant work atmosphere. Next I would also like to thank all of my colleagues at ECDL especially Tero Tikka, Mika Pulkkinen and Matthew Turnquist for helping me during the measurements of the chip.

At the end I would like to thank my family for their support and encouragement during my studies.

Espoossa 11.04.2011

Qaiser Nehal

Table of Contents

Symbols and Abbreviations

$A_{v1}(s)$ Voltage gain of stage 1 in the VGA

$A_{v2}(s)$ Voltage gain of stage 2 in the VGA

g_{mbs} MOSFET Body Transconductance

GBW_S Gain-Bandwidth Product of each stage

k Boltzmann's constant (1.38x10^{-23} J/K)

$SNDF$ Subsequent-stage noise degradation factor

T Absolute temperature (290 K)

$A_{v,RF}$ Voltage gain of RF front-end

ADC Analog-to-Digital Converter

CMFB Common-mode Feedback

CMRR Common-mode Rejection Ratio

DCR Direct conversion receiver

DUT Device-under-test

IIP3 Third-order input intercept point

LNA Low-noise amplifier

LPF Low Pass Filter

NF_{RF} Noise figure of the RF front-end

NF_{RX} Noise figure of the receiver

P-1dB 1 dB Compression point

PCB Printed Circuit Board

QFG Quasi-floating gate

SAR Synthetic Aperture Radar

VGA Variable Gain Amplifier

Chapter 1

Introduction

Synthetic Aperture Radar (SAR) is a well known technique for imaging the earth's surface. Some of its most important applications include disaster management, land and sea traffic observation, wide area surveillance, and environmental monitoring. SAR systems use radar signals and complex electronics to provide broad-area imaging capability. The most attractive feature of SAR systems is their ability to provide day-and-night imagery of earth, independent of weather conditions [1].

In order to overcome the limitation of imaging wide swath, with simultaneously high resolution, SAR systems employ receiving antenna with multiple sub-apertures, each sub-aperture with its own independent receiver [2] as shown in Fig. 1.1. Each of the N sub-apertures on the receive antenna has its own receiver. The digitized signals from each of these receivers can then be stored and digitally processed a posteriori to form a high resolution image of a large area. In such a system it would be beneficial to realize each of the independent receivers with highly integrated CMOS circuits that have small silicon footprint and an overall low power consumption. A block diagram representation of such a receiver is shown in Fig. 1.2. It is a direct conversion receiver (DCR) which downconverts the RF signal directly to its baseband. DCR has the advantage that it requires no off-chip image reject filters. Moreover, it only requires low-pass filters and amplifiers that are amenable to monolithic integration.

In this thesis, the design of a wideband variable gain amplifier (VGA) is described which is to be used in the DCR for SAR systems. Therefore small silicon area and low power consumption are the basic goals for the design. In the next few chapters VGA design goals will be explained along with the different circuits that can be used in the wideband amplifier design.

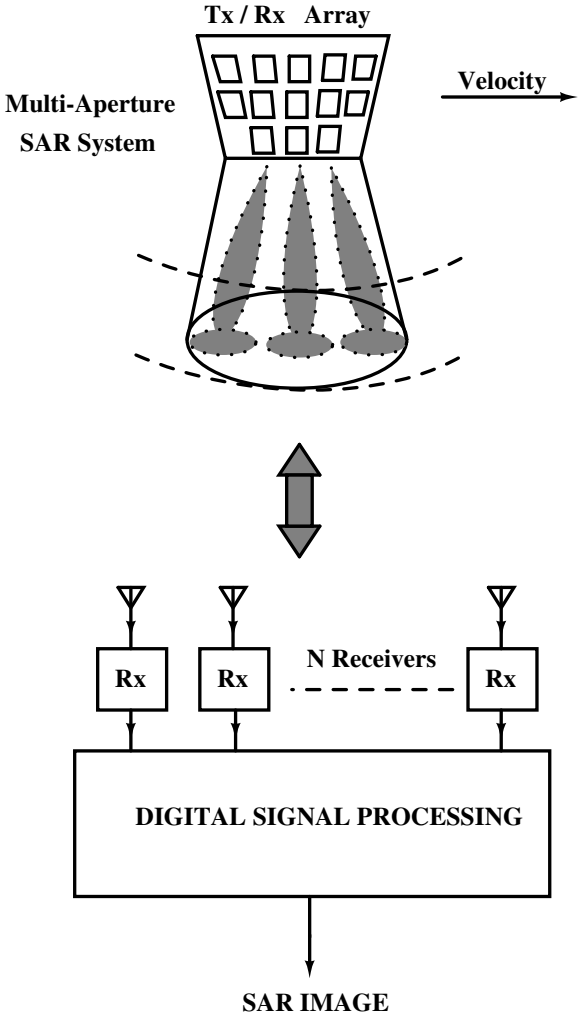

Figure 1.1: SAR multi-aperture system.

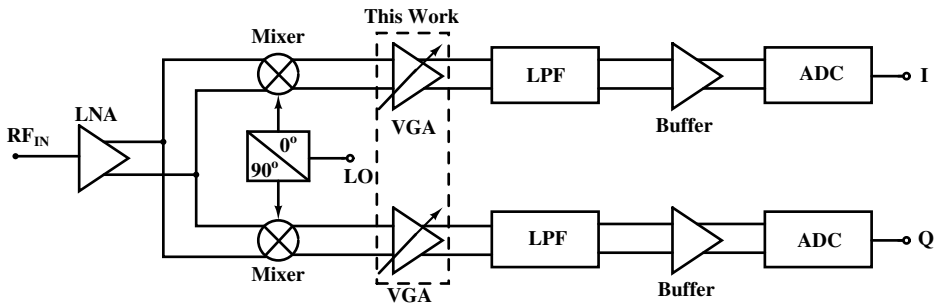

Figure 1.2: Block diagram of the SAR direct conversion receiver.

Chapter 2

Variable gain amplifier design goals

This chapter describes how the various design goals of the variable gain amplifier (VGA) were determined from the given requirements for the baseband of the direct conversion receiver for Synthetic Aperture Radar (SAR). It also explains the general theory behind multi-stage amplifier design.

2.1 Bandwidth

One of the requirements for the baseband of the receiver was to have an overall flat response in the passband. The baseband low pass filter (LPF) was a 5th-order Chebyshev filter with 0.3 dB passband ripple and cut-off frequency of 160 MHz. The filter was realized as a continuous-time gm-C leapfrog filter. It was synthesized using a lossy prototype as presented in [3]. In order to meet the passband gain flatness requirement while simultaneously achieving the necessary gain, the baseband was simulated using MATLAB and the magnitude response of the overall chain was compared to that of a 5th-order Chebyshev filter. In the simulations the bandwidth of the VGA was increased incrementally and its affect on the overall baseband response can be seen in Fig. 2.1.

From Fig. 2.1 it is quite clear that VGA affects the shape of the passband response as well as the cut-off frequency of the LPF, particularly when the bandwidth of the VGA is approximately the same as the LPF cut-off frequency. This is because the gain of VGA starts to roll-off at frequencies lower than the -3 dB bandwidth of the VGA. Therefore in order to have an over all flat response of the baseband the bandwidth of the VGA should be much higher than the cut-off frequency of the LPF. From Fig. 2.1 it can be seen that a VGA with -3 dB bandwidth of 1 GHz does not significantly influence the shape of the LPF. Therefore the bandwidth of the VGA was chosen to be 1 GHz.

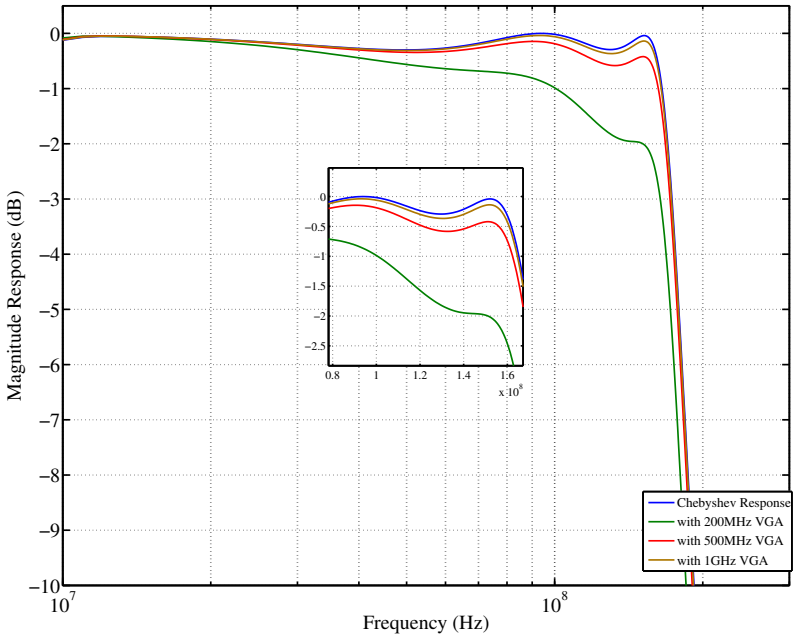

Figure 2.1: Simulated frequency response of the overall baseband chain of the receiver with varying VGA bandwidth.

2.2 Gain

The voltage gain of the receiver was calculated from the signal level at the input of the receiver and the desired full-scale voltage at the analog-to-digital converter (ADC). This value turned out to be 48 dB. It was decided that the RF front end of the receiver will provide 20 dB gain while the remaining will come from the baseband. According to [3], the Miller-effect degrades the filter response. Therefore in order to preserve the filter shape, the voltage gain from the LPF was kept small (about 8 dB) and the rest of the gain (20 dB) was assigned to VGA. Moreover the VGA should be able to provide $\pm$6 dB coarse gain adjustment steps. The tunable gain of the VGA would increase the dynamic range of the receiver.

2.3 Noise

The overall noise figure of the receiver (NF_{RX}) was targeted to be less than 10 dB. Assuming that the RF front-end noise figure (NF_{RF}) is about 8 dB and its voltage gain ($\mathrm{A}_{v,RF}$) is about 20 dB, the overall noise figure of the receiver can be written as

$$NF_{RX} = 10log_{10}\left[10^{\frac{NF_{RF}}{10}} + \frac{(\bar{v}_{n,BB,in})^2}{kT(2B)R_S(10^{\frac{A_{v,RF}}{20}})^2}\right], \tag{2.1}$$

where $\bar{v}^2_{n,BB,in}$ is the integrated input-referred noise of the baseband of the receiver, k is the Boltzmann's constant (1.38x10^{-23} J/K), T is the absolute temperature (290 K), R_S is the

source resistance (50Ω) and B is the baseband bandwidth (160 MHz). Therefore from (2.1), the noise density of the baseband circuit referred to the input of the baseband would be

$$\frac{\bar{v}_{n,BB,in}}{\sqrt{B}} = \left(10^{\frac{A_{v,RF}}{20}}\right)\sqrt{2kTR_S\left(10^{\frac{NF_{RX}}{10}} - 10^{\frac{NF_{RF}}{10}}\right)} \approx 12nV/\sqrt{Hz}. \qquad (2.2)$$

From Fig. 2.2 it can be seen that the noise of the VGA dominates the noise of the baseband circuit because the gain of VGA is much higher than that of the other blocks in the baseband. Therefore the noise density of VGA referred to its input should be lower than 12 nV/$\sqrt{Hz}$ so that the overall noise density of the baseband satisfy (2.2).

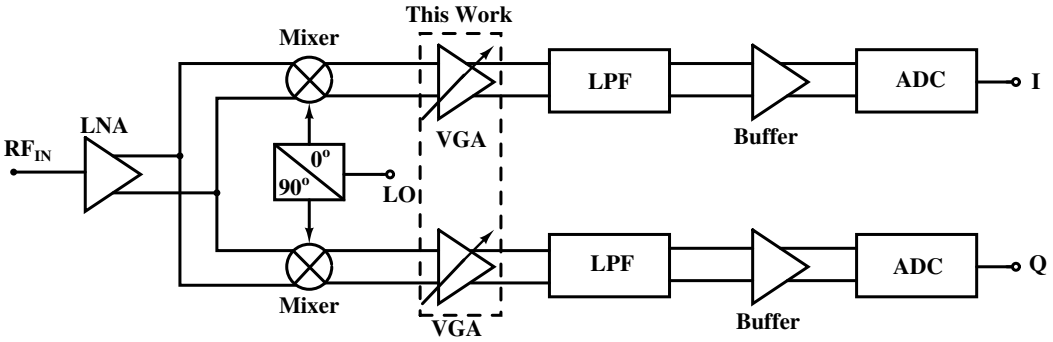

Figure 2.2: Block Diagram of the integrated receiver for SAR.

2.4 Input 1 dB compression point

The signal level at the input of the baseband will be -40 dBVrms. Since VGA is the first block in the baseband (see Fig. 2.2), its input 1 dB compression point should be higher than -40 dBVrms.

2.5 Power consumption

The power consumption of the VGA was targeted to be less than 10 mW so that the overall power consumption of the baseband circuit remains small.

Table 2.1 summarizes the design goals for the VGA.

Table 2.1: VGA Design Goals.

-3dB frequency	1 GHz
Gain	20 dB with ±6 dB steps
Input-referred noise density	$<$ 12 nV/$\sqrt{Hz}$
Input 1 dB compression point	$>$ -40 dBVrms
Power consumption	$<$ 10 mW

2.6 VGA design philosophy

The three important requirements for the VGA are wide bandwidth, low noise and a tunable gain. Wide bandwidth (over 1GHz at all gain settings) is required to keep the transfer function flat within the passband. Since most of the gain for baseband amplification comes from VGA, its input-referred noise density determines the overall input-referred noise density of the baseband. In order to meet these requirements, the following design approach was adopted. The amplifier was divided in to four design blocks: the low-noise input stage, variable gain stages, the input AC coupling and a DC-offset correction feedback stage (see Fig. 2.3). Gain adjustment could be incorporated in two of the three design blocks i.e., the low-noise input stage and the other variable gain stages. However, in order to get a good noise performance at all gain settings, the input stage was designed to have a fixed gain. Moreover, by keeping the gain of the input stage much higher than the remaining stages, the noise from the input stage dominates the overall input-referred noise of the VGA. The AC coupling removes any DC offset coming from the RF front end and the negative DC feedback network removes the DC offset voltage originating from the device mismatches in the low-noise input stage of the VGA.

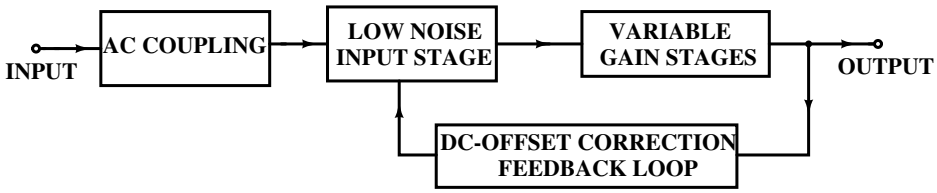

Figure 2.3: Design philosophy of VGA.

On the basis of the above arguments, it was decided that the low-noise input stage will provide the bulk of the gain (about 14 dB) whereas the variable gain stages will provide the rest of the gain. Table 2.2 summarizes the gain assignment to various stages at different gain steps.

Table 2.2: VGA gain assignment.

Total Gain	**Low-noise input stage**	**Variable gain stages**
14 dB	14 dB	0 dB
20 dB	14 dB	6 dB
26 dB	14 dB	12 dB

Several CMOS based VGA designs have been reported [4, 5, 6] and many of them use multiple stages cascaded together to provide the necessary gain and bandwidth. However there are some important points related to gain-bandwidth product and the noise of a multistage amplifier which are described below. These points are important as they will in turn

give the number of stages to be used in the variable gain section of the multistage architecture, so that the overall VGA design adheres to the goals presented earlier.

2.6.1 Gain-bandwidth considerations

Consider a multistage amplifier with a DC gain A_A and a -3 dB bandwidth w_A. Lets consider that the multistage amplifier is formed from a cascade of n identical stages (see Fig. 2.4), each with a single pole response

$$A_s(jw) = \frac{A_O}{1 + j\frac{w}{w_B}},$$

where A_O is the DC gain and w_B is the -3 dB bandwidth of each stage. Assuming that

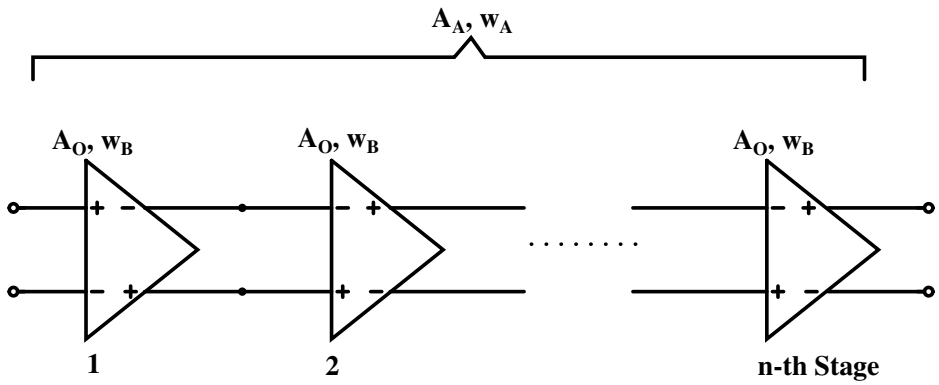

Figure 2.4: Multistage amplifier with n identical stages.

there is no interaction among the stages, then the overall transfer function of the multistage amplifier is

$$A_A(jw) = \left(\frac{A_O}{1 + j\frac{w}{w_B}}\right)^n, and \tag{2.3}$$

$$A_A = A_O^n. \tag{2.4}$$

The -3 dB bandwidth of the multistage amplifier w_A is the frequency at which

$$|A_A(jw_A)| = \frac{A_A}{\sqrt{2}} = \frac{A_O^n}{\sqrt{2}}.$$

Thus

$$\left[\frac{A_O}{\sqrt{1 + (\frac{w_A}{w_B})^2}}\right]^n = \frac{A_O^n}{\sqrt{2}},$$

$$1 + (\frac{w_A}{w_B})^2 = 2^{\frac{1}{n}},$$

$$w_A = w_B\sqrt{2^{\frac{1}{n}} - 1}.$$

The above relation shows that the bandwidth of the multistage amplifier w_A will be less than the bandwidth of the individual stages w_B.

In general a cascade of n identical gain stages, each having a bandwidth w_B, exhibits an overall bandwidth w_A of [7]

$$w_A = w_B \sqrt[m]{2^{1/n} - 1}\,, \tag{2.5}$$

where *m* is equal to 2 for first-order stages and 4 for second order stages. The gain A_O and bandwidth w_B of each stage can be written in terms of the overall gain A_A and bandwidth w_A as

$$A_0 = (A_A)^{\frac{1}{n}}$$
$$w_B = \frac{w_A}{\sqrt[m]{2^{1/n} - 1}}.$$

The gain-bandwidth product (GBW_S) of each stage is given by

$$GBW_S = \frac{f_A}{\sqrt[m]{2^{1/n} - 1}}.\,(A_A)^{\frac{1}{n}}\,, \tag{2.6}$$

where f_A is the -3 dB bandwidth of the multistage amplifier in Hz. Let us now define normalized quantities for the single-stage gain, bandwidth and the gain-bandwidth product as

$$GBWN_S \equiv \frac{GBW_S}{f_A.A_A} = \frac{A_A^{\frac{1}{n}-1}}{\sqrt[m]{2^{1/n} - 1}}, \tag{2.7}$$

$$GN_S \equiv \frac{A_O}{A_A} = A_A^{\frac{1}{n}-1}, and \tag{2.8}$$

$$BWN_S \equiv \frac{w_B}{w_A} = \frac{1}{\sqrt[m]{2^{1/n} - 1}} \tag{2.9}$$

Fig. 2.5 shows the normalized single-stage gain, bandwidth and the gain-bandwidth product as a function of n (number of single-stages) when A_A = 12 dB (this is the maximum gain required from variable gain section of VGA). The single-stage gain decreases as a function of the number of single-stages used in the amplifier. On the other hand, large single-stage bandwidth is needed when the number of stages is increased. The net effect is that the required gain-bandwidth product per stage to construct a multistage amplifier (with gain-bandwidth product $f_A A_A$) reaches its minimum value for $n = 4$. Thus using 4 stages in a multistage architecture to achieve $A_A = 12\,dB$ overall gain and wide bandwidth ($f_A > 1\,GHz$) will result in the minimum single-stage gain-bandwidth product.

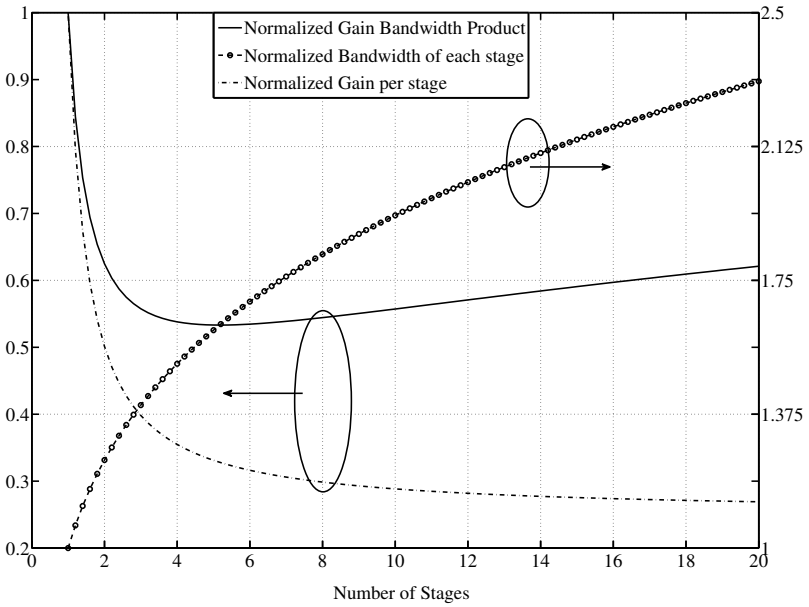

Figure 2.5: Normalized single-stage gain, bandwidth and the gain-bandwidth product as a function of n (number of single-stages).

2.6.2 Noise considerations

Lets now have a look at the noise performance of multistage amplifier. Assume that the multistage amplifier is made up of n identical stages each with power gain A_{OP} and noise figure F as shown in Fig. 2.6. The noise figure of the multistage amplifier F_n can be written

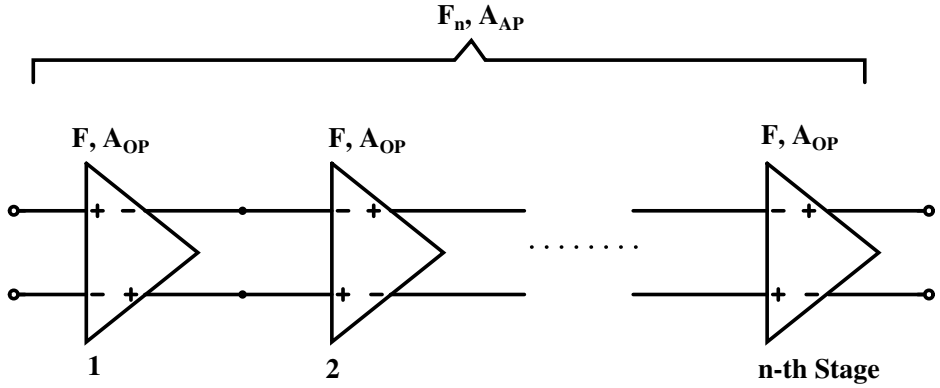

Figure 2.6: Multistage amplifier with n identical stages.

according to Friis formula as

$$F_n = F + \frac{F-1}{A_{OP}} + \frac{F-1}{A_{OP}^2} + \frac{F-1}{A_{OP}^3} + ... + \frac{F-1}{A_{OP}^{n-1}}. \tag{2.10}$$

As the number of cascaded stages is increased, the number of noise sources increases and the gain per stage reduces. As the gain per stage becomes less, the noise generated by the subsequent stages becomes important. A good way to quantify this effect is to define

subsequent-stage noise degradation factor ($SNDF$)

$$SNDF \equiv \frac{F_n - 1}{F - 1} = 1 + \frac{1}{A_{OP}} + \frac{1}{A_{OP}^2} + \frac{1}{A_{OP}^3} + ... + \frac{1}{A_{OP}^{n-1}}, \tag{2.11}$$

$$SNDF = \sum_{i=1}^{n} \frac{1}{A_{OP}^{i-1}}, \tag{2.12}$$

$$SNDF = \sum_{i=1}^{n} \left(\frac{1}{A_{AP}^{\frac{1}{n}}} \right)^{i-1}, \tag{2.13}$$

where A_{AP} is the overall power gain of the mutlistage amplifier.

The subsequent-stage noise degradation factor is plotted in Fig. 2.7 as a function of the number of stages. Note that SNDF increases rapidly in the beginning when number of stages is small. Thus keeping the number of stages to a minimum, makes the noise of subsequent stages less significant because of the high gain per stage.

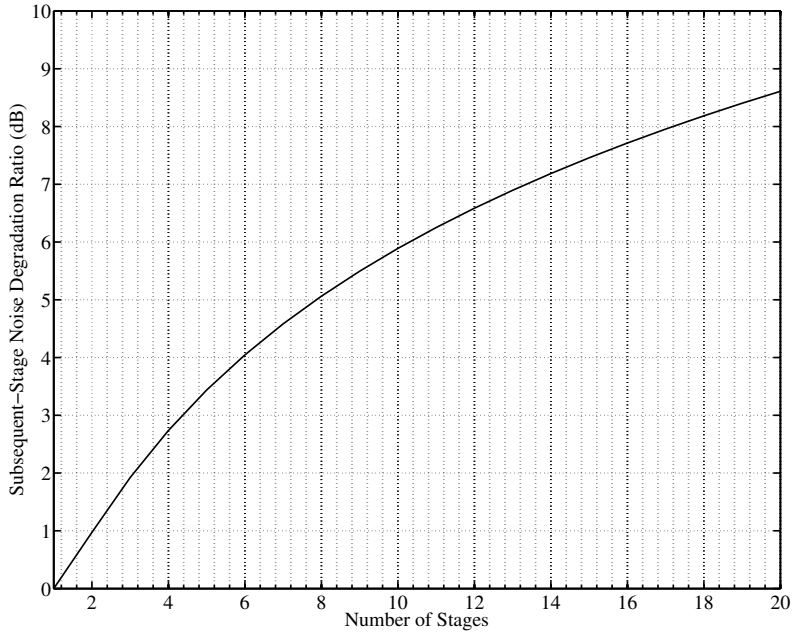

Figure 2.7: Subsequent-stage noise degradation ratio versus number of stages.

2.6.3 Number of stages

In the earlier sections, the effect of the number of stages on the single-stage gain-bandwidth product was shown and it was concluded that choosing 4 stages will give the minimum required single-stage gain-bandwidth product. However, the last section also showed that increasing the number of cascaded stages reduces the gain per stage and as the gain per stage becomes less, the noise generated by the subsequent stages becomes important. The goal should be to minimize the single-stage gain-bandwidth product and reduce the affect of the

noise generated by the subsequent stages. Therefore a figure-of-merit (FOM) was defined as

$$FOM = \frac{1}{GBWN_S.SNDF}. \tag{2.14}$$

The FOM is plotted in Fig. 2.8 as a function of the number of stages. It shows that the best

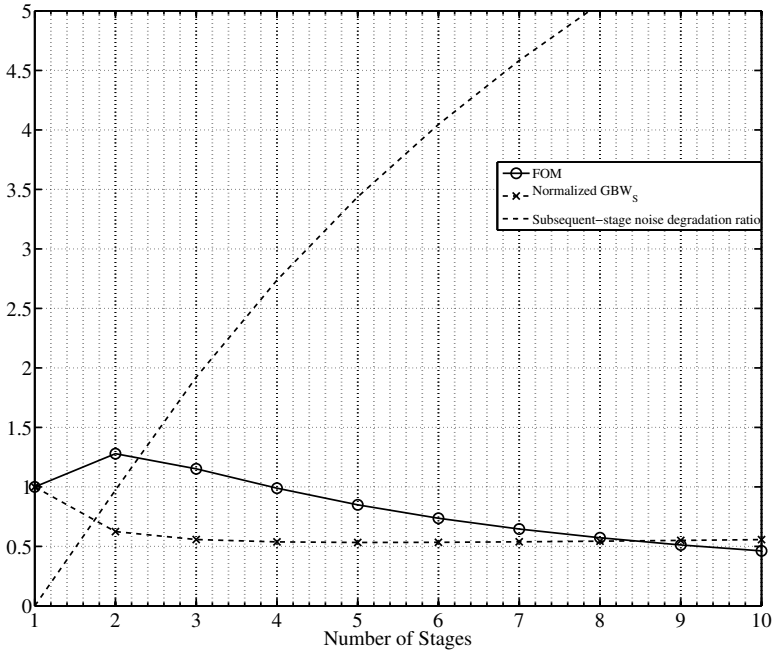

Figure 2.8: Figure-of-merit (FOM) versus number of stages.

FOM is achieved when $n = 2$. This means that using only two stages in the variable gain section of the VGA will give us the lowest noise performance while simultaneously lowering the required gain-bandwidth product per stage.

2.7 Summary

This chapter explained how the most important parameters for VGA design were extracted from the overall system requirements. Based on these VGA design goals a design philosophy for the VGA was presented. Next several important points related to multistage amplifier design were presented and it was concluded that using two stages in the variable gain section of the VGA gives the best figure-of-merit.

Chapter 3

Techniques for wideband stages and DC-offset compensation

The previous chapter discussed important issues related to multistage amplifier design. Note that using a multistage architecture relaxes the gain-bandwidth requirement per stage, but we still require wide bandwidth in each stage to ensure that the -3 dB bandwidth of the multistage amplifier w_A meets the design specification. In fact, the required single-stage bandwidth w_B is always greater than the multistage amplifier bandwidth i.e. $w_B > w_A$. Therefore, it is important to understand the various methods that can extend the bandwidth of stages. Moreover, the high gain of the VGA in baseband, makes the subsequent LPF susceptible to the DC-offset from the RF front-end [8]. In this chapter different techniques for DC-offset compensation will also be examined.

3.1 Wideband stages

3.1.1 Source-coupled differential pair

One of the simplest gain stages is the resistively loaded source-coupled differential pair shown in Fig. 3.1. M_1 and M_2 are the two source-coupled transistors with resistive load R_D and M_3 acts as the tail current source. R_S represents the source resistance. The differential mode ac half-circuit and the corresponding small signal circuit are shown in Fig. 3.2. For simplicity the load capacitance at the output node and the drain-body capacitance C_{db} have been ignored. Since these capacitances would be connected in parallel with R_D , their effect could be handled by replacing R_D with Z_L , where Z_L equals R_D in parallel with $C_{db} + C_L$. Using the dominant pole approximation, the differential mode transfer function is given by

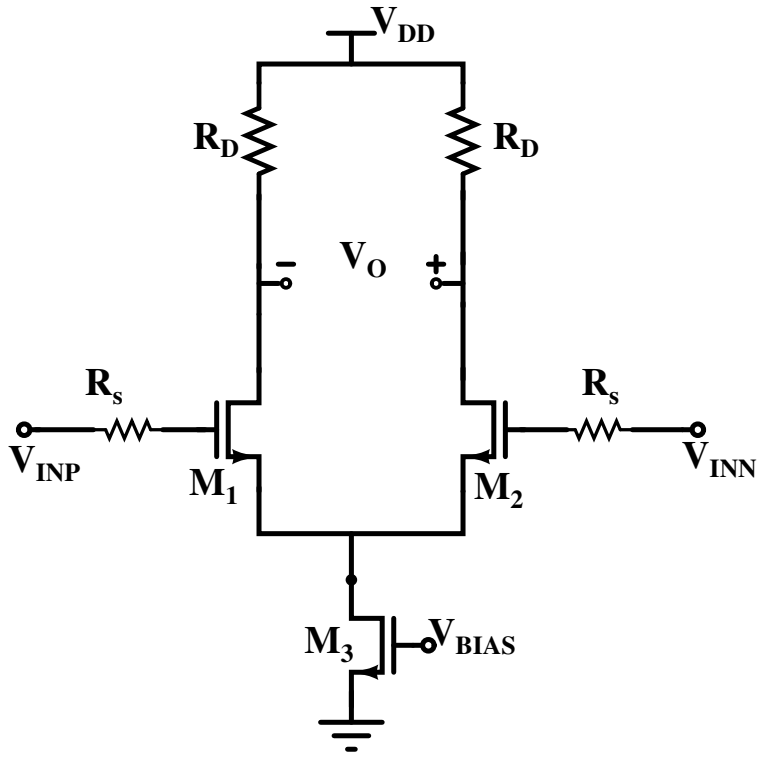

Figure 3.1: Schematic of Source-coupled Differential Pair.

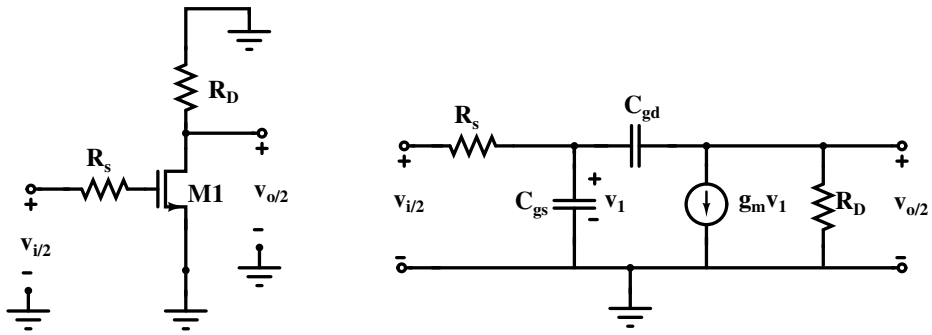

Figure 3.2: (a) Differential mode ac half-circuit of Source-coupled differential pair. (b) Small-signal equivalent circuit for (a).

$$\frac{v_O}{v_S} \approx -\frac{g_m R_D \left(1 - s\frac{C_{gd}}{g_m}\right)}{\left(1 + \frac{s}{p_1}\right)\left(1 + \frac{s}{p_2}\right)}, \tag{3.1}$$

$$p_1 = \frac{1}{R_S\left[C_{gs} + C_{gd}\left(1 + g_m R_D + \frac{R_D}{R_S}\right)\right]}, \; and \tag{3.2}$$

$$p_2 = \left(\frac{1}{R_D C_{gd}} + \frac{1}{R_S C_{gs}} + \frac{1}{R_D C_{gs}} + \frac{g_m}{C_{gs}}\right). \tag{3.3}$$

Note that in the expression of p_1 C_{gd} is increased by the factor $(1 + g_m R_D)$ (Miller-effect), thus making it the dominant pole. p_2 is a very high frequency pole (the last term in the expression of p_2, $\frac{g_m}{C_{gs}} > w_T$ (transition frequency for the transistor)). Thus the bandwidth of the source-coupled pair is determined by the input pole p_1.

3.1.2 Miller-effect suppression using cascode transistor

The previous section showed that the bandwidth of the source-coupled pair is determined by the input pole p_1. This is mainly due to the Miller-effect which increases the input capacitance by $C_{gd}(1 + g_m R_D)$. This effect is particularly detrimental when the gain of the differential pair $g_m R_D$ is high. One way to suppress Miller-effect is by stacking another transistor M_4 on top of the main transistor M_1 as shown in Fig. 3.3. In this case the input impedance looking in to the source of M_4 is about $1/g_{m4}$ and the voltage gain from the input to node x reduces from $g_m R_D$ to g_m/g_{m4}. If both M_1 and M_4 are of the same dimensions and carry the same current, then the input capacitance (seen looking in to the gate of M_1) is reduced to

$$C_{input} = C_{gs} + 2C_{gd}$$

Thus, by using the cascode technique the input pole can be pushed to higher frequency, resulting in an increase in the bandwidth. Note that the DC voltage gain from the input to output remains same because the cascode transistor acts as a common-gate stage (current buffer). Thus the overall DC voltage gain stays $g_m R_D$.

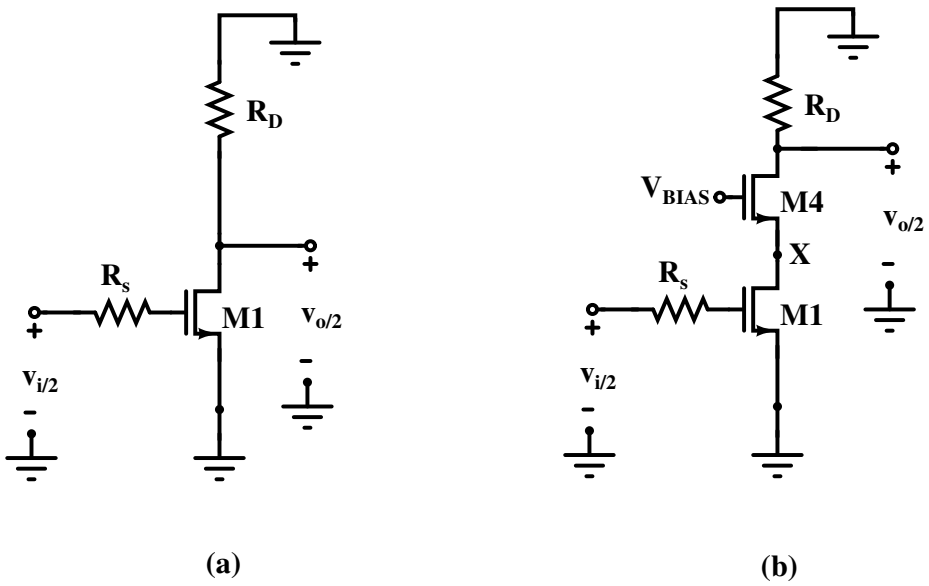

Figure 3.3: (a) Source-coupled differential pair ac half circuit. (b) Source-coupled differential pair ac half circuit with cascode transistor.

Unfortunately, the cascode technique has a few disadvantages: (1) the cascode transistor M_4 introduces a high frequency pole which can offset some of the bandwidth gained with this

technique and (2) the cascode transistor reduces the voltage headroom, which is a concern in low-voltage designs.

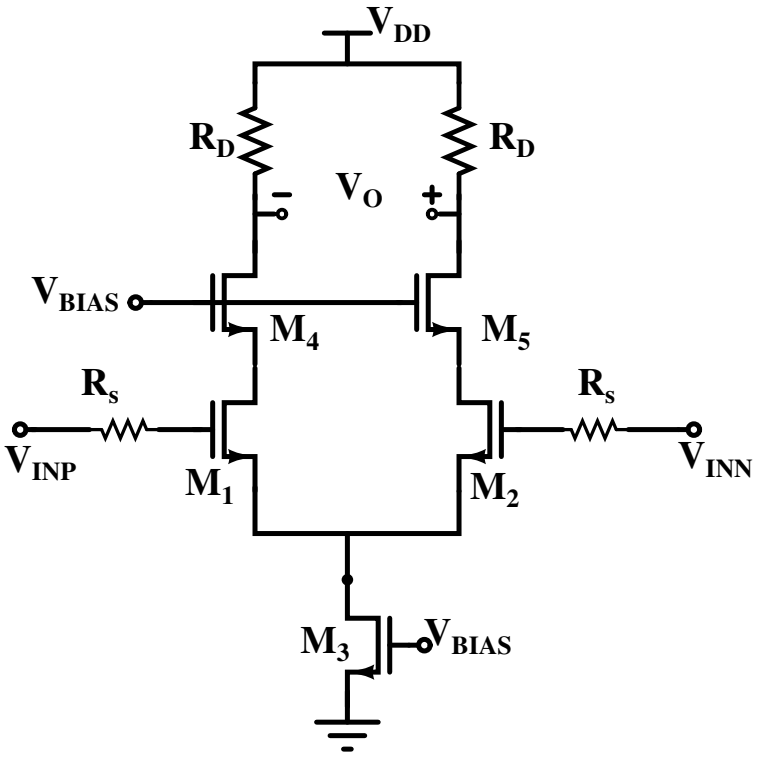

Figure 3.4: Schematic of a source-coupled differential pair with cascode transistor.

3.1.3 Negative Miller-capacitance

The previous subsection explained that by adding cascode transistors in the source-coupled differential pair we can reduce the input capcitance of the stage. This reduces the loading of the previous stage and thus helps to improve the amplifier bandwidth. Another method to reduce the input capacitance of the stage is by placing a negative capacitance in parallel with it. The net effect is a reduction in the input capacitance of the stage which results in an improved amplifier bandwidth. One way to create a negative capacitance is by exploiting the Miller-effect. Fig. 3.5 shows two consecutive stages in a multistage amplifier. The effective input capacitance seen at the input of the first stage in Fig. 3.5 is given by

$$C_{in,x} = C_{p,x} + (1 - A)C_{f,x}. \tag{3.4}$$

But if $A > 1$ the Miller capacitance $(1 - A)C_{f,x}$ becomes negative and reduces the effective input capacitance $C_{in,x}$ of the first stage. Fig. 3.6 shows how this idea can be applied to

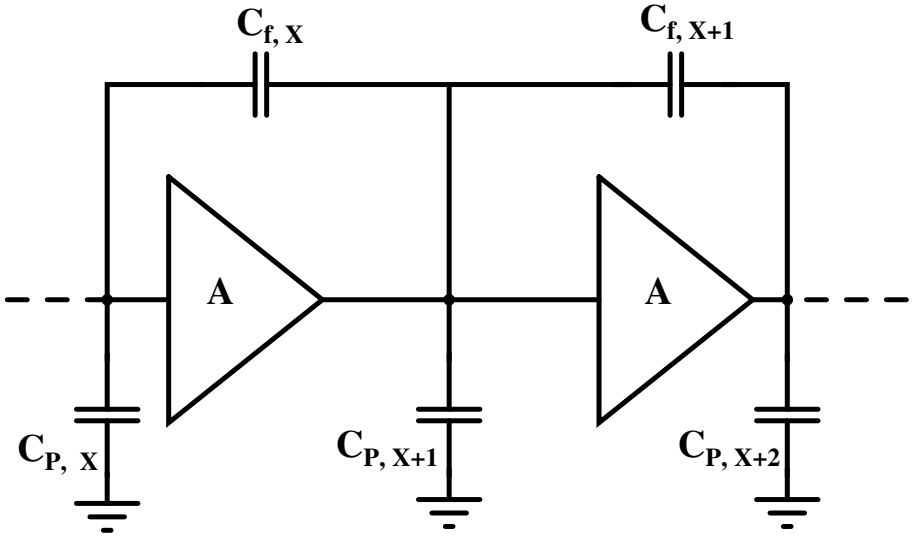

Figure 3.5: Implementation of the negative capacitors, making use of Miller-effect.

reduce the input capacitance of a differential stage. References [6, 7] present wideband amplifiers which utilize this technique to improve the amplifier bandwidth.

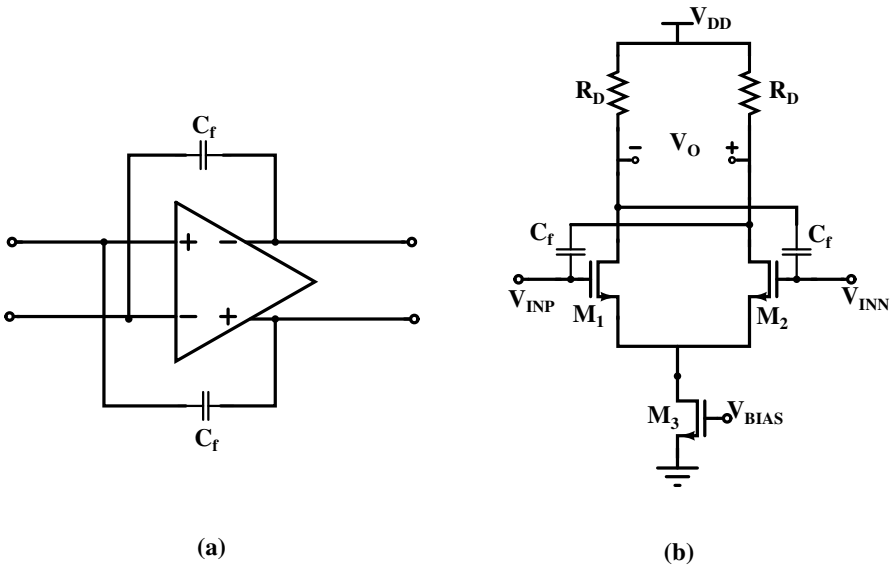

Figure 3.6: (a) Block diagram representation of negative Miller capacitance in a differential stage. (b) Circuit realization of (a).

3.1.4 Capacitive degeneration

Another method to achieve a broadband response is to degenerate the transistors in a differential pair such that the effective transconductance of the circuit G_m increases at high frequencies thereby compensating for the gain roll-off due to the pole at the output node.

Such an arrangment is shown in Fig. 3.7.

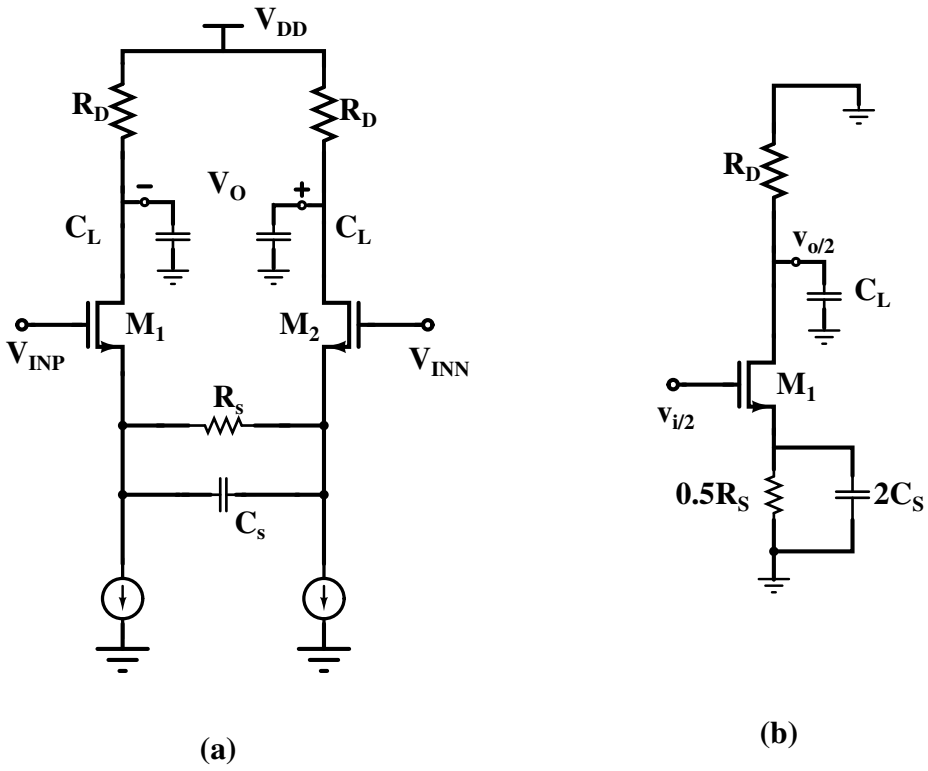

Figure 3.7: (a) Differential pair with capacitive degeneration. (b) AC half-circuit of (a).

Using the half-circuit from Fig. 3.7 the circuit transconductance can be expressed as [9]

$$G_m = \frac{g_m\left(R_sC_ss+1\right)}{R_sC_ss+1+g_m\frac{R_s}{2}}. \tag{3.5}$$

From 3.5 notice that the circuit transconductance G_m contains a zero z_1 and pole p_2 at frequencies

$$z_1 = \frac{1}{R_sC_s},\ and \tag{3.6}$$

$$p_2 = \frac{1+g_m\frac{R_s}{2}}{R_sC_s}. \tag{3.7}$$

If the zero z_1 cancels the pole $p_1 = \frac{1}{R_DC_L}$ at the drain node, then the amplifier's bandwidth can be extended to pole $p_2 = \frac{1+g_m\frac{R_s}{2}}{R_sC_s}$. However, this increase in amplifier bandwidth is obtained at the cost of a proportional reduction in the DC voltage gain $A_v = \frac{g_mR_D}{1+g_m\frac{R_s}{2}}$. Fig. 3.8 shows the variation in circuit transconductance G_m and the voltage gain A_v as a function of frequency. In a variation of this pole-zero cancellation technique explained above, if the zero is pushed slightly towards lower frequency (by making C_s large) the frequency response will show a peaking. This technique is called source-peaking. Note, however that C_s should not me made too large bacause the resulting gain peaking can distort the overall frequency response of the multistage amplifier. Other advantages of using this method include controlling

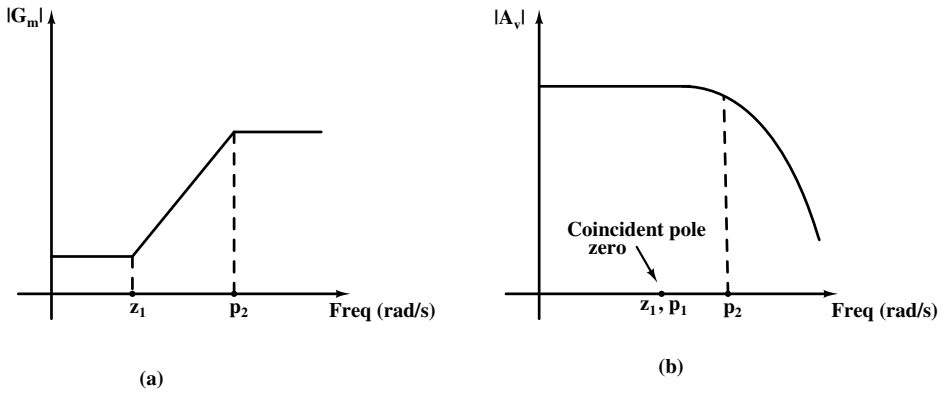

Figure 3.8: Variation of (a) Circuit transconductance G_m. (b) Voltage gain A_v with frequency (rad/s).

the stage gain by varying R_s and reducing the input capacitance of the stage.

3.1.5 Inductive peaking

From the above explanation, it is clear that the bandwdith of the amplifier is limited by the capacitive loading (usually at the output node). For a typical common-source amplifier the output pole is at $p_O = \frac{1}{R_D C_L}$. However if we include an inductor at the output node, then it is possible to suppress the affect of the load capacitance C_L and thus increase the bandwidth of the amplifier. This is the idea behind inductive peaking.

In order to understand inductive peaking, lets consider a common-source stage (shown in Fig. 3.9(a)) with an inductor L_P added in series with R_D. The equivalent small-signal circuit is shown in Fig. 3.9(b). For simplicity the parasitic capacitances of the transistor C_{gd} and C_{gs} are ignored. The equivalent impedance of the RLC network can now be written as

$$Z(s) = (sL_P + R_D) \,||\frac{1}{sC_L} = \frac{R_D\left[s(L_P/R_D)+1\right]}{s^2 L_P C_L + sR_D C_L + 1}. \tag{3.8}$$

Note that there is a zero and two poles in the expression of $Z(s)$. The voltage gain of the amplifier is

$$\frac{v_O(s)}{v_i(s)} = -g_m Z(s) = -\frac{g_m R_D\left[s(L_P/R_D)+1\right]}{s^2 L_P C_L + sR_D C_L + 1}. \tag{3.9}$$

Thus zero in the voltage gain expression can be used to increase the bandwidth of the amplifier.

Unfortunately there is no single correct value of L_P given R_D and C_L. Let us now define a factor m as the ratio of $R_D C_L$ and L_P/R_D

$$m = \frac{R_D C_L}{\frac{L_P}{R_D}}. \tag{3.10}$$

There are different values of m depending on how much increase in bandwidth is desired (and how much peaking in frequency response can be tolerated). Table 9.1 in [10] tabulates

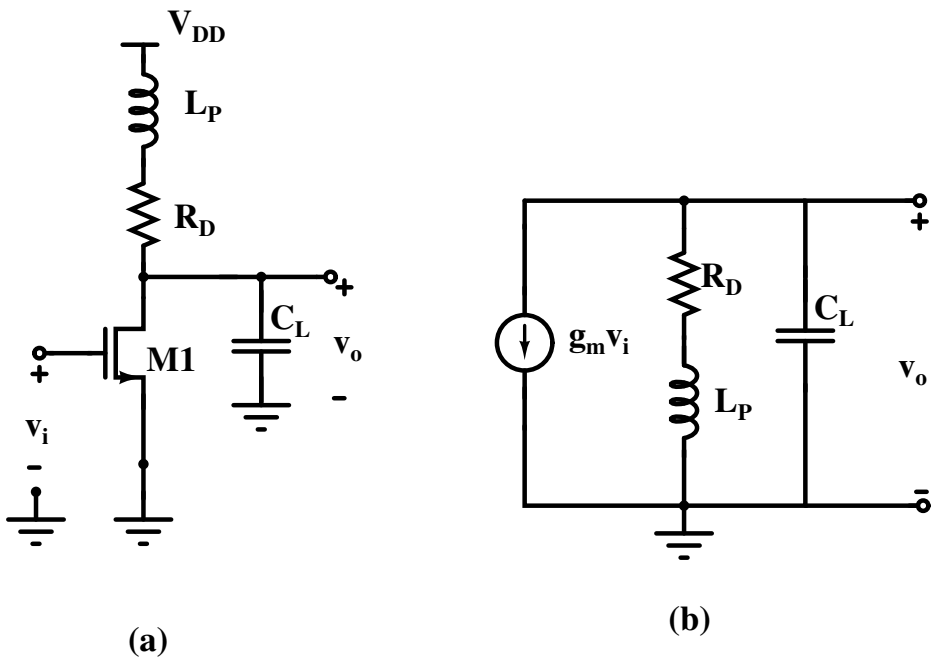

Figure 3.9: (a) Common-source stage with inductive peaking. (b) Equivalent small-signal circuit of (a).

the different values of m corresponding to the different bandwidths desired. [7] is an example of work that uses inductive peaking to increase the bandwidth of the amplifier. The inductor can be realized as an on-chip spiral inductor or a bond-wire inductor. However on-chip spiral inductors require a large silicon area especially in balanced circuits. An alternative method is to boost the inductance of smaller inductors with a transistor [11].

3.1.6 Cherry-Hooper amplifier

It is well known that negative feedback can be used to trade the high imprecise gain of the amplifier for a much lower but precise gain. Moreover the use of feeback can alter the effective input and output resistance of the amplifier and thus help to improve the amplifier response at high frequencies. In [12] it is shown that using alternate series- and shunt feedback stages results in the simplification of multistage amplifier design. This is because the interaction between the stages is reduced due to the use of feedback. One such amplifier known as the Cherry-Hooper amplifier has been widely used for designing amplifiers with high bandwidths. References [5, 13, 14, 15] are examples of designs that employ the Cherry-Hooper amplifier to create broadband amplifier responses.

The high frequency behavior of the Cherry-Hooper amplifier can be understood by using Fig. 3.10. The small-signal resistance seen at nodes X and Y is about $1/g_{m2}$. The pole frequencies at these nodes will be on the order of $w_{p,X} \approx g_{m2}/C_X$ and $w_{p,Y} \approx g_{m2}/C_Y$, which are at high frequency (typically g_{m2} is few mS). These approximations while intuitively appealing are inaccurate because at high frequencies C_Y shunts the output node which lowers the loop gain resulting in an increase in the impedance seen at node X. The accurate transfer

function of Cherry-Hooper amplifier is given in [5].

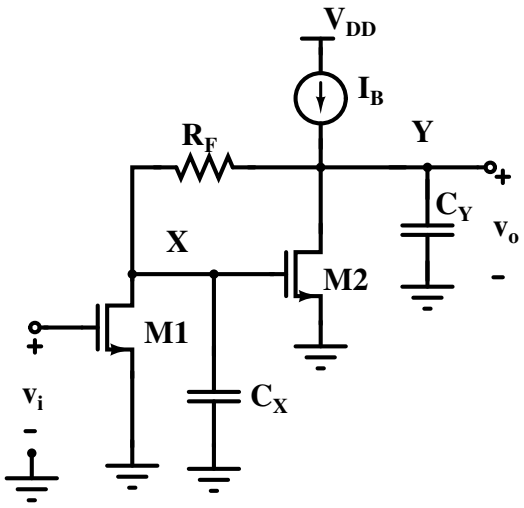

Figure 3.10: Simplified single-ended Cherry-Hooper amplifier.

Although Cherry-Hooper amplifier allows high speed designs, it faces difficulties at low supply voltages [5]. A balanced form of Cherry-Hooper amplifier is shown in Fig. 3.11.

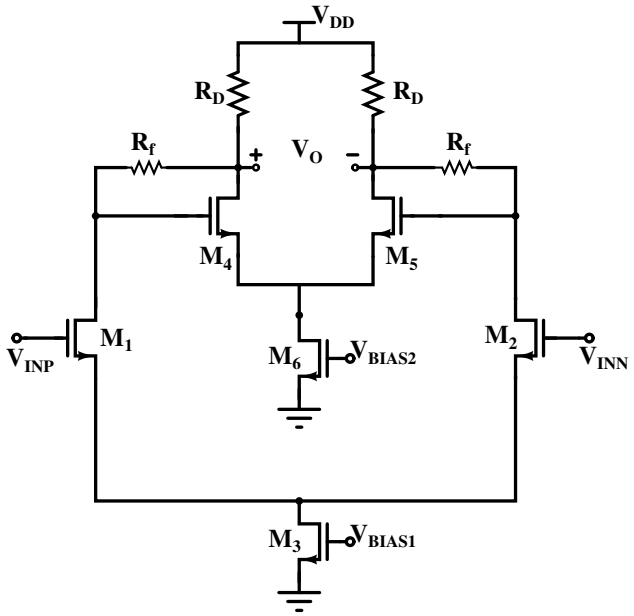

Figure 3.11: Balanced Cherry-Hooper amplifier.

3.2 DC-offset compensation techniques

This section focuses on the different continuous-time analog methods that can be used for DC-offset compensation in radio receivers. DC-offset compensation is necessary in receivers because the DC offsets at the output of the downconversion mixer are practically several millivolts. Without adequate DC-offset compensation these large DC offsets will saturate the back-end of the receiver due to the high gain at baseband [16]. The following subsections describe three techniques that are commonly used for DC-offset compensation.

3.2.1 AC coupling

The AC coupling technique can be used to filter out the DC-offsets at the output. A circuit that performs AC coupling is shown in Fig. 3.12. The transfer function of the circuit is

$$H_{AC}(s) = \frac{sRC}{1 + sRC}. \tag{3.11}$$

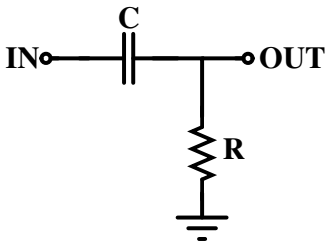

Figure 3.12: AC Coupling.

Note that the stage following the ac coupling must have a high-impedance input since it will be in parallel with the resistor R. In all-MOS impelementations the resistor R is replaced by a MOS transistor operating in triode region [17]. However for very low cut-off frequencies of $H_{AC}(jw)$, the product of RC must be high. This means that a large capacitor must be used which increases the silicon area for AC coupling, particularly in balanced circuits where two such large capacitors are needed. Note that the parasitics associated with the capacitor C (equivalent series resistance R_{ESR}) and the input capacitance of the next stage result in a loss and a shift in the -3 dB frequency of the high pass filter (formed as a result of the AC coupling) [16].

3.2.2 DC feedback loop

The block diagram of a DC feedback loop is shown in Fig. 3.13. The feedback loop transfer function $H_{FB}(s)$ for a single-pole low-pass system is

$$H_{FB}(s) = \frac{A_{FB}}{1 + \frac{s}{w_{FB}}}, \tag{3.12}$$

where A_{FB} is the DC gain of the feeedback loop and w_{FB} is the -3 dB frequency of the feedback loop. The overall transfer function of the circuit $H_{DC}(s)$ is given by

$$H_{DC}(s) = \frac{V_{OUT}(s)}{V_{IN}(s)} = \frac{A_O}{1 + A_O H_{FB}(s)} = \frac{A_O}{1 + A_O A_{FB}} . \frac{1 + \frac{s}{w_{FB}}}{1 + \frac{s}{(1+A_O A_{FB}) w_{FB}}}. \tag{3.13}$$

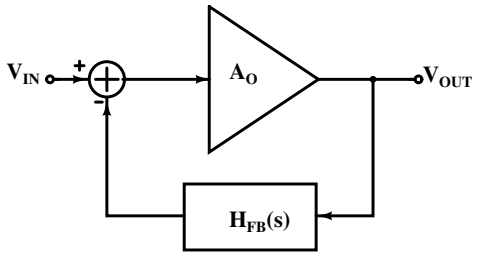

Figure 3.13: DC Feedback Loop.

Assuming that the loop gain $A_O A_{FB} >> 1$, (3.13) can be approximated as

$$H_{DC}(s) \approx \frac{1}{A_{FB}} . \frac{1 + \frac{s}{w_{FB}}}{1 + \frac{s}{(A_O A_{FB}) w_{FB}}}. \tag{3.14}$$

Note that the system has a DC gain of $\frac{1}{A_{FB}}$ and a left-half plane zero at w_{FB}. The low-pass response of the feedback loop transfer function $H_{FB}(s)$ now creates an overall high-pass response with a -3 dB cut-off frequency at $(A_O A_{FB})\, w_{FB}$. It should be noted that the corner frequency has moved to a higher value by the factor $A_O A_{FB}$. Thus in order to keep the -3 dB cut-off frequency of the overall response below the desired signal band, the -3 dB cut-off frequency of the feedback loop w_{FB} has to be very low, resulting in a large silicon area [18]. Moreover, if the gain of the forward amplifier A_O is varied the -3 dB cut-off frequency of the overall response also changes. Thus it is important to check that the -3 dB cut-off frequency of the overall response meets the design goals at all gain settings. Another important thing to note is that the DC feedback loop does not remove the DC offsets of the feedback loop i.e. $H_{FB}(s)$. The DC offset at the output V_{OUT} is approximately equal to the input-referred DC offset of $H_{FB}(s)$ [16].

3.2.3 Feedforward DC offset removal technique

A feedforward DC offset removal technique that has been used in [19, 20] is shown in Fig. 3.14. The DC offset in the input signal is isolated using the low pass filter RC. This DC offset is a common-mode signal for the amplifier A_O. If A_O uses a differential pair as the input stage then only a very small portion of the input DC offset passes through to the output due to the high common-mode rejection ratio (CMRR) of the differential pair. In this way a high pass filter is created from the input V_{IN} to the output V_{OUT}. The -3 dB frequency of the high pass filter is $1/(RC)$. However it should be noted that at the output V_{OUT} there is a DC offset component due to the amplifier A_O.

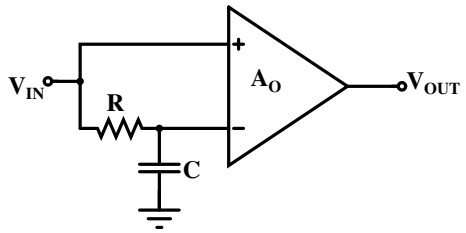

Figure 3.14: Feedforward DC offset removal circuit.

3.3 Summary

This chapter described different circuits and techniques that can be used to design stages with very high bandwidths. Technqiues like using a cascode transistor or negative Miller capacitance can be used to suppress the input capacitance of the stage. Moreover, circuits which use capacitive degeneration and inductive peaking can also provide broadband responses. Circuits using feedback to achieve wide bandwidth like Cherry-Hooper amplifier were also included in this chapter. Important limitations of these circuits and techniques were also pointed out in the explanation.

The second half of the chapter focussed on the DC-offset compensation methods. Three techniques (AC coupling, DC feedback loop and Feedforward DC offset removal method) were presented. The fundamental ideas behind these technqiues and their merits and demerits were also explained in this chapter.

After presenting an overview of the main building blocks of the VGA in this chapter, the next chapter is related solely to the design of the amplifier itself.

Chapter 4

VGA design and simulation results

In the previous chapters the fundamental ideas related to the design of multistage amplifiers were presented. It was concluded that the best figure-of-merit (FOM) was obtained when two stages are included in the variable gain section of the amplifier. Moreover, by placing a high gain low-noise stage as the first stage in the amplifier, the impact of the noise of the subsequent stages (in the variable gain section) on the overall noise performance of the VGA can be further reduced. The AC coupling removes any DC offset coming from the RF front. In addition to this, a DC feedback loop was added to compensate for the DC-offset originating in the first stage of the VGA. The block diagram in Fig. 4.1 represents the design philosophy of the VGA. In this chapter the design of the different blocks in the

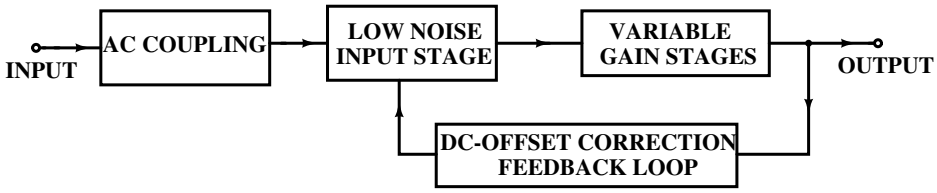

Figure 4.1: Design philosophy of VGA.

VGA is presented. The equations governing the small signal and the noise performance of each stage will be derived. Moreover the important simulation results of each stage i.e. the voltage gain versus frequency curve, noise and power consumption will be given.

4.1 VGA stage 1

As indicated earlier, the first stage of the VGA should be a high-gain, low-noise stage. Moreover the -3 dB bandwidth of this stage has to be much higher than the overall bandwidth of the VGA. Based on these requirements, a resistively loaded source-coupled differential pair was chosen. The schematic of the circuit is shown is Fig. 4.2. M_{1a} and M_{1b} form the source-coupled pair with resistors R_{D1a} and R_{D1b} as the load. Transistor M_2 acts as a tail current source. Resistor R_{g1} represents the resistance of the driving source. It has been indicated

in chapter 3 that the Miller-effect increases the input capacitance and the pole formed by R_{g1} and the total input capcitance of the stage limit the -3 dB bandwidth of the amplifier. In order to suppress the Miller-effect and increase the bandwidth of the stage, negative Miller capacitors (C_{c1a} and C_{c1b}) have been used. These capacitors were chosen to push the input pole to higher frequency. The values of these capacitors were found using simulations. C_{L1} represents the capacitive loading at the output V_{OUT1}. It includes the intrinsic capacitance of the transistor M_{1a}, the wiring capacitance and the input capacitance of the next stage.

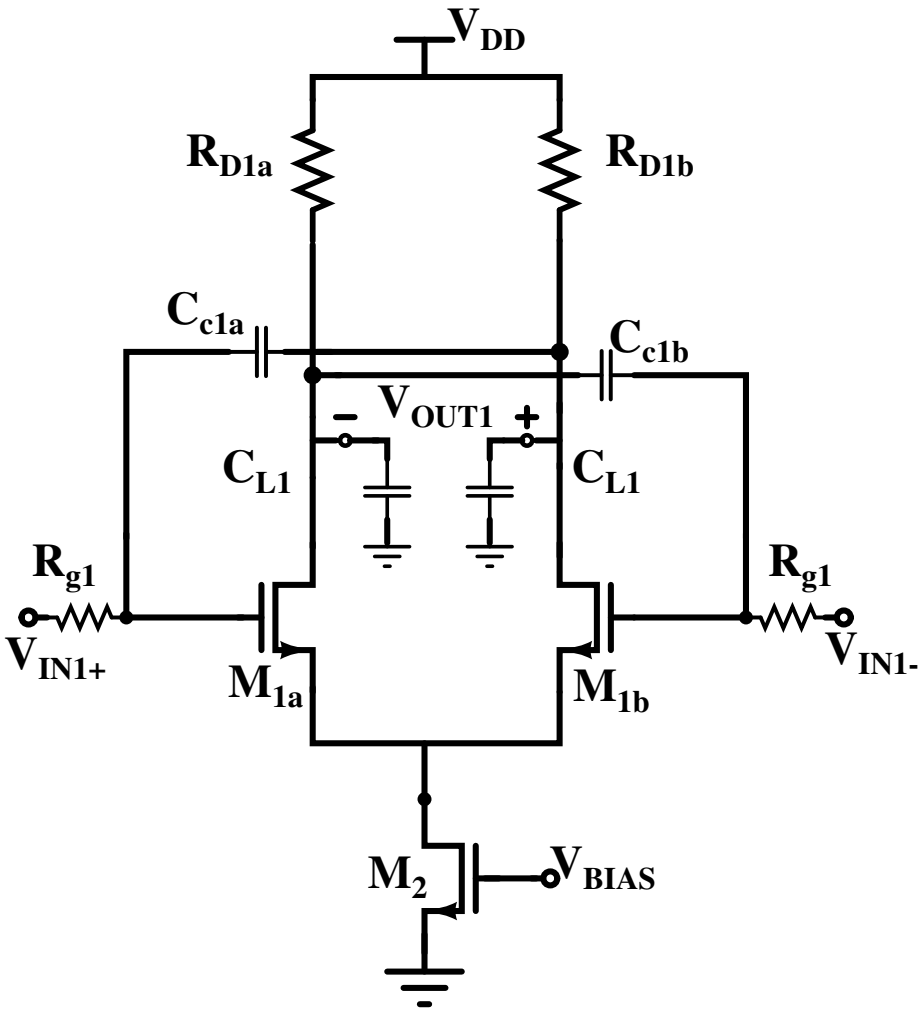

Figure 4.2: Schematic of VGA stage 1.

4.1.1 Small-signal analysis

The equivalent small-signal circuit for stage 1 is shown in Fig. 4.3. Because of the balanced structure of stage1 half-circuit analysis can be used. Since negative Miller capacitors (C_{c1a} and C_{c1b}) cancel out the gate-drain capacitance C_{gd} of the transistor M_{1a} and M_{1b}, they have been ignored in the equivalent small-signal circuit. The small-signal voltage v_{out1} can

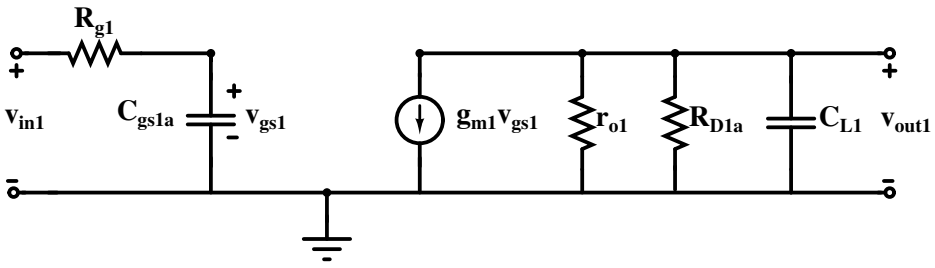

Figure 4.3: Equivalent small-signal circuit using the half-circuit concept.

be expressed as

$$v_{out1}(s) = -g_{m1}v_{gs1}(s)\left(r_{o1}||R_{D1a}||\frac{1}{sC_{L1}}\right),$$

where r_{o1} is the output resistance of the transistor. Assuming that $r_{o1} >> R_{D1a}$, v_{out1} can be written as

$$v_{out1}(s) = -g_{m1}v_{gs1}(s)\left(R_{D1a}||\frac{1}{sC_{L1}}\right),$$

$$v_{out1}(s) = -g_{m1}v_{gs1}(s)\left[\frac{R_{D1a}}{1+sR_{D1a}C_{L1}}\right]. \tag{4.1}$$

Using the voltage division formula, v_{gs1} can be written as

$$v_{gs1}(s) = v_{in1}(s)\left[\frac{1/sC_{gs1a}}{1/sC_{gs1a}+R_{g1}}\right],$$

$$v_{gs1}(s) = v_{in1}(s)\left[\frac{1}{1+sR_{g1}C_{gs1a}}\right]. \tag{4.2}$$

Substituting $v_{gs1}(s)$ from (4.2) in to (4.1)

$$v_{out1}(s) = -g_{m1}v_{in1}(s)\left[\frac{1}{1+sR_{g1}C_{gs1a}}\right]\left[\frac{R_{D1a}}{1+sR_{D1a}C_{L1}}\right],$$

Hence, the voltage gain of stage 1 $A_{v1}(s)$ can be written as

$$A_{v1}(s) = \frac{v_{out1}(s)}{v_{in1}(s)} = -\frac{g_{m1}R_{D1a}}{(1+sR_{g1}C_{gs1a})(1+sR_{D1a}C_{L1})}. \tag{4.3}$$

The DC voltage gain of stage 1 $A_{v1,0}$ and the two poles are given as

$$A_{v1,0} = -g_{m1}R_{D1a}, \tag{4.4}$$

$$p_1 = \frac{1}{R_{D1a}C_{L1}}, and \tag{4.5}$$

$$p_2 = \frac{1}{R_{g1}C_{gs1a}}. \tag{4.6}$$

Notice that typically p_1 forms the dominant pole because $C_{L1} > C_{gs1a}$. Also for high gain R_{D1a} should be increased but for high bandwidth R_{D1a} should be decreased. Thus there is an

optimum value of R_{D1a} that will staisfy both the gain and bandwidth requirements and in the VGA design, simulations (using ELDO) were used to determine it.

4.1.2 Noise analysis

As explained earlier, the noise performance of the overall VGA depends on the noise of the stage 1. In this subsection an expression is derived for the equivalent input noise voltage of the amplifier for low frequencies. For this analysis R_{g1} is ignored as it is a part of the preceding stage. Fig 4.4 shows half of the amplifier small-signal circuit including the dominant noise sources.

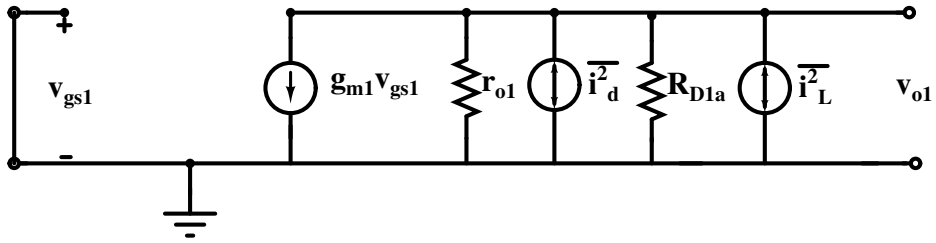

Figure 4.4: Half of the VGA stage 1 small-signal circuit including the dominant noise sources.

The mean square thermal noise current due to R_{D1a} is given as [21]

$$\overline{i_L^2} = 4kT\Delta f\left(\frac{1}{R_{D1a}}\right). \tag{4.7}$$

For MOS transistor the flicker and thermal noise can be lumped in to one noise generator $\overline{i_d^2}$ as [21]

$$\overline{i_d^2} = \left[4kT\left(\frac{2}{3}g_{m1}\right)(1+\eta) + \frac{(KF)\,I_{D1a}}{fC_{OX}L^2}\right]\Delta f, \tag{4.8}$$

where

k =Boltzmann's constant (1.38x10^{-23} J/K),

T =Absolute temperature (kelvin),

Δf = a small bandwidth (typically 1 Hz) at frequency f,

$\eta = \frac{g_{mbs}}{g_m}$,

KF =Flicker noise coefficient,

f =Frequency (Hz).

Since $v_{gs1} = 0$, the dependent source $g_{m1}v_{gs1}$ also becomes zero. Thus output noise voltage at node v_{o1} can be written as

$$\overline{v_{o1}^2} = \left[\overline{i_d^2} + \overline{i_L^2}\right](r_{o1}||R_{D1a})^2.$$

Assuming that $r_{o1} >> R_{D1a}$, the above equation can be written as

$$\overline{v_{o1}^2} = \left[\overline{i_d^2} + \overline{i_L^2}\right] R_{D1a}^2. \tag{4.9}$$

The output noise voltage at node v_{o2} (the other output terminal) is

$$\overline{v_{o2}^2} = \overline{v_{o1}^2} = \left[\overline{i_d^2} + \overline{i_L^2}\right] R_{D1a}^2. \tag{4.10}$$

The mean square differential noise voltage between terminals v_{o1} and v_{o2} at low frequency is

$$\begin{aligned} \overline{v_o^2} &= \overline{|v_{o1} - v_{o2}|^2}, && (4.11)\\ &= \overline{v_{o1}^2} + \overline{v_{o2}^2} - 2\overline{v_{o1}v_{o2}}, \\ &= \overline{v_{o1}^2} + \overline{v_{o2}^2} - 2C_{12}|\overline{v_{o1}^2}.\overline{v_{o2}^2}|^{1/2} && (4.12) \end{aligned}$$

where C_{12} is a measure of the correlation between the noise voltages at nodes v_{o1} and v_{o2} and always lies in the range $-1 \leq C_{12} \leq 1$. Using $C_{12} = -1$ as the noise voltages are anti-phase and fully correlated [14],

$$\overline{v_o^2} = 4\overline{v_{o1}^2} = 4R_{D1a}^2 \left[\overline{i_d^2} + \overline{i_L^2}\right]. \tag{4.13}$$

The input referred differential noise voltage can be obtained by dividing (4.13) by the square of low-frequency differential gain ($g_{m1}^2 R_{D1a}^2$)

$$\begin{aligned} \overline{v_{eq}^2} &= \frac{\overline{v_o^2}}{g_{m1}^2 R_{D1a}^2}, && (4.14)\\ &= \frac{4R_{D1a}^2 \left[\overline{i_d^2} + \overline{i_L^2}\right]}{g_{m1}^2 R_{D1a}^2}, \\ &= \frac{4\overline{i_d^2}}{g_{m1}^2} + \frac{4\overline{i_L^2}}{g_{m1}^2}. && (4.15) \end{aligned}$$

Substituting the values of $\overline{i_d^2}$ and $\overline{i_L^2}$ from (4.32) and (4.7) in to (4.15),

$$\overline{v_{eq}^2} = 4\left[\frac{8kT\left(1+\eta\right)}{3g_{m1}} + \frac{KF}{2fC_{OX}WLK'} + \frac{4kT}{g_{m1}^2 R_{D1a}}\right]\Delta f, \tag{4.16}$$

where
$C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}} =$ Capacitance per unit area of the gate oxide, and
$K' =$ Transconductance parameter ($\mu A/V^2$).

(4.16) shows that the equivalent input noise voltage can be lowered by increasing g_{m1} and the size of the transistor (width W and channel length L). However increasing the size of the transistor also increases the intrinsic capacitances (C_{db} and C_{gs}) which may limit

the amplifier bandwidth. Thus there is a trade-off between the noise performance and the bandwidth of the stage 1.

4.1.3 Common-mode feedback

The output common-mode voltage of the differential pair is sensitive to mismatches and component variations. To set the output common-mode voltage to a desired DC voltage, a negative feedback loop was added as shown in Fig. 4.5. Resistors R_{CM1} and R_{CM2} were used for sensing the output common-mode voltage (V_{CMFB}) which was then compared to a reference voltage (V_{CM}) using the common-mode feedback amplifier (CMFB amplifier). CMFB amplifier was a single-ended differential pair as shown in Fig. 4.5. Because it was a negative feedback loop, its stability was ensured by using capacitor C_f.

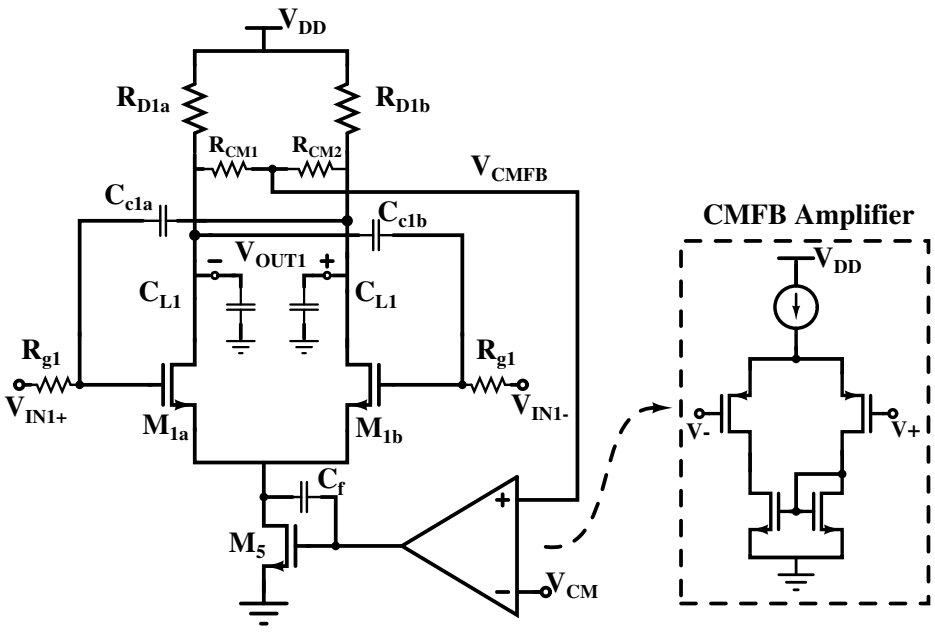

Figure 4.5: Schematic of VGA 1 with common-mode feedback included.

In order to show the need for C_f, the common-mode feedback loop gain was first simulated without C_f and it was found that feedback loop was unstable (poor phase margin) (see Fig. 4.6). However, with C_f the phase margin improves, making the common-mode feedback loop stable as shown in Fig. 4.7.

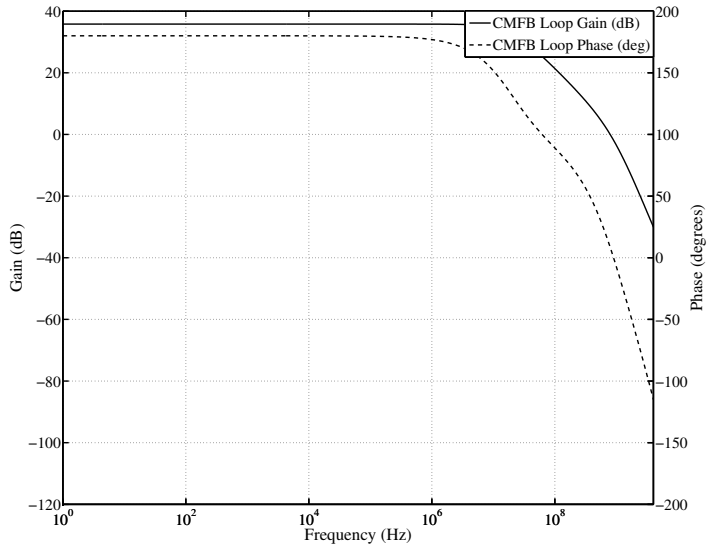

Figure 4.6: Simulated CMFB loop gain (magnitude and phase) without C_f .

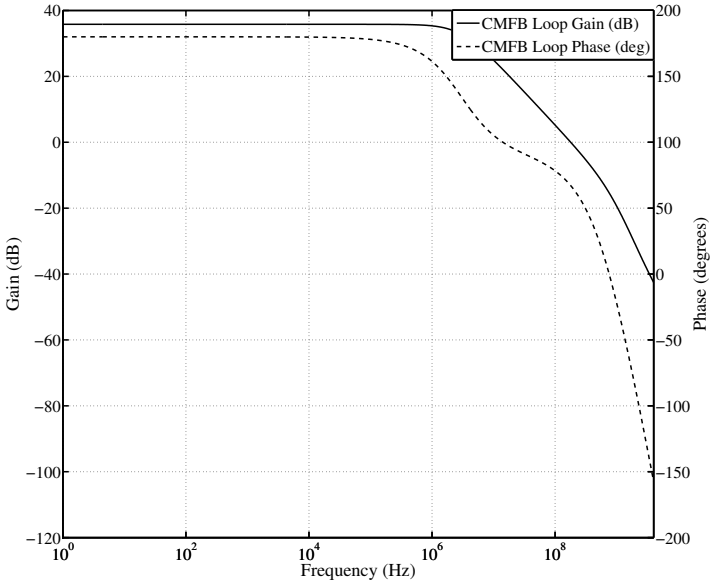

Figure 4.7: Simulated CMFB loop gain (magnitude and phase) with C_f included.

4.1.4 Simulation results

Fig. 4.8 plots the gain of stage 1 versus the frequency. Note that the low-frequency gain is about 13.3 dB instead of 14 dB. This slight reduction in the gain is because the common-mode sensing resistors (R_{CM1} and R_{CM2}) are in parallel with load resistors (R_{D1a} and R_{D1b}). The -3 dB bandwidth of stage 1 is more than 1.6 GHz. Table 4.1 summarizes the performance of the stage 1.

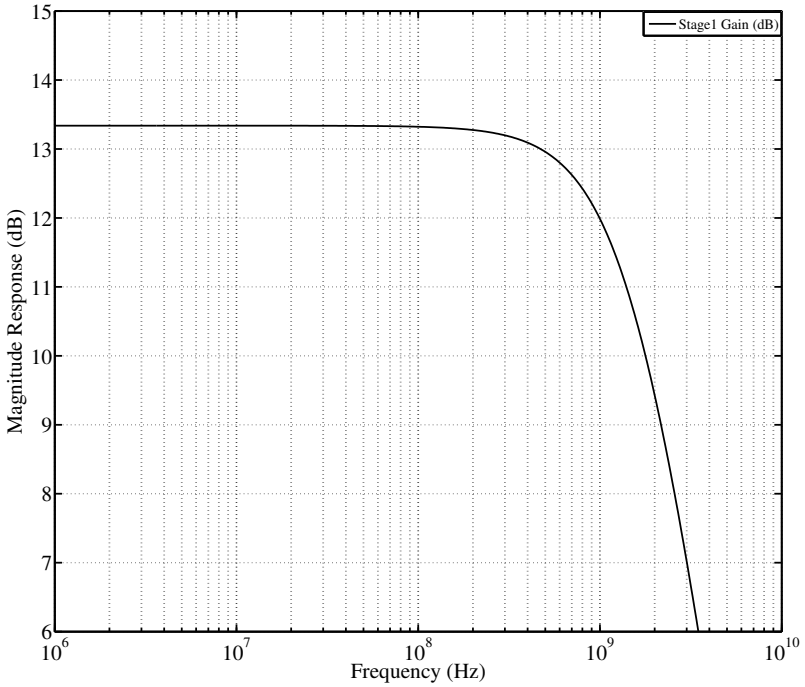

Figure 4.8: Simulated gain (dB) of stage 1 of VGA versus frequency (Hz).

Table 4.1: VGA Stage 1 Performance summary.

-3dB frequency	1.65 GHz
Gain	13.3 dB
Input-referred noise	0.083 mV_{rms}
Power consumption	2.08 mW

4.2 VGA stage 2 and stage 3

It has already been shown that using two stages in the variable gain section of the amplifier gives the best figure-of-merit (minimum input-referred noise and gain-bandwidth product). For this purpose, a capacitively degenerated source-coupled differential pair is used in these stages. The schematic of the circuit is shown is Fig. 4.9. M_{2a} and M_{2b} form the source-coupled pair with resistors R_{D2a} and R_{D2b} as the load. R_S and C_S are the degeneration resistor and capacitor. Transistors M_{6a} and M_{6b} act as tail current sources. Since stage 2 will be DC coupled with stage1, the gate voltage of M_{2a} and M_{2b} was chosen to be 0.7 V, same as that at the output of the stage 1. Resistor R_{g2} represents the resistance of the driving source (in the full integrated VGA it will be the output resistance of the stage 1). Just like stage 1, negative Miller capacitors (C_{c2a} and C_{c2b}) are used to suppress the Miller-capacitance. C_{L2} is the capacitive loading at the output V_{OUT2}. It includes the intrinsic capacitance of the transistor M_{2a}, the wiring capacitance and the input capacitance of the next stage.

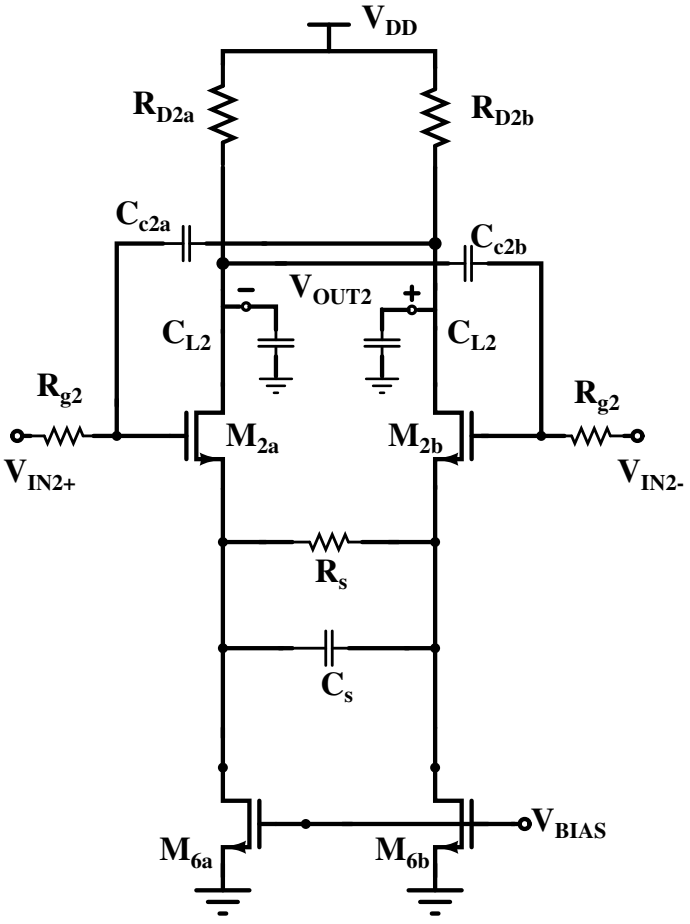

Figure 4.9: Schematic of VGA stage 2 and stage 3.

4.2.1 Small-signal analysis

The equivalent small-signal circuit for stage 2 is shown in Fig. 4.10. Because of the balanced structure of stage2, half-circuit analysis can be used. Since negative Miller capacitors (C_{c2a} and C_{c2b}) cancel out the gate-drain capacitance C_{gd} of the transistor M_{2a} and M_{2b} , they have been ignored in the equivalent small-signal circuit. Moreover the output resistance of the transistor r_{o2} has been ignored.

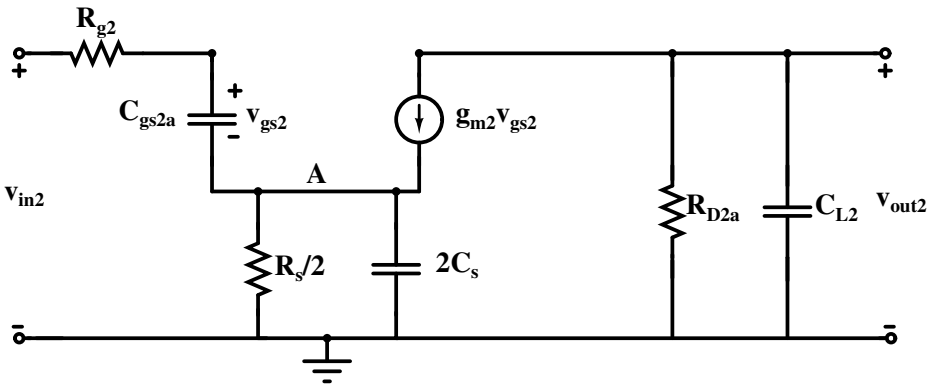

Figure 4.10: Equivalent small-signal circuit using the half-circuit concept.

The current through C_{gs2a} is

$$i_{gs2a} = sC_{gs2a}v_{gs2}. \tag{4.17}$$

The total current driving the source degeneration impedance at node A is

$$i_s = i_{gs2a} + g_{m2}v_{gs2}, \tag{4.18}$$

$$i_s = \left(sC_{gs2a} + g_{m2}\right) v_{gs2}. \tag{4.19}$$

The voltage at the input v_{in2} can be expressed as

$$v_{in2}(s) = i_{gs2a}R_{g2} + v_{gs2} + i_s\left(\frac{0.5R_S}{sR_SC_S + 1}\right). \tag{4.20}$$

Using the values of i_{gs2a} and i_s from above equations, v_{in2} becomes

$$v_{in2}(s) = \left(sR_{g2}C_{gs2a} + 1\right) v_{gs2} + \frac{0.5R_S\left(sC_{gs2a} + g_{m2}\right)}{sR_SC_S + 1}v_{gs2},$$

$$v_{in2}(s) = \left[\frac{s^2R_SC_SR_{g2}C_{gs2a} + s\left(R_SC_S + R_{g2}C_{gs2a} + 0.5R_SC_{gs2a}\right) + \left(1 + 0.5R_Sg_{m2}\right)}{sR_SC_S + 1}\right] v_{gs2}. \tag{4.21}$$

Writing the current equation at the output node gives

$$v_{out2}(s)\left(\frac{sR_{D2a}C_{L2}+1}{R_{D2a}}\right)+g_{m2}v_{gs2}=0,$$

$$v_{out2}(s)=\left[\frac{-g_{m2}R_{D2a}}{sR_{D2a}C_{L2}+1}\right]v_{gs2}. \tag{4.22}$$

From (4.21) substituting the value of v_{gs2} in to (4.22) gives

$$\frac{v_{out2}(s)}{v_{in2}(s)}=\left[\frac{-g_{m2}R_{D2a}}{sR_{D2a}C_{L2}+1}\right] \left[\frac{sR_SC_S+1}{s^2R_SC_SR_{g2}C_{gs2a}+s\left(R_SC_S+R_{g2}C_{gs2a}+0.5R_SC_{gs2a}\right)+\left(1+0.5R_Sg_{m2}\right)}\right]. \tag{4.23}$$

Hence the voltage gain of stage 2 (and stage 3) $A_{v2}(s)$ is given as

$$A_{v2}(s)=\left[\frac{-g_{m2}R_{D2a}}{sR_{D2a}C_{L2}+1}\right] \left[\frac{sR_SC_S+1}{s^2R_SC_SR_{g2}C_{gs2a}+s\left(R_SC_S+R_{g2}C_{gs2a}+0.5R_SC_{gs2a}\right)+\left(1+0.5R_Sg_{m2}\right)}\right]. \tag{4.24}$$

Using dominant pole approximation on (4.24), the voltage gain of stage 2 $A_{v2}(s)$ is approximated as

$$A_{v2}(s)\approx A_{v2,0}\left[\frac{\left(\frac{s}{z_1}+1\right)}{\left(\frac{s}{p_1}+1\right)\left(\frac{s}{p_2}+1\right)\left(\frac{s}{p_3}+1\right)}\right],$$

$$A_{v2,0}=-\frac{g_{m2}R_{D2a}}{1+0.5g_{m2}R_S}, \tag{4.25}$$

$$z_1=\frac{1}{R_SC_S}, \tag{4.26}$$

$$p_1=\frac{1}{R_{D2a}C_{L2}}, \tag{4.27}$$

$$p_2=\frac{1+0.5R_Sg_{m2}}{R_SC_S+R_{g2}C_{gs2a}+0.5R_SC_{gs2a}}, \tag{4.28}$$

$$p_3=\left[\frac{1}{R_SC_S}+\frac{1}{R_{g2}C_{gs2a}}+\frac{1}{2R_{g2}C_s}\right]. \tag{4.29}$$

(4.25) shows that the DC gain of stage 2 can be varied by changing the value of R_S. Therefore in the actual design R_S was realized as a cascade connection of nMOS transistors. The effective resistance of the transistors can be changed by changing the voltage V_{gate} (see Fig. 4.11).

Out of the three poles, p_1 is typically at lower frequency and hence limits the -3 dB bandwidth of the stage. This pole can be cancelled by the zero z_1 resulting in a wideband

stage. Since R_S is different for different gain settings, therefore C_S must also be made tunable to ensure proper pole-zero cancellation at all gain settings. In the actual design C_S has been implemented as a *Switchable Capacitor Matrix* as shown in Fig. 4.11.

Similar to stage 1, the output common-mode voltage of stage 2 was kept fixed irrespective of temperature and parameter variations by using a CMFB loop. In this case C_f was used to stabilize the CMFB loop. Fig. 4.11 shows the final schematic of stage 2 (and stage 3).

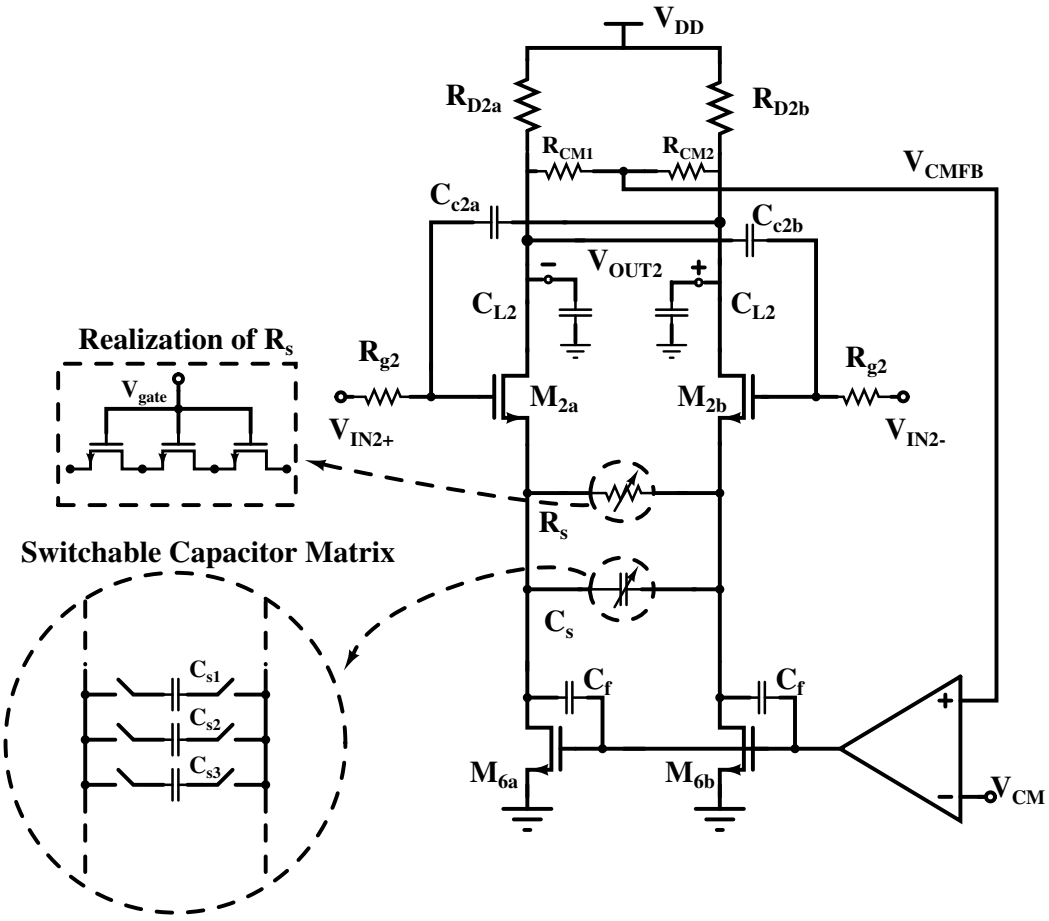

Figure 4.11: Final schematic of VGA stage 2 and stage 3.

4.2.2 Noise analysis

In this subsection an expression is derived for the equivalent input noise voltage of the stage 2 for low frequencies. For this analysis R_{g2} is ignored as it is a part of the preceding stage. Fig 4.12 shows half of the amplifier small-signal circuit including the dominant noise sources. The mean square thermal noise current due to R_{D2a} is given as

$$\overline{i_L^2} = 4kT\Delta f \left(\frac{1}{R_{D2a}}\right). \tag{4.30}$$

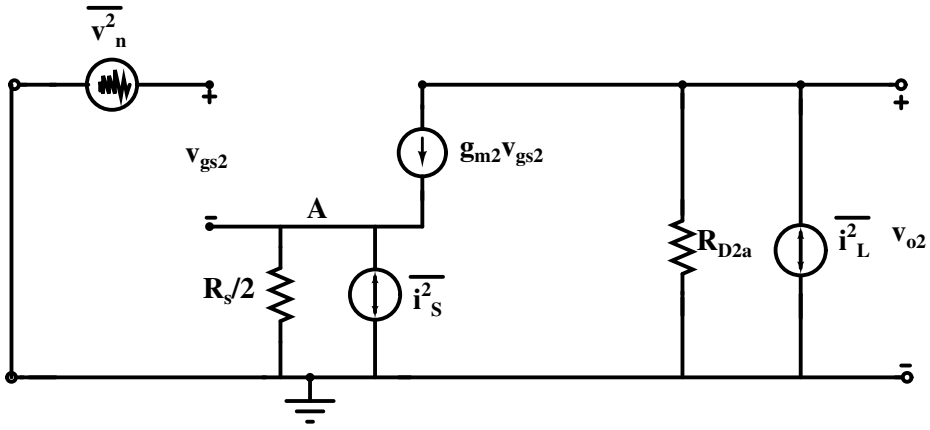

Figure 4.12: Half of the VGA stage 2 small-signal circuit including the dominant noise sources.

The mean square thermal noise current due to R_S is given as

$$\overline{i_S^2} = 4kT\Delta f \left(\frac{1}{0.5R_S}\right). \tag{4.31}$$

For MOS transistor the flicker and thermal noise can be lumped in to one noise generator $\overline{v_n^2}$ as [21]

$$\overline{v_n^2} = \left[\frac{8kT\left(1+\eta\right)}{3g_{m2}} + \frac{KF}{2fC_{OX}WLK'}\right]\Delta f, \tag{4.32}$$

where

k =Boltzmann's constant (1.38x10^{-23} J/K),

T =Absolute temperature (kelvin),

Δf = a small bandwidth (typically 1 Hz) at frequency f,

$\eta = \frac{g_{mbs}}{g_m}$,

KF =Flicker noise coefficient,

$C_{OX} = \frac{\varepsilon_{ox}}{t_{ox}}$ = Capacitance per unit area of the gate oxide, and

K' = Transconductance parameter ($\mu A/V^2$).

f =Frequency (Hz).

The output noise voltage at node v_{o2} due to the transistor noise is given by

$$\overline{v_{o2,n1}^2} = \left[\frac{g_{m2}R_{D2a}}{1+0.5R_Sg_{m2}}\right]^2 \overline{v_n^2}. \tag{4.33}$$

When the noise due to R_S is considered, the circuit behaves like a common-gate amplifier.

The output noise voltage due to $\overline{i_S^2}$ is

$$\overline{v_{o2,n2}^2} = \left[\frac{0.5R_S}{0.5R_S + \frac{1}{g_{m2}}}\right]^2 R_{D2a}^2 \overline{i_S^2},$$
$$\overline{v_{o2,n2}^2} = \left[\frac{0.5g_{m2}R_S}{1 + 0.5g_{m2}R_S}\right]^2 R_{D2a}^2 \overline{i_S^2}. \tag{4.34}$$

The output noise voltage due to $\overline{i_L^2}$ can be expressed as

$$\overline{v_{o2,n3}^2} = \left[R_{D2a}||0.5g_{m2}r_{o2}R_S\right]^2 \overline{i_L^2},$$
$$\overline{v_{o2,n3}^2} \approx R_{D2a}^2 \overline{i_L^2}. \tag{4.35}$$

where r_{o2} is the output resistance of M_{2a}. Thus the total mean square differential noise voltage between the output terminals is

$$\overline{v_{o2,tot}^2} = 4\left(\overline{v_{o2,n1}^2} + \overline{v_{o2,n2}^2} + \overline{v_{o2,n3}^2}\right),$$
$$\overline{v_{o2,tot}^2} = 4\left[\left(\frac{g_{m2}R_{D2a}}{1 + 0.5R_S g_{m2}}\right)^2 \overline{v_n^2} + \left(\frac{0.5g_{m2}R_S}{1 + 0.5g_{m2}R_S}\right)^2 R_{D2a}^2 \overline{i_S^2} + R_{D2a}^2 \overline{i_L^2}\right]. \tag{4.36}$$

The input referred differential noise voltage can be obtained by dividing (4.36) by the square of low-frequency differential gain ($\left[\frac{g_{m2}R_{D2a}}{1+0.5R_S g_{m2}}\right]^2$)

$$\overline{v_{eq}^2} = \left[\frac{1 + 0.5R_S g_{m2}}{g_{m2}R_{D2a}}\right]^2 \overline{v_{o2,tot}^2},$$
$$\overline{v_{eq}^2} = 4\overline{v_n^2} + 8kT\Delta f R_S\left[1 + \frac{R_S}{2R_{D2a}} + \frac{2}{g_{m2}R_{D2a}}\right] + \frac{16kT\Delta f}{g_{m2}^2 R_{D2a}}. \tag{4.37}$$

From (4.37) it can be concluded that with low values of R_S (higher DC gain), the input referred differential noise voltage will be small.

4.2.3 Simulation results

Fig. 4.13 plots the gain of stage 2 versus the frequency. Note that the low-frequency gain can be varied by changing the gate voltage v_{gate}. The -3 dB bandwidth of stage 2 stays above 1.5 GHz at different gain settings. Notice that the slight peaking at high ferquencies is due to the improper pole-zero cancellation. This has been made intentionally so as to improve the stage bandwidth. Table 4.2 summarizes the performance of the stage 2.

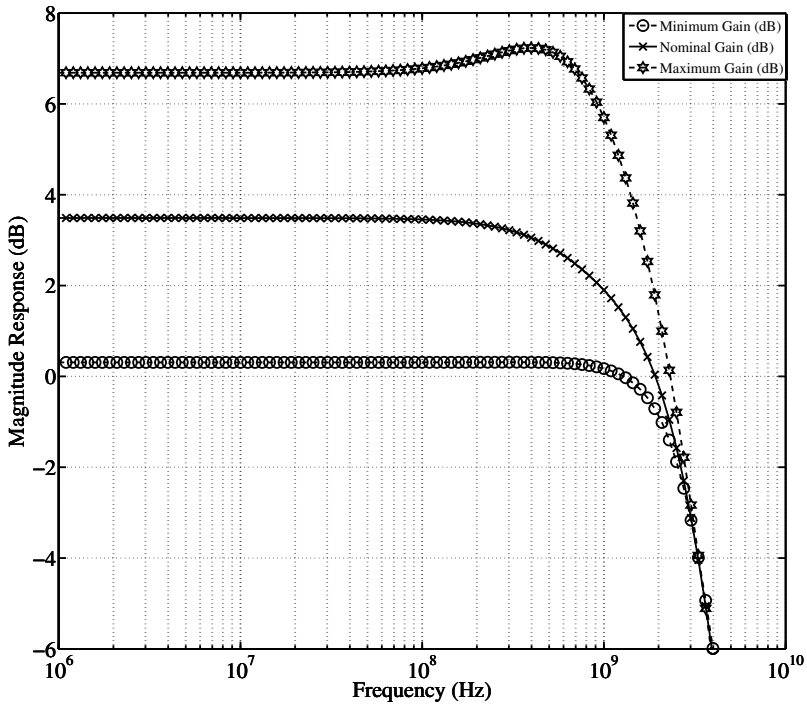

Figure 4.13: Simulated gain (dB) of stage 2 of VGA versus frequency (Hz).

Table 4.2: VGA Stage 2 (Stage 3) Performance summary.

-3dB frequency	1.5 GHz
Gain	0.3 dB, 3.6 dB, 6.7 dB
Input-referred noise	0.40, 0.29, 0.21 mV_{rms}
Power consumption	1.54 mW

4.3 DC-offset compensation

For the VGA, two methods for DC-offset compensation were used: AC coupling in the feedforward path and the DC feedback loop. In this design, resistor R_i and capacitor C_i were used off-chip. However for the full integrated receiver using only on-chip components, the major limitation comes from the high R_iC_i product value necessary for a low cut-off frequency of the AC coupling (high pass filter). Particularly in balanced circuits, making two large capacitors requires a lot of silicon area. This problem can be solved by making the resistor R_i very large. Such large value resistors (while keeping the area occupied by resistor) can be made by using sub-threshold transistors as seen in Fig. 4.14. The DC feedback loop is used to compensate for the offset originating from stage 1 (*VGA 1*). Again a very low cut-off frequency for the DC feedback loop was realized by using sub-threshold transistors in cascade [22].

Fig. 4.15 shows the equivalent resistance of the cascaded sub-threshold transistors. At 0.7 V the equivalent resistance is about 5 MΩ. Thus for a cut-off frequency of 20 kHz for the

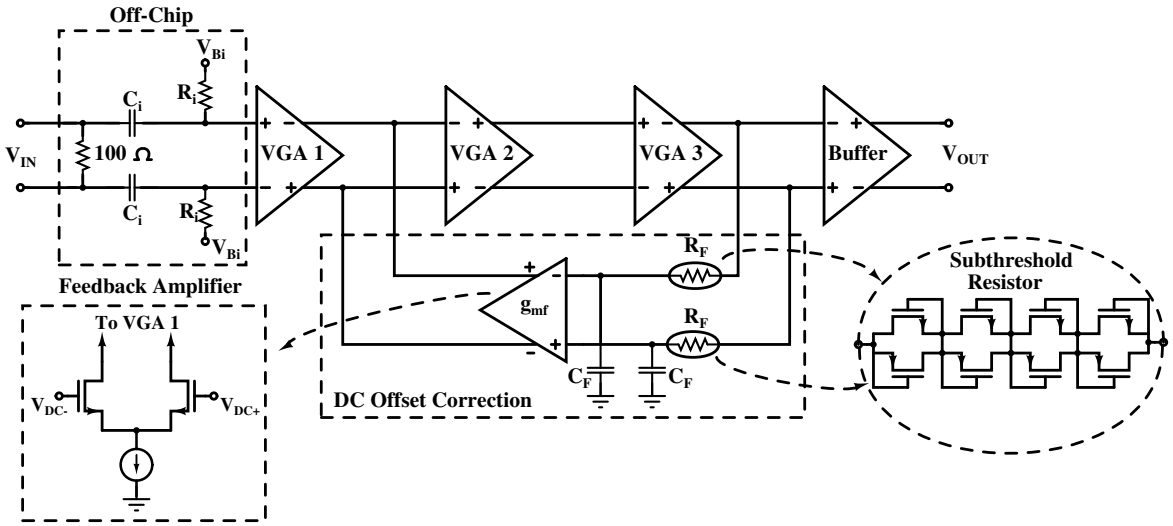

Figure 4.14: DC-offset compensation used along with subcircuit schematics.

DC feedback loop, a 1.6 pF capacitor is required. The output of stage 3 (*VGA 3*) is connected to the low-pass $R_F C_F$ pole of the DC feedback loop. The amplifier g_{mf} senses the output voltage from the low-pass $R_F C_F$ pole and then generates a correction current to the output of the stage 1 (*VGA 1*) to compensate for its DC offset. Fig. 4.16 shows a simplified VGA half-circuit to understand the operationof the DC feedback loop. A similar method for DC-offset compensation has been used in [22, 5].

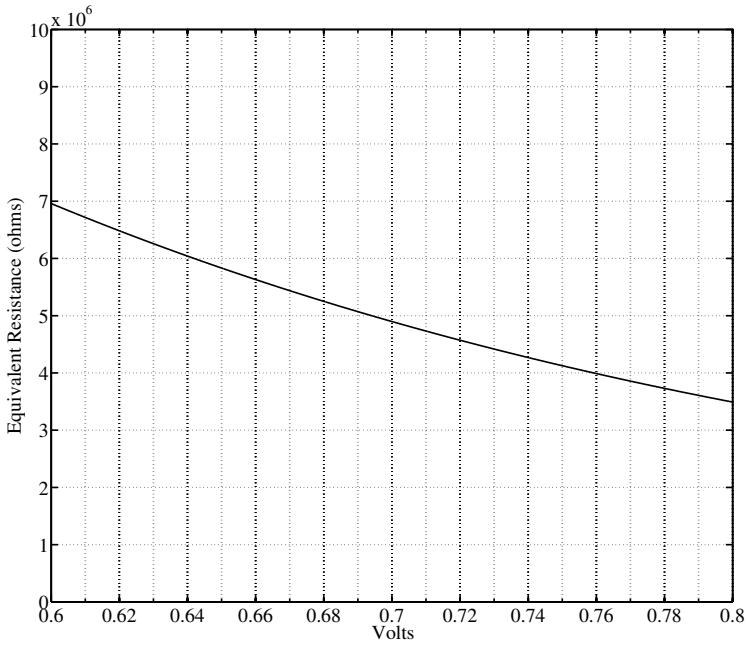

Figure 4.15: Simulated equivalent sub-threshold resistance as a function of voltage variation (around 0.7 V).

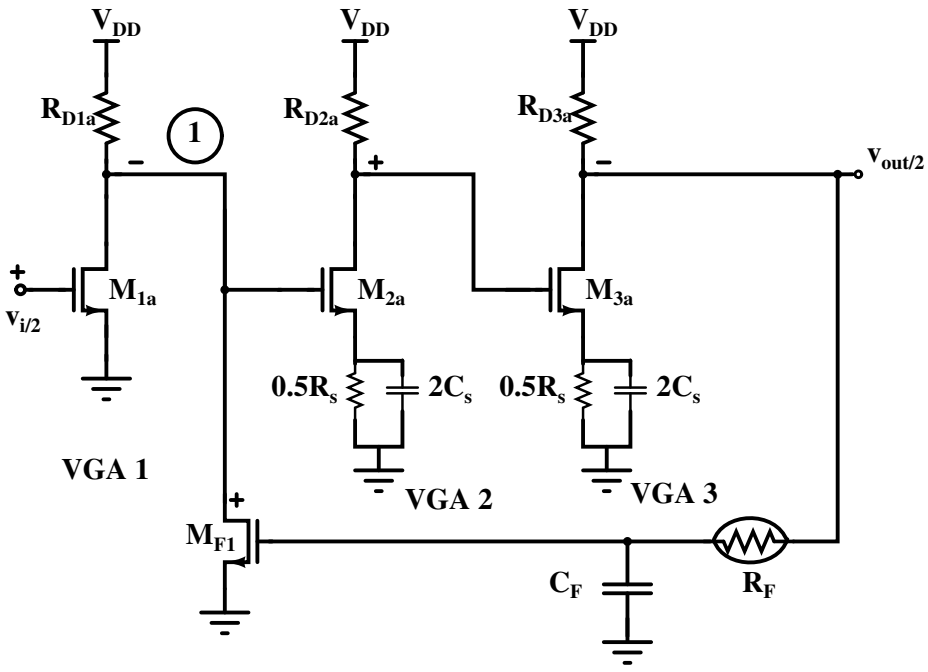

Figure 4.16: Simplified VGA half-circuit showing the operation of DC feedback loop.

4.4 Post-layout simulation results

VGA was designed and simulated in 0.13 μm CMOS technology. The overall VGA size was 290 μm $\times$ 130 μm. Fig.4.17 shows the (post-layout) simulated frequency response of the VGA at various gain settings. The voltage gain of the VGA varied from 14 dB to 26 dB and its -3 dB bandwidth remained above 1 GHz at all gain settings. The gain at 160 MHz (cut-off frequency of the LPF) was only 0.03 dB lower than its low-frequency value. The gain peaking observed at some gain settings is due to the improper pole-zero cancellation in stage 2 and stage 3 of VGA. This intentional gain peaking ensures that the bandwidth stays 1 GHz at different gain settings. Table 4.3 summarizes the simulated performance of VGA.

Table 4.3: VGA simulated performance summary.

-3dB frequency	1.0 GHz
Gain	14 dB, 20 dB, 26 dB
Input-referred noise	0.147, 0.103, 0.0865 mV_{rms}
Input 1 dB compression point	-26.5, -31.2, -37.4 dBV
Third-order input intercept point	-18.7, -25.3, -28.8 dBV
Power consumption	5.25 mW
Supply	1.2 V

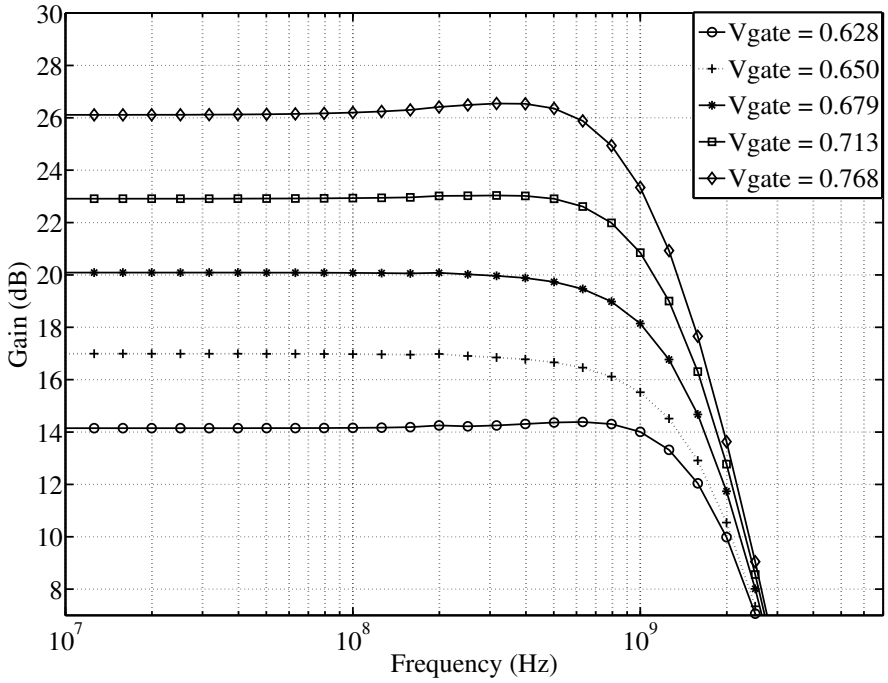

Figure 4.17: Simulated frequency response of VGA.

Chapter 5

VGA measurement results

The previous chapter explained the VGA design (small-signal and noise analysis of stages). The schematics of the various blocks in the VGA were presented and the simulation results of the gain stages were also shown. At the end post-layout simulation results were given. In this chapter the measured results from the chip will be presented. But before describing the measurement results, lets first look at how the VGA was implemented inside the chip and how the input-output connections were made with the off-chip components on the printed circuit board (PCB).

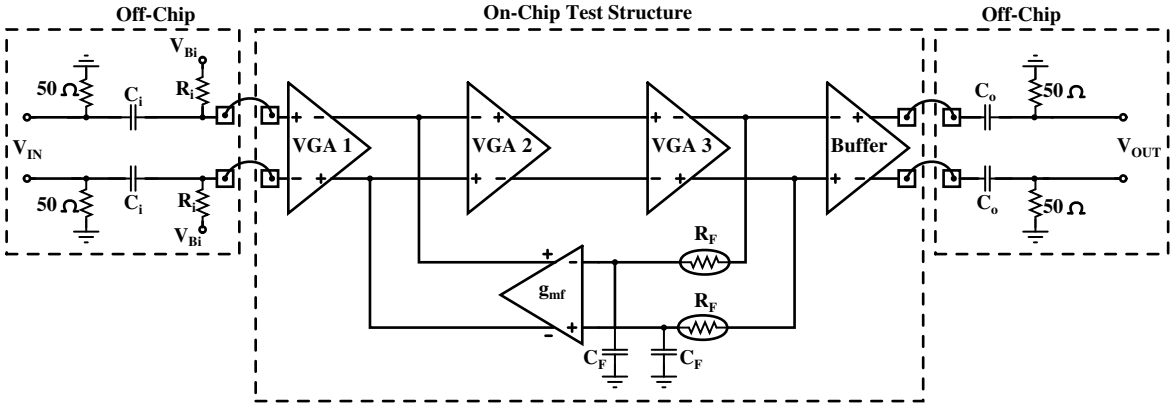

Figure 5.1: Block diagram representation of VGA and its connection with PCB.

5.1 Device-under-test (DUT)

Fig. 5.1 shows the block diagram of the test structure used for measuring the performance of VGA. It consists of two main parts: the on-chip test structure (*VGA + Buffer*) and the off-chip blocks. As explained earlier the input off-chip section forms a high-pass filter to remove any input DC-offset. Moreover V_{Bi} is used to bias VGA. The 50 Ω resistors are used at the input so that maximum power is transferred from the input source to the test structure. At the output, capcitors C_o prevent any DC voltage from the on-chip test structure to be coupled to the measurement instrument. Just like the input, 50 Ω resistors are used at the output so that

maximum power is transferred from the output to the measurement instrument. Inside the chip, the test structure is comprised of the VGA and a buffer. The buffer was used to drive the off-chip load resistors of 50 Ω. This combination of off-chip components and on-chip test structure will be referred to as the *device-under-test* (DUT). An important point to remember is that the overall gain of DUT was about 2.5 dB (when VGA is set at a gain of 20 dB). This is because of the loss incurred when driving the 50 Ω resistors from the buffer.

5.2 Measurement results

5.2.1 Gain vs. frequency

In order to characterize the frequency response of the fully-differential VGA, each of its terminals can be identifed as a port and thus VGA becomes a four-port device as shown in Fig. 5.2. First the S-parameters between ports 1 and 3 were measured, while the remaining ports 2 and 4 were terminated in 50 Ω (see Fig. 5.1). Next, S-parameters between port 1 and 4 were measured, while the remaining ports 2 and 3 were terminated in 50 Ω. Using the same procedure, S-parameters between ports 2 and 3 and then between ports 2 and 4 were measured. The differential-mode gain S_{dd} from the input of DUT to its output can then be calculated using [23]

$$S_{dd} = 0.5\left[S_{31} - S_{32} - S_{41} + S_{42}\right]. \tag{5.1}$$

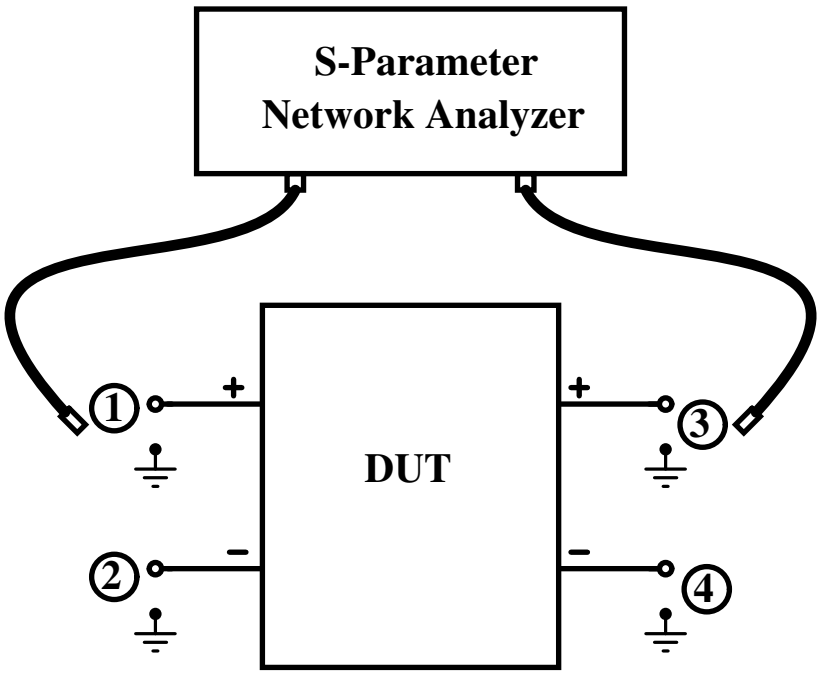

Figure 5.2: Block diagram representation of gain vs. frequency measurement setup.

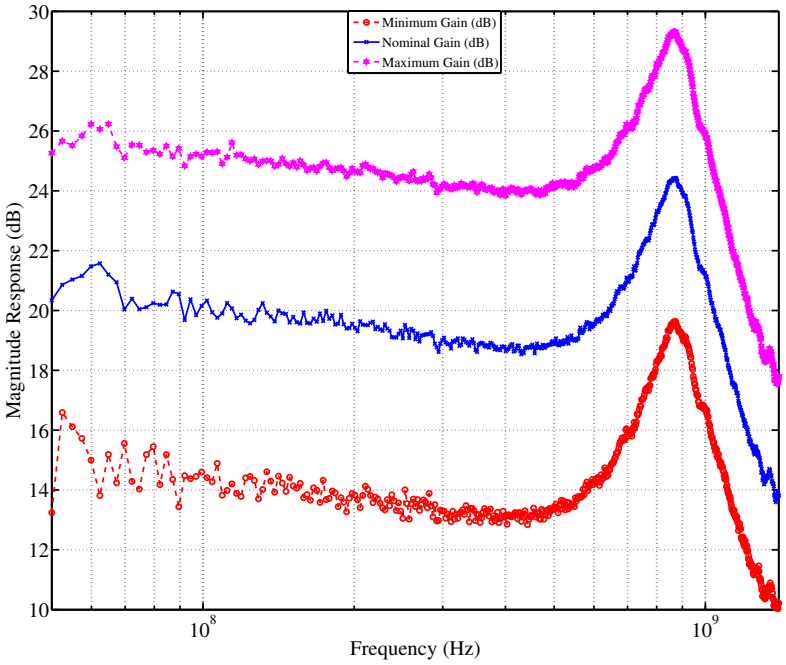

Figure 5.3: Measured gain vs. frequency curve of VGA.

The measured S_{dd} of the DUT using this method is shown in Fig. 5.3 (scaled to offset the loss due to the output buffer driving 50 Ω resistors). As can be seen from Fig. 5.3 the DC gain of VGA can be varied by about ± 6 dB. However the gain peaking around 1 GHz is much higher than that observed in the simulations. This implies an improper pole-zero cancellation. One reason could be that the capacitor matrix used in the design did not work correctly because the digital control of the chip (used to send the digital control word to the capacitor matrix) worked intermittently. There was no read out back from the chip to ensure that a correct digital word has been saved in the registers in side the chip. Thus the value of the capacitance C_S could not be controlled accurately to ensure that the zero formed by $R_S C_S$ cancel the pole formed by $R_{D2a} C_{L2}$.

Another source of error, more pronounced at high frequencies ($> 200MHz$), is due to the off-chip 50 Ω resistors. The parasistic capacitance of the 50 Ω resistors and the capacitance between the PCB copper track and the ground plane, become significant at high frequencies and this results in a shift in the effective impedance from 50 Ω. Equation (5.1) is true only when the unused ports are terminated in 50 Ω and a shift in the impedance value results in an error in the measurement. This error is especially significant for high frequency ($> 200MHz$) measurement. In order to avoid this error PCB should be designed carefully and small sized components, that are capable of high frequency operation, should be used.

5.2.2 Noise measurement

Fig. 5.4 shows the noise measurement setup. The inputs of the DUT were short circuited to ground. An external low-noise amplifier (LNA) was used to amplify the noise of the DUT above the noise floor of the spectrum analyzer. The noise measured by the spectrum analyzer is due to both DUT and the LNA. Next the noise of LNA was measured using the setup shown in Fig. 5.5. The noise of the external LNA was then subtracted from the results of Fig. 5.4 to get the noise due to VGA only.

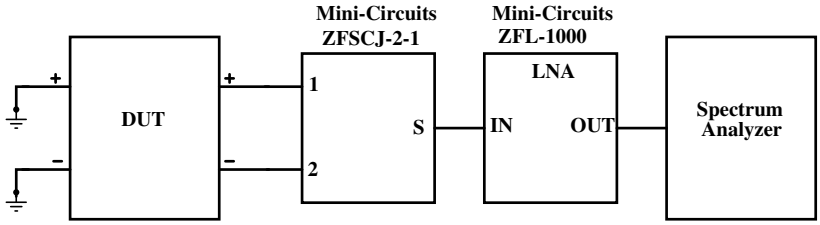

Figure 5.4: Block diagram representation of noise measurement setup.

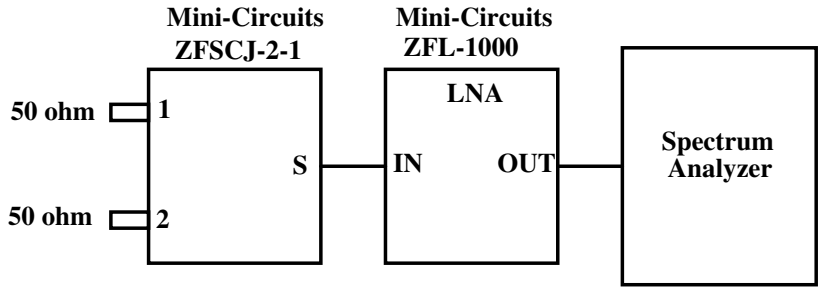

Figure 5.5: Block diagram representation of LNA noise measurement setup.

The noise of DUT was measured using the above arrangement in two frequency bands (100-110 MHz and 200-210 MHz). For each band five measurements were taken and noise was calculated using the mean of the five measurements. With VGA set for 20 dB gain, the input referred noise density of the VGA was 2.75 $nV/\sqrt{Hz}$ for the frequency band 100-110MHz,and for the frequency band 200-210MHz, the measured value was 2.58 $nV/\sqrt{Hz}$. The average of these two values is about 2.67 $nV/\sqrt{Hz}$. Comparing this to the simulated value of input noise density 2.9 $nV/\sqrt{Hz}$ (0.103 mV_{rms} divided by the square root of bandwidth 1.26 GHz), shows that the two values are in agreement. Using the same procedure, the input referred noise density of the VGA was measured for the 14 dB and the 26 dB gain settings. These values are given in Table 5.1.

Table 5.1: Mesaured input referred noise density of VGA.

VGA Gain	Measured noise density	Simulated noise density
14 dB	3.40 $nV/\sqrt{Hz}$	3.67 $nV/\sqrt{Hz}$
20 dB	2.58 $nV/\sqrt{Hz}$	2.90 $nV/\sqrt{Hz}$
26 dB	2.15 $nV/\sqrt{Hz}$	2.73 $nV/\sqrt{Hz}$

5.2.3 1 dB compression point

For small signals the amplifier behaves like a linear device. As the amplitude of the input signal is increased, the amplitude of the output rises proportionally. This continues until the amplifier is saturated by the large input signals. The 1 dB compression point (P-1dB) indicates the input power level at which the output power drops by 1 dB from its small signal value. The setup used for measuring the P-1dB is shown in Fig. 5.6.

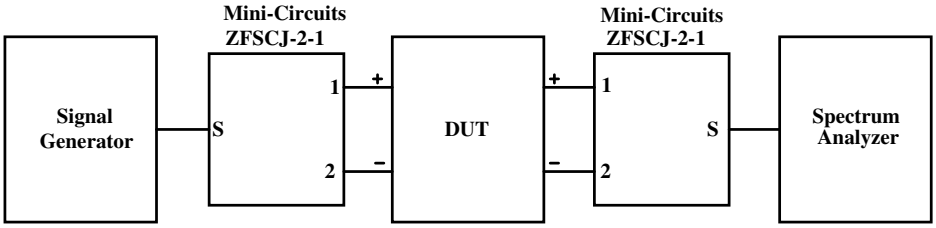

Figure 5.6: Block diagram representation of P-1dB measurement setup.

Signal generator feeds in a low-power test signal to the power splitter/combiner (ZFSCJ-2-1). The power splitter divides the test signal into two signals which are equal in magnitude but 180^0 out of phase. DUT amplifies these signals, which are then combined together using the power splitter/combiner. At the end Spectrum Analyzer is used to measure the output. The power level of the input signal is gradually increased and the output power is measured. From these measurements a graph between the input and output powers is plotted in Fig. 5.7 which shows that the input 1 dB compression point is -28.9 dBV when VGA is set to provide 14 dB gain. Table 5.2 gives the measured values of P-1dB of the VGA at different gain settings.

Table 5.2: Measured P-1dB of VGA.

VGA Gain	Measured P-1dB	Simulated P-1dB
14 dB	-28.9 dBV	-26.5 dBV
20 dB	-35.5 dBV	-31.2 dBV
26 dB	-40.3 dBV	-37.4 dBV

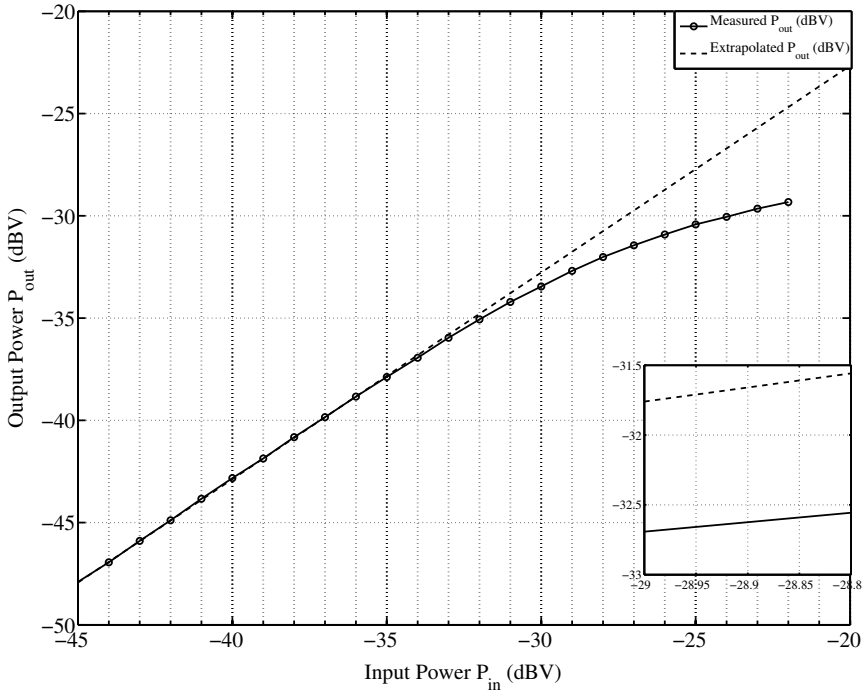

Figure 5.7: P_{out} vs. P_{in} curve for P-1dB measurement with 14 dB VGA gain.

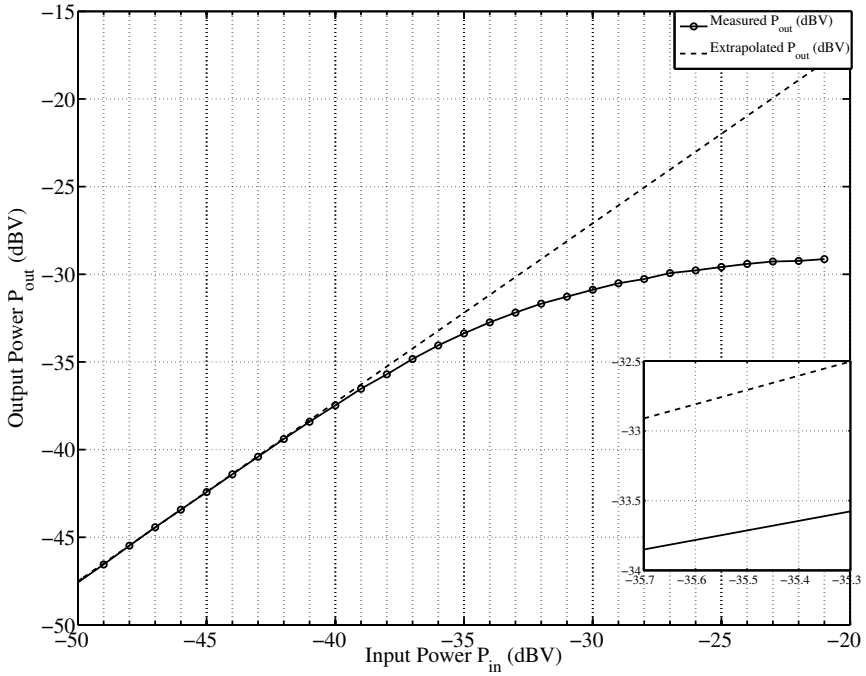

Figure 5.8: P_{out} vs. P_{in} curve for P-1dB measurement with 20 dB VGA gain.

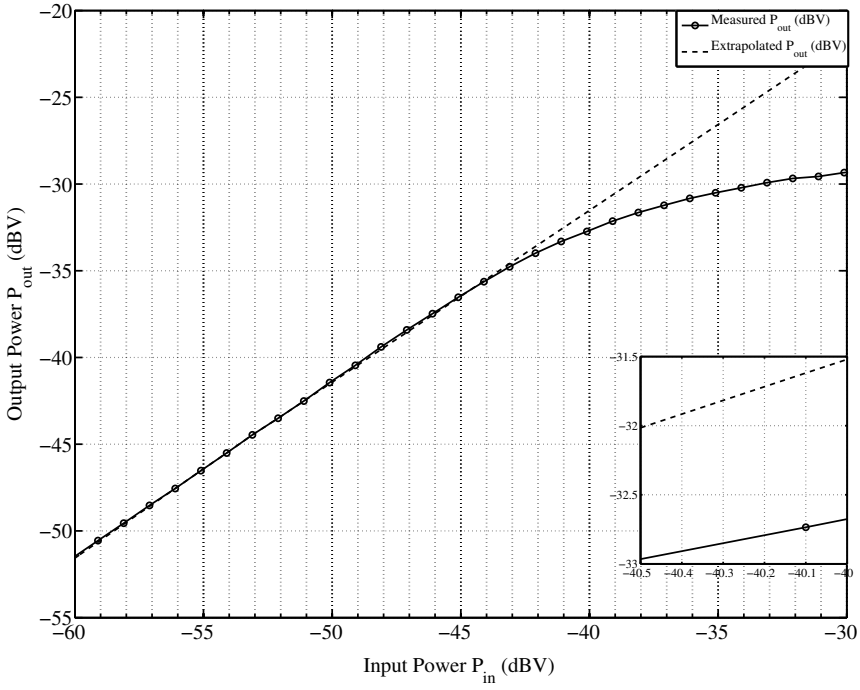

Figure 5.9: P_{out} vs. P_{in} curve for P-1dB measurement with 26 dB VGA gain.

5.2.4 Third-order input intercept point

When two signals at frequencies f_1 and f_2 are fed in to the amplifier, then at the output amplified signals at f_1 and f_2 are obtained along with their intermodulation products at $2f_1 - f_2$ and $2f_2 - f_1$. If f_1 and f_2 are closely spaced frequencies and lie within the amplifier bandwidth, then their intermodulation products at $2f_1 - f_2$ and $2f_2 - f_1$ will also lie within the amplifier's bandwidth. These intermodulation products are troublesome because they reduce the effective signal-to-noise ratio. In order to characterize this effect third-order input intercept point (IIP3) is used. IIP3 was measured for the VGA using the arrangement shown in Fig. 5.10.

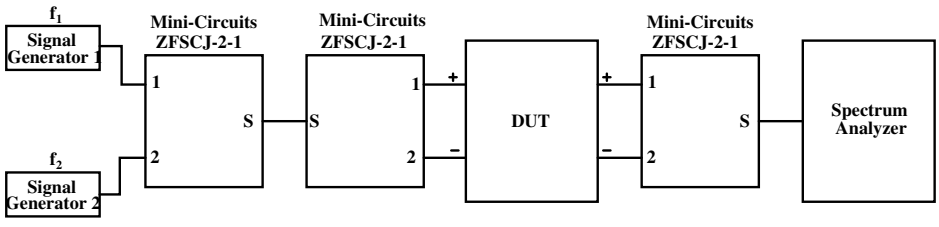

Figure 5.10: Block diagram representation of IIP3 measurement setup.

Using the two signal generators and power splitters/combiners a composite signal (made of two frequencies f_1 and f_2) was fed to the DUT. At the output Spectrum Analyzer was used to measure the signal power at f_1, f_2, $2f_1 - f_2$ and $2f_2 - f_1$. A graph was plotted between the output power versus the input power. Two curves were drawn: one for the linearly

amplified signal at f_1 and the other one for the intermodulation product $2f_1 - f_2$. Both curves were extrapolated and the input power at which the intermodulation product curve intersects the linearly amplified signal curve is the IIP3 of the DUT as shown in Fig. 5.11. From Fig. 5.11 it is clear that the IIP3 of the VGA (at 14 dB gain) is -20.15 dBV. Table 5.3 gives the measured values of IIP3 of the VGA at different gain settings. The measured values of IIP3 are somewhat lower than that of the simulated ones. The IIP3 of VGA is influenced strongly by the linearity of the R_S resistor realized using transistors. [24] explains the use of quasi-floating gate (QFG) to enhance the linearity of MOS resistors.

Table 5.3: Measured IIP3 of VGA.

VGA Gain	Measured IIP3	Simulated IIP3
14 dB	-20.15 dBV	-18.7 dBV
20 dB	-28.02 dBV	-25.3 dBV
26 dB	-33.59 dBV	-28.8 dBV

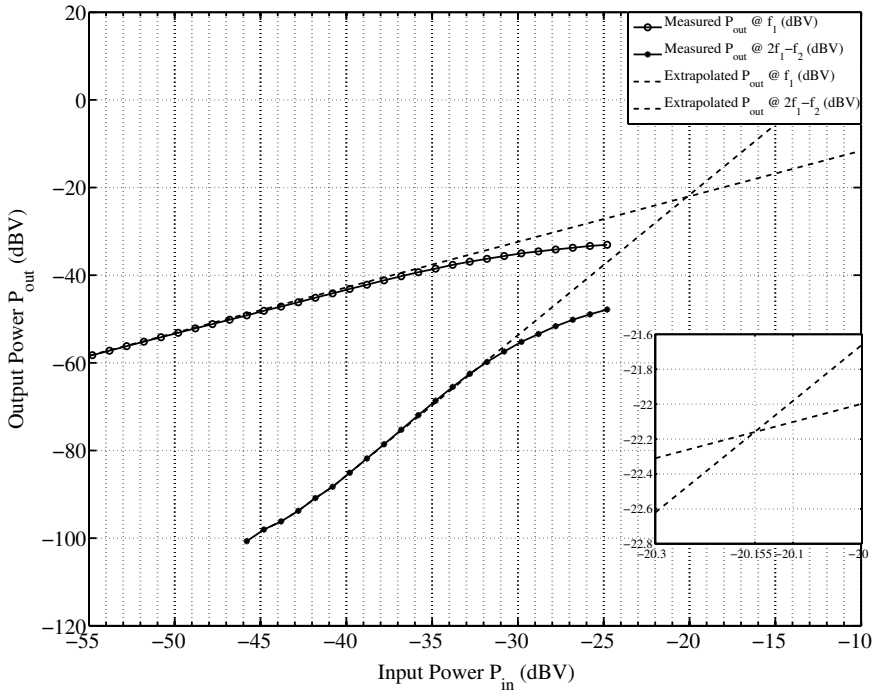

Figure 5.11: P_{out} vs. P_{in} curve for IIP3 measurement with 14 dB VGA gain.

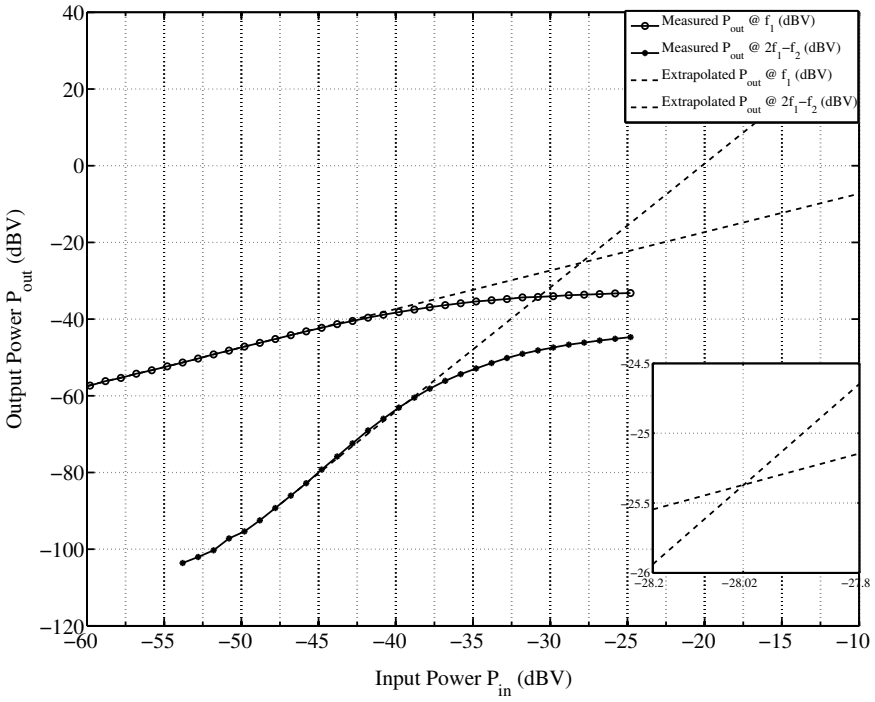

Figure 5.12: P_{out} vs. P_{in} curve for IIP3 measurement with 20 dB VGA gain.

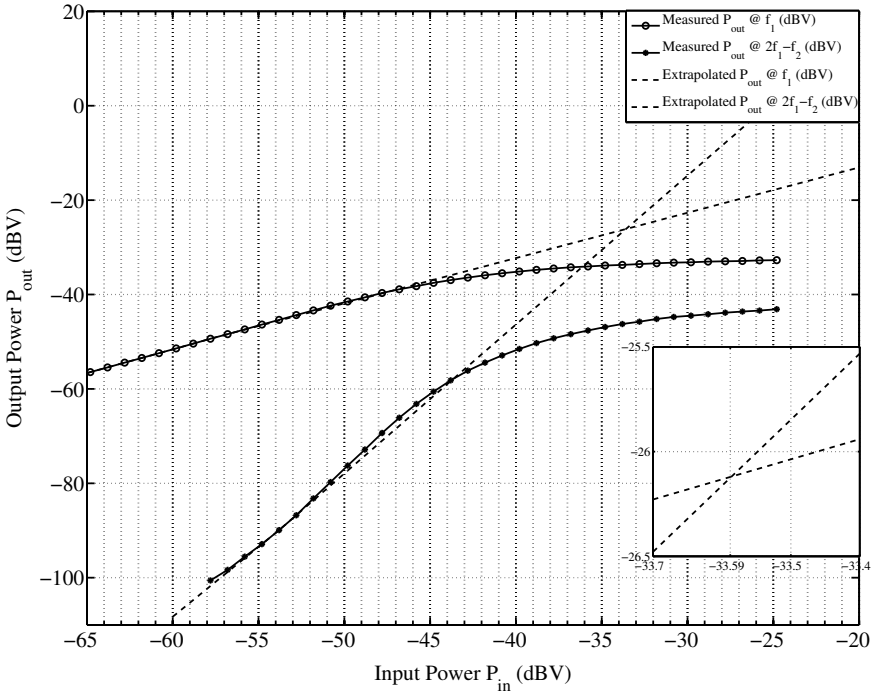

Figure 5.13: P_{out} vs. P_{in} curve for IIP3 measurement with 26 dB VGA gain.

5.3 Summary

This chapter presented the measured results of the VGA. In the beginning, the input-output connections of the chip with the PCB were shown. Next the gain versus frequency measurement for VGA was presented. Following that the setup used for measuring the noise density of the VGA was depicted and the measured noise density values were given in Table 5.1. Then the input 1 dB compression point and the third order input intercept point measurement setups were shown and their values at different VGA gain settings were summarized in Table 5.2 and Table 5.3 respectively.

Chapter 6

Conclusions

This thesis first explained the idea behind Synthetic Aperture Radar (SAR) since the VGA was to be used within such a system. Additional details about the receiver architecture for SAR were also provided. Next, VGA design goals such as its gain, bandwidth, noise and power consumption were presented which were extracted from the system requirements for the receiver. A multistage architecture for the VGA was also presented that could satisfy the design goals for VGA. The trade-off between the gain-bandwidth product requirement for each stage and noise performance of the VGA was explained and based on that a figure-of-merit (FOM) was defined. It was shown that using two stages in the variable gain section of the VGA gave the best FOM.

Chapter 3 described various circuits and techniques that could be used to create wide-band stages in the VGA. Another section in this chapter explained three analog methods for DC-offset compensation. The next chapter was solely related to the design of the VGA. Small-signal and noise analyses were given for each stage in the amplifier. The simulated performance of the stages was also shown. At the end, post-layout simulations for the entire VGA were provided.

The measured results for the VGA were presented in chapter 5. In the beginning, the input-output connections of the chip with the PCB were shown. Next the gain versus frequency measurement for VGA was presented. It was shown that the VGA met its gain and bandwidth design goals. However, since the digital control part of the chip was not working fully, the capacitor matrices in stage 2 and stage 3 could not be controlled accurately and this resulted in gain peaking. In another subsection, the noise measurement results for the VGA were given which matched well with the simulated values. At the end of the chapter 1 dB compression point and third order input intercept point measurement setups and results were shown. Appendix A shows the layout of the VGA and its photomicrograph. A picture of the PCB with the bonded chip is given in Appendix B.

In short the simulated and the measured results of the VGA showed that it satisfied the design goals set at the beginning of the thesis and thus could be used as a part of the baseband for the direct conversion receiver for SAR.

Bibliography

[1] ESA – Living Planet Programme – GMES – Synthetic Aperture Radar Missions. [Online]. Available: http://www.esa.int/esaLP/SEMZGU4KXMF_LPgmes_0.html

[2] N. Gebert, G. Krieger, and A. Moreira, "Digital Beamforming on Receive: Techniques and Optimization strategies for High-Resolution Wide-Swath SAR imaging," *Aerospace and Electronic Systems, IEEE Transactions on*, vol. 45, no. 2, pp. 564 –592, April 2009.

[3] M. Kaltiokallio, S. Lindfors, V. Saari, and J. Ryynanen, "Design of Precise Gain GmC-leapfrog Filters," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, May 2007, pp. 3534 –3537.

[4] R. Jindal, "Gigahertz-band high-gain low-noise AGC amplifiers in fine-line NMOS," *Solid-State Circuits, IEEE Journal of*, vol. 22, no. 4, pp. 512 – 521, Aug. 1987.

[5] Y. Wang, B. Afshar, T.-Y. Cheng, V. Gaudet, and A. Niknejad, "A 2.5mW inductorless wideband VGA with dual feedback DC-offset correction in 90nm CMOS technology," in *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE*, 2008, pp. 91 –94.

[6] F. Tavernier and M. Steyaert, "A low power, area efficient limiting amplifier in 90nm CMOS," in *ESSCIRC, 2009. ESSCIRC '09. Proceedings of*, 2009, pp. 128 –131.

[7] S. Galal and B. Razavi, "10-Gb/s limiting amplifier and laser/modulator driver in 0.18-um CMOS technology," *Solid-State Circuits, IEEE Journal of*, vol. 38, no. 12, pp. 2138 – 2146, 2003.

[8] B. Razavi, "Design considerations for direct-conversion receivers," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 44, no. 6, pp. 428 –435, June 1997.

[9] Razavi, *Design of Integrated Circuits for Optical Communications*, 3rd ed. McGraw-Hill, 2003.

[10] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*, 2nd ed. Cambridge University Press, 2003.

[11] Y.-H. Oh and S.-G. Lee, "An inductance enhancement technique and its application to a shunt-peaked 2.5 Gb/s transimpedance amplifier design," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 51, no. 11, pp. 624 – 628, 2004.

[12] E. Cherry and D. Hooper, "The design of wide-band transistor feedback amplifiers," *Electrical Engineers, Proceedings of the Institution of*, vol. 110, no. 2, pp. 375 –389, 1963.

[13] C. Holdenried, M. Lynch, and J. Haslett, "Modified CMOS Cherry-Hooper amplifiers with source follower feedback in 0.35 um technology," in *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, 2003, pp. 553 – 556.

[14] C. Holdenried, J. Haslett, and M. Lynch, "Analysis and design of HBT Cherry-Hooper amplifiers with emitter-follower feedback for optical communications," *Solid-State Circuits, IEEE Journal of*, vol. 39, no. 11, pp. 1959 – 1967, 2004.

[15] J. Abbott, C. Plett, and J. Rogers, "A 15 GHz, 1.8V, variable-gain, modified Cherry-Hooper amplifier," in *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, 2005, pp. 645 – 648.

[16] J. Jussila, "Analog Baseband Circuits for WCDMA Direct-Conversion Receivers," 2003.

[17] B. Razavi, "A 2.4-GHz CMOS receiver for IEEE 802.11 wireless LANs," *Solid-State Circuits, IEEE Journal of*, vol. 34, no. 10, pp. 1382 –1385, Oct. 1999.

[18] J. Järvinen, "Analog Baseband Circuits for Sensor Systems," May 2008.

[19] J. Wilson, R. Youell, T. Richards, G. Luff, and R. Pilaski, "A single-chip VHF and UHF receiver for radio paging," *Solid-State Circuits, IEEE Journal of*, vol. 26, no. 12, pp. 1944 –1950, Dec. 1991.

[20] G. Luff, R. Youell, J. Wilson, T. Richards, and R. Pilaski, "A Single-chip VHF And UHF Receiver For Radio Paging," in *Solid-State Circuits Conference, 1991. Digest of Technical Papers. 38th ISSCC., 1991 IEEE International*, Feb. 1991, pp. 120 –300.

[21] P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, 2nd ed. Oxford University Press USA, 2002.

[22] M. Elmala, B. Carlton, R. Bishop, and K. Soumyanath, "A 1.4V, 13.5mW, 10/100MHz 6th order elliptic filter/VGA with DC-offset correction in 90nm CMOS [WLAN applications]," in *Radio Frequency integrated Circuits (RFIC) Symposium, 2005. Digest of Papers. 2005 IEEE*, 2005, pp. 189 – 192.

[23] W. R. Eisenstadt, R. Stengel, and B. M. Thompson, *Microwave Differential Circuit Design using Mixed-Mode S-Parameters*, 1st ed. Artech House Publishers, 2006.

[24] B. Calvo, A. Lopez-Martin, S. Balasubramanian, J. Ramirez-Angulo, and R. Carvajal, "Linear-enhanced V to I converters based on MOS resistive source degeneration," in *Circuits and Systems, 2008. ISCAS 2008. IEEE International Symposium on*, May 2008, pp. 3118 –3121.

[25] V. Saari, M. Kaltiokallio, S. Lindfors, J. Ryynanen, and K. Halonen, "A 240-MHz Low-Pass Filter With Variable Gain in 65-nm CMOS for a UWB Radio Receiver," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 7, pp. 1488 –1499, 2009.

[26] S. D'Amico, M. De Matteis, and A. Baschirotto, "A 6.4mW, 4.9nV/$\sqrt{Hz}$, 24dBm IIP3 VGA for a multi-standard (WLAN, UMTS, GSM, and Bluetooth) receiver," in *Solid-State Circuits Conference, 2006. ESSCIRC 2006. Proceedings of the 32nd European*, 2006, pp. 82 –85.

[27] S. D'Amico, A. Baschirotto, M. De Matteis, N. Ghittori, A. Vigna, and P. Malcovati, "A CMOS 5 nV /$\sqrt{Hz}$ 74-dB-Gain-Range 82-dB-DR Multistandard Baseband Chain for Bluetooth, UMTS, and WLAN," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 7, pp. 1534 –1541, 2008.

[28] E. Sanchez-Sinencio and J. Silva-Martinez, "CMOS transconductance amplifiers, architectures and active filters: a tutorial," *Circuits, Devices and Systems, IEE Proceedings* -, vol. 147, no. 1, pp. 3 –12, Feb. 2000.

[29] H. D. Lee, K. A. Lee, and S. Hong, "A Wideband CMOS Variable Gain Amplifier With an Exponential Gain Control," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 55, no. 6, pp. 1363 –1373, 2007.

[30] Y.-H. Yu, Y.-S. Yang, and Y.-J. Chen, "A Compact Wideband CMOS Low Noise Amplifier With Gain Flatness Enhancement," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 3, pp. 502 –509, 2010.

[31] D. Barras, H. Jaeckel, and W. Hirt, "A wideband 0 to 60 dB CMOS variable gain amplifier for IR-UWB I/Q receivers," in *ESSCIRC, 2009. ESSCIRC '09. Proceedings of*, 2009, pp. 264 –267.

[32] H.-Y. Shih, C.-N. Kuo, W.-H. Chen, T.-Y. Yang, and K.-C. Juang, "A 250 MHz 14 dB-NF 73 dB-Gain 82 dB-DR Analog Baseband Chain With Digital-Assisted DC-Offset Calibration for Ultra-Wideband," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 2, pp. 338 –350, 2010.

[33] S. D'Amico, A. Baschirotto, K. Philips, O. Rousseaux, and B. Gyselinckx, "A 240MHz programmable gain amplifier and filter for ultra low power low-rate UWB receivers," in *ESSCIRC, 2009. ESSCIRC '09. Proceedings of*, 2009, pp. 260 –263.

[34] J. Alegre, S. Celma, B. Calvo, N. Fiebig, and S. Halder, "SiGe Analog AGC Circuit for an 802.11a WLAN Direct Conversion Receiver," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 56, no. 2, pp. 93 –96, 2009.

[35] S. Otaka, G. Takemura, and H. Tanimoto, "A low-power low-noise accurate linear-in-dB variable-gain amplifier with 500-MHz bandwidth," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 12, pp. 1942 –1948, Dec. 2000.

[36] Y. Zheng, J. Yan, and Y. P. Xu, "A CMOS VGA With DC Offset Cancellation for Direct-Conversion Receivers," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 56, no. 1, pp. 103 –113, 2009.

[37] H. Elwan, A. Tekin, and K. Pedrotti, "A Differential-Ramp Based 65 dB-Linear VGA Technique in 65 nm CMOS," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 9, pp. 2503 –2514, 2009.

[38] C.-H. Wu, C.-S. Liu, and S.-L. Liu, "A 2 GHz CMOS variable-gain amplifier with 50 dB linear-in-magnitude controlled gain range for 10GBase-LX4 Ethernet," in *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, 2004, pp. 484 – 541 Vol.1.

Appendix A

Layout and chip photomicrograph

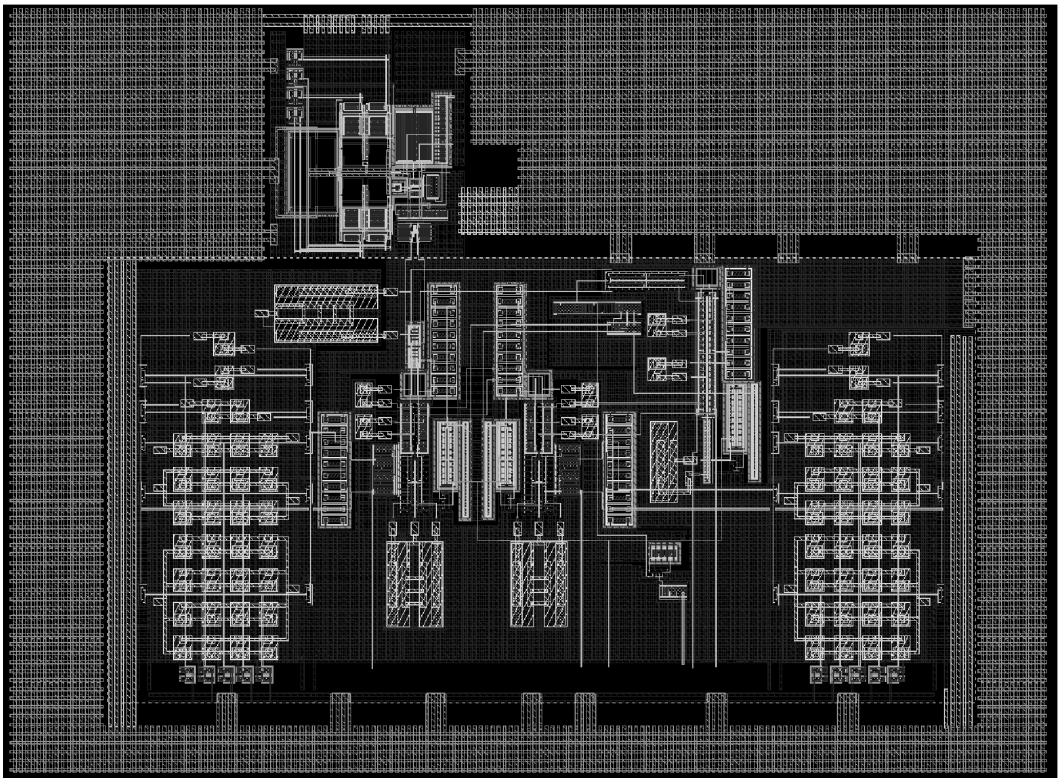

Figure A.1: Layout of VGA and buffer.

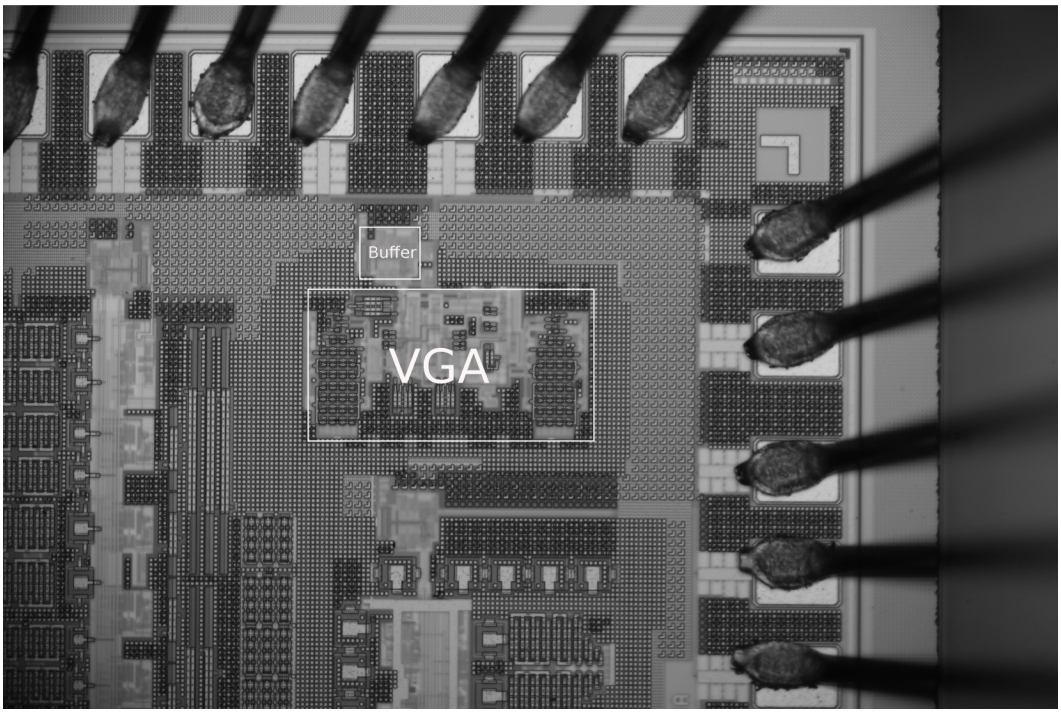

Figure A.2: Chip photomicrograph.

Appendix B

PCB

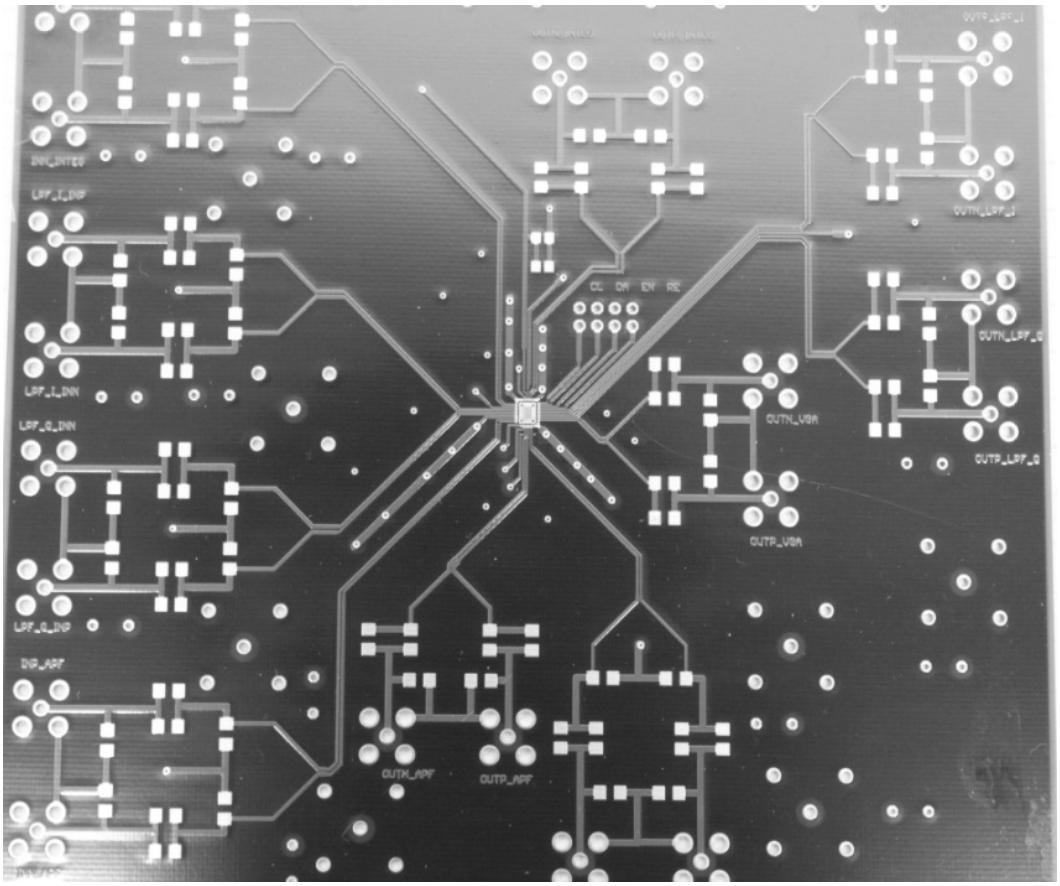

Figure B.1: PCB.