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10 Gigabit-capable Passive Optical Network Transmission Convergence layer design

Faculty of Electronics, Communications and Automation

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ABSTRACT OF THE
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With the emergence of new broadband telecommunication services and constantly increasing bandwidth demand, fixed access network infrastructure is evolving from electrical to optical. The European Commission funded research project Scalable Advanced Ring-based passive Dense Access Network Architecture (SARDANA) researches the next-generation passive optical access network technologies. The main goal of the project is to reduce expenses that are related to passive optical access networks.

This master's thesis discusses the design of the non-standardized 10 Gigabit-capable Passive Optical Network (XGPON) Transmission Convergence (TC) layer and its first implementation version for Optical Network Unit (ONU) for the SARDANA test network. The SARDANA XGPON TC (SXGTC) layer implements the Medium Access Control (MAC) protocol. The SXGTC layer is based on the standardized solution offered by the ITU-T G.984.3 Gigabit-capable Passive Optical Network (GPON) TC (GTC) layer recommendation [ITU08] but differs from it in many details. All the SXGTC layer features are compared to those of the GTC layer.

As a result, the SXGTC protocol is able to support operation on up to 9.95328 Gbps symmetrical transmission rates. The SXGTC layer is optimized for the 8-byte-word-based data processing. The first ONU SXGTC layer Field Programmable Gate Array (FPGA) implementation is presented in terms of functional blocks. The implementation supports operation on 9.95328 Gbps in the downstream offering 98 % bandwidth efficiency and on 2.48832 Gbps in the upstream offering 94.5 % bandwidth efficiency for the SARDANA test network configuration.

Keywords: Gigabit-capable passive optical network, GPON, 10 GPON, XGPON, Medium Access Control protocol, MAC, FPGA, access network

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Uusien laajakaistaisten tietoliikennepalvelujen ja kasvavan tiedonsiirtokapasiteetin tarpeen myötä kiinteiden liityntäverkkojen infrastruktuuri on muuttumassa sähköisestä optiseksi. Euroopan komission rahoittamassa Scalable Advanced Ring-based passive Dense Access Network Architecture (SARDANA)-tutkimusprojektissa tutkitaan seuraavan sukupolven passiivisten optisten liityntäverkojen teknologioita. Projektin päätavoitteena on pienentää passiivisiin optisiin liityntäverkkoihin liittyviä kustannuksia.

Tämä diplomityö käsittelee SARDANA-testiverkon standardoimattoman 10 Gigabit-capable Passive Optical Network (XGPON) Transmission Convergence (TC)-kerroksen suunnittelua ja ensimmäistä toteutusta optisessa verkkopäätteessä (ONU:ssa). TC-kerros toteuttaa Medium Access Control (MAC)-protokollan. SARDANA XGPON TC (SXGTC)-kerros perustuu standardoituun ITU-T G.984.3 Gigabit-capable Passive Optical Network (GPON) TC (GTC)-kerroksen [ITU08] tarjoamaan ratkaisuun mutta eroaa tästä yksityiskohdiltaan. Kaikki SXGTC-kerroksen oleelliset yksityiskohdat peilataan GTC-kerrokseen.

Suunniteltu SXGTC-protokolla tukee maksimissaan 9.95328 Gbps:n symmetrisiä tiedonsiirtonopeuksia. SXGTC-protokolla on optimoitu käsittelemään dataa 8 tavun sanoissa. Ensimmäinen ONU SXGTC-kerroksen toteutus ohjelmoitavassa Field Programmable Gate Array (FPGA)-piirissä esitellään funktionaalisten lohkojen avulla. Tämän implementaation tiedonsiirtonopeus alasuunnassa on 9.95328 Gbps 98 %:n kaistatehokkuudella ja yläsuunnassa 2.48832 Gbps 94.5 %:n kaistatehokkuudella SARDANA-testiverkkokonfiguraation tapauksessa.

Avainsanat: Gigabit-capable passive optical network, GPON, 10GPON, XGPON, Medium Access Control protokolla, MAC, FPGA, SARDANA, liityntäverkko

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23 April 2010, Espoo, Finland

Dmitri Leino

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Symbols

E	expected value
P	probability
R	frame drop rate

Abbreviations

10GEPON	10 Gigabit Ethernet Passive Optical Network
10GPON	10 Gigabit-capable Passive Optical Network
Alen	Asynchronoud Transfer Mode partition length
Alloc-ID	Allocation Identifier
AON	Active Optical Network
APON	Aynchrounous Transfer Mode Passive Optical Network
ASIC	Application-Specific Integrated Circuit
ATM	Asynchrounous Transfer Mode
AWG	Arrayed Wave Guide
BIP-8	8-bit Bit Interleaved Parity
BIP-64	64-bit Bit Interleaved Parity
BCH	Bose-Chaudhuri-Hocquenghem
BER	Bit Error Rate
Blen	Bandwidth map length
BPON	Broadband Passive Optical Network
bps	bits per second
BW	Bandwidth
CATV	Cable Television
CATVd	Cable Television frame downstream
CATVu	Cable Television frame upstream
C/M-Plane	Control and Management Plane
CO	Central Office
CRC-8	8-bit Cyclic Redundancy Check
CRC-32	32-bit Cyclic Redundancy Check
DBA	Dynamic Bandwidth Allocation
DBRu	Dynamic Bandwidth Report upstream
DS	Downstream
DSL	Digital Subscriber Line
DSP	Digital Signal Processing
DWDM	Dense Wavelength Division Multiplexing
EDF	Erbium Doped Fiber
EPON	Ethernet Passive Optical Network
FEC	Forward Error Correction
FPGA	Field Programmable Gate Array
FSAN	Full Service Access Network
FTTC	Fiber-To-The-Curb
FTTCab	Fiber-To-The-Cabinet
FTTB	Fiber-To-The-Building
FTTH	Fiber-To-The-Home
FTTH/B	Fiber-To-The-Home/Building
FTTP	Fiber-To-The-Premises

FTTx	Fiber-To-The-x
GEM	Gigabit-capable Passive Optical Network Encapsulation Method
GEPON	Gigabit Ethernet Passive Optical Network
GPON	Gigabit-capable Passive Optical Network
GTC	Gigabit-capable Passive Optical Network Transmission Convergence
HDL	Hardware Description Language
HEC	Header Error Correction
HFC	Hybrid Fiber Coax
Ind	Indication
Int	Interconnect
I/O	Input/Output
IEEE	Institute of Electrical and Electonics Engineers
IP	Intellectual Property
IPTV	Internet Protocol Television
ITU-T	International Telecommunication Union - Telecommunication standardization sector
LE	Logic Element
LUT	Look-Up Table
MAC	Medium Access Control
MCI	Microwave Communications, Inc
Message-ID	Message Identifier
MSB	Most Significant Bit
MUX	Multiplexer
NG-PON	Next Generation Passive Optical Network
NIU	Network Interface Unit
OADM	Optical Add Drop Multiplexer
OAM	Operations, Administration and Maintenance
OAN	Optical Access Network
ODN	Optical Distribution network
OLT	Optical Line Terminal
OMCI	Optical Network Unit Management and Control Interface
ONT	Optical Network Termination
ONU	Optical Network Unit
ONU-ID	Optical Network Unit Identifier
OS	Optical Switches
P2MP	point-to-multipoint
P2P	point-to-point
PCBd	Physical Control Block downstream
PHY	Physical layer
Plend	Payload length downstream
PLI	Payload Length Indicator
PLOAM	Physical Layer Operations, Administration and Maintenance
PLOAMd	Physical Layer Operations, Administration and Maintenance downstream

PLOAMu	Physical Layer Operations, Administration and Maintenance upstream
PLOu	Physical Layer Overhead upstream
PMD	Physical Media Dependent
PON	Passive Optical Network
Port-ID	Port Identifier
Psync	Physical synchronization
PSD	Packet Size Distribution
PTI	Payload Type Indicator
QoS	Quality of Service
RN	Remote Node
RSOA	Reflective Semiconductor Optical Amplifier
RTD	Round Trip Delay
RTL	Register Transfer Level
Rx	Receiver
SARDANA	Scalable Advanced Ring-based passive Dense Access Network Architecture
SBA	Static Bandwidth Allocation
SDU	Service Data Unit
SNI	Service Network Interface
SRAM	Static Random Access Memory
SXGEM	Scalable Advanced Ring-based passive Dense Access Network Architecture 10 Gigabit-capable Passive Optical Network Encapsulation Method
SXGPON	Scalable Advanced Ring-based passive Dense Access Network Architecture 10 Gigabit-capable Passive Optical Network
SXGTC	Scalable Advanced Ring-based passive Dense Access Network Architecture 10 Gigabit-capable Passive Optical Network Transmission Convergence
TC	Transmission Convergence
T-CONT	Transmission Container
TDD	Time Division Duplex
TDM	Time Division Multiplexing
TDMA	Time Division Multiple Access
TDM-PON	Time Division Multiplexed Passive Optical Network
TPON	Telephony on Passive Optical Network
Tx	Transmitter
UNI	User Network Interface
U-Plane	User Plane
US	Upstream
VHDL	Very High Speed Integrated Circuit Hardware Description Language
VLAN	Virtual Local Area Network
VLSI	Very Large Scale Integrated
WDD	Wavelength Division Duplex
WDM	Wavelength Division Multiplexing
WDM-PON	Wavelength Division Multiplexed Passive Optical Network

XGPON	10 Gigabit-capable Passive Optical Network

1 Introduction

Users of telecommunication access networks are today showing interest for the latest high-bandwidth demanding Internet applications and services such as on-line gaming, video telephony, video-on-demand, high-definition television and peer-to-peer applications. Furthermore, many households have multiple personal computers connected to Internet - all requiring a piece of bandwidth. The fast development of broadband telecommunication services is not only pushing the traditional copper-based access networks to the limits but requires an upgrade of access infrastructure. Fiber-To-The-Home/Building (FTTH/B) point-to-multipoint (P2MP) optical access networking is one of the most promising technological concepts that could meet this challenge, as it is evident that Digital Subscriber Line (DSL) technology is close to the end of its life cycle. [CPG+06]

Deployment of FTTH/B access networks has already started in many countries. According to the latest worldwide results of FTTH Council Europe [FTTH09a], South Korea was in February 2009 a promised land of FTTH/B with the world's highest household penetration rate of nearly 45 %. Hong Kong and Japan were following close behind. It seems that FTTH/B is slowly beginning to conquer also United States of America and Europe. In Europe the progress is mostly driven by small economies with Sweden being in the vanguard. The larger European economies such as France are also planning on investing in FTTH/B. For instance, in Paris 4 million households will be connected with FTTH/B access network by 2012 [Leb09]. As of September 2009, the European top 10 countries are currently having less than 11 % household penetration rates [FTTH09b].

Until recently, the uncertainty in the revenue due to a relatively long payback time was significantly slowing down FTTH/B deployment progress [HYS06]. The cost of the equipment has only lately begun to decrease with standardization and the extensive deployments especially in eastern Asia [CPG+06]. The near future forecast of [Fin09] predicts further growth in FTTH/B households worldwide.

The European Commission funded, multinational next-generation optical access network project referred to as Scalable Advanced Ring-based passive Dense Access Network Architecture (SARDANA) is a European attempt to reduce FTTH/B related costs. The SARDANA project started in January 2008 and will continue for three years until the end of 2010. The cost reduction in SARDANA is addressed through the introduction of the latest technological advances that enhance performance of the FTTH/B access networks and minimize infrastructure requirements. [SARDa]

One of the technological performance upgrade objectives imposed by the SARDANA consortium in the beginning of 2008 was an implementation of a Medium Access Control (MAC) protocol that could support higher transmission rates than standardized P2MP FTTH/B solutions [SARDa]. At that moment, Gigabit-capable Passive Optical Network

(GPON) was the most advanced P2MP FTTH/B system in terms of offered bandwidth per subscriber being an outstanding reference for the next-generation FTTH/B MAC protocol design. Consequently, the SARDANA MAC protocol is based on the Telecommunication Standardization Sector of International Telecommunication Union (ITU-T) G.984.3 GPON Transmission Convergence (GTC) layer recommendation [ITU08] that specifies GPON MAC protocol for up to 2.48832 Gbps symmetrical transmission rates [Soi08].

The topic of this thesis is the design and implementation of the SARDANA MAC protocol. Following the original ITU-T notations, SARDANA optical access network system is referred in this text to as SARDANA 10 GPON (SXGPON) and its MAC protocol implementing layer as SARDANA 10 GTC (SXGTC) layer, respectively.

The goal of this thesis is to design the SXGTC protocol and its first Field Programmable Gate Array (FPGA) implementation version for Optical Network Units (ONUs) to be used in the SARDANA test and demonstration network. The transmission rate targets for the SXGTC protocol are [Soi08]:

- 10 Gbps in the downstream (DS),
- 2.5 Gbps, 5 Gbps and 10 Gbps in the upstream (US).

The transmission rate targets for the first ONU SXGTC layer FPGA implementation are [Soi08]:

- 10 Gbps in the DS,
- 2.5 Gbps in the US.

The development process of the SXGTC layer was severely constrained by time and human resources. Following these constraints, this thesis aims to design and optimize the SXGTC layer in such a way that it would allow a straightforward implementation of the SXGTC layer in an FPGA. On the other hand, this thesis targets to include all relevant original GTC protocol functionalities required by the SARDANA test and demonstration network.

This thesis researches how to modify the GTC protocol to support the transmission rates specified for SXGPON, how to optimize the GTC protocol with respect to functional requirements, performance, FPGA related technological constraints, and workload to obtain a balanced SXGTC protocol solution, how to analyze the resulting SXGTC protocol bandwidth efficiency and throughput, how to implement the ONU SXGTC protocol in an FPGA with required performance and functionalities, and how to test the ONU SXGTC protocol FPGA implementation for correct operation without in-hardware verification. The in-hardware testing is not yet possible to perform because some hardware and software components of the SARDANA network are still developed. The emphasis of this research is put on reducing the design time and achievement of the required functionality.

The structure of this thesis follows the logical path of the SXGTC layer design and implementation process. The topics consequently mirror the required knowledge of modern and future technologies as well as the constraint-based design approach. The following chapters focus on presenting the SXGTC layer design process from the ONU perspective because the implementation of the ONU SXGTC layer was assigned to the writer.

Chapter 2 concentrates on the basic concepts and technological principles related to optical access network systems. Furthermore, it gives an insight on the current and the next-generation standards and a perspective on the long-term evolution of the optical access network technologies. Chapter 3 focuses on the SARDANA project, network architecture and network elements portraying the operational environment for the SXGPON system.

Chapter 4 provides an introduction to the FPGA-based digital system design and discusses the FPGA design methodology that was adopted and used in this thesis for the ONU SXGTC layer FPGA design, implementation and testing. Chapter 5 presents a logical model of the SXGTC layer. Chapter 6 describes the design of the SXGTC layer details and a number of optimizations carried out in order to fulfil the goals of this thesis. Chapter 7 analyses the SXGPON system overhead against a reference GPON system overhead presented in the literature, and evaluates the expected throughput of the SXPON system. Chapter 8 offers a high-level view on the ONU SXGTC layer implementation. Chapter 9 presents the SXGTC layer design and implementation results, and discusses future considerations.

2 Passive Optical Access Networks

This chapter serves as an introduction to passive optical access networking. Sections 2.1-2.4 present some basic technological concepts and principles used in passive optical access networks. Section 2.5 glances through the current and the future passive optical access network system standards and discusses the commercialization of these systems. Section 2.6 portrays a view on long-term evolution of passive optical access networks. Section 2.7 summarizes in short the key points of chapter 2.

2.1 Access network

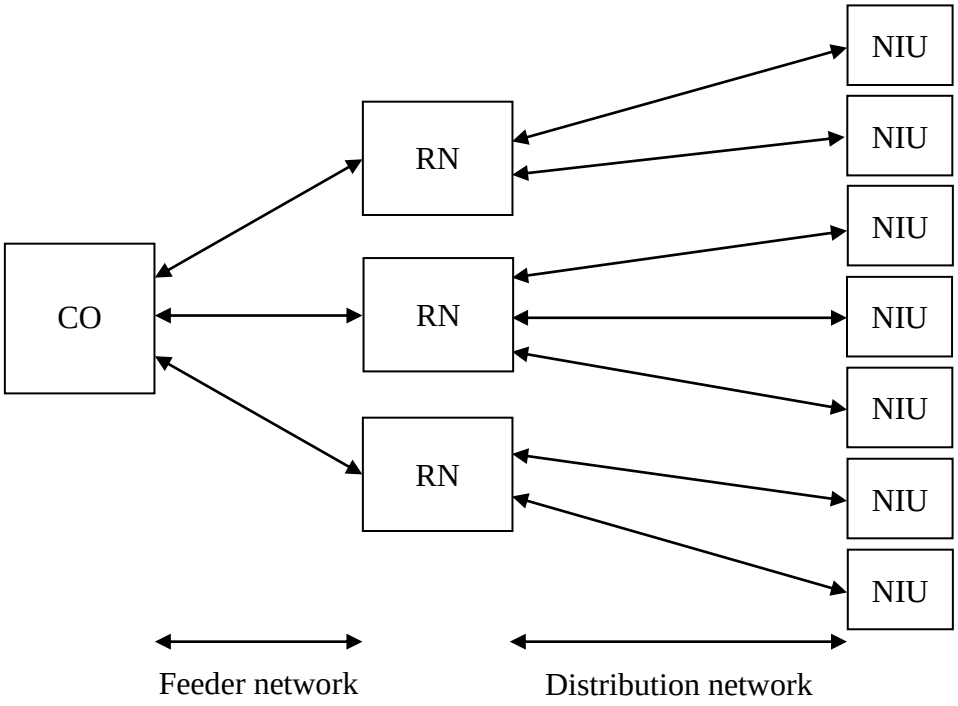

Figure 1. High-level architecture of an access network.
Adopted and modified from [RS02, p. 594, Fig. 11.1].

An access network is a network that connects a service provider with its home or business subscribers. The architecture of an access network (Figure 1) is composed of three major components [RS02, p. 593]:

- The first component is a hub, which is usually referred to as **Central Office (CO)**.
- The second component is referred to as **Remote Node (RN)**.
- The third component is referred to as **Network Interface Unit (NIU)**.

The CO notation will be used throughout this document. The CO is located at the service provider end and can be thought of as being either a source of data fed into the access network towards the user end or a part of a larger network. The CO is connected to a number of RNs deployed in the field that in turn are connected to a number of NIUs. A NIU may serve one or more subscribers and is usually found very close to or in the subscriber's location. Furthermore, an access network can be seen to consist of two different networks (Figure 1) [RS02, p. 593]:

- Distribution network is the network that connects the RNs with the NIUs.
- Feeder network is the network that connects the CO with the RNs.

2.2 Fiber-To-The-x (FTTx)

Today mainly two different access network architectures utilizing optical fiber are commercially deployed in the field. These are Hybrid Fiber Coax (HFC) and Fiber-To-The-x (FTTx). Both architectures comply with the general high-level access network architecture presented in the Figure 1. The structure of HFC is such that the feeder network takes advantage of the optical fiber as transmission medium and the distribution network employs coaxial cable infrastructure that has already existed in many places for many years. The concept of HFC is however out of scope of this thesis and will not be discussed any further. [RS02, p. 595, 598]

In FTTx, optical fiber is used in both feeder and distribution networks. The x letter in the FTTx usually stands for Cabinet (Cab), Curb (C), Building (B), Home (H) or Premises (P) depending on how close the optical fiber is drawn with respect to the subscriber's location. The rest of the transmission path between the x and the subscriber is electrical. The architectures are listed in the descending order with FTTCab having the longest and FTTH and FTTP the shortest electrical connections. These typical FTTx concepts according to [RS02, p. 599-600] are shown in Figure 2.

- In the first FTTCab architecture the fiber is terminated in a cabinet within 1 km radius from the subscriber. Usually some form of DSL technology over copper cable is used between the cabinet and the subscriber [FTTH09c].

- The second architecture is referred to as FTTC or FTTB. Here the optical fiber is typically terminated within the distance of about 100 m from the subscriber. The copper-based connection to subscriber is then organized using DSL or Ethernet [FTTH09c].

- In the last case that is referred to as FTTH or FTTP, the optical fiber goes straight to each subscriber's home.

On the subscriber end of the Optical Distribution Network (ODN), optical fiber is terminated with a node that is usually referred to as either:

- **Optical Network Unit (ONU)** or
- **Optical Network Termination (ONT)** [Lam07].

The ONU notation seems to be more widespread in the literature used for this thesis and hence will be also used in this text. The purpose of the ONU is to serve as an interface between optical and electrical medium. On the CO end, the feeder network is terminated with

- **Optical Line Terminal (OLT)**.

The purpose of the OLT [Lam07, p. 19-20, 152-153] is to multiplex transmissions of all ONUs belonging to the same access network and provide an interface from the access network to either a large network or some service.

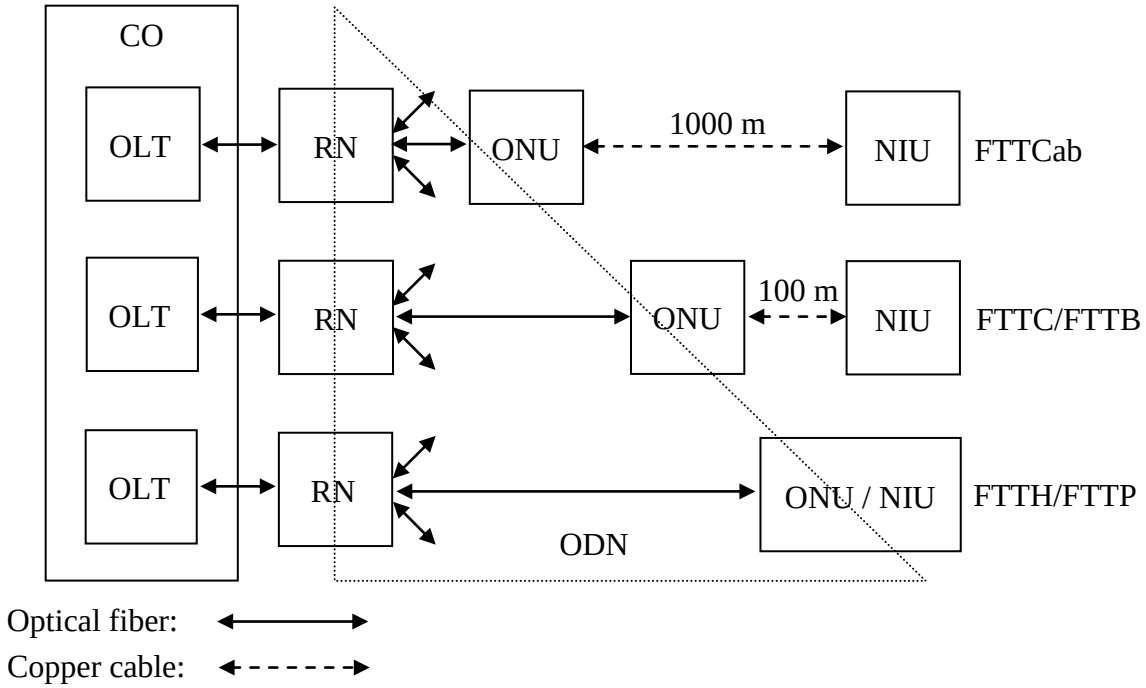

Figure 2. Different types of FTTx architectures.
Adopted and modified from [RS02, p. 600, Fig. 11.5].

2.3 Passive Optical Network (PON)

The FTTx architectures can be based either on an active RN or a passive RN. A network with an active RNs is referred to as Active Optical Network (AON). An active RN is an electronic device that requires constant power supply and backup power. This device can be an optical power amplifier or electronically more sophisticated switch. Furthermore, an active RN requires a cabinet for its placement. These features raise the total cost of the FTTx deployment and operation. [Zak04][KP02]

A passive RN-based FTTx access network is referred to as Passive Optical Network (PON). The passive component used, is usually an optical star coupler or a static wavelength router. This coupler or router combines the transmissions of different ONUs to the OLT in the upstream (US) and divides the transmission from the OLT to the ONUs in the downstream (DS). [RS02, p. 601]

Cost is identified as the major obstacle for worldwide FTTx deployments [CPG+06]. The FTTx access networks must hence be cheap and simple to build, operate and service. The motivation for using the passive architectures comes from the fact that they do not utilize any switching and need to be powered only in the end points that noticeably lowers the price of their operation compared to the AONs. Other advantages of using PONs are their reliability, easy maintenance and possibility for upgrade without infrastructure modifications. [RS02, p. 601]

There is a variety of proposed PON architectures and their modifications introduced in the literature. PON is generally referred in the literature to be a P2MP system due to the existence of the RN in the network [FTTH09c]. However, some literature sources such as [RS02, p. 601-602] argue that point-to-point (P2P) optical access network can be also considered a PON. This is due to the fact that P2P connection is completely passive between the OLT and the ONU. While the latter argument might sound closer to the precise PON term, this thesis will adopt the more widespread P2MP definition for PONs. Furthermore, this thesis will focus only on passive P2MP optical access systems.

2.4 Passive Optical Network architectures

2.4.1 Time Division Multiplexed Passive Optical Network (TDM-PON)

Time Division Multiplexed Passive Optical Network (TDM-PON) in Figure 3, originally referred to as Telephony on PON (TPON) [SBF+87], is the most common commercial PON architecture. Bidirectional transmission is based on Wavelength Division Duplex (WDD). In the DS direction the OLT broadcasts the traffic through an optical power splitter to all the ONUs in the access network. Correspondingly, all broadcasted information is received at every ONU. The data streams for different ONUs can be virtually differentiated using

ONU address labels that are embedded in the transmission. At the ONU, only the relevant data with correct address labels is processed and all other data is discarded. There is an apparent security issue as the data intended for one ONU also reaches all the other ONUs in the PON. To avoid information security problems, commercial TDM-PONs use encryption. [RS02, p. 603] [Lam07, p. 21-22]

The US ONU transmissions are coupled through the same optical power splitter. Time Division Multiplexing (TDM) is employed in order to avoid the collisions between transmissions of different ONUs in the feeder network. The TDM-based method for accessing the transmission medium is referred to as Time Division Multiple Access (TDMA). A MAC protocol is required in order for TDMA to be supported. Variable length transmission time slots can be assigned for each ONU depending on the required Quality of Service (QoS). This mechanism is commonly known as Dynamic Bandwidth Allocation (DBA). [RS02, p. 603-604]

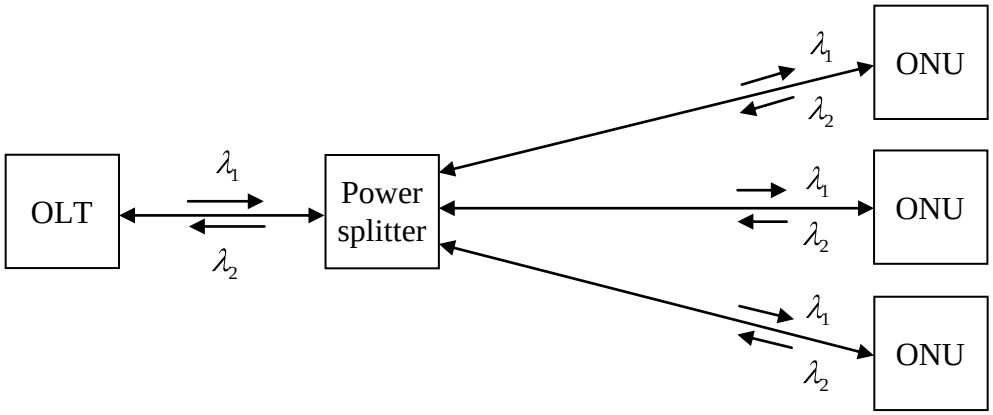

Figure 3. An example of a one-stage splitting TDM-PON architecture. Adopted and modified from [Lam07, p. 29, Fig. 2.9a].

Comparatively mature low-cost optical transmitters and receivers can be successfully used in both the OLT and the ONU. The ONU electronics must run with the aggregate bit rate of the system raising the complexity and the cost of the ONU. Due to the P2MP architecture, the cost of the TDM-PON OLT can be shared among the subscribers. [RS02, p. 604]

There are three basic alternatives to organize P2MP connection using power splitters [Lam07, p. 29-30]:

- The first alternative is a one-stage splitting architecture shown in Figure 3.
- The second possibility is to use cascaded splitters in the field like in
- Figure 4.
- In the third approach depicted in Figure 5, the feeder network is actually an optical bus connected to the ONUs at different locations along the network.

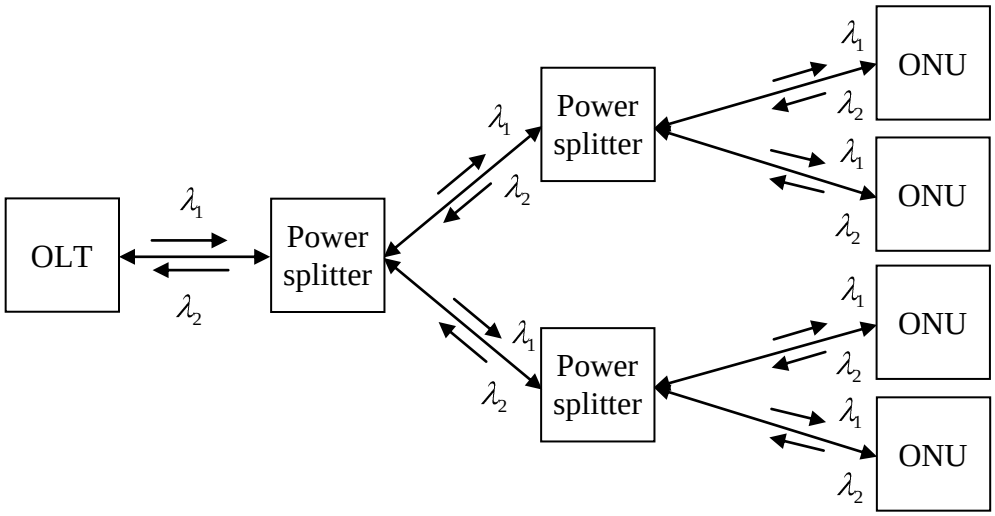

Figure 4. An example of a multistage splitting TDM-PON architecture.
Adopted and modified from [Lam07, p. 29, Fig. 2.9b].

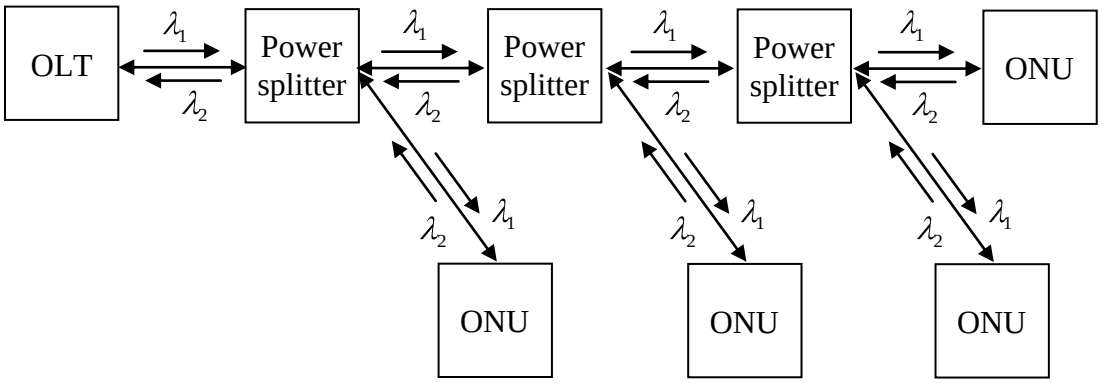

Figure 5. An example of an optical bus TDM-PON architecture.
Adopted and modified from [Lam07, p. 29, Fig. 2.9c].

The splitting architecture used in practice strongly depends on the demographic locations of the subscribers. In the one-stage architecture the splitter can be in principle put at the OLT location. This simplifies network maintenance and minimizes splicing and connector losses but on the other hand increases fiber mileage. A high splitting ratio allows to reduce fiber mileage in the field and share the cost of the OLT among more ONUs but on the other hand it has an immediate impact on the system power budget and transmission loss. Therefore, it is vital for a system with high splitting ratio to have high-power transmitters, high-sensitivity receivers and low-loss optical components in order to cope with the losses. Furthermore, a high splitting ratio decreases the amount of available bandwidth per subscriber because all ONUs share the channel. This limits the maximum number of subscribers in the PON. Most of the commercial TDM-PONs have 1:16 or 1:32 splitting ratios. [Lam07, p. 29-30]

2.4.2 Wavelength Division Multiplexed Passive Optical Network (WDM-PON)

The term Wavelength Division Multiplexed Passive Optical Network (WDM-PON) is used somewhat loosely to describe a PON that employs Wavelength Division Multiplexing (WDM). A common feature of WDM-PONs is that separate wavelengths are used for each ONU in the DS. In the US, traffic multiplexing can be achieved either by WDD or Time Division Duplex (TDD). Hence a variety of different WDM-PON architectures are possible. Some of the cornerstone WDM-PON architectures are reviewed in [BPC+05]. [BPC+05]

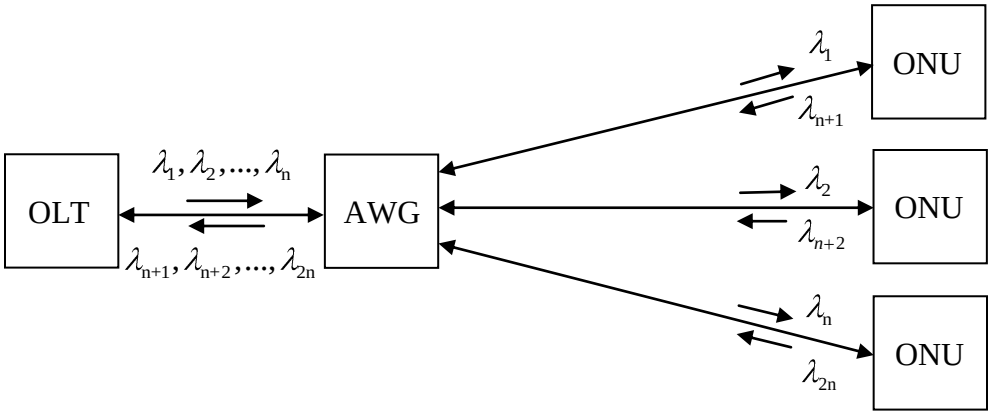

Figure 6. An example of a WDM-PON architecture.
Adopted and modified from [BPC+05, p. 740, Fig. 1].

The usage of a separate wavelength in the DS provides superb information security since each ONU receives only the information that is intended for it. Different wavelengths can be assigned different bit rates according to the required QoS, and the ONU electronics can run at the data receive rate. The WDM-PON OLT is quite costly because it needs to have an array of transceivers to be able to operate on different wavelengths. The cost of the WDM-PON OLT can be shared among the subscribers just like in the TDM-PON case. The WDM-PON ONU also needs to support operation on different wavelengths and hence requires a tunable transceiver that is a relatively expensive component. [RS02, p. 605-606] [BPC+05]

An Arrayed Wave Guide (AWG) router that is a wavelength routing passive optical device is usually used as a RN (Figure 6). This router separates different wavelengths to the different ONUs in the DS and removes the splitting loss problem that would arise if a basic optical power splitter was used instead. In the US direction, AWG router simply passes through all transmitted wavelengths within the transmission band. [BPC+05]

2.4.3 TDM-PON vs. WDM-PON

Bandwidth demands are constantly growing with new evolving services and increase in the number of users requiring enhanced access network performance. The performance of TDM-PON systems is limited by mainly two factors [Lam07, p. 30] [RS02, p. 604]:

- The ONUs must run at the aggregate bit rate of the whole PON making the hardware design more difficult with higher transmission rates.
- The splitting ratio introduced by the passive splitter that limits:
    - the maximum number of ONUs in a PON,
    - the maximum reach of a PON decreasing scalability,
    - the bandwidth per ONU-ratio because the channel is divided among the ONUs.

These TDM-PON problems can be shunned with the WDM-PON that in contrast to the TDM-PON features [RS02, p. 603-609]:

- Each ONU operates on an individual bit rate relaxing the hardware requirements.
- The usage of the AWG router removes the splitting loss problem increasing the reach and scalability of the WDM-PON architecture.
- Each ONU can be assigned an individual wavelength to provide a high bandwidth per ONU-ratio.

The WDM-PON however has one main drawback [Lam07, p. 21]:

- The WDM-PON architectures are generally significantly more expensive than the TDM-PON architectures because of the more costly optical components. Some technological challenges related to the practical WDM-PON systems are discussed in [Chu06].

2.5 Passive Optical Network standards

There are several standardized TDM-PON fiber access systems for FTTx but there are still no standards based on WDM-PONs. The success of TDM-PONs in standardization is due to the fact that WDM-PONs are simply more expensive as compared to TDM-PONs [Lam07, p. 21]. In this section, the TDM-PON standards are presented in short to introduce the framework of the current and future PON systems.

2.5.1 Broadband Passive Optical Network (BPON)

In 1995 the world's leading telecommunication operators and manufacturers founded Full Service Access Network (FSAN) group to develop for optical access network standards capable of delivering a full set of narrowband and broadband telecommunication services [QBC+98]. The first TDM-PON system developed by FSAN was called Broadband Passive Optical Network (BPON). It is based on Asynchronous Transfer Mode (ATM) and is sometimes referred to as Asynchronous Transfer Mode Passive Optical Network (APON). The first BPON standard was published in 1998 in the ITU-T G.983 series recommendations [ITU09]. The ITU-T G.983.1 recommendation [ITU98] specified the aggregate transmission rates for up to

- 622.08 Mbps in the DS,
- 155.52 Mbps in the US.

Since then the G.983 series recommendations have been refined several times. The latest release of the G.983.1 recommendation [ITU05] specifies the aggregate transmission rates for up to

- 1.24416 Gbps in the DS,
- 622.08 Mbps in the US.

2.5.2 Gigabit-capable Passive Optical Network (GPON)

The next generation ITU-T PON referred to as Gigabit-capable Passive Optical Network (GPON) was also developed by FSAN. It is defined in the ITU-T G.984 series recommendations [ITU09] first published in 2003. The G.984.2 recommendation [ITU03] specifies the aggregate GPON system transmission rates for up to

- 2.48832 Gbps in the DS,
- 2.48832 Gbps in the US.

However, only up to 1.24416 Gbps US rates are used in practice with current technology as 2.48832 Gbps US link is still studied [Lam07, p. 44]. The GPON transportation mechanism is referred to as GPON Encapsulation Method (GEM).

2.5.3 Ethernet Passive Optical Network (EPON)

ATM did not achieve the position of a universal network protocol but Ethernet seems to have attained this goal. The Ethernet was adopted in PON technology by the Institute of Electrical and Electronics Engineers (IEEE) in 2004. This Ethernet-based PON is known as Ethernet PON (EPON) but is sometime also referred to as Gigabit EPON (GEPON). EPON is now a part of the IEEE 802.3 standard [IEEE08]. EPON offers the aggregate symmetrical line rates of:

- 1.25 Gbps in the DS,
- 1.25 Gbps in the US.

Due to 8B/10B line-coding, 20 % of the line rate is lost. For this reason, the DS and the US transmission rates of EPON are also often referred to be 1 Gbps. [Lam07, p. 43, 54, 59]

2.5.4 10 Gigabit Ethernet Passive Optical Network (10GEPON)

To address the growing bandwidth demand [CKH+09], the IEEE has recently developed a next-generation EPON standard IEEE802.3av referred to as 10 Gigabit Ethernet Passive Optical Network (10GEPON). The standard was published in September 2009 [IEEE09] and defines the aggregate line rates for up to:

- 10.3125 Gbps in the DS,
- 10.3125 Gbps in the US.

2.5.5 10 Gigabit-capable Passive Optical Network (XGPON)

As of November 2009, the FSAN is currently working on the next-generation GPON standard that is referred to as 10 Gigabit-capable Passive Optical Network (XGPON). The X corresponds to the Roman numeral X that is equivalent to 10 in decimal numeral system. The evolution towards XGPON will be performed in two phases. It is expected to encounter severe clock and data recovery related technological challenges in the practical OLT receivers at or above 5 Gbps transmission rates due to the discontinuous US transmissions of ONUs. [KBC09] [ME09]

In the first phase, XGPON is planned to achieve 10 Gbps transmission rate in the DS and n*2,5 Gbps in the US, where n is 1, 2 or 3. This asymmetric XGPON is referred to as XGPON1. The second phase will result in symmetric 10 Gbps DS and US XGPON that is referred to as XGPON2. FSAN expects XGPON2 to become practical in a longer time frame. Other XGPON system parameters are expected to be the same or better than those of

the ITU-T G.984 series GPON. The current standard development time frame is 2009-2012 for XGPON1 and 2013-2015 for XGPON2. [KBC09] [ME09]

2.5.6 Commercialization of Passive Optical Networks

GPON and EPON were the two competing systems in the beginning of 2009 due to the fact that GPON and EPON offered more bandwidth per subscriber than BPON. EPON has mostly thrived in Eastern Asia countries such as China, Korea and Japan [BPM09], whereas GPON has succeeded very well in the North America [Lam07, p. 70]. According to [PLC+09] it is likely that the first commercial 10GEPON solution will be deployed in 2010 in Asia and 2012-2015 in Europe. There is also a lot of interest among operators and vendors towards development of XGPON. For instance, Ericsson has recently demonstrated its non-standardized XGPON solution [Eri08] which is not however available commercially.

GPON is a more advanced system than EPON from the technological parameters point of view. It provides higher bandwidth efficiency and higher splitting ratio but generally costs more than EPON. The cost per EPON ONU link was about 78 % compared to that of GPON in 2008 [GE08]. According to [BPM09], the EPON worldwide revenue in the fourth quarter of 2008 was about twice than that of GPON. However, it is forecasted in [BPM09] that the GPON revenue might eventually not only overhaul the EPON revenue but become approximately 3 times higher in 2013. There exists also an entirely opposite forecast, where EPON still leads the race [Tek09].

2.6 Evolution from TDM-PON to WDM-PON

The latest propositions for the next-generation PONs are usually referred to as Next-Generation Passive Optical Networks (NG-PONs). The most general requirement for an NG-PON is that it should have better techno-economic performance than current PONs. The main features of NG-PON according to [LPC+08] are listed below:

- long reach,
- high number of users,
- high speed,
- high bandwidth per user,
- single fiber interface,
- strictly passive outside plant,
- simple scalability and upgradeability,
- easy migration,
- multi-operability (fiber infrastructure shared by several operators),

- centralized management and monitoring,
- resiliency and traffic balancing,
- colorless i.e. wavelength-independent ONU equipment,
- robustness.

It is a common view that due to the drawbacks discussed in section 2.4.3 the next-generation TDM-PON systems can hardly provide adequate performance for future optical access networks with increased traffic. It is expected that TDM-PONs will eventually evolve into WDM-PONs. The cost of WDM-PON is however a very serious obstacle. The most promising migration path towards the WDM-PON is an approach often referred as Hybrid WDM/TDM-PON. This PON combines the features from both TDM-PON and WDM-PON in a flexible way and allows more cost efficient network design. [GE08]

The main techno-economical idea behind the Hybrid WDM/TDM-PON is that each wavelength of WDM-PON is multiplexed in time between the ONUs. This allows sharing the cost of the WDM/TDM-PON among a larger number of users, thus reducing the cost per user as compared to WDM-PON. The key concepts and architectural variants related to the WDM-PON evolution as seen in 2007 and 2008 are reviewed in [MPLP07] and [GE08], respectively. Furthermore, the techno-economical comparison in [MPLP07] shows that one particular Hybrid WDM/TDM-PON architecture referred to as SARDANA offers the most cost efficient migration path towards broadband NG-PONs. SARDANA architecture will be presented in detail in chapter 3.

2.7 Summary

This chapter presented an overview of passive optical access network technologies and architectures that are gradually replacing DSL. The current and future FTTx PON standards were discussed. Furthermore, the current FTTx PON market situation was partly covered in addition to FTTH/B household penetration reports already introduced in chapter 1. The future PON market prognoses were also referred to in order to present the near-future commercial FTTx PON eco-system.

This chapter also portrayed the long-term evolution path for PONs. The aim of this chapter was to present the basics of optical access networking and point out that FTTx is coming in form of TDM-PONs. The FTTx PON evolution began with 1 Gbps TDM-PONs and is now continuing with the 10 Gbps TDM-PONs. Moreover, a gradual transition to WDM-PONs using Hybrid WDM/TDM-PONs as an intermediate step is expected in the longer time frame.

3 Scalable Advanced Ring-based Passive Dense Area Network Architecture (SARDANA) Research Project

This chapter offers an insight on SARDANA research project. SARDANA project goals and environment are discussed in section 3.1. Section 3.2 presents the SARDANA concept network and section 3.3 the SARDANA demonstration and test network. Section 3.4 focuses on the SARDANA CO equipment and section 3.5 on the SARDANA OLT. Section 3.6 describes the SARDANA feeder and distribution networks. Section 3.7 discusses the SARDANA RN. Section 3.8 presents the SARDANA ONU and section 3.9 summarizes in short the key points of chapter 3.

3.1 SARDANA project overview

SARDANA is an NG-PON research project funded by the European Commission. The aim of this project is to design and demonstrate an optical access network that is capable of providing all the features required from the NG-PON that were discussed in section 2.6 and thus extend the limitations of the standardized FTTx TDM-PON solutions. [SARDa]

The key targets of SARDANA are to enhance scalability and robustness of PONs. These enhancements are strongly related to decreasing PON associated investments making the technology more attractive for operators. SARDANA is primarily intended for operators whose strategy is to invest in an easily scalable network that enables continuous increase in the number of network users. [SARDa][LPC+08]

There are several partners contributing to SARDANA [SARDc]. The partners and their responsibilities are enlisted below:

- Universitat Politècnica de Catalunya, Spain.
  Responsibilities: project coordination, subsystem design.

- France Telecom – Orange, France.
  Responsibilities: architecture definition, field-trial, technical management, techno-economic studies.

- Tellabs, Finland.
  Responsibilities: OLT and ONU equipment provision, MAC protocol, lab demonstrations.

- Intracom, Greece.
  Responsibilities: service platform, management and control planes.

- Instituto de Telecommunicações, Portugal.
  Responsibilities: monitoring system, non-linear transmission.

- High Institute of Communication and Information Technology, Greece.
  Responsibilities: RNs, non-linear amplification.

- Research and Educational Laboratory in Information Technology, Italy.
  Responsibilities: electronic PON impairment compensation, techno-economic studies.

3.2 SARDANA network architecture

The SARDANA network architecture is shown in Figure 7. The architecture is based on a double-fiber ring that is used to enhance network scalability and resilience against failures. The transmission scheme of SARDANA takes advantage of Dense WDM (DWDM) [ITU02] with 32 wavelengths. Each wavelength is multiplexed in time between different ONUs in both the US and the DS. This approach makes SARDANA a Hybrid WDM/TDM-PON. [LPC+08]

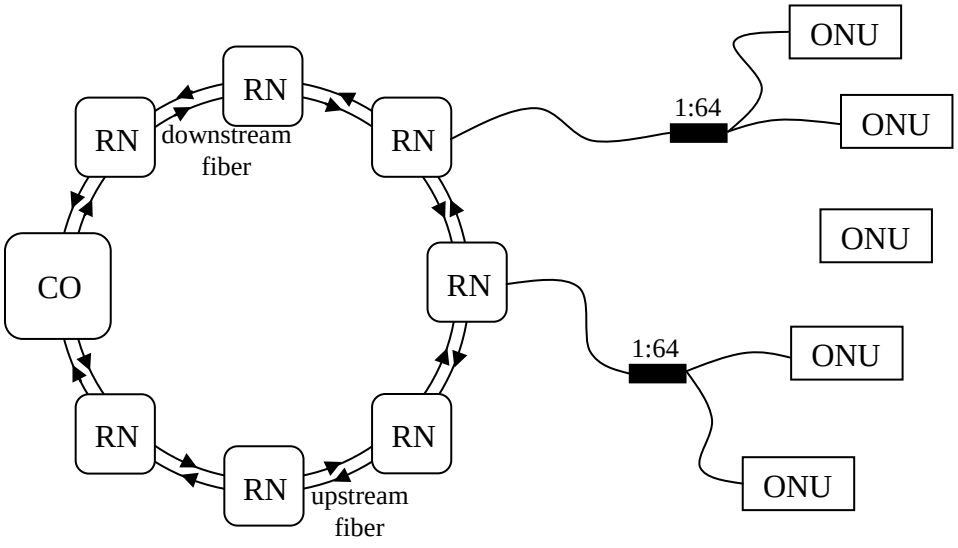

Figure 7. SARDANA network architecture.
Adopted and modified from [LPC+08, Fig. 1].

In the DS, the DWDM wavelengths are transmitted from the CO along the DS fiber ring. Each RN routes the predefined wavelength to a single-fiber access tree connected to it, and correspondingly to all ONUs in the access tree. The splitting factor of each access tree can

be for up to 1:64. This enables for up to 64 ONUs to share the same wavelength in time domain. The maximum number of the ONUs in the SARDANA network is thus 2048. [LPC+08]

The ONUs transmit in the US direction on the same wavelength they receive the DS transmission. These US transmissions are coupled by the RNs to the US fiber ring and delivered to the CO. The signals are transmitted over the double-fiber ring between the CO and the RNs according to the less attenuated path. Bidirectional communication on the same wavelength over single fiber is achieved by means of orthogonal modulation or careful control of reflections. The SARDANA system operates in full-duplex mode. The alternatives for modulation formats are under investigation. [LPC+08][SARDb]

The maximum number of ONUs in the network is dependent on the optical link budget and the number of wavelengths used. The optical link budget is limited by the access tree splitting ratio and the distances between the CO and the ONUs. The number of wavelengths is restricted by the amount of DWDM wavelengths and a number of available laser sources. Since each wavelength is multiplexed in time domain, the maximum transmission rate per ONU heavily depends on the number of ONUs operating on that wavelength. Table 1 demonstrates these relations.

Table 1. SARDANA network study scenarios. Copied from [PLC+09].

Scenarios	Urban 1	Urban 2	Metro	Rural	Collector
Maximum CO-ONU distance (km)	20	20	60	100	20/60
Ring length (km)	17	10	50	80	80
Feeder network length (km)	2,9	9	9	19	19
Distribution network length (km)	0,1	1	1	1	1
Number of wavelengths	32	32	16	16	16
Splitting ratio	1:64	1:32	1:32	1:16	1:8
Number of ONUs	2048	1024	516	256	128
Guaranteed bandwidth/ONU (Mbps)	>140	>280	>280	>560	300/1000

Scalability is achieved by the fact that when the amount of users increases, new TDM trees can be added to the existing main WDM double-fiber ring. The network can be easily modified according to the geographical and functional scenarios, distances, user density and user distribution. Five different SARDANA network scenarios are defined for transmission and dimensioning studies. These are shown in Table 1. The collector scenario is proposed for other access systems integration study. For instance, DSL can be integrated with the SARDANA network. [PLC+09]

SARDANA was so far proven to be feasible for up to 1024 users in half-duplex mode with 10 Gbps DS and 2.5 Gbps US transmission rates. There is now ongoing research to achieve 2.5 Gbps, 5 Gbps and 10Gbps US transmission rates in full-duplex mode. Table 2 summarizes the results from [LPC+08] and [LBP+07].

Table 2. SARDANA half duplex mode proof-of-concept.

Number of ONUs	Ring (km)	DS rate (Gbps)	US rate (Gbps)
512	50	10	2.5
512	100	10	2.5
1024	50	10	2.5
1024	100	10	1.25

3.3 SARDANA test and demonstration network

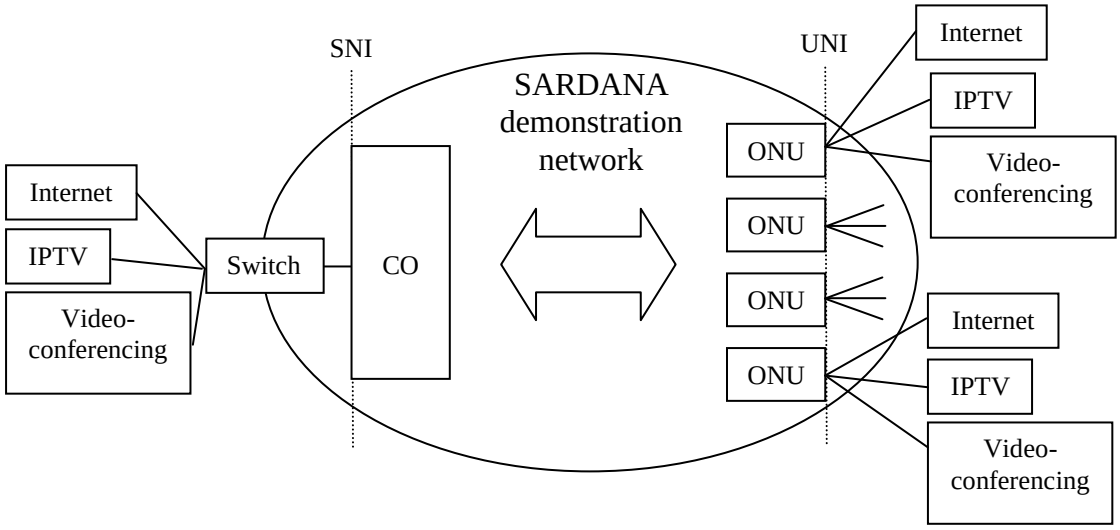

Figure 8. SARDANA test demonstration network.

The SARDANA demonstration network is much smaller in terms of equipment compared to the SARDANA concept network presented in section 3.2. The demonstration network is planned to support at maximum 4 ONUs. Both Service Network Interface (SNI) and User Network Interface (UNI) are based on Ethernet. Three different services are planned to be demonstrated across the network. These are Internet access, Internet Protocol Television (IPTV) and video-conferencing. All service network switching is performed outside the SARDANA network based on the Ethernet Virtual Local Area Network (VLAN) tags in the Layer2/Layer3 Ethernet switch. In the ONUs, each service has a separate physical Ethernet port so that no switching is required in the user network. Figure 8 depicts the intended network configuration.

3.4 SARDANA Central Office (CO)

The SARDANA CO shown in Figure 9 contains a number of SARDANA OLTs that provide different DWDM signal wavelengths and MAC functions for the SARDANA network. Only three OLTs are depicted to simplify the illustration. The CO is responsible for wavelength routing of the DS signal, selection of the strongest US signal from the double-fiber ring, remote amplification pumping to the RNs and overall network performance monitoring. The US and the DS DWDM wavelengths are coupled into the corresponding double-fiber ring fibers through Optical Switches (OS) and wavelength multiplexers (MUX). These allow dynamic adjustment of the transmission direction for each of the wavelengths offering traffic balancing capabilities and providing a connection to all the RNs even in case of fiber failure. Moreover, the CO has an additional Control Plane that is responsible for network control, management, performance monitoring and impairment compensation. The service platform is responsible for the SARDANA network test services, and the switch organizes interconnections between the service platform and the OLTs. [LPC+08] [LPB+06]

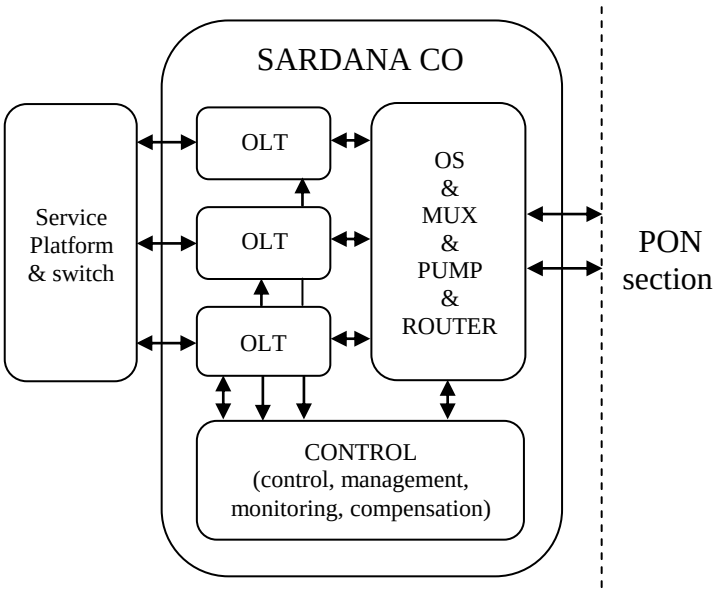

Figure 9. SARDANA CO.
Adopted and modified from [LPC+08, Fig. 2].

3.5 SARDANA Optical Line Terminal (OLT)

The high-level structure of the SARDANA OLT is presented in Figure 10. The OLT transceiver is based on a precise wavelength semiconductor laser transmitter (Tx) and a photo detector receiver (Rx) that are coupled to the single fiber with diplexer. A very precise wavelength laser is required for DWDM. The transceiver details are defined by Physical Media Dependent (PMD) layer and as such are out of scope of this thesis.

The SXGTC layer in the OLT incorporates MAC and service adaptation functions. The service adaptation instance is a signal transformation interface between the PON section and the service platform signals. The service platform connection in the SARDANA test and demonstration network is based on 10 Gbps Ethernet thus requiring only one service adaptation instance in contrast to the standardized TDM-PON systems that might incorporate several different service signal formats such as data and voice.

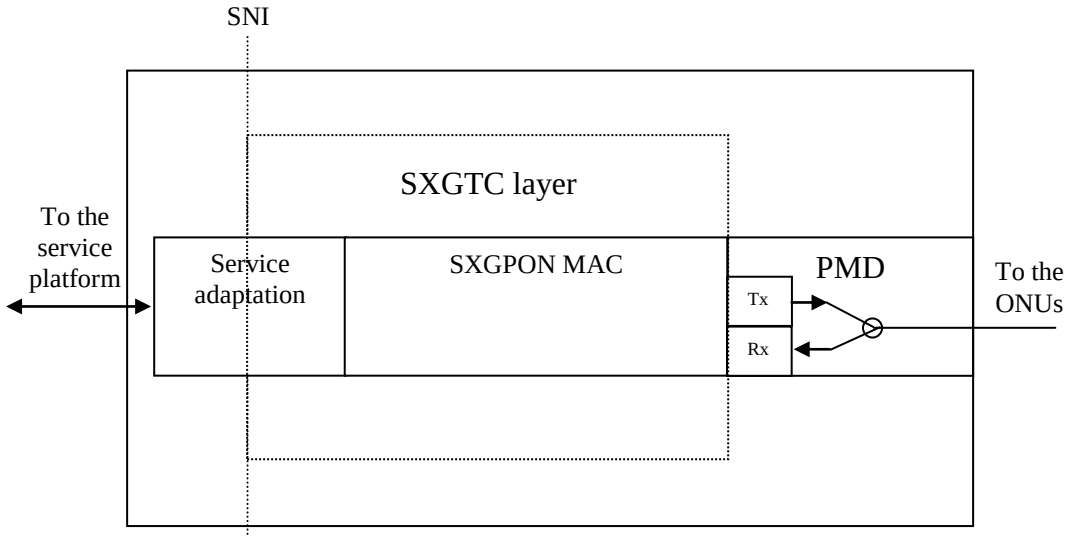

Figure 10. A high-level structure of the SARDANA OLT.
Adopted and modified from [ITU08, p. 13, Fig. 6-1].

3.6 SARDANA feeder and distribution networks

The importance of resilience against failures in the network increases with [LGH04]:

- the amount of data transmitted in the network,
- imposed QoS requirements.

In general, optical fiber is used as transmission medium for connections that require high capacity and consequently high data rates. Furthermore, the amount of users and thus the data rates are constantly growing in the optical networks following latest technological advances. A single fiber cut may affect hundreds of users notably reducing revenue for both the operators and the subscribers. For this reason, protection schemes for optical fiber networks are becoming more and more important [Ehr07]. Availability measures the time the connection is accessible. The common target for unavailability is considered to be 5 minutes/year [RS02, p. 537]. According to [Hea08], the standardized deployed unprotected TDM-tree-based PON architectures in Figure 3, Figure 4 and Figure 5 have the unavailability of up to 47 min/year, 48 min/year and 53 min/year, respectively.

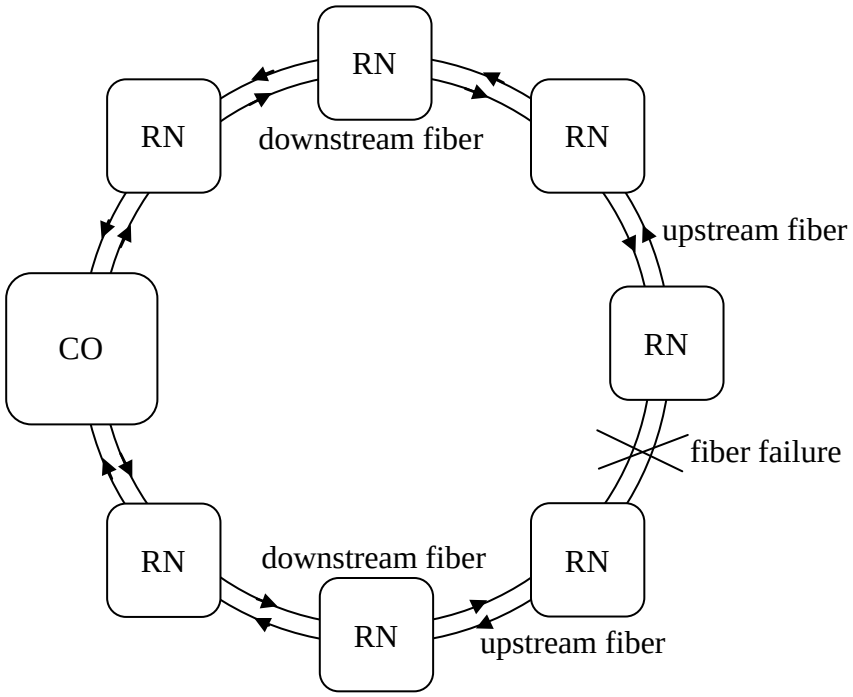

Figure 11. Protection offered by the ring architecture.

The ring-based feeder network architecture of SARDANA provides protection and hence enhances the availability of the access network in case of a fiber cut demonstrated in Figure 11. Furthermore, the ring architecture enables easy network scalability due to the fact that there is no need for a maintenance break in case of a new RN or access tree addition to the network as there exists an alternative transmission path. The double-fiber ring is utilized also for transmission duplexing as the DS and the US traffic are transmitted over different fibers. This scheme optimizes the spectrum and helps to avoid main Rayleigh backscattering impairments. The distribution network of SARDANA is a basic 1:64 single-fiber TDM-PON access tree presented in section 2.4.1 and shown in Figure 3 with the

exception that the DS and the US transmissions take place at the same wavelength. [BPA+08] [LPC+08]

3.7 SARDANA Remote Node (RN)

The SARDANA RN implements two functions:

- routing,
- amplification.

The RN routes different wavelengths from the WDM DS fiber ring to each of the dedicated wavelength TDM access trees in the DS. In the US the RN couples the TDM access trees to the US ring fiber. This functionality is implemented by a 2-to-1 fiber Optical Add Drop Multiplexer (OADM) that allows selecting operating wavelengths for each TDM tree. The RN is thus transparent to all the other wavelengths in the fiber ring. [BPA+08] [LPC+08] [PLC+09]

Moreover, the RN amplifies the optical DS and the US signals passively by means of remote amplification. The remote amplification power is provided by pumping lasers that are found in the CO. The signal amplification is then achieved in the RN by means of Erbium Doped Fibers (EDFs). As of March 2009, possible implementations of the RN are currently studied and the design of RN is still evolving. The most advanced proposition so far is described in [BPA+08]. [LPB+06]

3.8 SARDANA Optical Network Unit (ONU)

In the WDM access architectures, the ONUs should support operation on different wavelengths in contrast to the standard TDM-PON ONUs where every ONU receives on one wavelength and transmits on another. Wavelength-dependent ONUs however cannot be used in WDM networks since the production and management of the ONUs would be infeasible [BPW07]. A straightforward approach using tunable transceivers is quite costly [RS02, p. 603-609]. Recent techno-economic studies [SBP05] and [MPLP07] suggest that colorless i.e. non-wavelength specific ONUs offer reduction in cost of operation, administration and maintenance functions in the WDM networks. Moreover, the cost of the colorless ONU can be further reduced by mass production [LPC+08].

The signal transmission scheme for colorless ONUs in the SARDANA network is such that the OLT lasers provide the wavelengths to be used by the SARDANA ONUs. The ONU transceiver guides most of the received DS signal power to the ONU photo detector but a portion of the DS signal is also coupled to the Reflective Semiconductor Optical Amplifier

(RSOA). This connection is demonstrated in Figure 12. The seeded DS signal applied to RSOA enables stimulated emission on the DS signal's wavelength generating the same wavelength US signal. This way, the ONU can transmit on any of the DWDM wavelengths provided by the OLTs and thus be colorless. The US transmission power of the RSOA is dependent on the RSOA power control circuitry. [Pin07]

The colorless ONU can generate serious amplified spontaneous emission noise and Rayleigh backscattering impairments operating on the same wavelength in both the DS and the US over a single fiber. Moreover, current transmission rates of commercially available RSOAs are limited to 2.5 Gbps. The colorless 5 Gbps and 10 Gbps transmitters based on RSOA, as well as the compensation of impairments for SARDANA are discussed in [POK+08] [OPS+09]. [OPS+09]

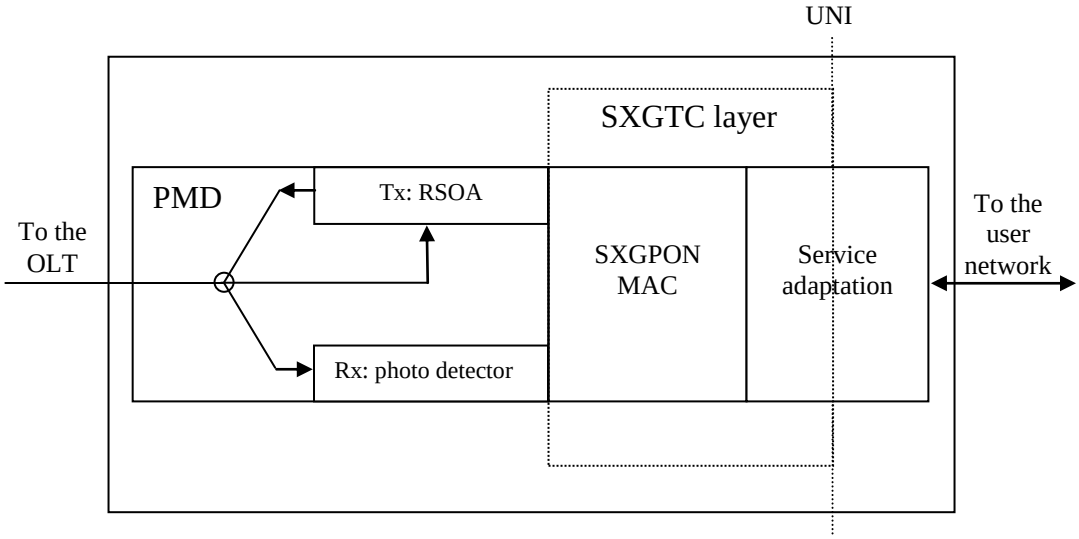

Figure 12. A high-level structure of the SARDANA ONU.
Adopted and modified from [ITU08, p. 14, Fig. 6-2].

Figure 12 shows that the ONU SXGTC layer incorporates MAC and service adaptation functions just like the SXGTC layer in the OLT. The service adaptation instance is a signal transformation interface between the PON section and the client network equipment signals. The UNI in the SARDANA test bed is based on three 1 Gbps Ethernet connections thus requiring only one service adaptation instance for Ethernet. The logical model of the SXGTC layer is discussed in the chapter 5. The implementation details of the ONU SXGTC layer are presented in chapters 6 and 7.

3.9 Summary

This chapter discussed the SARDANA project presenting the its environment, goals, technological approaches and references to related publications for more details. The high-level description was given of the SARDANA network equipment to engage the reader's interest on the latest technological advances in FTTx PONs. The key technologies such as TDM on WDM, DWDM, remote amplification with EDFs and colorless RSOAs researched in SARDANA today, might well be utilized in commercial FTTx networks tomorrow. Furthermore, the SXGTC layer was identified and positioned inside the OLT and the ONU to demonstrate the relation between the functional instances and lay the foundation for the presentation of the logical model of the SXGTC layer.

4 FPGA-based Digital System Design

This chapter begins with a short presentation of a Field Programmable Gate Array (FPGA) and an Application-Specific Integrated Circuit (ASIC) as implementation alternatives for modern complex digital systems in general and the SXGTC layer in particular. Further emphasis is put on the FPGA-based system design as it is a more suitable option for the SXGTC layer implementation as will become clear in section 4.1. Section 4.2 presents the generic FPGA architecture. Section 4.3 covers some data processing related concepts. Section 4.4 discusses goals associated with the FPGA-based design. Section 4.5 introduces the FPGA design flow. Section 4.6 offers a small summary of the topics. The overall purpose of this chapter is to give a short high-level insight on the FPGA technology and design process.

4.1 Complex digital system design options

An FPGA is a fully manufactured programmable device for digital logic implementations. There are both permanently programmed and reprogrammable FPGAs. A reprogrammable FPGA offers a very flexible environment for logic implementation and testing as the FPGA can be reprogrammed as many times as required during the design process. Furthermore, the design process and testing can advance hand in hand as the FPGA program can be continuously refined, uploaded into the FPGA and tested in the hardware environment. [Wol04, p. 8]

Today high-end reprogrammable FPGAs such as Altera Stratix IV [Alt09] and Xilinx Virtex 6 [Xil09a][Xil09b] take advantage of 40-nm semiconductor technology and consist of 680 000 - 760 000 logic elements (LEs) and theoretically support clock frequencies for up to 600 MHz. An FPGA start-up Achronix however, claims to be able to offer up to 1.5 GHz performance with its Speedster FPGA [Ach09]. The maximum clock frequency sets a theoretical limit for the FPGA speed but the real performance of the FPGA design is limited by the design itself.

The most notable alternative to the FPGAs are custom Very Large Scale Integrated (VLSI) purpose-dedicated chips referred to as ASICs. ASICs are designed and optimized for some particular logical task or function. They are first designed and simulated in software and only then manufactured. Manufacturing of ASICs usually takes up to several months and the hardware testing can begin only after manufacturing. ASICs are generally cheaper than FPGAs when manufactured in large volumes but the cost for manufacturing the first 10-20 engineering samples of ASICs can rise up to $ 2-3 millions for the 45-32 nm process technology [WMS+08, p. 21-26]. [Wol04 s. 7-14]

Some FPGAs have one or more CPUs on chip for embedded computing applications and/or several different types of programmable structures for more efficient implementation of specific functions such as Digital Signal Processing (DSP). This class of FPGAs is referred to as platform FPGAs. The platform FPGAs lower the technological performance gap between the FPGAs and the ASICs. In fact, the above mentioned high-end Altera and Virtex FPGAs are platform FPGAs. [Wol04, p. 11, 457, 460]

There are also platform ASIC solutions that target to reduce design time and development costs of an ASIC by offering a basis silicon platform with Intellectual Property (IP) blocks and design methodology. The performance of platform ASICs is generally lower compared to a fully customized ASIC. [Kha05]

The main advantages of reprogrammable FPGAs as compared to ASICs are:

- The FPGA design cycle is simpler and more predictable [Xil09c] than that of the ASIC due to design tools automation. This results in faster time-to-market [Wol04, p. 7-14].
- The FPGAs are much cheaper in small quantities [Wol04, p. 7-14].
- Reprogrammable FPGAs allow early software/hardware integration testing as the design can be loaded into the FPGA quickly at any moment in the field [Smi97, p. 3-5].
- The design can be continuously refined in both software and hardware. Reprogrammable FPGAs are very suitable for design prototyping as they can be reprogrammed as many times as needed [Smi97, p. 3-5].
- The same reprogrammable FPGA can be re-used for different designs [Wol04, p. 7-14].

The main advantages of ASICs as compared to FPGAs:

- ASICs are generally faster and consume less power than FPGAs as they are designed and optimized for some particular task [Wol04, p. 7-14].
- ASIC manufacturing is generally cheaper in very high volumes [Xil09c].

A shorter design cycle and the reprogrammability of the reprogrammable FPGA makes it a more adequate implementation option than ASIC or permanently programmed FPGA for research projects like SARDANA. On the other hand, the high ASIC costs for small digital circuit quantities simply rule out the use of ASIC in SARDANA project.

4.2 Generic FPGA architecture

There are several different approaches to design an FPGA. The three major FPGA circuit technologies are referred to as Static Random Access Memory (SRAM)-based, antifuse-based and flash-based. SRAM-based and flash-based approaches are utilized for the reprogrammable FPGAs, whereas antifuse-based approach is used for the permanently programmed FPGAs. Table 3 summarizes some of the main differences between these technologies. [Wol04, p. 110, 128] [Max06]

Table 3. A comparison of different FPGA programming technologies.
Adopted and modified from [Max06, Table 1].

Feature	SRAM-based	Antifuse-based	Flash-based
Ability to reprogram	Yes	No	Yes
Volatile	Yes	No	No
Power consumption	Medium	Low	Medium
Good for prototyping	Yes (very good)	No	Yes (reasonable)
Reprogramming speed	Fast	-	3x slower than SRAM

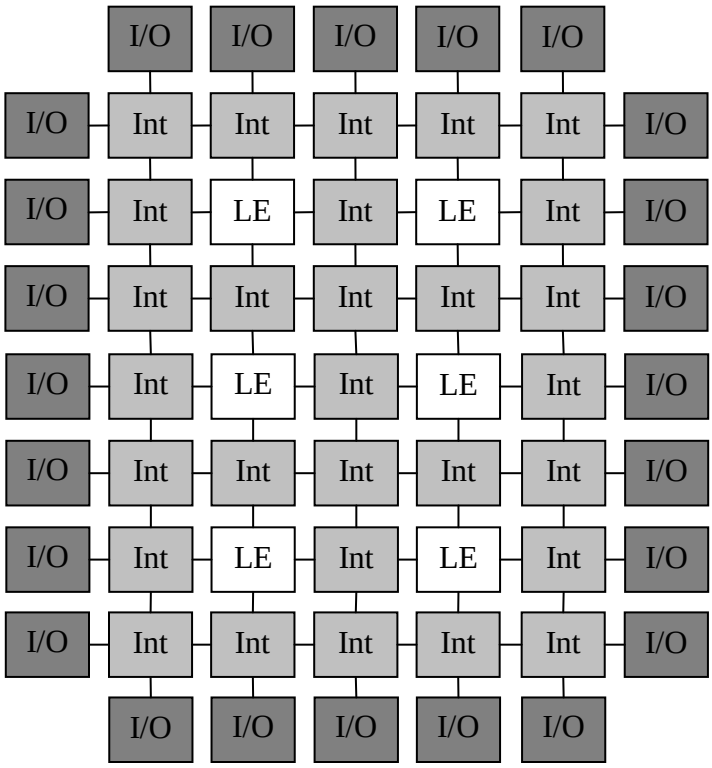

Figure 13. Generic architecture of an FPGA.
Adopted and modified from [Wol04, p. 106, Fig. 3-1].

All three technological approaches however have the same generic high-level FPGA architecture that consists of three types of basic elements (Figure 13):

- Logic Elements (LEs),
- Interconnect (Int),
- Input/Output (I/O) blocks and pins.

The programmability of FPGAs comes from the fact that all three of these basic elements are programmable. I/O blocks and pins are the FPGA signal interfaces to the outside. LEs implement combinational logic functions based on logic gates, multiplexers or Look-Up Tables (LUTs). The LE blocks are usually relatively small as each block can typically form a function equivalent to a combination of several logic gates. The LEs are surrounded by a programmable wiring referred to as interconnect. The interconnect ties the LEs and the I/O blocks together. FPGAs typically offer several types of interconnect structures. Different interconnect types are used for different connection distances between the LEs. Furthermore, clock signals have a separate clock interconnect network to achieve more accurate logic synchronization by minimizing clock delay differences between the distant parts of the FPGA. [Wol04, p. 105-107]

4.3 FPGA clock frequency and data rate

The data rate defines how many bits are transmitted or processed in one second. From the FPGA implementation perspective the data rate can be represented to be directly proportional to the data path width and the data processing frequency i.e. the frequency at which data is processed in the FPGA. The data processing frequency is referred to as clock frequency in the FPGA context. This relationship is represented by

$$\text{data rate (bps)} = \frac{\text{bits}}{\text{second}} = \text{data path width (bits)} \times \text{clock frequency (Hz)}. \quad (1)$$

It is possible to widen or narrow the data path width by some factor and decrease or increase the clock frequency by exactly the same factor, and hence maintain the same data rate. This relationship is demonstrated by Equation (2). This approach is used to process the data rates higher than the FPGA's maximum clock frequency inside the FPGA.

$$\text{data rate (bps)} = \text{data path width (bits)} \times \text{clock frequency (Hz)} \times \frac{\text{factor}}{\text{factor}} \quad (2)$$

The clock frequency is inversely proportional to the data processing time referred to as clock cycle in the FPGA context. This relationship is given by the Equation (3). The length

of the clock cycle restricts the amount and the complexity of logic operations that can be performed during each clock cycle.

$$\text{clock cycle (s)} = \frac{1}{\text{clock frequency (Hz)}} \tag{3}$$

Correspondingly, the complexity of the logic sets a constraint on the minimum clock cycle length and the maximum clock frequency of the FPGA implementation. In fact, the clock frequency of the implementation can be much lower than the FPGA's theoretical maximum clock frequency. The highest implementation clock frequency for a particular design can be only roughly estimated in advance.

4.4 FPGA-based digital system design goals

There are several design goals listed in [Wol04, p.13-14, 168] that form the basis for all FPGA-based system design projects:

- Correctness of logical function. The FPGA design performs all expected operations correctly.
- Performance. The performance of the FPGA design is usually measured in maximum clock frequency, latency and throughput. The FPGA design needs to be run at some required speed i.e. clock frequency. Latency measures how many clock cycles are required to process the data from the input to the output. Throughput defines the maximum amount of data that can be processed in a certain time frame.
- Power consumption and heat dissipation. The FPGA chip must run within defined power and heat dissipation budget. This is estimated when choosing the most suitable FPGA and packaging technology for the design.
- Logic size. The amount of the required logic directly affects the size of the required FPGA and hence has an impact on FPGA cost as larger FPGAs cost more.
- Design time. Design time is usually limited and the time limitation must be taken into account.
- Design cost**.** The design cost must be within project budget limits. The design cost consists of FPGA development platforms, design tools and design time.
- Manufacturing cost. The manufacturing cost defines the cost of system replication and consists of FPGA chips and time spent on FPGA programming.

4.5 Reprogrammable FPGA design flow

The design of a complex chip consumes a lot of time and money. The earlier design errors are found, the easier, faster and cheaper they are to correct. The design flow that is also referred to as design methodology introduces a means to design a chip as fast as possible and with as few errors as possible. [Wol04, p. 414]

Different literature sources use somewhat different terminology in context of the FPGA design flow. The general stages of the flow are however the same. The following detailed reprogrammable FPGA design flow (Figure 14) is generated-based on the analysis of [Wol04, p. 169, 414-416] [Xil09c] and [1-C09].

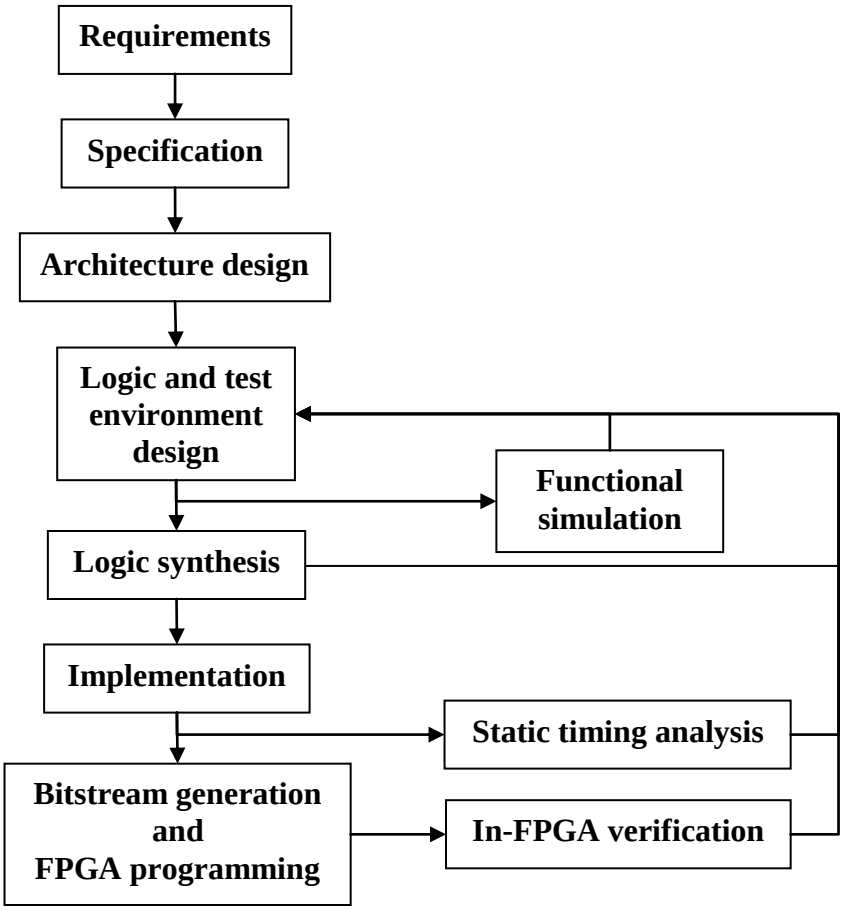

Figure 14. FPGA design flow.
Adopted and modified from [Wol04, p. 414, Fig. 6-32], [Xil09c] and [1-C09].

Requirements and specification

The first step is to document the requirements associated with the design. The requirements are typically more of general nature and are usually originated from customers and marketing. The next step is to reshape the requirements to a detailed technical specification, which describes what exactly needs to be done. If the requirements are misunderstood then the mistake will propagate to all the following design flow steps resulting in a working chip with incorrect functionality.

Architecture design

Architectural design is based on the careful analysis of the requirements and technical specification. The output architecture design consists of a complete device architecture including structural blocks and their functions, data path widths, clock domains as well as inner and outer interfaces. Furthermore, the architecture design includes the architecture of a test simulator referred to as a test bench and a preliminary test suit. The FPGA model for the design is usually chosen during the architecture design stage, because the choice of the FPGA requires understanding of the design implementation details.

Logic design

The device logic is traditionally designed based on textual description using a Hardware Description Language (HDL) but there are also schematics-based alternatives that are usually referred to as graphical tools. Some graphical tool features hasten the design process but the HDL still remains the key instrument that is used to describe the complete design in a generic and understandable way. Today the most widely used HDLs in are Very High Speed Integrated Circuit Hardware Description Language (VHDL) and Verilog HDL [ME08, p. 145-147]. The FPGA program description is provided in these languages on the Register Transfer Level (RTL) meaning that the logic is described with an accuracy of a clock cycle from register to register. In addition to device logic, the test bench is designed in this step.

Functional simulation

In the functional simulation phase, the design is simulated on RTL with a test bench designed for that particular design. If the simulation points out functional errors they are corrected by refining the HDL description. If no errors are found the logic synthesis may begin.

Logic synthesis

In this stage RTL HDL description is optimized and converted to a netlist, which represents a formally written circuit schematic of the design. The synthesis is a fully automated process that is performed in a software. The synthesis may reveal potential errors that may have been left unnoticed in the functional simulation and lead to corrections in the HDL description.

Implementation

In the implementation phase, the netlist is mapped into the internal structure of the FPGA in software. This process is generally referred to as place-and-route as the FPGA resources such as LEs are allocated and interconnected with each other. This process may be fully automated but sometimes a designer's intervention is required to obtain better timing properties.

Static timing analysis

The static timing analysis is performed on the placed-and-routed design. The analysis is based on the software calculations and represents estimated timing properties of the particular design. The two most crucial parameters provided by the analysis are the critical path and the maximum estimated clock frequency that can be applied to design. The critical path defines the longest signal path between two registers. The maximum clock frequency in turn is restricted by the time that is required for a signal to propagate through the critical path. If the maximum clock frequency given by static timing analysis is lower than the target clock frequency, the design is not adequate and a modification of the HDL description is necessary.

Bitstream generation and FPGA programming

A bitstream file is generated after the place-and-route process. The file contains a program that is used to program the FPGA for the particular design. The FPGA is programmed by uploading the bitstream file into the FPGA.

In-FPGA verification

In this final step, the design functionality is verified inside the FPGA initially using some test set-up for easier debugging. The test set-up depends on the FPGA design and future usage environment. Finally, the design is verified in the real application environment. If problems with the design are detected, the HDL description needs to be refined.

Design iterations

Ideally, the design cycle described above is gone through only once. However, that is rarely the case with complex designs, partly due to the complexity and partly due to the fact that early design stages may be based on incomplete information. Advancing in the design accumulates design related information which may point out that some of the previous assumptions were incorrect. This requires going one or more stages back and refining the design.

4.6 Summary

This chapter discussed the alternatives for digital system design in hardware and identified ASICs and FPGAs as two main approaches. The FPGA was considered a more suitable alternative for the SXGTC layer implementation mainly for two reasons. First of all the usage of FPGA for the SXGTC layer is much cheaper due to the million class initial ASIC costs. Secondly, the reprogrammability of the FPGAs makes the technology much more applicable for usage in prototyping and research projects like SARDANA. Moreover, this chapter presented a short introduction to FPGA technologies, design process and design goals to portray the framework for the ONU SXGTC layer design and implementation.

5 SARDANA 10 Gigabit-capable Passive Optical Network Transmission Convergence Layer: Logical Model

The ITU-T G.984.3 GTC layer recommendation [ITU08] specifies the GPON MAC protocol for up to 2.5 Gbps transmission rates for both the US and the DS directions. The transmission rate targets for the SXGPON MAC protocol were set to [Soi08]:

- 10 Gbps in the DS,
- 2.5 Gbps, 5 Gbps and 10 Gbps in the US.

The development process of the SXGTC layer was severely constrained by:

- human resources,
- time.

Due to these constraints, the objective was to develop a straightforward implementation of the SXGTC layer. The requirements for the SXGTC layer imposed by the SARDANA test network allowed for the reduction of the complexity of the G.984.3 recommendation [ITU08] in terms of some not needed GPON related features [Soi08]. On the other hand, the SXGTC protocol had to incorporate all relevant GTC functionalities. These targets served as a starting point for the complete SXGTC layer system design. This and the following chapters concentrate on presenting the SXGTC layer design process from the ONU perspective because the implementation of the ONU part of the SXGTC layer was assigned to the writer.

The target of chapter 5 is to describe the logical model of the SXGTC layer with a special emphasis on the ONU. The manner of representation is such that the logical link to the G.984.3 recommendation [ITU08] is maintained in all contexts. Furthermore, this text addresses also the very first G.984.3 recommendation [ITU04]. Chapter 5.1 portrays the protocol stack of the SXGTC system. Chapter 5.2 introduces the SXGTC layer framing mechanisms. Chapter 5.3 describes the SXGTC layer multiplexing architecture and MAC functions. Chapter 5.4 presents the logical model for the complete ONU SXGTC layer system. Chapter 5.5 serves as a summary of the logical model differences between the SXGTC and GTC layers.

5.1 SXGTC protocol stack

Figure 15 shows the protocol stack for SXGTC layer. The protocol stack and its functions are congruent with those described by the G.984.3 GTC layer recommendation [ITU08].

The main responsibility of the SXGTC layer is:

- To provide traffic multiplexing between the OLT and the ONUs.

The SXGTC layer is situated on top of the SXGPON PMD layer and is offering a transportation mechanism over the PON for SXGTC layer clients found directly above it. The SXGTC layer consists of two sub-layers:

- SXGTC Framing sub-layer,
- SXGTC Adaptation sub-layer.

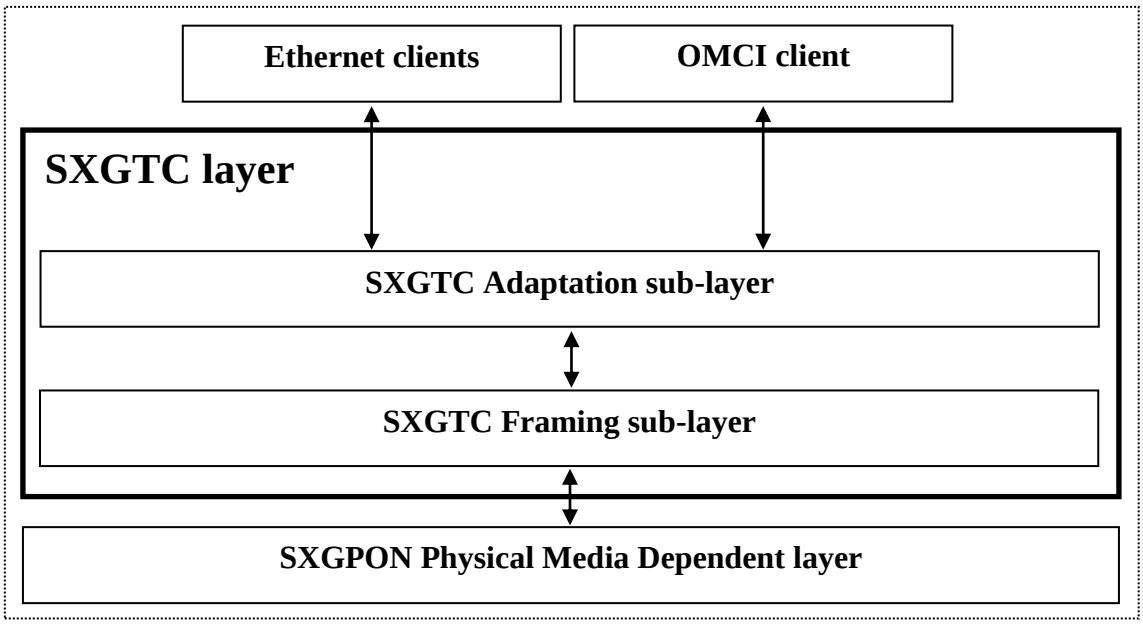

Figure 15. Protocol stack for SXGTC layer system.
Adopted and modified from [ITU08, p. 16, Fig. 7-1].

In the G.984.3 recommendation [ITU08], the GTC layer consists of the GTC Framing sub-layer and the GTC Adaptation sub-layer, respectively. The Optical network unit Management and Control Interface (OMCI) enables management and control of service defining layers found above the SXGTC layer. These higher layers are beyond the scope of this work. The OMCI client is the OMCI message processing entity that communicates with the SXGTC Adaptation sub-layer. The outer interfaces of the SXGPON OLT and ONU are based on Ethernet. The Ethernet clients communicate directly with the SXGTC Adaptation sub-layer.

5.2 SXGTC layer transmission and framing mechanisms

Two different transmission mechanisms are specified for usage inside the GPON system by the original G.984.3 GTC recommendation [ITU04]:

- Asynchronous Transfer Mode (ATM) over GTC framing method,
- GPON Encapsulation method (GEM) over GTC framing method.

The latest release of the G.984.3 recommendation [ITU08] deprecates all the ATM related features. This is because of the fact that ATM is not needed for any service in the FTTx networks. Following the technological trend SXGPON supports only for similar

- SXGPON Encapsulation Method (SXGEM) over SXGTC framing method.

5.2.1 SXGTC layer Service Data Units (SDUs)

The Service Data Units (SDUs) of the SXGTC layer are generated by the OMCI and Ethernet clients shown in Figure 15. The SDUs are defined respectively as:

- Ethernet frame i.e. user frame,
- OMCI frame.

Similarly, both user and OMCI frames are defined to be SDUs of the GTC layer in the G.984.3 recommendation [ITU08].

5.2.2 SXGEM framing principle

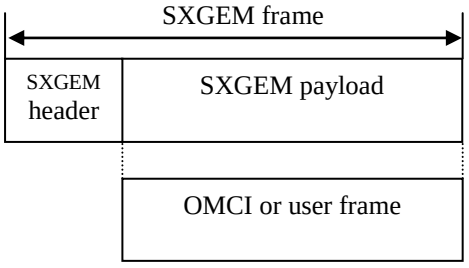

Figure 16. SXGEM framing.

The SXGEM is a variable-length framing mechanism that provides a transparent SDU encapsulation and connection-oriented transportation over the PON. The SXGEM framing is identical in both the DS and the US. The SXGEM frame consists of the SXGEM header

and an SXGEM payload sections. The SXGEM header is of fixed length. The SXGEM payload section length depends on the length of the encapsulated SDU. Figure 16 demonstrates this SXGEM framing approach. Furthermore, the idle SXGEM frame is defined for the case when there is no SDU to be carried over the PON. SXGEM provides a similar to GEM transportation method. The exact SXGEM frame format is however different from GEM described by the G.984.3 recommendation [ITU08]. The SXGEM frame is optimized for 8-byte-based data processing in both the OLT and the ONU. The changes and the reasons for modifications are further discussed in sections 6.3, 6.4 and 6.5**.** [ITU08]

5.2.3 Downstream SXGTC framing principle

The DS SXGTC frame (Figure 17) defines a periodic 125 µs time interval that consists of the variable length SXGTC frame overhead and the SXGTC frame payload sections. The SXGTC frame overhead provides a control channel for the PMD and the SXGTC layers. The SXGTC payload section carries SXGEM frames that encapsulate user and OMCI frames. The length of the SXGTC payload section depends on the length of the SXGTC frame overhead. The SXGTC frames are broadcasted contiguously in the DS and correspondingly received by all ONUs. The DS synchronization between the OLT and all ONUs is hence always maintained in normal operation. The SXGTC framing principle is identical to that of the GTC although the exact frame formats are different. The DS SXGTC frames are optimized for 8-byte-based data processing in both the OLT and the ONU. The differences and the reasons for difference are discussed in sections 6.6, 6.7 and 6.8. [ITU08]

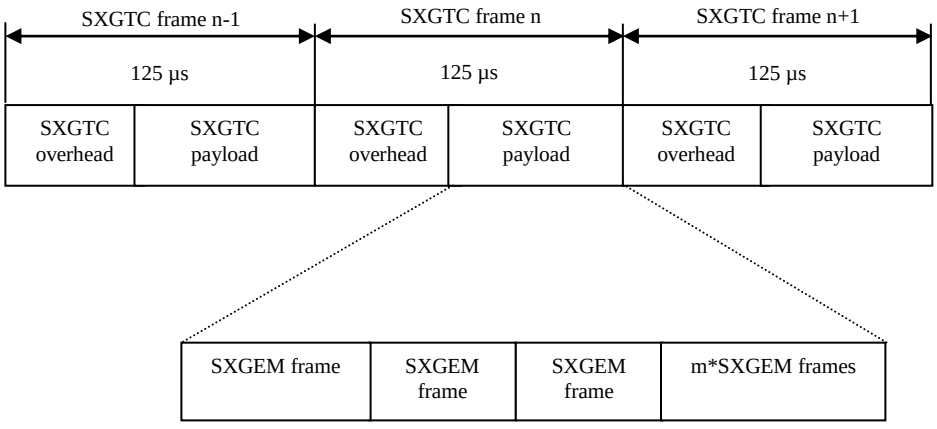

Figure 17. DS SXGTC framing principle.
Adopted and modified from [ITU08, p. 31, Fig. 8-2].

5.2.4 Upstream SXGTC framing principle

The US transmission is different compared to the DS transmission. Since there is only one receiver at the OLT and all ONUs share the same wavelength over a single fiber in the feeder network, the transmitter of each ONU must be shut down whenever the ONU is not transmitting anything in order not to interfere with transmissions from other ONUs. Moreover, because of the transmitter shut down, synchronization with the OLT is lost. This on/off-like transmission by different ONUs is referred to as a burst mode transmission. Each ONU transmission time is correspondingly referred to as a burst. [Lam07, p. 33]

To obtain synchronization at the OLT, each ONU must transmit a preamble in the beginning of each burst prior to transmission of actual data. The preamble provides the OLT receiver with a training sequence, based on which a phase lock can be achieved and synchronization performed. Moreover, guard intervals between the bursts are required in order for the OLT receiver to return to its initial state before the beginning of the next burst. [Lam07, p. 33]

The US SXGTC frame shown in Figure 18 defines a periodic 125 µs time interval that consists of the bursts from all transmitting ONUs and guard intervals in between the bursts. The number of bursts and their lengths are defined by the Transmission Containers (T-CONTs) that are assigned by the OLT to each ONU in the DS SXGTC frame overhead. The T-CONT concept will be discussed in more detail in section 5.3.2. [ITU08]

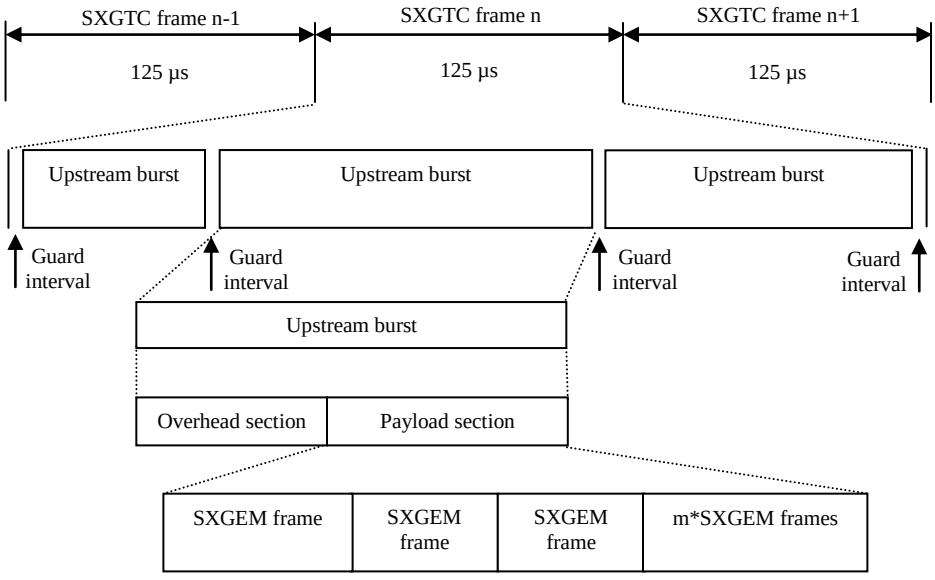

Figure 18. The US SXGTC framing principle.
Adopted and modified from [ITU08, p. 30, Fig. 8-1].

Each burst in SXGPON consists of the US burst overhead and the US burst payload sections. Both the US burst overhead and payload sections are of variable length. Burst overhead embodies both the PMD and the SXGTC layer related information. The US burst payload section is composed of SXGEM frames. The US framing principle of SXGPON is similar to that of GPON [ITU08]. The more detailed structures of the US bursts of SXGPON however differ from those of GPON. The SXGPON US bursts are optimized for 8-byte-based data processing in both the OLT and the ONU. The differences and the reasons for the changes are presented in sections 6.9 and 6.10. [ITU08]

5.2.5 User and OMCI frame fragmentation

In the G.984.3 recommendation [ITU08] the GTC layer supports user and OMCI frame fragmentation over several GEM frames (Figure 19) but there is no such functionality in the first implementation version of the SXGTC layer [Soi08]. In GPON, fragmentation allows for filling the payload sections of both the DS GTC frame and the upstream burst completely with SDUs independently of their lengths.

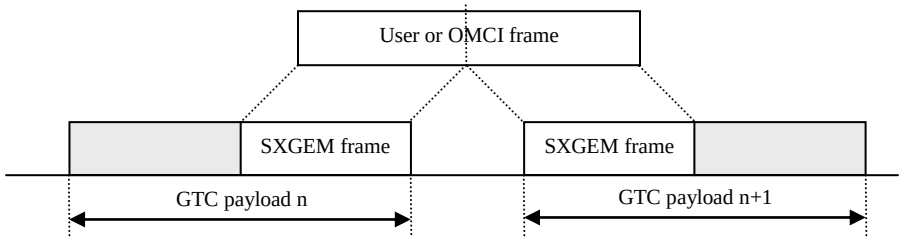

Figure 19. User and OMCI frame fragmentation process in GPON.
Adopted and modified from [ITU08, p. 43, Fig. 8-13b].

Due to the lack of frame fragmentation in SXGPON, each user and OMCI frame is encapsulated by exactly one SXGEM frame as demonstrated in Figure 16. The potential free space at the end of each DS SXGTC frame or upstream burst payload section is filled with idle SXGEM frames. Furthermore, the lack of frame fragmentation makes the SXGTC layer design easier but results in extra overhead that is discussed in sections 7.3.5 and 7.4.

5.3 SXGPON Medium Access Control (MAC) and flow multiplexing

5.3.1 In the downstream

In the DS, the OLT broadcasts the SXGTC and SXGEM frames continuously to all ONUs. Correspondingly, all SXGTC and SXGEM frames are received by all ONUs. Each SXGEM frame is marked by the OLT with a special traffic identifier label referred to as

SXGEM Port-ID according to the destination ONU. The DS SXGEM frames for different ONUs are thus multiplexed in time based on the SXGEM Port-IDs, as shown in Figure 17.

The SXGEM Port-ID labels are used to identify different SXGEM frame flows over the PON and thus represent logical connections between the OLT and the ONUs (Figure 20). Each ONU recognizes the SXGEM frames intended for it by inspecting the SXGEM Port-ID labels. The SXGEM frames with inappropriate SXGEM Port-IDs that are not intended for the particular ONU are discarded. This flow multiplexing scheme is identical to that of GPON [ITU08].

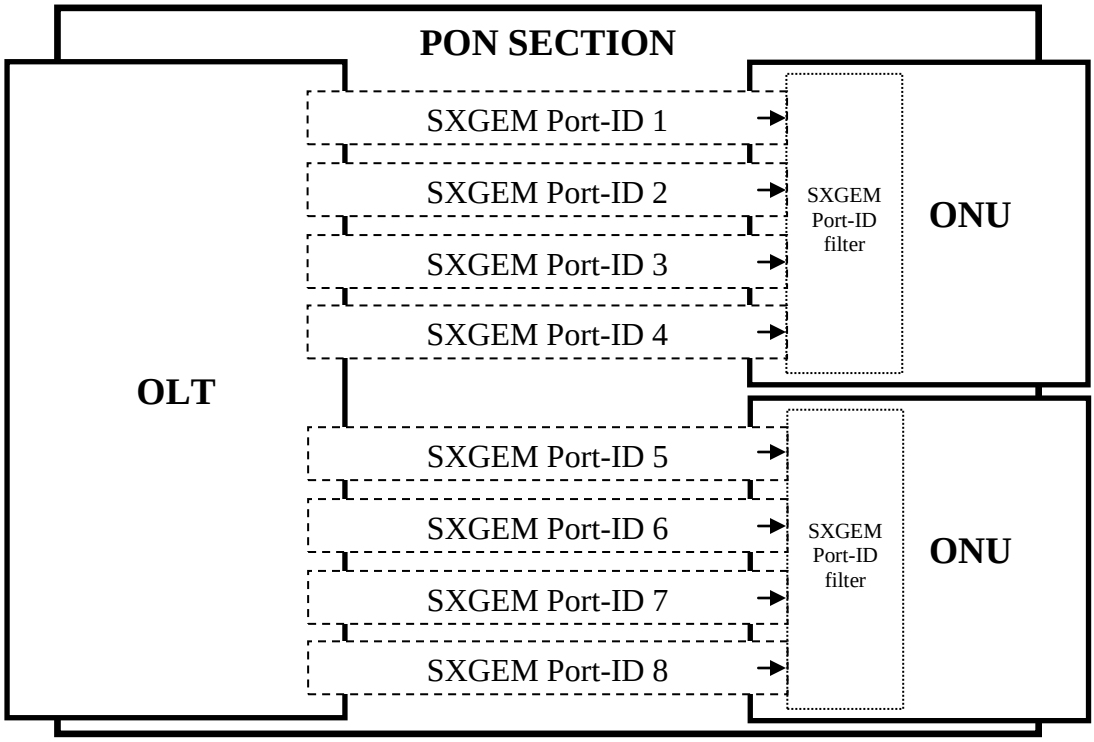

Figure 20. Logical multiplexing in the DS based on SXGEM Port-ID.
Adopted and modified from [ITU08, p. 9, Fig. 5-1].

5.3.2 In the upstream

The US ONU transmissions in SXGPON are multiplexed in time based on Transmission Containers (T-CONTs). The OLT schedules the starting and the ending time of each T-CONT allocation for every ONU. Thus, a T-CONT offers a means for the OLT to grant an ONU a specific US transmission time. This transmission time allocation policy results in the fact that the ONU SXGTC layer is a client of the OLT SXGTC layer.

The US Bandwidth (BW) map field of each DS SXGTC frame contains the US transmission allocation information for each T-CONT for all ONUs and defines completely the next US SXGTC frame structure. Figure 21 illustrates this MAC process. The US burst overhead block added by the ONU in front of the T-CONTs is primarily used for synchronization. Furthermore, this OLT controlled transmission time allocation scheme guarantees that only one ONU at a time will access the medium avoiding the US burst collisions in normal operation. The MAC control principles presented here are identical with those described in the G.984.3 recommendation [ITU08].

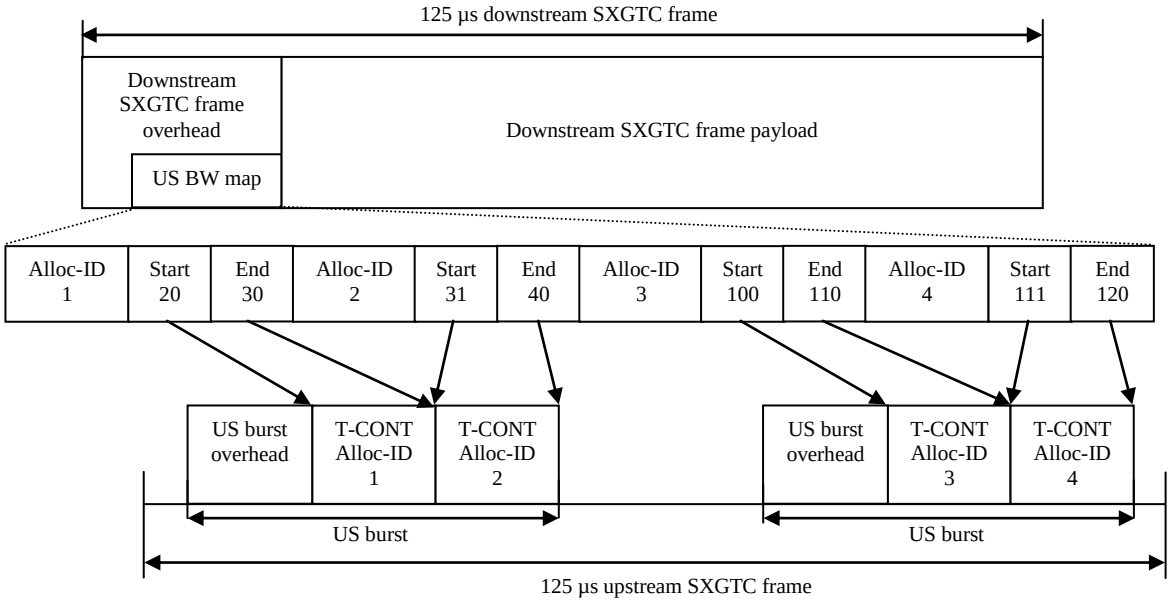

Figure 21. MAC process in SXGPON.
Adopted and modified from [ITU08, p. 19, Fig. 7-4].

Each T-CONT defines a logical communication link between the OLT and an ONU in the US. Each T-CONT is identified by a specific Allocation-ID (Alloc-ID). The total number of the US transmission allocations in an US SXGTC frame thus equals to the number of T-CONTs, as emphasized by Equation (4). T-CONTs carry different SXGEM frame flows identified by the SXGEM Port-ID tags. The same SXGEM Port-IDs are used in both the DS and the US transmissions and hence there is no ambiguity in logical mapping between the US and the DS flows. Figure 22 depicts the concept of the T-CONT and the logical flow multiplexing in the US. This US traffic multiplexing scheme is identical in both GPON [ITU08] and SXGPON.

$$\text{Number of upstream allocations} = \text{Number of T-CONTs} \tag{4}$$

There are five different types of T-CONTs defined in the G.984.3 recommendation [ITU08] and shown in Table 4. Each type is associated with a different US bandwidth allocation strategy. According to Table 4, these strategies vary from Static Bandwidth Allocation (SBA) to DBA discussed in section 2.4.1. Furthermore, in GPON the OLT may assign a variable number of T-CONT to each ONU and the type of a T-CONT can be changed by reconfiguration.

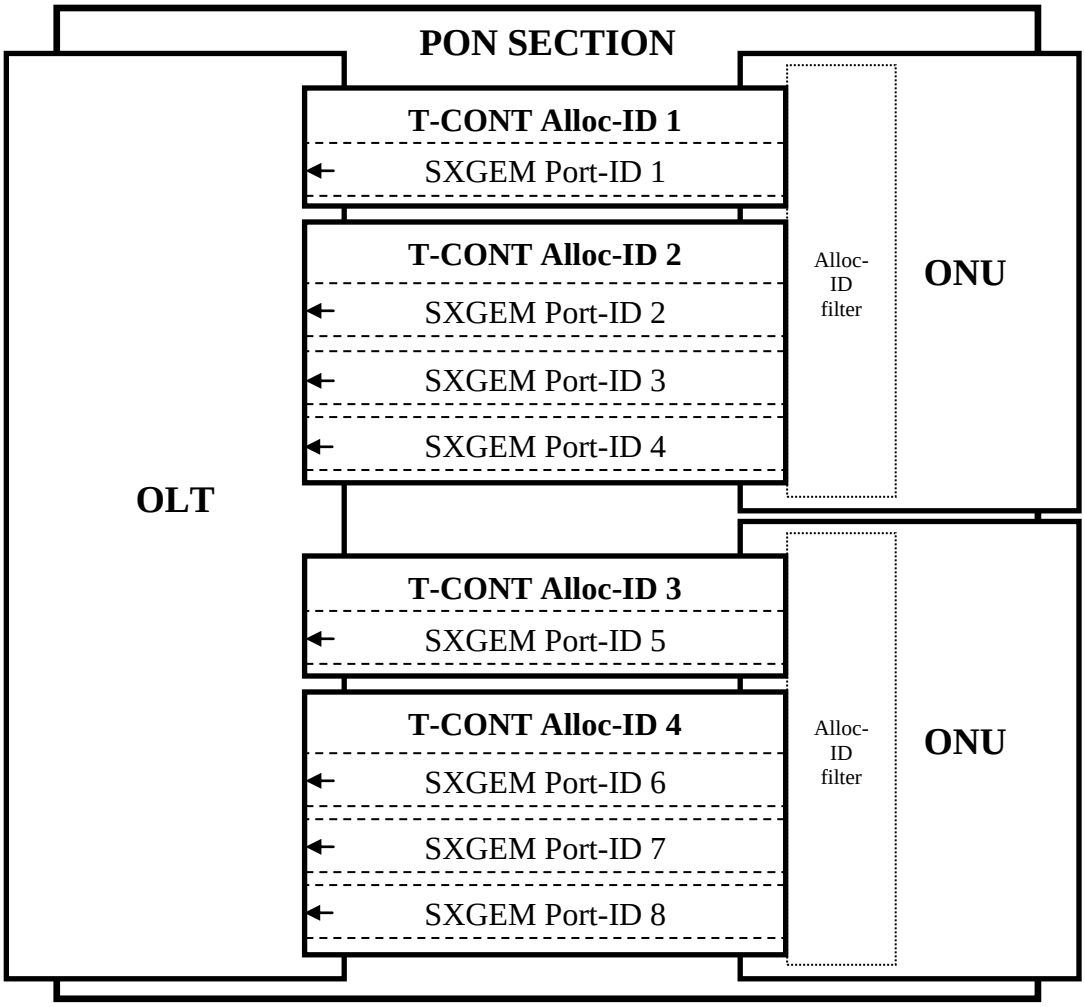

Figure 22. Logical US multiplexing based on T-CONT Alloc-ID and SXGEM Port-ID. Adopted and modified from [ITU08, p. 10, Fig 5-2].

Table 4. GPON T-CONT type summary. Copied from [ITU08, p. 28, Table 7-1].

Traffic descriptor component	**Type 1**	**Type 2**	**Type 3**	**Type 4**	**Type 5**
Fixed BW	R_F				R_F
Assured BW		R_A	R_A		R_A
Maximum BW	$R_M = R_F$	$R_M = R_A$	$R_M > R_A$	R_M	$R_M \geq R_F + R_A$
Additional BW eligibility	None	None	NA	BE	Any

SXGPON will always allocate exactly two contiguous T-CONTs of Type 1 per ONU as shown in Figure 21-23:

- 1 T-CONT per ONU is allocated for the transmission of OMCI SXGEM frames only and is referred to as OMCI T-CONT in this text [Soi08].
- 1 T-CONT per ONU is allocated for the transmission of user SXGEM frames only and is referred to as data T-CONT in this text [Soi08].

Type 1 T-CONT is characterized by a Fixed BW component only. This results in SXGPON having only SBAs. The allocations themselves are configurable and hence T-CONTs may generally be of variable length. The lack of DBA functions and the fixed number of T-CONTs simplifies the SXGTC layer system design and implementation, as there is no need for intelligent DBA management capabilities in the OLT or the ONU.

Furthermore, the G.984.3 recommendation [ITU08] defines that an ONU generates an US burst based on the T-CONT allocation by adding an US burst overhead block in front of the T-CONT. In case of two or more contiguous T-CONTs only one US burst overhead block is added in front of the T-CONTs. The SXGPON OLT allocates always two T-CONTs for each ONU and consequently each ONU generates only one US burst overhead block ahead of the T-CONTs as shown in Figure 21 and Figure 23.

The relation between the T-CONT and the US burst is different in SXGPON (Figure 23) compared to the GPON [ITU08]:

- In SXGPON data T-CONT consists of user SXGEM frames only.
- In SXGPON OMCI T-CONT consists of OMCI SXGEM frames only.

In the G.984.3 recommendation [ITU08] each T-CONT may consist of

- US burst overhead sections,
- US burst payload section containing:
    - GEM and OMCI frames,

    - GEM frames only,
    - OMCI frames only,
- a combination of the overhead and payload sections.

The absence of additional burst overhead sections in the SXGPON T-CONTs is related to the lack of the DBA related signaling capabilities and optimization of the original GPON US burst overhead structure for 8-byte-based data processing. These modifications are discussed in sections 6.9 and 6.10. The detailed SXGPON US burst structure is presented in section 6.10.

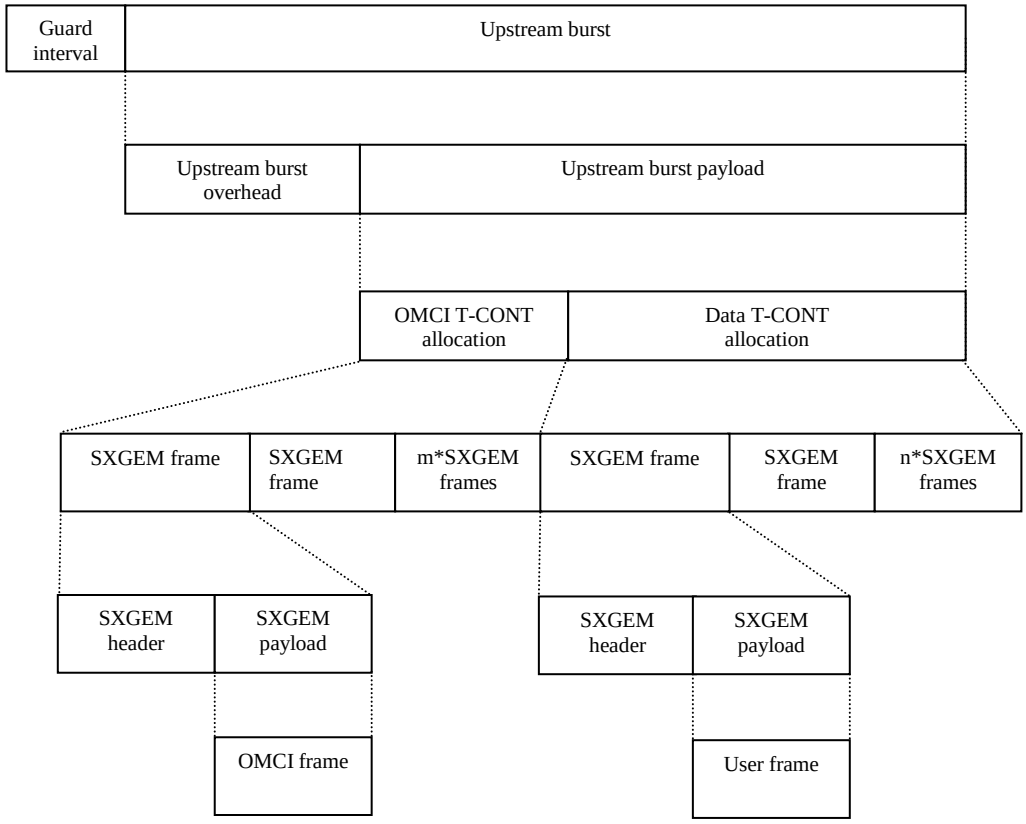

Figure 23. Relation between T-CONT and the US burst in SXGPON.

5.3.3 ONU ranging

The ONUs are at different locations and hence their distances to the OLT are different. This implies that normal operation can be achieved only if all the ONUs are synchronized to a common timing reference, otherwise the US bursts of different ONUs would eventually collide. The establishment of the common timing reference takes place in the ranging

process, where the delay from the OLT to the ONU and back to the OLT is measured. [Lam07, p. 33-35]

First the OLT sends a ranging request to each ONU and waits for that ONU to respond with a ranging response. Based on the response time, the OLT computes equalization delay and communicates it to the ONU. The equalization delay is stored in the ONU and used to align that particular ONU to the common timing reference. After ranging has been completed no collisions occur within GPON or SXGPON systems. [Lam07, p. 33-35]

5.4 User and Control/Management Planes of ONU SXGTC layer system

The functionality of the ONU SXGTC layer system is described in the User Plane (U-Plane) and in the Control/Management Plane (C/M-Plane), in chapters 5.4.1 and 5.4.2 respectively. The U-plane in Figure 24 presents the SXGTC protocol layers, their functional blocks and interactions with clients from user frame processing. The C/M-Plane in Figure 25 presents the SXGTC protocol layers from the ONU management and control functions point of view. The SXGPON U- and C/M-Planes are similar to those of GPON [ITU08].

5.4.1 ONU SXGTC layer system in User Plane

User frame processing in the downstream:

In the DS, the SXGTC payload gets separated from the SXGTC frame in the SXGTC Framing sub-layer and forwarded to the SXGEM TC adapter at the SXGTC Adaptation sub-layer. The SXGEM TC adapter delineates the individual SXGEM frames from the SXGTC payload. All SXGEM frames are filtered by the SXGEM Port-ID filter that allows only the SXGEM frames having appropriate SXGEM Port-IDs to propagate to the Ethernet adapter entity. An appropriate Port-ID indicates that the SXGEM frame is sent by the OLT to this particular ONU and encapsulates a user frame. Ethernet adapter de-encapsulates the SXGEM payload, adapts it to the format required by the Ethernet clients and forwards it to the appropriate Ethernet client.

User frame processing in the upstream:

In the US, the user frames coming from the Ethernet clients, are adapted to the SXGTC layer processing format in the Ethernet adapter. They are further encapsulated by the SXGEM frames and put in the data T-CONT queue in the SXGEM adapter. The Alloc-ID filter picks user SXGEM frames from the data T-CONT queue based on the Alloc-ID received from the OLT and maps them into the data T-CONT allocation. The data T-CONT allocation is in turn multiplexed into the US burst

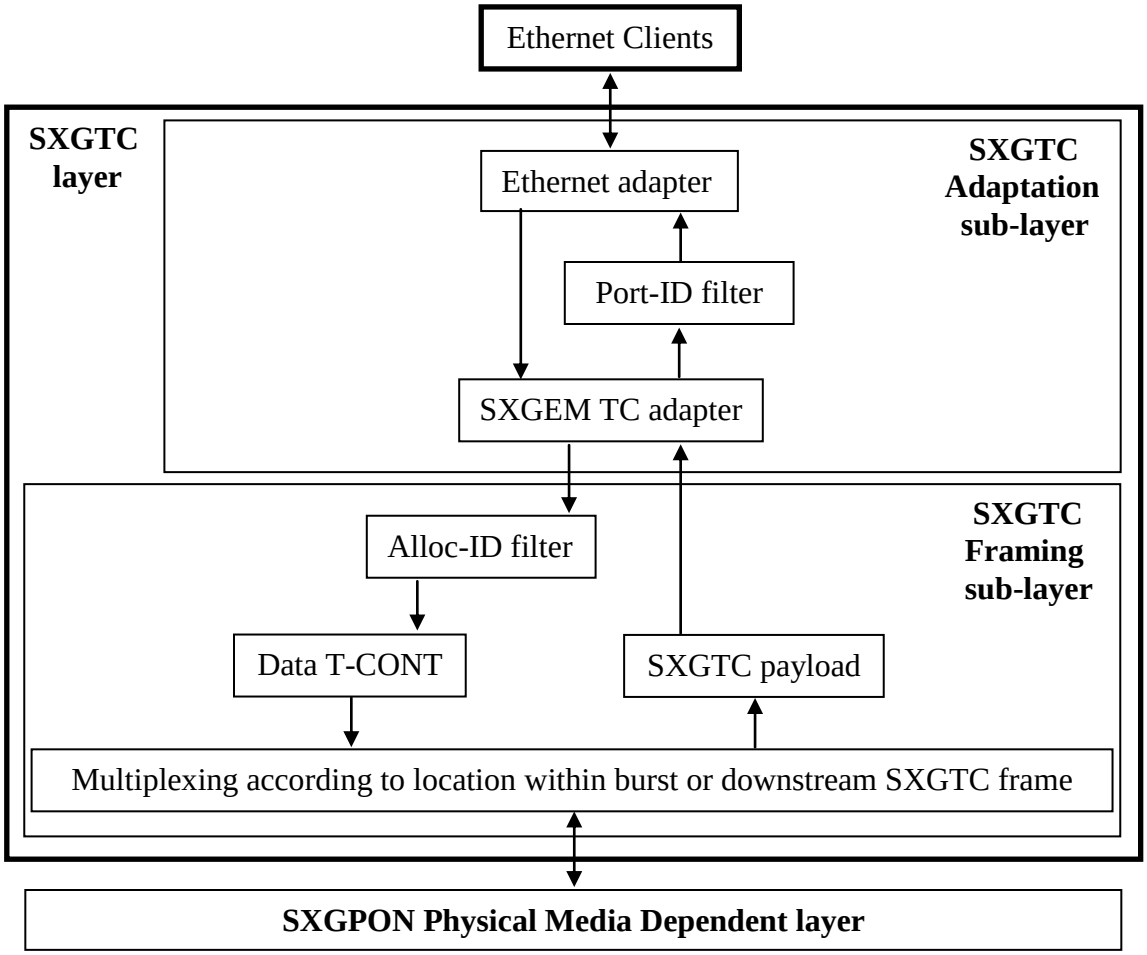

Figure 24. U-Plane view on ONU SXGTC layer.
Adopted and modified from [ITU08, p. 18, Fig. 7-3].

5.4.2 ONU SXGTC layer system in Control/Management Plane

There are three control and management mechanisms defined by the G.984.3 GTC recommendation [ITU08] that are also implemented in SXGPON:

- Embedded Operations, Administration and Maintenance (OAM),
- Physical Layer Operations, Administration and Maintenance (PLOAM),
- Optical Network Unit Management and Control Interface (OMCI).

Embedded OAM processing in the downstream and the upstream:

The purpose of the Embedded OAM is to provide a low latency channel for time critical control information needed by the PMD and the SXGTC layers. Low latency is achieved by

predetermined field mapping in the SXGTC frame overhead. The main function of the Embedded OAM in SXGPON is the US bandwidth granting. The Embedded OAM processing is handled at the SXGTC Framing sub-layer. In GPON [ITU08], Embedded OAM has also other important signaling responsibilities that are related to DBA, transmission encryption and transmission power leveling functions. These are deprecated in SXGPON [Soi08]. The encryption is simply not required in the SARDANA demonstration network. Transmission power level adjustment is irrelevant since the envisioned transmission distances are expected to require maximum transmission power.

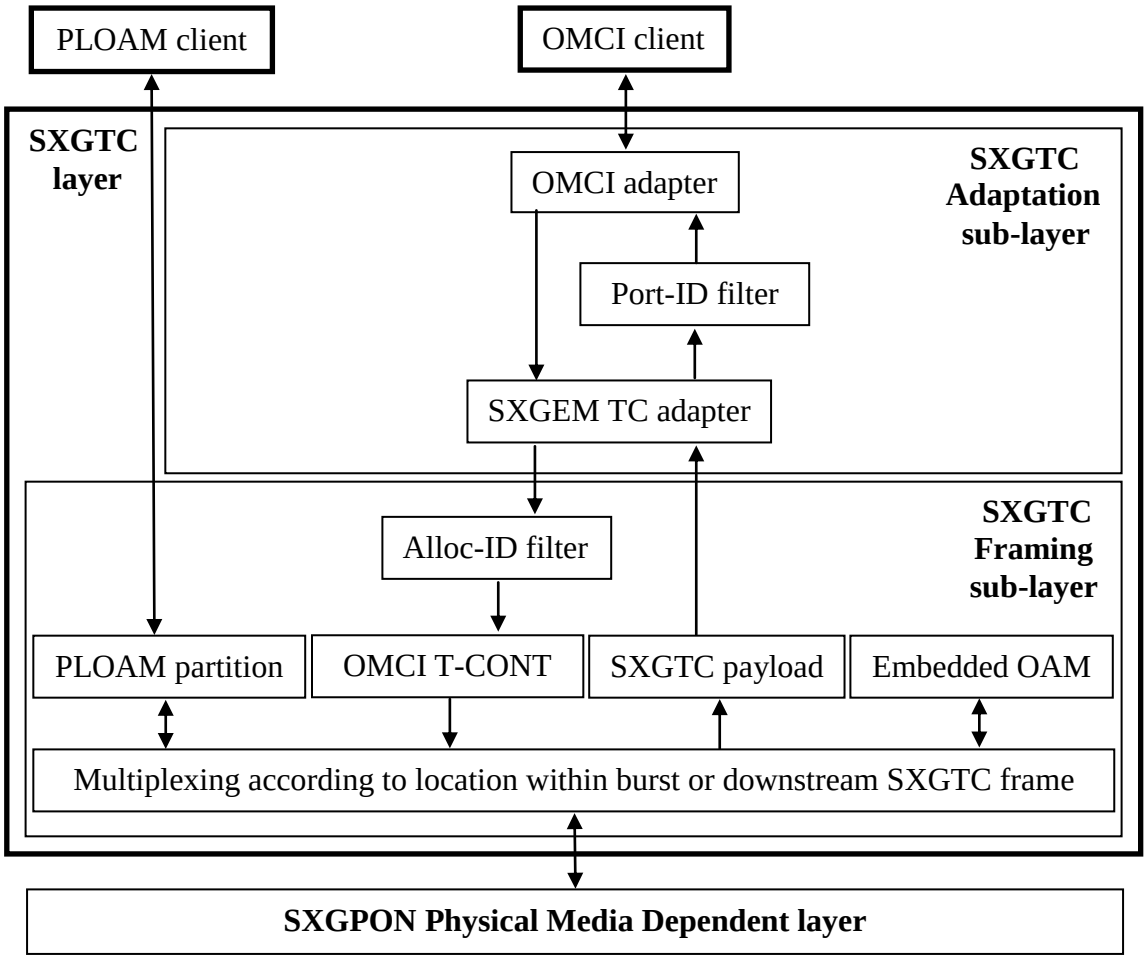

Figure 25. C/M-Plane view on ONU SXGTC layer.
Adopted and modified from [ITU08, p. 17, Fig. 7-2].

PLOAM processing in the downstream and the upstream:

The PLOAM provides a channel for all the other PMD and SXGTC layer information that is not that time critical. This channel communicates different control messages in a

dedicated SXGTC overhead field. The PLOAM messages are processed in the PLOAM block that is a client to the SXGTC Framing sub-layer.

OMCI processing in the downstream:

The SXGTC payload gets separated from the SXGTC frame in the SXGTC Framing sub-layer and forwarded to the SXGEM TC adapter. The SXGEM TC adapter delineates individual SXGEM frames from the SXGTC payload. All SXGEM frames are filtered by the SXGEM Port-ID filter that allows only the SXGEM frames having an appropriate SXGEM Port-ID to propagate to the OMCI adapter. An appropriate SXGEM Port-ID indicates that the SXGEM frame is sent by the OLT to this particular ONU and contains an OMCI message. The OMCI adapter de-encapsulates the SXGEM frames. The OMCI frames are then adapted to the format required by the OMCI client and passed to the OMCI client.

OMCI processing in the upstream:

The OMCI frames coming from the OMCI client are adapted to the SXGTC layer processing format in the OMCI adapter. The OMCI frames are then forwarded to the SXGEM TC adapter that is responsible for SXGEM encapsulation and the OMCI T-CONT queuing. The Alloc-ID filter picks the OMCI SXGEM frames from the OMCI T-CONT queue based on the Alloc-ID received from the OLT and maps them into the OMCI T-CONT allocation that is multiplexed into the US burst. The OMCI frame processing in both the US and the DS is very similar to the user frame processing over the SXGTC layer. This is a natural consequence of fact that both OMCI and user frames are SDUs with respect to SXGEM framing mechanism.

5.5 Summary of SXGPON and GPON logical model differences

Chapter 5 described the logical model of the SXGTC layer that is congruent with the G.984.3 recommendation [ITU08] on a high level of abstraction. This logical model was presented from the ONU perspective. The subjects covered were the SXGTC layer framing and multiplexing mechanisms, MAC, U-Plane and C/M-Plane. On the OLT side the protocol is very similar but contains somewhat different features related to network mastering functions.

The two main logical model differences between GPON and SXGPON that came up in this chapter are user and OMCI frame fragmentation and T-CONT allocation policy. GPON [ITU08] divides OMCI and user frames into fragments to avoid empty space at the end of the DS GTC frame and the US T-CONT allocation. Each fragment is encapsulated with the GEM frame. SXGPON in contrast does not utilize user or OMCI frame fragmentation in the first implementation version [Soi08]. Some portion of the bandwidth efficiency is lost

because of this. On the other hand, SXGTC layer implementation gets easier, which is the primary goal of the SXGTC layer design. The impact on the bandwidth efficiency is investigated in sections 7.3.5 and 7.4.

Furthermore, GPON specification [ITU08] allows for the dynamic T-CONT allocation and management, meaning that a T-CONT can be always created, modified and removed. In SXGPON, exactly two static T-CONTs are allocated for each ONU [Soi08]. The length of the allocations is configurable by the user. One T-CONT is intended for the OMCI messages and the other for the Ethernet user frames i.e. data traffic. This T-CONT allocation scheme considerably reduces the complexity of the SXGTC layer.

The US burst, DS SXGTC and SXGEM frame structures are different from those of GPON [ITU08]. The difference and the drivers behind them are discussed in chapter 6. In addition, some GPON [ITU08] OAM related features are not implemented in SXGPON due to the fact that they are not needed in the demonstration network. The functional differences of the SXGTC layer compared to the standard GTC layer are listed below:

- Only 10 Gbps DS transmission rate is supported in SXGPON [Soi08].
- Only 2.5 Gbps, 5 Gbps and 10 Gbps US transmission rates are supported in SXGPON [Soi08].
- Only Ethernet interface is supported at SXGPON UNI/SNI [Soi08].
- Only static T-CONT allocation scheme with two T-CONTs is used in SXGPON. The T-CONT allocation lengths are configurable but DBA is deprecated. One T-CONT is intended for the OMCI frames and the other for the Ethernet user frames. [Soi08]
- User and OMCI frame fragmentation is not used in the first implementation version of the SXGTC layer [Soi08].
- Forward Error Correction (FEC) is not used in the first implementation version of the SXGTC layer [Soi08].
- Transmission encryption in not used in SXGPON [Soi08].
- Transmission power leveling functions are not used in SXGPON [Soi08].
- Different GEM frame format referred to as SXGEM.
- Different DS GTC frame format referred to as DS SXGTC frame.
- Different US burst format.

6 SARDANA 10 Gigabit-capable Passive Optical Network Transmission Convergence Layer: System Design and Optimization

The general FPGA design goals were listed in the section 4.4. All of these have an effect on the design in case of the SXGTC layer. The most critical aims for the SXGTC layer system design can be summarized as:

- reduction of the design time,
- achievement of the required performance and the correctness of logical function.

The G.984.3 protocol is modified to support for the targeted transmission rates [Soi08]:

- 10 Gbps in the DS,
- 2.5 Gbps, 5 Gbps and 10 Gbps in the US.

The modifications made to the GPON protocol are driven by the two goals presented above. The emphasis is to reduce coding effort and thus simplify the SXGTC layer as much as possible. The modifications are such that they take into account functional requirements, workload issues and FPGA related technological constraints associated with the SXGTC layer design. This chapter presents a balanced solution for the SXGTC layer that preserves relevant GPON related features yet enables relatively straightforward implementation.

The structure of this chapter is such that in section 6.1, the exact transmission rates for the SXGPON system are defined. Section 6.2 describes the FPGA implementation clock frequency and the data path width selection for the design. Sections 6.3-6.5 discuss the applicability of the GEM frame format for the SXGTC layer implementation. Sections 6.6-6.8 deal with the DS GTC frame structure suitability for the DS SXGTC framing. Sections 6.9-6.10 in turn focus on the GPON US burst structure adequacy for the SXGTC layer implementation. Section 6.11 concludes discussion on the SXGTC layer design.

6.1 Definition of transmission rates for SXGPON

As described in sections 5.2.3 and 5.2.4, the US and the DS GTC as well as the US and the DS SXGTC frames are defined as periodic 125 µs structures. Furthermore, the G.984.3 recommendation [ITU08] specifies the GTC frame to be composed of:

- 19440 bytes at 1.24416 Gbps transmission rate,
- 38880 bytes at 2.48832 Gbps transmission rate.

The interdependency of these parameters is represented by

$$\text{transmission rate (bps)} = \frac{\text{bits}}{\text{frame duration (s)}} = \frac{\text{bytes} \times 8}{\text{frame duration (s)}}. \quad (5)$$

Following the G.984.3 recommendation [ITU08], the base transmission rate of 2.48832 Gbps is kept the same and the faster SXGPON transmission rates are obtained by multiplying the base rate of 2.48832 Gbps by a factors of two and four. According to Equation (5) this also increases the SXGTC frame length in bytes respectively. Table 5 summarizes the SXGPON transmission rates and the corresponding SXGTC frame details.

Table 5. SXGPON transmission rate and SXGTC frame details.

Direction	SXGTC frame duration	SXGTC frame length	Transmission rate
US	125 µs	38880 bytes	2.48832 Gbps
US	125 µs	77760 bytes	4.97664 Gbps
US	125 µs	155520 bytes	9.95328 Gbps
DS	125 µs	155520 bytes	9.95328 Gbps

6.2 FPGA implementation clock frequency and data path width estimation

The estimation of the SXGTC layer FPGA implementation maximum clock frequency and the data path width has an important role in the design and implementation of the protocol. This is due to the SXGTC layer specific implementation issues as will be seen in the following sections. The highest data rate of SXGPON is 9.95328 Gbps. The only way an FPGA can process such a high data rate is to parallelize the data to a wide enough data path as parallelization enables dropping the FPGA clock frequency to an achievable value as described in section 4.3.

Furthermore, a real FPGA logic implementation clock frequency is highly dependent on the amount of logical operations needed to be performed during one clock cycle. The SXGPON protocol implementation involves a number of complicated and time consuming functions. It was estimated that a high frequency design will require a significant amount of optimizations and hence a relatively long design time, which is against the SXGTC layer design goals. It was further proposed that the best option for the SXGTC layer implementation with a reasonable logic design is to use the 64-bit wide data paths for a 9.95328 Gbps rate. Using Equation (1), this results in FPGA's clock frequency of

$$\text{clock frequency (Hz)} = \frac{9.95328 \text{ Gbps}}{64 \text{ bits}} = 155.52 \text{ MHz}. \quad (6)$$

The resulting highest data path implementation clock frequency with the 64-bit wide data path is thus 155.52 MHz and hence the implementation must support at least this clock frequency. The clock frequencies with the 64-bit data path widths for lower 4.97664 Gbps and 2.48832 Gbps data rates are obtained using (1) again. The resulting clock domains are summarized in Table 6.

Table 6. SXGTC layer clock domains.

Data rate	Data path width	Clock domain
2.48832 Gbps	64 bits	38.88 MHz
4.97664 Gbps	64 bits	77.76 MHz
9.95328 Gbps	64 bits	155.52 MHz

6.3 GEM frame structure

The G.984.3 recommendation [ITU08] GEM frame format is presented in the Figure 26.

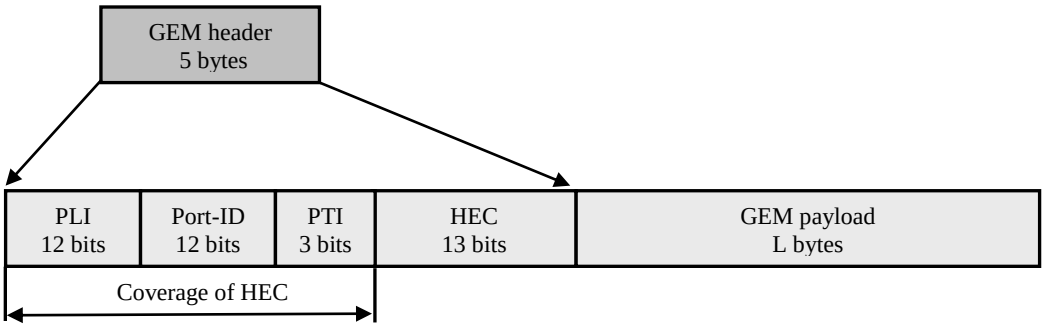

Figure 26. GEM frame format.
Adopted and modified from [ITU08, p. 41, Fig. 8-11].

- **Payload Length Indicator (PLI)** defines the length of the GEM frame payload partition in bytes. Being a 12-bit number it limits the GEM payload to 2^{12}-1 = 4095 bytes.

- **GEM Port Identifier (GEM Port-ID)** is a 12-bit indicator that is used to provide unique traffic identifiers and traffic multiplexing on the PON.

- **Payload Type Indicator (PTI)** is used to provide additional information of the payload content type.

- **Header Error Correction (HEC)** provides error detection and correction functions for the header. It is a combination of Bose-Chaudhuri-Hocquenghem (BCH) (39, 12, 2) code and a single parity bit.

- **GEM payload** is of variable length, measured in bytes and restricted from above by the PLI field.

Furthermore, an idle GEM frame is defined to have an all-zero PLI. As a consequence of this, the GEM payload is zero bytes long and the idle GEM frame is only 5 bytes long.

6.4 Applicability of GEM frame structure in SXGPON

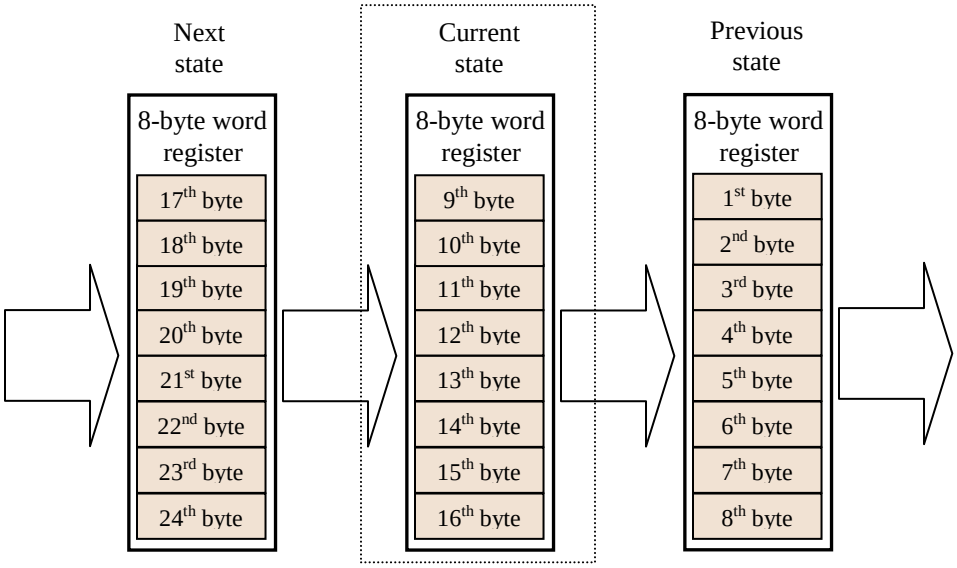

Figure 27. An arbitrary registered 8-byte-word on the 8-byte data path.

For simpler illustration the 64-bit data path is referred to as a 8-byte data path in the rest of the text. Furthermore, each 8 bytes on the data path represent one entity that is referred to as an 8-byte-word. Figure 27 illustrates these concepts presenting an arbitrary data sequence seen on the 8-byte wide data path moving through the 8-byte register in time to the right.

When delineating the GEM frames from the GTC payload partition in the ONU DS the beginning of the next GEM frame is not known until the header of the previous GEM frame is processed with HEC and PLI pointer extracted. The GEM header and hence the GEM idle frames are only 5 bytes long and are smaller compared to the 8-byte data path width.

A GEM frame is of variable length and may in general begin on any of the 8 bytes on the 8-byte data path. It is hence possible to have pieces of up to three GEM frames in one 8-byte-word on one clock cycle. The case with three GEM frames is the most complex case for the GEM frame delineation process. This case may take place for instance when there is an 8-byte-word consisting of one last byte of the previous GEM frame 1, a current idle 5-byte GEM frame 2, and two first bytes of the next GEM frame 3 header (Figure 28).

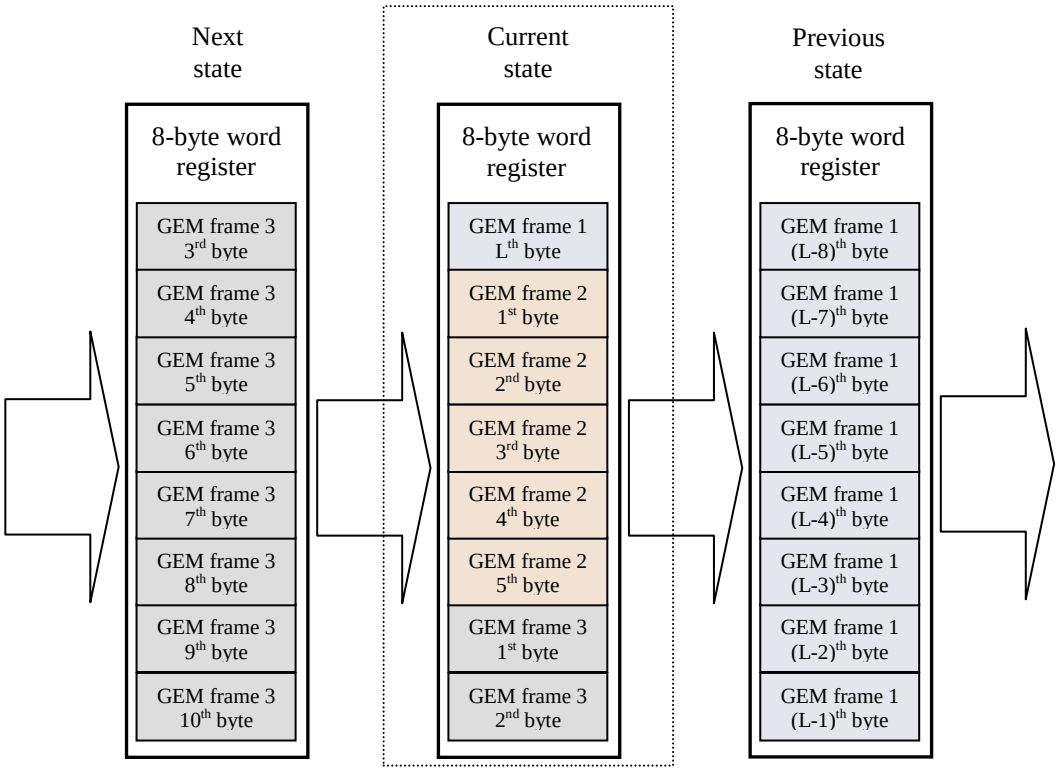

Figure 28. Example of having 3 different GEM frames on the 8-byte data path during one clock cycle.

All 8 bytes of the 8-byte-word need to be processed simultaneously and every word contiguously because GEM frames are sent as a continuous flow in the DS. The following actions must be performed in one clock cycle:

- delineate the last byte of GEM frame 1,
- start decoding GEM frame 2 header,
- dtart decoding the next potential GEM frame 3, as the length of the GEM frame 2 being decoded currently is unknown.

Every potential occurrence scenario of the GEM frames on the 8-byte data path must be taken into account in order to implement the GEM frame delineation in the DS. The

requirement to process two GEM frames with unknown lengths on the same clock cycle notably complicates the processing of the GEM frames in the DS. In the US, the process of packaging the GEM frames in the GTC payload partition is similar but reverse. This results in the complicated US implementation. Furthermore, exactly the same difficulties are encountered in the OLT.

An alternative solution to the GEM frame delineation involves changing the data path width and the clock frequency but keeping the data rate fixed as described in section 4.3. To minimize the coding effort associated with the GEM frame delineation and processing, the GEM frames should be processed byte-by-byte i.e. on the 1-byte data path (Figure 29). Only then each GEM frame can be processed independently of its alignment on the data path. This approach however requires decreasing the data path width by a factor of 8, hence increasing the frequency by a factor of 8. Using Equation (1), this results in the FPGA clock frequency of

$$\text{clock frequency (Hz)} = \frac{9.95328 \text{ Gbps}}{8 \text{ bits}} = 1244.16 \text{ MHz}. \quad (7)$$

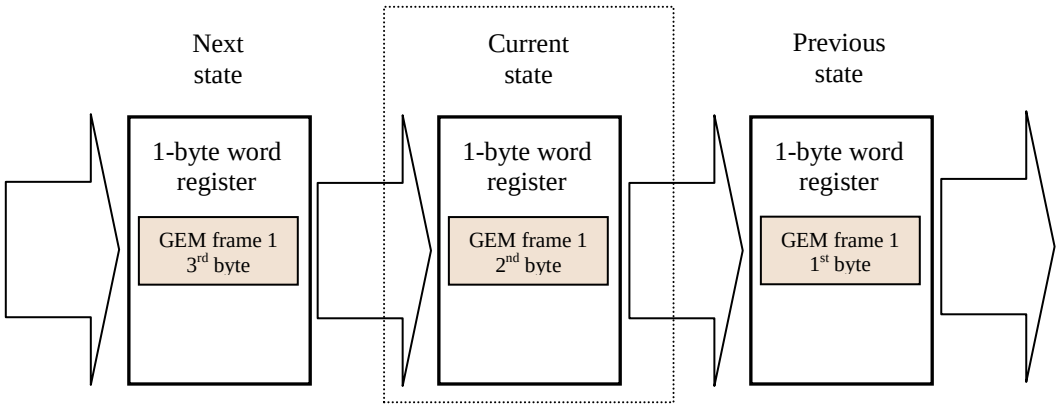

Figure 29. Example of processing data on 1-byte wide data path.

This frequency is in fact much higher even than the theoretical FPGA clock frequency and hence unachievable. Using Equation (1) for 32-bit data path width results in FPGA clock frequency of

$$\text{clock frequency (Hz)} = \frac{9.95328 \text{ Gbps}}{32 \text{ bits}} = 311.04 \text{ MHz}. \quad (8)$$

This frequency would decrease the complexity of the delineation function, as there could be only one beginning GEM frame on the data path during one clock cycle (Figure 30). However, the alignment would still be variable. Moreover, designing the SXGTC layer for higher frequencies than 155.52 MHz would probably require more design time due to

tighter timing requirements. It is also possible that GEM delineation function is not implementable at 311.04 MHz as the frequency might be too high for the complex logic.

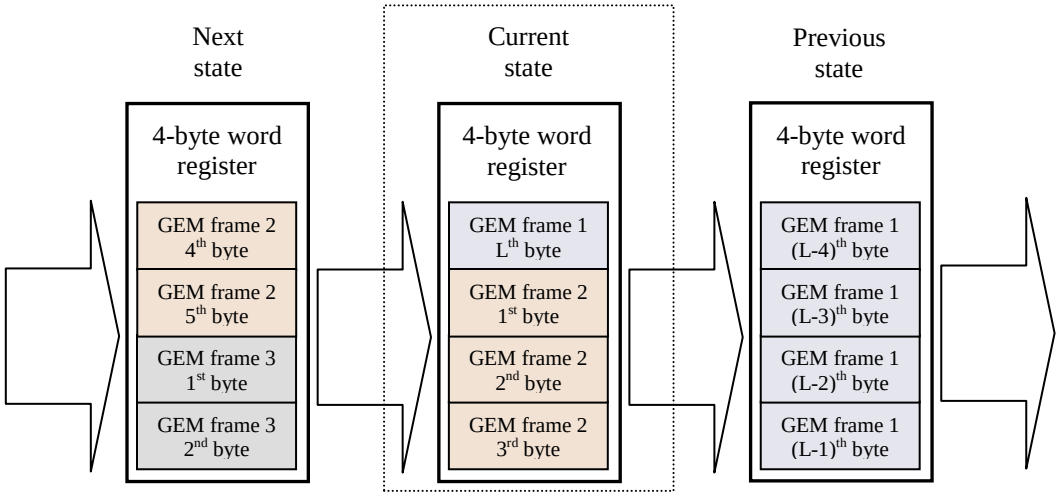

Figure 30. Example of GEM frame processing on 4-byte wide data path.

6.5 SXGEM frame structure

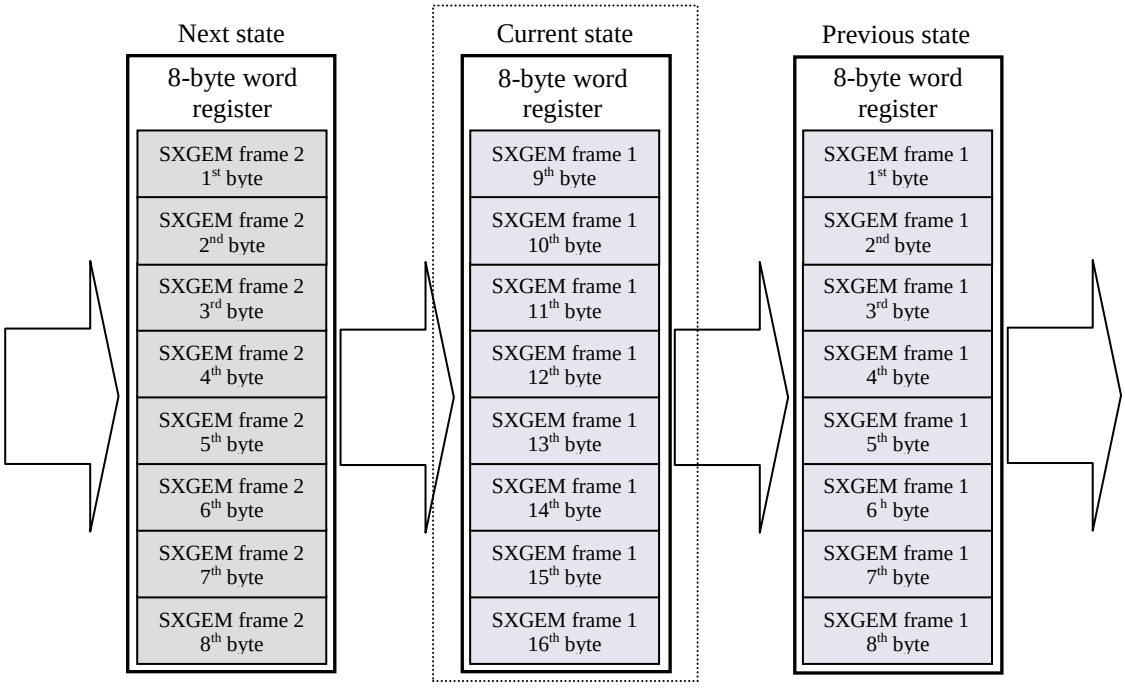

Figure 31. Alignment of SXGEM on 8-byte wide data path.

Another way to simplify the 8-byte wide data path design and reduce the workload associated with coding is to extend the GEM header to occupy 8 bytes and the GEM frame length to be a multiple of 8 bytes. This new format is referred to as SXGEM. This way each SXGEM header and SXGEM frame is always equally aligned with respect to the 8-byte data path (Figure 31). The processing of each SXGEM frame header can be performed equally, minimizing the amount of the required logic. Possible unused payload bytes at the end of each SXGEM frame can be simply padded with zeroes to keep the alignment.

Furthermore, the 8-byte SXGEM header permits the usage of 32-bit Cyclic Redundancy Check (CRC-32) instead of 13-bit GEM HEC code. The positive aspects of using CRC-32 are:

- GEM HEC code needs not be implemented,
- CRC-32 implementation already exists.

The re-use of the existing CRC-32 block in the design hence notably reduces coding effort. CRC-32 lacks error-correcting capabilities and hence the SXGEM frame error-tolerance is expected to be lower than that of the standard GEM frame. The resulting SXGEM frame format is presented in detail in Figure 32. The modified SXGEM frame encapsulation and validation mechanism has an impact on the SXGPON protocol overhead and throughput. These are studied in chapter 7.

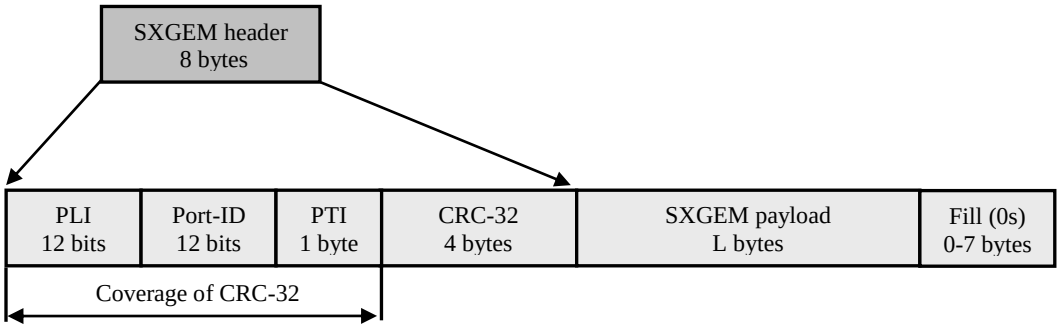

Figure 32. SXGEM frame format.

- **Payload Length Indicator (PLI)** defines the length of the SXGEM frame payload partition in bytes. Being a 12-bit number it limits the SXGEM payload to 2^{12}-1 = 4095 bytes.

- **SXGEM Port Identifier (SXGEM Port-ID)** is a 12-bit indicator that is used to provide unique traffic identifiers and traffic multiplexing on the PON.

- **Payload Type Indicator (PTI)** is used to provide additional information of the payload content type. The extension of the PTI field to 1 byte is related only to the

extension of the header. The additional 5 Most Significant Bits (MSBs) are simply zero-padded.

- **CRC-32** provides error detection functions for SXGEM frame header.

- **SXGEM payload** is of variable length, measured in bytes and restricted from above by the PLI field.

- **Fill (0s)** is a zero-padded field for making the SXGEM frame length divisible by 8 bytes**.** The length of this field is 0-7 bytes depending on the SDU length.

6.6 Downstream GTC frame structure

The G.984.3 [ITU08] DS GTC frame structure is presented in Figure 33. Section 5.2.3 describes the DS GTC frame to consist of the GTC frame overhead and payload partitions. The overhead partition is of variable length and is referred to as Physical Control Block downstream (PCBd).

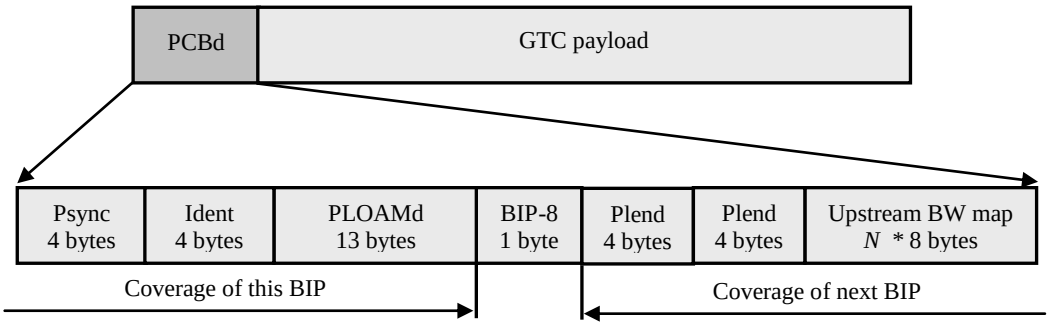

Figure 33. GPON DS GTC frame structure.
Adopted from [ITU08, p. 31, Fig. 8-3].

- **Physical synchronization (Psync)** is a 4-byte fixed pattern field that is used for DS synchronization.

- **Ident** field is used to indicate usage of FEC in the DS and larger framing structures required by encryption system. Furthermore Ident field can be used for additional synchronization check. Ident is 4 bytes long.

- **PLOAM downstream (PLOAMd)** field (Figure 34) is used for transmission of PLOAM messages. One PLOAM message occupies the entire PLOAMd field. This results in the fact that only one PLOAM message can be sent in one DS GTC frame. PLOAMd is a 13 bytes long field that consists of

- **ONU identifier (ONU-ID)** that occupies 1 byte.
- **Message identifier (Message-ID)** that occupies 1 byte.
- **Message data** that occupies 10 bytes.
- **8-bit Cyclic Redundancy Check (CRC-8)** field that is used to verify the correctness of the PLOAMd message.

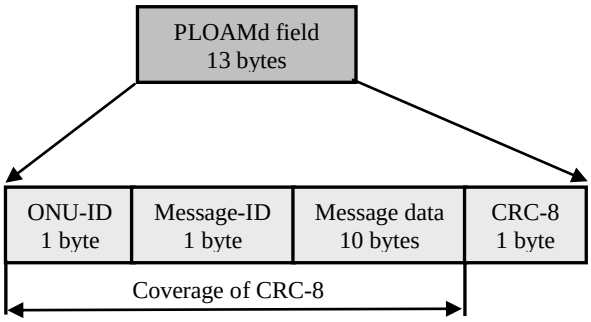

Figure 34. GPON PLOAMd and PLOAMu field.
Adopted and modified [ITU08, p. 49, Fig. 9-1].

- **8-bit Bit Interleaved Parity (BIP-8)** field contains the 8-bit interleaved parity of all bytes transmitted since the last BIP-8.

- **Payload length downstream (Plend)** shown in Figure 35 is a 4-byte field that is composed of three fields:

  - **Bandwidth map length (Blen)** that defines the length of the US BW map partition in terms of bandwidth map allocation structure count. Blen is 12-bits long.
  - **12-bit zero-padded field** that is part of Plend due to historical reasons. This field was used previously in G.984.3 [ITU04] to indicate the length of the ATM partition. The latest release of the G.984.3 recommendation [ITU08] deprecates the usage of ATM and pads this ATM field with zeros.
  - **CRC-8** error-detecting code field that is used to verify the correctness of Plend field.

  As shown in Figure 33, there are two Plend fields in the PCBd. These fields carry exactly the same information. The repetition of Plend provides with better error tolerance and error-correction possibilities when processed interdependently. This dual Plend field transmission and processing scheme offers robustness against up to 3 bit errors. If Blen field cannot be parsed successfully, the complete DS GTC frame is rejected. Due to this fact, the US allocation information is lost and no US bursts are sent during the next US GTC frame.

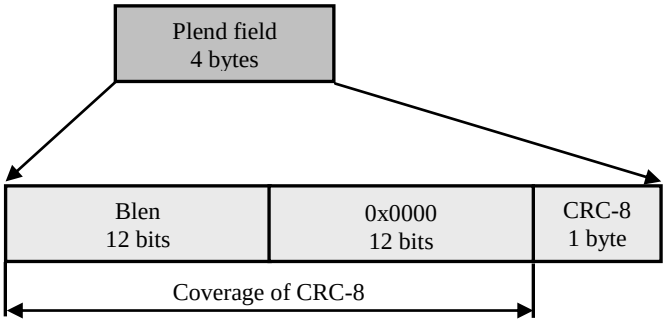

Figure 35. GPON Plend field.
Adopted and modified from [ITU08, p. 34, Fig. 8-6].

- **Upstream (US) Bandwidth (BW) map** specifies the US transmission times for all T-CONTs of all ONUs in the PON and hence completely defines the next US GTC frame. 8 bytes are required to define the transmission time for each T-CONT. The length of the US BW map is thus always a multiple of 8 bytes and depends on the number of T-CONTs that are granted transmission time. Each allocation structure in the Figure 36 provides an ONU with all required information regarding a certain T-CONT transmission.

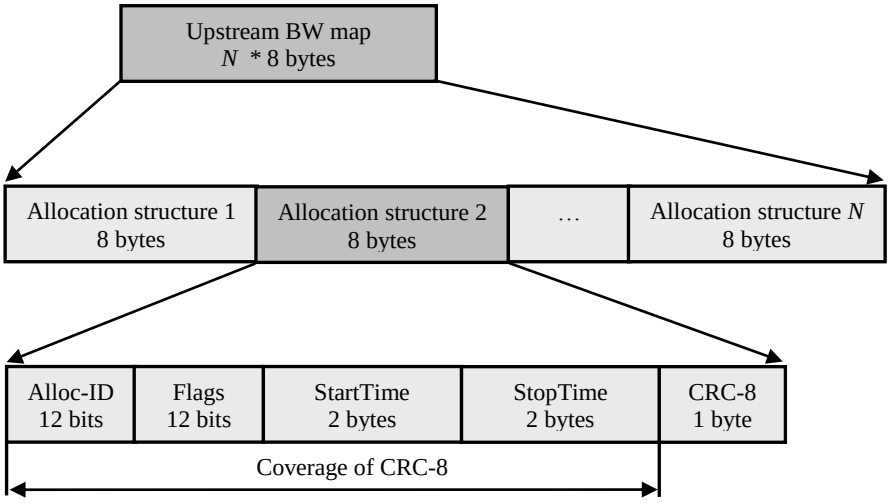

Figure 36. GPON US bandwidth map structure.
Adopted and modified from [ITU08, p. 34, Fig. 8-7].

  - Each T-CONT is identified by a 12-bit **Allocation Identifer (Alloc-ID)** field described in section 5.3.2.
  - **Flags** field provides T-CONT related indicators. Flags field is 12 bits long.
  - **StartTime** is a 2-byte field that defines the beginning of the T-CONT transmission time in bytes.

- **StopTime** is a 2-byte field that defines the end of the T-CONT transmission time in bytes.
- **CRC-8** field protects each allocation structure.

Downstream GTC payload partion

The GTC payload partition carries GEM frames. The length of the GTC payload partition depends on the PCBd length and equals to whatever is left after the PCBd

$$\text{GTC payload length} = \text{GTC frame length} - \text{PCBd length}\ . \quad (9)$$

6.7 Applicability of downstream GTC frame structure in SXGPON

The DS SXGTC frame is 155520 bytes long and hence divisible by 8 bytes. There is no conflict from the perspective of processing the entire frame on the 8-byte data path with the same alignment, as the length of the frame is divisible by 8 bytes. If the original GTC PCBd block structure is used in the DS SXGTC frame, there are no particular difficulties in PCBd processing as:

- The beginning of every PCBd aligns evenly with the respect to the 8-byte data path because SXGTC frame length is divisible by 8 bytes.
- The beginning of the variable part of PCBd i.e. the US BW map partition is always known.
- The US BW map partition length is divisible by 8 bytes.

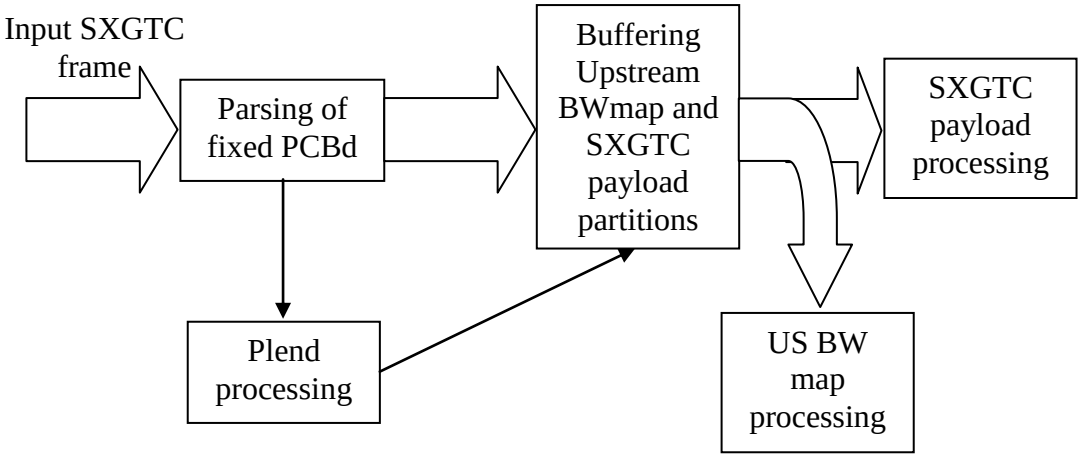

Figure 37. DS SXGTC frame parsing with the original G.984.3 PCBd format.

The actual problem with the GTC frame processing is that the length of PCBd affects the length of the SXGTC payload partition. The SXGTC payload partition is never divisible by

8 bytes because the fixed part of GTC PCBd is 30 bytes long (Figure 33). The proposed SXGEM format does not fully fit into the SXGTC frame if the PCBd format is not altered to ensure the SXGTC payload divisibility by 8 bytes.

The length of the US BW map is not known until both Plend fields are evaluated and checked with CRC-8. This requires Plend comparison logic with possible error-correcting measures and buffering of the US BW map and SXGTC payload partitions. A high-level view on the overall SXGTC frame parsing with the original GPON PCBd structure [ITU08] is shown in Figure 37. It is evident that the frame processing is not particularly straightforward due to dual Plend processing requirement and could be simplified in SXGPON.

6.8 Downstream SXGTC frame structure

The SXGTC frame structure is based on the SXGEM format and a modification of the GPON PCBd format to better suit the 8-byte-word-based processing. Increasing the length of the fixed PCBd part to be divisible by 8 bytes at the expense of the SXGTC payload partition:

- allows usage of SXGEM frame format,
- simplifies the DS SXGTC frame parsing.

As a consequence, the fixed part of PCBd, the US BW map partition and the SXGTC payload partition can be always processed with the same alignment on the 8-byte data path. Further simplifications and modifications of PCBd were studied and carried out to achieve better suitability with 8-byte data path in SXGPON:

- 4-byte **Psync** and 4-byte **Ident** fields are not modified as they are used to provide synchronization.

- BIP-8 is changed to **64-bit Bit Interleaved Parity (BIP-64),** as it results in a more straightforward implementation for the 8-byte data path.

- **Plend** is modified to be 2 bytes long (Figure 38). Since ATM is not used, the 12-bit zero fill field is completely removed. CRC-8 protection is also discarded. Furthermore, the mutual processing of the Plend fields is simplified to reduce coding effort by abolishing one of the Plend fields from the PCBd. This results in losing the 3-bit error-correcting capability provided by two copies of CRC protected Plend fields. The protection scheme used for Plend is discussed below.

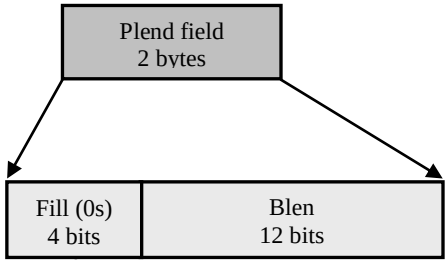

Figure 38. SXGPON Plend field.

- **PLOAMd-Plend.** Both GPON Plend and PLOAMd fields are protected by CRC-8s. The first step in the processing of Plend and PLOAMd is similar in the sense that before processing of actual data the CRC-8s need to be calculated in order to find out whether the data is valid. If the CRCs are incorrect both fields are completely discarded. It is realized that coding effort can be further reduced by combining PLOAMd and Plend into one PLOAMd-Plend field protected by one CRC-32 field. The PLOAMd message is kept as defined in the G.984.3 recommendation [ITU08].

  Based on the experience gained from analyzing the original DS GTC frame PCBd structure the length of PLOAMd-Plend field is extended to 24 bytes to make it divisible by 8 bytes by inserting 6 fill bytes into it. The SXGPON PLOAMd-Plend field structure is demonstrated in Figure 39. If Blen field cannot be parsed successfully, the complete DS SXGTC frame is rejected. Due to this fact, the US allocation information is lost and no US bursts are sent during the next US SXGTC frame. The modified DS SXGTC frame validation mechanism affects the system throughput. The throughput of the SXGPON system with implemented frame modifications is examined in section 7.5.

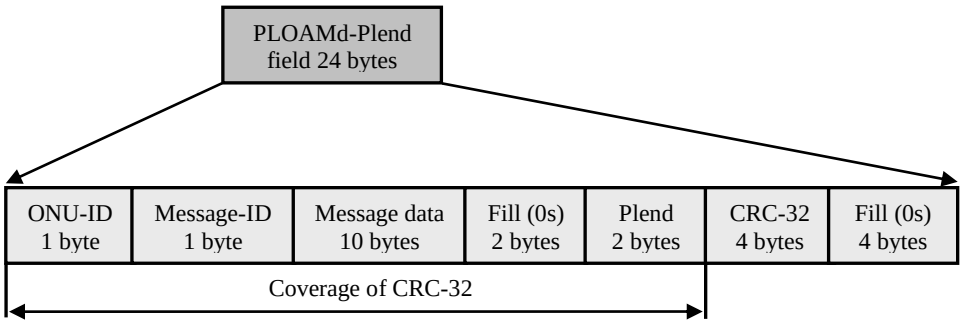

Figure 39. SXGPON PLOAMd-Plend field structure.

- **Fixed part of the PCBd** consists of Psync, Ident, PLOAMd-Plend and BIP-64 and is redefined to be 40 bytes long (Figure 40). The DS SXGTC frame PCBd is divisible by 8 bytes.

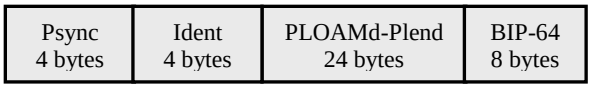

Figure 40. SXGPON fixed part of the PCBd.

- **US BW map** partition format is modified. In the G.984.3 [ITU08] both the StartTime and the StopTime pointers are 16-bit numbers limiting the US GTC frame to 2^{16}-1 = 65535 bytes. Using (5), this is sufficient to address the US transmission rates only for up to

$$\text{transmission rate} = \frac{65535 \text{ bytes} \times 8}{125\mu\text{s}} = 4.1942 \text{ Gbps}. \quad (10)$$

The 9.95328 Gbps US transmission rate can be achieved using the 16-bit StartTime and StopTime fields if these are used to indicate 4-byte- or 8-byte-words. Since the data path in the US also needs to be 8-byte wide at 9.95328 Gbps, the StartTime and StopTime pointers in SXGPON indicate 8-byte-words instead of bytes. This change allows the logical US transmission rate to be for up to

$$\text{transmission rate} = \frac{65535 \text{ 8-byte words} \times 64}{125\ \mu\text{s}} = 33.55392 \text{ Gbps}. \quad (11)$$

The lower transmission rates can be also processed in the 8-byte-word mode on the 8-byte wide data path using lower clock frequencies. Furthermore, each allocation structure is protected by CRC-8 in the G.984.3 recommendation [ITU08]. Re-using the 4-byte CRC-32 at the expense of CRC-8 requires extending each allocation structure by 3 bytes. To further decrease the coding effort, the allocation structure is modified in the following way:

  - The length of each allocation structure is extended from 8 bytes to 16 bytes i.e two 8-byte-words.
  - Allocation information occupies the first 8-byte-word.
  - Original CRC-8 field in the first 8-byte word is zero-padded.
  - CRC-32 field occupies first 4 bytes of the second 8-byte-word.
  - The latter 4 bytes of the second 8-byte-word are zero-padded.

This new SXGPON US BW map scheme provides re-use of CRC-32 block and easy implementation for 8-byte processing and CRC-32 verification. The scheme is shown in the Figure 41.

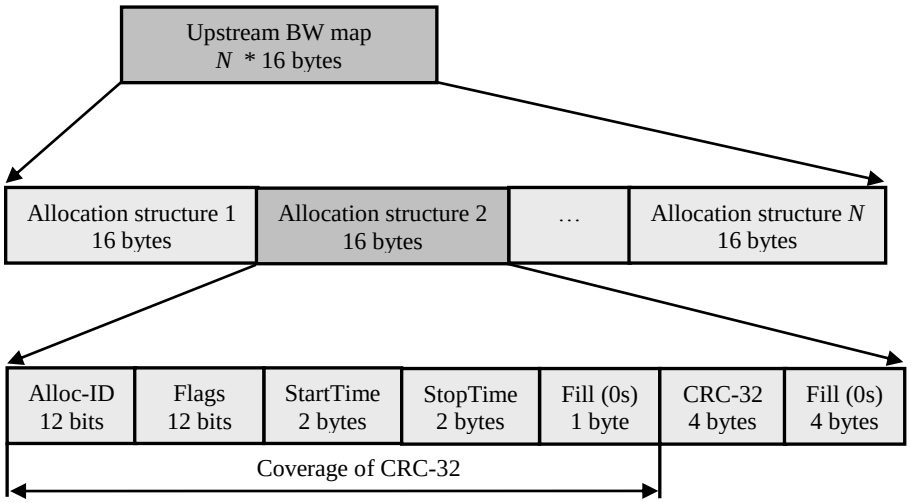

Figure 41. SXGPON US bandwidth map format.

- **Downstream SXGTC frame** in SXGPON is modified to have both the fixed and the variable part of PCBd to be divisible by 8 bytes (Figure 42). As a direct consequence of this the SXGTC payload partition is also divisible by 8 bytes. The length of the SXGTC payload partition is obtained using

$$\text{SXGTC payload length} = \text{SXGTC frame length} - \text{PCBd length}\ . \tag{12}$$

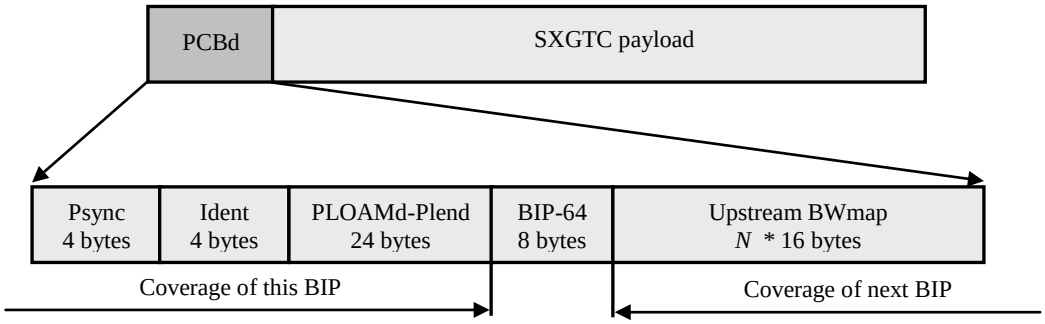

Figure 42. DS SXGTC frame.

The modified DS SXGTC frame structure has an impact on the SXGPON protocol overhead and throughput. These are studied in chapter 7.

6.9 GPON upstream burst structure

The detailed figure of the G.984.3 [ITU08] GPON US burst structure with possible mandatory and optional overheads for 2 T-CONTs is presented in Figure 43. The optional fields are sent only if they are requested by the OLT.

GPON upstream burst

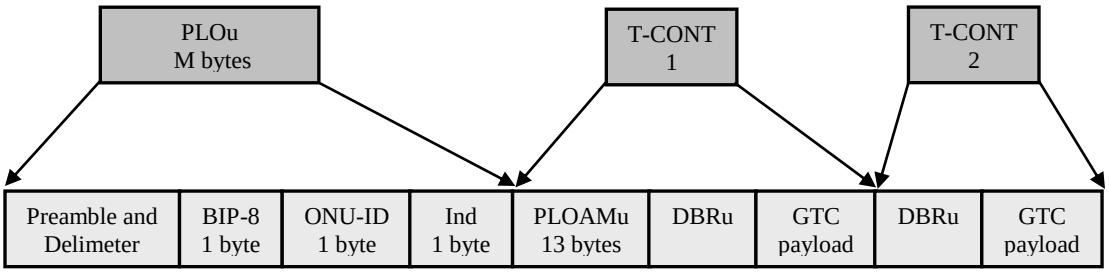

Figure 43. GPON US burst structure with 2 T-CONTs.
Adopted and modified from [ITU08, p. 38, Fig. 8-8].

- **Physical Layer Overhead upstream (PLOu)** is a mandatory block for each US burst. It consists of:
  - variable length **Preamble** field,
  - variable length **Delimiter** field,
  - 1-byte **BIP-8** field,
  - 1-byte **ONU-ID** field,
  - 1-byte **Indication (Ind)** field used for signaling.

- **PLOAM upstream (PLOAMu)** is an optional block with respect to each GPON US burst. The PLOAMu field is used to communicate PLOAM messages in the US direction. The block is identical to the PLOAMd block and contains only one PLOAM message. The PLOAMu length is 13 bytes consisting of 12-byte PLOAM message and 1-byte CRC-8 field (Figure 34). The PLOAMu is sent in the beginning of a T-CONT. In case of a multiple T-CONTs, the PLOAMu is sent in one T-CONT allocation only. The command to send the PLOAMu in specific allocation is communicated to the ONU by the OLT.

- **Dynamic Bandwidth Report Upstream (DBRu)** is an optional block with respect to each T-CONT. It provides the OLT with the information about T-CONT traffic waiting at the ONU. The possible lengths of DBRu are 1, 2 and 4 bytes depending on the DBA report mode.

- **Payload** partition length is defined by Equation (13) as a function of the T-CONT StartTime and StopTime pointers and requested overheads.

$$\text{Payload length} = \text{StopTime} - \text{StartTime} + 1 - \text{requested overheads} \quad (13)$$

T-CONT StartTime pointer indicates the beginning of the T-CONT and StopTime the end of the T-CONT, respectively. The StartTime points at the next byte after the PLOu. The T-CONT may thus consist of the GTC payload only, requested overheads only or both.

6.10 SXGPON upstream burst structure

The modifications of the US GPON burst structure are based on the analysis and modifications introduced to the DS GTC frame as the US burst processing is very similar. It is understood from the DS analysis that each SXGPON US burst and its separately processed building blocks need to be divisible by 8 bytes. The GPON US burst structure was hence analyzed and modified to achieve better applicability with the 8-byte-word-based data processing scheme. As the result of the analysis:

- **DBRu** signaling blocks are not implemented. As discussed in section 5.3.2 SXGPON will have static bandwidth allocations and hence the DBRu block is unnecessary.

- **PLOAMu-Ind**. Following the component re-use approach utilized for the PLOAMd, the PLOAMu is also modified to be protected by CRC-32 instead of CRC-8. Since the DBRu is not implemented in SXGPON, the only optional and relatively small overhead left is the PLOAMu. The PLOAMu is made a mandatory block in SXGPON for each US burst because this reduces the implementation effort associated with burst building logic. The reduction in logic is achieved due to implementation of only one US burst structure compared to two alternative structures if the PLOAMu block was optional.

  Furthermore, 1-byte ONU-ID field of the GPON PLOu can be discarded as a direct consequence of the fact that PLOAMu message always includes ONU-ID. Another overhead of the GPON PLOu is 1-byte Ind field. It is combined with the PLOAMu field and protected with CRC-32. The resulting mandatory block is referred to as PLOAMu-Ind. Furthermore, the block is extended to 24 bytes to be divisible by 8 bytes. The PLOAMu-Ind field is shown in Figure 44. Since PLOAMu-Ind is a mandatory block for every US burst, it is redefined to be a part of the PLOu structure instead of being a part of a T-CONT.

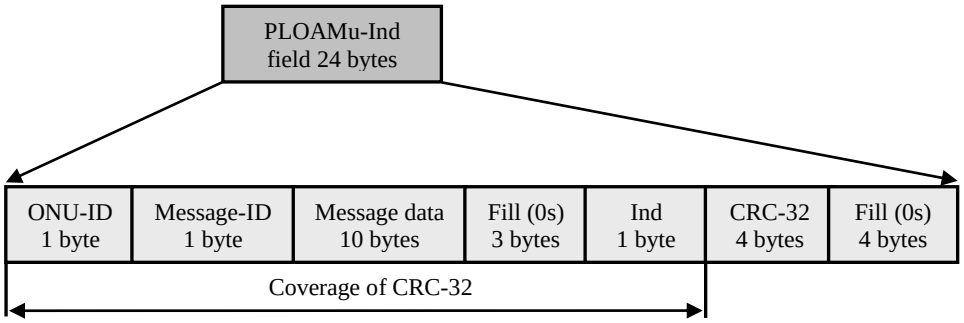

Figure 44. SXGPON PLOAMu-Ind field.

- **PLOu** (Figure 45) is redefined to have a length that is a multiple of 8 bytes due to the fact that synchronizing to the 5 Gbps and 10 Gbps might require a longer preamble and the length of preamble may need to be extended. The PLOu structure is changed to consist of:

  - Variable length **preamble**, } the length of preamble and delimiter is
  - Variable length **delimiter**, } a multiple of 8 bytes
  - 8-byte **BIP-64** that compensates for BIP-8 like in the DS,
  - 24-byte **PLOAM-Ind.**

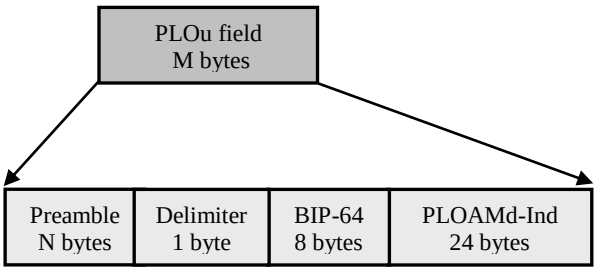

Figure 45. SXGPON PLOu field.

- **SXGTC payload** is equivalent to a T-CONT due to including the PLOAMu in the PLOu and excluding the DBRu block. As shown in Figure 46, the T-CONT StartTime pointer points at the beginning of the SXGTC payload partition. Furthermore, each T-CONT is actually already obliged to be divisible by 8 bytes due to the redefinition of StartTime and EndTime pointers to indicate the first and the last 8-byte-words of the T-CONT, respectively. Consisting of the PLOu and two T-CONTs each US burst is thus divisible by 8 bytes.

The modified US burst structure has an impact on the SXGPON protocol overhead and throughput that are studied in chapter 7.

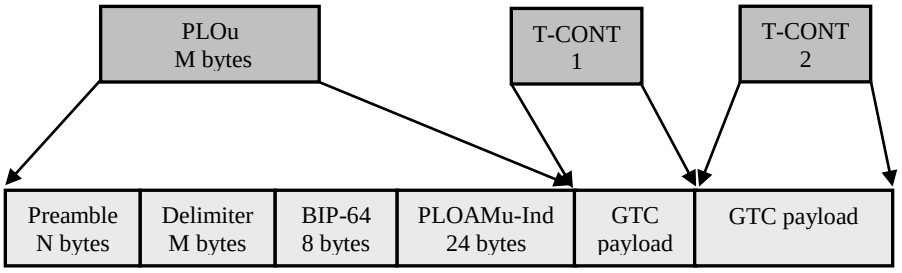

Figure 46. SXGPON burst structure.

6.11 Summary of SXGTC layer system design and optimization

Chapter 6 described the design of the SXGTC layer system details from the SARDANA ONU perspective. As a result of the design, the SXGTC layer is able to logically support transmission at exactly:

- 9.95328 Gbps in the DS,
- 2.48832 Gbps, 4.97664 Gbps and 9.95328 Gbps in the US.

To achieve these transmission rates and the targeted reduction of coding effort on the SXGTC layer implementation, the original DS GTC frame, GPON US burst and GEM frame structures defined by the G.984.3 recommendation [ITU08] were all modified. The resulting frame structures are referred to as DS SXGTC frame, SXGPON US burst and SXGEM frame, respectively.

The approach used for frame structure modifications was based on the estimation of a suitable implementation clock frequency for the FPGA and a corresponding data path width. The data path was specified to be 64-bit i.e. 8-byte wide. All the modifications of the frame structures were targeted to make processing of the frames as straightforward as possible on the 8-byte wide data path. The SXGTC layer system is thus optimized for the 8-byte data path processing. Since the OLT incorporates mostly the same functions as ONU, the reduction of the implementation effort in the OLT is expected to be close to that of the ONU.

7 SARDANA 10 Gigabit-capable Passive Optical Network Transmission Convergence Layer: Bandwidth Efficiency and Expected Throughput

As comes across in the G.984.3 recommendation [ITU08] GPON protocol overhead heavily depends on the GPON system configuration parameters such as transmission rates, number of ONUs, number of T-CONTs, type of T-CONT used, as well as on the traffic Packet Size Distribution (PSD). The logical model of SXGPON is congruent with GPON and hence the SXGPON protocol overhead is affected by the same parameters.

An assessment and comparison of GPON and SXGPON bandwidth efficiency can be made using similar system configuration parameters. In this chapter, the overhead of the SXGPON system is compared to the reference GPON system presented in [HSM06]. The reference GPON configuration parameters used in [HSM06] are:

- 1.25 Gbps transmission rate in the DS,
- 1.25 Gbps transmission rate in the US,
- 16 ONUs,
- 1 T-CONT per ONU,
- even bandwidth allocations between all ONUs,
- several specific frame lengths used for the evaluation of expected GEM overhead.

The GPON reference system overhead is re-evaluated as the [HSM06] lacks some overhead calculation details. The re-evaluated results for GPON are compared to those obtained in [HSM06] to establish a baseline for the reliability of the results presented in this analysis.

As of October 2009, there exists no specification on exact guard time, preamble and delimiter bits for 5 Gbps and 10 Gbps US transmission rates for SXGPON and hence the computation of protocol overhead for these data rates is not yet possible. The SXGPON reference system protocol overheads are estimated based on the reference GPON configuration using as similar as possible overhead affecting parameters to those used in [HSM06]:

- 10 Gbps transmission rate in the DS,
- 2.5 Gbps transmission rate in the US,
- 16 ONUs,
- 2 T-CONTs per ONU,
- even bandwidth allocations between all ONUs,
- same frame lengths as in [HSM06].

Furthermore the SXGPON protocol overhead is evaluated for the SXGPON demonstration network scenario with:

- 10 Gbps transmission rate in the DS,
- 2.5 Gbps transmission rate in the US,
- 4 ONUs,
- 2 T-CONTs per ONU,
- even bandwidth allocations between all ONUs,
- same frame lengths as in [HSM06].

All three of the above configuration scenarios are assessed throughout this chapter. The US burst overheads are researched in section 7.1. The DS GTC and SXGTC frame overheads are examined section 7.2. GEM and SXGEM encapsulation overheads are studied in section 7.3. In section 7.4, the total DS and US overheads for both the GPON and SXGPON systems, analyzed and compared to those presented in [HSM06]. Section 7.5 evaluates expected throughput of the SXGPON system with 10^{-10} BER. Section 7.6 provides a summary of the overhead and throughput results obtained in this chapter.

7.1 Upstream burst overhead

In the GPON reference system [HSM06] general US burst overhead is assumed to consist of:

- PLOu: guard time [ITU03], preamble [ITU03], delimiter [ITU03], BIP, ONU-ID and Ind fields.
- GTC layer overhead: DBRu field.

In the SXGPON reference system the US burst has a comparable structure:

- PLOu: guard time [ITU03], preamble [ITU03], delimiter [ITU03], BIP-64 and PLOAMu-Ind.
- SXGTC layer overhead: OMCI T-CONT allocation.

As discussed in section 5.4.2, the OMCI channel is used for communication between the service defining layers above the SXGTC layer in SXGPON and is hence expected to have some grade of traffic. SXGPON allocates always two T-CONTs per ONU, one for the OMCI control messages and the other for the user frames transmission, thus separating control functions from data. Being dedicated to control, the OMCI T-CONT allocation is thus a part of the US overhead in SXGPON.

The exact bandwidth requirement for the OMCI T-CONT in SXGPON is not known. Initially, each OMCI T-CONT will be allocated for one OMCI message only. If this is not sufficient, the T-CONT allocation will be increased. Each OMCI SXGEM frame allocates exactly 56 bytes consisting of 8-byte SXGEM header and 48-byte OMCI message. The OMCI T-CONT is hence initially 56 bytes long.

Only one T-CONT allocation is used per ONU in the GPON reference system [HSM06]. Both user frames and OMCI frames are sent in this T-CONT allocation. The impact of OMCI on overhead in this case is not discussed in [HSM06], probably due to the fact that exact overhead is very hard to estimate or the impact is relatively low. To make the calculations comparable with those presented in [HSM06], potential OMCI overhead of the GPON US burst is also neglected in this study.

Table 7. US burst overheads.

	Reference 1.25G DS / 1.25G US GPON	**Reference 10G DS / 2.5G US SXGPON**	**Test network 10G DS / 2.5G US SXGPON**
Number of ONUs	16	16	4
GTC or SXGTC frame	19440 bytes	38880 bytes	38880 bytes
Burst length	1215 bytes	2430 bytes	9720 bytes
Guard time	4 bytes	8 bytes	8 bytes
Preamble	5.5 bytes	13.5 bytes	13.5 bytes
Delimiter	2.5 bytes	2.5 bytes	2.5 bytes
BIP field	1 byte	8 bytes	8 bytes
ONU-ID field	1 byte	-	-
Ind field	1 byte	-	-
PLOAMu-Ind	-	24 bytes	24 bytes
Total PLOu overhead	**15 bytes**	**56 bytes**	**56 bytes**
DBRu	2 bytes	-	-
OMCI T-CONT	-	56 bytes	56 bytes
Total GTC or SXGTC layer overhead	**2 bytes**	**56 bytes**	**56 bytes**
Total burst overhead	**17 bytes / 1.40 %**	**112 bytes / 4.61 %**	**112 bytes / 1.15 %**

Both, the GPON and SXGPON US burst overheads can be computed by summing the relevant burst overhead components found in Table 7. The burst length is obtained by dividing the US GTC or SXGTC frame length by the number of ONUs in the system using Equation (14). Final burst overhead results are presented in Table 7.

$$\text{Burst length} = \frac{\text{upstream GTC or SXGTC frame length}}{\text{number of ONUs}} \quad (14)$$

7.2 Downstream GTC and SXGTC frame overhead

In the GPON reference system [HSM06], the DS GTC frame overhead consists of:

- the fixed part of PCBd: PSync, Ident, PLOAMd, BIP, and two PLend fields,
- the variable length US bandwidth map partition: each bandwidth map is 8 bytes long.

In SXGPON the SXGTC frame overhead has a very similar composition:

- the fixed part of PCBd: PSync, Ident, PLOAMd-PLend and BIP-64 fields,
- the variable length US bandwidth map partition: each bandwidth map is 16 bytes long.

Table 8. DS GTC and SXGTC frame overheads.

	Reference 1.25G DS / 1.25G US GPON	**Reference 10G DS / 2.5G US SXGPON**	**Test network 10G DS / 2.5G US SXGPON**
DS GTC or SXGTC frame length	19440 bytes	155520 bytes	155520 bytes
PSync field	4 bytes	4 bytes	4 bytes
Ident field	4 bytes	4 bytes	4 bytes
PLOAMd field	13 bytes	-	-
Plend fields	8 bytes	-	-
PLOAMd-PLend field	-	24 bytes	24 bytes
BIP field	1 byte	8 bytes	8 bytes
Total fixed PCBd overhead	**30 bytes**	**40 bytes**	**40 bytes**
Number of ONUs	16	16	4
Number of T-CONTs per ONU	1	2	2
Length of 1 BW map	8 bytes	16 bytes	16 bytes
US BW map partition overhead	**128 bytes**	**512 bytes**	**128 bytes**
Total DS GTC or SXGTC frame overhead	**158 bytes / 0.81 %**	**552 bytes / 0.35 %**	**168 bytes / 0.11 %**

The DS GTC and SXGTC frame overhead for both GPON and SXGPON can be computed using Equation (15) and Equation (16). The overhead components and the results are summarized in Table 8.

$$\text{US BW map partition overhead} = \text{BW map length} \times \text{T-CONTs per ONU} \times \text{number of ONUs} \quad (15)$$

$$\text{PCBd overhead} = \text{fixed PCBd overhead} + \text{US BW map partition overhead} \quad (16)$$

In the DS, each OMCI frame travels inside the GTC or SXGTC payload partition and cannot be assigned a specific bandwidth. For this reason, the effect of the OMCI channel in the DS is not taken into account in either GPON [HSM06] or SXGPON calculations.

7.3 GEM and SXGEM user frame encapsulation overhead

The effect of SXGEM encapsulation on the overhead compared to GEM encapsulation depends on the expected user frame length. The reference average frame lengths used in [HSM06] are 542 bytes for Microwave Communications, Inc. (MCI) backbone measurement and 655 and 511 bytes for the DS and the US Cable TV (CATV) frames, respectively. These frame lengths are also used for the estimation of GEM and SXGEM encapsulation overheads in the following calculations. GEM and SXGEM frame overheads are defined by Equation (17) and Equation (18), respectively.

$$\text{GEM frame overhead} = \text{GEM header length} \quad (17)$$

$$\text{SXGEM frame overhead} = \text{SXGEM header length} + \text{zero pad length} \quad (18)$$

7.3.1 Length of GTC and SXGTC payload partitions

In the DS, the GEM and SXGEM user frames are carried in the GTC and SXGTC payload partitions, respectively. Neglecting the OMCI channel overhead, the free space for the GEM and SXGEM user frames i.e. the GTC and SXGTC payload partition lengths are evaluated with system specific parameters gathered in Table 9 using Equation (9) and Equation (12), respectively.

In the US, the SXGEM user frames have a dedicated data T-CONT allocation that is equal to the SXGTC payload partition in the US. The length of the data T-CONT depends on the burst overhead and the OMCI T-CONT length. In section 7.1, the OMCI T-CONT allocation was included in the US burst overhead. Due to this fact, the data T-CONT allocation length can be obtained using Equation (19) and SXGPON specific parameters listed in Table 9.

$$\text{Burst payload partition length} = \text{burst length} - \text{burst overhead} \quad (19)$$

Due to neglecting the effect of the OMCI channel in GPON case, the single GPON T-CONT is considered being equal to the GTC payload partition that is correspondingly filled with GEM encapsulated user frames only. Hence, the length of this T-CONT can be computed by the same Equation (19) using GPON specific parameters of Table 9.

Table 9. Common parameters used for GEM and SXGEM DS overhead evaluation.

	Reference 1.25G DS / 1.25G US GPON	**Reference 10G DS / 2.5G US SXGPON**	**Test network 10G DS / 2.5G US SXGPON**
Number of ONUs	16	16	4
DS GTC or SXGTC frame length	19440 bytes	155520 bytes	155520 bytes
DS GTC or SXGTC frame overhead	158 bytes	552 bytes	168 bytes
DS GTC or SXGTC payload length	19282 bytes	154968 bytes	155352 bytes
US GTC or SXGTC frame length	19440 bytes	38880 bytes	38880 bytes
US burst length	1215 bytes	2430 bytes	9720 bytes
US burst overhead	17 bytes	112 bytes	112 bytes
US GTC or SXGTC payload length	1198 bytes	2318 bytes	9608 bytes
GEM or SXGEM header length	5 bytes	8 bytes	8 bytes
Average frame length (MCI) [HSM06]	542 bytes	542 bytes	542 bytes
Average frame length (CATVd) [HSM06]	655 bytes	655 bytes	655 bytes
Average frame length (CATVu) [HSM06]	511 bytes	511 bytes	511 bytes
Average zero padded SXGEM payload length (MCI)	-	544 bytes	544 bytes
Average zero padded SXGEM payload length (CATVd)	-	656 bytes	656 bytes
Average zero padded SXGEM payload length (CATVu)	-	512 bytes	512 bytes

7.3.2 GEM user frame encapsulation overhead

The GEM encapsulation overhead consists of 5 header bytes per encapsulated frame. Since frame fragmentation is used in GPON, it is very likely that a user frame will be fragmented at the end of the GTC payload partition in both the DS and the US. In the frame fragmentation process, the user frame gets divided into two pieces – the first piece occupies the end of the current GTC payload partition and the second the beginning of the next GTC payload partition (Figure 19). The GTC payload partition must begin with GEM header and hence the fragmented user frame will be actually encapsulated with two GEM headers. The total GEM user frame overhead for the DS GTC frame or the US burst can be approximated using:

$$\text{GEM frames in GTC payload} = \frac{\text{GTC payload length - GEM header length}}{\text{average user frame length} + \text{GEM frame overhead}}, \quad (20)$$

$$\text{DS or US GEM overhead} = \text{round up to an integer (GEM frames in GTC payload)} \times \text{GEM header length}. \quad (21)$$

7.3.3 SXGEM user frame encapsulation overhead

The SXGEM encapsulation overhead consists of 8 header bytes per encapsulated frame and possible zero padding bytes. The average frame length from [HSM06] cannot be used directly because of zero padding. Instead, the average length frame is rounded up using Equation (22) to be divisible by eight bytes to reflect the average zero padded SXGEM payload length for SXGEM (Table 9). Since frame fragmentation is not used in SXGPON, the total SXGEM overhead for the SXGTC payload partition can be thus approximated using Equation (23) and Equation (24).

$$\text{average zero padded SXGEM payload length} = \text{round up to a multiple of 8 bytes (average user frame length)} \quad (22)$$

$$\begin{aligned}\text{SXGEM frames in SXGTC payload} &= \frac{\text{SXGTC payload length}}{\text{average SXGEM frame length}} \\ &= \frac{\text{SXGTC payload length}}{\text{average zero padded SXGEM payload length} + \text{SXGEM header length}}\end{aligned} \quad (23)$$

$$\begin{aligned}\text{US or DS SXGEM overhead} &= \text{integer part of (SXGEM frames in SXGTC payload)} \\ &\times \text{SXGEM frame overhead} \\ &+ \text{decimal part of (SXGEM frames in SXGTC payload)} \\ &\times \text{average SXGEM frame length}\end{aligned} \tag{24}$$

7.3.4 GEM and SXGEM user frame encapsulation overhead results

Table 10. GEM and SXGEM DS overhead.

	Reference 1.25G DS / 1.25G US GPON	**Reference 10G DS / 2.5G US SXGPON**	**Test network 10G DS / 2.5G US SXGPON**
DS GTC or SXGTC payload length	19282 bytes	154968 bytes	155352 bytes
GEM or SXGEM frames in GTC or SXGTC payload (MCI)	35.24	280.74	281.43
GEM or SXGEM frames in GTC or SXGTC payload (CATVd)	29.21	233.39	233.96
DS GEM or SXGEM overhead (MCI)	**180 bytes / 0.93 %**	**3208 bytes / 2.06 %**	**3050 bytes / 1.96 %**
DS GEM or SXGEM overhead (CATVd)	**150 bytes / 0.77 %**	**2353 bytes / 1.51 %**	**2737 bytes / 1.76 %**

Table 11. GEM and SXGEM US overhead.

	Reference 1.25G DS / 1.25G US GPON	**Reference 10G DS / 2.5G US SXGPON**	**Test network 10G DS / 2.5G US SXGPON**
US GTC or SXGTC payload length	1198 bytes	2318 bytes	9608 bytes
GEM or SXGEM frames in GTC or SXGTC payload (MCI)	2.18	4.20	17.41
GEM or SXGEM frames in GTC or SXGTC payload (CATVu)	2.31	4.46	18.48
US GEM or SXGEM overhead (MCI)	**15 bytes / 1.23 %**	**150 bytes / 6.17 %**	**394 bytes / 4.05 %**
US GEM or SXGEM Overhead (CATVu)	**15 bytes / 1.23 %**	**274 bytes / 11.28 %**	**410 bytes / 4.22 %**

Table 10 presents the GEM and SXGEM encapsulation overheads in the DS computed with the parameters found in Table 9 and Equations (17-24). Correspondingly, Table 11 shows the US GEM and SXGEM encapsulation overheads results obtained using Equations (17-24) and parameters listed in Table 9.

7.3.5 The effect of user frame fragmentation on SXGEM overhead

As noted in section 5.2.5 the fragmentation is utilized in GPON whereas in SXGPON it is not. In SXGPON frame fragmentation was left out intentionally to reduce the amount of work associated with initial SXGTC layer implementation. This section provides an estimate for how large portion of bandwidth is in fact wasted due to the absence of frame fragmentation. The effect of fragmentation on the SXGPON protocol can be estimated applying the fragmented GEM overhead related Equations (20-21) for SXGEM along with the SXGPON parameters found in Table 9. The fragmented SXGEM overhead results are shown in Table 12 for the DS and in Table 13 for the US cases, respectively.

Table 12. SXGEM overhead in the DS with frame fragmentation.

	Reference 10G DS / 2.5G US SXGPON	**Test network 10G DS / 2.5G US SXGPON**
DS SXGTC payload length	154968 bytes	155352 bytes
SXGEM frames in SXGTC payload (MCI)	280.72	281.42
SXGEM frames in SXGTC payload (CATVd)	233.37	233.95
DS SXGEM overhead (MCI)	**2248 bytes / 1.45 %**	**2256 bytes / 1.45 %**
DS SXGEM overhead (CATVd)	**1872 bytes / 1.20 %**	**1872 bytes / 1.20 %**

Table 13. SXGEM overhead in the US with frame fragmentation.

	Reference 10G DS / 2.5G US SXGPON	**Test network 10G DS / 2.5G US SXGPON**
US SXGTC payload length	2318 bytes	9608 bytes
SXGEM frames in SXGTC payload (MCI)	4.18	17.39
SXGEM frames in SXGTC payload (CATVu)	4.44	18.46
US SXGEM overhead (MCI)	**40 bytes / 1.65 %**	**144 bytes / 1.48 %**
US SXGEM overhead (CATVu)	**40 bytes / 1.65 %**	**152 bytes / 1.56 %**

7.4 GPON and SXGPON protocol total overhead results

The final GPON and SXGPON protocol overhead results are gathered in Table 14 and Table 15. Table 14 DS results are obtained by summing the overhead results of Table 8 and Table 10 together. Table 14 US results are obtained by summing the overhead results of Table 7 and Table 11 together. Table 15 results for the DS are obtained by summing the overhead results of Table 8 and Table 12 together. Table 15 results for the US are obtained by summing the overhead the results of Table 7 and Table 13 together.

Table 14 reveals that the results obtained for GPON in this chapter are essentially the same as those presented in [HSM06] implying reliability of this overhead analysis. The slight difference in the DS is probably caused by a rounding error and the error in section 2.B.4 of [HSM06] where the fixed part of PCBd is computed to be 26 bytes instead of the standard 30 bytes.

Furthermore, Table 14 portrays that the DS GPON and the DS SXGPON protocol overhead percentage does not vary significantly in any of the presented system scenarios even without the SXGPON frame fragmentation capability, thus justifying the modification made to the DS GTC and GEM frames. Table 15 demonstrates that the effect of frame fragmentation on the SXGPON protocol overhead is rather small in the DS, hence justifying omission of fragmentation in the DS. This is an expected result because of the huge length difference between the DS SXGTC frame and the user frame of maximum length. The SXGTC frame is more than 100 times longer than an Ethernet user frame of maximum length i.e. 1518 bytes. Hence, the effect of frame fragmentation must be less than 1 %.

Table 14. GPON and SXGPON total overhead.

	Reference 1.25G DS / 1.25G US GPON [HSM06]	**Reference 1.25G DS / 1.25G US GPON**	**Reference 10G DS / 2.5G US SXGPON**	**Test network 10G DS / 2.5G US SXGPON**
Number of ONUs	16	16	16	4
Total DS overhead (MCI)	**1.71 %**	**1.74 %**	**2.42 %**	**2,07 %**
Total DS overhead (CATVd)	**1.55 %**	**1.58 %**	**1.87 %**	**1.87 %**
Total US overhead (MCI)	**2.63 %**	**2.63 %**	**10.78 %**	**5.21 %**
Total US overhead (CATVu)	**2.63 %**	**2.63 %**	**15.88 %**	**5.37 %**

Contrary to the DS, Table 14 demonstrates that in the US there is a clear difference in the overheads. The US SXGPON protocol overhead of the reference system is approximately six times higher compared to the GPON reference system overhead with the CATVu packets. According to Table 15, the US SXGPON overhead would be only 2.5 times higher if frame fragmentation was utilized. The lack of frame fragmentation in the US hence significantly affects the SXGPON reference system overhead.

The amount of the US overhead was initially estimated to be around 30 %. The US overhead is expected to be high because the US SXGTC frame is 4 times shorter than the DS SXGTC frame. Furthermore, the US SXGTC frame is divided into the bursts that all are likely to have a portion of unused bandwidth when frame fragmentation is not used. With 16 ONUs, each US data T-CONT allocation was calculated to have a length of 2318 bytes (Table 9). The data T-CONT is in this case only around 1.5 times longer than the maximum length Ethernet user frame. The worst case for bandwidth loss results from the situation where there are 1517 bytes of free space at the end of the data T-CONT allocation and an SXGEM encapsulated maximum length Ethernet frame waiting to be transmitted. This situation results approximately in an overhead of

$$\text{SXGPON upstream overhead} = \frac{\text{SXGEM header 8 bytes + Ethernet packet 1518 bytes + 2 zero pad bytes}}{\text{burst payload length 2318 bytes}} = \frac{1528 \text{ bytes}}{2318 \text{ bytes}} = 0.659 \approx 66\ \% \quad . \quad (25)$$

Table 15. Total SXGPON overhead with frame fragmentation.

	Reference 10G DS / 2.5G US SXGPON	**Test network 10G DS / 2.5G US SXGPON**
Number of ONUs	16	4
Total DS overhead with fragmentation (MCI)	**1.80 %**	**1.56 %**
Total DS overhead with fragmentation (CATVd)	**1.56 %**	**1.31 %**
Total US overhead with fragmentation (MCI)	**6.26 %**	**2.63 %**
Total US overhead with fragmentation (CATVu)	**6.26 %**	**2.72 %**

If SXGPON was aimed to support 64 ONUs in the SARDANA network, the lack of user frame fragmentation in the US would completely destroy the system performance. The

SXGPON protocol will however be used only in the SARDANA test and demonstration network with at maximum 4 ONUs and the US protocol overhead for this case is estimated to be around 5,5 % without frame fragmentation (Table 14). This justifies the US burst and GEM frame modifications and the omission of frame fragmentation in the US.

7.5 Expected throughput of SXGPON

The BER of optical budgets in GPON should be no worse than 10^{-10} [ITU03]. The SARDANA network does not have a strict Bit Error Rate (BER) requirement since different optical link budgets and transmission schemes are studied. However, it is reasonable to assume that BER in the SARDANA network should be less or equal to the standard GPON BER. Consequently, the throughput analysis in this section is limited to 10^{-10} BER.

Both the DS and the US SXGTC frames are dropped only if the DS SXGTC frame Plend field is received erroneously. In SXGPON, the Plend field is a part of the PLOAMd-Plend field which is protected by CRC-32 (Figure 39). However, the actual PLOAMd-Plend field region that is vulnerable to bit errors consists of the first 20 bytes only. The 4 last bytes are padded with zeroes and are not protected by CRC-32. The probability of receiving an erroneous 20-byte PLOAMd-Plend region with 10^{-10} BER is

$$P_{\text{Errored PLOAMd-Plend}} = R_{\text{SXGTC drop rate}} = 1-(1-\text{BER})^{(20\text{ bytes}\cdot 8\text{ bits})}. \quad (26)$$

The SXGEM frame is dropped if its header is received erroneously. Furthermore, the following SXGEM frame is also dropped. Synchronization is restored after two dropped SXGEM frames. This is a direct consequence of the SXGEM synchronization state machine shown in Figure 47. The exception is the last SXGEM frame of the SXGTC payload partition. If the header of the last SXGEM frame is received incorrectly, then only this frame is dropped. This is due to the fact that SXGEM synchronization is automatically restored at the beginning of the next SXGTC payload partition. The probability of receiving an erroneous SXGEM header is

$$P_{\text{Errored SXGEM header}} = P_{\text{1 or 2 dropped SXGEM frames}} = R_{\text{SXGEM drop rate 1}} = 1-(1-\text{BER})^{(8\text{ bytes}\cdot 8\text{ bits})}. \quad (27)$$

The drop rate of SXGEM frames according to Figure 47 synchronization state machine is

$$R_{\text{SXGEM drop rate 2}} = 2\cdot R_{\text{SXGEM drop rate 1}}. \quad (28)$$

The expected value of correctly received SXGEM frames in an SXGTC frame is obtained using Equation (29), where $n_{\text{SXGEM frames}}$ is the number of the SXGEM frames that are dropped

according to Figure 47 synchronization state machine and $m_{\text{SXGEM frames}}$ is the number of the SXGEM frames that are dropped according to the erroneous header only.

$$E_{\text{SXGEM frames in SXGTC frame}} = (1 - R_{\text{SXGEM drop rate 2}}) \cdot n_{\text{SXGEM frames}} + (1 - R_{\text{SXGEM drop rate 1}}) \cdot m_{\text{SXGEM frames}} \quad (29)$$

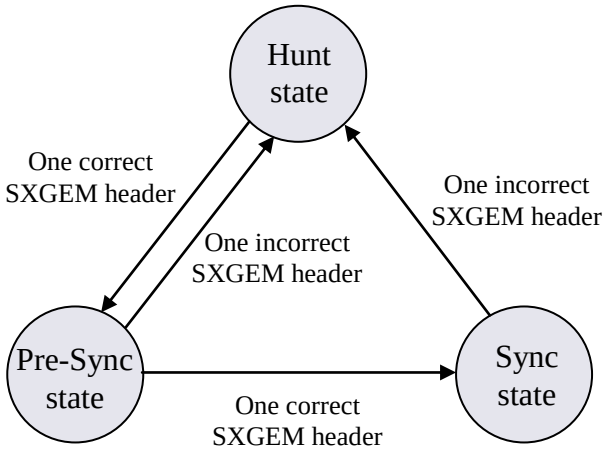

Figure 47. SXGEM synchronization state machine.
Adopted and modified from [ITU08, p. 42, Fig. 8-12].

The expected value of correctly received user frame bytes in one SXGTC frame is

$$E_{\text{user frame bytes in SXGTC frame}} = (1 - R_{\text{SXGTC drop rate}}) \cdot E_{\text{SXGEM frames in SXGTC frame}} \cdot L_{\text{expected user frame length in bytes}}. \quad (30)$$

Table 16. Expected throughput of SXGPON.

	Throughput in 10G DS / 2.5G US SXGPON test network with BER=10^{-10}	**Throughput in 10G DS / 2.5G US SXGPON test network with BER=0**	**Throughput difference between an ideal channel and a channel with BER=10^{-10}**
Number of ONUs	4	4	4
Total DS overhead (MCI)	**9 747 327 720 bps**	**9 747 328 000 bps**	**$2.88 \cdot 10^{-8}$**
Total DS overhead (CATVd)	**9 767 359 719 bps**	**9 767 360 000 bps**	**$2{,}88 \cdot 10^{-8}$**
Total US overhead (MCI)	**2 358 783 933 bps**	**2 358 784 000 bps**	**$2.84 \cdot 10^{-8}$**
Total US overhead (CATVu)	**2 354 687 933 bps**	**2 354 688 000 bps**	**$2.84 \cdot 10^{-8}$**

The expected throughput is

$$E_{\text{Throughput}} = \frac{E_{\text{user frame bytes in SXGTC frame}} \cdot 8 \text{ bits}}{\text{SXGTC frame duration}}. \quad (31)$$

Table 16 summarizes the throughput results obtained for the US and the DS in SXGPON with an error-free channel and a channel having 10^{-10} BER using Equations (26-31) and reference values from Table 9, Table 10 and Table 11. The expected throughput results presented in Table 16 indicate that a channel with 10^{-10} BER is estimated to decrease the throughput by a magnitude of 10^{-8} compared to the ideal channel throughput. The results are considered acceptable for the SXGPON system thus justifying the PLOAMd-Plend field and GEM header modifications.

7.6 Summary of SXGPON bandwidth efficiency and throughput analysis

This chapter presented a detailed comparison of the GPON and SXGPON protocol overheads. The results of the comparison show that the modifications made to the DS GTC frame, US burst and GEM frames had very little impact on the bandwidth efficiency of the SXGPON system. The SXGPON protocol bandwidth efficiency suffers mostly from the lack of frame fragmentation in the US.

However, due to the utilization of SXGPON system only in the SARDANA test and demonstration network with 4 ONUs, the lack of frame fragmentation imposes no real issue. SXGPON is still able to deliver very high bandwidth efficiency, around 98 % in the DS and around 94.5 % in the US for the demonstration and test network.

Furthermore, a channel with 10^{-10} BER is estimated to have only minor effect on the SXGPON system throughput in both the DS and the US. A channel with 10^{-10} BER is estimated to lower the throughput by a factor of 10^{-8} relative to the ideal channel throughput justifying the PLOAMd-Plend field and the GEM header modification. The trade-off between the protocol overhead and the targeted straightforward implementation of the protocol is hence considered welcome.

The GPON overhead results obtained in this chapter are very similar to those obtained in [HSM06]. The SXGPON overhead and bandwidth efficiency were computed using similar formulas applied to SXGPON case and hence is the presented results are considered reliable. The expected throughput results are also considered reliable as they are of the expected magnitude.

8 SARDANA 10 Gigabit-capable Passive Optical Network Transmission Convergence Layer: Implementation for Optical Network Unit

In this chapter, the first ONU SXGTC layer implementation version is described in terms of functional blocks. The ONU SXGTC layer system was implemented in Verilog HDL according to system description and specifications presented in chapters 5 and 6 based on the 64-bit wide data path approach. Sections 8.1 and 8.2 focus on describing the structural and functional implementation. Section 8.3 presents simulation environment and simulation results. Section 8.4 gives a short overview of the implementation results.

8.1 ONU SXGTC implementation environment

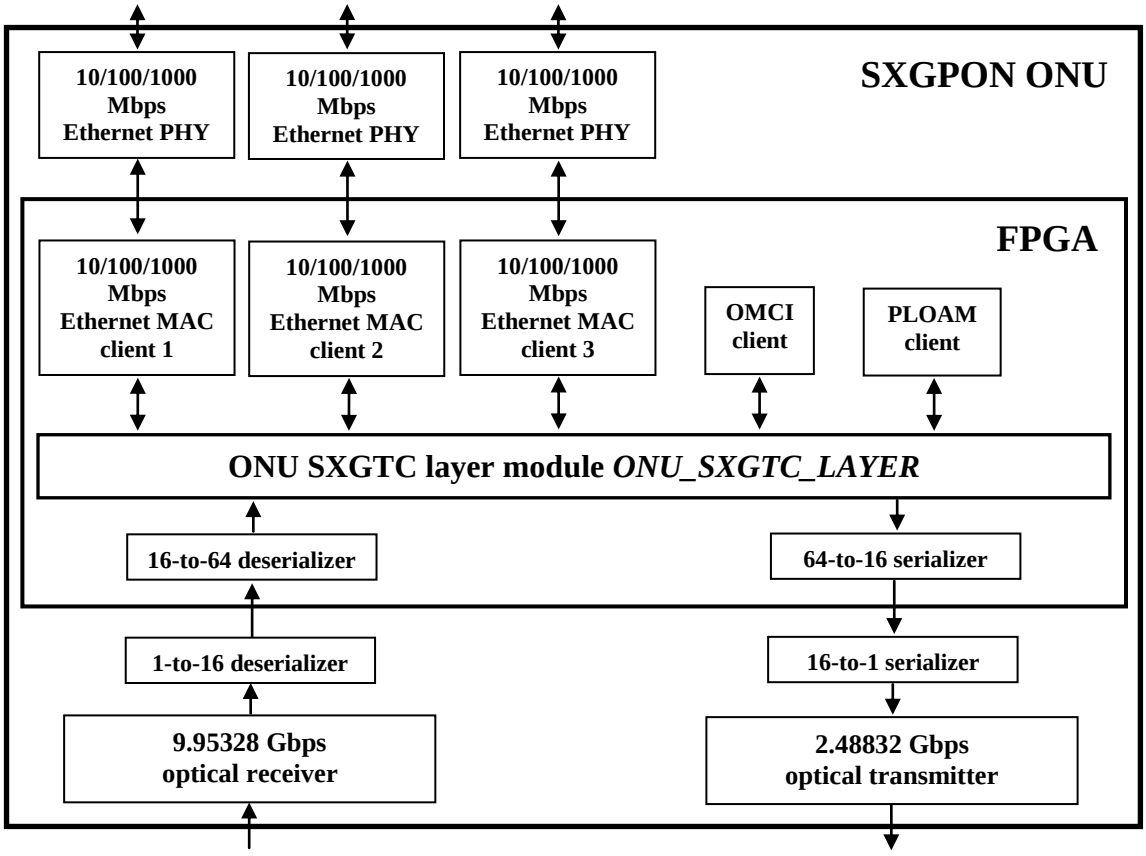

Figure 48. ONU SXGTC layer FPGA implementation environment.

The FPGA implementation environment of the ONU SXGTC layer is depicted in Figure 48. The *ONU_SXGTC_LAYER* module implements the ONU SXGTC layer. Furthermore, Figure 48 reflects the fact that the SXGPON ONU has three 10/100/1000 Mbps Ethernet

connections on the UNI. The Ethernet MAC functions are implemented in the FPGA whereas the Ethernet Physical layer (PHY) blocks are external to the FPGA.

As of December 2009, *ONU_SXGTC_LAYER* is able to operate on:

- 9.95328 Gbps in the DS,
- 2.48832 Gbps in the US.

On the receive side of the PON section interface the *ONU_SXGTC_LAYER* module is connected to the 9.95328 GHz optical receiver via the 1-to-16 and 16-to-64 deserializers. On the transmit side of the PON section interface the *ONU_SXGTC_LAYER* module is connected to the 2.48832 GHz optical transmitter using the 64-to-16 and 16-to-1 serializers, respectively. The serialization and deserialization are performed in two steps because the interfaces of the FPGA used for implementation cannot support 9.95328 Gbps rate.

8.2 ONU SXGTC layer Verilog HDL modules

8.2.1 ONU_SXGTC_LAYER module

ONU_SXGTC_LAYER is a top level structural HDL module that defines the SXGTC protocol interfaces shown in Figure 48 and binds the following lower level architectural HDL modules together:

- *ONU_SYNC,*
- *ONU_DESCRAM,*
- *SXGTC_FRM_PARSER,*
- *USBWMAP_PROCESSOR,*
- *SXGEM_DELINEATOR,*
- *SXGEM_PORT_ID_MUX,*
- *OMCI_ADAPTER_DS,*
- *ETH_ADAPTER_DS,*
- *OMCI_ADAPTER_US,*
- *ETH_ADAPTER_US,*
- *BURST_TX,*
- *ONU_SCRAM,*
- *ONU_REGS.*

The following sections describe the functionality of each Verilog HDL module. The input and the output relationships between all modules are demonstrated in Figure 49.

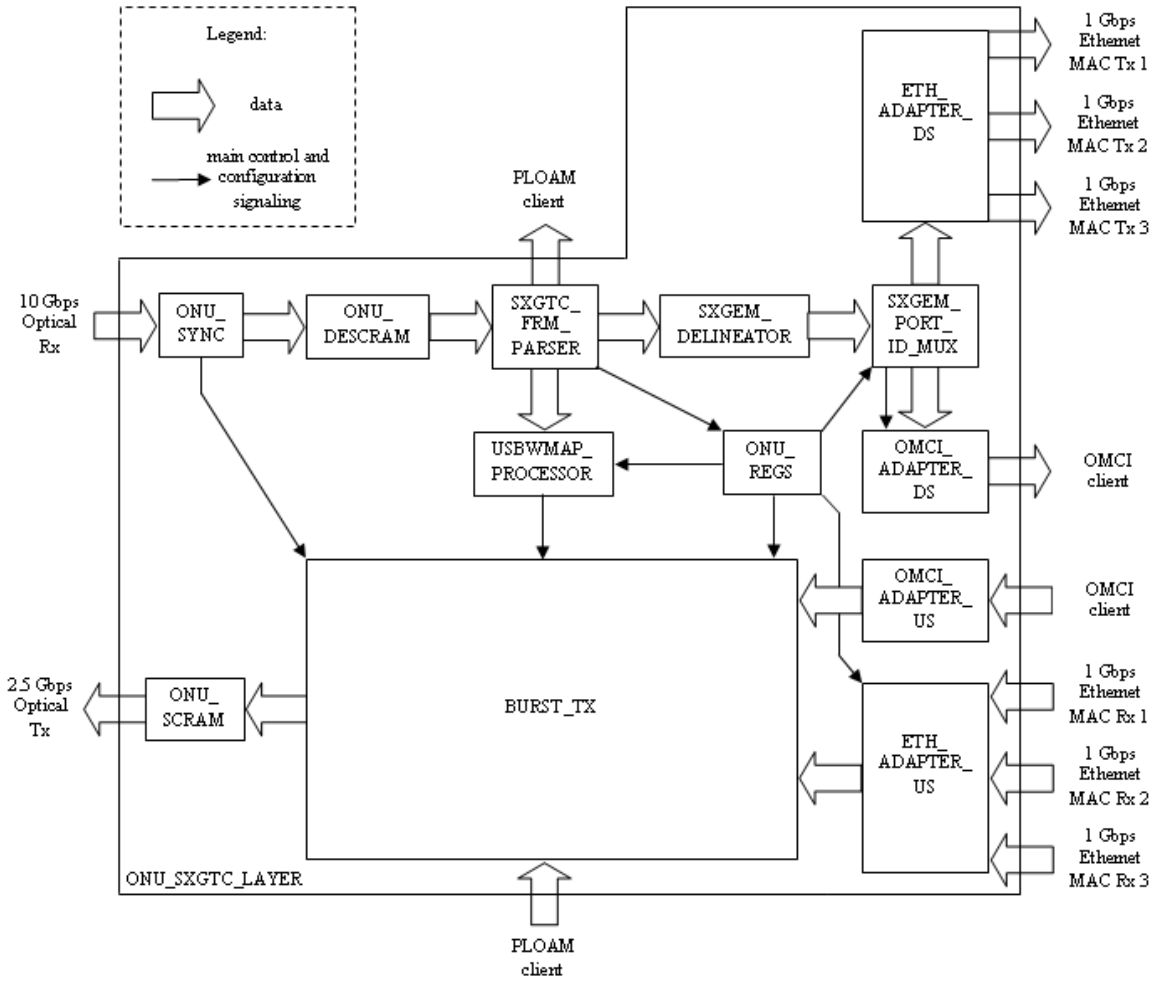

Figure 49. *ONU_SXGTC_LAYER* functional block diagram.

8.2.2 ONU_SYNC module

Main input:

- The DS signal received from the *optical receiver*.

Functionality: *ONU_SYNC* is the DS SXGTC frame and the US burst synchronization module that has the following functions:

- DS synchronization is performed based on the SXGTC frame PCBd PSync field and a synchronization state machine described in the G.984.3 recommendation [ITU08] that is also shown in Figure 50.
- The DS SXGTC frame is aligned to the 8-byte data path.

- US synchronization is performed based on the DS SXGTC frame PCBd PSync field and the equalization delay communicated by the OLT in accordance with the G.984.3 recommendation [ITU08].

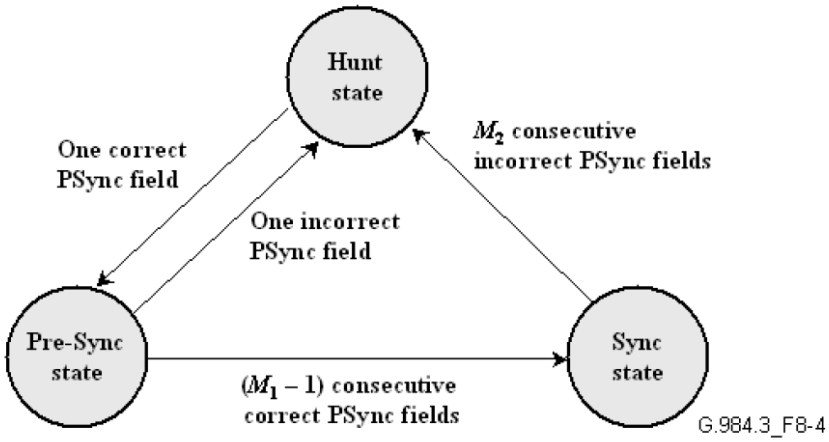

Figure 50. GPON and SXGPON DS synchronization state machine.
Copied from [ITU08, p. 32, Fig. 8-4].

Main outputs:

- Aligned and scrambled DS SXGTC frames to the *ONU_DESCRAM* module.
- US burst synchronization pulse to the *BURST_TX* module.

8.2.3 ONU_DESCRAM module

Main input:

- Scrambled DS SXGTC frames from the *ONU_SYNC* module.

Functionality: *ONU_DESCRAM* implements the DS SXGTC frame descrambler.

- *ONU_DESCRAM* takes advantage of 8-bit scrambler implementation of scrambling polynomial described in the G.984.3 recommendation [ITU08]. This 8-bit scrambler is used to provide the same 8-bit scrambling pattern for each byte of the 8-byte-word.

Main output:

- Descrambled DS SXGTC frames to the *SXGTC_FRM_PARSER* module.

8.2.4 SXGTC_FRM_PARSER module

Main input:

- Descrambled DS SXGTC frames from the *ONU_DESCRAM* module.

Functionality: *SXGTC_FRM_PARSER* is the DS SXGTC frame parsing module that incorporates the following functions:

- Parsing of the DS SXGTC frame into the BIP-64, Blen, PLOAMd, US BW map and SXGTC payload partitions.
- Verification of the Plend-PLOAMd CRC-32 field.
- Processing of the BIP-64 field.

Main outputs:

- PLOAMd messages that are written into the *PLOAMd FIFO* that serves as a DS interface to the *PLOAM entity* found outside the SXGTC layer.
- US BW map partitions that are forwarded to the *USBWMAP_PROCESSOR* module.
- SXGTC payload partitions that are forwarded to the *SXGEM_DELINEATOR* module.

8.2.5 USBWMAP_PROCESSOR module

Main input:

- US BW map partitions from the *SXGTC_FRM_PARSER* module.

Functionality: *USBWMAP_PROCESSOR* is the US bandwidth map processing module that implements the following functions:

- Verification of the correctness of each bandwidth map in the US BW map partition using CRC-32 and discarding of erroneous maps. If either or both of data and OMCI T-CONT bandwidth maps are erroneous the complete allocation structure is discarded.
- Filtering of the bandwidth maps based on the Alloc-IDs. Implementation chooses valid bandwidth maps associated with the data T-CONT and the OMCI T-CONT intended for the particular ONU and discards the irrelevant bandwidth maps.

Main outputs:

- Start time for the OMCI T-CONT to the *BURST_TX* module.
- End time for the OMCI T-CONT to the *BURST_TX* module.
- Start time for the data T-CONT to the *BURST_TX* module.
- End time for the data T-CONT to the *BURST_TX* module.

8.2.6 SXGEM_DELINEATOR module

Main input:

- SXGTC payload partitions from the *SXGTC_FRM_PARSER* module.

Functionality: S*XGEM_DELINEATOR* is the DS SXGEM frame delineation module that implements the following functions:

- The SXGEM frames are parsed from the SXGTC payload partition based on the SXGEM header PLIs and a synchronization state machine described in the G.984.3 recommendation [ITU08]. The correctness of the SXGEM header is verified based on CRC-32 instead of standard GEM HEC [ITU08]. The SXGEM frames with erroneous SXGEM headers are discarded. The adopted state machine is shown in Figure 47.
- The idle SXGEM frames are recognized and discarded.

Main output:

- SXGEM frames to the *SXGEM_PORT_ID_MUX* module.

8.2.7 SXGEM_PORT_ID_MUX module

Main input:

- SXGEM frames from the *SXGEM_DELINEATOR* module.

Functionality: *SXGEM_PORT_ID_MUX* is the DS SXGEM frame filtering module that incorporates the following functions:

- Only the OMCI frames intended for the particular ONU are passed through to the *OMCI_ADAPTER_DS* module. Filtering is based on the SXGEM Port-ID.

- Only the data SXGEM frames intended for the particular ONU are passed through to the *ETH_ADAPTER_DS* module. Filtering is based on the SXGEM Port-ID.
- All the other SXGEM frames are discarded.
- The physical Ethernet client port number is generated based on the SXGEM Port-ID.

Main outputs:

- OMCI SXGEM frames to the *OMCI_ADAPTER_DS* module.
- Data SXGEM frames to the *ETH_ADAPTER_DS* module.
- Physical Ethernet port number to the *ETH_ADAPTER_DS* module.

8.2.8 OMCI_ADAPTER_DS module

Main input:

- OMCI SXGEM frames from the *SXGEM_PORT_ID_MUX* module.

Functionality: *OMCI_ADAPTER_DS* is the DS OMCI SXGEM frame adaptation module that implements the following functions:

- OMCI frame is de-encapsulated from the SXGEM frame.
- OMCI frame is re-arranged into the format required by the *OMCI entity*.

Main output:

- OMCI frames to the *OMCI client* outside the SXGTC layer.

8.2.9 ETH_ADAPTER_DS module

Main inputs:

- Data SXGEM frames from the *SXGEM_PORT_ID_MUX* module.
- Physical Ethernet port number from the *SXGEM_PORT_ID_MUX* module.

Functionality: *ETH_ADAPTER_DS* is the DS data SXGEM frame adaptation module that implements the following functions:

- Ethernet frames are de-encapsulated from the SXGEM frame.

- Ethernet frame are re-arranged into the format required by the *10/100/1000 Mbps Ethernet client.*
- De-encapsulated Ethernet frames are routed to the correct *Ethernet client* based on the physical Ethernet port number.

Main outputs:

- Ethernet frames to the 10/100/1000 Mbps *Ethernet client 1* outside the SXGTC layer.
- Ethernet frames to the 10/100/1000 Mbps *Ethernet client 2* outside the SXGTC layer.
- Ethernet frames to the 10/100/1000 Mbps *Ethernet client 3* outside the SXGTC layer.

8.2.10 OMCI_ADAPTER_US module

Main input:

- OMCI frames from the *OMCI client* outside the SXGTC layer.

Functionality: *OMCI_ADAPTER_US* is the US OMCI frame adaptation and encapsulation module that implements the following functions:

- OMCI frames are acquired from the *OMCI client*.
- OMCI frames are re-arranged to fit into the SXGPON 8-byte wide data path.
- OMCI frames are encapsulated with the SXGEM header. The SXGEM Port-ID is generated based on the information found inside the OMCI frame.
- OMCI SXGEM frames are written into the *OMCI T-CONT FIFO*.

Main output:

- OMCI SXGEM frames into the *OMCI T-CONT FIFO*.

8.2.11 ETH_ADAPTER_US module

Main inputs:

- Ethernet frames from the 10/100/1000 Mbps *Ethernet client 1* outside the SXGTC layer.

- Ethernet frames from the 10/100/1000 Mbps *Ethernet client 2* outside the SXGTC layer.
- Ethernet frames from the 10/100/1000 Mbps *Ethernet client 3* outside the SXGTC layer.

Functionality: *ETH_ADAPTER_US* is the US Ethernet frame adaptation and encapsulation module that implements the following functions:

- Ethernet frames are acquired from the *10/100/1000 Mbps Ethernet client* based on the physical Ethernet port number assigned by the round robin scheduler.
- Ethernet frames are re-arranged to fit into the SXGPON 8-byte wide data path.
- The length of the Ethernet frame is computed.
- Ethernet frames are encapsulated with the SXGEM frames. The SXGEM Port-ID is based on the physical Ethernet port number and the ONU-ID. The SXGEM PLI is based on the computed Ethernet frame length.
- The resulting data SXGEM frame is written into the *DATA T-CONT FIFO*.

Main output:

- Data SXGEM frames into the *DATA T-CONT FIFO*.

8.2.12 BURST_TX module

Main inputs:

- US burst synchronization pulse from the *ONU_SYNC* module.
- Start time for the OMCI T-CONT from the *USBWMAP_PROCESSOR* module.
- End time for the OMCI T-CONT from the *USBWMAP_PROCESSOR* module.
- Start time for the data T-CONT from the *USBWMAP_PROCESSOR* module.
- End time for the data T-CONT from the *USBWMAP_PROCESSOR* module.
- PLOAMu messages from the *PLOAMu FIFO* that serves as the US interface from the *PLOAM client* found outside the SXGTC layer.
- OMCI SXGEM frames from the *OMCI T-CONT FIFO*.
- Data SXGEM frames from the *DATA T-CONT FIFO*.

Functionality: *BURST_TX* is the US burst building and transmitting module that:

- Computes and controls the US burst transmission time.
- Builds the burst overhead consisting of the preamble, delimiter, embedded OAM and PLOAMu partitions.

- Builds the burst OMCI T-CONT allocation partition based on the OMCI T-CONT allocation start and end times provided by the *USBWMAP_PROCESSOR* and the OMCI SXGEM frames found in the *OMCI T-CONT FIFO.*
- Builds the burst data T-CONT allocation partition based on the data T-CONT allocation start and end times provided by the *USBWMAP_PROCESSOR* and the data SXGEM frames found in the *DATA T-CONT FIFO*.
- Fills the OMCI and data T-CONT allocation partitions with the idle SXGEM frames if needed.

Main outputs:

- The US bursts to the *ONU_SCRAM* module.
- Transmit enable/disable signal to the *optical transmitter*.

8.2.13 ONU_SCRAM module

Main input:

- The US bursts from the *BURST_TX* module.

Functionality: *ONU_SCRAM* implements the US burst scrambler.

- ONU_SCRAM takes advantage of 8-bit scrambler implementation of scrambling polynomial described in the G.984.3 recommendation [ITU08]. This 8-bit scrambler is used to provide the same 8-bit scrambling pattern for each byte of the 8-byte-word.

Main output:

- Scrambled US bursts to the *optical transmitter*.

8.2.14 ONU_REGS module

ONU_REGS is a module that consists of memory mapped global registers used for the ONU control and statistics functions. The registers are accessible via the register read and write interface. This configuration interface is not a part of the SXGTC layer and hence the related details are not discussed in this work. The configuration registers themselves however are an essential part of the *ONU_SXGTC_LAYER*. The following SXGTC layer related registers are accessible:

- preamble registers (read/write),
- delimiter registers (read/write).
- ONU-ID register (read/write),
- BIP-64 register (read).

8.2.15 ONU activation state machine module

The ONU activation state machine exchanges PLOAM messages with the OLT. The PLOAM processing entity is implemented in software. For this reason, the activation state machine of the SXGPON ONU is also implemented in software. Furthermore, in commercial GPON, the activation state machine provides the ONU state related information for the network management software. The software implementation of this state machine can hence be considered more adequate than the HDL-based approach. The ONU activation state machine is beyond the scope this thesis due to its software implementation.

8.3 ONU SXGTC layer simulation and implementation verification

ONU_SXGTC_LAYER design process was performed according to the FPGA design flow described in section 4.5 and shown in Figure 14. The test bench used for the RTL design simulations is a combination of SXGTC, SXGEM, Ethernet, OMCI and PLOAM frame generator. The verification in simulations was performed by observing the *ONU_SXGTC_LAYER* module outputs for specific input patterns designed to reveal as many potential functionality errors as possible. The simulations were successfully passed implying the correctness of logical functions. The test bench simulation environment is demonstrated in Figure 51.

As a result of synthesis and place-and–route implementation process described in section 4.5 the design was fitted in the FPGA. The static timing analysis was successfully passed indicating that the ONU SXGTC layer is implementable with 8-byte wide data path approach running at 155.52 MHz in the DS and at 38.88 MHz in the US. Hence, all the design flow verification stages except for the final in-FPGA verification step (Figure 14) were successfully passed for the ONU SXGTC layer HDL implementation.

The in-FPGA verification and the final verification of the SXGTC system will be conducted when all the SARDANA network components are integrated. Verification of complex digital systems is a continuous process and functional problems are yet expected to be encountered in the ONU SXGTC layer implementation.

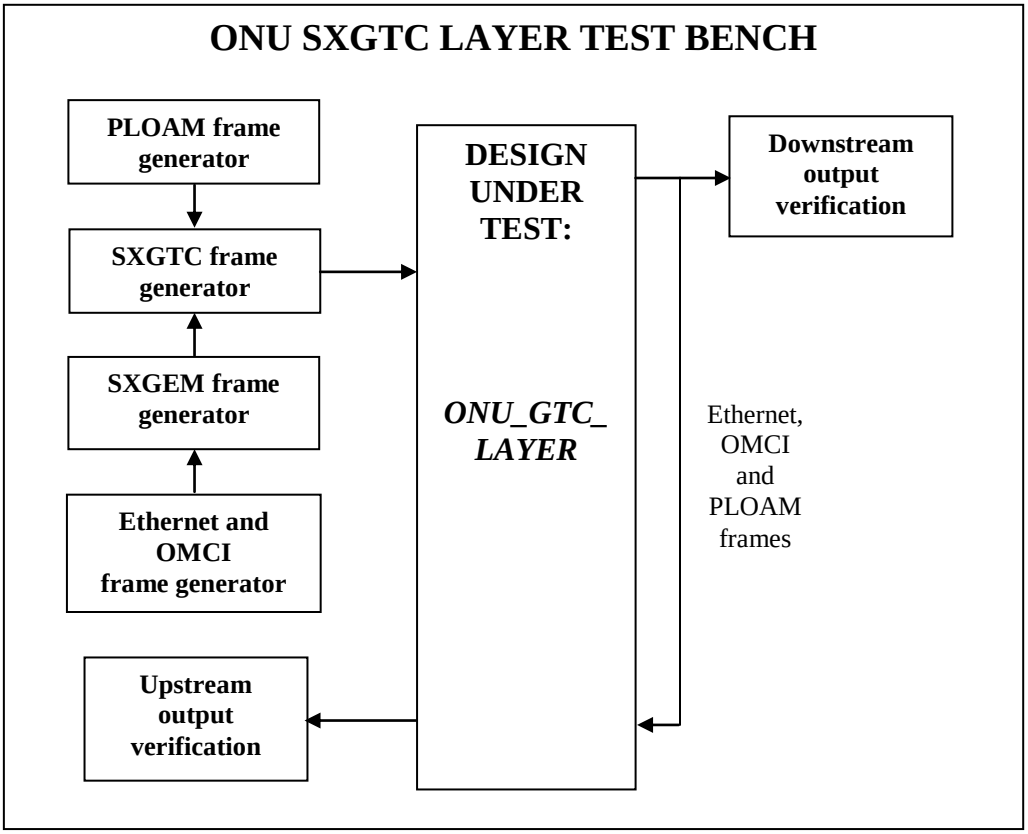

Figure 51. *ONU_SXGTC_LAYER* module simulation environment.

8.4 Summary of ONU SXGTC layer implementation results

This chapter described functional implementation of SXGTC layer in SARDANA ONU. A full set of ONU SXGTC layer implementing Verilog HDL modules and their interconnections were presented. Furthermore, design simulation and testing environment along with the latest results were discussed. As a result, the first ONU SXGTC layer implementation version supports for:

- 9.95328 Gbps transmission rate in the DS,
- 2.48832 Gbps transmission rate in the US.

ONU SXGTC layer modules were successfully implemented in Verilog HDL, simulated with a test bench, placed-and-routed and analyzed for timing but in-FPGA testing was not yet performed due to the lack of some SXGPON OLT and ONU hardware and software components. The successful implementation of the ONU SXGTC layer indicates that 8-byte data path optimized SXGTC protocol developed in this work is indeed implementable in the chosen FPGA.

9 Results and future considerations

9.1 SXGTC layer design and implementation results

The next-generation FTTH/B access network project SARDANA aims to research and test the latest access network technologies with the help of the SARDANA test and demonstration network. SARDANA is a Hybrid WDM/TDM-PON. This thesis presented a MAC protocol solution for the SARDANA test and demonstration network. This MAC protocol is based on the ITU-T G.984.3 GTC layer recommendation [ITU08] that describes the GPON MAC method for up to 2.48832 Gbps. The modified GTC layer was named SXGTC layer, and the complete system was named SXGPON in accordance with ITU-T and FSAN terminology. As a result, the SXGTC protocol is able to support logically for the following transmission rates:

- 9.95328 Gbps in the DS,
- 2.48832 Gbps, 4.97664 Gbps and 9.95328 Gbps in the US.

To achieve the required transmission rates and the targeted reduction in implementation effort, the original DS GTC frame, US GTC burst and GEM frame structures defined by the G.984.3 GTC recommendation [ITU08] were all modified. The resulting new frame structures were named DS SXGTC frame, US SXGTC burst and SXGEM frame, respectively. Moreover, some of the G.984.3 recommendation [ITU08] functionalities considered unnecessary for the SARDANA test and demonstration network were not included in the SXGTC protocol in order to simplify its implementation. The principle of the GPON MAC protocol operation was however left untouched.

The approach used for frame structure modifications was based on the estimation of a suitable clock frequency for the SXGTC protocol implementation in FPGA and a corresponding data path width. The data path was defined to be 8-byte wide. All the modifications of all frame structures were aimed to make the processing of the frames as straightforward as possible on the 8-byte data path. The SXGTC protocol is thus optimized especially for the 8-byte data path processing. The changes and the optimizations were analyzed in this thesis according to the data processing mechanisms of the ONU because the implementation of the ONU SXGTC protocol was assigned to the writer. The OLT incorporates mostly the same functions as the ONU, and hence the reduction of the implementation effort in the OLT is expected to be close to that of the ONU.

The functional implementation of the ONU SXGTC layer presented in this thesis is able to support operation on:

- 9.95328 Gbps in the DS,
- 2.48832 Gbps in the US.

These transmission rates constitute to the first milestone of the SXGPON system development plan [Soi08]. The ONU SXGTC layer was designed and tested according to the FPGA design and verification methodology described in section 4.5 The ONU SXGTC layer was implemented in Verilog HDL, simulated with a test bench designed for the ONU SXGTC layer simulations, synthesized, placed-and-routed and run through static timing analysis successfully. The in-FPGA verification i.e. the final step of the FPGA design and verification flow was not yet possible to perform due to the lack of some SXGPON OLT and ONU hardware and software components. Verification of complex digital systems is a continuous process and functional problems are yet expected to be encountered in the ONU SXGTC layer implementation.

In addition, the SXGPON protocol overhead analysis was carried out for the implemented transmission rate configuration. SXGPON is estimated to have in case of the SARDANA demonstration and test network assembly and configuration approximately 98 % bandwidth efficiency in the DS and 94.5 % in the US, respectively. A channel with 10^{-10} BER is estimated to decrease the throughput by a factor of 10^{-8} compared to the ideal channel throughput. The trade-off between the protocol overhead and the targeted straightforward implementation appears to be very reasonable.

The theoretical SXGPON bandwidth efficiency results are considered very reliable. The bandwidth efficiency was first calculated for a GPON reference system described in [HSM06]. The calculated results are similar to those presented in [HSM06]. The SXGPON bandwidth efficiency was calculated using the same approach as in the case of the reference GPON system. Thus, the bandwidth efficiency results obtained for SXGPON are comparable to the results presented in [HSM06]. The SXGPON bandwidth efficiency with the real traffic may however differ from the theoretical results because the bandwidth efficiency is highly dependent on the PSD. The expected throughput results are also considered reliable as they appear to be of the expected magnitude. In overall, all the requirements and goals imposed for this thesis were successfully achieved.

9.2 SXGPON future development and considerations

The next step of the ONU SXGTC layer verification is to integrate the OLT and the ONU SXGTC layers with the required software components and simulate the combined OLT-ONU SXGTC layer system on the RTL. This simulation step can be followed by the integration of the hardware components and in-FPGA verification. Furthermore, during the project life, the SXGPON implementation is considered to be extended to support:

- 4.97664 Gbps and 9.95328 Gbps transmission rates in the US,
- FEC,
- user and OMCI frame fragmentation.

The implementation of FEC is considered very important in further SXGPON development, as it can help to extend physical reach of the SARDANA network. User and OMCI frame fragmentation in the US is seen desirable for SXGPON if used with more than 4 ONUs. In the SARDANA test and demonstration network there will be only 4 ONUs and hence SXGEM fragmentation can be either implemented as the last feature or completely left out based on the SXGPON bandwidth efficiency results. As such, the SXGTC layer system is not expected to yield any particular value outside the SARDANA project. The protocol cannot be used in a commercial system due to the lack of several vital functions such as encryption and DBA.

9.3 Commercial XGPON future development and considerations

Most of the changes made in SXGPON are not expected to have significance outside the SARDANA project as they were made only to reduce the workload associated with the SXGTC layer implementation and are not expected to affect the future XGPON standard directly. All the GPON functionalities that were not included in SXGPON are expected to be implemented in future commercial XGPON. DBA is considered very important for the next-generation networks. Traffic encryption is a must in TDM-PON systems. For the commercial case with 8-64 ONUs each burst will be shorter with respect to the increasing number of ONUs and hence implementation of user frame fragmentation in the US is expected to be critical to system performance.

Valuable lessons learned in SXGPON protocol development are the 8-byte-word-based data processing approach for the DS SXGTC frame and the US burst, and a new 8-byte-word-based SXGEM encapsulation format that considerably simplifies the implementation effort on the 8-byte data path. It is likely that due to technological limitations and complexity, the future XGPON standard will be optimized towards more convenient implementation rather than bandwidth efficiency [Eff09], and hence incorporate similar to the SXGTC protocol frame changes. The latest XGPON recommendation draft [FSAN10] seems to imply optimization with respect to the 4-byte-based data processing. The base SXGTC layer HDL descriptions developed as a part of this thesis are hence considered very useful for the future commercial XGPON development.

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