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TRANSMITTER ARCHITECTURES WITH DIGITAL MODULATORS, D/A CONVERTERS AND SWITCHING-MODE POWER AMPLIFIERS

Doctoral Dissertation

Johan Sommarek

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Dissertation for the degree of Doctor of Science in Technology to be presented with due permission of the Department of Electrical and Communications Engineering for public examination and debate in Auditorium S4 at Helsinki University of Technology (Espoo, Finland) on the 20th of June, 2007, at 12 noon.

Helsinki University of Technology
Department of Electrical and Communications Engineering
Electronic Circuit Design Laboratory

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Opponent(s)	Prof. Mohammed Ismail El-Naggar
Supervisor	Prof. Kari Halonen
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Abstract

This thesis is composed of nine publications and an overview of the research topic, which also summarises the work. The research described in this thesis focuses on research into the digitalisation of wireless communication base station transmitters. In particular it has three foci: digital modulation, D/A conversion and switching-mode power amplification. The main interest in the implementation of these circuits is in CMOS.

The work summarizes the designs of several circuit blocks of a wireless transmitter base station. In the baseband stage, a multicarrier digital modulator that combines multiple modulated signals at different carrier frequencies digitally at baseband, and a multimode digital modulator that can be operated for three different communications standards, are implemented as integrated circuits. The digital modulators include digital power ramping and power level control units for transmission bursts. The upconversion of the baseband signal is implemented using an integrated digital quadrature modulator.

The work presented provides insight into the digital-to-analogue interface in the transmitters. This interface is studied both by implementing an intermediate frequency D/A converter in BiCMOS technology and bandpass Delta-Sigma modulator-based D/A conversion in CMOS technology.

Finally, the last part of the work discusses switching-mode power amplifiers which are experimented with both as discrete and integrated implementations in conjunction with 1-bit Delta-Sigma modulation and pulse-width modulation as input signal generation methods.

Keywords digital modulator, current-steering D/A converter, Delta-Sigma modulator, switching-mode power amplifier

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Tiivistelmä
Tämä väitöskirja koostuu yhdeksästä julkaisusta ja tutkimusaiheen yhteenvedosta. Väitöskirjassa esitetty tutkimus keskittyy langattaman viestinnän tukiasemien lähettimien digitalisoinnin tutkimukseen. Yksityiskohtaisemmin tutkimusalueet ovat: digitaalinen modulaatio, D/A muunnos ja kytkinmuotoiset tehovahvistimet. Näiden elektronisten piirien toteutuksessa keskitytään CMOS teknologiaan.

Työ vetää yhteen useiden langattoman viestinnän tukiasemien lähettimien piirilohkojen suunnittelun. Kantataajuusasteella toteutetaan integroituna piirinä monikantoaaltoinen digitaalinen modulaattori, joka yhdistää useita moduloituja signaaleja eri kantoaalloilla digitaalisesti ja monistandardi digitaalinen modulaatori, joka tukee kolmea eri viestintästandardia. Digitaaliset modulaattoripiirit sisältävät digitaalisen tehoramping ja tehotason säätöyksikön lähetyspurskeita varten. Kantataajuussignaalin ylössekoitus toteutetaan integroitua digitaalista kvadratuurimodulaattoria käyttäen.

Esitetty työ antaa näkemystä lähettimien digitalia-analogia rajapintaan, jota tutkitaan toteuttamalla välitaajuinen D/A muunnin BiCMOS teknologialla ja päästökaistainen Delta-Sigma-modulaattoripohjainen D/A muunnin CMOS teknologialla.

Lopuksi työn viimeinen osa käsittelee kytkinmuotoisia tehovahvistimia, joita tutkitaan kokeellisesti sekä erilliskomponteina toteutettuina piirein että integroiduin piirein toteutettuina käyttäen sisääntulosignaalin muodostamismenetemänä yksibittistä Delta-Sigma-modulaatiota ja pulssin leveys modulaatiota.

Asiasanat digitaalinen modulaattori, D/A-muunnin, Delta-Sigma modulaattori, kytkinmuotoinen tehovahvistin

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Preface

This thesis was researched at the Electronic Circuit Design Laboratory, Helsinki University of Technology. Some of the projects that this thesis is based on were financed by TEKES and Nokia Networks. My studies were also funded by the Graduate School in Electronics, Telecommunications and Automation (GETA). So an enormous “Thank you” goes to Iiro Hartimo, the boss of GETA at TKK, for all the support he and GETA have given me.

I feel very grateful to Professor Kari Halonen for giving me the opportunity to work as part of the projects and for giving me an opportunity to write this thesis. I want to thank my instructors Jouko Vankka and Hannu Tenhunen for the guidance they have given me and also Emil Aaltosen Säätiö, Nokia Foundation, Tekniikan Edistämissäätiö and Elektroniikka Insinöörien Säätiö for the financial support they have given.

I would like to thank Jaakko Ketola, Ilari Teikari, Jonne Lindeberg, Olli Väänänen, Marko Kosunen, Antti Virtanen, Ville Saari and Pasi Juurakko for their contribution to the work. I am also grateful to my room mates Jaakko, Ilari, Olli, Lasse Aaltonen and Yang Fan and all the staff of the Electronic Circuit Design Laboratory for all the help and support they have given and for creating a stimulating working ambience.

I would also like to thank my friends, parents, sister and girlfriend for their all kind of support for my educational and non-educational activities.

Espoo, 21st May 2007

Johan Sommarek

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Contents

Symbols and abbreviations

A_{VT}	Threshold factor matching parameter of a transistor
A_{β}	Current factor matching parameter of a transistor
B	Bandwidth
C_d	Drain capacitance
C_g	Gate capacitance
E	Signal envelope
E_L	Inductive energy loss
E_d	Capacitive energy loss
E_g	Energy lost at the gate of a switching-mode PA
E_m	Maximum value of $E(t)$
F_r	Phase increment or frequency control word
G	Gain
H	Transfer function
H_e	Loop filter transfer function
I_+	Output current (+ node)
I_-	Output current (- node)
I_d	Drain current
I_g	Current to the gate of a transistor
I_{out}	Output current
L	Interpolation factor

L	Phase accumulator word length
L	Transistor gate length
L_d	Drain inductance
N	DAC resolution
N	Number of elementary angles
N_0	Wordlength of input signal
N_1	Wordlength of the output of an interpolator
P_L	Inductive power loss
P_{SAT}	Power loss due to saturation voltage
P_d	Capacitive power loss
$P_{g,\sin}$	Power loss at the gate of a switching-mode PA with a sinusoidal drive signal
P_{gs}	Power loss at the gate of a switching-mode PA with a square wave drive signal
P_{in}	Input power
P_{out}	Output power
Q	Charge
R	Oversampling ratio, resistance
R_g	Gate resistance
R_{load}	Load resistance
V_{GS}	Gate-source voltage
V_{SAT}	Saturation voltage of a switch transistor
V_T	Threshold voltage
V_{ct}	Voltage from the node between the switch transistors to ground
V_{dd}	Positive supply voltage
V_d	Drain voltage
V_{gs}	Gate-source voltage

V_{in}	Input voltage
V_{out}	Output voltage
W	Phase accumulator output wordlength
W	Transistor gate width
δ_s	Skin depth
γ	Coarse rotation angle
κ	Quadrant rotation angle
μ_0	Permeability in vacuum
μ_i	Rotation sequence
ω	Fundamental frequency
ϕ	Phase
σ	Conductivity
$\sigma(I)$	Unit current source standard variation
inv_norm	Inverse cumulative normal distribution.
θ	Rotation angle
b_l	Control bit of the switches of a current-steering DAC
$e(n)$	Error signal
$f(x)$	Approximation function in interpolation
f_N	Data rate
f_T	Gain bandwidth
f_{clk}	Clock frequency
f_{out}	Output frequency
f_s	Sampling frequency
f_{sw}	Switching frequency of a switching-mode power amplifier
m_k	Slope of segment k

p_k	Second order interpolation coefficient for segment k
s	Number of segments
w_l	Weight coefficient
x	Input signal
x_f	Final x-coordinate
y	Output signal
y_f	Final y-coordinate
y_k	Initial amplitude of segment k
ACLR	Adjacent channel leakage ratio
AM	Amplitude modulation
BP	Bandpass
BPF	Bandpass filter
BiCMOS	Bipolar CMOS
CDMA	Code division multiple access
CIFB	Cascade of integrators feedback
CIFF	Cascade of integrators feedforward
CMCD	Current-mode class-D
CMOS	Complementary metal oxide semiconductor
CORDIC	Coordinate rotation digital computer
CRFB	Cascade of resonators feedback
CRFF	Cascade of resonators feedforward
CSD	Canonic signed digit
D/A	Digital-to-Analogue
DAC	D/A converter
dBc	Decibels below carrier

DC	Direct current
DDFS	Direct digital frequency synthesizer
DDRM	Direct digital RF modulation
DDS	Direct digital synthesizer
DEM	Dynamic element matching
DNL	Differential nonlinearity
DRFC	Direct digital RF converter
EDGE	Enhanced data rates for GSM evolution
EEAS	Extended Elementary Angle Set
EER	Envelope elimination and restoration
ENOB	Effective number of bits
FET	Field-effect transistor
FIR	Finite impulse response
FPGA	Field programmable gate array
GSM	Global System for Mobile Communications
I	In-phase
IF	Intermediate frequency
IF	Interpolation filter
INL	Integral nonlinearity
LINC	Linear amplificaton with nonlinear components
LO	Local oscillator
LSB	Least significant bit
LUT	Look-up table
MASH	Multi-stage noise shaping
MOS	Metal oxide semiconductor

MSB	Most significant bit
MSE	Mean square error
MTPR	Multi-tone power ratio
MVR	Modified vector rotational
NL	Noise-shaping loop
NTF	Noise transfer function
OSR	Oversampling ratio
PA	Power amplifier
PF	Post-filter
PM	Phase modulation
PWM	Pulse-width modulation
Q	Quadrature
QAM	Quadrature amplitude modulation
R	Resistor
RAM	Random access memory
RF	Radio frequency
ROM	Read-only memory
SFDR	Spurious-free dynamic range
SNDR	Signal-to-noise-and-distortion ratio
SNR	Signal-to-noise ratio
STF	Signal transfer function
VCO	Voltage controlled oscillator
VDD	Positive supply voltage
VHDL	VHSIC Hardware Description Language
VMCD	Voltage-mode class-D

WCDMA	Wideband CDMA
ZCS	Zero-current-switching
ZVS	Zero-voltage-switching

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List of Publications

P1 J. Vankka, J. Pyykönen, J. Sommarek, M. Honkanen and K. Halonen, A Multicarrier GMSK Modulator for Base Station, IEEE Journal of Solid-State Circuits, Vol. 37, No 10, pp. 1226-1234 October 2002.

P2 J. Vankka, J. Ketola, O. Väänänen, J. Sommarek, M. Kosunen and K. Halonen 'A GSM/EDGE/WCDMA Modulator With On-chip D/A Converter for base station,' IEEE Trans. on Circuits and Systems Part II, Vol 49, No.10, pp: 645-655, Oct. 2002

P3 J. Sommarek, M. Kosunen, J. Vankka, K. Halonen, '14-bit 110 MHz CMOS D/A Converter', Proc. 21st Norchip Conference, Nov. 10 - 11, 2003, Riga, Latvia, pp. 104-107.

P4 J. Vankka, J. Sommarek, J. Ketola, I. Teikari and K. A. I. Halonen, 'A Digital Quadrature Modulator With On-Chip D/A Converter', IEEE Journal Of Solid-State Circuits, Vol. 38, No 10, October 2003, pp. 1635-1642

P5 J. Sommarek, J. Vankka, J. Ketola, J. Lindeberg and K. Halonen, 'A Digital Modulator with Bandpass Delta-Sigma Modulator', Springer Science + Business Media Inc., Analog Integrated Circuits and Signal Processing, Vol. 43, No 1, pp. 81-86, April 2005

P6 J. Lindeberg, J. Sommarek, J. Vankka and K. Halonen, 'A 1.5V direct digital synthesizer with tunable Delta-Sigma modulator in 0.13 μm CMOS,' IEEE Journal of Solid-State Circuits Vol. 40, No 9, pp. 1978-1982 September 2005

P7 J. Sommarek, A. Virtanen, J. Vankka and K. Halonen, 'Comparison of Different Class-D Power Amplifier Topologies for 1-bit RF Band-Pass Delta-Sigma D/A Converters', International Symposium on Signals Systems and Electronics, ISSSE 2004

P8 J. Sommarek, A. Virtanen, J. Vankka and K. Halonen, 'Comparison of Different Class-D Power Amplifier Topologies for 1-bit Band-Pass Delta-Sigma D/A Converters, Proceedings of 22nd Norchip Conference, November 8-9, 2004, Oslo, Norway, pp. 115-118.

P9 J. Sommarek, V. Saari, J. Lindeberg, J. Vankka and K. Halonen, 'A 20 MHz BP-PWM and BP-DSM Class-D PA in 0.18 μm CMOS', Proc. of International Conference on Electronics, Circuits and Systems, December 11 - 14, 2005, Gammarth, Tunisia

Contribution of the author

As a general guideline, the first author of each publication carries the main responsibility for the manuscript.

In paper P1, I carried out the circuit design, analysis and measurements. Jouko Vankka was involved as instructor and in system and architecture design and was behind the idea of the ramp generator. Jaakko Pyykönen designed the D/A converter and Mauri Honkanen was involved in the system specification.

In paper P2, I designed the ramp generator and the D/A converter, which is presented in more detail in paper P3, Jaakko Ketola designed the digital part of the circuit and Olli Väänänen and Jouko Vankka were involved in system and architecture design.

I designed the D/A converter presented in P3, Marko Kosunen instructed me in the design and performed the SFDR measurements with the cascade transistors by-passed.

In paper P4, I designed the digital part, including VHDL code and circuit design, but excluding the multiplexer at the digital-analogue interface, which was designed by Jaakko Ketola. Ilari Teikari designed the D/A converter. I performed the measurements related to the digital part of the circuit. Jouko Vankka was involved in system and architecture design and as instructor.

In paper P5, I designed the VHDL code of the upconverter and performed the measurements of the circuit. Jaakko Ketola designed the $\Delta\Sigma$-modulator and performed the integrated circuit of the digital part. Jonne Lindeberg designed the D/A converter. Jouko Vankka was involved as instructor and in system and architecture design.

I designed the digital part of the circuit presented in paper P6, while Jonne Lindeberg designed the D/A converter and measured the circuit. Jonne Lindeberg and Jouko Vankka were involved in system and architecture design and Jouko Vankka as instructor.

In paper P7, I performed the simulations and was the instructor of Antti Virtanen, who wrote the APLAC code that I developed further for the simulations. The introduction was written by Antti Virtanen. Jouko Vankka was involved as instructor.

In paper P8, I performed the simulations, the circuit design and all the measurements. I developed further the APLAC code that had originally been designed by Antti Virtanen in paper P7. Jouko Vankka was involved as instructor.

In paper P9, I made the simulations, and all the measurements. In the simulations of the $\Delta\Sigma$-modulator I utilized Matlab code originally written by Jonne Lindeberg. Ville

Saari designed the integrated power amplifier. Jouko Vankka was involved as instructor.

Chapter 1

Introduction

1.1 Background

Mobile communication systems had gained high market penetration by the time of writing this thesis. Competition has forced the price of mobile communication down, thereby forcing the system manufacturers to cut costs in order to gain higher profit margins. In particular, mobile telephony has seen fierce competition; not only does this competition put pressure on the prices of mobile phones and calls, but also on the prices of the hardware used in the base stations. In addition to mobile telephony, the newest generations of mobile communications also provide mobile internet services where the clients tend to demand higher and higher bandwidths all the time. Thus the development is towards reduced cost and higher bandwidths.

Also, the transition from older to newer generations sets demand for support of multiple standards as the generation shift is not instantaneous; also, integration of several standards into a single chip involves higher volumes for the chip and thereby aids the reduction of its unit cost. Thus the pressure is on to demand flexibility from the base station to accommodate transmission of multiple standard communication signals and to be able to service an increasing number of clients simultaneously. Moreover, the cost pressure motivates a movement towards the digitalization and higher integration level of the transmitters as the analogue parts tend to be more costly, less flexible and require more tuning.

The switching-mode power amplifiers have theoretically superior efficiencies compared to those of linear power amplifiers. Also, in practice, in many applications they attain significantly higher efficiencies than linear power amplifiers.

Therefore, this thesis contributes to this digitalization effort by presenting research on multicarrier, multimode digital modulators and digital quadrature modulators. At the digital-analogue interface both Nyquist-rate D/A converters and oversampling $\Delta\Sigma$-modulation based D/A converters are researched. Finally switching-mode power amplifi-

ers are studied in combination with ΔΣ-D/A converters.

1.2 Objectives of the work

The research described in this thesis focuses on the design of digital modulators based on direct digital frequency synthesis, digital quadrature modulator based upconversion of the digital baseband signal to IF, D/A conversion using a Nyquist-rate current-steering D/A converter and ΔΣ-modulator-based D/A conversion at IF. Another objective was to investigate the suitabilities of a 1-bit bandpass ΔΣ-modulator and a bandpass pulse-width modulator to drive a Class-D power amplifier.

1.3 Contents of the thesis

The thesis is organised into two parts. In the first part, an overview of the design issues related to the digital modulation, upconversion, D/A conversion and power amplification in wireless communication base station transmitters is given to put into context and summarize the technical work that has been carried out. First, Chapter 2 reviews transmitter architectures for wireless communication base station applications. In Chapter 3, issues related to the design of digital modulators for wireless communication base station transmitter systems are discussed and CORDIC and LUT-based direct digital synthesizers are reviewed. Chapter 4 summarizes different digital-analogue conversion methods for wireless communication base station transmitter systems, concentrating on current-steering D/A converters and D/A converters utilising ΔΣ modulation. In Chapter 5, switching-mode power amplifier topologies are briefly reviewed and the theory and fundamental concepts behind Class-D power amplifiers are introduced. The second part of this thesis is composed of the published papers.

Chapter 2

Transmitter architecture in wireless communication base stations

Conventionally, the signal processing in wireless communication takes place in the digital domain with signal frequencies significantly lower than the radio frequency (RF) that is needed for transmission. Thus, in order to perform the transmission, an upconversion of the baseband signal is needed. This upconversion can be accomplished in various manners including analogue mixing, direct digital conversion and combined digital/analogue upconversion.

2.1 Analogue Up-mixing

In a fully analogue upconversion the digital baseband signal is converted into an analogue signal and then upconverted into a radio frequency signal in the analogue domain. The upconversion chain can consist of one, two or more mixer stages.

2.1.1 Direct-Conversion Transmitters

If the transmitted carrier frequency equals the local oscillator frequency, the architecture is called direct conversion. In this case, the modulation and upconversion coincide [Razavi 98]. A block diagram of the architecture is shown in Figure 2.1. In this architecture, the power amplifier may disturb the transmit local oscillator; this is because the output of the power amplifier is a modulated high-power signal centred at the LO frequency. Despite the existence of difference shielding techniques employed to isolate the VCO, it is still difficult the avoid the problem completely [Razavi 98].

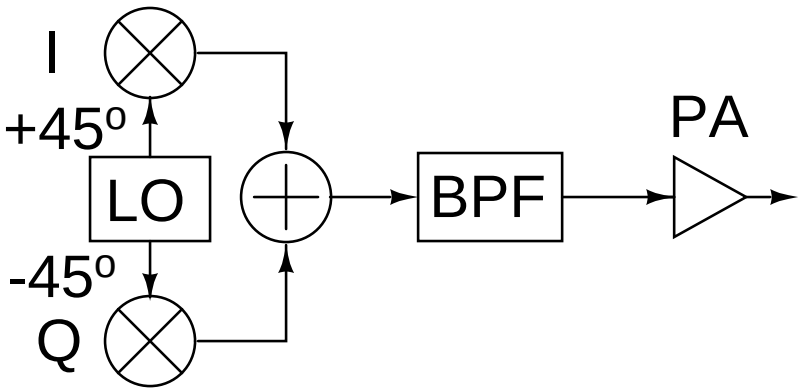

Figure 2.1 Direct conversion transmitter

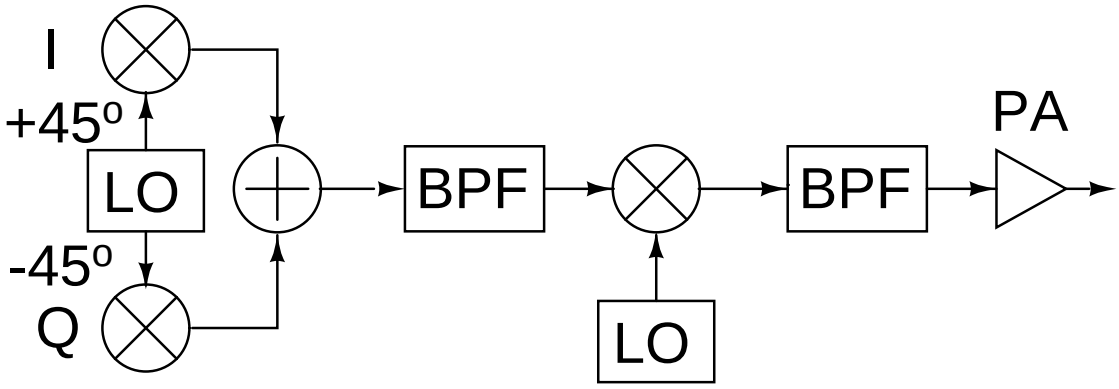

Figure 2.2 Two-step transmitter

2.1.2 Two-Step Transmitters

One approach to circumventing the LO pulling problem is to upconvert the baseband signal in two or more steps so that the power amplifier output spectrum is far from the frequency of the VCOs. For example, the architecture could look as in Figure 2.2, where the baseband I and Q channels are quadrature modulated at a lower frequency $\omega_1$and the result is upconverted to $\omega_1 + \omega_2$ by mixing and bandpass filtering. The first bandpass filter suppresses the harmonics of the IF signal, whilst the second one removes the undesired sideband around $\omega_1 - \omega_2$ [Razavi 98].

2.2 Digital/Analogue

In digital/analogue upconversion, the signal is first upconverted digitally into an intermediate frequency (IF) signal using a digital quadrature modulator and then mixed up to the radio frequency using analogue techniques. This decreases the need for analogue components in the system. In addition, performing the quadrature modulation digitally yields high precision and a perfect I/Q-channel matching. Figure 2.3 shows an example block

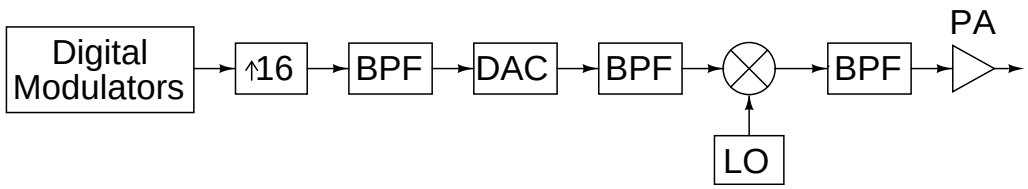

Figure 2.3 Block diagram of a digital/analogue upconversion chain

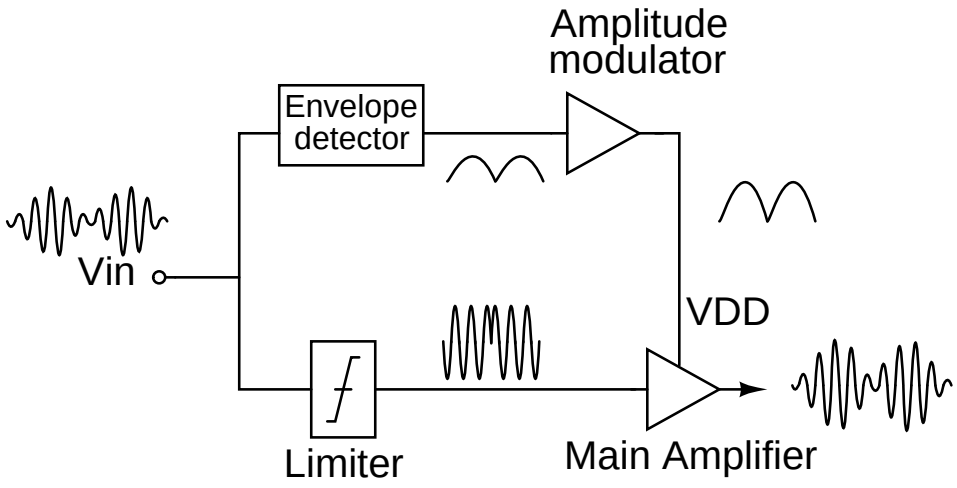

Figure 2.4 EER system block diagram

diagram of the system.

2.3 Transmitter architectures utilising non-linear power amplifiers

2.3.1 Envelope Elimination and Restoration

An envelope elimination and restoration (EER) architecture endeavours to achieve high efficiency on non-constant envelope signals by feeding in the envelope of the transmitted signal to a non-linear, i.e. Class-E [Funk 96, Saari 05], Class-D [Raab 94b, Raab 94a] or Class-F [Weiss 01], power amplifier through its supply voltage, whilst the power amplifier is driven with a phase modulated signal. The idea is based on the fact that any narrow-band signal is equivalent to simultaneous amplitude and phase modulation of a carrier [Weiss 01]. So, in this architecture, the signal is split into an amplitude modulated (AM) and a phase modulated (PM) signal, which are then processed separately before combining them at the non-linear power amplifier, as shown in Figure 2.4. The amplitude and phase modulated signals can be generated with analogue circuitry or by digital signal processing [Saari 05], in which case it can also be called polar modulation. Polar modulation can also be used to create multimode operation in a transmitter [Heinbach 01]. This

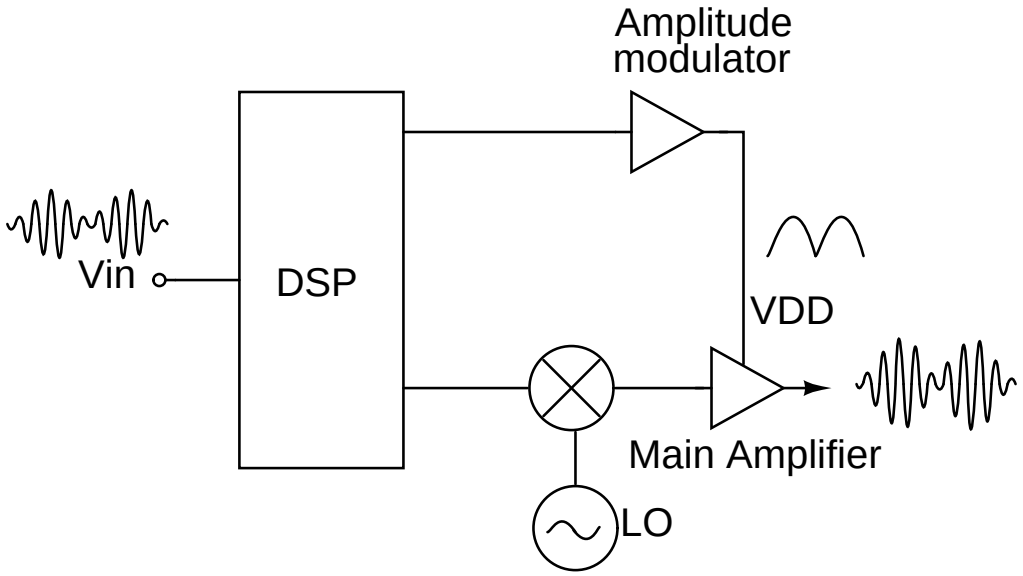

Figure 2.5 EER with digital generation of the PM and AM signals

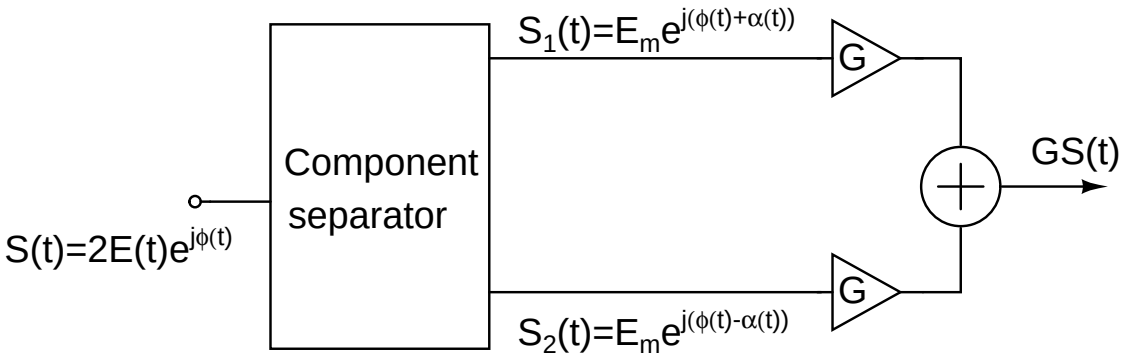

Figure 2.6 LINC amplifier system

kind of system is illustrated in Figure 2.5.

2.3.2 Linear Amplification with Nonlinear Components

Linear amplification with non-linear components (LINC), which is also known as Chireix outphasing, is based on the idea of separating the signal to be amplified in two constant amplitude signals, whose phases are modulated in such a way that their sum after amplification is the desired amplified signal. A block diagram of a LINC system is depicted in Figure 2.6.

The incoming signal ($S(t)$), which may be both amplitude and phase modulated, can be expressed as

$$S(t) = 2E(t)e^{j\phi(t)}, \tag{2.1}$$

where $E(t)$ represents the envelope of the signal. If we denote the maximum value of $E(t)$

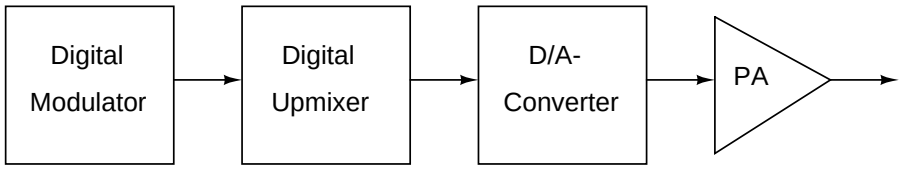

Figure 2.7 Direct Digital Conversion Architecture

as E_m, then the signal $S(t)$ can be separated into two constant envelope signals, $S_1(t)$ and $S_2(t)$, as follows [Cox 74, Zhang 01].

$$\begin{aligned} S_1(t) &= E_m e^{j(\phi(t)+\alpha(t))} \\ S_2(t) &= E_m e^{j(\phi(t)-\alpha(t))} \end{aligned} \tag{2.2}$$

where

$$\alpha(t) = \arccos\left(\frac{E(t)}{E_m}\right) \tag{2.3}$$

Both the constant envelope signals are then amplified with two nonlinear PAs with the same gain G, which yields:

$$G(S_1(t)+S_2(t)) = GS(t). \tag{2.4}$$

The resulting signal is a linearly amplified version of the incoming signal. The system has potential for higher efficiency than a system utilising a linear PA, since it employs high-efficiency non-linear amplifiers [Raab 85]. The system is vulnerable to the mismatch either in the phases of the branches or in the gains of the amplifiers, which cause distortion. In an endeavour to quit the phase mismatch problems, both analogue [Shi 00] and digital [Zhang 01, Zhang 00, Gerhard 05] component separators have been developed.

2.4 Direct Digital Conversion

In direct digital conversion, the baseband signal is generated with a digital modulator using a Direct Digital Frequency Synthesizer (DDFS). Then it is upconverted with a digital upmixer to radio frequency. The D/A conversion is performed at RF and the D/A converter is followed by a power amplifier. However, a multi-bit D/A converter is susceptible to glitches and spurious noise (as the output frequency increases), which is difficult to remove by filtering. Moreover parts of the digital circuitry are processing RF frequency signals, therefore their sampling frequency needs to be very high. This causes high power dissipation. Figure 2.7 illustrates the architecture.

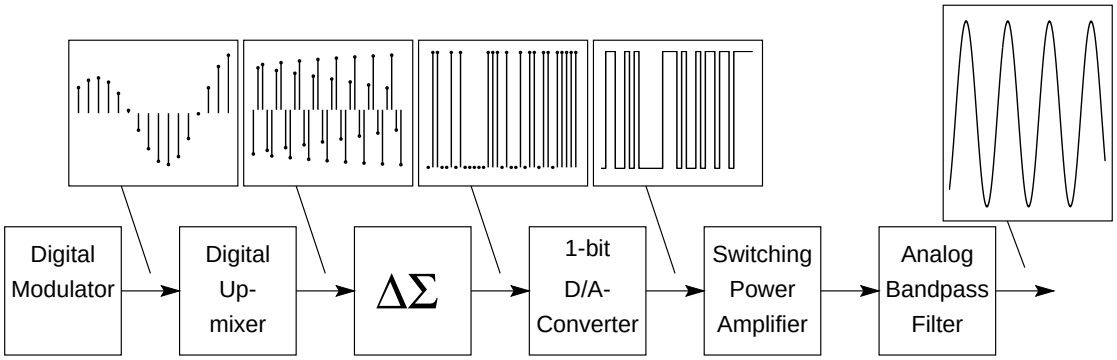

Figure 2.8 Block diagram of a digital upconversion chain using a Delta-Sigma DAC [Ketola 04]

2.5 Delta-Sigma Direct Digital Conversion

A transmitter architecture based on Delta-Sigma Direct Digital Conversion is similar to the aforementioned Direct Digital Conversion, but the multi-bit D/A converter is replaced with a 1-bit ΔΣ D/A converter, which, due to its noise shaping, is suitable only for relatively narrowband signals. However, in many wireless communication standards, the signal bands are relatively narrow compared to the RF carrier frequency and therefore the narrowband nature of the ΔΣ D/A converter does not impede its application in them.

The 1-bit ΔΣ D/A converter overcomes some of the problems related to the multi-bit D/A converter. Since the output of the 1-bit ΔΣ D/A only has two levels, any misplacement of the levels results only in gain error or offset. Neither of those is of great importance in many transmitter applications. The 1-bit ΔΣ D/A converter is an all-digital circuit, which has several advantages over analogue signal processing, such as flexibility, noise immunity, reliability and potential improvements in performance and power consumption, because of the scaling of the technology. In addition, the design, synthesis, layout and testing of digital systems can be highly automated [Lindeberg 05]. The combination of a Direct Digital Frequency Synthesizer (DDFS) with a 1-bit ΔΣ-D/A converter is attractive in digital transmitters, since it allows the power amplifier to be a switching-mode power amplifier, which may thus attain a high efficiency [Norsworthy 97].

2.6 Direct Digital RF Modulation

Direct Digital RF Modulation (DDRM) architecture is depicted in Figure 2.9. It is built around a Direct Digital RF Converter (DRFC) that combines the functionalities of a D/A converter and mixer [Eloranta 05]. The DRFC is based on a conversion cell of a current-steering D/A converter such that the current source and the current switches have been replaced with a mixer structure. The output currents from the conversion cells are summed at the output. The architecture is reminiscent of the Direct Conversion Transmitter of Section 2.1.1, but uses fewer analogue circuit blocks.

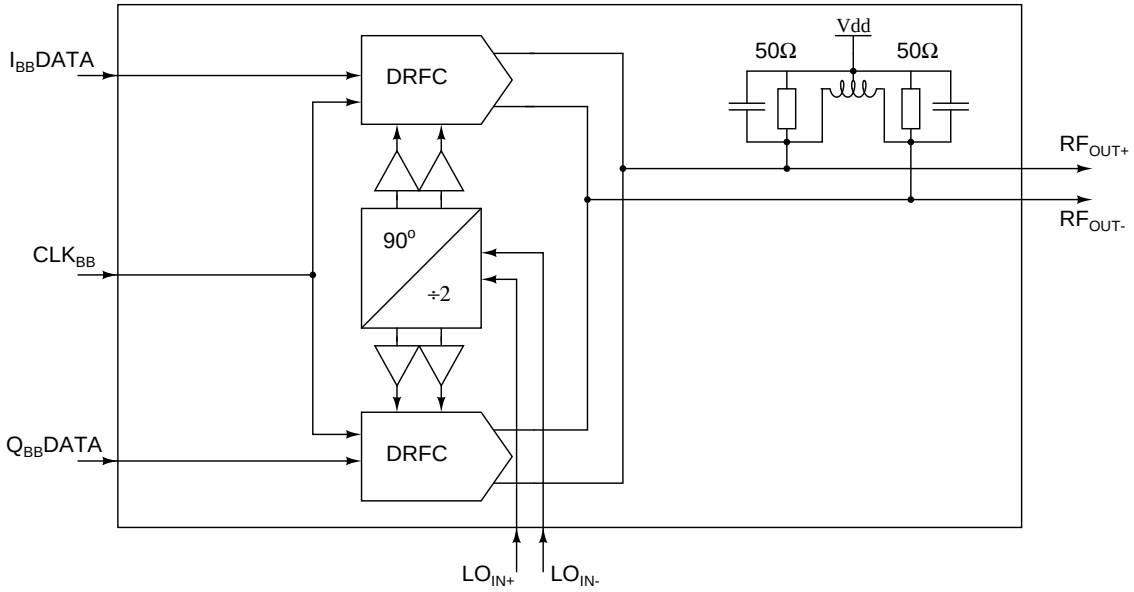

Figure 2.9 Direct Digital RF Modulator Architecture [Eloranta 05]

2.7 Transmitter architectures researched

The digital modulators presented in papers P1 and P2 have their output signals centered between (11 and 16.5) and 19.2 MHz respectively. Therefore they are meant for the two-step transmitter architecture presented in Subsection 2.1.2. The architecture-level novelty of paper P1 is the multicarrier modulator that combines the carriers in the digital domain, whilst paper P2 presents a novel multimode modulator with GSM, EDGE, and WCDMA realised with the same modulator circuitry.

Paper P4 presents an upconverter for the Digital/Analogue architecture described in Section 2.2. The concept would also be applicable for a direct digital conversion architecture (Section 2.4), either when the transmitted RF frequency is low enough or if the digital circuits and D/A converter could be operated at a higher frequency.

The architecture-level novelty of the implementation is the multiplier-free digital quadrature modulation at a quarter or half of the sampling frequency. The circuit was one of the first digital quadrature modulators operating at 500 MHz. In the state of the art found in the literature the implementation of paper P4 is best compared with the hybrid CORDIC-based implementations in [Wu 03] and [Caro 07] or the multiplier-free implementation based on circular shift registers in [Lin 97].

Paper P5 presents a digital quadrature modulator with a 1-bit bandpass $\Delta\Sigma$ D/A converter, which could be used as part of a Delta-Sigma direct digital conversion architecture as described in Section 2.5. However, as in Paper P4, the circuit implemented did not reach operation at a high enough RF frequency for GSM, EDGE, or WCDMA, although the concept worked at a sampling frequency of 700 MHz and a signal frequency of 175 MHz in the VHF band.

The novelty is the combination of a multiplier-free digital quadrature modulator with a bandpass Delta-Sigma D/A converter. Therefore it is best compared to the same state of the art as paper P4. A similar architecture with a multi-bit $\Delta\Sigma$ modulator is discussed in [Neitola 01].

Paper P6 presents a DDFS combined with a tunable $\Delta\Sigma$ D/A converter capable of phase, amplitude, and quadrature amplitude modulation, which could be used as part of a transmitter architecture such as the $\Delta\Sigma$ direct digital conversion architecture. The architecture is general-purpose in that it allows the IF to be selected freely within the Nyquist range. In the implemented circuit the maximum output frequency was 100 MHz, in the VHF band.

Papers P7-P9 present research on the switching mode power amplifier part of the Delta-Sigma direct digital conversion architecture described in Section 2.5. The architecture is best compared with those presented in the literature in [Jayaraman 98, Midya 02] and [Larson 05]. The state of the art is extended by simulations and measurements on topologies not found in prior art encountered in the literature. Experimental research on the transformer coupled voltage mode Class-D topology with $\Delta\Sigma$-modulated input is presented in paper P8 and research into the bandpass PWM-controlled Class-D power amplifier presented in [Midya 02] is extended to measurements in paper P9.

Chapter 3

Digital modulator architectures for wireless communication base station transmitters

In this chapter, the most prominent methods of digital modulation based on direct digital frequency synthesis are concisely reviewed. The perspective is that of a wireless communication base station transmitter. The two most important direct digital frequency synthesis methods are based on the use of a coordinate rotation digital computer (CORDIC) or look-up tables (LUT).

A direct digital frequency synthesizer is composed of a phase accumulator followed by a phase-to-amplitude converter, as illustrated in Figure 3.1.

3.1 Phase accumulator

An operational block diagram of phase accumulator is depicted in Figure 3.2. The phase accumulator calculates the phase of the sine wave to be generated by adding a phase increment to the phase in an accumulator each clock cycle. The rate of the overflows of the accumulator gives the output frequency

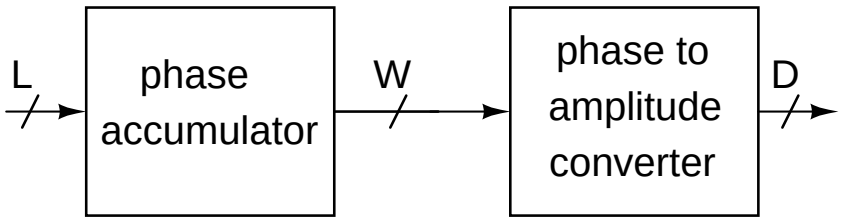

Figure 3.1 Direct digital frequency synthesizer

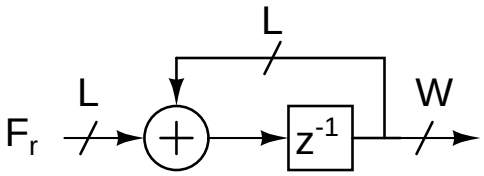

Figure 3.2 Phase accumulator

$$f_{out} = \frac{F_r}{2^L} f_{clk} \tag{3.1}$$

where F_r is the phase increment (which is also called *frequency control word*), L the phase accumulator word length and W the word length of the output of the phase accumulator, which is usually truncated. F_r is an integer, hence the frequency resolution is obtained by substituting $F_r = 1$:

$$\Delta f = \frac{f_{clk}}{2^L} \tag{3.2}$$

The maximum output frequency is limited by the sampling theorem to $f_{out} = f_{clk}/2$.

Phase truncation to W-bits causes spurs in the output spectrum of the DDS. The effects of the phase truncation have been analyzed in [Nicholas 87, Cheng 04]. Modified phase accumulator structures that reduce the worst-case spur levels exist [Nicholas 87].

3.2 CORDIC

The coordinate rotation digital computer (CORDIC) algorithm was introduced in [Volder 59]. It is a simple and efficient algorithm used to calculate hyperbolic, trigonometric and linear functions. CORDIC is based on the idea of decomposition of the desired rotation angle into the weighted sum of a set of predefined elementary rotation angles with the purpose of enabling the rotation without a multiplier, with shift and add operations [Hu 92b] and small LUT [Walther 71]. Therefore, it is found in applications such as simple microcontrollers and FPGAs. The algorithm is suitable for pipelining.

The tasks in the CORDIC algorithm are formulated as rotations of a 2×1 vector. The rotations can be performed in three different coordinate systems, i.e. hyperbolic, linear and circular coordinate systems, and can be used for the calculation of hyperbolic and trigonometric functions, amongst others.

There are two modes in which a CORDIC algorithm can be operated:

- *Rotation mode* [Valls 06, Timmermann 92], which has also been called *vector rotation mode,* [Hu 92b] or *forward rotation mode*. The desired rotation angle θ is given. The objective is to compute the final coordinate $[x_f\, y_f]^t$ [Hu 92b].

- *Vectoring mode* [Valls 06, Timmermann 92], which has also been called *angle accumulation mode* [Hu 92b] or *backward rotation mode.* The desired rotation angle

θ is not given. The objective is to rotate the given initial vector $[x(0)\,y(0)]^t$ to the x-axis so that the angle between them can be accrued [Hu 92b].

CORDIC in circular coordinate system

The circular variant is of interest in this chapter since it can be used for direct digital frequency synthesis [Kang 06, Yang 03, Kang 02]. Therefore rest of the section concentrates on it. The rotation angle θ is decomposed into the weighted sum of the elementary rotation angles as follows [Hu 92b].

$$\theta = \sum_{i=0}^{N-1} \mu_i a_i \tag{3.3}$$

where N is the number of elementary angles, $\mu_i \in -1,1$ is the rotation sequence and $a_i = \arctan(2^{-i})$ [Wu 01].

The inputs to the algorithm are x_0, y_0, z_0. The algorithm executes the following loop from $i = 0$ through N.

$$\begin{aligned} \begin{pmatrix} x_{i+1} \\ y_{i+1} \end{pmatrix} &= \begin{pmatrix} 1 & -\mu_i 2^{-i} \\ \mu_i 2^{-i} & 1 \end{pmatrix} \begin{pmatrix} x_i \\ y_i \end{pmatrix} = k_i \begin{pmatrix} \cos(a_i) & \mu_i \sin(a_i) \\ -\mu_i \sin(a_i) & \cos(a_i) \end{pmatrix} \begin{pmatrix} x_i \\ y_i \end{pmatrix}_i \\ z_{i+1} &= z_i - \mu_i a_i \end{aligned} \tag{3.4}$$

where μ_i =sign(z_i) in rotation mode (in vectoring mode μ_i =−sign($x_i y_i$)) and $a_i = \arctan 2^{-i}$, $i = 0, 1, 2, ..., N-1$ [Kang 06, Wu 01] and $k_i = \sqrt{1+2^{-2i}}$. The algorithm has a gain of $\prod_{i=0}^{N-1} k_i$. In order to maintain the norm the same as that of the input vector, scaling is needed:

$$\begin{pmatrix} x_f \\ y_f \end{pmatrix} = \frac{1}{\prod_{i=0}^{N-1} k_i} \begin{pmatrix} x_N \\ y_N \end{pmatrix} = \frac{1}{\prod_{i=0}^{N-1} \sqrt{1+2^{-2i}}} \begin{pmatrix} x_N \\ y_N \end{pmatrix} \tag{3.5}$$

where $[x_f\, y_f]^t$ is the final output vector and z_N is the output phase [Wu 01]. When the gain can be tolerated, the scaling can be omitted and $[x_N\, y_N]^t$ and z_N can be output instead. In a hardware realisation of the CORDIC algorithm, the loop is replaced by consecutive micro-rotation stages, each realising Equation (3.4). The quantization errors due to the finite word lengths of x_i, y_i and z_i and the number of iterations N determine the accuracy of the algorithm; the effect of these parameters have been studied in [Kota 93, Hu 92a, Vankka 00].

CORDIC can be used in polar-to-cartesian conversion [Gielis 91] for high-speed waveform synthesis. Here, its rotation mode is used in a circular coordinate system by setting $y_0 = 0$. CORDIC has also been used for cartesian-to-polar conversion, as in [Gerhard 05], where it operates as a LINC digital component separator in a WCDMA transmitter. Here

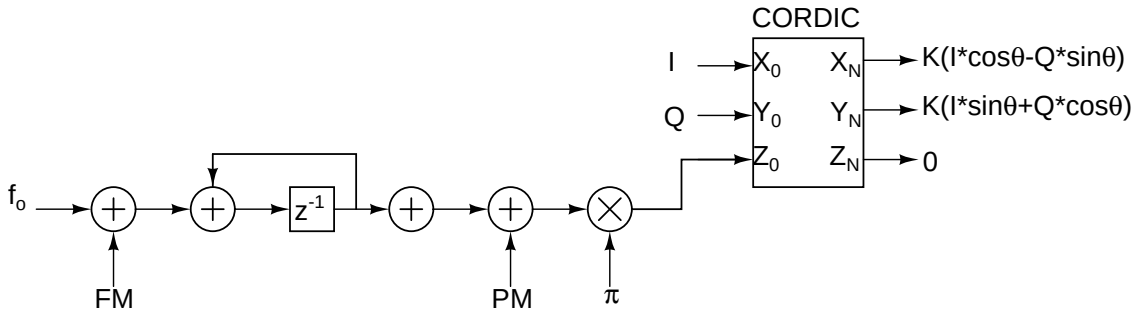

Figure 3.3 Rotation-mode CORDIC used for digital modulation [Valls 06]

the vectoring mode is employed in a circular coordinate system.

Rotation-mode CORDIC can be operated as a phase-to-amplitude converter of a direct digital frequency synthesizer (DDFS) [Kang 02]. The use of CORDIC as part of a direct digital synthesizer is explained in detail in [Valls 06]. A recent implementation of DDFS using differential CORDIC is reported in [Kang 06].

The rotation-mode CORDIC has also been used to perform quadrature modulation; e.g. in [Kosunen 01], it has been used in a QAM-modulator for a WCDMA base station and in [Vankka 02a] for a multimode base station. In both, the quadrature modulation has been accomplished by feeding the baseband I and Q data, as in Figure 3.3, and taking the quadrature modulated signal output from X_N.

Modified CORDIC algorithms

Latency time reduction and chip area savings have been sought in [Timmermann 89] by use of a modified CORDIC algorithm that employs multiplication and division operations in order to decrease the number of iterations. In [Wang 97], a hybrid CORDIC algorithm for rotation mode that replaces the least significant rotation angles with radix-2 coefficients is introduced.

Angle recoding is a modified CORDIC algorithm for vector rotation that is based on the idea of introducing a null rotation in the set of possible operations in the CORDIC iteration stages, i.e. $\mu_i \in -1, 0, 1$ in (3.4) [Hu 93, Wu 02]. This can be interpreted as adding flexibility to the conventional CORDIC algorithm with an intention of making it faster and more accurate. A similar approach is that of the modified vector rotational (MVR) CORDIC [Wu 01]. In Extended Elementary Angle Set (EEAS)-based CORDIC in addition to relaxed μ_i as above, the elementary angle set is extended [Wu 00].

A differential CORDIC algorithm utilizing redundant arithmetic [Dawid 96] has been used in [Kang 06] to realise a digit-pipelined DDFS where the phase-accumulator has been incorporated in the digit-level pipelining framework.

Hybrid LUT/CORDIC algorithms presented in [Janiszewski 01b,Janiszewski 01a,Janiszewski 04, Janiszewski 02] that combine the speed of LUTs and precision of CORDIC

have been developed for direct digital frequency synthesis applications, which are suitable especially when quadrature modulation is not needed.

Fine/coarse coordinate rotation

In fine/coarse coordinate rotation, the rotation is decomposed in three parts as follows [Song 04]:

$$\theta = \frac{\pi}{2}\kappa + \frac{\pi}{16}\gamma + \frac{\pi}{128}\eta + \delta \tag{3.6}$$

The components are called quadrant, coarse and fine rotation ($\frac{\pi}{128}\eta + \delta$), respectively. κ, γ and η are integers and γ,$\eta \in [0, 7]$. The quadrant rotation only needs interchange and/or negation operations. For the coarse rotation, the values of $\cos(\frac{\pi}{16}\gamma)$ and $\sin(\frac{\pi}{16}\gamma)$ are stored in LUT and for the fine rotation the $\cos(\frac{\pi}{128}\eta + \delta)$ and $\sin(\frac{\pi}{128}\eta + \delta)$ are calculated utilizing linear interpolation. The fine and coarse rotations are performed by complex multipliers. The fine/coarse approach results in a LUT size that increases polynomially with the resolution, whilst, in a pure LUT DDFS the dependence is exponential [Song 04]. This method has been used in [Torosyan 03, Song 04] for implementation of a Quadrature Direct Digital Synthesizer/Mixer with an output resolution of 13 and 15 bits and a sampling frequency of 300 and 330 MHz, respectively.

3.3 Direct Digital Synthesizer based on Look up Tables

In Direct Digital Frequency Synthesizers (DDFS) based on Look-up Tables (LUTs) the phase-to-amplitude converter of Figure 3.1 is realised with a random access memory (RAM), often mostly a read-only memory (ROM), since, in most DDFSs found in the literature, no remapping of the phase-to-amplitude characteristic have been needed as in [Gotoh 94, Prasad 06].

3.3.1 Sine memory compression

The most elementary technique of sine memory compression is to utilise the quarter wave symmetry of the sine function for memory compression and store only one quarter of the full period of the sine function in the memory and generate the rest from it as presented in Figure 3.4.

Further methods of compressing the quarter wave memory can be divided into three categories, angular decomposition, amplitude compression and interpolation, which, in turn, can be categorized by the order of the approximation polynomial.

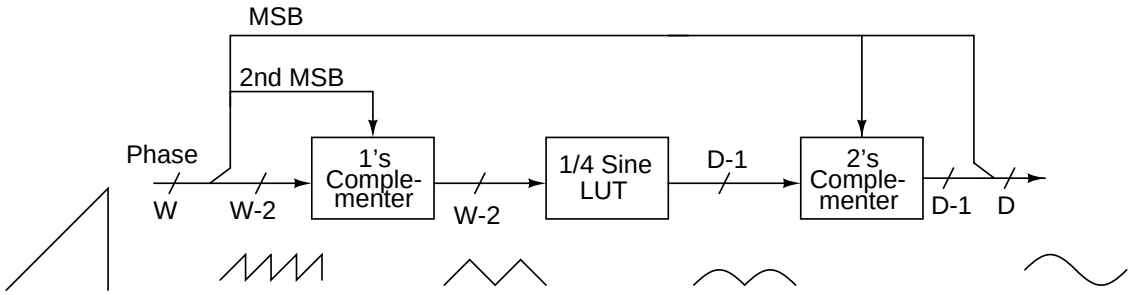

Figure 3.4 Sine memory compression by quarter wave symmetry

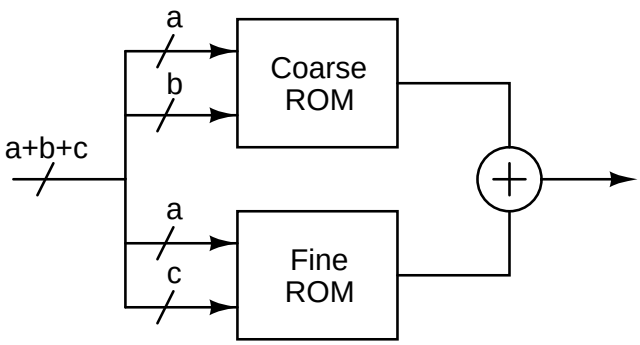

Figure 3.5 Sunderland architecture

Compression by angular decomposition

The compression of quarter sine memory through angular decomposition is based on the idea of splitting the phase into smaller fractions and using these fractions to address two or more smaller LUTs, such that the total amount of LUT memory is decreased.

Sunderland architecture [Sunderland 84] (illustrated in Figure 3.5) is based on splitting the argument of sine function into three fractions: $\phi = \alpha + \beta + \gamma$, where the word lengths of the terms are *a*, *b* and *c*, respectively. α, β and γ are such that [Sunderland 84, Goldberg 96].

$$\alpha < \frac{\pi}{2}\,,\ \beta < \frac{\pi}{2}2^{-a}\,,\ \gamma < \frac{\pi}{2}2^{-(a+b)}. \tag{3.7}$$

Thus, using trigonometric identities, we have

$$\sin(\alpha+\beta+\gamma) = \sin(\alpha+\beta)\cos(\gamma) + \cos(\alpha)\cos(\beta)\sin(\gamma) - \sin(\alpha)\sin(\beta)\sin(\gamma) \tag{3.8}$$

This can be approximated as

$$\sin(\alpha+\beta+\gamma) \approx \sin(\alpha+\beta) + \cos(\alpha)\sin(\gamma) \tag{3.9}$$

The values of the first term of (3.9) are stored in the coarse ROM and the values of

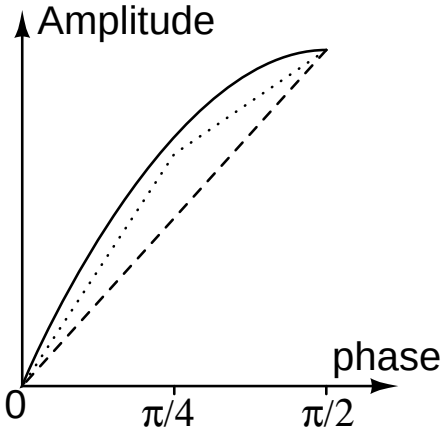

Figure 3.6 Trigonometric approximations: sine-phase difference (dashed) and double trigonometric (dotted)

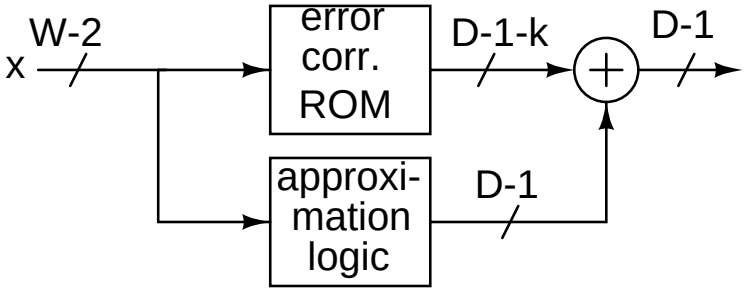

Figure 3.7 Amplitude compression circuit for memory compression in DDFS [Langlois 01]

the second term are stored in the fine ROM. A similar technique is presented in [Curticapean 01].

An improvement to the Sunderland method is to calculate the values of coarse and fine ROM such that either the mean square error (MSE) or the maximum error is minimized [Nicholas 88, Tang 02].

Amplitude compression

The amplitude compression techniques for sine memory exploit the redundancy between the value of the phase angle and the corresponding sine amplitude [Langlois 01]. The sine-phase difference algorithm is the simplest of these techniques. It approximates the sine function as a straight line, as shown in Figure 3.6. Only the approximation error is stored in a LUT. A generic block diagram of the amplitude compression method is shown in Figure 3.7. The double trigonometric approximation architecture [Yamagishi 98] combines the sine-phase difference algorithm with the subtraction of another triangular waveform, as shown in Figure 3.7. The implementation of this algorithm requires an additional complementer as additional logic hardware. More sophisticated amplitude compression methods have been presented in [Kim 03, Langlois 01, Yang 04], and [Sodagar 00]. The

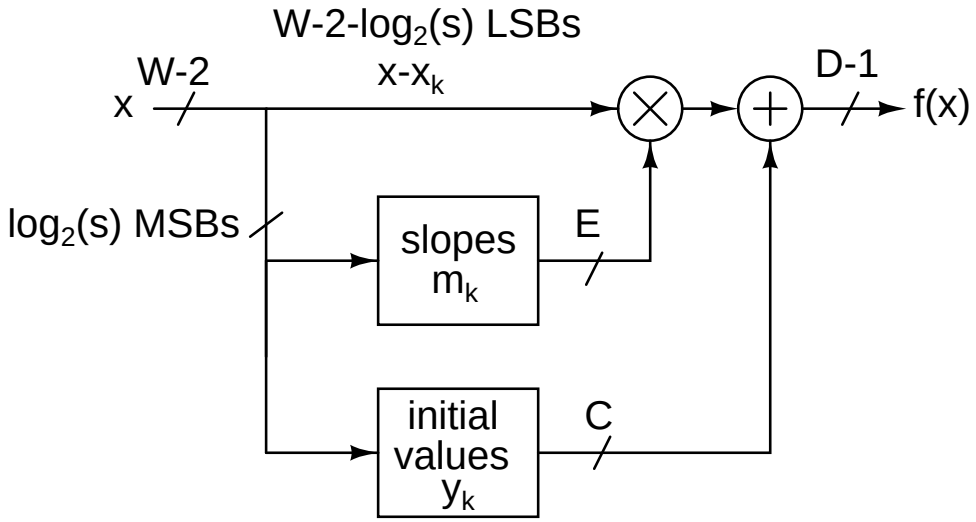

Figure 3.8 Linear interpolation [Langlois 03b]

latter approximates the sine function with a parabolic function, therefore the implementation requires a multiplier. Second-order polynomial approximation with fixed coefficients utilizing canonic signed digit (CSD) hyperfolding has been presented in [Caro 04].

Linear interpolation

In a DDFS based on linear interpolation, the first quadrant of the sine function is divided into segments that are approximated with a piecewise linear function $f(x)$ in (3.10) [Langlois 03a, Langlois 03b, Bellaouar 00]

$$f(x) = y_k + m_k(x - x_k), \text{ for } x \in [x_k, x_{k+1}), \text{ for all } k \in \mathbb{Z},\ 0 \leq k \leq s-1, x_0 = 0, x_s = 1, \tag{3.10}$$

where s is the number of segments and m_k and y_k are the slope and initial amplitude of each segment, respectively. The values of m_k and y_k are stored in LUTs. Figure 3.8 shows a block diagram of an implementation of a quadrant phase to amplitude converter of a DDFS based on linear interpolation. It needs two smaller LUTs and a multiplier to replace the 1/4 sine LUT of a pure LUT-based DDFS, as shown in Figure 3.4.

The dual slope approach [Strollo 03, Strollo 04] is a variation of the linear interpolation concept in that, instead of one slope per segment it utilizes two slopes per segment. Linear and nonlinear addressing schemes for the LUTs in a linear interpolation DDFS have been studied and implemented in [Chimakurthy 06].

Second-order polynomial interpolation

In a DDFS based on second-order polynomial interpolation. the first quadrant of the sine function is divided into segments that are approximated with a piecewise polynomial

function $f(x)$ of second order as follows:

$$f(x) = y_k + m_k(x - x_k) - p_k(x - x_k)^2 \tag{3.11}$$

where the interpolation coefficients: y_k,m_k,p_k are stored in LUTs. The implementation requires 2 multipliers. The compression method is also called *parabolic interpolation* [Fanucci 01] or *piecewise polynomial approximation* [Caro 05].

Quasi-linear interpolation [Ashrafi 05] is a hybrid between linear and second-order polynomial interpolation using parabolic interpolation for the more curved part and linear interpolation for the more linear part of the quadrant.

Other variations of the concept involve multi-stage linear interpolation [Hikawa 04] and piecewise parabolic interpolation using a Farrow structure [Eltawil 02b, Eltawil 02a].

Conclusion of compression methods

The sine memory compression methods trade computational complexity for memory. The key is to find a balance between performance in terms of SFDR and area and power consumption [Langlois 03a]. A study of this balance for an FPGA realisation is presented in [Cardells-Tormo 03]. The different methods of memory compression can be combined in order to find a balance for design as has been done in [Yang 04], which uses a quad-line approximation method for amplitude compression and Sunderland architecture for angle decomposition with fine and coarse ROMs and quantization and error ROM technique for additional ROM compression [Yang 04]. Comparisons of the compression ratios, SFDRs, memory sizes etc. of different compression methods have been reported in, for example, [Vankka 00, Yang 04, Kim 03, Chimakurthy 06, Langlois 03a] and [Said 03].

Finite Word Length Effects in LUT based DDFSs

The phase-to-amplitude converter introduces two different types of errors to the signal: the error due to memory compression nonlinearity and the error due to the amplitude quantization of the sine samples [Nicholas 88]. The deterioration of the SFDR of the signal caused by these errors has been studied in, for example, [Nicholas 88, Cheng 04, Vankka 00].

3.4 Conclusion and implemented DDFSs

Direct Digital Frequency Synthesizers can be realised using a variety of methods and architectures that can be divided into two categories, i.e. CORDIC based and LUT based. The computational complexity of CORDIC involves higher circuit complexity compared to a pure LUT-based DDFS with no computational complexity and high requirement of

memory. Between these two extremes, there is a trade-off with multiple solutions of CORDIC that utilize LUTs and LUT-based DDFSs that utilize adders and multipliers to save memory. One prominent difference between CORDIC and LUT-based DDFS is, however, found in their application in QAM modulation, where an LUT-based DDFS requires 2 multipliers [Vankka 01] and complex QAM 4 multipliers [Valls 06], but no multipliers are needed in CORDIC-based implementation [Valls 06]. However, CORDIC requires higher datapath precision than LUT, in order to attain the same spectral purity [Song 04]. CORDIC and LUT-based DDFSs have been further compared in [Janiszewski 02]. Table 3.1 compares various implemented DDFSs.

3.4.1 Implemented DDFSs

Papers P1 and P6 present LUT-based DDFS designs. The DDFS in paper P6 employs second-order polynomial interpolation for sine memory compression, achieving an SFDR of 87.09 dBc with an f_{clk} of 200 MHz. The total ROM size was 1600 bits, resulting in a high compression ratio of 123. The phase resolution (W) 14 and the output resolution (D) of the DDFS was 12. The chip was fabricated on a CMOS technology of 0.13 μm with a total chip area of 2.02 mm^2.

The DDFS in paper P1 employs an angular decomposition method for sine memory compression called the modified Nicholas architecture, attaining an SFDR of 87 dBc with an f_{clk} of 52 MHz. The phase resolution (W) was 14 and the output resolution (D) of the DDFS was 12. The total ROM size was 3840 bits, resulting in a compression ratio of 51:1. The chip was fabricated on a BiCMOS technology of 0.35 μm. The paper demonstrates the use of LUT-based DDFS for a multicarrier modulator architecture.

Paper P2 presents a CORDIC-based DDFS design. The resolution of the CORDIC is 18 bits, attaining an SFDR of 90 dBc with an f_{clk} of 76.8 MHz. The paper demonstrates the use of CORDIC for the realisation of a multimode GSM/EDGE/WCDMA modulator. The implementation was the first published multimode GSM/EDGE/WCDMA modulator with an on-chip D/A converter.

Paper P1 introduces a novel digital power ramping and control unit based on a recursive digital sinusoidal oscillator and an enhanced version with more configurability is presented in paper P2. Conventionally, LUT- or FIR-based units were used.

Table 3.1 Comparison of implemented DDFSs .

Ref.	Type	ROM size	comp. ratio	SFDR dBc	Area mm^2	f_{clk} MHz	resol. W,D	Tech μm	com-ments
[Caro 05]	Polyn. Interp.	-	-	84	0.05	526	15 12	0.25	IQ
[Sunderland 84]	Angular decomp.	3840	51.2	65	48	7.5	14 12	3.5	DAC
[Langlois 03a]	Linear interp.	448	402:1	84	0.28	320	16 11	0.35	
[Yang 04]	Amplit. compr.	368	200:1	55	1.47	800	32 9	0.35	DAC
[Caro 04]	Amplit. compr.	0	0	80	0.22	98	14 12	0.35	IQ
[Strollo 04]	Linear interp.	-	-	80	0.09	600	24 12	0.25	IQ
[Curticapean 01]	Angular decomp.	576	455:1	96	0.23	100	16 16	0.35	IQ 2 mults
[Tang 02]	Angular decomp.	3840	51:1	83	2	200	14 12	0.35	IQ mixer
[Nicholas 91]	Angular decomp.	3072	128:1	90	24	100	15 12	1.25	
[Chimakurthy 06]	Interp.	1216	404:1	90	-	25	15 15	FPGA	
[Song 04]	CORDIC fine/coarse	-	-	100	0.51	330	18 15	0.25	IQ mixer
[Torosyan 03]	CORDIC fine/coarse	442	-	90	0.36	300	15 13	0.25	IQ mixer
[Gielis 91]	CORDIC	-	-	60	25	540	12 10	1	IQ mixer
Paper P1	Angular decomp.	3840	51:1	87		52	14 12	0.35	
Paper P2	CORDIC			90		76.8	18 18	0.35	IQ
Paper P6	Interp.	1600	123:1	87	2.02	200	14 12	0.13	

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Chapter 4

Digital/Analogue Conversion in base station transmitters

As expressed in the chapter that discusses the transmitter and upconversion architectures, the final output signal from the antenna is analogue, whilst, at baseband, digital signal processing is utilised. Thus, conversion from digital to analogue is needed at some point of the transmitter chain. There is a wide range of alternative D/A conversion architectures available for this purpose, and they can be divided into three subcategories: Nyquist rate D/A converters, oversampling D/A converters and undersampling D/A converters.

4.1 Performance metrics of D/A converters

The most important performance metrics for D/A converters in wireless communications transmitters can be divided into two classes: static metrics and dynamic metrics. The most important static metrics are differential nonlinearity (DNL) [Razavi 95] and integral nonlinearity (INL) [Razavi 95].

The most important dynamic metrics are signal-to-noise ratio (SNR) [Andersson 05], signal-to-noise-and-distortion ratio (SNDR) [Andersson 05], spurious-free dynamic range (SFDR) [Andersson 05] , effective number of bits (ENOB) [Andersson 05] and multi-tone power ratio (MTPR) [Andersson 05].

4.2 Nyquist rate D/A converters

A Nyquist rate D/A converter samples the input data with a rate that is slightly higher than twice the bandwidth, as required by the sampling theorem [Shannon 49]. The most important Nyquist rate D/A converter architectures are current-steering, charge-redistribution, R-2R ladder and resistor-string D/A converters. Out of these only current-steering has been found suitable for the transmitter applications.

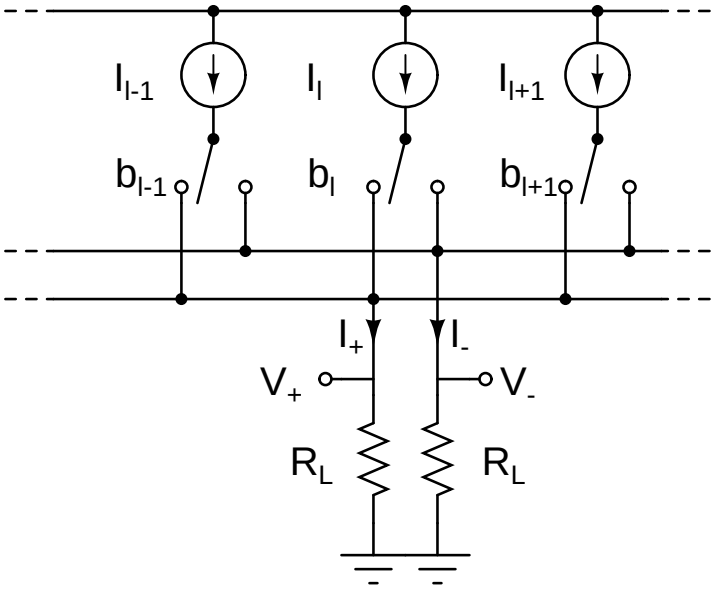

Figure 4.1 Current-steering D/A converter [Andersson 05]

4.2.1 Current-steering D/A converters

A current-steering D/A converter is based on switched current technique. Figure 4.1 depicts the structure of a differential current-steering D/A converter. It is composed of weighted current sources, switches and two load resistors.

The weighted currents are summed in the outputs. Depending on the control bits b_l, the current I_l is steered either in the positive or negative load resistor. So the output currents are [Andersson 05]

$$I_+ = \sum_l b_l I_l$$

$$I_- = \sum_l \overline{b_l} I_l.$$

The currents I_l may or may not vary, depending on the weighting scheme employed. In general, the weighting of the current sources can be expressed as follows

$$I_l = w_l I_{unit}.$$

The most common current steering D/A converter architectures are binary, thermometer (also called unary [van den Bosch 01a]) and segmented. In a binary weighting

$$w_l = 2^l,$$

whilst in a thermometer-coded architecture, the weights are

$$w_l = 1.$$

Segmented architecture is a hybrid of the above, i.e. some of the current sources are binary weighted, while the others are thermometer-coded.

The binary weighted architecture is more vulnerable to glitches than the thermometer-coded architecture, because a small change in the value of the input signal can trigger a state transition in many (or all in the worst case) of the binary weighted bits. For example, a transition from '100000' to '011111' can cause a glitch if the MSB transition is slower than the LSB transitions [Kosunen 06]. In a segmented architecture, the glitches due to the use of a binary weighted LSB end are small, therefore is common that the MSB bits are thermometer coded and the LSB bits are binary weighted [Razavi 95].

Static performance limitations

Static non-linearities that deteriorate INL and DNL emanate from two categories of non-idealities: random process variations and gradient process variations.

To enable the prediction of INL variation due to the random variation, the concept of INL yield has been defined as the percentage of the functional D/A converters with an INL specification of less than half an LSB [van den Bosch 01b]. This parameter has the following relationship with the relative unit current source standard variation $\sigma(I)/I$ and DAC resolution N [van den Bosch 01b, van den Bosch 01a].

$$\frac{\sigma(I)}{I} = \frac{1}{2C\sqrt{2^N}} \text{ with } C = \text{inv\_norm}(0.5 + \frac{\text{yield}}{2}) \tag{4.1}$$

where inv_norm stands for inverse cumulative normal distribution. Based on (4.1) and the relation between the size and matching of MOS transistors [Pelgrom 89], the dimensions of the current sources can be calculated in the case of MOS current sources [van den Bosch 01c]:

$$WL = \frac{1}{2\left(\frac{\sigma_I}{I}\right)^2}\left[A_\beta^2 + \frac{4A_{VT}^2}{(V_{GS}-V_T)^2}\right] \tag{4.2}$$

where A_β and A_{VT} are technological parameters and $(V_{GS}-V_T)$ is the gate overdrive voltage of the current source transistors. This relationship between mismatch and area imposes a minimum constraint on the area of the D/A converter, depending on the resolution.

Gradient variations mainly emanate from the variation of the oxide thickness on the wafer and die stress gradients. There are layout design techniques the purpose of which is to mitigate the effects of gradient process variations that result in static nonlinearity. Two categories of these techniques can be identified as heuristic [Bastos 98, Deveugele 04] and analytic [van der Plas 99, Cong 00] methods that require a priori cognizance of the gradients [Kosunen 06].

Loss of resolution emanating from matching errors such as gradient and random errors can be compensated for using calibration techniques, two main categories of which can

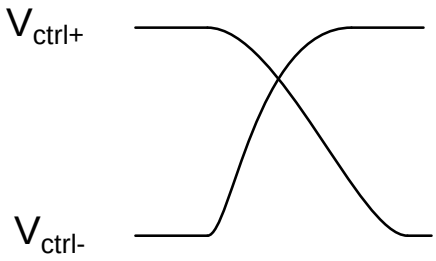

Figure 4.2 Switch control signal intersection point

be identified as [Kosunen 06] continuous [Groeneveld 89] and quantized [Manoli 89, Cong 03, Schofield 03, Tiilikainen 01].

Another way to tackle the problem is to use dynamic element matching (DEM) to convert spurious tones caused by matching errors into white or shaped noise [Andersson 05, O'Sullivan 04].

Dynamic performance limitations

The dynamic performance of a current-steering D/A converter is principally limited by the imperfect synchronization of the control signals of the switches, drain voltage variation of the current-source transistors and feedthrough of the control signals to the output of the switches [van den Bosch 01a].

These problems can be minimized by using differential signals and careful design of the driving circuitry of the current switches. The switch control signal intersection point (Figure 4.2) must be such that the switches are never simultaneously off; attention must therefore be paid to the correct timing of the signals [van den Bosch 01a]. The feedthrough problem can be decreased by lowering the switch driving signal voltage range [van den Bosch 01a] or by using dummy switches [Teikari 02].

Time-interleaved current-steering structures

Time-interleaved current-steering D/A converter structures have been published where the performance of the D/A converter is increased by multiplexing parallel time-interleaved sub-D/A converters that are operated at the sampling rate divided by the number of sub-DACs [Yang 01, Vankka 02b], as illustrated in Figure 4.3. The structure increases the area of the DAC in proportion to the number of sub-DACs. At high frequencies, jitter can adversely impact the performance of the converter [Yang 01].

Time-interleaved structures have also been applied to L-fold linear interpolation D/A conversion [Zhou 03], where the time-interleaved structure is created by dividing the main clock into sub-clocks using delay-elements, as shown in Figure 4.4. Using sub-clocks, linear interpolation of the output samples is approximated by an L-fold linear interpolation where the output rises to the next sample value in L steps, as illustrated in

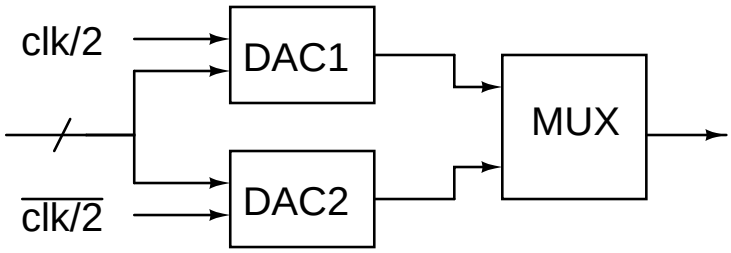

Figure 4.3 Time-interleaved DAC

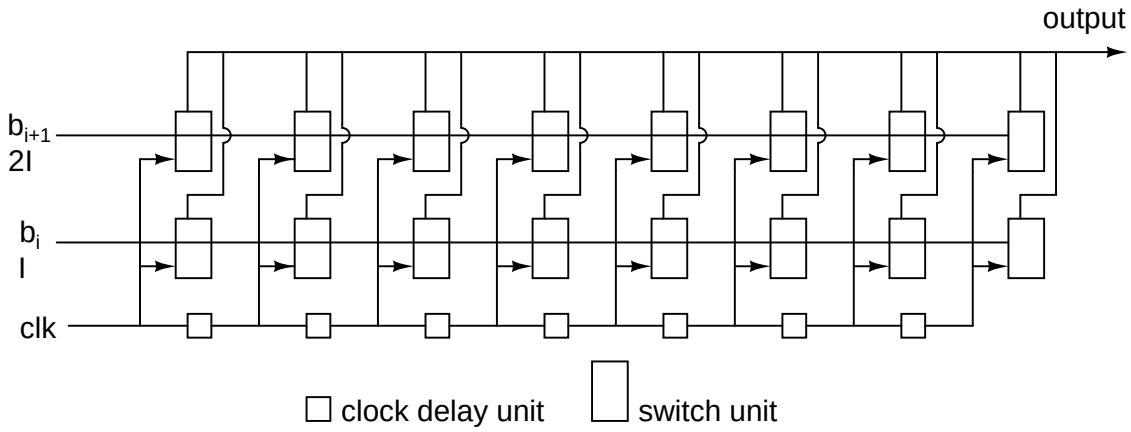

Figure 4.4 Time-interleaved L-fold interpolation current-steering structure

Figure 4.5, which compares the desired signal with the usual zero-order hold DAC output signal, linear interpolation DAC output signal and L-fold linear interpolation DAC output signal. The advantage of L-fold linear interpolation over a zero-order hold type DAC is that its frequency response has the images attenuated approximately by the square of the sinc function [Zhou 03], thus easing the requirements on the reconstruction filter.

4.2.2 Survey of published current-steering converters

This subsection summarizes some recent current-steering D/A converters that fit the field of focus of this thesis as far as the resolution and sampling frequency are concerned, i.e. a sampling frequency range from 100 MHz to 1 GHz and resolution from 10 to 16 bits. Table 4.1 encapsulates the quoted resolution, sampling rate, die area, power dissipation and SFDR of the published D/A converters.

4.2.3 Implemented D/A converter

The D/A converter presented in papers P2 and P3 represented the state of the art of current-steering Nyquist rate D/A converters; we achieved an SFDR of 68 dB at a frequency of 30 MHz and at a sampling frequency of 76.8 MHz, a resolution of 14 bits; the die area was 3.45 mm^2 . The power dissipation was 52 mW with a sampling frequency

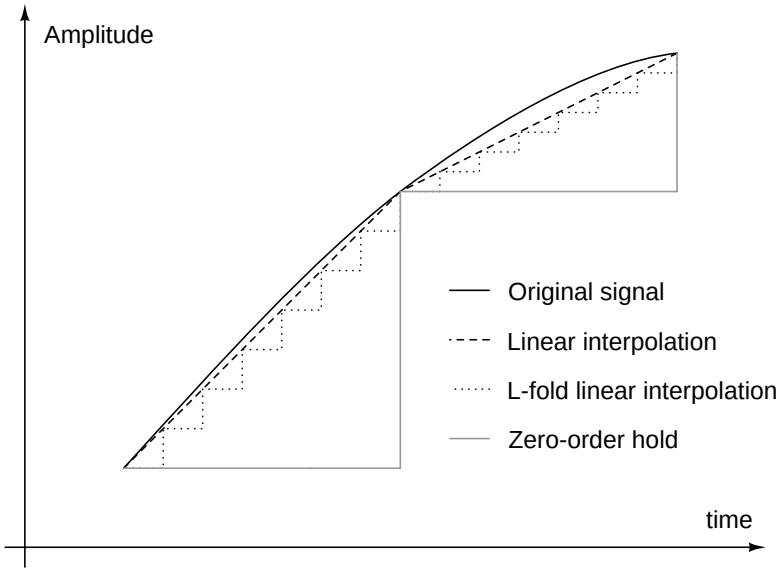

Figure 4.5 Time domain DAC responses of zero-order-hold, linear interpolation and L-fold linear interpolation [Zhou 03]

Table 4.1 Summary of published D/A converters

Publication	resolution bits	sampling rate (MHz)	die area (mm^2)	power dissipation (mW)	SFDR (dBc @ MHz)
[van den Bosch 01a]	10	1000	0.35	110	61 @ 490
[van den Bosch 98]	12	200		140	65 @ 1
[Baek 03]	12	1000		950	72 @ 1.8
[Tesch 97]	14	100	16.7	650	87 @ 10
[Manganaro 04]	10	200	2.28	694	70 @ 34
[Ueno 05]	12	200	0.75		55 @ 60
[Albiol 03]	12	400			40 @ 53
[O'Sullivan 04]	12	320	0.44	82	60 @ 60
[Hwang 04]	10	500		45	65 @ 8
[Yoo 02]	10	300	1.56	84	59 @ 3
Paper P3	14	110	3.45	52	68 @ 30

of 100 MHz. As can be seen from Table 4.1, the faster D/A converters generally have a lower resolution than the one in papers P2 and P3.

A novelty of the D/A converter was integrating it on the same chip as a multi-mode GSM/EDGE/WCDMA modulator. This provided a design challenge, as the digital part would cause noise and disturbances. The permeation of these to the D/A converter was impeded by carefully designing the layout and placing a deep-n-well under the D/A-converter.

Segmented architecture was used for the current sources. The segmentation ratio was optimized for area and SFDR, resulting in 4 MSBs thermometer-coded and 10 LSBs binary-coded. A 4¡ LSB digital calibration system was designed to cancel the mismatch between the differently sized MSB and LSB unit current sources.

Cascode transistors were used to increase the output impedance of the current cells. Moreover, the effect of the cascode transistors in the output lines was studied experimentally and was found to have a relatively small effect on SFDR.

The switch driver was designed for high dynamic performance. Here the amplitude and timing of the switch control signal were optimized.

The D/A converter had separate supply voltages from the digital part in order to impede crosstalk and the voltage supply lines were wide in order to decrease their resistance, which could cause code-dependent fluctuation in the supply voltage and hence cause the SFDR performance to deteriorate.

4.3 Oversampling D/A converters

An oversampling D/A converter employs interpolation to attain a higher oversampling ratio (OSR).

$$\mathrm{OSR} = f_s/2\mathrm{B}, \tag{4.3}$$

where B is the bandwidth of the signal and f_s is the sampling frequency. The use of oversampling eases the requirements for the reconstruction filter.

This thesis concentrates on oversampling noise-shaping D/A converters that, in addition to the interpolation, utilize quantization and noise shaping. In particular, the focus lies on ΔΣ-D/A converters. The motivation for using a ΔΣ-D/A converter is to make higher accuracy and linearity feasible than those achieved by Nyquist rate D/A converters. By oversampling and noise shaping the need for expensive trimming or long conversion time, typical of high-accuracy Nyquist rate converters, can be circumvented and robust and simple analogue circuitry can be used.

The idea and purpose of quantization is to process input data such that a lower number of bits can be used in the presentation of the signal in the digital parts of the D/A converter. This idea is used in conjunction with a noise-shaping technique that moves

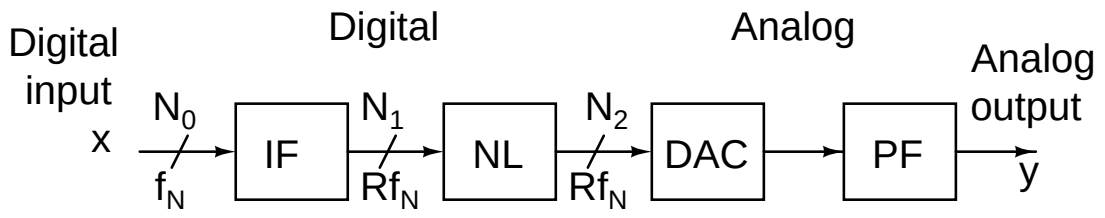

Figure 4.6 Block diagram of an oversampling interpolating DAC with noise-shaping

quantization noise arising from the lowering of the number of bits outside the signal band, from there it is filtered out to form the final output of the D/A converter. Figure 4.6 depicts a generic block diagram of an oversampling interpolating D/A converter with noise shaping. The input x is an N_0-bit digital signal with a data rate f_N; the interpolation filter (IF) changes the sample rate to RF_N and suppresses the spectral replicas at f_N,$2f_N$..., $(R-1)f_N$ [Norsworthy 97]. The N_1-bit signal from the interpolation filter is fed to the noise-shaping loop (NL) block (for instance a $\Delta\Sigma$-modulator) that involves quantization to a drastically smaller number of bits N_2. The N_2-bit signal is D/A converted and filtered with an analogue post-filter (PF).

4.3.1 Interpolation

Common to all types of oversampling D/A converters is the presence of interpolation, i.e. the process of adding samples. An interpolation by an integer factor of L means adding $L-1$ zeros after each sample and filtering out the appearing images from the spectrum with an appropriate filter while increasing the sampling rate by a factor of L. Only together with interpolation is it possible to decrease the number of bits by quantization without losing resolution.

The interpolator can comprise one or more stages. A multi-stage interpolator is usually preferred to a single-stage interpolator in applications with high sampling rates, due to the fact that the multi-stage interpolation enables the use of high-efficiency filter structures, such as half-band filters that are suitable for stages with interpolation ratios of 2, ternary-encoded FIR filters and sinc^K filters. The two latter obviate the need of multipliers [Norsworthy 97].

4.3.2 $\Delta\Sigma$ D/A converters

Quantizer

In a $\Delta\Sigma$ D/A converter, the number of bits used in the representation of the signal in the internal digital parts is decreased by the quantizer. A $\Delta\Sigma$ D/A converter employing a single-bit quantizer gives a 1-bit output, hence it only needs to be followed by a post-filter. However, a $\Delta\Sigma$ D/A converter employing a multi-bit quantizer needs to be followed

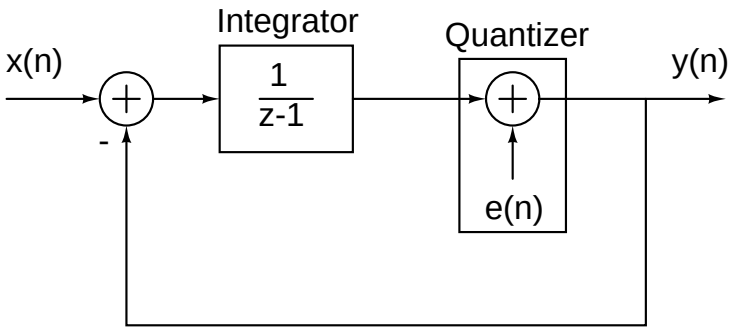

Figure 4.7 A first order ΔΣ-modulator

by another D/A converter with a number of bits equal to that of the quantizer.

Quantization is a highly non-linear operation, but a quantizer can be modelled by linear model that comprises the addition of an error signal $e(n)$.

$$y(n) = Gx(n) + e(n), \tag{4.4}$$

where $x(n)$ is the incoming signal to the quantizer, G is the gain of the quantizer and $y(n)$ is the output [Norsworthy 97]. In a 1-bit or two-level quantizer, G is arbitrary and a ΔΣ-DAC with such a quantizer has zero INL and DNL [Andersson 05].

The addition of the error signal can be interpreted as the introduction of noise to the signal by the quantizer. $e(n)$ is fully dependent of the input, but under the condition that the y changes from sample to sample sufficiently, to enable its position within the quantization interval to be random, whilst not over-loading, it can be justified to assume that e is white noise [Schreier 05].

Noise Shaping Loop

Since the error $e(n)$ is only dependent of the input to the quantizer it is possible to design a noise transfer function for the quantization noise such that it is attenuated inside the signal band and amplified outside it. This is what is done in ΔΣ-D/A converters with a ΔΣ-modulator. Figure 4.7 shows a model of a first order ΔΣ-modulator, which consists of an integrator, a quantizer and a feedback loop.

The operation of the ΔΣ-modulator can be described in z-domain as

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})E(z) \tag{4.5}$$

In the equation the noise transfer function (NTF) is $(1 - z^{-1})$ and the signal transfer function (STF) is z^{-1}. It can be seen that the NTF is a high pass function that indeed attenuates the quantization noise at low frequencies and amplifies it at high frequencies and that the signal transfer function is an all-pass function.

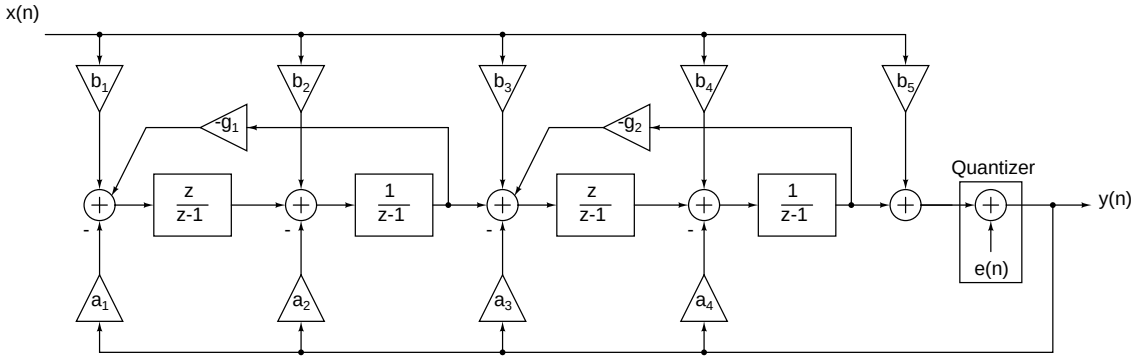

Figure 4.8 Cascade of resonators with distributed feedback and input (CRFB) structure [Schreier 05]

Various noise-shaping loop architectures can be, and have been, used in the implementation of $\Delta\Sigma$ D/A converters, such as single-stage loops, error-feedback structures and cascade or multi-stage noise shaping (MASH) structures [Schreier 05].

Single-stage loops

Several different architectures for realizing the desired NTF using a single stage are available in the literature. Degrees of freedom in the design of the NTF are provided by the number and location of poles and zeros. The number of poles defines the order of the NTF and equals the number of zeros. The placement of the zeros can be optimized for the NTF attenuation on the signal band [Schreier 05], whilst the placement of the poles can be optimized for stability, taking account of the realizability considerations [Schreier 05].

Typical higher-order single-stage architectures are cascade of integrators feedback form (CIFB), cascade of resonators feedback form (CRFB), cascade of integrators feedforward form (CIFF), cascade of resonators feedforward form (CRFF) [Schreier 05]. Design methodology for the implementation of these are available in literature such as [Schreier 05].

Error feedback structure

The noise-shaping technique was first introduced with an error feedback structure in [III 62]. Figure 4.9 shows a block diagram of the error feedback structure. Its operation can be characterized by Equation 4.6, where NTF is $(1-H_e)$ and STF is 1. Similar criteria can be used in the design of the NTF as above [Schreier 05].

$$Y(z) = X(z) + (1 - H_e(z))E(z) \tag{4.6}$$

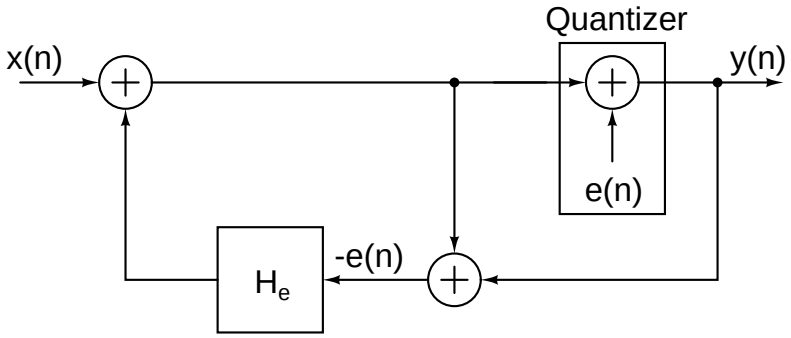

Figure 4.9 Error feedback structure

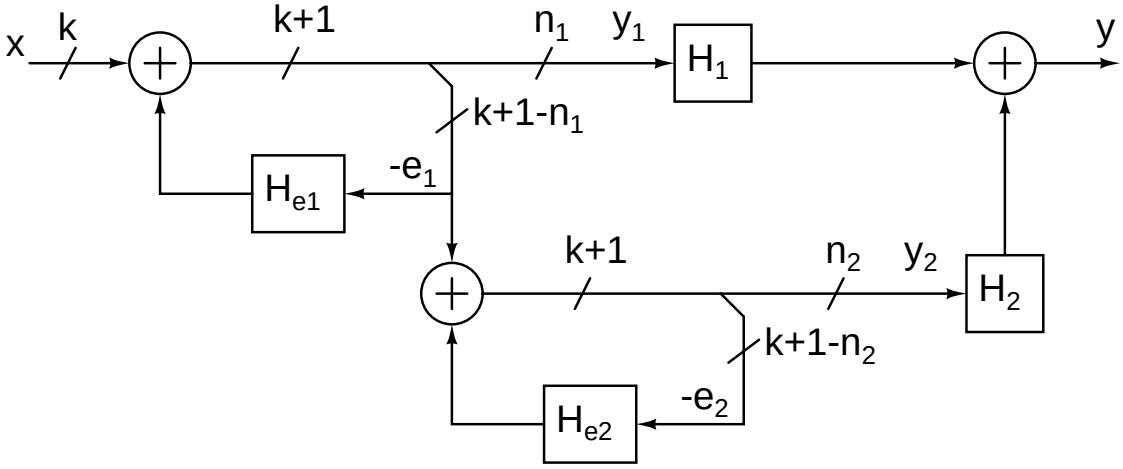

Figure 4.10 Noise-shaping loop with a cascade structure [Schreier 05]

Cascade structures

Multi-stage noise-shaping (MASH) architectures or cascade structures can circumvent the problems with stability of higher-order loops and achieve high-order noise-shaping by cascading separate noise-shaping loops of first or second order [Schreier 05]. Figure 4.10 shows a block diagram of a cascade of two noise-shaping loops. The D/A converter can be placed either after the last adder, where it needs to be multi-bit, or separate D/A converters can be used for each stage in which case single-bit D/A converters can be employed in one [Choi 01] or more of the stages [Schreier 05].

4.3.3 Multi-bit quantization

If in Figure 4.10, we have $n_2 > 1$, the noise-shaping loop with cascade structure involves multi-bit quantization. In a similar fashion, other noise-shaping architectures can be modified to accommodate multi-bit quantizers, furthermore there are specific architectures that only are feasible with multi-bit quantizers.

Noise-shaping loops involving multi-bit quantizers are more stable than their single-

bit counterparts due to their increased linearity as the variation of the effective gain of the quantizer varies less with the input signal [Schreier 05] enabling the use of more aggressive NTF. Another advantage of using multi-bit quantization is the relaxed requirements of analogue post filtering [Schreier 05] since the slewing and out-of-band noise of the D/A converter are reduced [Schreier 05].

4.3.4 Problems

Idle tones

Single stage ΔΣ-modulator architectures have been found to be susceptible to idle tones [Norsworthy 97]. The phenomenon plagues the first-order single-bit loops the most and, to a less severe extent, higher-order and multi-bit and multistage architectures [Norsworthy 97]. Bandpass ΔΣ-modulators are also subject to this problem [de la Rosa 01]. In applications where idle tones are found to be a problem, dithering has been used to tackle it [Norsworthy 97].

Stability

Instability in ΔΣ-modulators means the existence of large, but not necessarily unbounded, states, leading to SNR that is degraded compared to that predicted by the linear model; other typical phenomena exhibited by unstable ΔΣ-modulators are oscillation frequencies at or near the signal band, producing long strings of '1's and '0's in lowpass ΔΣ-modulators [Norsworthy 97].

In general, ΔΣ-modulators are unstable if the input exceeds a certain level defined as stable input range, over which it operates properly [Schreier 05].

For the first-order and, to some extent, for the second-order modulators there are theories that accurately predict the stability of the modulator, e.g. the invariant set method [Goodson 95, Norsworthy 97]. Moreover, the describing function method [Ardalan 87, Norsworthy 97] can be used for higher order modulators, but it is an approximate method. Lee's criterion 4.7 provides a rule of thumb for predicting stability in single-bit higher order modulators [Chao 90, Schreier 05].

$$\max_{\omega} \left| H(e^{j\omega}) \right| < 1.5, \tag{4.7}$$

where $H(z) =$NTF. However, this is neither a necessary nor sufficient condition for modulator stability. Computer simulations need to be used to ensure the stability of higher order modulators until rigorous theoretical results appear.

For multi-bit loops, theoretical bounds for the stable input range can be found, due to the fact that the quantizer gain only slightly varies with the input signal [Schreier 05].

4.3.5 Bandpass and quadrature

Most of the literature on ΔΣ-modulation concentrates on low-pass ΔΣ-modulation, however, the noise-shaping capabilities can also be employed in bandpass cases. Bandpass ΔΣ-modulation is achieved by, for example, applying $z \rightarrow -z^2$ transformation to a low-pass prototype [Norsworthy 97], discrete-time low-pass-to-bandpass transformation [Norsworthy 97, Lindeberg 05] or by a generalized filter approximator/optimizer [Norsworthy 97]. A bandpass ΔΣ-modulator has been used in conjunction with digital quadrature modulation in [Sommarek 04] and [Neitola 01], similarly ΔΣ-noise-shaping can form an integral part of the digital quadrature modulator [Barkin 04]. The idea of using bandpass ΔΣ-modulation together with undersampling has been presented in [Ketola 04] and [Fuji 04].

4.3.6 Post-filter for the out of band noise

The post-filter following the oversampling noise-shaping D/A converter is required to remove all out-of-band portions of the signal of the internal D/A converter without introducing nonlinear distortion. The application may impose requirements on linearity of the phase characteristics. [Schreier 05].

There are various filter architectures available for the realization of an analogue post-filter [Schreier 05]. But the filtering posterior to the ΔΣ D/A conversion can also be accomplished utilising an embedded semi-digital FIR reconstruction filter [Taleie 06, Barkin 04].

In an architecture utilizing a bandpass or quadrature ΔΣ-modulation, the post-filter needs to be a bandpass filter. In a wireless communication transmitter the specification of the standard imposes requirements on the bandpass-filter through, for example, the specification of the spectrum emission mask and ACLR [3GPP 00]. However, the post-filter specifications also depend on the noise-transfer function, i.e., a wider NTF stop band may widen the transition band of the post-filter.

4.3.7 Pulse-width modulation

In pulse-width modulation (PWM), the duty cycle of a square wave is modulated resulting in the variation of the average value of the waveform. When PWM is to be used for D/A conversion, it needs to be generated digitally, imposing exacting requirements on the sampling frequency to enable the D/A conversion to attain a high resolution [Sandler 93]. This problem can be tackled by the use of quantization and noise-shaping such as ΔΣ-modulation. A comprehensive overview of the use of PWM for D/A conversion is provided in [Sandler 93]. The most common form of PWM uses two-level or binary pulse, but also three-level or ternary pulses have been used [Rueger 04]. PWM is mostly

used in audio D/A converters. However, as a method of D/A conversion for IF or RF, it is less common, although it has been used together with class-S or class-E, class-F or class-D RF power amplifiers to drive the power amplifier using an optical PWM signal [Paolella 05] and as part of an EER system with the PWM signal driving the envelope amplifier [Raab 98] inter alia. Moreover, [Midya 02] introduces a method to produce a RF modulated signal using digital PWM; however, the method is more computationally intensive than ΔΣ-modulation and hardware implementations are scarce or non-existent in the literature. Bandpass-PWM is introduced in [Rosnell 05] as a modulation method for new transmitter architectures utilizing nonlinear power amplifiers and linearly modulated signals.

4.3.8 Implemented ΔΣ D/A-converters

Paper P5 presents a digital quadrature modulator integrated on the same chip as a 1-bit bandpass ΔΣ D/A converter with a centre frequency of 175 MHz and a sampling frequency of 700 MHz, achieving ACLR1 and ACLR2 of 50.26 and 40.27 dB for WCDMA. This high-frequency performance is remarkable in comparison to the prior art encountered in the literature.

The bandpass ΔΣ modulator topology was chosen for the sake of maximum speed. Since the notch of the noise transfer function is at a quarter of the sampling frequency, it was possible to construct a fast architecture by $z \rightarrow -z^2$ conversion from a low pass topology. Additionally, the coefficients were chosen to be realizable with shift operations. Because of the two aforementioned design selections, it was possible to employ a pipelining scheme that utilizes the inherent delay elements of the bandpass ΔΣ modulator, resulting in a critical path of two full adders and one inverter.

Paper P6 presents a tunable ΔΣ D/A converter integrated on the same chip with a DDS. The ΔΣ D/A converter is tunable within the whole Nyquist band and it was operated with a sampling frequency of 200 MHz. The in-band is 2.5 MHz wide, with an SFDR of 83 dBc. In prior art the implemented ΔΣ D/A converters can best be compared with similar systems in [Neitola 01] or [Barkin 04].

The wideband transmit ΔΣ D/A converter [Neitola 01] was implemented on an FPGA and involved a 5-bit 12th-order bandpass ΔΣ modulator with a centre frequency of 15.4 MHz and a sampling frequency of 61.4 MHz, achieving ACPR1 and ACPR2 of 69.8 and 70.5 dBc for WCDMA.

The bandpass cascaded ΔΣ D/A converter in [Barkin 04] was integrated in a 0.25um CMOS technology, providing 83 dB of dynamic range for a 6.25-MHz signal band centered at 50 MHz with a sampling rate of 200 MHz, and suppresses out-of-band quantization noise by 38 dB.

A novelty in the ΔΣ D/A converter presented in paper P6 is the tunability of the ΔΣ

modulator. Tunable ΔΣ modulators are found in A/D converters and in receivers for example in [Yang 94, Shoaei 97, Cosand 04]. The ΔΣ modulator was designed using the discrete time low-pass-to-bandpass transform and the tunability was implemented by means of a multiplier inside the loop filter with a tunable coefficient.

In both papers P5 and P6, 1-bit quantization was chosen in order to benefit from the linearity features of a 1-bit D/A converter. The 1-bit D/A converter implemented is a current-steered differential pair with one current source. The differential structure makes the output rise and fall waveforms symmetrical. In order to ensure that the two switches of the differential pair are never off at the same time, a differential driver circuitry was designed to optimize the crossing point and amplitude of the control signals.

4.4 Summary

D/A conversion in wireless communication is usually accomplished using current-steering D/A converters. Both Nyquist-rate and oversampling D/A converters are applicable; however, their different characteristics lead to them possessing relative advantages and disadvantages in different transmitter architectures. Nyquist-rate current-steering D/A converters are common in transmitter architectures with a linear power amplifier, whilst in transmitter architectures, utilizing non-linear power amplifier oversampling current-steering D/A converters such as ΔΣ-DACs have been proposed and PWM has been used in some of these architectures such as EER architectures for the conversion of the envelope signal.

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Chapter 5

Switching-mode power amplifiers

The idea of the switching-mode power amplifiers is to attain higher efficiency than in linear power amplifiers at the expense of linearity by using the transistors as switches. Switching-mode power amplifier classes include D, E and S classes, of which class-D will be reviewed in more detail in the section dedicated to it. Whilst class-F is not a switching-mode by the strictest definitions, it is also briefly reviewed.

5.1 Class-E power amplifier

A Class-E power amplifier consists of a single transistor operating as a switch, an RF choke, a parallel capacitor Cp, a resonant circuit and a load resistance, as depicted in Figure 5.1 [Krauss 80]. The parallel capacitance consists of the parasitic capacitance between the drain and the source of the switch transistor and an additional parallel capacitor, whose purpose is to improve the performance.

The transistor is switched on and off at the signal frequency and the resonant circuit between the load and the transistor only permits the signal frequency to pass through to the load, not its harmonics that form a rectangular voltage waveform at the drain of the transistor. An ideal Class-E power amplifier has an efficiency of 100%.

Class-E also endeavours to attain high efficiency using a method called *soft switching,* which involves a load network that is designed in such a way that, 1) the voltage across the switch is minimised when a current flows through, 2) the current through the switch is minimised when there is a voltage across, 3) the switching time is minimised, 4) there is delay in the rise of the voltage of the switch at turn-off so that the current has decreased to practically zero by the time the voltage increases (this can be accomplished by dimensioning the Cds capacitance appropriately), 5) the voltage of the switch returns to zero before the current starts flowing at turn-on, 6) and the slope of the voltage is zero at switch turn-on, allowing some error in the timing of the turn-on without substantial loss of efficiency 7) the voltage and current waveforms of the switch have flat tops [Sokal 75].

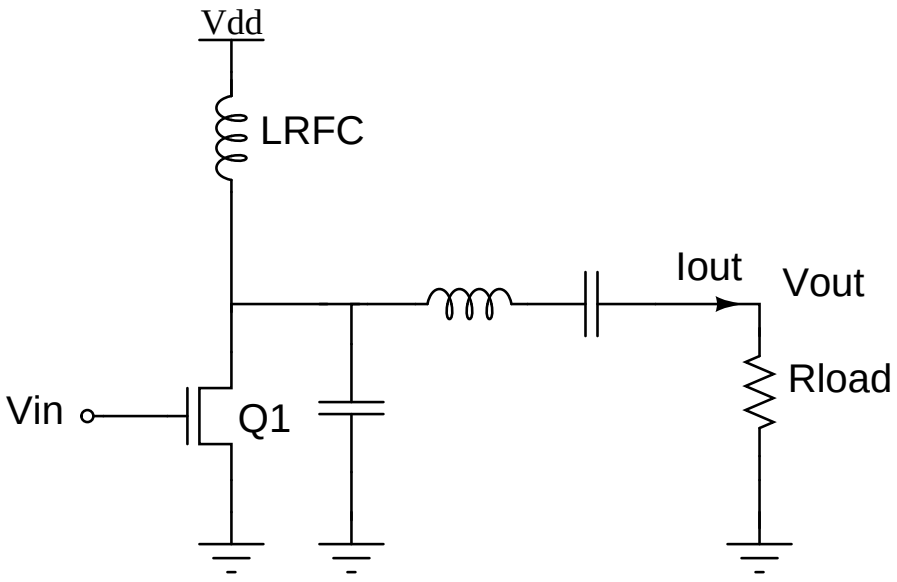

Figure 5.1 Class-E amplifier

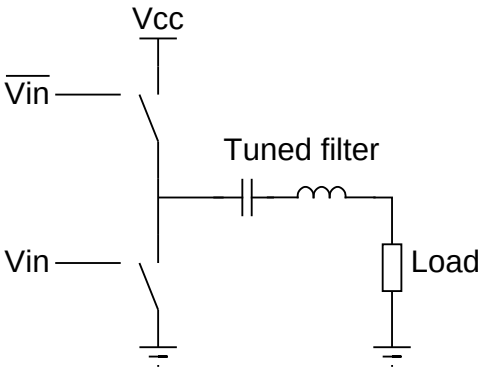

Figure 5.2 A simple class-D amplifier

5.2 Class-D power amplifier

A Class-D power amplifier is composed of two switches and a tuned output filter. The switches either switch currents in which case the configuration is called a *current-mode class-D (CMCD)* power amplifier, or voltage, in which case it is called a *voltage-mode class-D (VMCD)* power amplifier. A voltage-mode amplifier has a constant supply voltage, whereas a current-mode amplifier has a constant current flowing into the circuit. Usually the switches are realised with transistors.

Figure 5.2 shows a simple schematic of a class-D power amplifier. The input signal of a class-D power amplifier can be a pulse-width modulated (PWM) signal or a $\Delta\Sigma$ modulated signal or a delta-modulated signal [Dallago 97]. Some topologies need a differential input in order to enable the use of two identical transistors in an endeavour to achieve better symmetry. The inverted signal can, for instance, be achieved using a transformer [Kobayashi 01, Krauss 80] for the input signal or it can be generated digitally.

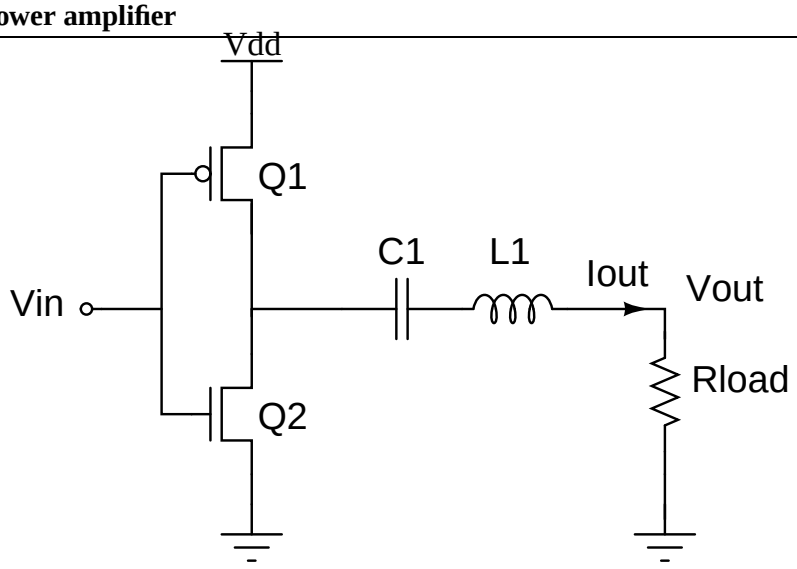

Figure 5.3 Complementary voltage-mode class-D power amplifier

5.2.1 Complementary voltage-mode configuration

In the complementary configuration shown in Figure 5.3, the switches are driven in a complementary fashion, so that one is on when the other is off. If even the transistors are complementary, then that is accomplished with the same driving signal, otherwise a differential driving signal is needed.

If we assume that the two transistors work as ideal switches, we can derive the equations that describe the operation of the PA in the ideal case as follows: when V_{in} is low, Q1 is on and Q2 is off. The potential V_{ct} between the two transistors is V_{dd}. On the other hand, when V_{in} is high, Q2 is on and Q1 is off and V_{ct} is zero. Thus the signal at V_{ct} is a square wave varying between zero and V_{dd}. Therefore its Fourier-series representation is

$$V_{ct} = \frac{1}{2}V_{dd} + \frac{2V_{dd}}{\pi}(\sin(2\pi ft) + \frac{1}{3}\sin(6\pi ft) + ...). \tag{5.1}$$

This waveform is then applied to a bandpass filter, whose centre frequency is tuned to the signal frequency f. Therefore the output voltage V_{out} is a sine wave with a maximum value [Krauss 80]

$$V_{out,max} = \frac{2V_{dd}}{\pi}. \tag{5.2}$$

The output current I_{out} through the load is a sine wave at the fundamental frequency f :

$$I_{out} = \frac{2V_{dd}}{\pi R_{load}}\sin(2\pi ft) \tag{5.3}$$

This current flows alternately through transistors Q1 and Q2 and the currents through them are half-wave rectified sine waves. The average value I_{dc} of the half-wave rectified current pulled through Q1 is

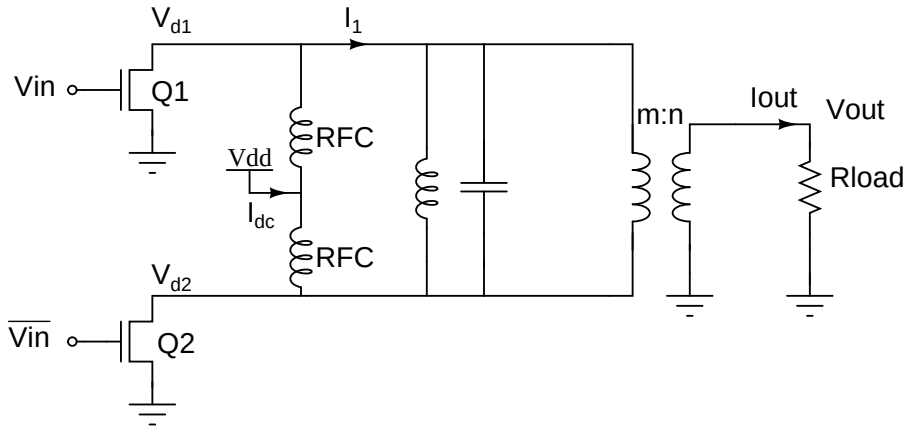

Figure 5.4 A current-mode class-D amplifier

$$I_{dc} = \frac{I_{out,max}}{\pi} = \frac{2V_{dd}}{\pi^2 R_{load}}. \tag{5.4}$$

The input power is determined by (5.5). The output power P_{out} can be calculated by multiplying the maximum value of the output voltage from (5.2) by the maximum value of the output current from (5.3) and dividing the product by two (the effective value of a sine wave). The result shows that output power equals the input power and the efficiency really equals 100% in the ideal case [Krauss 80].

$$P_{in} = P_{out} = I_{dc} V_{dd} = \frac{2V_{dd}^2}{\pi^2 R_{load}} \tag{5.5}$$

The voltage-mode configuration may need to provide a path for reverse currents to protect the transistors if they cannot tolerate reverse currents; in this case the path can be provided by diodes in parallel with the transistors.

5.2.2 Current-mode class-D amplifier

A current-mode class-D amplifier, shown in Figure 5.4, has a constant current I_{dc} flowing to the circuit through two current chokes. When Q1 is off and Q2 on, half of the current I_{dc} goes through the filter circuit to Q2. The other half flows directly to Q2 through the other choke. The current I_1 flowing to the load network is a square wave with amplitude $I_{dc}/2$.

$$I_1 = \frac{4I_{dc}}{2\pi}\left(\sin(\omega t) + \frac{1}{3}\sin(3\omega t) + ...\right) \tag{5.6}$$

Only the first harmonic flows through the primary winding of the balun, whilst other frequency components pass through the parallel LC circuit. It is then transformed to the

Table 5.1 Summary of published Class-D power amplifiers

Publication	technology	signal (MHz)	η	f_{clk} (MHz)	P_{out} (W)	topology
[Iwamoto 00]	discrete CMOS	10	33	40	0.4	VM
[Kobayashi 01]	discrete GaAsFET	900	75.6		0.73	CM
[El-Hamamsy 94]	discrete MOSFET	13.56	90	-	300	
[Kim 05]	discrete LDMOS FET	1800	63	-	50	TC-CM
[Raab 03]	discrete MOSFET	21	70	-	100	TC-VM
[Hung 05]	integrated GaAs HBT	700	78.5	-	0.89	CM
[Koizumi 94]	discrete	1	96	-	1	VM
[Varona 03]	CMOS (0.18 μm)	audio	76	5.6	7.5 m	
[Lee 00]	CMOS (0.65μm)	audio	90	-	2	VM

secondary winding, where it flows through the load causing output voltage

$$V_{out} = R_{load} I_{out} = \frac{2 I_{dc} R_{load}}{\pi} \frac{m}{n} \sin(\omega t). \tag{5.7}$$

The voltage V_d over the primary winding is a sine wave with peak value $m/nV_{out,max}$. Since one of the transistors is always on, one extreme of the primary winding is always at zero potential and the voltage over one transistor is a half-wave rectified sine wave whose DC-component is V_{dd}. Since we know by analogy from (5.4) that the maximum value of V_d is πV_{dd}, the value of I_{dc} can be derived from (5.7).

$$I_{dc} = (\frac{n}{m})^2 \frac{\pi^2 V_{dd}}{2 R_{load}}. \tag{5.8}$$

The input power P_{in} of the current-mode class-D amplifier is given in (5.9). Since the input power is I_{dc} multiplied by V_{dd}, which equals the output power, the efficiency of the amplifier is 100%.

$$P_{in} = P_{out} = V_{dd} I_{dc} = (\frac{n}{m})^2 \frac{\pi^2 V_{dd}^2}{2 R_{load}} \tag{5.9}$$

5.2.3 Survey of published class-D power amplifiers

This subsection summarizes some recent class-D power amplifiers. The focus lies on implementations at higher frequencies but two audio class-D power amplifiers have been included for comparison. Table 5.1 encapsulates the quoted signal frequency, drain efficiency, output power, topology, technology and sampling rate in cases where relevant, of the published class-D power amplifiers. TC stands for transformer-coupled, CM for current mode and VM for voltage mode.

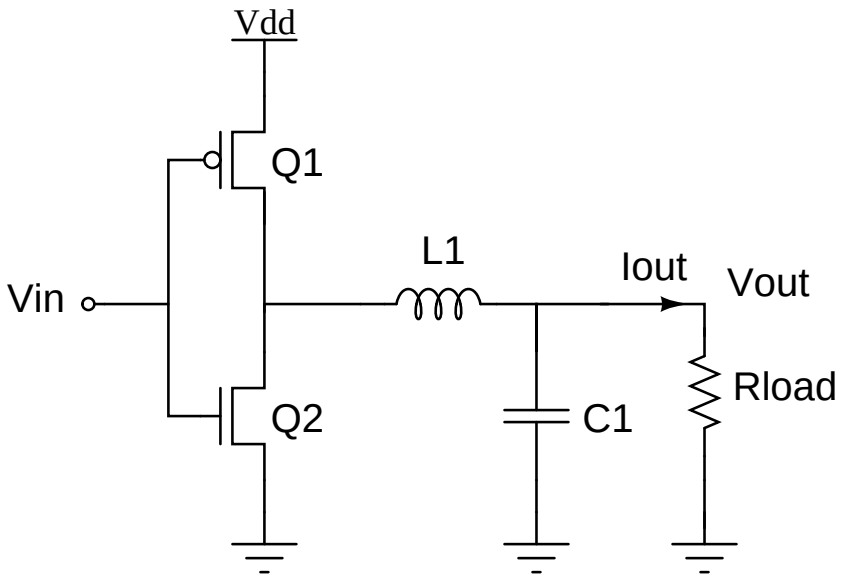

Figure 5.5 Class-S power amplifier

5.3 Class-S power amplifier

A Class-S power amplifier (Figure 5.5) is otherwise similar to Class-D except that instead of a bandpass filter (or a series resonator) it has a lowpass filter. Therefore, it only permits the slowly varying DC or average voltage component to pass to the load. Hence it is not, as such, of much interest in most transmitter architectures; instead it is more frequently found employed in audio applications. However, in EER transmitters, a Class-S power amplifier can be used to amplify the envelope signal, fed into a Class-E [Funk 96, Saari 05] or Class-D [Raab 94b, Raab 94a] or Class-F [Weiss 01] power amplifier as its supply voltage. Because of the envelope amplification it is called a Class-S amplitude modulator in this application, although the circuit topology may be the same as in a Class-S amplifier.

5.4 Class-F power amplifier

The main characteristics of a Class-F amplifier is that its load network has resonances at one or more frequencies in addition to the carrier frequency, whilst the transistor operates primarily as a current source [Krauss 80]. Figure 5.6 shows an example Class-F amplifier with a load network containing a third harmonic resonator.

The resonances in the load network produce either zero or infinite impedance at the harmonic frequencies, in such a way that either voltage or current, but not both, are present at any given harmonic frequency. In a typical Class-F power amplifier, the voltage waveform contains the odd harmonics, whilst the current waveform contains the even harmonics [Raab 97]. The waveforms can then be formulated as follows:

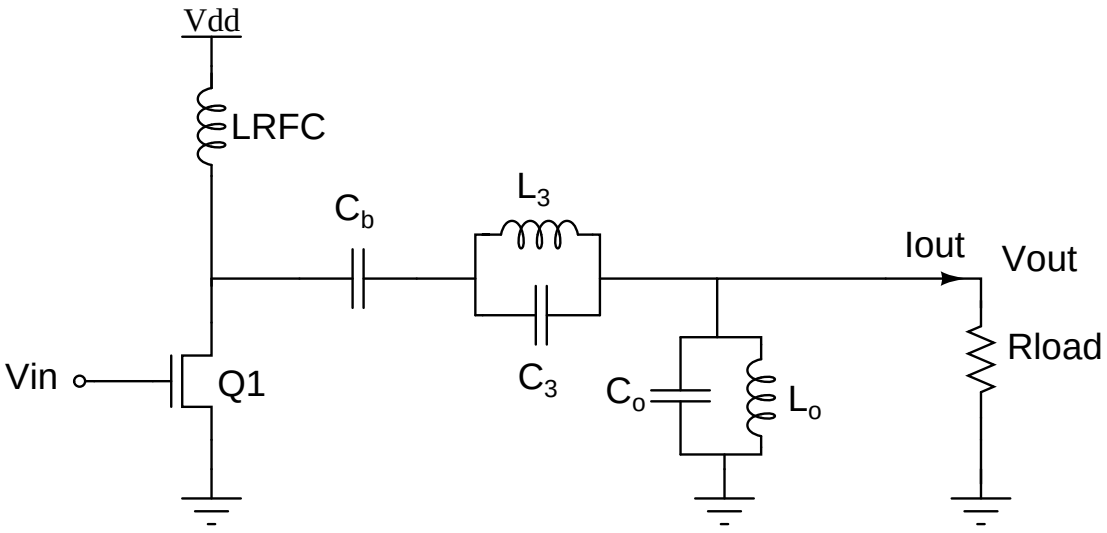

Figure 5.6 Class-F

$$\begin{aligned} v_D(\omega t) &= V_{DD} + V_{om}\sin\omega t + V_{3m}\sin 3\omega t + V_{5m}\sin 5\omega t + \ldots \\ i_D(\omega t) &= I_{dc} - I_{om}\sin\omega t - I_{2m}\cos 2\omega t - I_{4m}\cos 4\omega t - \ldots \end{aligned} \tag{5.10}$$

where ω is the fundamental frequency [Raab 97].

An alternative configuration where the voltage waveform contains the even harmonics and the current waveform contains the odd harmonics is called an *inverse Class-F power amplifier* [Wei 00].

As a result of the non-existence of the same harmonic components in both the current and voltage waveforms, power is only generated at the fundamental frequency [Krauss 80]. The more the harmonics are contained in this way in the waveforms, the better the efficiency that can be achieved. With an infinite number of resonators, the ideal efficiency is 100% as with class-D and class-E amplifiers. The effect of the finity of the number of resonators on the theoretical maximum efficiency has been studied in [Raab 01]. A typical Class-F power amplifier with resonators up to the third harmonic has a theoretical maximum efficiency of 81.6% [Raab 01].

5.5 Losses in non-linear amplifier circuits

In fact lossless switches are not available, so power losses and hence efficiency deterioration due to, for example, saturation, parasitic effects, drain capacitances, finite switching time and resistances cannot be circumvented [Raab 02]. Power is lost in non-linear power amplifier circuits with the following principal mechanisms: conduction loss, turn-on and turn-off switching losses, and gate drive loss [Jayaraman 98, El-Hamamsy 94]. Also any circuitry driving the amplifier dissipate power.

Conduction loss occurs in the resistive impedances of the circuit, including all para-

sitic resistances in passive elements such as the output filter and in the resistances associated with the transistors and in diodes associated with their on voltage.

One of the most important of these conductive losses is the one occurring in the transistors due to their on-resistance which manifests its existence by a voltage drop V_{SAT}. Then the power lost in the transistor is

$$P_{SAT} = I_{dc} V_{SAT} \tag{5.11}$$

where I_{dc} is the DC current through the transistor. This is the main source of loss in class-E, class-F and inverse class-F power amplifiers with inverse class-F attaining higher efficiency because on-resistance causes smaller losses in them [Woo 06].

Conductive loss is dependent on frequency only through skin effect, which causes only a small portion (1/e part) of the current to flow deeper than the skin depth δ_s (5.12).

$$\delta_s = \frac{1}{\sqrt{\mu_0 \sigma \pi f}}, \tag{5.12}$$

where μ_0 is the permeability in vacuum, σ the conductivity of the material and f the frequency. At low frequencies, loss due to the skin effect is relatively small if wide and flat connectors are used [El-Hamamsy 94], but at tens of megahertz or higher, skin effect cannot be fully ignored, except in the transistors where in the GHz range the skin effect has a minimal effect.

Turn-on loss occurs when a switch turns on. During transistor turn-on and turn-off there is always a period of time when neither the drain voltage V_d nor the drain current I_d are zero. During this crossover period power equal to $V_d * I_d$ is lost at any given moment. The value of power lost is proportional to the length of this period.

Another loss mechanism during the switching is the charging and discharging of the output capacitance of the switches. If FET transistors are used, output capacitance is the drain capacitance C_d. The drain capacitance is charged to rail voltage V_{dd} every time the transistor turns off and then discharged when the transistor is turned on. Each cycle energy E_d is lost [El-Hamamsy 94]. This causes power loss P_d at switching frequency f_{sw} in a transistor.

$$P_d = E_d f_{sw} = \frac{1}{2} C_d V_{dd}^2 f_{sw} \tag{5.13}$$

Capacitive power is lost in every transistor placed between the supply voltage and ground. In voltage-mode class-D amplifiers, the drain capacitance can become a dominant loss mechanism and hence limit its use at high frequencies, class-E, however, endeavours to minimise this loss using soft switching, i.e. it allows the drain capacitance to discharge to the load before the switch turns on.

Inductance L_d in the drain causes power losses when the switch turns off. At the

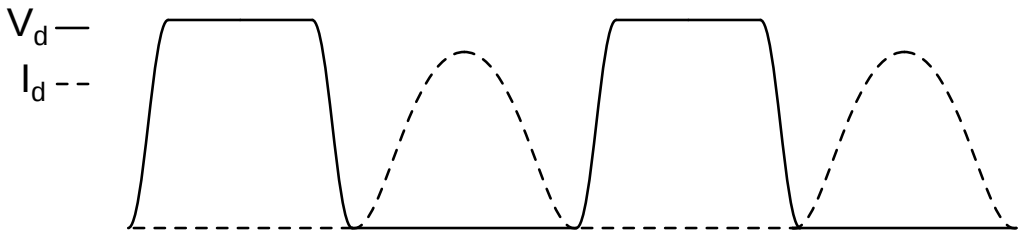

Figure 5.7 Zero current switching

moment of turn-off, current I_d flows through the transistor and inductive energy E_L is stored to the parasitic inductances. This energy is then released when the current suddenly stops. E_L is lost every cycle, but only when the switch turns off. Power P_L is lost at switching frequency f_{sw} in every transistor connected to ground [El-Hamamsy 94].

$$P_L = E_L f_{sw} = \frac{1}{2} L_d I_d^2 f_{sw} \tag{5.14}$$

This loss can be minimised by employing zero-current-switching (ZCS), where the current is always zero when the switch turns on or off. The idea is illustrated in Figure 5.7. In Class-E, ZCS is achieved by a proper design of the load network.

Losses also appear at any capacitive gate during switching. The gate capacitance charges and discharges as the switch turns on and off. At small frequencies, the loss is very small, but as the frequency grows, gate drive loss cannot be ignored anymore. The gate can be modelled as a series RC circuit consisting of a gate resistance R_g and a gate capacitance C_g [El-Hamamsy 94]. Gate drive loss depends on the drive signal and is thus different with a sine wave from with a square wave. If the gate is driven with a square wave, the current to the gate is a pulse whenever the gate voltage changes state. As the voltage at the gate rises to its maximum (V_{gs}), charge Q is stored in the gate capacitance. As the gate is charged and discharged resistively, the energy E_g is lost every time the gate turns on and off. Total power loss P_{gs} at the gate with a square wave signal frequency f is then

$$P_{gs} = 2E_g f = V_{gs} Q f. \tag{5.15}$$

When a sinusoidal gate drive is used, current I_g to the gate is sinusoidal. Power loss $P_{g,\sin}$ at the gate drive at the frequency f is then

$$P_{g,\sin} = \frac{1}{2} I_g^2 R = \frac{1}{2} (2\pi f Q)^2 R, \tag{5.16}$$

where R is the sum of gate resistance and drive circuit resistance [El-Hamamsy 94].

Turn-on and turn-off switching losses are clearly dominant loss mechanisms in modern Class-D amplifiers operating at MHz and GHz range. Capacitive loss becomes the dominant loss mechanism when switching frequencies rise to hundreds of MHz and the

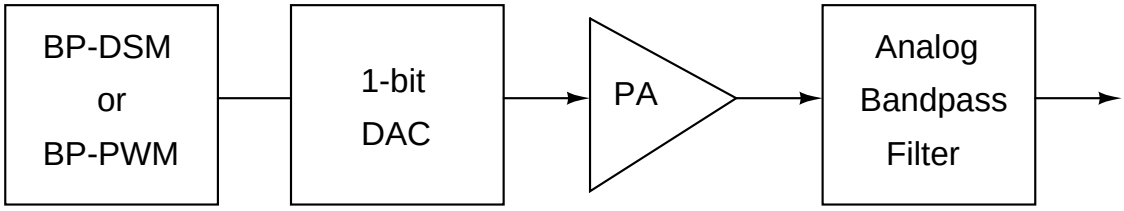

Figure 5.8 Switching-mode power amplifier driven by an oversampling noise-shaping D/A converter

significance of inductive loss gets smaller [Krauss 80]. In order to reduce the capacitive loss, the voltage across the switch should be zero when it turns on or off. This is called *zero-voltage-switching* (ZVS) and can be achieved with a current-mode class-D amplifier, if the switching frequency is the same as the signal frequency [Kobayashi 01], by including the drain capacitance in the filter as a parallel capacitance. Then voltage over a closed switch is zero due to the filter resonance.

For a voltage-mode class-D it is more difficult to achieve ZVS. However, it can be accomplished by using a dead time between the pulses [El-Hamamsy 94, Lau 00]. A disadvantage of using dead time is that it may cause distortion, however, it has been shown in [Nyboe 06] that in some cases dead time actually decreases distortion. Class-E is based on the idea of designing the load network in such a way that the ZVS conditions are fulfilled [Sokal 75].

5.6 Switching-mode power amplifiers with oversampling noise-shaping D/A converters

The switching-mode power amplifier classes are non-linear and, as such, are therefore most prominently suitable for constant envelope modulation signals. However, many of the wireless communication standards require the transmitted signal to contain amplitude modulation in addition to phase modulation. The envelope can be modulated and a high linearity achieved [Jayaraman 98] if the switching-mode power amplifier is driven by an oversampling noise-shaping D/A converter using $\Delta\Sigma$-modulation or pulse-width modulation.

The concept is depicted in Figure 5.8. The digitally upconverted signal is noise-shaped using a 1-bit bandpass $\Delta\Sigma$-modulator [Keyzer 01] or a bandpass pulse-width modulator [Midya 02]. The output signal from this block is D/A converted with a 1-bit D/A converter. The 1-bit D/A converter drives the switching-mode power amplifier and the reconstruction filter of the D/A converter is posterior to the power amplifier; this must be a bandpass filter since the bandpass noise shaping moves the quantization noise to both sides of the signal band.

The switching-mode power amplifier class most suitable for amplifying bandpass ΔΣ-modulated or bandpass pulse-width modulated signals is Class-D. However, in [Dupuy 04], a variation of the Kahn EER technique is reported, where the envelope of the signal is ΔΣ-modulated and the phase is modulated with this envelope. The resulting signal drives a Class-E amplifier.

Whilst switching-mode power amplifiers have the potential for reaching very high efficiencies [Kobayashi 01], the high efficiencies are difficult to reach with non-constant envelope modulated signals when the crest factor of the envelope is high since the switching activity of the 1-bit signal from bandpass noise-shaped oversampling D/A converters is not dependent on the signal level. Moreover, the proximity of the quantization noise to the signal band makes the spectral requirements of the communication standard challenging to comply with [Keyzer 01, Larson 05].

5.6.1 Cases researched in the papers

Papers P7, P8, and P9 all study the combination of a Class-D power amplifier with 1-bit oversampling bandpass noise-shaping D/A converters at high frequencies. The focus is on 1-bit bandpass ΔΣ D/A conversion, but in P9 bandpass PWM is also experimented with. The ΔΣ cases are best compared in the literature with [Jayaraman 98], which reaches higher efficiency than the measured cases in papers P8 and P9, but on the other hand papers P7-P9 experiment with several topologies and use higher sampling frequencies. The PWM case is best compared with [Midya 02].

Paper P7 compares by simulation different topologies of a Class-D power amplifier to be driven by a 1-bit ΔΣ modulated signal. Paper P8 extends this comparison to measurements of two of the topologies. Paper P9 compares the 1-bit bandpass ΔΣ modulated and 1-bit bandpass pulse width modulated drive signals for a Class-D power amplifier. The comparison includes measurements, unlike in [Midya 02]. The measured efficiencies were 16.8% for ΔΣ and 20.3% for PWM.

5.7 Comparison of the classes

The application of a voltage-mode class-D amplifier using complementary devices is limited at RF-frequencies as p-type transistors tend to have low gain bandwidth f_T [Krauss 80]. Using two n-type transistors imposes the use of transformers that cannot readily be integrated. Also, the output capacitance of the transistors causes losses that limit the applications at high frequencies.

In current-mode class-D and in class-E, the output capacitance can form part of the load network, so that it is not the main factor that deteriorates the efficiency at high frequencies. In other words they endeavour to achieve ZVS. Class-F employs a multihar-

monic resonator to achieve ZVS (or ZCS). Class-E and Class-F have been used in RF applications and the use of high efficiency current-mode class-D has been demonstrated at RF frequencies.

Class-S has been used in RF transmitters based on the EER technique to amplify the envelope signal, but it is obviously more frequently found in low frequency applications.

Chapter 6

Summary of Publications

In this chapter, a brief overview of each publication is given.

[P1] A Multicarrier GMSK Modulator for Base Station

In this paper, a multicarrier Gaussian minimum shift keying (GMSK) modulator with a 14-bit on-chip digital-to-analogue (D/A) converter is presented. The design contains four GMSK modulators, which generate GMSK modulated carriers at the user-defined centre frequencies. In the wireless base stations, the modulated transmit signals are usually combined at the RF frequency after power amplification. The multicarrier modulator combines four GMSK modulated signals in the digital domain, thereby eliminating the need for an antenna microwave combiner. A new digital ramp generator and output power-level controller performs both the burst ramping and the dynamic power control in the digital domain. The maximum dynamic performance is obtained by multiplexing two D/A converters with output sampling switches. The digital multicarrier GMSK modulator is designed to fulfil the derived spectrum and phase-error specifications of the GSM 900/1800/1900 base stations for pico-, micro, and macrocells. The circuit was integrated in a 0.35-μm CMOS technology.

[P2] A GSM/EDGE/WCDMA Modulator With On-chip D/A Converter for base station

This paper presents a GSM/EDGE/WCDMA modulator with a 14-bit on-chip D/A converter. The modulator consists of several digital signal processing building blocks, including a programmable pulse shaping filter, interpolation filters, re-sampler, CORDIC rotator, programmable output power level controller and ramping unit, and x/sinx filter. The pre-compensation filter, which compensates the sinc droop above the Nyquist frequency, makes it possible to use WCDMA signal images for up-conversion. The new pro-

grammable up/down unit allows power ramping on a time-slot basis as specified for GSM, EDGE and TDD-WCDMA. The multi-standard modulator meets the spectral, phase and error vector magnitude (EVM) specifications. The integrated circuit was implemented in a 0.35 μm CMOS technology.

[P3] 14-bit 110 MHz CMOS D/A Converter

This paper provides a more detailed presentation of the 14-bit D/A current steering converter used in the multimode modulator presented in paper P2. The D/A converter utilizes a segmented current source architecture and well designed and carefully laid out switch drivers and current switches. The measured INL and DNL are 1.04 and 0.83, respectively. The D/A converter was fabricated with a 0.35 μm CMOS technology.

[P4] A Digital Quadrature Modulator With On-Chip D/A Converter

This paper describes a digital quadrature modulator that can replace the first analogue IF mixer stage of a base station transmitter. It interpolates orthogonal input carriers by 16 and performs digital quadrature modulation at carrier frequencies $f_s/4$, $-f_s/4$ and $-f_s/2$. A 12-bit D/A converter is integrated on-chip using a segmented current source architecture and a proper switching technique to reduce spurious components and to enhance dynamic performance. The modulator is designed to fulfil the spectral, phase, and EVM specifications of GSM, EDGE and WCDMA base stations.

[P5] A Digital Modulator with Bandpass Delta-Sigma Modulator

In this paper, the digital quadrature modulator of the previous paper is further developed and combined with a bandpass $\Delta\Sigma$-modulator. It interpolates orthogonal input carriers by 16 and performs a digital quadrature modulation at carrier frequencies $f_s/4$, $-f_s/4$, (f_s is the sampling frequency). After quadrature modulation, the signal is converted into an analogue IF signal using a bandpass $\Delta\Sigma$ modulator and a 1-bit D/A converter. The circuit was integrated in a 0.13μm CMOS technology and operated at a clock frequency of 700MHz.

[P6] A 1.5V direct digital synthesizer with tunable Delta-Sigma modulator in 0.13 μm CMOS

This paper introduces a new direct digital synthesizer architecture that combines a direct digital synthesizer with a tunable $\Delta\Sigma$ modulator whose signal band of the $\Delta\Sigma$ modulator can be tuned tuned according to the DDS output frequency. We use a hardware-efficient phase-to-sine amplitude converter in the DDS that approximates the first quadrant of the sine function with 16 equal-length piecewise second-degree polynomial segments. The DDS is capable of frequency, phase and quadrature amplitude modulation. The circuit was integrated in a 0.13 μm CMOS technology and operated at a clock frequency of 200 MHz.

[P7] Comparison of Different Class-D Power Amplifier Topologies for 1-bit RF Band-Pass Delta-Sigma D/A Converters

In this paper the suitabilities of different class-D power amplifier architectures are compared for using a 1-bit bandpass $\Delta\Sigma$ D/A converter as a driving stage, operating with RF signals. The objective is to find out which architecture provides the best efficiency. The architectures considered are voltage-mode, H-bridge voltage-mode, current-mode and transformer-coupled voltage- and current-mode class-D amplifiers. These architectures are compared by APLAC simulation for discrete GaAs MESFET realisations.

[P8] Comparison of Different Class-D Power Amplifier Topologies for 1-bit Band-Pass Delta-Sigma D/A Converters

This paper is a continuation of the previous paper and it compares the suitabilities of two different class-D power amplifier architectures for 1-bit bandpass $\Delta\Sigma$ D/A converters operating with RF signals. The objective is to find out which architecture provides the best efficiency. The architectures considered are H-bridge voltage-mode class-D amplifier and transformer-coupled voltage-mode class-D amplifier. These architectures are compared by APLAC simulation using a $\Delta\Sigma$ modulated signal and by measuring discrete component GaAs MESFET realisations.

[P9] A 20 MHz BP-PWM and BP-DSM Class-D PA in 0.18 μm CMOS

This paper juxtaposes a Class-D power amplifier for bandpass pulse-width modulated (BP-PWM) with a bandpass delta-sigma modulated (BP-DSM) signals at 20 MHz. A 1-bit sixth order topology is used in the $\Delta\Sigma$-modulator and 6-bit fourth-order integral noise shaping is used in the generation of the bandpass pulse-width modulated signal. The pulse-width modulation is two-sided. The push-pull amplifier part of the Class-D amplifier was fabricated on a 0.18 μm CMOS process and the bandpass filter was composed of a LC ladder network realised with discrete components.

Chapter 7

Conclusions

In wireless base station transmitters there is a trend towards digitalisation. From the baseband to radio frequency, more and more parts in the baseband end are being implemented with digital circuitry. This thesis contributes to various parts of this process of digitalisation.

In the baseband stage, a multicarrier digital modulator that combines multiple modulated signals at different carrier frequencies digitally at the baseband, has been designed. The research was motivated by the need to seek cost reductions in base station transmitter circuits by digitalization as the analogue circuitry needed for multicarrier transmitters needs expensive tuning.

Moreover, a multimode digital modulator that can be operated for three different communications standards was implemented. The research was motivated by the need for base station transmitters to support multiple communications standards. By integrating the multistandard modulator in a single chip, the production volume of the chip can be increased and cost reductions achieved thereby.

Direct digital frequency synthesizers (DDFSs), both LUT- and CORDIC-based, were found to be suitable for the generation of several different modulations in wireless communication. How they are used for multicarrier or multistandard modulator architectures was demonstrated. In multicarrier architectures, the integration of the power level control and ramping unit was motivated by the need to have different power levels for different carriers and the choice of digital recursive oscillators for this purpose was shown to be suitable because of its hardware efficiency.

In an endeavour to move the digital-analogue interface antenna-wards in base station architectures, digital upconversion was researched. Digital quadrature modulation utilizing a multiplier-free quadrature modulator was found to be an advantageous method to replace the first analogue mixer stage of a two-step transmitter architecture with digital circuitry.

The digital-analogue interface in the transmitters was a focal point of the research in the thesis. The D/A converters in all the implemented circuits were integrated on the

same chip with a digital modulator circuit, in order to avoid high-speed data crossing over the inter-chip boundary. A challenge that was posed was to impede the digital part from disturbing the D/A converter operation; this was successfully achieved in the implemented D/A converters.

The research on ΔΣ D/A converters was motivated by the lack of high-speed high-resolution capabilities of the Nyquist-rate D/A-converters shown in Table 4.1. An alternative D/A conversion method for them was therefore sought. The emphasis on 1-bit bandpass ΔΣ modulators within this ΔΣ D/A converter research was motivated by the possibility of combining it with a switching mode power amplifier. An advantage of the selected 1-bit quantization was its inherent linearity. In the implementation of a bandpass ΔΣ modulator for the digital quadrature modulator chip, a fast topology was achieved utilizing $z \rightarrow -z^2$ conversion.

Finally, even power amplification can, in a sense, be performed in a digital fashion by using a switching-mode power amplifier. This was researched experimentally with both discrete and integrated implementations using 1-bit ΔΣ modulation and pulse-width modulation as the input signal generation methods.

The combination of switching-mode power amplifiers with 1-bit Delta-Sigma modulator-based D/A conversion was further motivated by the need to seek more efficient transmitter architectures and therefore more efficient power amplifiers and was a continuation of the previous research on Delta-Sigma D/A converters. The combination of a switching mode power amplifier and a 1-bit Delta-Sigma D/A converter did not prove to be an efficient transmitter architecture.

7.1 Further work

Digital modulator and upconverter research could proceed towards a completely programmable general-purpose architecture that could be configured to accommodate new standards and different frequency bands according to needs. The research on software-defined radios and cognitive radios is going in this direction [Devroye 06].

As for ΔΣ D/A converters, further work could include investigating the possibilities of pipelining further from the extent of paper P5 based on inherent delay elements.

In the field of the transmitter architecture based on 1-bit ΔΣ D/A converters and switching-mode amplifiers, further work could include the development of better bandpass filters that would contribute to a good performance and a higher efficiency. The architecture imposes exigent requirements on the transition bands of the bandpass filter.

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