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Low-Noise Amplifiers for Integrated Multi-Mode Direct-Conversion Receivers

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Abstract

The evolution of wireless telecommunication systems during the last decade has been rapid. During this time the design driver has shifted towards fast data applications instead of speech. In addition, the different systems may have a limited coverage, for example, limited to urban areas only. Thus, it has become important for a mobile terminal to be able to use different wireless systems, depending on the application chosen and the location of the terminal.

The choice of receiver architecture affects the performance, size, and cost of the receiver. The superheterodyne receiver has hitherto been the dominant radio architecture, because of its good sensitivity and selectivity. However, superheterodyne receivers require expensive filters, which, with the existing technologies, cannot be integrated on the same chip as the receiver. Therefore, architectures using a minimum number of external components, such as direct conversion, have become popular. In addition, compared to the superheterodyne architecture, the direct-conversion architecture has benefits when multi-mode receivers, which are described in this thesis, are being designed.

In this thesis, the limitations placed on the analog receiver by different system specifications are introduced. The estimations for the LNA specifications are derived from these specifications. In addition, the limitations imposed by different types of receiver architectures are described. The inductively-degenerated LNA is the basis for all the experimental circuits. The different components for this configuration are analyzed and compared to other commonly-used configurations in order to justify the use of an inductively-degenerated LNA. Furthermore, the design issues concerning the LNA-mixer interface in direct-conversion receivers are analyzed. Without knowing these limitations, it becomes difficult to understand the choices made in the experimental circuits.

One of the key parts of this thesis describes the design and implementation of a single-chip multi-mode LNA, which is one of the key blocks in multi-mode receivers. The multi-mode structures in this thesis were developed for a direct-conversion receiver where only one system is activated at a time. The LNA interfaces to a pre-select filter and mixers and the different LNA components are analyzed in detail. Furthermore, the design issues related to possible interference from additional systems on single-chip receivers are analyzed and demonstrated.

A typical receiver includes variable gain, which can be implemented both in the analog baseband and/or in the RF. If the variable gain is implemented in the RF parts, it is typically placed in the LNA or in a separate gain control stage. Several methods that can be used to implement a variable gain in the LNA are introduced and compared to each other. Furthermore, several of these methods are included in the experimental circuits.

The last part of this thesis concentrates on four experimental circuits, which are described in this thesis. The first two chips describe an RF front-end and a direct-conversion receiver for WCDMA applications. The whole receiver demonstrates that it is possible to implement A/D converters on the same chip as sensitive RF blocks without significantly degrading receiver performance. The other two chips describe an RF front-end for WCDMA and GSM900 applications and a direct-conversion receiver for GSM900, DCS1800, PCS1900 and WCDMA systems. These ICs demonstrate the usability of the circuit structure developed and presented in this thesis. The chip area in the last multi-mode receiver is not significantly increased compared to corresponding single-system receivers.

Keywords: analog integrated circuit, BiCMOS, direct-conversion, low-noise amplifiers, mobile communication, multi-mode, radio receivers.

Preface

The research for this thesis has been carried out in Electronic Circuit Design Laboratory of Helsinki University of Technology between 1998 and 2003. The work presented in this thesis is part of a research project funded by Nokia Networks, Nokia Mobile Phones, and Finnish National Technology Agency (TEKES). During years 2001-2003, I had the privilege of participating the Graduate School in Electronics, Telecommunications, and Automation (GETA), which partially funded my studies. I also thank the following foundations for financial support: Nokia Foundation, the Finnish Society of Electronics Engineers (EIS), Emil Aaltonen Foundation, the Foundation of Technology (TES), Jenny and Antti Wihuri Foundation, and the Foundation for Financial Aid at Helsinki University of Technology.

I would like to thank my supervisor Prof. Kari Halonen for the opportunity to work relatively freely on an interesting research topic and his encouragement and guidance during the research. I also warmly thank Prof. John Long and Dr. Petteri Alinikula for reviewing my thesis and for their valuable comments and suggestions.

I want to express my gratitude to all my present and former colleagues at the laboratory for creating a relaxed and pleasant atmosphere. I wish to thank Dr. Aarno Pärssinen for his valuable advices and instructions and for teaching me a lot of things about the design of RF circuits and direct-conversion receivers. I am also grateful to Dr. Jarkko Jussila for advices and comments in the field of integrated radio receivers and analog baseband circuits. In addition, I would like to thank Mikko Hirvonen, Jouni Kaukovuori, and Kari Stadius for their help and comments during the project.

The members of the research team “SuMu”, Dr. Jarkko Jussila, Dr. Kalle Kivekäs, Dr. Aarno Pärssinen, and Dr. Lauri Sumanen, deserve special thanks for creating an excellent working atmosphere. Without their help and contributions this thesis had never been finished. Especially the high motivation and friendly atmosphere among this team helped this thesis. In addition, the junior researchers in direct conversion receiver projects and power amplifier projects, Mikko Hotti, Jere Järvinen, Pasi Juurakko, Jouni Kaukovuori, Arto Malinen, and Ville Saari, is also gratefully acknowledged.

Finally, my warmest thanks go to my parents Hillevi and Kari and my brother Heikki for their support and encouragement during my studies. A huge thanks goes to my dear wife, Kirsi, who has shared the good as well as the difficult times during this doctoral work.

Jussi Ryynänen

Espoo, June 2004

Contents

Symbols and abbreviations

Symbols

A	Area of bipolar transistor
A_1,A_2…	Amplitude, amplifier
A_V	Voltage gain
B	Channel bandwidth, Amplitude
C	Capacitor, capacitance
C_{je}	Base-emitter capacitor of bipolar transistor
C_{gs}	Gate-source capacitor of MOS transistor
C_π	Base-emitter capacitor of bipolar transistor
e_n	Noise voltage
E_b	Bit energy
B_n	System noise bandwidth
f	Frequency
f_1, f_2,	Signal frequencies
f_{CLK}	Clock frequency
$f_{flicker}$	Corner frequency of flicker noise
f_{HPF}	Cutoff frequency of highpass filter
f_{LO}	Local oscillator frequency
f_{RF}	Radio frequency
f_{SYS}	Frequency of the additional system
f_T	Unity-gain frequency
f_{TX}	Transmitter frequency
G	Gain
g_m	Transconductance
G_m	Transconductance
i	AC current
I	In-phase
I_B	Base current of a bipolar transistor
I_C	Collector current of a bipolar transistor
Idd	Current consumption
k	Boltzmann's constant ≈ $1.3807 \cdot 10^{-23}$J/K

K	Constant
k_{cmod}	Empirical factor
L	Inductor, loss, effective channel length of a MOSFET
M	MOSFET
m_c	Frequency conversion term
n	Bipolar transistor ideality factor
N_{in}	Noise power at input
N_{out}	Noise power at output
Pcmod	Cross modulation power in the user channel
P_d	Power dissipation
P_{in}	Input power
P_{imd2}	Power of second-order intermodulation product at output
P_{imd3}	Power of third-order intermodulation product at output
P_{LO}	Power of local oscillator
P_{out}	Output power
P_1, P_2	Signal powers
q	Electron charge $\approx 1.602 \cdot 10^{-19}$C
Q	Quadrature-phase, quality factor, bipolar transistor
R	Resistor, resistance
r_o	Output resistance
r_π	Base-emitter resistance of bipolar transistor
R_S	Source resistance
S_{in}	Signal power at input
S_{out}	Signal power at output
$S_{sensitivity}$	Sensitivity level
S_{th}	Thermal noise floor
S11	Scattering parameter of two-port (reflection)
T	Absolute temperature
T_{bit}	Bit duration
T_{chip}	Chip duration
V	DC voltage, signal amplitude
V_{BE}, V_1, V_π	Base-emitter voltage of a BJT
V_{gs}	Gate-source voltage of a MOSFET
v_{out}	Output signal

v_s	Source voltage
V_T	Thermal voltage
W	Effective channel width of a MOSFET
Z_{IN}	Input impedance
Z_L	Load impedance
Z_S	Source impedance
α_1, α_2…	Nonlinearity coefficients
β	Bipolar transistor current gain
δ	MOS transistor noise constant
ΔP_2	Power difference between fundamental and second-order signals
ΔP_3	Power difference between fundamental and third-order signals
γ	MOS transistor noise constant
τ_F	Forward transit time of a BJT
ω	Angular frequency
ω_r	Angular frequency at resonance

Abbreviations

AC	Alternating current
ADC	Analog-to-digital converter
AGC	Automatic gain control
AM	Amplitude modulation
AMPS	Advanced mobile phone system
BER	Bit-error rate
BiCMOS	Bipolar complementary metal oxide semiconductor
BJT	Bipolar junction transistor
BPF	Bandpass filter
BS	Base station
CDMA	Code division multiple access
CMFB	Common-mode feedback
CMOS	Complementary metal oxide semiconductor
CG	Coding gain
CLK	Clock
CW	Continuous wave

DAC	Digital-to-analog converter
DC	Direct current
DCR	Direct-conversion receiver
DCS1800	Digital cellular system
DNL	Differential nonlinearity
DS	Direct Sequence
DSB	Double sideband
DSP	Digital signal processor
ENOB	Effective number of bits
ESD	Electrostatic discharge
F	Noise factor
FDD	Frequency division duplex
FER	Frame error rate
FFT	Fast Fourier transform
FH	Frequency hopping
GMSK	Gaussian minimum shift keying
GPS	Global positioning system
GSM, GSM900	Global system for mobile communications
HPF	Highpass filter
IC	Integrated circuit
ICP	Input compression point
IF	Intermediate frequency
IIP2	Second-order input intercept point
IIP3	Third-order input intercept point
INL	Integral nonlinearity
ITU	International Telecommunications Union
LC	Inductor-capacitor
LNA	Low-noise amplifier
LO	Local oscillator
LSB	Least significant bit
MS	Mobile station
MOS	Metal oxide semiconductor
NF	Noise figure
NMOS	N-channel metal oxide semiconductor

OFDM	Orthogonal frequency division multiplex
OIP3	Third-order output intercept point
PCB	Printed circuit board
PCS1900	Digital cellular system
PMOS	P-channel metal oxide semiconductor
PSD	Power spectral density
QPSK	Quadrature phase shift keying
RC	Resistor-capacitor
RC-PP	Resistor-capacitor polyphase filter
RF	Radio frequency
RMS	Root-mean-square
RX	Receiver
SAW	Surface acoustic wave
SF	Spreading factor
SFDR	Spurious free dynamic range
SG	Spreading gain
SHF	Super high frequency
SiGe	Silicon-germanium
SNDR	Signal-to-noise and distortion ratio
SNR	Signal-to-noise ratio
SS	Spread spectrum
SSB	Single sideband
TDD	Time division duplex
TDMA	Time division multiple access
TX	Transmitter
UHF	Ultra high frequency
UTRA	UMTS terrestrial radio access
VCO	Voltage controlled oscillator
WCDMA	Wide-band code division multiple access
WLAN	Wireless local area network
2G	Second generation
3G	Third generation

1 Introduction

1.1 Motivation for the thesis

The evolution of current wireless communication systems has been very rapid. The goal has been small-size and low-cost terminals that can be programmed for different applications. Hence, the trend has been towards digital transceivers. The implementation of a "full" digital transceiver is still unrealistic and, therefore, many analog circuits that shape and transform the data are required. In addition, the implementation of future systems sets new challenges for circuit and system level design. The implementation of high data rates in wireless systems may require for example, wide channel bandwidths, continuous-time reception, and, because of the available frequency bands, usually high receive and transmit frequencies (> 2GHz). In addition, new systems should be implemented using low supply voltages without significantly degrading the performance compared to the current systems. For example, the operation time of a terminal with fast data rates should be the same as in current terminals. Therefore, the design of integrated analog circuits becomes very challenging and new circuit- and system-level solutions will be needed.

The first terminals using 3G wide-band code division multiple access (WCDMA) systems are already available to consumers. These terminals can provide high-speed data connections, thus partly making possible fast and real-time Internet connections. At first, these systems will cover urban areas and, in order to maintain a connection to these terminals, the terminal should be able to use other existing systems in rural areas. In addition, it may be more optimal to use the other systems for different types of applications. For example, GSM-based systems could be used for speech connections when high-speed data is not required. The integration of these multi-system, multi-band terminals is challenging because, in order to minimize the size of these transceivers, the different systems should share most of their building blocks.

One of the most challenging building blocks in multi-mode receivers is the low-noise amplifier (LNA). In order to achieve a sufficient performance, frequency-selective components are usually required in the LNA. Therefore, the operation bandwidth of the LNA is not sufficient for multi-band and multi-system operation without the addition of adjustable components. Furthermore, when the LNA is integrated on the same chip as the other building blocks, the interference from these blocks can deteriorate the performance of the LNA.

1.2 Research contribution and publications

This thesis concentrates on the design and implementation of LNAs for multi-mode direct-conversion receivers (DCRs). The author describes and proposes solutions for the design and implementation of this type of LNA. The approach in this thesis has been to start the design from the system requirements. The requirements for the LNA are derived from the specifications, together with the designers of the other blocks. The circuit structures for multi-mode receivers are developed from the LNA specifications. The goal has not been to develop or model different devices on the IC. The IC manufacturer provided the detailed models for the passives, transistors, and bonding pads including ESD, used in the experimental circuits.

A huge number of LNAs have been reported in the literature. It is not the purpose of this thesis to review the development of these LNAs comprehensively. The focus is on the recently-

published designs. The author has designed and implemented all the LNAs presented in this thesis. The first two experimental circuits are designed for a WCDMA receiver, and the other two are targeted for multi-mode applications. The main emphasis in this thesis is on finding circuit solutions to make multi-mode operation possible by sharing devices already in the LNA, thus excluding straightforward parallel structures. In addition, the focus is on how to implement a variable gain in single-system and multi-mode LNAs.

The research team which designed, implemented, and measured the receivers published in this thesis consisted of five members, including the author. The other researchers were Dr. Jarkko Jussila, Dr. Kalle Kivekäs, Dr. Aarno Pärssinen, and Dr. Lauri Sumanen. In each paper, the first author had the main responsibility for the manuscript.

Papers P1 and P2 describe a chip-set for a direct-conversion receiver designed for the WCDMA system. Dr. Pärssinen and Dr. Jussila made the system design for the receiver. The author is responsible for the design, implementation, and partitioning of the RF front-end, together with Dr. Pärssinen. Dr. Jussila and Dr. Sumanen are responsible for the analog baseband and A/D converter chips, respectively.

Paper P3 is a conference article based on P1 and P2 and presents the RF front-end of the chip-set in P1. The contribution of the author is the same as in P1 and P2.

Paper P4 is a single-chip version of the receiver presented in P1. Only minor modifications were made to the RF front-end of the receiver. The author's contribution is the same as in P1.

Papers P5 and P6 present a single-chip receiver designed for WCDMA systems. The author contributed to the RF front-end partitioning, LNA design, and implementation. He also participated in the receiver measurements. The A/D converter, which was implemented on the same chip as a sensitive RF front-end, had only a minor effect on the performance of the receiver. Dr. Jussila and Dr. Pärssinen participated in the receiver partitioning. In addition, Dr. Pärssinen contributed to the RF front-end design; Dr. Kivekäs contributed to the RF front-end partitioning and mixer design and implementation. Dr. Jussila and Dr. Sumanen are responsible for the analog baseband and A/D converter circuits, respectively.

Papers P7 and P8 present an RF front-end, which is targeted for WCDMA and GSM applications. The RF front-end can use all devices except the LNA input stage in both modes. The author is responsible for the RF front-end partitioning, the LNA, and single-ended-to-differential converter design and implementation. Dr. Kivekäs and Dr. Pärssinen contributed to the RF front-end partitioning and Dr. Kivekäs was responsible for the mixer design.

Paper P9 is a journal article which deals with the single-chip quad-mode direct-conversion receiver. The component sharing of this receiver is optimised and it uses only four on-chip inductors. In addition, the gain control transients from the LNA gain control are significantly improved compared to those in previous publications by the same author. The author is responsible for the receiver partitioning, together with Dr. Kivekäs and Dr. Jussila. In addition, the author is responsible for the LNA design and LNA-mixer interface design. The receiver was implemented in co-operation with Dr. Jussila, Dr. Kivekäs, Dr. Pärssinen, and Dr. Sumanen.

P1 A. Pärssinen, J. Jussila, J. Ryynänen, L. Sumanen, K. Halonen, "A Wide-Band Direct Conversion Receiver for WCDMA Applications," ISSCC Digest of Technical Papers, pp. 220-221, Feb. 1999.

P2 A. Pärssinen, J. Jussila, J. Ryynänen, L. Sumanen, K. Halonen, "A 2-GHz Wide-Band Direct Conversion Receiver for WCDMA Applications," IEEE J. Solid-State Circuits, vol. 34, pp. 1893-1903, Dec. 1999.

P3 J. Ryynänen, A. Pärssinen, J. Jussila, K. Halonen, “An RF Front-End for the Direct Conversion WCDMA Receiver,” IEEE RFIC Digest of Papers, June 1999, pp. 21-24.

P4 A. Pärssinen, J. Jussila, J. Ryynänen, L. Sumanen, K. Kivekäs, K. Halonen, “A Wide-Band Direct Conversion Receiver With On-Chip A/D Converters,” in Symposium on VLSI Circuits Digest of Technical Papers, pp. 32-33, June 2000.

P5 J. Jussila, J. Ryynänen, K. Kivekäs, L. Sumanen, A. Pärssinen, K. Halonen, “A 22-mA 3.7dB NF Direct Conversion Receiver for 3G WCDMA,” ISSCC Digest of Technical Papers, pp. 284-285, Feb. 2001.

P6 J. Jussila, J. Ryynänen, K. Kivekäs, L. Sumanen, A. Pärssinen, K. Halonen, “A 22-mA 3.0-dB NF Direct Conversion Receiver for 3G WCDMA,” IEEE J. Solid-State Circuits, vol. 36, pp. 2025-2029, Dec. 2001.

P7 J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, “A Dual-Band RF Front-End for WCDMA and GSM Applications,” in Proceedings of Custom Integrated Circuits Conference, pp. 175-178, May 2000.

P8 J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, K. Halonen, “A Dual-Band RF Front-End for WCDMA and GSM Applications,” IEEE J. Solid-State Circuits, vol. 36, pp. 1198-1204, Aug. 2001.

P9 J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, K. Halonen, “A Single-Chip Multimode Receiver for GSM900, DCS1800, PCS1900, and WCDMA,” IEEE J. Solid-State Circuits, vol. 38, pp. 594-602, April 2003.

Other publications related to the topic:

P10 J. Ryynänen, K. Kivekäs, J. Jussila, A. Pärssinen, K. Halonen, “Direct Conversion Receiver for GSM900, DCS1800, PCS1900, and WCDMA,” IEEE ICECS Conference, pp. 942-945, Dec. 2003.

P11 M. Hotti, J. Kaukovuori, J. Ryynänen, K Kivekäs, J. Jussila, K. Halonen, “A Direct Conversion RF Front-End for 2-GHz WCDMA and 5.8-GHz WLAN Applications,” Radio Frequency Integrated Circuit (RFIC) Symposium, pp. 45-48, June 2003.

P12 J. Kaukovuori, M. Hotti, J. Ryynänen, J. Jussila, K. Halonen, “A Linearized 2-GHz SiGe Low Noise Amplifier for Direct Conversion Receiver,” IEEE International Symposium on Circuits and Systems (ISCAS), pp. 200-203, June 2003.

P13 K. Kivekäs, A. Pärssinen, J. Ryynänen, J. Jussila, K. Halonen, “Calibration Techniques of Active BiCMOS Mixers,” IEEE Journal of Solid-State Circuits, vol. 37, pp. 766-769. June 2002.

P14 J. Ryynänen, K. Kivekäs, A. Pärssinen, J. Jussila, K. Halonen, “RF Gain Control in Direct Conversion,” IEEE International Symposium on Circuits and Systems (ISCAS), Phoenix, pp. 117-120, May 2002.

P15 J. Ryynänen, K. Kivekäs, J. Heikkinen, J. Jussila, A. Pärssinen, K. Halonen, “Integrated RF Front-End for WCDMA and GSM 900,” IEEE European Conference on Circuit Theory and Design, Espoo, pp. 1-4, Aug. 2001.

1.3 Organization of the thesis

In Chapter 2, an introduction to the LNA requirements is given. These requirements depend on the system specifications, receiver architecture, and receiver partitioning. Therefore, it is important to understand the basic concepts and limitations. Furthermore, this helps the designer in implementing and combining multiple systems on a single chip. At the end of Chapter 2, a short introduction to the collected results from the realized circuits intended for multi-mode receivers is presented.

Chapter 3 describes the different LNA components and describes the limitations of these components. This chapter concentrates on the design of single-system LNAs. The main emphasis is on justifying why an inductively-degenerated LNA is chosen as the basis for all the experimental circuits. The LNAs in this thesis are targeted on DCRs. Thus, the design aspect of the LNA-mixer interface is also considered in this chapter.

Chapter 4 concentrates on the design of the multi-mode LNA. At the beginning of this chapter, the interface between the pre-select filter and the LNA is described, since it imposes limitations on LNA design. The input stage, load, and the LNA interface with the mixers are analyzed in detail. In addition, a description of recent multi-mode LNAs is given in this chapter.

Typically, receivers require some type of gain control. This gain control can be implanted in the baseband and/or in the RF front-end. If this variable gain is implemented in the RF front-end, it is typically placed in the LNA or in a separate gain control stage. Chapter 5 describes possible ways to implement this variable gain in the LNA. Several different gain control methods are described in this chapter. In addition, the effect of a variable gain in the RF front-end in continuous-time systems, such as WCDMA, is analyzed in this chapter.

Chapter 6 describes the experimental circuits. Two of the experimental circuits describe an RF front-end and a DCR which are intended for WCDMA applications. The last two describe an RF front-end for GSM900 and WCDMA systems and a DCR for GSM900, DCS1800, PCS1900, and WCDMA systems. The experimental circuits demonstrate the usability of the circuit structures described in the previous chapters.

2 Requirements for low-noise amplifiers in wireless communications

The integration of radio receivers has reached a state where the transceiver can mostly be implemented on a single chip. However, this integration level depends partly on the receiver architecture, which will be discussed in this chapter. Furthermore, the chosen architecture affects the LNA performance requirements. For example, output matching may be required, and the combination of different systems in multi-band receivers may not be allowed in the LNA. The emphasis of this chapter is to point out the challenges in LNA design in modern telecommunication systems and to justify some of the choices made in the circuits design. In addition, some of the system issues related to multi-mode receiver design are addressed at the end of the chapter.

2.1 Superheterodyne receiver

The block diagram of a superheterodyne receiver, with one intermediate frequency (IF) is shown in Figure 2.1. This architecture was introduced in its current form by Armstrong in 1918 [1]. It is well known, it has superior selectivity and sensitivity, and it is still widely used in different applications. In a superheterodyne receiver, the signal passes through the LNA, which is usually connected and matched to filters at both sides. The pre-select filter preceding the LNA passes the whole reception band for the desired system and attenuates signals outside this band. The following filter is required for image noise filtering because the LNA frequency response is not usually selective enough to suppress the noise at the image band. Hence, without this filter, the mixer[1] would downconvert the noise from the image to the first IF. In addition, this filter may be used to filter out possible out-of-band tones that could corrupt reception. As an alternative, this filter can be replaced with an image-reject downconverter [2], [3]. However, this requires additional hardware and good matching between different components in order to achieve high image suppression. After downconversion, a channel-select filter limits the spectrum for the following stages to the desired signal by attenuating those signals which are out-of-channel. Hence, the linearity of the following stages is relaxed. The channel-select filter is usually an external passive surface acoustic wave (SAW) filter, which is not an adjustable filter. Therefore, the first VCO must have a frequency which is adjustable for the whole reception band. Furthermore, the first IF must be higher than half of the reception bandwidth. Hence, the image is then always outside the reception band. The channel-select filter is followed by a variable-gain amplifier and demodulator, which divides the signal into I and Q branches.

This basic concept may be altered to achieve block specifications that are sufficient for the targeted applications. A second IF stage may be used, which performs part of the channel filtering and interference cancellation. However, the use of a second IF may increase costs, and, because of the third LO, frequency planning becomes more difficult. Obviously, the channel filtering and gain may be distributed among different blocks in order to achieve an adequate performance. This distribution of gain and filtering is the reason why this architecture gives a

[1] In the case of a superheterodyne mixer, the single sideband (SSB) noise figure is used. The downconverted signal is only on one sideband, while the noise is downconverted from both sidebands.

good performance. The main reason why this architecture is currently unpopular is that it requires expensive external components. The pre-select, image, and channel-select filters cannot be integrated with current technologies. Thus, the size and cost of the receiver increase. Therefore, other architectures, which can be integrated on a single chip, have been widely explored. The suitability of the superheterodyne architecture for multi-mode receivers is discussed in Section 2.6.

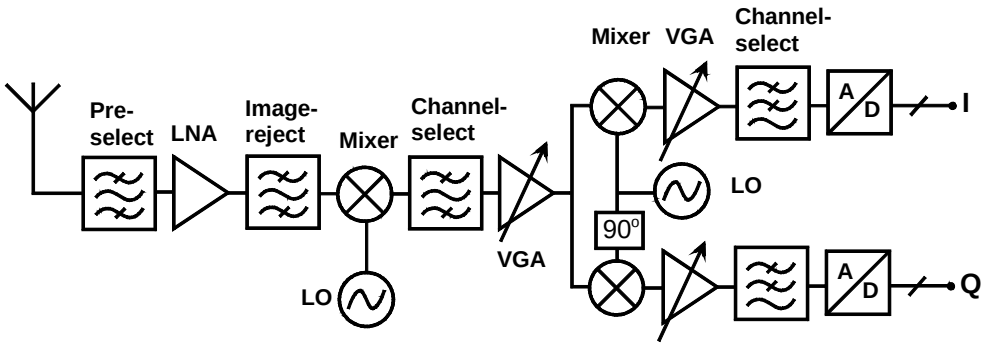

Figure 2.1. Block diagram of a superheterodyne receiver.

2.2 Direct-conversion receiver

The direct-conversion architecture, shown in Figure 2.2, is well suited for single-chip integration. This architecture, which is also known as zero-IF or homodyne, converts the center of the desired RF signal directly to DC in the first mixers. The first publications on homodyne receivers, using a single vacuum tube, were published as early as 1924. However, the first practical implementations were published in 1947 [4]. The direct-conversion receiver suffers from special problems that do not appear in superheterodyne receivers. These problems limited the use of DCRs until the 1980s and 1990s, when they were first applied in paging and digital cellular receivers, respectively [5].

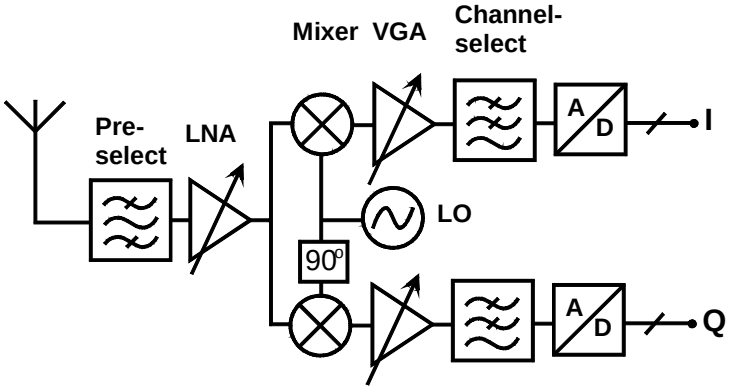

Figure 2.2. Block diagram of a direct-conversion receiver.

A typical DCR includes a pre-select filter, an LNA, and quadrature mixers, followed by channel-select filters, variable-gain amplifiers, and A/D converters. The pre-select filter is required prior to the LNA in order to attenuate out-of-band signals, as in the superheterodyne receiver, because of poor front-end selectivity. The image filter after the LNA is not required

because the desired signal is on both side bands. Obviously, this relaxes the design of the LNA-mixer interface because there is no need to drive external impedance, for example, 50Ω. The quadrature I and Q channels are necessary while receiving typical phase- and frequency-modulated signals, because the two sidebands of the RF spectrum contain different information and result in irreversible corruption if they overlap each other without being separated into two phases [6]. Channel filtering in DCRs is performed with lowpass filters, which can be implemented with on-chip active circuits. The amplification and channel filtering can be distributed across the baseband chain to improve the performance of the receiver.

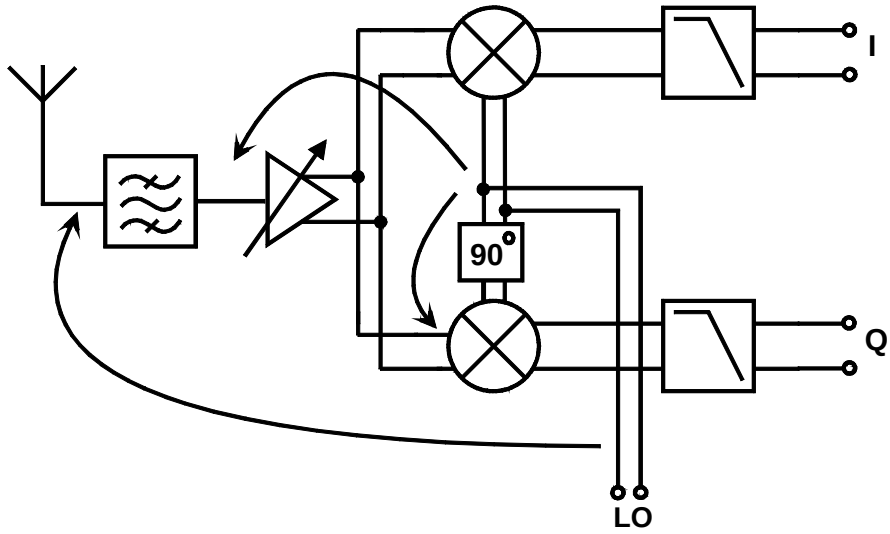

Figure 2.3. LO leakage in DCRs.

An extensive study of the advantages and challenges of the DCR can be found in [6] and [7]. The major challenge in DCRs, compared to the superheterodyne receiver, arises from the LO signal, which is located at the same frequency as the desired signal. Thus, for example, the center of the desired signal is downconverted to DC. Figure 2.3 illustrates these problems arising from LO leakage. The leaked LO is on the passband of the pre-select filter and antenna. Hence, it can radiate out and may appear as an in-band interferer to other nearby receivers in the same frequency band. The maximum emission levels allowed are limited by different organizations, such as ITU-R. In addition, LO leakage causes DC offsets because of selfmixing. The LO signal can couple to different nodes at the receiver through capacitive and substrate coupling and, if the LO signal is provided externally, through bond wire coupling. The coupled LO signal is then mixed down to DC. In general, a selfmixed LO causes static DC offset. However, when this LO signal leaks to the antenna and the radiated LO signal is reflected back from moving objects, it causes dynamic or time-variant DC offsets. A similar time-variant DC offset can occur if the RF input signal leaks to the mixer LO port and selfmixes to DC. Furthermore, all blocks create static DC offsets because of random and systematic device mismatches. The DC offset can corrupt the reception because a DC offset of only a few mV at the mixer output saturates the receiver if the typical voltage gain from 40dB to 70dB is implemented at the baseband. The DC offset can be removed in the baseband using different approaches. For example, it can be filtered out after the mixers using a highpass filter, such as an AC coupling. However, the highpass filter removes part of the signal and, therefore, the -3dB corner frequency must be sufficiently low compared to the signal bandwidth. The low -3dB corner frequency of the highpass filter corresponds to a large time constant. Hence, the

highpass filter may require a large chip area. A detailed discussion of issues relating to the baseband requirements for DCRs can be found, in [8].

Direct downconversion also has limitations which affect the whole channel and not only DC. For example, if two interferers, $A_1\cos(\omega_1 t)$ and $A_2\cos(\omega_2 t)$, are fed into a device which has a second-order nonlinearity, $y(t)=\alpha_1 x(t)+\alpha_2 x^2(t)$, then y(t) results a term $\alpha_2 A_1 A_2 \cos(\omega_1-\omega_2)t$. Hence, second-order nonlinearity creates low-frequency interference if $\omega_1 \approx \omega_2$. If the RF signal has amplitude modulation (AM), this AM creates interference to the baseband. This phenomenon has only a minor effect on LNA design, because the interference created by the LNA is mostly upconverted in the mixers. Hence, issues related to this phenomenon are mostly left out of this thesis. The second problem is flicker noise. It can corrupt the reception because the signal is already converted to DC after the LNA. Flicker noise can cause severe degradation in noise characteristics, especially at smaller RF front-end gains, but always has significant impact in baseband design. Flicker noise must already be considered at the quadrature mixers and its effect on total receiver NF compared to thermal noise can be calculated as [9]

$$\overline{V_n^2} = \int_{f_{HPF}}^{f_{flicker}} \frac{K}{f} df + \int_{f_{HPF}}^{B_n} S_{th} df = K \ln\left(\frac{f_{flicker}}{f_{HPF}}\right) + (B_n - f_{HPF}) S_{th} \,, \qquad (2.\ 1)$$

where f_{HPF} is the cutoff frequency of the highpass filter, $f_{flicker}$ is the corner frequency of the 1/f-noise, B_n is the system noise bandwidth, and S_{th} is the thermal noise floor. Constant $K=f_{flicker}S_{th}$ because at the flicker noise corner frequency, the flicker noise is equal to the thermal noise, as illustrated in Figure 2.4. Figure 2.5 shows how much flicker noise increases the total system noise figure. In the simulation the corner frequency of the highpass filter f_{HPF} is set to 0.1% of system noise bandwidth. According to [6] this is the maximum highpass filter corner frequency at which the signal degradation is negligible. As can be seen with the wider bandwidths, the effect of the flicker noise is reduced. Thus, a technology with a higher flicker noise can be used in wideband systems.

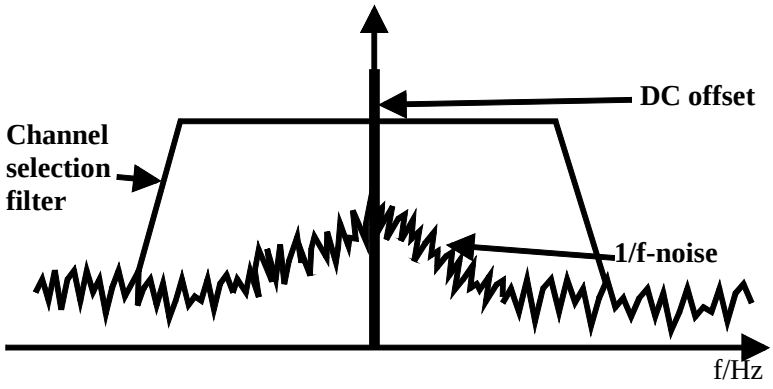

Figure 2.4. Downconverted spectrum in DCR.

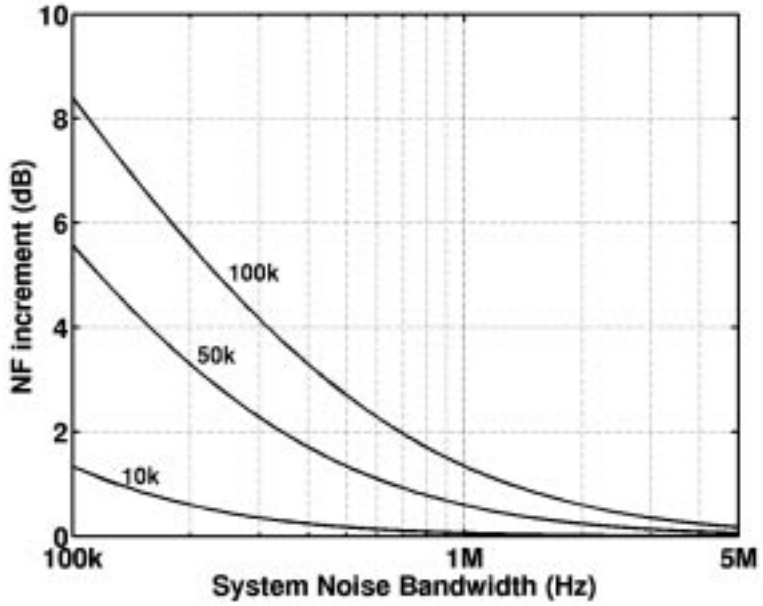

Figure 2.5. The system noise figure increment with different flicker noise corners.

2.3 Other architectures

Figure 2.6 illustrates the block diagram of a low-IF receiver. The low-IF receiver differs from the previous architectures in that the first IF is placed above DC but lower than half of the system reception bandwidth. The low-IF architecture tries to circumvent the problems related to previous architectures. In this receiver the problems related to DCR DC offsets are mitigated because there is no signal information at around DC. Thus, DC offsets can be filtered without signal information being removed. However, matching between the I and Q branches is critical if sufficient image rejection is to be achieved.

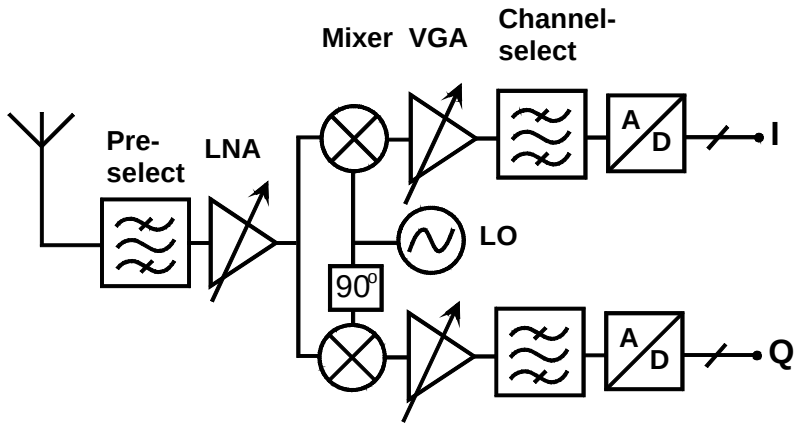

Figure 2.6. Block diagram of a low-IF receiver.

A detailed description of, and comparison between, low-IF and other architectures, such as a wide-band IF receiver and direct digital receiver, can be found in [10] and [11]. In general, the other architectures set similar performance requirements for the LNA. The main differences between the different architectures, as regards LNA design, are the output load, reverse isolation, and the different spurious signals on-chip. The load can be an external filter or an on-chip device. For example, if the load is not an external filter, the interface between the LNA and mixer can be altered to optimize receiver performance. As a result of spurious emissions, the reverse isolation of the LNA is important if the LO is on the reception band of the receiver. Furthermore, it affects the DC offsets, as previously mentioned. The on-chip spurious signals can couple to the LNA input and thus can corrupt the received signal. These phenomena will be discussed in the following chapters.

2.4 Wireless telecommunication systems

Telecommunication systems were originally developed mostly for voice applications and used analog signal processing. However, in modern systems, the signal processing is mostly performed in the digital domain. Furthermore, in the last few years, the main design driver has become data rather than the voice. In Table 2.1, the key parameters of several existing standards are collected. The reception bands for these systems are usually located in the UHF band (i.e. between 0.3-3GHz). However, due to the limited spectrum in this band, systems such as WLAN 802.11a are operating in the SHF band (3-30GHz). In addition, it can be seen that the trend in system development has been to increase channel bandwidths in order to make communication at higher data rates possible.

Table 2.1. Wireless telecommunication systems.

	Main Application	Access method	Duplexing	Reception Bands (BS and MS) [MHz]	Channel spacing [kHz]	Sensitivity Level [dBm]
WCDMA	Data, Voice	DS-CDMA	FDD	1920-1980 2110-2170	5000	-117*)
GSM900	Voice	TDMA	TDD/FDD	880-915 925-960	200	-102**)
DCS1800	Voice	TDMA	TDD/FDD	1710-1785 1805-1880	200	-102**)
PCS1900	Voice	TDMA	TDD/FDD	1850-1910 1930-1990	200	-102**)
WLAN 802.11b	Data	DS-CDMA	TDD	2400-2483.5***)	22000	-76
WLAN 802.11a	Data	OFDM	TDD	5150-5250 5250-5350 5725-5825	20000	-82/-65****)
GPS	Location	-	-	1575.42	-	-136
Bluetooth	Data	FH-CDMA	TDD	2400-2483.5	1000	-70

*) user equipment
**) for small MS
***) national differences exist
****) for 6Mbits/s and 54 Mbits/s data rate

2.5 Design parameters for low-noise amplifiers

In general, the LNA should amplify the desired signal without adding noise and without distorting the desired signal. These LNA requirements are determined during the receiver partitioning, which is based on the system specifications. The system specifications determine the acceptable figures of merit for the whole receiver. From these requirements, the specifications for the analog part must be determined separately. Methods for estimating analog receiver performance can be found in the literature: [9], [11], [12]. However, in order to have accurate requirements for the analog receiver, a good knowledge of the digital signal processing, combined with extensive system simulations, is usually required. Therefore, since this is not within the scope of this thesis, it is mostly omitted. After the performance requirements for the analog receiver are determined, the designers must be able to divide and calculate the specifications for individual blocks. This section describes the essential parameters needed in LNA design and explains how these can be calculated from the analog receiver requirements. Several parts of this section can be used for all receiver architectures, but the main focus is on LNAs for DCRs. Furthermore, some requirements for GSM and WCDMA systems are discussed, because the receivers implemented in this thesis are targeted for these systems.

2.5.1 Sensitivity and noise figure

The sensitivity level determines the minimum signal, which has to be detected with a sufficient signal quality, typically determined either as bit or frame error rate (BER/FER). This level can be determined as

$$S_{sensitivity} = -174dBm + 10\log(B) + \frac{S_{\min}}{N_{\min}} + NF, \tag{2. 2}$$

where -174dBm is the available noise power from the source at a temperature of 290K i.e. kT, B is the channel bandwidth, S_{min}/N_{min} (or SNR_{min}) is the minimum signal-to-noise ratio required for signal detection with an acceptable BER, and the NF is the noise figure for the receiver. Thus the NF of the receiver is

$$NF = S_{sensitivity} + 174dBm - 10\log(B) - \frac{S_{\min}}{N_{\min}}. \tag{2. 3}$$

The sensitivity level for the GSM900, DCS1800, and PCS1900 is –102dBm, B is 200kHz and SNR_{min} is 9dB. Thus, the maximum NF is 10dB. This calculation does not assume any implementation margin. An implementation margin of 1dB is assumed for the chosen detector in [12]. Hence, the required receiver NF is set to 9dB. The calculation of NF in the WCDMA system is not as straightforward as in GSM. The WCDMA system uses spread-spectrum (SS) technology. In the spread-spectrum system, the transmitted data is multiplied with a code that is independent of the data and has a much higher bandwidth. This code is a pseudorandom sequence and has maximized orthogonality to other known codes used by different users in the same channel. In the receiver, the spread-spectrum signal is multiplied with the same in-phase code, and the narrow-band information is recovered. The important terms of the spread-spectrum system are the spreading factor (SF) and the spreading gain (SG). SF describes the ratio of the information data rate (represented by the bit duration T_{bit}) to the rate of the spreading code (represented by chip duration T_{chip})[11]

$$SF = \frac{T_{bit}}{T_{chip}} \tag{2. 4}$$

The SG is defined from the SF as

$$SG[dB] = 10\log(SF) \tag{2. 5}$$

Hence, an additional gain resulting from the spread-spectrum (SS) technology must be taken into account when receiver sensitivity is being calculated. In [11] and [13], the total gain from coding (CG) and spreading (SG) is 25dB, the implementation margin at the digital baseband is 2dB, and the required bit energy to interference power spectral density (PSD) ratio $E_{b,req}/I$ is 5dB. With these values the required S/N before despreading becomes

$$\frac{S}{N} = \frac{E_{b,reg}}{I} + IL_{bb} - G_{spread,coding} = 5dB + 2dB - 25dB = -18dB \tag{2. 6}$$

Hence, the receiver signal-to-noise ratio is negative before despreading. The sensitivity level in WCDMA specifications is –117dBm. From Equations (2.3) and (2.6) the required NF for WCDMA becomes 9dB.

The NF of the whole receiver describes how much the receiver can deteriorate the signal-to-noise-ratio of the signal received. It is defined as

$$NF = 10 \cdot \log\left(\frac{\frac{S_{in}}{N_{in}}}{\frac{S_{out}}{N_{out}}} \right), \tag{2. 7}$$

where $S_{in,}$ $S_{out,}$ N_{in} and N_{out} are the signal and noise powers at the input and output of the receiver, respectively. The NF of the different blocks can be calculated using different approaches. The traditional way is to use Friis' formula [14]

$$F_{tot} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + ... + \frac{F_n - 1}{G_1 \cdots G_{n-1}} \tag{2. 8}$$

$$NF_{tot} = 10\log(F_{tot}), \tag{2. 9}$$

where F_n and G_n are the noise factor and available power gain of the nth block, respectively. Friis' formula shows that the noise contribution of each block is reduced when the gain of the preceding stages is increased. Hence, the most dominant blocks in the case of the NF are the first blocks. Figure 2.7 shows the cascaded receiver stages in Friis' equation. For each block, the NF and available power gain, G, are characterized. The available power gain is defined as the ratio of the power delivered to a conjugate-matched load ($V_{outn}^2/4R_{outn}$) and the power available from the source delivered to a conjugate-matched circuit ($V_s^2/4R_s$). Friis' formula is especially useful if the receiver employs various off-the-shelf building blocks that are characterized independently by manufacturers [15]. Thus, this formula is useful for the superheterodyne architecture because it has off-chip components, which use defined characteristic impedances.

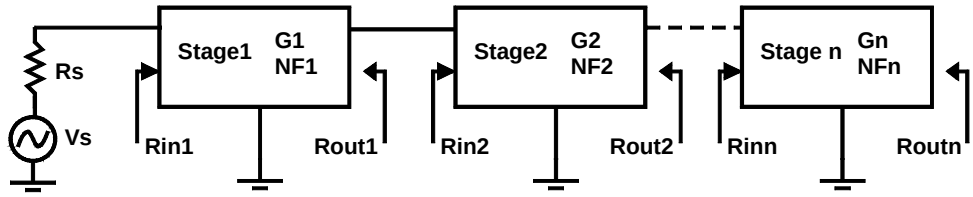

Figure 2.7. Cascaded receiver stages.

In DCR, there is typically no need to drive any off-chip circuits, such as external filters. Thus, no matching to a certain impedance, such as 50Ω, between different blocks is required. For example, the load of the LNA is usually the mixer input, which can be modeled with lumped elements. Furthermore, the integrated filters can be designed to have an appropriate impedance level. The signal is typically transferred in voltage mode, and in a ideal case, the zero impedance source drives the infinite input impedance of the following block. Therefore, the conversion gains and noise levels should be defined with voltages and impedance levels rather than power throughout the receiver [10]. Hence, Friis' formula is not useful in the form in which it is presented. In [10], Friis' formula is presented using the voltage gains of different blocks as

$$F_{tot} = F_1 + \frac{F_2 - 1}{A_{0,1}^2 A_{v1}^2} + \frac{F_3 - 1}{A_{0,1}^2 A_{1,2}^2 A_{v1}^2 A_{v2}^2} + ... + \frac{F_n}{(A_{0,1}^2 \cdots A_{n-2,n-1}^2)(A_{v1}^2 \cdots A_{vn-1}^2)}, \qquad (2.10)$$

where A_{vn} is the voltage gain of the nth stage to open load and $A_{n\text{-}2,n\text{-}1}$ transform the impedance between different stages as

$$A_{n-2,n-1} = \frac{Z_{in,n-1}}{Z_{in,n-1} + Z_{out,n-2}}, \qquad (2.11)$$

where Z_{in} and Z_{out} are the input and output impedances of the corresponding stages. In addition, a rather similar approach can be found in [16], where the noise factor in Friis' formula is also translated to noise voltage. In both formulas, it is assumed that the noise from each individual block follows the gain behavior if the impedance levels between different blocks are altered, i.e. the noise behavior of different blocks is not altered. If it is assumed that the input impedance of the following stage is much higher than the output impedance of the preceding stage, which is usually the case in DCRs, the mismatch term $A_{n\text{-}2,n\text{-}1}$ can be ignored. Therefore, these equations give a good basis for NF partitioning in system design. Figure 2.8 and Figure 2.9 show the effect of the LNA gain on the NF of the whole receiver ($A_{n\text{-}2,n\text{-}1}$ is set to 1). In Figure 2.8, the curves are shown with three different LNA noise figures and in Figure 2.9 with three different NFs for the stages following LNA. As discussed earlier, the receiver NF should be approximately 9dB. The loss of the pre-select filter preceding the LNA must be taken into account. The loss of this filter is approximately 3dB in mobile terminals [12], [13], [17]. Furthermore, this filter is passive. Hence, the filter NF is equal to its loss and the receiver NF without this filter becomes 6dB. Leaving some implementation margin, it can be roughly estimated from these numbers that the LNA voltage gain should be over 15 dB and NF below 2 dB in order to meet the 3-5-dB NF requirement of the receiver. In addition, it must be noted that when the baseband circuitry for DCRs is being designed, the NF of the baseband circuitry may have a strong effect on the total NF of the receiver because of the moderate gain of the RF front-end.

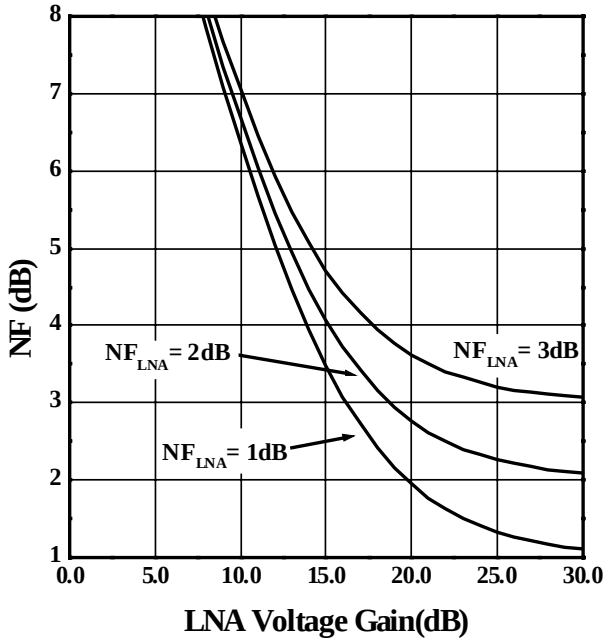

Figure 2.8. NF of the receiver with three different NF values for the LNA. The DSB NF of the stages following the LNA is 15 dB.

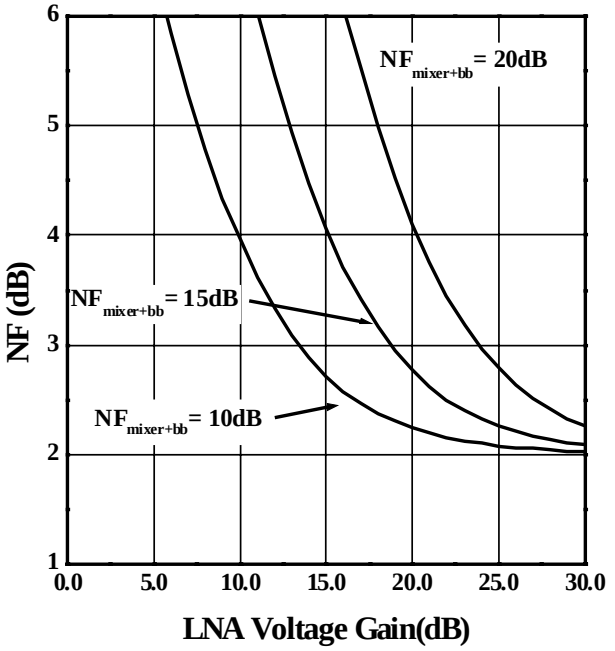

Figure 2.9. NF of the receiver with three different DSB NF values for the stages following the LNA. The NF of the LNA is 2 dB.

In circuit-level design, a slightly different approach is suggested in this thesis for DCRs in order to take into account the effects of the interface between different blocks. A noise factor for a single block can be defined as

$$F = \frac{SNR_{in}}{SNR_{out}} = \frac{v_s / 4kTBR_s}{v_{out}^2 / e_{nout}^2} = \frac{\overline{e_{nout}^2}}{4kTBR_s \left(\frac{v_{out}}{v_s} \right)^2} , \quad (2.12)$$

where v_s is the source voltage, v_{out} and e_{nout} are the total signal and noise voltages at the output, k is Boltzman's constant, B is the bandwidth, and R_s is the source resistance [15]. In RF circuits, the noise is determined for the 1Hz bandwidth at a given frequency and known as spot-noise, which is also the case in this thesis if not otherwise mentioned. In LNA design, this is a useful formula, since the source impedance of the LNA is fixed and accurately defined. The NF in the LNA case can be defined to infinite load impedance and estimate the mismatch term. However, in order to get an accurate simulation result the mismatch term can be taken into account to get by using the following stage as a load and defining it as noiseless. Thus, an accurate load gives accurate gain and does not affect the LNA output noise. The gain of the LNA is usually frequency-dependent and includes reactive components. Thus, for example, the capacitive input of the mixers changes the LNA frequency response. In practice, similar NF modeling of other blocks in circuit simulators is not necessary because the impedance level at the output of the previous stage is one of the design parameters and, as already mentioned usually contains reactive components. Hence, when the source impedance is not well defined, the input-referred noise voltage is a useful a noise definition. The input referred noise must be determined in this case by simulating the output noise, when the block is driven from the impedance of the previous stage, which is defined as noiseless, and dividing it by the voltage gain of the stage

$$e_{nin}^2 = \frac{e_{nout}^2}{m_c \left(\frac{v_{out}}{v_s} \right)^2} , \quad (2.13)$$

where the term m_c represents the frequency conversion term. The frequency conversion term is 1 with blocks that have no frequency conversion. For blocks with mixing phenomena this term is 1 for mixers defined with an SSB noise figure and 2 for mixers with a DSB noise figure [16]. Thus, a factor of 2 must be used for direct-conversion mixers. For example, the F for two cascaded blocks, where the input impedance of the first block is accurately defined, can now be calculated using Equation (2.12) by replacing e_{nout} with

$$e_{nout}^2 = e_{nout,Rs}^2 + e_{nout,1}^2 + e_{nin,2}^2 . \quad (2.14)$$

$e_{nout,Rs}$ and $e_{nout,1}$ are the total output noise voltages from the source and the first block, and $e_{nin,2}$ is the input-referred noise of the second stage. For multiple stages where the first block is accurately defined the total output noise is

$$e_{nout}^2 = e_{nout,Rs}^2 + e_{nout,1}^2 + \frac{e_{nout2}^2}{m_{c2}\left(\frac{v_{out2}}{v_{in2}}\right)^2} + ... + \frac{e_{noutn}^2}{\prod_{i=2}^{n}\left[m_{cn}\left(\frac{v_{outn}}{v_{inn}}\right)^2\right]}, \quad (2.15)$$

where e_{noutn} is the output noise voltage of the n^{th} stage, m_c is the conversion term of the nth stage and v_{out} and v_{in} are the signal voltages at the input and output of the corresponding stage, respectively. Equations (2.12) and (2.15) are very useful in receivers where only the driving impedance of the first stage is defined. Now, the NF can be defined for the LNA only or the total NF of the receiver can be determined using the output noise voltages of the block without determining the Fs for each block, which may be difficult for the reason described above.

2.5.2 Linearity

The receiver must be able to detect the desired signal in the presence of other interfering signals. The signal powers at the receiver input may vary from -110dBm to 0dBm. These signals are partially filtered out by the pre-select filter, but the signals at the reception band pass through the filter. Besides that, the transmitter signal and other signals used in the transceiver may leak to the LNA input. In the worst case, these signals and their mixing products can corrupt the reception of the desired signal by desensitizing some particular receiver block. Usually, the linearity of the receiver is characterized using the gain compression and third-order input intercept point (IIP3). In addition, the second-order input intercept point (IIP2) must be characterized for some architectures, such as DCRs, as previously mentioned.

2.5.2.1 Gain compression and harmonic distortion

The gain compression determines how large an input signal can be accepted at the receiver input. This can easily be determined with a single-tone analysis. As the power is increased, the gain of most circuits decreases, as shown in Figure 2.10.

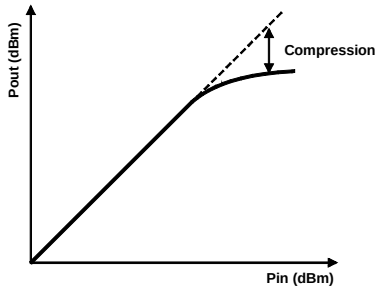

Figure 2.10. Definition of gain compression.

The gain compression can be calculated using the following well-known formulas [15]. The first three terms of a nonlinear memoryless and time-variant system are

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) . \quad (2.16)$$

If $A\cos(\omega t)$ is used as an input signal, the output signal becomes

$$y(t) = \frac{\alpha_2 A^2}{2} + \left(\alpha_1 + \frac{3\alpha_3 A^3}{4} \right) \cos(\omega t) + \frac{\alpha_2 A^2}{2} \cos(2\omega t) + \frac{\alpha_3 A^3}{4} \cos(3\omega t). \qquad (2.17)$$

It can be seen that the term at the frequency of interest (i.e. the fundamental frequency) also depends on the third-order term. Thus, the output signal is decreased when α_3 has an opposite sign to α_1. In RF circuits, the gain compression is defined as the "-1dB compression point", which is the point where the gain is decreased by 1dB from the gain at small signal levels. In receivers, the compression point is usually defined at the input (ICP) and in transmitters at the output (OCP). Furthermore, it can be seen from Equation (2.17) that the output includes the harmonics of the signal. Using Equation (2.17) the harmonic distortion, which is the magnitude of the ratio between the signal at the nth frequency and fundamental frequency, can be defined.

2.5.2.2 Third- and second-order intercept points

The characterization of the RF circuits with harmonic distortion is not practical, since RF circuits are usually frequency-dependent and the harmonic components fall far away at the stopband of the circuit. A more useful characterization for RF circuits is to use the intermodulation products. Instead of using the single-tone input in the system defined in Equation (2.16), two signals at different frequencies ($A\cos(\omega_1 t)+B\cos(\omega_2 t)$) are used as input signals. Thus it can be calculated that the following signals appear at the system output:

$$\begin{aligned}
y(t) &= \frac{1}{2}\alpha_2 (A^2 + B^2) + \alpha_1 A \cos(\omega_1 t) + \\
&\alpha_3 \left(\frac{3}{4} A^3 + \frac{3}{2} A B^2 \right) \cos(\omega_1 t) + \alpha_1 B \cos(\omega_2 t) + \alpha_3 \left(\frac{3}{4} B^3 + \frac{3}{2} A^2 B \right) \cos(\omega_2 t) + \\
&\frac{1}{2}\alpha_2 A^2 \cos(2\omega_1 t) + \frac{1}{2}\alpha_2 B^2 \cos(2\omega_2 t) + \\
&\frac{1}{4}\alpha_3 A^3 \cos(3\omega_1 t) + \frac{1}{4}\alpha_3 B^3 \cos(3\omega_2 t) + \\
&\alpha_2 AB \cos(\omega_1 - \omega_2)t + \alpha_2 AB \cos(\omega_1 + \omega_2)t + \\
&\frac{3}{4}\alpha_3 A^2 B \cos(2\omega_1 - \omega_2)t + \frac{3}{4}\alpha_3 AB^2 \cos(2\omega_2 - \omega_1)t + \\
&\frac{3}{4}\alpha_3 A^2 B \cos(2\omega_1 + \omega_2)t + \frac{3}{4}\alpha_3 AB^2 \cos(2\omega_2 + \omega_1)t.
\end{aligned} \qquad (2.18)$$

Hence, the output signals include the signal, harmonics, and intermodulation components. The most harmful intermodulation products in LNA design are at the frequencies $2f_2$-f_1 and $2f_1$-f_2. Figure 2.11 illustrates the problem arising from these intermodulation distortion products. Two large unwanted signals occur at the frequencies (f1, f2) and the harmful intermodulation product falls directly on the same frequency as the small desired signal. Obviously, the two unwanted input signals are most harmful if the signals are placed at the passband of the pre-select filter.

A test resembling the situation described above can be found, for example, in GSM and WCDMA receiver specifications. In the GSM specifications, the minimum desired signal, which must be correctly demodulated with BER < 10^{-3}, is 3dB above the sensitivity level. The two signals, which are located 800kHz and 1600kHz from the desired signal, have a power of -49dBm. In addition, the signal at 800kHz is a continuous sine wave and the 1600kHz signal is

modulated. This information can be used in a system simulator to achieve the receiver specification. However, in practice, both of these signals must be continuous time sine waves in circuit simulators. This is sufficient for basic estimations and further information can be found in [18]. The receiver linearity for these signals can now be specified using the third-order intercept point. Again, in receivers, the intercept point is usually referred to the input (IIP3) and in transmitters to the output (OIP3). The intercept point is determined as the crossing point where the fundamental and third-order terms have equal power, as illustrated in Figure 2.12. The third-order intercept point IP3 must be defined when the device is operating in a weakly nonlinear area (i.e. the input power is far below the compression point). As illustrated in Figure 2.12, the fundamental and third-order terms have different slopes at higher input power levels. Furthermore, the behavior of the third-order term at high signal levels is not always compressive, as illustrated.

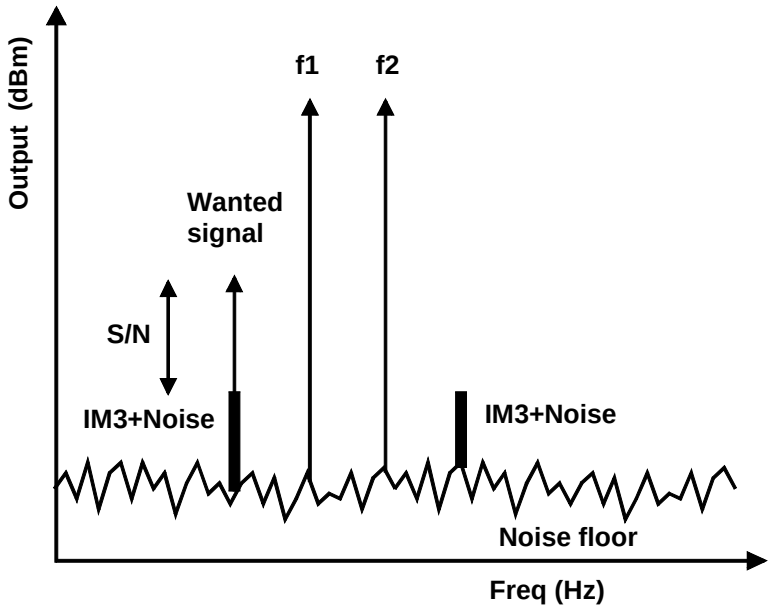

Figure 2.11. The effect of intermodulation on the desired signal in reception.

The IIP3 of the device can be calculated from the information given above as

$$IIP3 = \frac{3}{2}P_{out} - \frac{1}{2}P_{imd3} - G = P_{in} + \frac{\Delta P_3}{2}, \qquad (2.19)$$

where P_{out} and P_{in} are the input and output powers (dBm), P_{imd3} is the third-order intermodulation product (dBm) at the output, and ΔP_3 is the difference between the fundamental and intermodulation products (dBc). The power gain (G) can be replaced with the voltage gain (A_v) in Equation (2.19) [10]. The IIP3 of the GSM receiver can be calculated using the signals given earlier in this section. The S/N of the receiver must be 9dB for proper reception. Hence, in order for the signal to be detected the input-referred noise plus intermodulation must be 9dB below the desired signal, which has a power of –99dBm. The input referred noise plus intermodulation must be below –108dBm. If the receiver is designed for the maximum NF (10dB), the noise level is at –111dBm. Thus, when the third-order intermodulation component does not correlate with the noise, the third-order component must be below –111dBm in order

to meet the specifications. Using Equation (2.19) the IIP3 of the GSM receiver becomes –18dBm. A similar test can be found in the WCDMA specifications, where the desired signal is 3dB above the sensitivity level (-114dBm) and the two tones at 10MHz and 20MHz offset have a power of –46dBm. Again, one signal is a continuous sine wave and the other a modulated channel. Using a similar approach as in GSM, it can be calculated that the sum of the input-referred noise and intermodulation component must be below –96dBm with a 25dB coding and spreading gain. Thus, the third-order intermodulation must be below –99dBm, resulting that the IIP3 of a WCDMA receiver is –19.5dBm. These are both estimates of the actual IIP3 requirements. For example, in [13] the following assumptions were made for WCDMA in order to achieve more accurate results. The sum of noise and interference power is divided, assuming the following distribution between different components; noise, 50% of power (-3dB), intermodulation, 15% of power (-8dB), CW interferer's blocking effect, 15% of power (-8dB), modulated interferer's blocking effect, 15% of power (-8dB), and oscillator noise, 5% of power. Furthermore, second-order distortion products are ignored. Thus, the IIP3 requirement increases to –17dBm. In [11], it is also stated that the previous presentation does not take into account the modulated signal and that the limited orthogonality between the signals received may alter the Gaussian noise distribution model. Thus, for accurate results system simulators such as HP ADS are recommended.

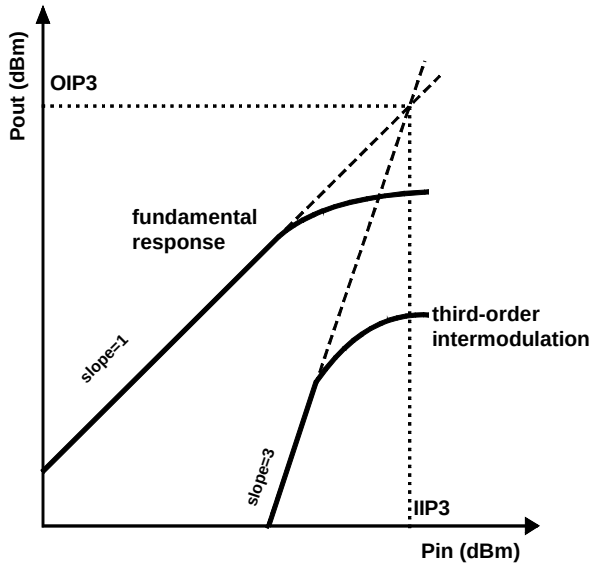

Figure 2.12. Behavior of fundamental and third-order components in an intermodulation test.

The IIP3 requirements for the receiver blocks can be calculated using the following equation. The cascaded IIP3 of a coherent receiver is

$$\frac{1}{iip3_{tot}} = \frac{1}{iip3_1} + \frac{G_1}{iip3_2} + \ldots + \frac{\prod_{i=1}^{n-1} G_i}{iip3_n}, \qquad (2.20)$$

where $iip3_n$ is the iip3 (magnitude) of the nth block and G_n is the power gain (magnitude) of the nth block. This equation assumes that spurious signals are in the same phase, which gives a

worst-case assumption for the IIP3 result. The power gain in Equation (2.20) can be replaced with the square of the voltage gain (A_v^2) as in the noise figure calculations. In addition, to get accurate results, gain should be determined using correct source and load impedances. Thus, as in NF calculations, no mismatch term is required. However, the source and load impedances of the designed stage should be linear in order not to affect the results. Therefore, it may be necessary to model these impedances with linear components, which may be difficult in some cases. Hence, the IIP3 of cascaded blocks should be checked for several blocks in the final simulations. The IIP3 of passive filters is almost infinite and therefore only the gain of these stages need be taken into account when determining cascaded IIP3. In addition, the passive channel selection filter used in some receiver architectures filters out the unwanted tones. Therefore, the stages after this filter can be neglected. In DCRs the channel-select filter is an active structure and filtering may be merged with the amplification. This leads to finite IIP3 in the filter and therefore it must be taken into account in the calculations. Figure 2.13 and Figure 2.14 illustrate the receiver IIP3 with three different LNA intercept points, and with three intercept points of the stages following the LNA. When a sufficient IIP3 is being determined the loss of the pre-select filter must be taken into account, which decreases the IIP3 requirements by the amount of its loss for the following receiver. For example, from Figure 2.13 and 2.15 it can be roughly estimated that the voltage gain of the LNA should be below 25 dB in order to have a sufficient IIP3 for WCDMA and GSM.

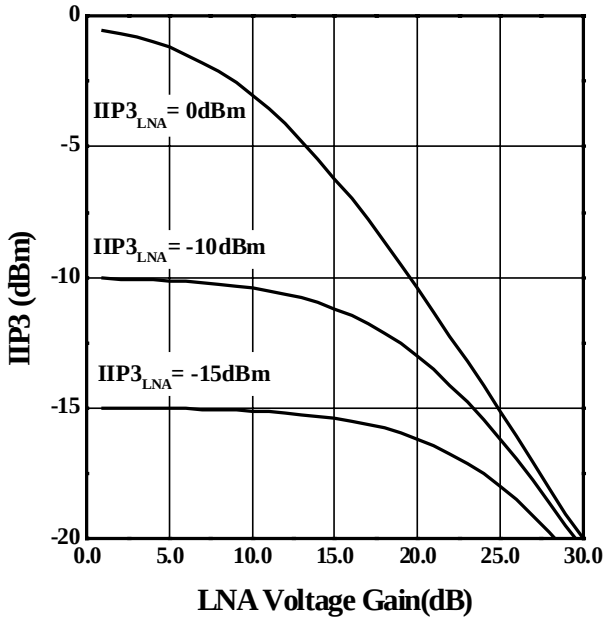

Figure 2.13. IIP3 of the receiver with three different IIP3 values for the LNA. The IIP3 for the stages following the LNA is +10 dBm in Eq. (2.20).

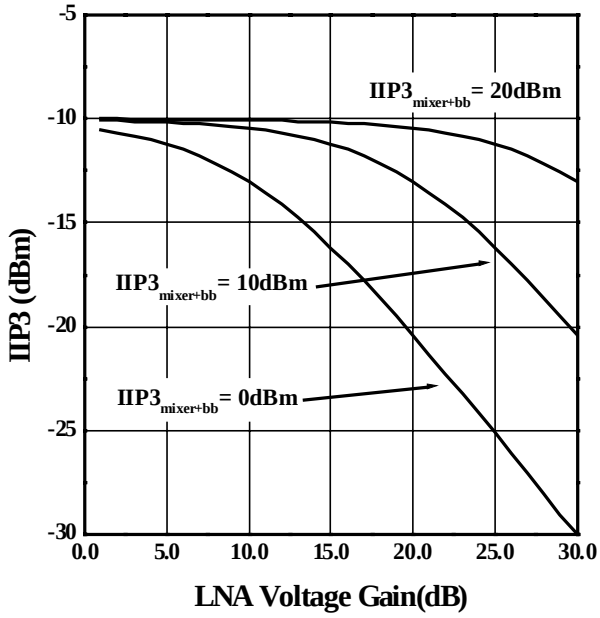

Figure 2.14. IIP3 of the receiver with three different IIP3 values for the stages following the LNA. The IIP3 of the LNA is set to -10 dBm in this case.

In the WCDMA system, the IIP3 requirements might be limited by other factors than the intermodulation test. The first issue which should be taken into account is the transmitter, which may transmit during reception in UTRA/FDD. The transmitter signal leaks to the LNA input as a result of finite out-of-band filtering in the pre-select filter and finite PCB isolation. The leaked transmitter signal can create an in-channel interferer if a blocker is located between the transmit and reception bands which maps directly on the wanted signal, illustrated in Figure 2.15. Both of the interferers have different powers that should be used in the IIP3 test. An equivalent power to be used in the two-tone test can be derived from Equation (2.18). Depending on whether the IM3 result is above or below the two tones, the equivalent power is

$$\begin{aligned} &tone\,(2\omega_2-\omega_1);\quad \frac{3}{4}\alpha_3 AB^2=\frac{3}{4}\alpha_3 C^3 \\ &tone\,(2\omega_1-\omega_2);\quad \frac{3}{4}\alpha_3 A^2 B=\frac{3}{4}\alpha_3 C^3 \end{aligned}, \tag{2. 21}$$

where the terms in Equation (2.21) give equal power compared to the situation where the two tones have equal powers (A=B). If both signals are given in dBm it can be calculated that the equal power is

$$\begin{aligned} &tone\,(2\omega_2-\omega_1);\quad C[dBm]=\frac{1}{3}A[dBm]+\frac{2}{3}B[dBm] \\ &tone\,(2\omega_1-\omega_2);\quad C[dBm]=\frac{2}{3}A[dBm]+\frac{1}{3}B[dBm] \end{aligned}. \tag{2. 22}$$

The IIP3 at the LNA input can be calculated for signals with different powers as

$$IIP3 = \frac{1}{2}P_{\omega 1} + P_{\omega 2} - \frac{1}{2}P_{imd3,i}\,, \tag{2. 23}$$

where $P_{\omega 1}$ and $P_{\omega 2}$ are the input powers (dBm) of the two interferers and $P_{imd3,I}$ (dBm) is the power of the input-referred third-order intermodulation component. The loss of the pre-select filter must be taken into account when the power of the intermodulation component is being determined. Equation (2.23) is valid only when the two interferers are at lower frequencies than the intermodulation component (i.e. ω_1, $\omega_2 < \omega_{imd3}$). If the factors of $P_{\omega 1}$ and $P_{\omega 2}$ are interchanged the equation is valid for intermodulation components at lower frequencies. In [13], it is estimated that the leaked transmitter signal has power less than –30dBm and the CW blocker has power less than –45dBm, which leads to –8 dBm IIP3 at the LNA input, when the loss of the pre-selection filter is 4dB. In [19], the IIP3 at the pre-select filter input is defined as being –9dBm. The accurate determination of the IIP3 caused by transmitter leakage depends heavily on the properties of the pre-selection filter, PCB design, and IC design (if the receiver and transmitter are on the same chip). Therefore, isolation from the transmitter to the receiver should be determined as early as at the system level design stage. The IIP3 requirements for the stages following the LNA can be relaxed by using an external filter between the LNA and mixers, which filters out the transmitter and interfering signals. However, the presence of the external filter decreases the integration level of the receiver.

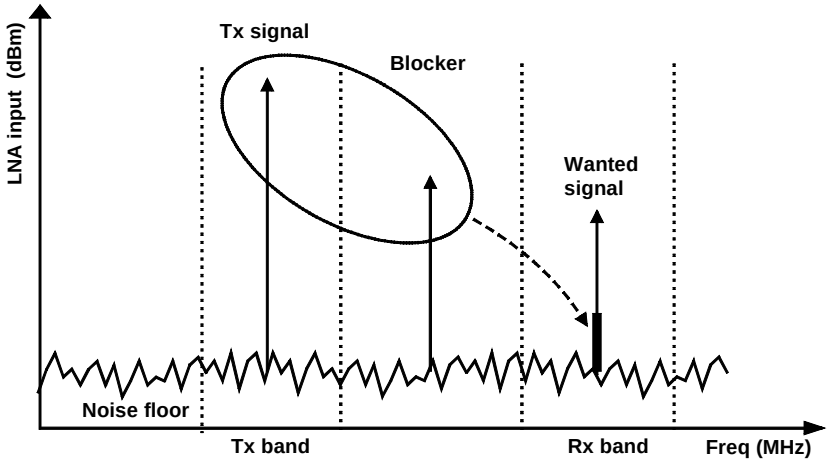

Figure 2.15. Third-order intermodulation resulting from Tx leakage.

Another issue that must also be considered in simulations is cross-modulation. This is caused by the transfer of an amplitude modulation of a strong signal (such as transmitter in a handset) onto another signal (the adjacent channel) in a nonlinear circuit (i.e. LNA, mixer etc.). This is an important issue in WCDMA receivers because the transmitter can be active during reception and the high output power (up to +21dBm) is only filtered by a duplex filter with a selectivity between –40 and –50dB in front of the LNA. Additionally, it is possible that the adjacent channel may be 41dB stronger than the desired channel. The cross-modulation is a third-order nonlinearity and it can be calculated with the following expression [18].

$$Pc\,\mathrm{mod} = 2P_{TX} + P_{ADJ} - 2IIP3_{LNA} + k_{CMOD} \tag{2. 24}$$

Pcmod is the cross-modulation power in the user channel, P_{ADJ} is the adjacent channel power, and P_{TX} is the transmitter power at the LNA input. The k_{cmod} is an empirical factor (in dB), which takes into account the crest factor and signal bandwidth. Equation (2.24) is slightly modified from the original formula, where k_{CMOD} was divided into three terms [20]. The effect of cross-modulation on the signal received is shown in Figure 2.16. Without the transmitter signal the adjacent channel signal does not spread outside the reception band. When the transmitter signal is applied, the adjacent channel spreads into the reception band of the desired signal because of the cross-modulation.

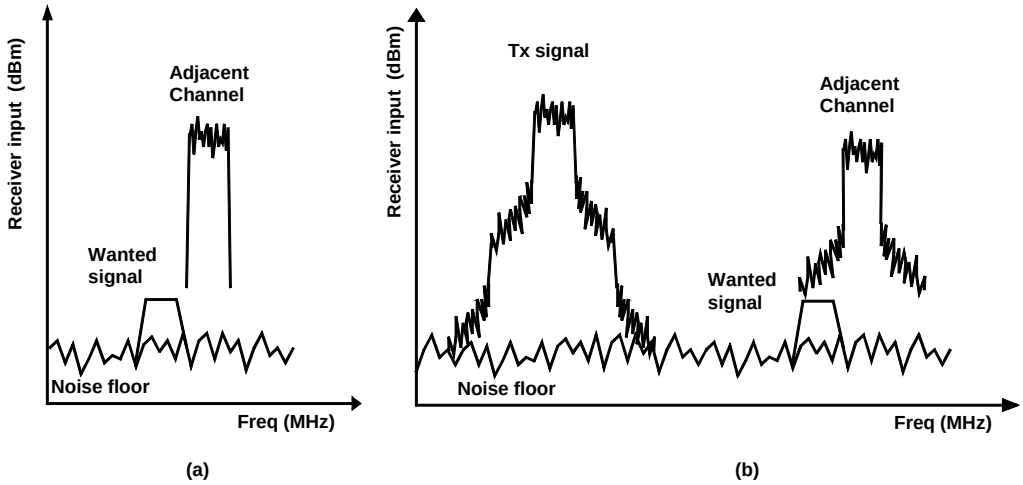

Figure 2.16.(a) Received signal without Tx signal. (b) Received signal with Tx signal.

The definition of other intermodulation products in the LNA is not usually necessary. In the case of DCRs, the second-order nonlinearity is a serious problem and, therefore, the intermodulation products at frequencies of f_2-f_1 must be checked. As previously stated, in the LNA there is usually no problem with these intermodulation products, because they can be filtered out at the output of the LNA and, in addition, the mixer upconverts these products to the RF. The IIP2 of the receiver can be determined as

$$IIP2 = 2P_{out} - P_{imd2} - G = P_{in} + \Delta P_2 , \qquad (2.\ 25)$$

where P_{imd2} (dBm) is the second-order intermodulation product at the output and ΔP_2 is the difference between the fundamental and second-order product (dBc). For example, the transmitter signal sets the IIP2 in the WCDMA system because of limited isolation between receiver and transmitter, and, in addition, other issues, such as modulation and the number of code channels composing a traffic channel affect the IIP2. However, as previously mentioned, the IIP2 is rarely considered in LNA design. Therefore, IIP2 considerations are left out of this thesis. Details for IIP2 specifications and design parameters can be found in [6], [7], [10], [11], [13], [16], [19], [21], [22], [23].

2.5.2.3 Blocking and desensitization

The receiver must tolerate large interfering signals in the adjacent channels. For example, in the GSM and WCDMA specifications, a blocking test is applied to the receiver. In this test, a large blocker is applied at the receiver input together with the weak desired signal. The receiver must be able to demodulate the desired signal with a sufficiently low BER. The power level of the

blocker depends on frequency. When the blocker is applied at the reception band of the receiver with some frequency offset to the desired signal, it is defined as an in-band blocker. If the blocker is applied outside the reception band, it is defined as an out-of-band blocker. Figure 2.17 illustrates the blocking mask of a WCDMA receiver. The in-band blocking test can be applied to the receiver without a pre-select filter. However, out-of-band blocking requires a pre-select filter, since the test signals are at the stopband of the pre-select filter.

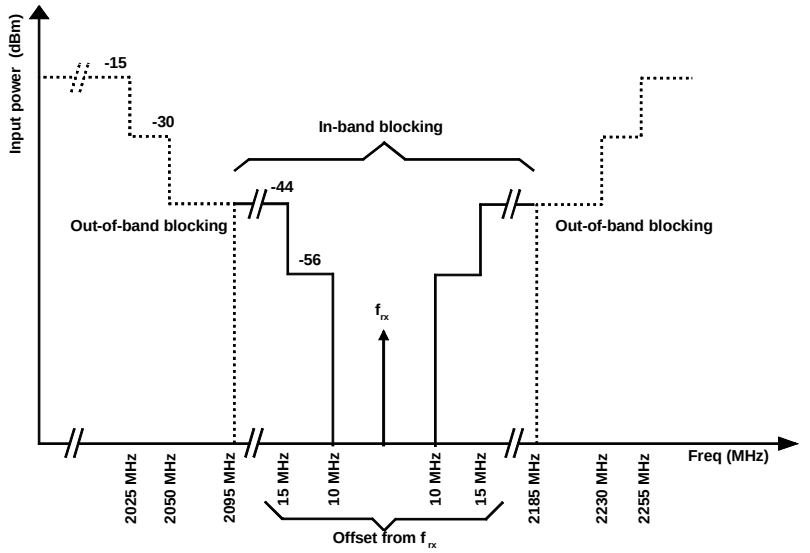

Figure 2.17. Power levels in the blocking test in WCDMA.

A large blocker can desensitize the desired signal by means of two mechanisms [24]. The first is the gain compression caused by a third-order nonlinearity. As shown in Equation (2.18), if two tones are applied at the input of a nonlinear element, the amplitude at the fundamental frequency is affected by the third-order term. If the opposite signs for α_1 and α_3 are assumed, as in the single-tone test, a compression of the fundamental is observed. Hence, the large blocker compresses the small desired signal. The second mechanism is the desensitization caused by the second-order nonlinearity. In this case, there is a mixing mechanism between (relatively) low-frequency noise sources in the amplifier and the interfering signal, which results in the low-frequency noise being up-converted to the desired signal frequency. This may corrupt the signal-to-noise-ratio.

2.6 Receivers with multi-mode capabilities

The design challenges of a multi-mode or multi-standard receiver are greater than those presented by a single-mode receiver. These receivers have some additional issues which must be considered even during the early phases of the receiver's design. The interferences from different standards depend on the chosen systems, receiver architecture, and circuit level issues. First of all, the chosen standards may require simultaneous operation (concurrent reception) or one standard may be active at a time. The approach which is taken in this thesis is that the receiver "chooses" the standard which is optimal for the desired signal from among those of the implemented standards which are available at the location of the receiver. For example, in addition to this cellular connection, some type of short-range link (to a computer) might be wanted in the future. However, the integration of this type of receiver requires separate LO and

clock signals, which can generate unwanted spurious signals on the IC. In addition, parallel structures may be required in some stages for optimal reception. The specifications for these other links may also differ drastically from those used in a cellular link. Thus, it may be optimal to use separate chips for these receivers. This would make possible the use of different IC technologies for different receivers and obviously remove the spurious signals of other systems from the IC. Therefore, the implementation of concurrent receivers has been left out of this thesis.

A straightforward design strategy for the multi-mode receiver would be to use parallel signal paths for each standard. If different signal paths were switched to be active this approach could be used both in concurrent and one-standard-at-a-time receivers. However, the chip area of this type of receiver would be the sum of the individual receivers, which would lead to large and expensive chips. Thus the goal in this thesis has been to implement a multi-mode receiver which shares as many building blocks as possible between different systems without significantly degrading the performance of the individual receivers.

All architectures require a pre-select filter prior to the LNA. Therefore, the pre-select filter has quite similar performance demands, regardless of the architecture. Depending on the receiver, either a single multi-band pre-select filter [25] or parallel filters for individual systems are needed. The benefit of a single multi-band filter is that it needs only one input, thus increasing the number of shared components compared to the situation where all systems have individual inputs. However, the matching at the LNA input usually has a narrow bandwidth and thus complicated external matching networks are usually required for a single-input receiver, as will be shown in Chapter 4. Furthermore, the receiver may contain different standards, depending on the targeted market area. This would require modifications to the whole pre-select filter if a multi-band filter were used, instead of just one filter being replaced in a multi-input receiver. The other issue which must be considered in pre-select filter design is blocking caused by other systems. For example, if there is no band-select switch at a multi-band pre-select filter, all reception bands have only pass-band loss to the LNA input. The power levels of these bands can have much higher power levels than the in-band blockers for individual systems, which may increase the receiver's blocking requirements.

After the pre-select filter, the possible solutions depend on the receiver architecture. The problems in superheterodyne receivers relate to the passive filters. The image-noise filter has the same limitations as the pre-select filter. Depending on the standards chosen, some of these image filters may be shared between different systems [26]. However, multiple filters require separate matching networks or multi-band filters require complicated matching networks, at the LNA output and mixer input. In addition, the bandwidth of the channel-select filter should be programmable if different standards are implemented. Hence, with current technologies, a multi-mode receiver using a superheterodyne architecture would be large and expensive. A possible application for this architecture is a multi-band receiver. Hence, the architecture works when the channel bandwidths and spacing between the systems used are the same, thus leading to only one external channel-select filter. For example, the GSM900, DCS1800, and PCS1900 standards operate in very similar manner, with the exception of the reception band. Thus, the multi-band receiver can share the same IF and only the RF blocks need to use parallel structures. The direct conversion architecture is more suitable for multi-mode operation because the channel-select filter operates near DC, and it can be relatively easily programmed for different channel bandwidths. In addition, the downconversion mixer typically has a wide operation bandwidth, and therefore does not require programmability for different standards. The LNA is the only component that uses frequency-selective components and requires programmability for multi-band operation. The detailed design issues of the multi-band LNA will be discussed in Chapter 4. Similarly to DCRs, the image reject architectures can be used to implement multi-mode receivers. As previously mentioned, these architectures do not require

off-chip filters, which would lead to a need for complicated matching circuits, as in superheterodyne receivers. However, depending on the systems and LO frequencies chosen, the image rejection must be achieved at different frequencies, which may require additional hardware. The filters used in these architectures must also be programmable for different frequencies and bandwidths, which again increases complexity if the filter needs to operate at higher frequencies as in DCRs.

A summary of the multi-mode or multi-band receivers and multi-mode RF circuits found in the literature is given in Table 2.2. A comparison between these receivers reveals that only a few blocks have been shared so far between different systems. Furthermore, many of these receivers use a superheterodyne architecture, which requires external IF channel-select filters and therefore is not very suitable for multi-mode operation.

Table 2.2. IC implementations of radio receivers with multi-band or multi-mode capabilities.

Ref	Application	Technol-ogy	Architecture	Shared blocks between all systems	Includes
[26]	GSM/DCS/PCS	BiCMOS	Super	IF Amplifier	RF and 1st IF amp.
[27]	0.9/2 GHz	BiCMOS	Super	-	LNA
[28]	CDMA/AMPS /WCDMA*)	GaAs	Super	- **)	RF and 1st IF amp
[29]	WCDMA/ CDMA/AMPS	BiCMOS	Super	VGA and analog baseband	RF,IF and analog baseband
[30]	GSM/DCS	SOI BiCMOS	Super	IF and analog baseband	RF,IF and analog baseband
[31]	CDMA/AMPS/ WCDMA/GPS	SiGe BiCMOS	Super	IF mixer	RF and IF mixer
[32]	0.9/1.8 GHz	CMOS	Image reject	BPF, 2nd mixers and Los	RF, IF and 2LOs
[33]	GSM/DCS/PCS	SiGe BiCMOS	Image reject	IF polyphase and IF amplifier	RF and IF
[34]	GSM/DCS/PDC	na	DCR	Analog baseband	RF and analog baseband ***)
[35]	GSM850/GSM /DCS/PCS	SiGe:C BiCMOS	DCR	Analog baseband	RF and analog baseband ***)
[36]	GSM850/GSM /DCS/PCS	BiCMOS	DCR	Analog baseband	RF and analog baseband ***)

*) Requires layout changes

**) Shared blocks between part of the systems

***) At the receiver side

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3 Single-system low-noise amplifier design

This chapter concentrates on the design issues of single-system low-noise amplifiers. The emphasis is on the single-stage inductively-degenerated common-emitter amplifier, which is the basis for the circuits designed in this thesis. The design of the input transistor, load, and biasing are discussed in detail. In addition, a comparison between the most common LNA topologies and design issues is given. However, the feedback theory is only addressed briefly in this section. Ideal feedback does not add noise; however, resistive feedback does add additional noise sources. For this reason, resistive feedback is to be avoided in low noise amplifiers [1]. It is also assumed, if not otherwise mentioned that the load for the LNA is on-chip. Thus, no matching is required at the LNA output.

3.1 Single-stage LNA configurations

LNAs are usually circuits with few transistors, in order to limit the number of devices generating additional noise. The design methodology in this thesis has been to achieve as low an NF as possible with sufficient bandwidth and linearity for cellular applications. Hence, the circuits which have been designed, are not targeted for wide-band receivers although this kind of LNA would be useful in some multi-mode applications [2], [3]. This subsection compares four different single-ended LNA input stage configurations, illustrated in Figure 3.1. The three configurations, resistively terminated LNA, feedback LNA, and common-base LNA, which have all been used as LNA input stages, are included to clarify why the inductively-degenerated common-emitter LNA was chosen. All four configurations use bipolar transistors, which can be replaced with MOS counterparts. In addition, all configurations use npn transistors, which are usually preferred because of their higher speed. The focus is on the inductively-degenerated bipolar LNA, which is the basis for all the experimental circuits in this thesis. This chapter includes also basic design issues for MOS LNAs since most of the design issues for bipolar LNA can be directly applied to MOS LNAs. However, it is not in the scope of this thesis to make full comparison between different technologies. Figure 3.2 shows the simplified small-signal models for bipolar and MOS transistors, which are valid in the forward-active region in BJT and saturation in MOS. These models have been used for comparison in this section, if it is not stated otherwise, and the results are partly compared to the results simulated for the detailed models used in the design of the experimental circuits.

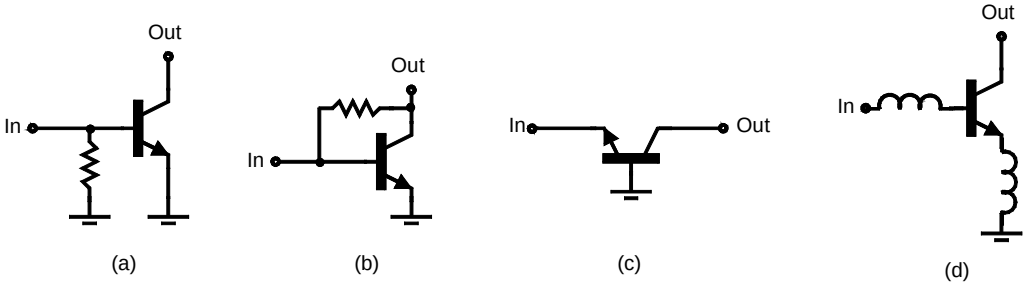

Figure 3.1. Schematics of (a) resistively matched LNA, (b) feedback LNA, (c) common-base LNA, and (d) inductively-degenerated LNA.

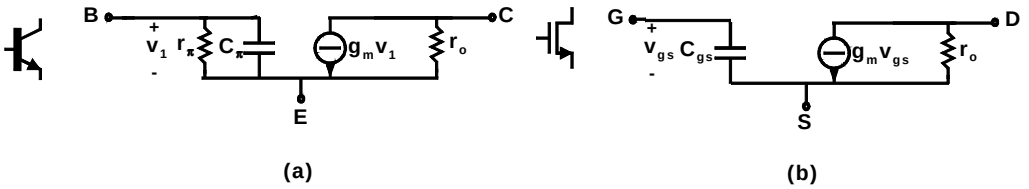

Figure 3.2. Simplified small-signal model of (a) bipolar transistor and (b) MOS transistor.

3.1.1 Input matching

The input matching of the LNA is required because the frequency response of a pre-select filter or balun is valid only for specific output impedance. The matching of the LNA is typically defined using the return loss, S11. The S11 [dB] at the LNA input is defined as

$$S11 = 20\log\left(\left|\frac{Z_{IN} - Z_S}{Z_{IN} + Z_S}\right|\right) \quad , \tag{3. 1}$$

where Z_{IN} is the LNA input impedance and Z_S is the source impedance. Usually a –10 dB S11 is considered to be a sufficient value in the reception band [4]. If the single-ended LNA is matched to the typical 50Ω input impedance, the –10 dB S11 corresponds to an LNA input impedance, which is between 26Ω and 96Ω. However, a different LNA input impedance may be required for the selected pre-select filter or balun.

The input matching of the four configurations in Figure 3.1 is based on different approaches. The first LNA uses resistive termination, where the input matching is simply performed by connecting an appropriate resistor between the input and ground. Hence, the LNA input impedance is

$$Z_{in} = R_m \| Z_{in,T} \, , \tag{3. 2}$$

where R_m is the matching resistor and $Z_{in,T}$ is the input impedance of the transistor. If the input is matched to 50Ω the matching resistor is usually much smaller than the input impedance of the transistor and dominates matching. In the feedback LNA, the transconductance of the transistor and the input impedance of the LNA determine the input matching, if the load of the LNA is much larger than the feedback resistor. Thus the input impedance is

$$Z_{in} = \frac{1}{1/Z_{in,T} + g_{m,T}}, \tag{3. 3}$$

where $g_{m,T}$ is the transconductance of the transistor. As in the resistive termination, the input matching is dominated by the transconductance when 50 Ω matching is required. Figure 3.1 (c) illustrates the common-base configuration. The matching in this case is determined only by the transconductance of the device,

$$Z_{in} = \frac{1}{g_{m,T}} \, . \tag{3. 4}$$

However, this is only valid if the load of the device is much smaller than the output resistance of the transistor, r_o. Otherwise, the load increases the input impedance of the LNA. Figure 3.1 (d) shows the inductively-degenerated LNA, where the base and emitter inductors are used for matching purposes. The input impedance of this LNA is [5]

$$Z_{in} = \frac{g_{m,T} L_e}{C_\pi} + j\left(\omega(L_b + L_e) - \frac{1}{\omega C_\pi}\right). \tag{3. 5}$$

Hence, Equation (3.5) has only a real part at the resonance frequency of the series resonator formed by the base and emitter inductors L_b, L_e, and base-emitter capacitor, C_π. Equation (3.5) assumes that C_π dominates the input impedance of the transistor at the operating frequency ($C_\pi << R_\pi$).

Figure 3.3 illustrates the S11 of the four configurations in which the simplified model is compared to the more accurate model used in the multi-mode receiver design. To avoid the dependence of S11 on load impedance, the feedback LNA is simulated using a high impedance load and the other three use a low impedance load. The g_m of the transistor is set to 20mS and r_π, and C_π are the same as in the detailed transistor model. The –10 dB S11 can be achieved in all four cases, though the matching in a degenerated LNA has a narrow operating band compared to other LNAs. However, the matching at the reception frequency of one wireless communication system (Chapter 2.4) can be achieved. In addition, the matching in the first three LNAs begins to decrease at high frequencies, which is due to C_π . Depending on the reception frequency of the LNAs, the matching at high frequencies must be compensated with additional devices.

3.1.2 Voltage gain

The voltage gain of the four configurations in Figure 3.1 can be compared by comparing the transconductance ($G_m = |I_{out}/v_{in}|$) of each LNA, since

$$A_v = G_m |Z_L(j\omega)|, \tag{3. 6}$$

where $Z_L(j\omega)$ is the load impedance of the LNA. The G_m of the resistively-terminated LNA and G_m of the common-base LNA are equal to the transconductance of the transistor ($G_m=g_m$). The difference between these two configurations is that the g_m in the common-base configuration is determined by matching ($R_{in}=1/g_m$). Hence, the voltage gain in the common-base LNA is

$$A_v = \left|\frac{Z_L(j\omega)}{R_{in}}\right|. \tag{3. 7}$$

The voltage gain of the resistively-matched LNA can be adjusted more freely because the g_m and the load impedance affect the voltage gain, but the matching does not depend on g_m. The G_m of the feedback LNA is

$$G_m = \left|\frac{g_m R_{fb} - 1}{R_{fb} + Z_L}\right|, \tag{3. 8}$$

where R_{fb} and Z_L are the feedback resistor and load impedance, respectively. If the Z_L is assumed to be much larger than the feedback resistor, which was also done in the case of matching, then the voltage gain of the feedback LNA is

$$A_v \approx \left| g_m R_{fb} - 1 \right|. \tag{3. 9}$$

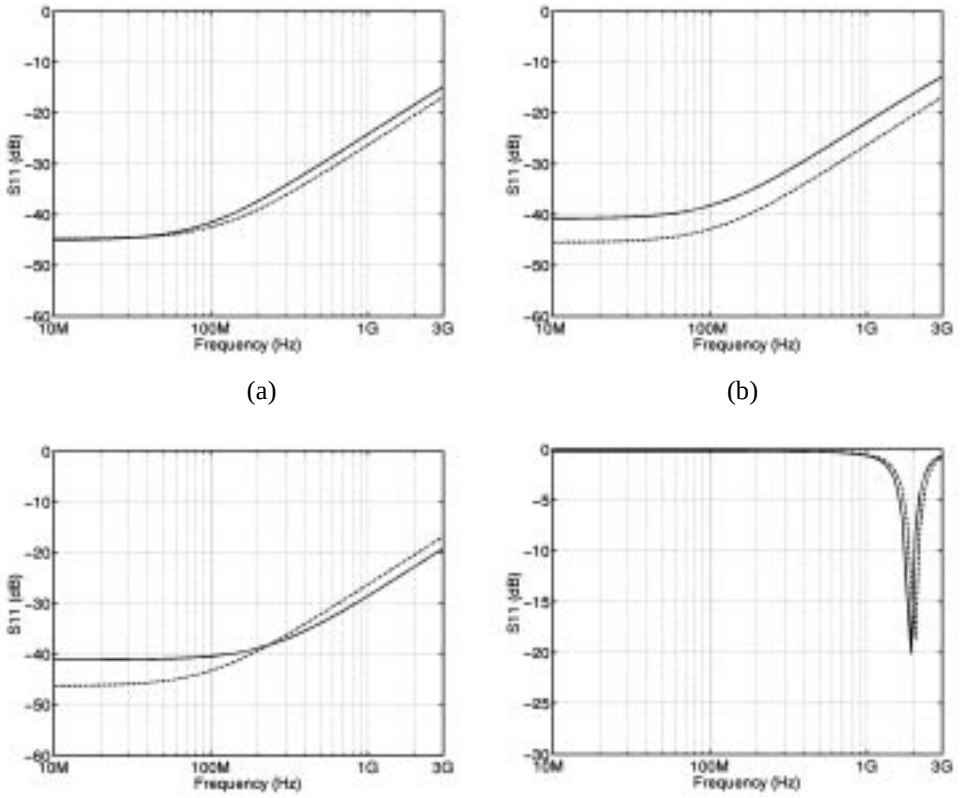

Figure 3.3. The simulated S11 of (a) resistively-matched, (b) feedback-matched, (c) gm-matched, and (d) inductively-degenerated LNA. The dashed line is simulated using the simplified BJT model in Figure 3.2 and the solid line using a complicated BJT model, which was used in the design of a multi-mode receiver.

The voltage gain of the feedback LNA is determined by the feedback resistor, since the input matching determines the g_m of the input transistor. The G_m of the inductively degenerated LNA is

$$G_m = \left| \frac{g_m}{\left(j\omega L_b + j\omega L_e + 1/\, j\omega C_\pi \right) j\omega C_\pi + j\omega L_e g_m} \right| \tag{3. 10}$$

At the resonance frequency the term in parentheses becomes equal to zero and the G_m becomes

$$G_m = \frac{1}{\omega_r L_e}, \tag{3. 11}$$

where ω_r is the angular frequency of the matching. Thus, the transconductance of the inductively degenerated LNA cannot be adjusted by changing the g_m of the transistor itself without changing the LNA matching.

3.1.3 Noise figure

The NF determines how much the LNA (or any device) degrades the signal to noise ratio. Before comparing the four configurations in Figure 3.1, a short introduction to transistor noise models is given. Figure 3.4 illustrates the small-signal models of bipolar and MOS transistors, including the most important noise sources. Both transistor models include current noise sources in parallel to the g_m and between the base and the emitter (or the gate and the source). In addition, both models include voltage noise sources. Usually, the most important voltage noise sources are those at the base or at the gate of the device, because the noise from these sources is multiplied by the g_m of the device to the collector or the drain. The mean-square values for the noise sources of a bipolar transistor are

$$\begin{aligned} \overline{i_c^2} &= 2qI_cB \\ \overline{i_b^2} &= 2qI_bB \\ \overline{v_x^2} &= 4kTBR_x \end{aligned}, \tag{3. 12}$$

where q is the electron charge ($1.602*10^{-19}$ C), k is Boltzmann's constant ($1.38*10^{-23}$ J/K), T is the absolute temperature, and R_x is the resistance of the resistor associated with the noise source. All these noise sources are independent because they arise from separate, independent physical mechanisms [6]. However, the flicker and burst noise terms are not included in the equation because the experimental circuits included in this thesis operate well above the noise corner frequency. The corresponding noise equations for MOS transistors are

$$\begin{aligned} \overline{i_d^2} &= 4kT\gamma g_mB \\ \overline{i_g^2} &= 4kT\delta g_gB \\ \overline{v_g^2} &= 4kTr_gB \end{aligned}, \tag{3. 13}$$

where γ is a bias dependent factor, which is 2/3 for long-channel transistors in saturation, while for short-channel devices operating in saturation it increases to 2-3 [7]. δ is the coefficient of gate noise and for long channel devices it is equal to 4/3. A crude approximation is to assume that δ is about twice as large as γ for short-channel devices. Hence δ can vary between 4 and 6 [8]. r_g is the distributed gate resistance and g_g is [8]

$$g_g = \frac{\omega^2 C_{gs}^2}{5g_m}. \tag{3. 14}$$

The gate noise is proportional to ω^2 and thus is not white noise. The gate noise and drain noise in Equation (3.13) are correlated, because both noise currents are generated by thermal fluctuation in the channel. According to [9], the magnitude of the correlation is 0.395. Again, the flicker noise is excluded from the noise equations.

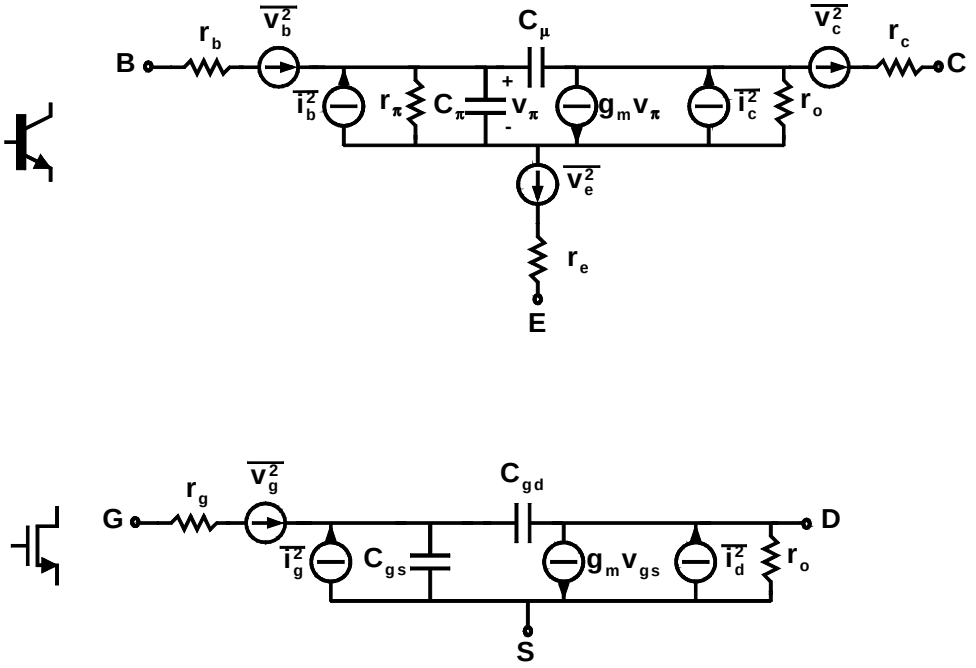

Figure 3.4. Small-signal models of bipolar and MOS transistors including the noise sources.

The resistively degenerated LNA in Figure 3.1 has a relatively high minimum NF, because the noise from the termination resistance can be directly added to the noise from the source resistance. Thus, if the source resistance is equal to the matching resistor, the NF of this configuration is

$$NF = 10\log\left(2 + \frac{\overline{e_{n,out,q}^2}}{kTBR_s(A_v)^2}\right), \tag{3. 15}$$

where $\overline{e_{n,out,q}^2}$ is the noise voltage of the transistor at the output and A_v is the voltage gain. If the transistor was noiseless, the minimum NF would still be 3dB, which is usually too large for communication systems. The NF of the feedback LNA is

$$NF = 10\log\left(1 + \frac{R_s}{R_{fb}}\left(1 + \frac{R_{fb} + R_s}{R_{fb} - R_s}\right)^2 + \frac{\overline{e_{n,out,q}^2}}{kTBR_s(A_v)^2}\right) \tag{3. 16}.$$

Equation (3.16) assumes perfect matching and that the g_m of the transistor dominates input matching (i.e. $g_{m,t}>>1/Z_{in,t}$). It can be noticed that the NF of the feedback LNA decreases as the feedback resistor increases. Hence, the transistor noise becomes dominant at large resistor values, as can be expected.

In order to compare the common base configuration to the other topologies, it is assumed that all transistor noise originates from the drain or collector current noise source. With this assumption, the NF of this configuration becomes

$$\begin{aligned} NF &= 10\log\left(\frac{3}{2}\right) \\ NF &= 10\log(1+\gamma) \end{aligned}, \tag{3. 17}$$

for BJT and CMOS transistors, respectively. For BJT, the noise figure is 1.76dB and for CMOS, the NF is 2.2dB – 6dB with γ values between 2/3 and 3. The NF of an inductively-degenerated LNA can be calculated as

$$NF = 10\log\left(1+\frac{e_{n,out,q}^2}{kTBR_s(A_v)^2}\right), \tag{3. 18}$$

because there are no noise sources other than the transistor itself. More details of the NF of this configuration are given in the next section. However, it can be stated at this point that the lowest NF of all four configurations can be achieved using inductively-degenerated LNA.

3.1.4 NF of the inductively-degenerated common-emitter LNA

Several studies of the NF calculations of an inductively-degenerated LNA can be found in the literature [4], [10]-[13]. The method which is presented in this thesis is based on the Y parameters of a bipolar transistor. This approach can be easily used in device dimensioning in order to achieve a low NF. Fukui and Voiniegescu [10], [11] have showed that the minimum achievable NF for a common-emitter configuration when matched to optimum source impedance is

$$NF_{\min} = 1+\frac{n}{\beta_{DC}}+\sqrt{\frac{2I_C}{V_T}(r_e+r_b)\left(\frac{f^2}{f_T^2}+\frac{1}{\beta_{DC}}\right)+\frac{n^2}{\beta_{DC}}}\,. \tag{3. 19}$$

r_e and r_b are the emitter and base resistors, I_c is the collector current, f_t is the unity gain frequency, β_{DC} is the DC current gain, n is the collector current ideality factor, which is approximately between 1 and 1.2, and f is the operation frequency. The small-signal models used for NF calculations are practically the same as in Figure 3.4. The model used by Voiniegescu excludes the collector resistance and Fukui's model excludes both collector and emitter resistances. However, the collector noise usually has a negligible effect on the NF since it is in series with the high-impedance collector node. Hence, it can be excluded from the model [6]. The minimum NF in Equation (3.19) is obtained when the source resistance is

$$R_{S-opt} = \frac{f_T}{f}\left(\frac{n^2}{2I_C} + (r_e + r_b)\right)\left(\frac{\sqrt{\frac{I_C}{2V_T}(r_e + r_b)\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2 f_T^2}{4\beta_{DC} f^2}}}{\frac{I_C}{2V_T}(r_e + r_b)\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right) + \frac{n^2}{4}\left(1 + \frac{f_T^2}{\beta_{DC} f^2}\right)}\right) \quad (3.\ 20)$$

Figure 3.5 shows the minimum NF calculated using Equation (3.19). The parameters used in the calculations are taken from the models used in the experimental circuits. As can be seen, the NF_{min} has a minimum value at a certain collector current. In addition, the minimum NF is not significantly degraded if there are small variations in the collector current. Figure 3.6 shows the corresponding optimum source resistances, in which the minimum NF is achieved. The optimum NF is achieved by adjusting the collector current of the unit transistor according to Equation (3.19). Then by keeping a constant current through the unity transistor, the number of parallel transistors is increased until the appropriate source resistance is achieved.

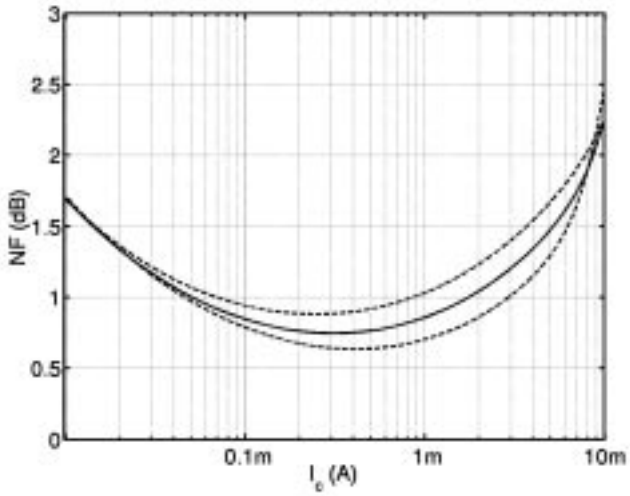

Figure 3.5. Minimum NF at 2.1GHz as a function of the transistor collector current. The solid line is simulated with typical parameters and the dashed lines show the variations at process corners.

Reference [13] compares the equations presented to some classical equations, for example to the noise analysis performed by van der Ziel [9] for minimum NF and concludes that the method presented does not give exactly the same results. According to [13], the input-referred noise sources presented in this section does not take into account the series resistances of the transistor. However, it is stated that it can be conveniently used for rough estimates. Furthermore, the method presented is based on a complicated model of a bipolar transistor. It includes the output conductance, base-collector capacitance, and emitter series resistance, which the other methods in [13] do not take into account. In [4], the inductively-degenerated LNA is modified by including an external capacitor between the base and the emitter of the input transistor. The noise calculations are based on [11] and assume that the capacitor is in parallel to C_π. With this additional capacitor, the NF_{opt} and $R_{s,opt}$ in Equations (3.19) and (3.20) can be adjusted more freely, thus giving additional parameters to optimize LNA performance. Similar equations for a CMOS LNA can be found in [14]. It must also be noted that the bonding pad and ESD-protection, which are at the LNA input, increase the NF. The bonding pad and

ESD-protection have a parasitic capacitance to substrate, which couples noise and other interferences from the substrate to the LNA input. The effect of the bonding pad on NF is analyzed in [15] and [16], and the effect of ESD-protection is discussed in [17] and [18].

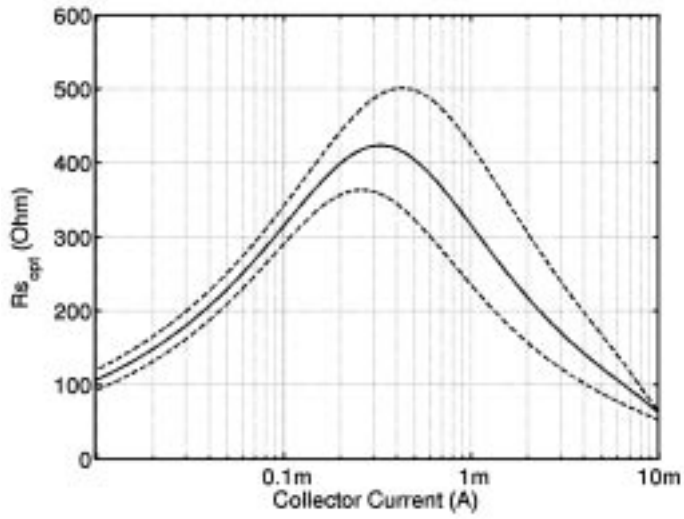

Figure 3.6. Optimum source resistance as a function of the transistor collector current at 2.1GHz. Solid line is simulated with typical parameters and dashed lines shows the variations at process corners.

3.1.5 IIP3

The comparison of the linearity of the four configurations is performed using bipolar transistors. CMOS transistors require detailed models because the simplified CMOS model is based on the square law behavior and therefore no third-order phenomena can be seen. Since the details of the CMOS are not within the scope of this thesis the CMOS configurations are left out. However, some of the linearity issues can be directly applied to CMOS transistors.

The IIP3 for the memoryless and time-invariant system in Equation (2.18) is

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}, \tag{3. 21}$$

assuming that α_1 dominates at the fundamental frequency. The IIP3 [dBm] becomes

$$IIP3 = 10\log\left(\frac{A_{IIP3}^2}{2R_S}\cdot 1000\right), \tag{3. 22}$$

where R_s is the input resistance of the device. Using Equation (3.22) and modeling the collector current with a Taylor series as

$$I_c = I_S e^{\frac{V_{BE}+v_{in}}{V_T}} = I_S e^{\frac{V_{Be}}{V_T}}\left[1+\frac{v_{in}}{V_T}+\frac{1}{2}\left(\frac{v_{in}}{V_T}\right)^2+\frac{1}{6}\left(\frac{v_{in}}{V_T}\right)^3+..\right], \quad (3.\ 23)$$

a rough estimate for the IIP3 of a bipolar transistor can be calculated. This becomes

$$IIP3 = 10\log\left(\frac{4V_T^2}{R_S}\cdot 1000\right). \quad (3.\ 24)$$

Comparing the four configurations, the resistively-terminated and common-base configurations do not use feedback unlike the other two configurations. Using Equation (3.24), the first approximation for the IIP3 of a resistively-terminated LNA is at 290 K –13dBm. Using Volterra series analysis it can be calculated that the IIP3 of a common-base LNA is equal to that of the common-emitter LNA [19]. The other two configurations use feedback to increase the IIP3. An example of a resistive-feedback LNA IIP3 is shown in Figure 3.7. It illustrates IIP3as a function of the feedback resistor using the transistor model used in the experimental circuits.

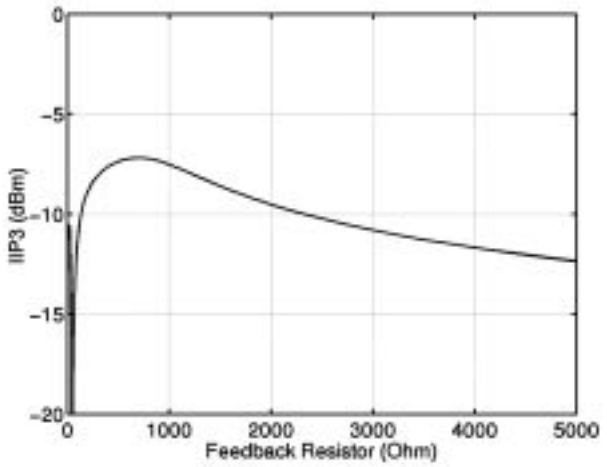

Figure 3.7. IIP3 of a resistive feedback LNA as a function of the feedback resistor value.

Before giving detailed equations for the IIP3 of an inductively degenerated LNA, the IIP3 is calculated for the resistively-degenerated LNA shown in Figure 3.8. If frequency dependencies and the base current of the LNA are ignored and it is assumed that i_{out} is zero when there is no input, i.e. v_{in}=0 V, the Taylor series coefficients can be calculated using implicit derivation. The coefficients are

$$\alpha_1 = \frac{g_m}{1+g_m R_e}, \qquad \alpha_2 = \frac{g_m}{2V_T(1+g_m R_e)^3},$$
$$\alpha_3 = \frac{1}{6(1+g_m R_e)^4}\frac{g_m}{V_T^2}\left(1-\frac{3g_m R_e}{1+g_m R_e}\right) \quad . \tag{3. 25}$$

The IIP3 of a resistively-degenerated LNA becomes

$$A_{IIP3} = \sqrt{\left|\frac{8(1+g_m R_e)^4 V_T^2}{1-2g_m R_e}\right|} \quad . \tag{3. 26}$$

Thus, it can be seen from Equation (3.26) that the IIP3 increases as the value of the degeneration resistor, R_e, is increased.

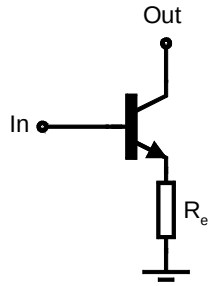

Figure 3.8. Resistively-degenerated LNA.

For the inductively-degenerated LNA, the detailed IIP3 analysis based on the Volterra series is presented in [1] and [20]. The magnitude of the upper third-order intermodulation product IM3 (at the frequency $2f_a$-f_b) is [20]

$$|IM3| \approx \left|\frac{A_1(s)}{I_Q}\right|^3 \left|\frac{V_T}{4}\left[1+sC_{je}Z(s)\right]\right.$$
$$\left.\left\{-1+\frac{A_1(\Delta s)}{g_m}\left[1+\Delta s C_{je}Z(\Delta s)\right]+\frac{A_1(2s)}{2g_m}\left[1+2sC_{je}Z(2s)\right]\right\}\right|V_s|^2 \quad , \tag{3. 27}$$

where

$$\Delta s = (s_a - s_b) \langle s, s_a = j2\pi f_a, s_b = j2\pi f_b$$
$$s \approx s_a \approx s_b, s_a > s_b$$
$$A_1(s) = \frac{g_m}{\left[sC_{je}Z(s)+s\tau_F g_m Z(s)+g_m Z(s)/\beta_0+1+g_m Z_e(s)\right]} \tag{3. 28}$$
$$Z(s) = Z_b(s)+Z_e(s)$$

I_Q is the bias current of the input transistor, C_{je} is the base-emitter capacitor assumed to be constant, and τ_F is the forward transit time, relating to the base-charging capacitor in parallel with C_{je}. $Z_b(s)$ and $Z_e(s)$ are the impedances at the base and the emitter of the input transistor. The $A_1(\Delta s)$ term in the inductive degeneration case is much larger than those in the resistive and capacitive degeneration cases. Hence, the IIP3 of an inductively-degenerated LNA is higher than the IIP3 of a resistively- or capacitively-degenerated LNA.

3.1.6 Summary of the input stage comparison

Table 3.1 compares the four different LNA input configurations presented above. How good the configuration is for a wireless single-system telecommunication system has been evaluated. A resistive termination LNA has a very high NF (NF >> 3dB), which limits its usage as a first stage in the LNA in cellular systems. However, it is a very simple configuration, and therefore it could be used in some blocks requiring off-chip matching after the first LNA. In addition, it could be used in systems which do not require good sensitivity, such as wireless sensors. The goal in the experimental circuits was to achieve as low an NF as possible. If the three remaining configurations are compared, it can be seen that the inductively-degenerated LNA achieves the lowest NF and has no additional features which would limit its usage. Therefore, this configuration has been the basis for all the experimental circuits in this thesis. However, it must be noted that all the configurations except the resistive termination are possible candidates for the first LNA stage in wireless receivers. For example, neither a resistive-feedback LNA or a common-base LNA requires inductors, which require a large chip area or an additional bonding pad for an external inductor.

Table 3.1. Performance comparison of four different input stages for wireless telecommunication receivers.

	Resistive termination	Resistive feedback	Common base/gate	Inductively degenerated
S11	+	+	+	+
Gain	+	+ / -	+ / -	+ / -
NF	- -	-	-	+
IIP3	+ / -	+	+ / -	+
Bandwidth	+	+	+	-

3.2 Cascode transistor

The inductively-degenerated input transistor can be used as an LNA by adding a load to the transistor collector. This solution is simple and does not include any additional components which could increase the NF of the LNA. As it can be seen from Appendix 1, this configuration has been widely used in recently-published LNAs. However, the experimental LNAs in this thesis use cascode transistors between the load and input transistor, as shown in Figure 3.9 (a). The cascode transistor has several benefits which make it especially suitable for DCRs. The cascode transistor reduces the Miller effect in the input transistor, since the input impedance of the cascode transistor is usually smaller than the load impedance. In addition, the cascode

transistor increases the separation between the input and output terminals of the LNA compared to a single-transistor LNA. Hence, the input matching, size of input transistor, and load can be separately optimized. The increased separation can have a significant effect on the performance of the DCR. The improved reverse isolation reduces the LO leakage to the LNA input. The specifications determine the maximum spurious emissions for the terminal. Because the LO signal is located in the receiver reception band, the pre-select filter does not significantly increase the isolation as, for example, in superheterodyne receivers, where the leaked LO is located in the stop band of the pre-select filter. The improved isolation can have a significant effect on the transient caused by the variable gain in the LNA. This effect is discussed in detail in Chapter 5.

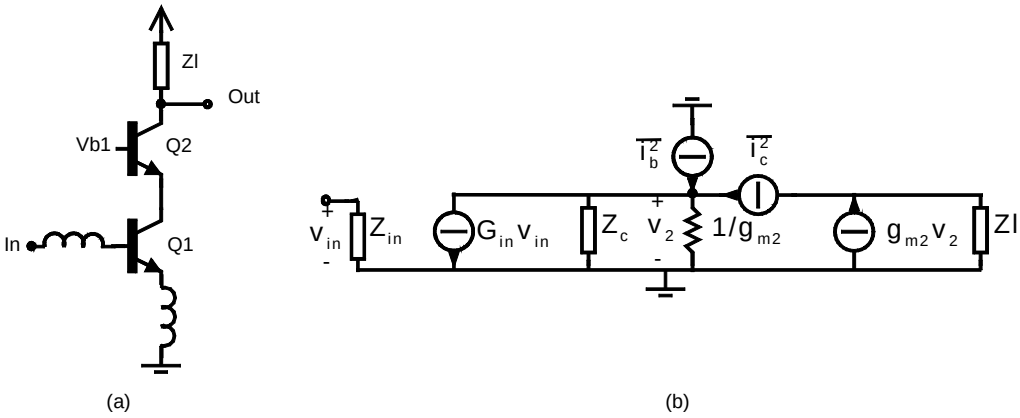

Figure 3.9. (a) Inductively-degenerated LNA with a cascode transistor. (b) Noise sources of a cascode transistor.

The drawback in using a cascode transistor is increased LNA NF. Figure 3.9 (b) shows the small-signal model of an inductively-degenerated cascode bipolar LNA, which can be used to calculate the effect of the cascode device on the NF of the LNA. G_{in} is the transconductance of the degenerated input transistor, $\overline{i_c^2}$ and $\overline{i_b^2}$ are the collector and base current noise sources of the cascode transistor, Z_C is the parallel combination of all impedances at the collector of the input transistor excluding the resistor $1/g_{m2}$ of the cascode transistor, and Zl is the load impedance. Both noise sources are independent and therefore the noise sources can be calculated independently. The output noise voltage of the cascode LNA with the two noise sources becomes

$$\overline{v_{nout}^2} = \left(\frac{1/g_{m2}Z_C}{1+1/g_{m2}Z_C} \right)^2 \overline{i_c^2} Zl^2 + \left(\frac{1}{1+1/g_{m2}Z_C} \right)^2 \overline{i_b^2} Zl^2 . \qquad (3.29)$$

The voltage gain of the matched cascode LNA is

$$A_v = G_{in} \frac{1}{1+1/g_{m2}Z_C} Zl \qquad (3.30)$$

Using Equations (3.29) and (3.30), the NF of the LNA becomes

$$NF = 10\log\left(F_{in} + \frac{\overline{i_c^2}\left(1/g_{m2}Z_C \right)^2}{kTBR_S G_{in}^2} + \frac{\overline{i_b^2}}{kTBR_S G_{in}^2} \right), \quad (3.\ 31)$$

where F_{in} represents the noise factor of the input transistor. It can be seen from Equation (3.31) that the effect of the collector noise on the LNA NF depends on the impedance, Z_C, and the base shot noise has a constant value. Therefore, to minimize NF degradation caused by collector shot noise, the impedance Z_C must be maximized, for example, by using small devices. The base shot noise can be minimized by selecting the collector current of a unit transistor as maximum beta to achieve minimum base current. In addition, the impedance at the collector of the input transistor affects the voltage gain of the LNA. The voltage gain of the LNA can be adjusted by changing the load impedance. However, if the load impedance is increased the noise of the load is also increased, as is the LNA NF. The noise caused by the base resistor was excluded from the equations because its effect decreases as the Z_C is increased and hence it can be excluded with practical values of Z_C. A similar equation can be calculated for the MOS transistor by removing the base shot noise and replacing the collector shot noise with MOS transistor drain noise [21]. In the case of a MOS transistor, the g_m of the cascode transistor depends on the drain current and the width and length of the transistor. In bipolar transistors the g_m depends only on collector current. Therefore, using a MOS cascode, the g_m can be increased by increasing the transistor width, which reduces the Miller effect in the input transistor. The increase of the width also increases the capacitance at the drain of the input transistor, which on the other hand increases the noise of the cascode transistor. Hence, the MOS cascode transistor usually has a size equal to the input transistor [8].

Solutions to increase the impedance, Z_C, which decreases the effect of the cascode transistor on the LNA, can be found. The capacitance, which is mainly formed by Z_C can be canceled by adding an inductor between the signal ground and the collector or drain of the input transistor [21], [22]. This solution has, however, a few drawbacks. The inductor requires a large chip area and, because of the finite Q of the on-chip inductor, increases the NF of the LNA. If an external inductor is used, at least an additional bonding pad would be needed in the LNA. Therefore, this solution is not widely used. In MOS technology, the capacitance can be minimized using the dual gate configuration, in which the drain of the input transistor is shared with the source of the cascode transistor [23], [24].

3.3 Load of the LNA

In this section the possible passive load alternatives for the LNA are studied. The three types of passive loads which are addressed are resistive load (R), resonator load (LC), and resistively-damped resonator load (RLC). The active loads are not within the scope of this thesis. These loads, for example, the PMOS load, tend to be noisy, to consume power, or require a higher supply than the LC load. Thus these are left out of this thesis.

3.3.1 Resistive load

An ideal resistance has an infinite bandwidth and, compared to loads which use inductors, the resistive load has a small chip area. Hence, a simple resistor would be an attractive alternative for wide- and multi-band solutions. However, even with an ideal resistor, the LNA output can

be assumed to be resistive only at low frequencies. At high frequencies, the different capacitors at the LNA output begin to limit the usable bandwidth. In a cascode common-emitter LNA, which drives the quadrature mixers, the output capacitance is the sum of the mixer input capacitance, the cascode transistor parasitic capacitance, and the load resistor parasitic capacitance. For example, the matching inductor at the emitter of the input transistor in the multi-mode LNA in Chapter 6.4 is 0.7nH. Hence, according to Equation (3.11) the G_m of the LNA at 2GHz is 114mS. If a 20-dB voltage gain is the target, the load resistor value becomes 88Ω. However, the input capacitance of quadrature mixers is typically in the range of pFs. For example, a 1pF input capacitance is observed in the multi-mode receiver in Chapter 6.4. Thus, the –3dB frequency of this RC load is 1.8GHz, which is below the operating frequency. Therefore a 20dB gain cannot be achieved without changing the LNA input stage or mixer input, which usually degrades the receiver performance, as previously described. If the operational frequency of the LNA is above the RC pole, the gain of the LNA will obviously vary between different reception channels. The process variations also alter the –3dB frequency, which affects the gain of the LNA. In addition, if the LNA has a low supply voltage, the resistive load drops the output voltage, which may degrade LNA performance because of an insufficient supply voltage to the input or cascode transistor.

3.3.2 Resonator load

The basic resonator load is formed from a parallel inductor and capacitor. With ideal components it has infinite impedance at an infinitely small bandwidth at the resonance frequency

$$f_r = \frac{1}{2\pi\sqrt{LC}}. \tag{3. 32}$$

Hence, it would be useless in LNA design. However, the losses in the inductor (and in the capacitor) reduce the resonator impedance and increase the resonator bandwidth. In addition, the parallel resistor has a similar effect on the impedance and bandwidth, as will be shown later. The on-chip inductor differs greatly from an ideal inductor and therefore requires accurate modeling. Detailed analysis and modeling information of the on-chip spiral inductor can be found in [25]-[30]. In this thesis the models and the layout for spiral inductors in the experimental circuits were given by the IC manufacturer. However, the LNA designer must be aware of the basic spiral inductor constraints. Figure 3.10 (a) shows a typical model of an on-chip spiral inductor. As can be seen, the inductor has a parasitic capacitance to the signal ground. In addition, the series resistance of the inductor reduces the losses of the inductor. Thus, on-chip inductor forms a resonator with finite impedance. In addition, the problem in the on-chip inductors is the required IC area. As can be seen from the chip microphotographs in Chapter 6, the inductors occupy a large area in RF circuits. This increases the cost of the chip and the distances between different circuits or transistors increase if many inductors are used, thus decreasing receiver performance, because losses resulting from the parasitics of the long wiring increase.

A simplified model of the cascode LNA using a resonator load is shown in Figure 3.10 (b). The on-chip inductor is modeled with an inductor, L, having a series resistance R_L; the capacitor, C, includes the parasitic capacitance of the inductors, the mixer input capacitance, the cascode transistor parasitic capacitance, and the on-chip capacitor. R_P is the parallel on-chip resistor, the purpose of which is to adjust the resonator impedance, as will be shown later. In the case of

LNA design, the most significant resonator figure is the impedance, since it determines the gain of the LNA. In the resonator in Figure 3.10 (b), the impedance is

$$Z_r(j\omega) = \frac{1}{\frac{1}{R_P} + \frac{R_L}{R_L^2 + \omega^2 L^2} + j\left(\omega C - \frac{\omega L}{R_L^2 + \omega^2 L^2}\right)} \tag{3. 33}$$

The resonance frequency and the impedance at the resonance frequency are

$$f_r = \frac{1}{\sqrt{LC}}\sqrt{1 - \frac{R_L^2 C}{L}} \tag{3. 34}$$

$$Z(f_r) = \frac{1}{\frac{1}{R_P} + \frac{R_L}{R_L^2 + \omega_r^2 L^2}}. \tag{3. 35}$$

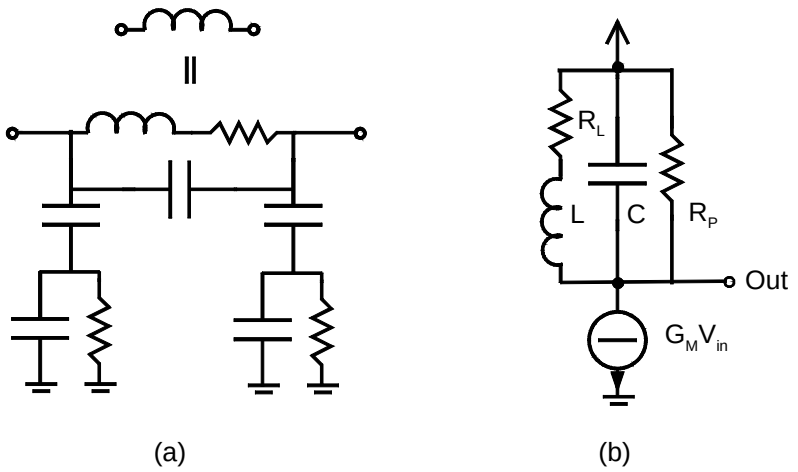

Figure 3.10. (a) Typical model of an on-chip planar inductor. (b) Simplified LNA with a resonator load. R_L represents the series resistance of the inductor.

Thus the impedance of the resonator can be adjusted with the parallel resistance, R_P, or inductance, L. If L is changed the inductance and inductor series resistance, which both affect the impedance are also changed. In addition, the capacitance, C, must be adjusted to keep the resonance frequency constant. The resonator noise at the resonance frequency equals the noise of the resistor calculated using Equation (3.35).

Instead of the impedance of the resonator being used, the resonator is usually defined using a resonator quality factor, Q. The general definition of the quality factor is the ratio of the stored energy and the dissipated energy per frequency cycle in the system

$$Q = 2\pi \frac{energy\ stored}{energy\ dissipated\ in\ one\ oscillation\ cyckle}. \quad (3.\ 36)$$

The quality factor determines the "sharpness" of the resonator. In addition, the Q of the resonator is usually determined using the –3dB bandwidth of the resonator as

$$Q = \frac{\omega_r}{\omega_{-3dB}}. \quad (3.\ 37)$$

For the resonator in Figure 3.10 it can be derived that the Q of the resonator is

$$Q = \frac{R_P\left(R_L + \omega_r^2 L^2\right)}{\left(R_L + \omega_r^2 L^2 + R_L R_P\right)\omega_r} \quad (3.\ 38)$$

If $R_L << \omega^2 L^2$, the Q of the load resonator becomes

$$Q \approx \frac{R_P \omega_r L}{\omega_r^2 L^2 + R_L R_P} \quad (3.\ 39)$$

When the parallel resistor is set to infinity, using Equations (3.35) and (3.39), the impedance of the resonator becomes

$$Z\left(f_r\right) = Q\omega_r L \quad (3.\ 40)$$

Therefore, the maximum gain from the LNA is achieved by maximizing the inductance of the inductor. The maximum inductance is seldom used, because the resonator capacitor is then formed by the parasitic capacitance at the LNA output and the inductor is operating close to its self-resonance frequency. Hence, the resonance is sensitive to process parameters. In addition, large inductance values require more chip area. The DC voltage at the LNA output, when resonator is being used, is, in practice, close to the supply voltage. Thus, the load does not limit the required supply voltage. In addition, the resonator acts as a band pass filter. However, the resonator Q-value must be sufficiently low to cover the whole reception band in all process corners. Therefore, in practice, the filtering because of the load resonator is only marginal.

3.4 LNA biasing

This section concentrates on the biasing of an inductively-degenerated cascode bipolar LNA. The current or voltage references, which track the process parameters, and temperature are not discussed in this thesis. Design issues for these bias references can be found in [8] and [31]. A typical biasing of an inductively-degenerated LNA, which is also used in the experimental circuits, is shown in Figure 3.11. The current flowing through the LNA is determined by the current mirror formed by Q1 and Qb1. The impedance, Zb1, blocks input signal leakage to the biasing circuit and the bias voltage, Vcas, determines the V_{CE} voltages of the input and cascode transistors. If the impedance, Zb1, is realized using a resistor, the resistor, Zb2, is required in order to have an accurate current mirror. The Zb1 can also be realized using an inductor. In this case, the Zb2 is replaced with a short-circuit since there is no voltage drop across the inductor. Since the Zb1 blocks the RF signal, the required inductance value becomes large and in

practice, cannot be realized on-chip. The transistor, Qb2, increases the accuracy of the current mirror, since the required base current for Q1 and Qb1 is not taken from the reference current, Iref. However, it may be necessary to remove Qb2 for low supply voltages, since the current mirror formed by Q1, Qb1, and Qb2 requires a supply which is at least two times the base-emitter voltage. In addition, if the emitter inductor Le is on-chip the series resistance of the spiral inductor effects on the accuracy of the current mirror. There are alternative methods for biasing the LNA. For example, the current of Q1 can be fixed using a current source below the inductor, Le, connecting a capacitor in parallel to the current source to remove the noise from the current source, and make the node between the current source and inductor to signal ground. The proper voltage at the bias node of the Zb1 is required even it does not determine the bias current of Q1. In general, the current through the LNA input transistor can be realized by using a proper impedance, Zb1, and connecting the other end of the Zb1 to a bias voltage.

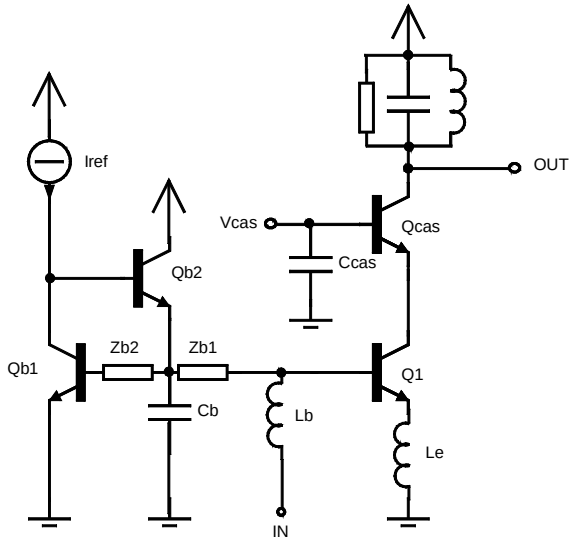

Figure 3.11. Inductively-degenerated LNA including bias.

The effect of the different biasing configurations to the LNA performance, and the sensitivity of the LNA to bias variations with process parameters must be checked during design process. An improper bias arrangement can significantly decrease the LNA performance. The NF of the LNA is increased if the noise from the bias is not properly filtered out. This can be done by using appropriate filtering capacitors as Cb and Ccas, as shown in Figure 3.11. The capacitances, Cb and Ccas, shunt the noise from the biasing to ground. In this case, the blocking impedance is the only component producing noise to the signal path. However, the Zb1 is in parallel to the source resistor, which reduces its noise contribution significantly. The biasing also affects the linearity of an inductively-degenerated LNA. In [20], [32]-[35], the analysis states that the IIP3 of an inductively-degenerated LNA depends on the output impedance of the bias circuit (= Zb1 in Figure 3.11). In [20] it is stated that the output impedance of the bias circuitry should be kept small, relative to r_π, in order to increase the linearity of the transconductance stage. However, the output impedance is typically designed to have a large resistance in order to reduce the noise contribution from the bias circuitry, and to avoid significant loading on the RF input port. References [32]-[35] analyze or use an impedance, which has a frequency-selective output impedance at the biasing circuit to increase the IIP3 of the LNA. The dependence of the IIP3 on the frequency can be observed from Equation (3.27), where the IMD3 term depends on the Δs, which is the difference between the two test tones. For example, the previously mentioned use of an inductor in the bias circuit forms a low impedance

near DC and a high impedance near the RF signal band. Therefore it is difficult to compare different bipolar LNAs if the biasing arrangement is not mentioned. For example, the use of an external bias-Tee can increase the IIP3 of an LNA compared to an LNA with an on-chip bias. A slightly different method used to increase the IIP3 of the LNA by biasing is presented in [36] and shown in Figure 3.12. The biasing is constructed using two different bias paths. The primary biasing is a current mirror and the secondary bias a diode bias feed circuit. With a small signal, the current mirror provides the bias current for the LNA. When the signal is increased, the base current increases and the voltage across the biasing resistor increases, reducing the base voltage. However, as the voltage drops, the current to the base of the input transistor through the diode bias-feed (Qd1) increases, compensating the base-voltage drop. Therefore, the LNA linearity and compression point are both improved.

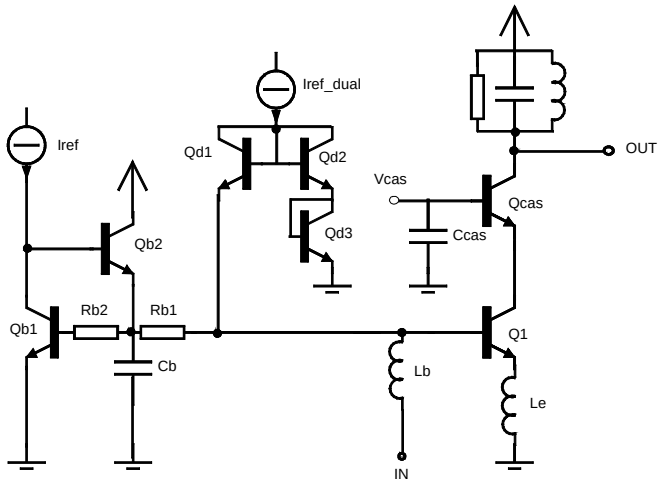

Figure 3.12. Low-noise amplifier with dual bias-feed.

3.5 Single-ended and balanced LNAs

The LNA can be designed as single-ended, balanced, or as a combination of both, i.e. single-ended input and balanced output. The LNA designer cannot always choose between all these configurations since the LNA input and output configurations or networks may be fixed and cannot be altered or redesigned. The LNA input is determined by the pre-select filter or the combination of a pre-select filter and balun, which also determines the input impedance of the LNA. Excluding the LNA, the issues which can determine the type of the pre-select filter are availability, cost, and size. The interface with the mixers and its limitations are discussed in the next section.

What are the benefits and drawbacks of balanced and single-ended structures? When the antenna signal drives a balanced low-noise amplifier through a power-splitting balun, the NF is exactly the same as directly driving the signal into a single-ended version with the same component values. However, the balanced circuit consumes twice the current of the single-ended half-circuit [37]. Hence, the two major problems in balanced structures, compared of single-ended counterparts, are the doubled power consumption and the area at the signal path. The area of the active devices in the LNA is insignificant compared to the area of the whole receiver. The double area becomes a problem if the LNA requires on-chip inductors. The balanced inductively-degenerated LNA requires four on-chip inductors, instead of two in the single-ended version. For example, the area of the experimental balanced single system LNA in

Chapter 6.2 is 0.78mm^2, which is 10-% of the whole receiver chip area excluding the bonding pads. The benefit of using balanced structures is the improved immunity against different spurious tones. The spurious tones, which leak to the supply lines, become common-mode signals. In addition, if the balanced signal paths are drawn close to each other and have very similar environments it is very likely that the spurious signals leaking to these lines will become common-mode signals. The tones which are most likely to cause problems are the harmonics and mixing products of the LO and clock signals. LO leakage is discussed in the following chapters and the clock signal is discussed in Chapter 6 and in [38]. In addition, the benefit of using balanced circuits is that the circuit can share some part of the circuit. For example, the biasing can be shared or a current source can be placed below the emitter inductors. In both cases the noise from these devices becomes common mode and the filtering of noise coming from these circuits is not so critical as in single-ended circuits. The use of balanced circuits is also beneficial in DCRs, especially after the LNA, since the even-order nonlinearities are significantly reduced compared to their single-ended counterparts. In an ideal balanced circuit the IIP2 is infinite. However, due to mismatches, the even-order products appear at the output.

3.6 Interface to mixer

The LNA must be able to drive the designed mixers or an external filter. The mixers which are used in recently-published wireless receivers, are typically based on Gilbert cell-type mixers. Gilbert cell-type mixers provide gain and have a sufficient linearity for wireless applications. A simplified schematic of a Gilbert cell-type mixer which can be used in the DCRs is shown in Figure 3.13. The key issue for the LNA designer is the configuration of the mixer input transistors. The mixer is based on two switching pairs, Q1-Q4, and the input transistors, M1-M2. The mixer input signal can be differential or single-ended if the other input is properly AC-grounded. In addition, the input transistor is part of the LNA load, as discussed previously. Thus, it must be taken into account with simulations. If the LNA uses a resonator load, the mixer input capacitance shifts the resonance to lower frequencies unless properly designed. In Figure 3.13, a DC blocking capacitor is placed between the mixer input transistor and LNA output. In the previous chapter, it was stated that the IIP2 of the LNA is not a major issue. This is because, in theory, the low-frequency term (f_1-f_2) that is generated in the LNA is upconverted in the mixer, and therefore is not at the same frequency as the desired signal. However, the isolation between mixer signal input and output is not infinite. Hence, the second-order nonlinearity generated by the LNA leaks to the mixer output and can decrease the IIP2 of the whole receiver. The blocking capacitor increases the low-frequency isolation between the mixer input and output, which improves the IIP2 of the receiver [39].

Depending on the mixer input and pre-select filter output, a single-ended-to-differential conversion may be required in the LNA. In this case, the converter must be taken into account in system simulations as a separate block or the LNA-converter combination must achieve the performance given to the LNA. Figure 3.14 shows a few examples of how to implement this conversion. The passive transformer in Figure 3.14 (a) uses two coupled inductors. This solution requires the accurate modeling of the transformer [40]. Thus, the use of transformers in the linearization of the LNA as in [41], was also excluded. If an active transformer, as shown in Figure 3.14 (b), is used, it must be noted that the power dissipation of the LNA-balun combination can be equal to that of a fully-differential LNA. A similar active balun is used in one of the experimental circuits in Chapter 6.3. However, in this case, the balun was mainly needed to combine several systems into a single silicon chip.

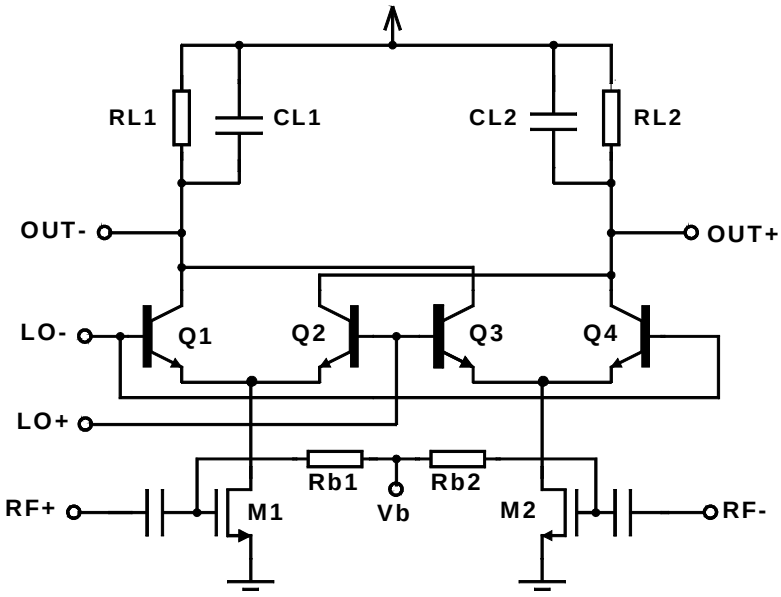

Figure 3.13. Schematic of a Gilbert cell-type mixer.

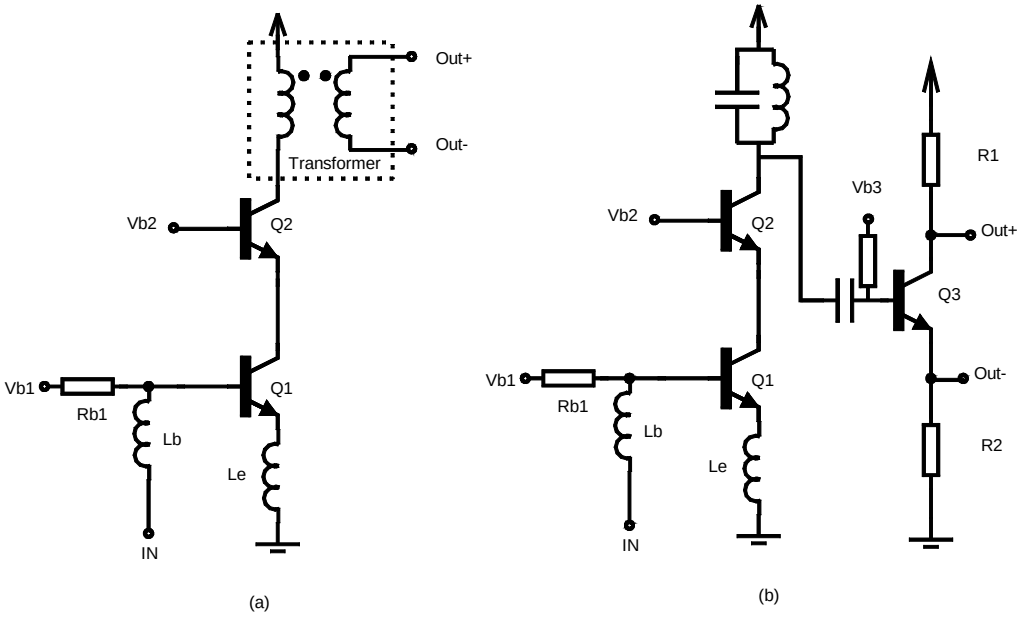

Figure 3.14. Schematic of an inductively-degenerated LNA, which has (a) a passive and (b) an active single-ended-to-differential converter.

A different approach to the design of the LNA-mixer interface is the stacking of the two blocks, as shown in Figure 3.15. In this case, the LNA and the mixers use the same DC current flowing through the blocks, which reduces the power dissipation of the RF front-end compared to a front-end with separate blocks. This configuration is used, for example, in [42]. This configuration is suitable for transceivers which have sufficiently large supply voltages and

when the supply requirement is limited by other blocks than the LNA and the mixers. The trend of using supplies that are as low as possible tends to limit the use of this type of front-end, which is also the case in the experimental circuits. The problem with a low supply can be solved using a structure presented in [43] and [44], where the front-end is simply a common-base stage driving a switching quad. This configuration can be designed to operate from supply voltages as low as the Gilbert cell-type mixer. However, this configuration has one gain stage less than the previous one, which limits its usage in wireless telecommunication applications. Thus is was not used in the experimental circuits.

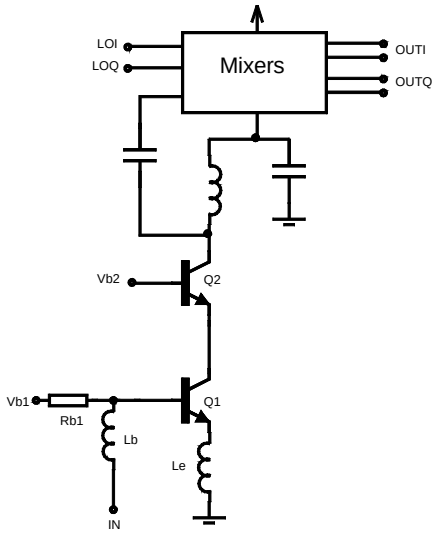

Figure 3.15. Simplified schematic of a stacked LNA-mixer

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4 Design of multi-mode low-noise amplifiers for DCRs

This chapter concentrates on multi-mode LNA design. The input stage, load, and interface to the mixer are discussed in detail. The target in multi-mode LNA design has been to achieve as similar a performance as possible compared to single-system LNAs. The focus is on the inductively-degenerated LNA. This choice was justified in the previous chapter. In addition, design issues relating to the interference between different wireless systems are discussed.

4.1 Multi-mode input stage design

In this thesis, the focus is on receivers, which choose an appropriate system for the application requested. Thus, only one system is operational at a time. In Chapter 2, justification was given for why this type of receiver was chosen for the experimental circuits. Before going into the details of circuit design, possible configurations for the pre-select filter-LNA interface are discussed. Figure 4.1 shows possible configurations on the LNA input interface. Figure 4.1(a) illustrates a receiver which includes an adjustable or programmable pre-select filter, which can be adjusted according to the operational system. In all probably, this solution would be optimal for the receiver described above, since the pre-select filter would pass only the signals of the operational system. However, this solution suffers from a few drawbacks which prevent its usage in practice in existing solutions. In addition to the adjustment of the filter frequency response, the matching impedance should be kept well-defined (or constant) in all reception bands and the loss in the filter passband should be low. Furthermore, the LNA input should be matched in all reception bands and, obviously, it should have a performance appropriate for the chosen system. Figure 4.1(b) illustrates a receiver which has a different type of pre-select filter compared to the previous receiver. The pre-select filter in this receiver is a multi-band structure. This type of filter can be found in [1]. However, this kind of filter may not be optimal for the receiver described above. The problem with this filter is related to interference between the different systems. The different signals and their mixing products, which may appear at the LNA input in DCRs, are

$$f_{input} = \pm mf_{RF} \pm nf_{LO} \pm kf_{CLK} \pm lf_{TX} \pm tf_{SYS,j}\,, \tag{4. 1}$$

where f_{RF} is the desired RF signal, f_{LO} the local oscillator signal, f_{CLK} the clock signal, f_{TX} the transmitter signal, and $f_{SYS,j}$ are the signals from different systems which can pass through the multi-band pre-select filter. The factors m, n, k, l, t, and j are constant positive integers. When the number of different systems increases, the number of possible interfering signals that may cause the signal quality to deteriorate increases. These interfering signals are also observed at the LNA input in the previous configuration, shown in Figure 4.1(a). However, only the signals of the operational system are within the passband of the pre-select filter. Thus, the interferences from additional systems are decreased to LNA input compared to the receiver in (b). In addition, the LNA input in Figure 4.1 (b) has similar requirements as the previous receiver. This type of receiver is optimal for concurrent reception, where the signals of at least two wireless systems are received simultaneously.

Figure 4.1 (c) and (d) illustrate receivers, which have switched parallel pre-select filters for different systems. The difference between these two is that the receiver in (c) has a single input and the receiver in (d) has a separate input for each system. All inputs in the multi-input receiver (d) can be separately optimized, which is beneficial compared to the single-input

configuration. In addition, if several inputs are used, the isolation between different systems can be increased. However, the multi-input solution requires more chip area and more parallel devices, which increases the cost of the chip. If the parallel pre-select filters (c) and (d) are compared to the single multi-mode filter (a) and (b) the parallel structure is more flexible. If one system is added or removed, which may be required in different market areas, only one parallel filter is removed or added. In the single-filter case, the whole filter must be re-designed. However, the use of a single filter may be cheaper and require a smaller area than parallel pre-select filters.

The four configurations in Figure 4.1 do not include all the variations of this type of receiver. For example, the first receiver (a) may have several inputs instead of only one multi-band input. The switch in (c) may be removed or moved to the other side of the pre-select filter. In addition, all the receivers in Figure 4.1 include only one antenna. This thesis does not discuss antenna design or whether this kind of solution is optimal or possible with current technologies. All four structures and the variations between these were considered in the design of the experimental circuits. The selected input interface is based on the approach in Figure 4.1(d), because of its benefits, which are described in this chapter.

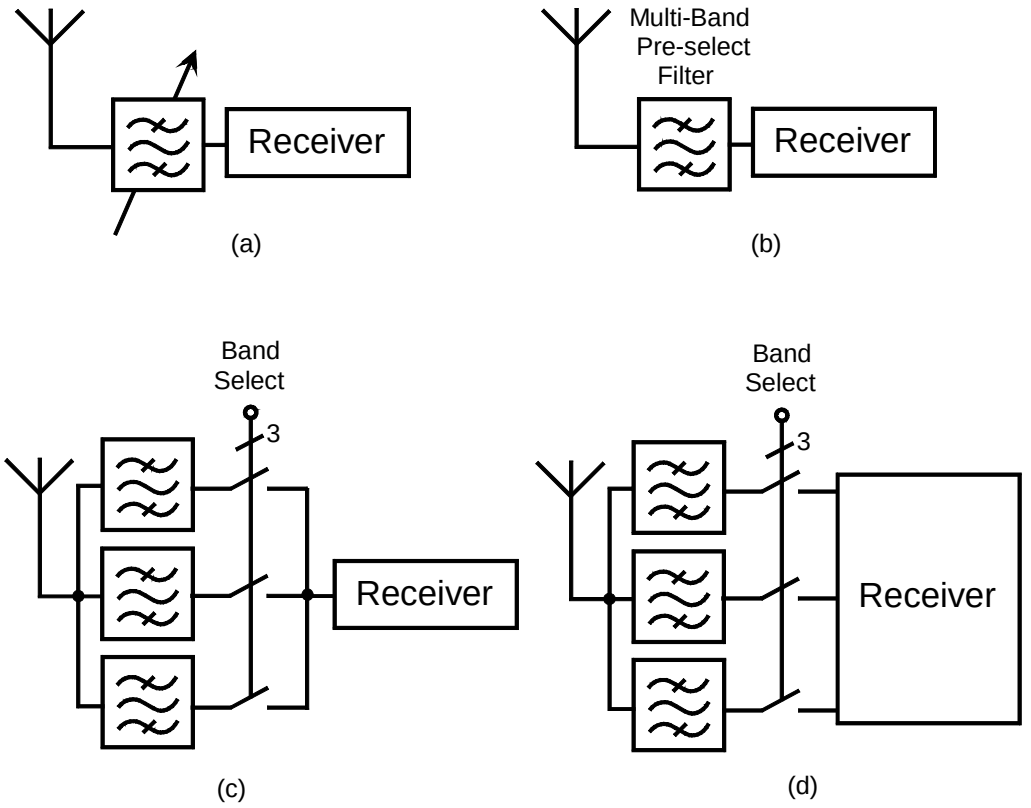

Figure 4.1. Block diagram of different possible configurations for the stage preceding the LNA.

The previous configurations are all feasible for multi-system reception. However, as this chapter discusses the design of a multi-mode LNA, the receiver in Figure 4.2 must be

mentioned. The receiver in Figure 4.2 is designed to operate in different reception bands or systems. However, compared to the receivers in Figure 4.1, the operational system is already selected at the manufacturing stage. Thus, different reception bands or systems cannot be selected with different control codes. Although this type of receiver may not be optimal for future mobile phones, it may be used, for example, in base station (BS) applications. A BS is designed to operate in one system but, because of IC design costs, it may not be optimal to design a dedicated IC for all the different BS receivers. In addition, this type of receiver may include different external components which cannot be used in the previous receiver configurations. For example, a different type of bonding diagram may be used, depending on the system in which the receiver is targeted.

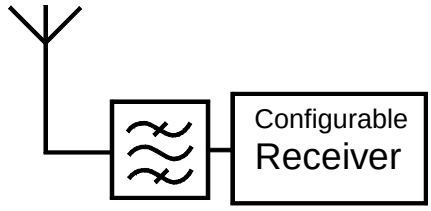

Figure 4.2. Single-system configurable receiver.

Figure 4.3 illustrates two different input-stage configurations for an inductively-degenerated LNA. The matching and noise of these two topologies will be compared. The LNA in Figure 4.3(a) uses one input and output for all systems, and the LNA in (b) uses parallel structures for different systems. The input matching in (a) depends on the receiver configuration. If the receiver configurations of Figure 4.1(a)-(c) are used, the input matching must be achieved in all reception bands. However, if the receiver in Figure 4.2 is used, the input matching for different band can be adjusted with external components at the manufacturing stage, because the receiver operates in one system after manufacturing stage. If L_b is replaced by Zin in Equation (3.5), the matching of the LNA becomes

$$Z_{in} = \frac{g_{m,T} L_e}{C_\pi} + Zib + j\left(\omega L_e - \frac{1}{\omega C_\pi}\right). \tag{4. 2}$$

Zib is the impedance between the input and the base of the input transistor. Zib must be a reactive component in order to avoid the degradation of NF. Hence, at the matching frequency,

$$Zib + j\left(\omega L_e - \frac{1}{\omega C_\pi}\right) = 0. \tag{4. 3}$$

In [2] the input matching of two different reception bands is achieved by adding a parallel LC resonator between the RF input and base inductor; this is shown in Figure 4.4. Thus, the matching is achieved at the frequencies

$$\omega_r = \sqrt{\frac{\left(L_b + L_e\right)/L_r + C_r/C_\pi + 1 \pm \sqrt{\left(\left(L_b + L_e\right)/L_r + C_r/C_\pi + 1\right)^2 - 4\left(L_b + L_e\right)C_r/C_\pi L_r}}{2\left(L_b + L_e\right)C_r}}, \tag{4. 4}$$

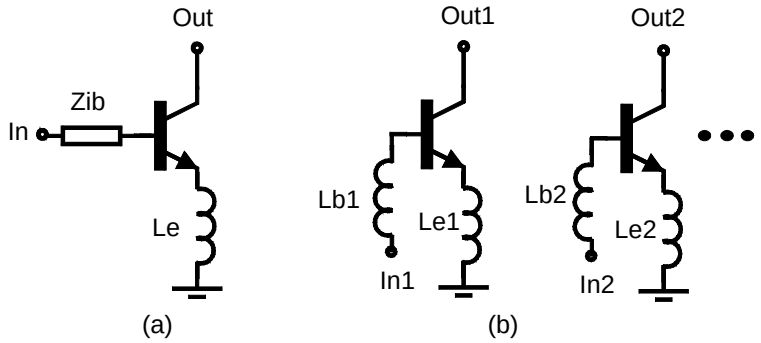

Figure 4.3. Input stage of an inductively-degenerated multi-mode LNA using (a) a single-input and (b) a multi-input configuration.

where L_e and L_b are the base and the emitter inductors, C_π is the base-emitter capacitor, and L_r and C_r form the parallel resonator before the base inductor. Assuming that

$$\frac{(L_b + L_e)}{L_r} + \frac{C_r}{C_\pi} >> 1, \tag{4. 5}$$

the resonance frequencies become

$$f_{r1} = \frac{1}{2\pi\sqrt{L_r C_r}} \qquad f_{r2} = \frac{1}{2\pi\sqrt{(L_b + L_e)C_\pi}}. \tag{4. 6}$$

Thus, using the assumption above, it can be seen from Equation (4.6) that one resonance is formed by the parallel resonator L_r and C_r and the other resonance is at the same frequency as in single-system LNAs. If the receiver in Figure 4.2 is the design target, depending on the target system, all that need to be done is to choose an appropriate inductor as Zib in the manufacturing stage.

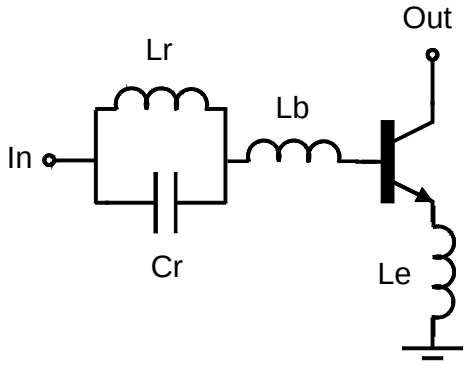

Figure 4.4. Inductively degenerated LNA with dual-frequency matching.

The drawback of using a single-transistor input is the increased NF. Figure 4.5 and Figure 4.6 illustrate the minimum NF_{min} and the optimum source resistance at 1GHz and 2GHz for the transistor which was used in the experimental circuits. It can be observed that the NF_{min} and $R_{s,opt}$ are achieved at different transistor collector currents. Thus, at a constant collector current the optimal performance is achieved in one frequency band only. In addition, the optimum

NF_{min} cannot be achieved simply by using an adjustable input transistor biasing, because this would change the input matching. In order to optimize transistor performance in several frequency bands, an adjustable base-emitter capacitor or emitter inductor would be required, which is very difficult to implement in practice, as shown later in this chapter. Another drawback of the configuration illustrated in Figure 4.4 is the increased number of off-chip components, such as Lr and Cr, which increase the size and cost of the receiver.

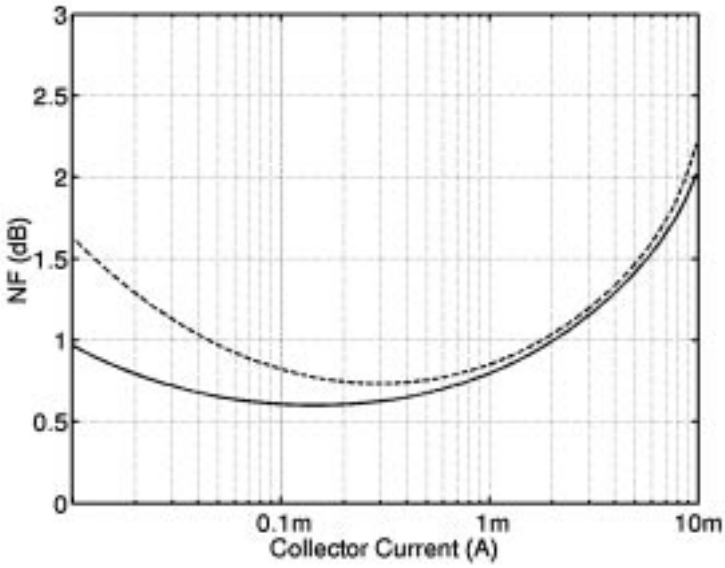

Figure 4.5. Minimum NF as a function of the collector current at 1GHz (solid) and 2GHz (dashed) frequencies.

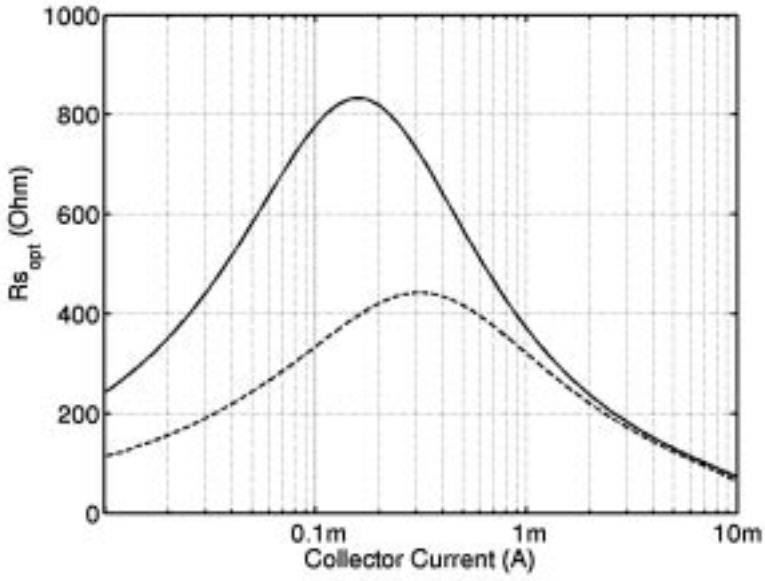

Figure 4.6. Optimum source resistance as a function of the collector current at 1GHz (solid) and 2GHz (dashed) frequencies.

Each system in the multi-mode LNA shown in Figure 4.3 (b) can be optimized separately, as in a single-system LNA. Thus, there is no need for any compromises between the different systems. Furthermore, in theory there is no interaction between the different systems at the LNA input. The drawback of this configuration is the number of inductors required. Each system requires a separate base inductor, bonding pad, and emitter inductor, which increases the chip area. In this configuration, the chip area easily becomes too large when the number of different systems is increased. The problem of the number of emitter inductors can be reduced by sharing these inductors as in Figure 4.7(a), where the dual-system LNA shares the emitter inductor, Le1. In order to get an approximation of the effect of the second input on LNA performance, the non-operational input device, which is not conducting, is modeled with a capacitor, C_{par}, and a resistor, R_{par}, in series, as shown in Figure 4.7(b). In this case, the input matching becomes

$$Z_{in} = \frac{g_{m,T} L_e \left(1 + R_{par}\right)}{C_\pi \left(1 + R_{par} - \omega^2 L_e C_{par}\right)} + j\left(\omega L_e - \frac{1}{\omega C_\pi} + \frac{1}{\frac{1}{\omega L_e} - \frac{\omega C_{par}}{1 + R_{par}}}\right). \quad (4.7)$$

It can be seen from Equation (4.7) that with a small R_{par} and a large C_{par} the device can become unstable and matching becomes impossible. The model shown in Figure 4.6(b) is very simplified and, in practice, LNA performance must be checked using a circuit simulator. The different systems have frequency-selective components and different types of biasing configurations may be used, which affects LNA performance.

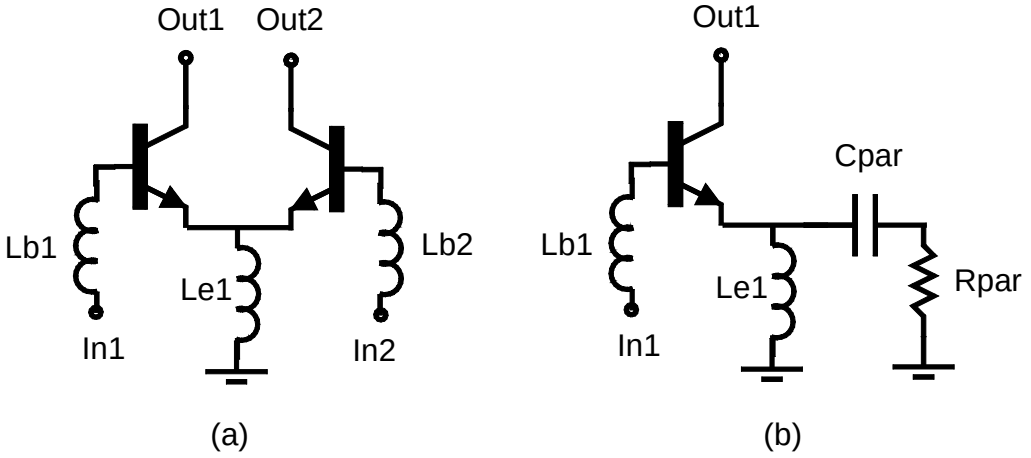

Figure 4.7. (a) Dual-system inductively-degenerated LNA. (b) A simplified model of the circuit in Figure 4.7(a) with the second input (In2) non-active.

4.2 Load in multi-mode LNAs

The load of a multi-system LNA must be appropriate at all operating frequencies. If the operating frequencies and the capacitance at the LNA output are small, a resistive load is an alternative. In the experimental circuits, the fact that the operating frequencies of the selected systems were a few GHz made this solution impossible. In addition, the resistive load has other

drawbacks, as was explained in the previous chapter. Different resonator topologies represent alternative ways to implement the load of the LNA. The solutions considered in this thesis are separate resonators, a multi-band resonator, and an adjustable resonator. Examples of multi-band and adjustable resonators are shown in Figure 4.8; they were used, for example, in [2] and [3]. The resonance frequencies of the multi-band resonator are

$$\omega_r = \sqrt{\frac{C_2/C_1 + L_1/L_2 + 1 \pm \sqrt{\left(C_2/C_1 + L_1/L_2 + 1\right)^2 - 4C_2L_1/C_1L_2}}{2C_2L_1}} \tag{4. 8}$$

By assuming

$$\frac{C_2}{C_1} + \frac{L_1}{L_2} >> 1, \tag{4. 9}$$

the resonator in Figure 4.8 (a) has resonance at

$$f_{r1} = \frac{1}{2\pi\sqrt{L_1C_1}} \qquad f_{r2} = \frac{1}{2\pi\sqrt{L_2C_2}}. \tag{4. 10}$$

The challenge in this structure is to adjust the impedances at the resonance frequencies to appropriate levels by using on-chip inductors. The impedances at resonance frequencies become

$$Z(f_{r1,r2}) = \frac{1}{\dfrac{R_{L1}}{R_{L1}^2 + \left(\omega_{r1,r2}L_1 - 1/\omega_{r1,r2}C_1\right)^2} + \dfrac{R_{L2}}{R_{L2}^2 + \omega_{r1,r2}^2L_2^2}}, \tag{4. 11}$$

assuming that both inductors L_1 and L_2 have series resistance R_{L1} and R_{L2}, respectively. From Equation (4.11) it can be seen that the losses in both inductors affect the resonator impedances at both resonance frequencies. Thus, accurate models of the on-chip inductors are required.

The adjustable resonator shown in Figure 4.8 (b) has a limited tuning range as a result of impedance reduction. Excluding the effect of the switch transistor, the impedance of the resonator is given in Equation (3.35). Thus, if the resonance is adjusted to a lower frequency using a capacitor, the impedance of the resonator decreases. For example, if the resonance is adjusted to half of the original, the voltage gain of the LNA is reduced by approximately 12dB. A similar effect to the voltage gain of the LNA can be seen in Figure 4.9, where the resonance is shifted from 2GHz to 1GHz with an additional capacitor and scaled to 0dB at 2GHz. The effect of the impedance reduction can be compensated by adding an adjustable resistor in parallel with the resonator. Thus, according to Equation (3.35), it can be noted that if the resistor value, R_p, is increased, the impedance of the resonator increases. However, in practice, the usability of this compensation scheme is limited. At the highest resonance frequency, the resistor with the lowest value must be connected to the resonator to achieve constant resonator impedance over the entire tuning range, which may lead to too low a resonator impedance.

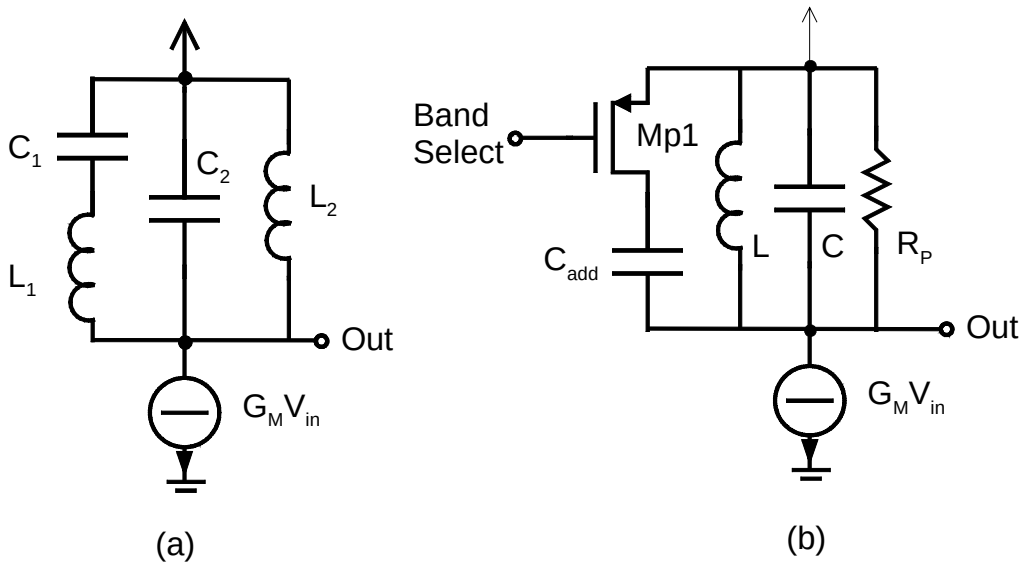

Figure 4.8. LNA with (a) a dual-band resonator load and (b) an adjustable dual-band resonator.

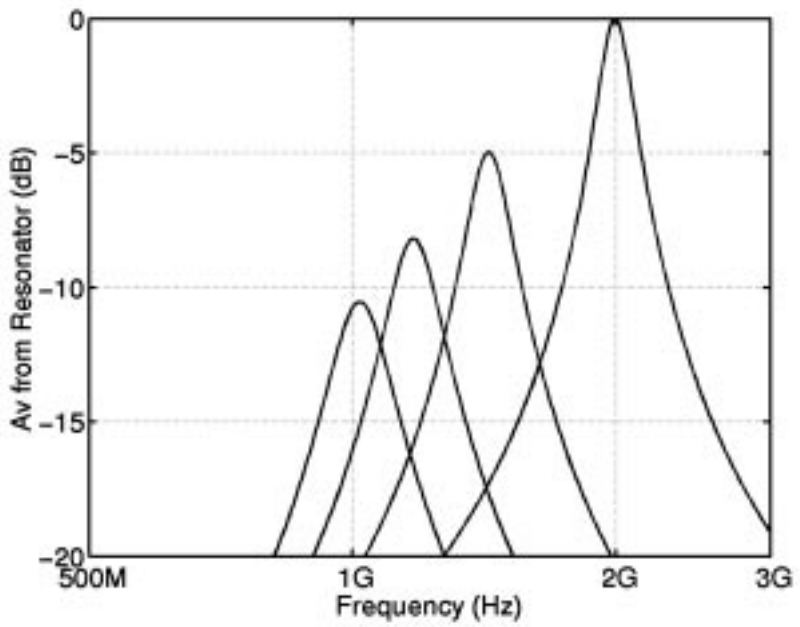

Figure 4.9. Effect of capacitor adjustment on the voltage gain of the LNA in decibels. The capacitor values are 2pF, 4pF, 6pF, and 8pF, and the inductor value is 3nH. The inductor uses a detailed model used in the experimental circuits.

Depending on the load chosen, the load can be connected to the LNA input stage using different circuit configurations. A multi-band or wide-band load can be directly connected to the output of the single-input LNA in Figure 4.4 without additional devices. If different loads are designed for different frequency bands, an LNA with several outputs, as in Figure 4.7 (a) can be used without any modifications. The appropriate load is connected to the LNA output designed for

this operating frequency. Examples of other load and input stage combinations are illustrated in Figure 4.10. In Figure 4.10 (a), two loads, which can be, for example, two differently-sized resonators, are connected to the single-input LNA using switched cascode transistors. In Figure 4.10 (a), the load-select signal controls which load and which output is operational by steering the signal current through Qc1 or Qc2. In Figure 4.10 (b), two LNA input stages, which are used at different reception bands, are connected to a single load, which can be, for example, one of the loads illustrated in Figure 4.8. In a receiver which uses only one system at a time, the non-operational input can be biased off to reduce the power consumption. The signal path in (b) can also be combined at the collectors of the input transistors, as in Figure 4.11, which decreases the number of cascode devices. However, this solution decreases the isolation between the different RF inputs and increases the capacitance at the collector of the input transistor, which increases the NF of the LNA, as shown in Equation (3.31).

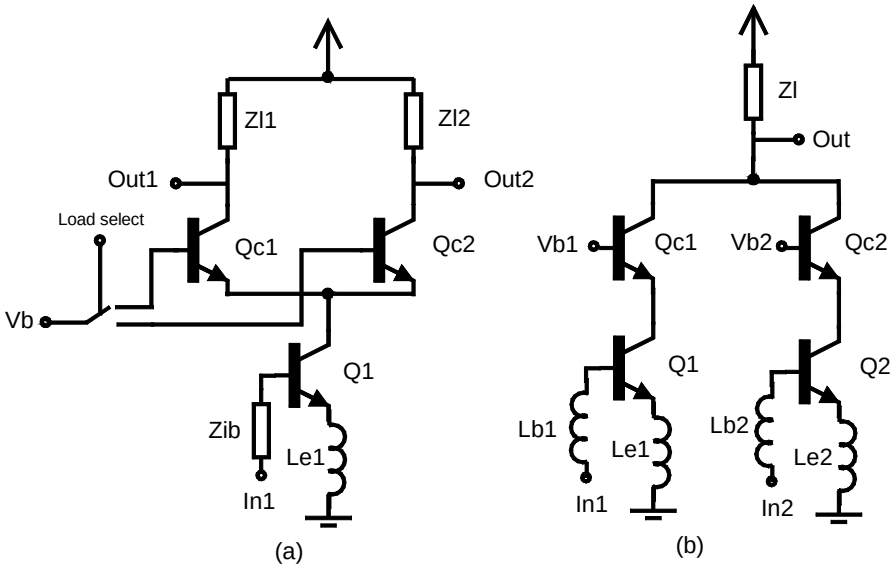

Figure 4.10. (a) Single-input, dual-load LNA (b) Dual-input, single multi-band load LNA.

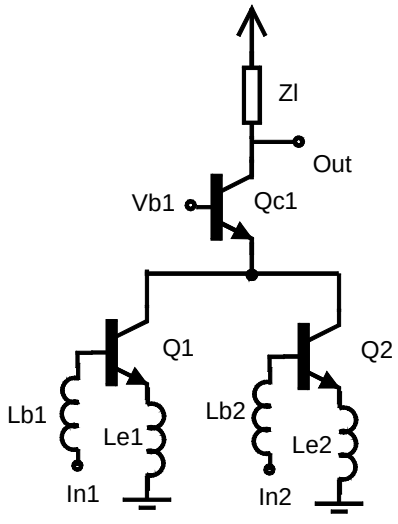

Figure 4.11. Dual-input LNA with combined load and cascode transistor.

4.3 LNA and mixer interface

In a multi-mode DCR LNA, the interface to the quadrature mixers may require additional devices for proper receiver operation. If the LNA has only one output, it can be connected to the mixer in a similar manner as in single-system receivers. In general, the Gilbert cell-type mixer is a wide-band circuit. However, in practice, the mixer input has a finite operating bandwidth. Thus, if systems with very large frequency differences are connected to the same mixer input, the mixer performance may not be optimal for all systems. The design of the LNA-mixer interface becomes more challenging if the LNA has several outputs for different systems. Figure 4.12 illustrates possible ways to combine several RF inputs to the same signal path. In Figure 4.12 (a), several RF front-ends are in parallel and the signal path is combined in the baseband. The combination of the signal paths in the baseband depends on the blocks which are needed in the baseband in different modes. For example, if the baseband signal path is the same in all modes, the signal combination can be placed at the mixer output. For RF design, this approach is straightforward, since each block can be separately optimized and designed. However, this approach increases the chip area, which is at least the area of a single-system front-end times the number of parallel front-ends. The power consumption of this type of front-end does not increase if only one system is activated at a time and the others are biased off. In Figure 4.12 (b), the different outputs from the LNA are combined using an additional combiner/buffer. For example, this buffer may be required because a direct connection between the two differently-sized parallel resonators would form a single resonator. The benefit of this structure is that only one pair of quadrature mixers is needed, which reduces the chip area. However, the active buffer consumes power, increases noise, and reduces linearity, which must be taken into account. In general, a front-end with a buffer must be designed to meet the same specification as a receiver without one. Figure 4.12(c) illustrates a receiver in which the LNA outputs are directly connected to a multi-input mixer. Compared to the previous configuration, the current-consuming buffer is removed. The challenge in this configuration is the multi-input mixer design.

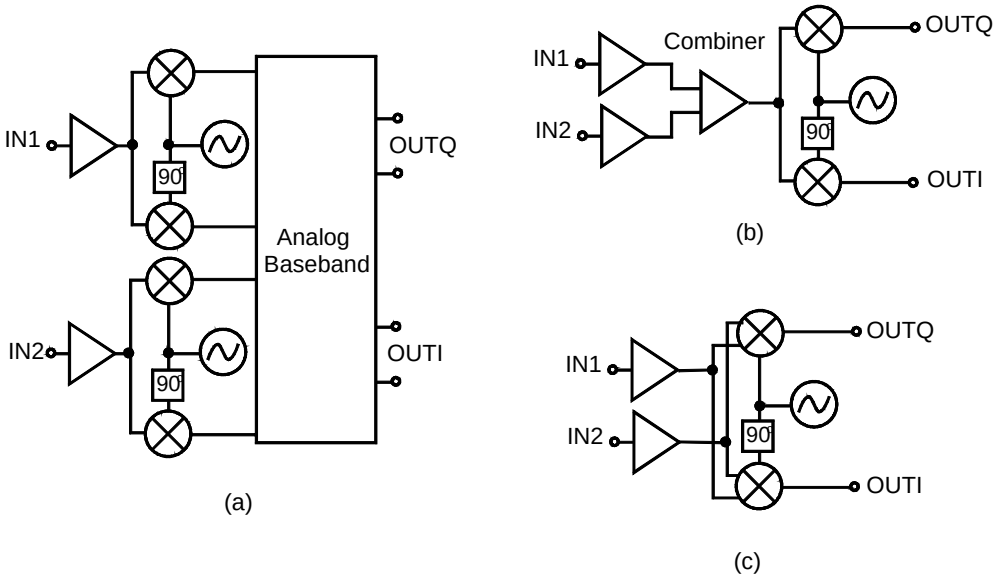

Figure 4.12. Different ways to combine the signal paths from a dual-output LNA. (a) Combining in the baseband. (b) Combining using a buffer between the LNA and the mixer. (c) Combining using a dual-input mixer.

Examples of the combiner buffer and dual-input mixer are shown in Figure 4.13. Circuits which are based on these configurations were used in the experimental receivers presented in Chapter 6. Figure 4.13 (a) illustrates a buffer which combines the two LNA outputs. In addition, it performs a single-ended-to-differential conversion to enable the use of single-ended LNA and double-balanced mixers. The two LNA outputs are connected to RF1/Vb1 and RF2/Vb2. Using switched biasing, which turns on either of the two transistors, Q11 or Q12, one of the LNA outputs is connected to the mixer inputs. In Figure 4.13 (b), a possible implementation of a dual-input mixer is shown. Without the transistor, M12, the mixer is a Gilbert cell-type mixer with a single-ended input and double-balanced switching quad. The selection between the two LNA outputs is performed by biasing either of the transistors, M11 or M12, on. The additional input also changes the impedance at the emitters of the switching pairs. This may increase the receiver NF since the noise from the LO is not fully common-mode at mixer output. Thus, this difference between the two impedances at the emitters of the switching pairs should be minimized. This can be achieved, for example, by using an additional dummy transistor at the emitter of the other switching pair.

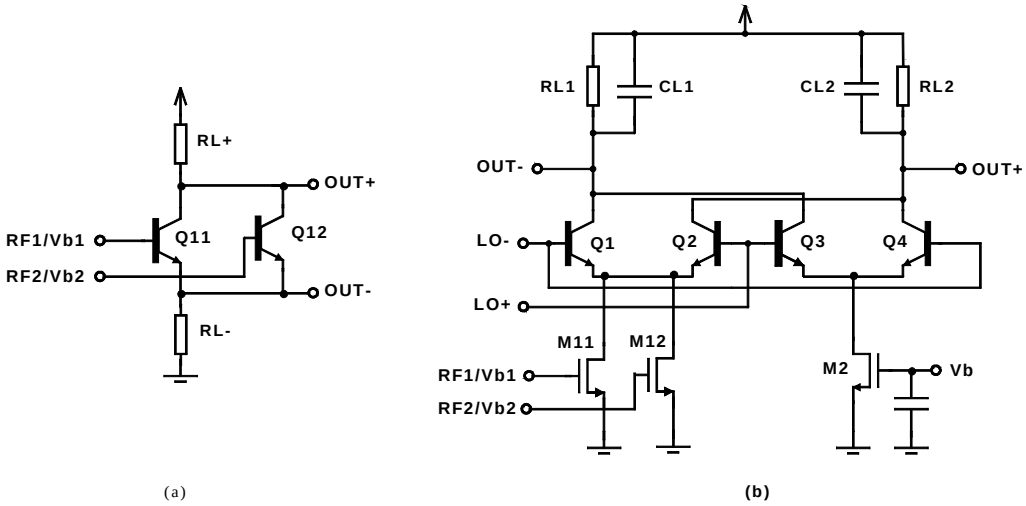

Figure 4.13. (a) Buffer and a single-ended-to-differential converter combining the two LNA outputs. (b) A dual-input Gilbert cell mixer.

4.4 Interference between different systems

In single-system DCRs the possible mixing products, which can corrupt the signal-to-noise ratio are a combination of the LO signal, TX signal, CLK signal, and signals in the passband of the pre-select filter. Depending on the receiver input configuration, the spurious tones from the non-operational system can be decreased by means of appropriate LNA design and by selecting an appropriate pre-select filter. If the DCR uses a single-input multi-band configuration, as shown in Figure 4.4, the effect of the spurious tones can be reduced either by using a properly-selected pre-select filter, which passes only through the reception band of the operational system, or by designing an LNA which filters out signals from the non-operational reception band. Thus, the pre-select filter should be either a programmable filter, as shown in Figure 4.1 (a), or a combination of parallel switched pre-select filters, as shown in Figure 4.1 (c). To reduce the interference in the LNA, a single-input inductively-degenerated LNA, as shown in Figure 4.14, is discussed. The LNA must achieve good matching, voltage gain, linearity, and

power consumption at each operating frequency. Since the LNA uses a single input transistor, the filtering of the signals from the non-operational band must be carried out with adjustable/selectable input-matching and/or adjustable/selectable load impedance. The design of adjustable or selectable input matching is difficult or impossible with current on-chip devices. For appropriate matching in different frequency bands, the impedances, Zib and Ze, should be adjustable or selectable. If the multi-resonance input, as shown in Figure 4.4, is excluded, the impedance for different systems must be formed using differently-sized inductors as in single-system LNAs, or using switched capacitors together with the base inductor. An adjustable inductor or capacitor must be formed using active devices, and a selectable inductor or capacitor would require switches. Both of these approaches will lead to a too-high NF in the LNA. For example, if the switched input impedance, Zib, is formed using parallel inductors, as shown in Figure 4.15, the NF of the LNA will increase by 0.8 dB if a 10Ω on-resistance is assumed for each switch in a 50Ω matching environment. In addition, if the matching inductor is realized using a bond wire, each inductor will require a separate bonding pad and bond wire. The interference in a single-input LNA can also be increased using an adjustable or a switched load. For example, the LNA shown in Figure 4.10 (a) has such a configuration. The benefit of this configuration depends on the frequency difference between the operating systems. If the operating systems have a small frequency difference the on-chip load resonator will pass through the non-operational system with only a small gain difference because of the low Q of the resonator. In addition, if the LNA has multi-band matching instead of adjustable or selectable matching, the spurious tones generated in the nonlinear input transistor can corrupt the signal-to-noise ratio before the signal passes to the LNA load.

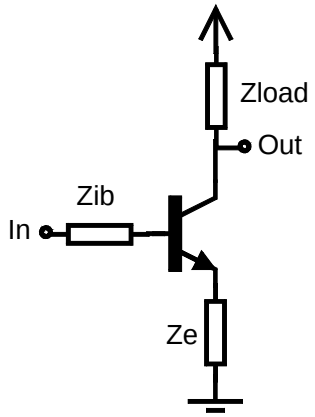

Figure 4.14. Multi-band single-input degenerated LNA.

In a DCR which uses a multi-input LNA or parallel LNAs, additional design methods for reducing the effect of the interference between different systems, compared to a single-input multi-band DCR, can be found. Figure 4.16 illustrates signals which can leak to a non-operational input and signals which can leak from the non-operational input to different receiver blocks and corrupt the signal-to-noise ratio. In practice, the leaked signals at the receiver inputs are the same as in a single-system receiver with additional signals caused by different systems. The possible signals at different inputs are given in Equation (4.1). The level on the additional spurious tones, compared to single-system receivers, depends of the isolation between the different RF inputs and isolation between non-operational input to other disturbing signals. For example, in theory, if the receiver uses perfectly parallel signal paths and the isolation between different signal paths is infinite, there is no interference between different systems and the spurious tones at the receiver input are similar to those in single-system receivers.

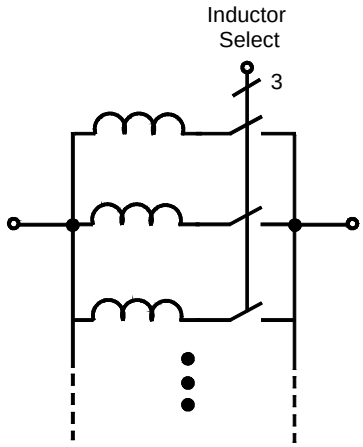

Figure 4.15. Selectable inductor.

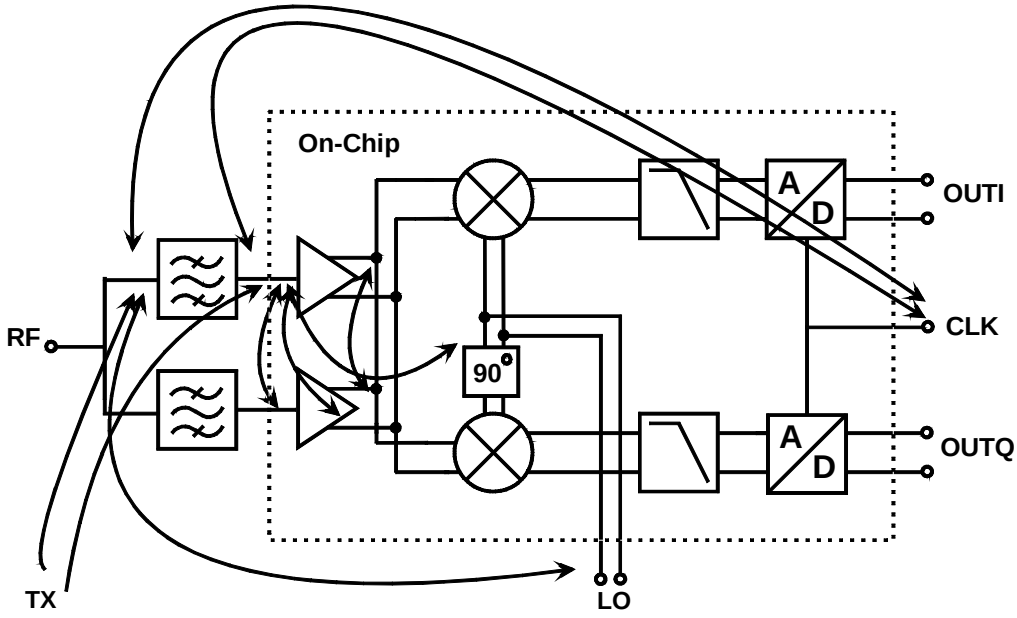

Figure 4.16. Interference between different systems in multi-input DCR.

The isolation can be increased using switched structures, additional devices, or a different type of IC layout. The switched structures in this case are defined as devices or blocks which are on or off depending on the operational system. Without switched structures, the spurious signals which appear at the input of the non-operational LNA are increased to the output of the non-operational LNA. Thus, the levels of the possible spurious tones, which can deteriorate the signal quality, are increased on the chip. To maximize this isolation, the devices in the signal path of the non-operational system should be turned off. The improvement in isolation using additional devices is based on the separation of the signal-paths of different systems or on the adjustment of frequency-selective structures. In practice, the separation of the signal-paths is performed using parallel structures, which have the effect of increasing the chip area, especially if the number of on-chip inductors is increased. With the adjustment of frequency-selective

components, the isolation is improved as a result of the better filtering of the spurious tones. For example, if an adjustable resonator is used instead of a resonator with a low Q, the level of the spurious tones can be decreased. Finally, the isolation between the different systems can be increased with different layout structures. Isolation in layout can be improved in similar way to that in which the spurious tones in single-system DCRs are reduced. The isolation can be improved, for example, with orthogonal wiring, or by using isolating wells between different blocks. However, it must be noted that if the isolation between the two systems is improved, the isolation from other disturbing signals may be decreased. For example, if two inputs of different systems are drawn orthogonally, the LO-to-RF isolations into the two system inputs are different. Details of the layout issues can be found in Chapters 3 and 5.

4.5 Recent publications describing multi-mode LNAs

Compared to single-system receivers, the recent publications describing circuits, which are targeted for multi-mode or multi-band receivers, have only a few shared components. In references [4], [5], [6], [8], and [10], parallel LNAs are used for different signals. The only difference to single-system LNAs may be in the dimensioning of the different LNAs or shared controls. For example, the operational LNA can be chosen with different control codes. In references [7], [9], [11], [12], [13], and [14], a slightly higher level of component sharing is achieved by using only one LNA for systems which have a small difference between different reception bands, for example, DCS1800 and PCS1900. Compared to single-system LNA design, the reception band of this LNA must be slightly broader. Furthermore, in references [7] and [9], the shared LNA includes a gain control to meet the different system standards with the same LNA. References [2], [15], and [16] describe the design of LNAs, which have shared components between systems with a large difference between their reception bands. The solutions used in these LNAs were described and referenced earlier in this chapter. In addition, a detailed description of the LNA design of [15] and [16] is given in Chapter 6.

4.6 References

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5 Variable gain in inductively-degenerated LNAs

The maximum LNA gain is determined by the receiver noise figure and linearity requirements, as explained in the previous chapters. These requirements are usually specified for a received signal, which is close to the sensitivity level. However, the analog receiver must also be able to tolerate high signal levels, for example, when the mobile station is close to a base station. This requirement can be taken into account simultaneously when the NF and linearity are determined. Hence, the receiver is designed to receive different signal levels without any modifications. For example, the input-referred compression point is sufficient for all signal levels. An alternative way to achieve this requirement is to use different gain settings in the receiver. If the receiver signal is not at the sensitivity level, the NF of the receiver is allowed to increase simultaneously. The variable gain can be implemented both in the RF and/or baseband circuits. This chapter describes different ways to implement the variable gain on an inductively degenerated LNA. In addition, this chapter describes the DC offset problem, which is related to DCRs having variable gain in a continuous time system, such as WCDMA.

5.1 Analog and digital gain control

Variable gain in an RF front-end can be implemented using either analog or digital control. In this thesis, analog adjustment means that the RF front-end can have all the gain values between the maximum and minimum gain settings, and a digitally-adjusted RF front-end can be programmed only to different discrete gain settings. Figure 5.1 illustrates the RF front-end voltage gain as a function of a control code or control voltage for digital and analog gain controls.

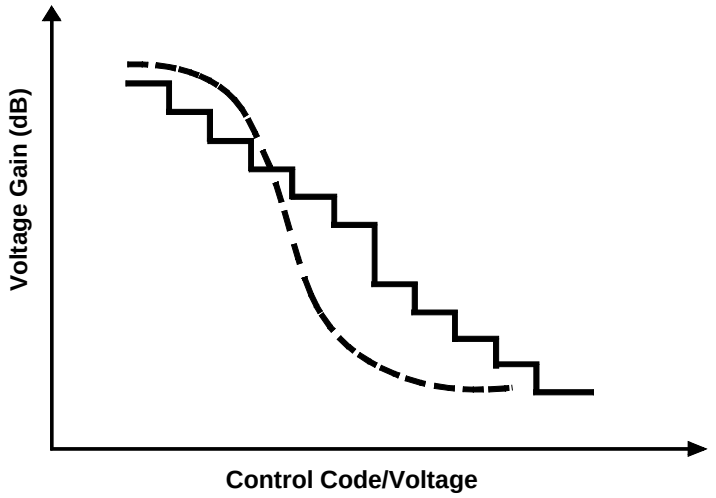

Figure 5.1. Gain of an RF front-end using digital (solid line) and analog (dashed line) gain control.

Both of these methods have benefits compared to the other scheme. Using analog adjustment, the RF front-end can achieve all gain values within a certain gain range, whereas digital control achieves certain gain values only. Hence, if the number of gain levels required increases, the

complexity of the digital control increases. Digital control can produce transients to the receiver output, which corrupt the reception. This important issue of RF gain control is addressed later in this chapter. The problem with analog control may be the nonlinear behavior of the voltage gain as a function of the control voltage or current, which is shown in Figure 5.1. The RF gain can be sensitive to the control voltage at certain ranges and less sensitive elsewhere. Thus, it becomes difficult to implement the tuning engine controlling the LNA gain. Using digital control, this is not a problem. However, as illustrated in Figure 5.1, the gain step with digital control may not be constant, which may lead to big gain changes that cannot be handled in the analog baseband or in A/D converters. In addition, if the gain control is divided between the RF front-end and baseband, the gain adjustment must be monotonic. For example, a 1dB gain increase is designed to be implemented by increasing the RF gain by 10dB and lowering the baseband by 9dB. If the gain change in the RF circuits is 8dB instead of 10dB as a result of errors in the gain steps, the gain is lowered by 1dB, which can lead to errors in the reception. If both the RF and baseband block use digital control, the error must be

$$G_{err} = G_{err,RF} + G_{err,BB} < G_{step,\min}\,, \tag{5. 1}$$

where $G_{step,min}$ is the minimum gain step and $G_{err,RF}$ and $G_{err,BB}$ are the errors of the gain steps in the RF front-end and baseband, respectively.

In the experimental circuits, the RF front-end and baseband use digital gain control for the reasons described above. In addition, simply by using the control codes calculated in the DSP, the gain of the receiver can be altered without D/A converters. When the DSP is used to calculate the receiver gain these D/A converters would be required to produce the control voltage or current, if analog tuning were used.

5.2 Gain control in inductively-degenerated LNA

The voltage gain of an inductively-degenerated LNA can be controlled in different manners. Gain control using an input stage adjustment, load adjustment, current steering, resistor chain, and separate signal paths is analyzed in this section.

5.2.1 Variable gain using input stage and load adjustment

Figure 5.2 illustrates the variable gain implementation in the load or input stage of an inductively-degenerated LNA. According to the equations of the inductively-degenerated LNA in Chapter 3, the voltage gain of the LNA depends on the load impedance and G_m of the input stage. Thus, if either of these parameters is adjustable, the LNA gain can be altered. In Equation (3.11), the G_m of an inductively-degenerated LNA is given. Since the G_m and the input matching of the LNA are related to each other, the adjustment of a single parameter affects both parameters. For a variable gain and constant input matching, both the g_m and the inductors, Le1 and Lb1, in Figure 5.2 must be adjusted. In practice, this leads to a too-complicated adjustment and increases the NF as a result of the switched adjustable inductors, as explained in Chapter 4.4.

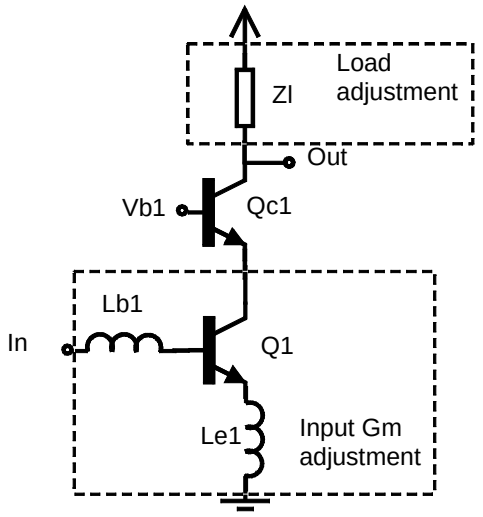

Figure 5.2. Gain adjustment by changing the load or input G_m of an inductively-degenerated LNA.

Gain adjustment by means of load tuning can be implemented in different ways and it depends on the type of load which is chosen for the LNA. The passive loads, which have been discussed earlier in this thesis, are the resistive load and the resonator load. Figure 5.3 shows an example of load adjustment using (a) a resistive load and (b) a resonator load. The resistive load impedance can be adjusted by connecting an additional resistor, R_{add}, in parallel with the nominal resistor, R_p, with the switch Mp1. The benefit of this arrangement is that both the additional and nominal resistor can be fabricated from the same material. Hence, when the process variations are taken into account, the LNA gain varies but the gain step is constant. The problem with this adjustment is the additional capacitance at the LNA output. When the number of gain steps increases, the parasitic capacitance resulting from the additional resistors and switches increases and limits the available operation frequencies, which also affects the gain step at high frequencies. In addition, the resistive load suffers from the problems described in Chapter 3.

The resonator load in Figure 5.3 (b) does not suffer from similar problems, since the additional capacitance can be taken into account when dimensioning the resonator. According to Equation (3.35), the impedance at the resonance frequency of the resonator shown in Figure 5.3 is

$$Z(f_r) = \frac{1}{\frac{1}{R_{add}} + \frac{R_L}{R_L^2 + \omega_r^2 L^2}}, \tag{5. 2}$$

where R_{add} includes the on-resistance of the switch. Thus, if the R_{add} is connected in parallel with the resonator, the gain decreases. This approach has two aspects which must be taken into account during the design phase. When the LNA has the maximum gain, the inductor and parallel resistor determine the impedance value. However, at the lower gain settings, the resistor has a larger effect on resonator impedance, compared to the inductor. When the process variations are taken into account, the gain step does not remain constant, since the inductor value and resistor value depend on different process parameters, which do not track each other. The other aspect is the gain step variation as a function of frequency, which is illustrated in Figure 5.4. It must be noted that the Equation (5.2) determines the gain step at the resonance

frequency. However, this step is not constant, as a result of the frequency dependence of the resonator impedance, which is given in Equation (3.33). Thus, if the resistor, R_{add}, is changed, the Q-value of the resonator changes. The maximum gain step is at the resonance frequency and the step value reduces towards zero as the operating frequency moves away from resonance. In practice it is possible to use this adjustment but the amount of the gain step error must be checked using a circuit simulator. Resistor load tuning was used in the experimental circuits and, for example, in [1].

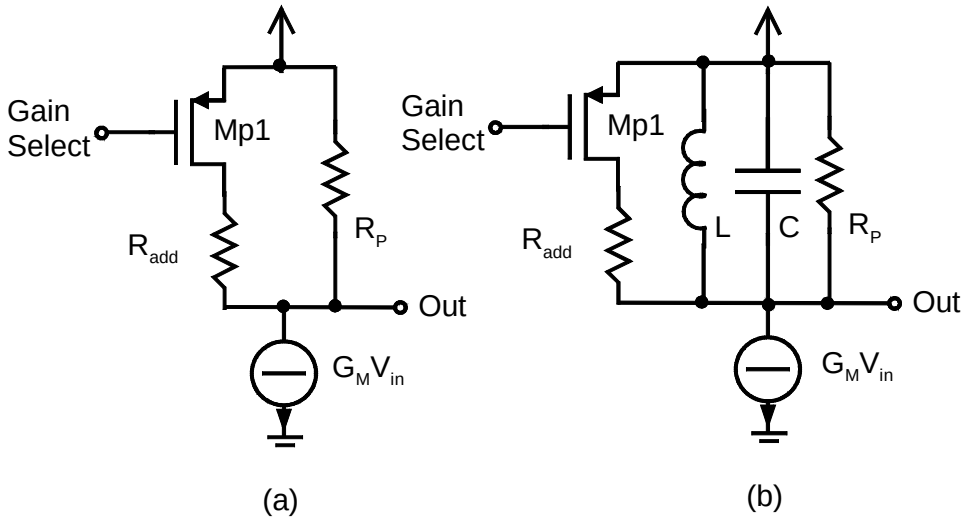

Figure 5.3. Gain adjustment of (a) a resistive-load LNA and (b) a resonator-load LNA.

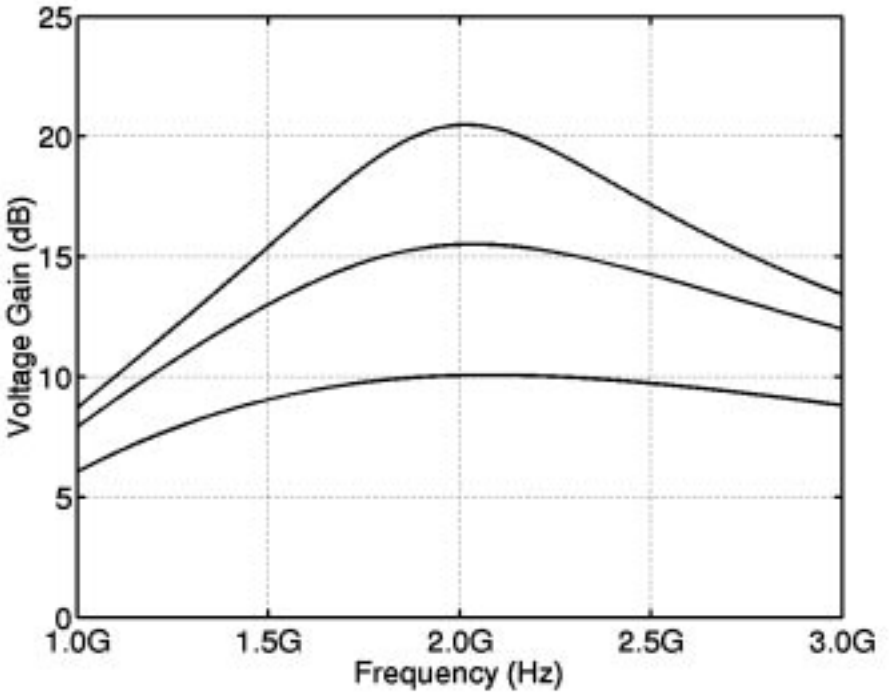

Figure 5.4. Example of the LNA voltage gain with different parallel resistor values.

5.2.2 Variable gain implemented using analog or digital current steering

Figure 5.5 shows an inductively-degenerated LNA which uses current steering for adjustable gain [2]. The transistor Qc1 is a regular cascode and the transistor Qc2 determines the amount of signal flowing to the load and supply, respectively. Figure 5.6 illustrates the voltage gain of the inductively-degenerated LNA as a function of the voltage difference (V_ctrl-Vb1). The voltage gain begins to decrease as V_ctrl approaches Vb1. A 6-dB gain step is observed when both voltages are equal and the gain drops as V_ctrl increases. The minimum achievable gain depends on the isolation to output from different signal nodes. In [3], a gain range of at least 60dB at 1.85GHz is achieved with this method. As can be seen from Figure 5.6, the dependence of the gain on the control voltage is not linear and the control voltage range is relatively small. Thus, the generation of an appropriate control voltage becomes difficult. For example, in [3] a 6bit D/A-converter controls the AGC loop in order to achieve a linear attenuation of 1.1dB for each step.

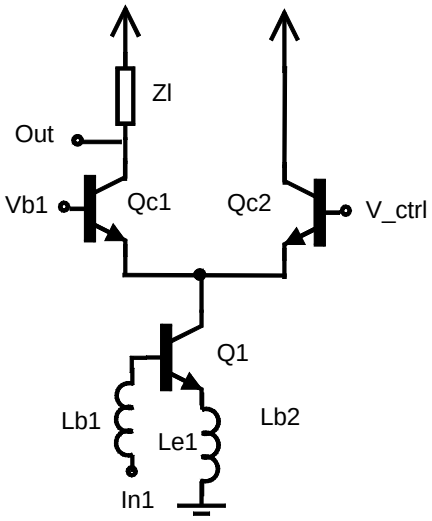

Figure 5.5. LNA using an analog current steering for variable gain.

The current steering can be designed to use digital information without D/A converters, as shown in Figure 5.7. The gain adjustment is performed using additional cascode-transistor pairs in parallel with the cascode transistor Qc1 [4]. One of the collectors in each pair is connected to the signal output and the other collector is connected to the positive supply. If the bases of the transistors Qc2 and Qc4 are connected to the same bias voltage as the base of the transistor Qc1, and the base voltage of Qc3 and Qc5 is equal to ground, the LNA has the maximum gain. If the base voltages of one pair are reversed, the voltage gain decreases as

$$\Delta G = \frac{A_{out}}{A_{out} + A_{VDD}}, \tag{5. 3}$$

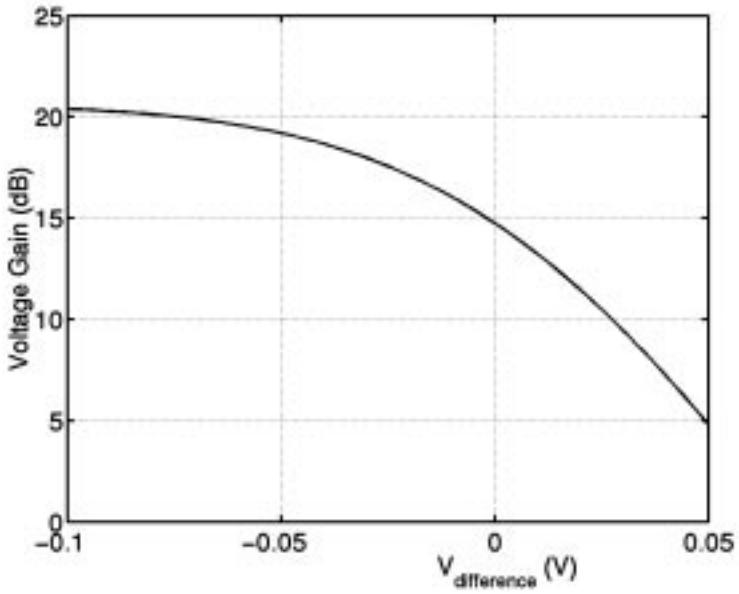

Figure 5.6. Voltage gain of an inductively-degenerated LNA as a function of the voltage difference between the cascode transistor base voltages.

where A_{out} is the number of cascode transistors conducting signals to the output and A_{VDD} is the number of cascode devices conducting signals to the positive supply voltage. Equation (5.3) assumes that all the cascode devices are similar and biased as described above. For example, if the base of the transistor Qc5 is connected to Vb1 and the base of the transistor Qc4 is at ground, the voltage gain of the LNA is reduced by 6dB. Figure 5.8 illustrates the voltage gain of the inductively-degenerated LNA shown in Figure 5.7. The models used in the experimental circuits were used in the simulations, and the gain adjustment was performed by reducing the number of cascode transistors conducting signals to the output to half. Thus, the LNA has two gain steps.

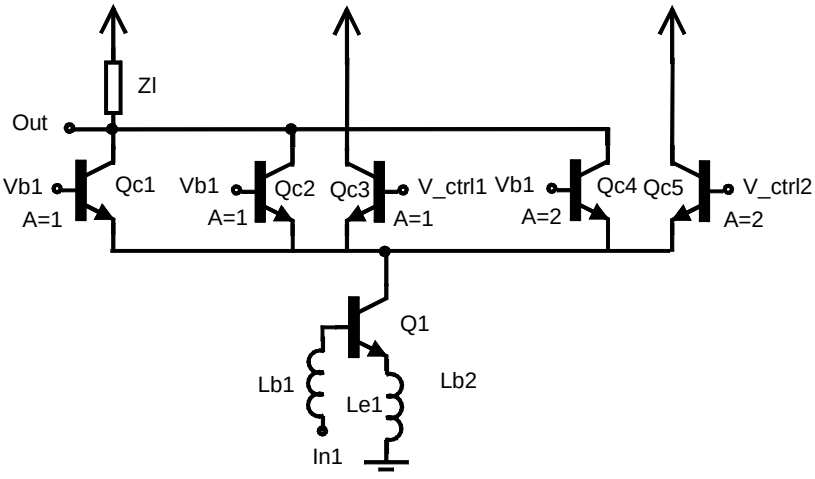

Figure 5.7. LNA using a digital current steering for variable gain.

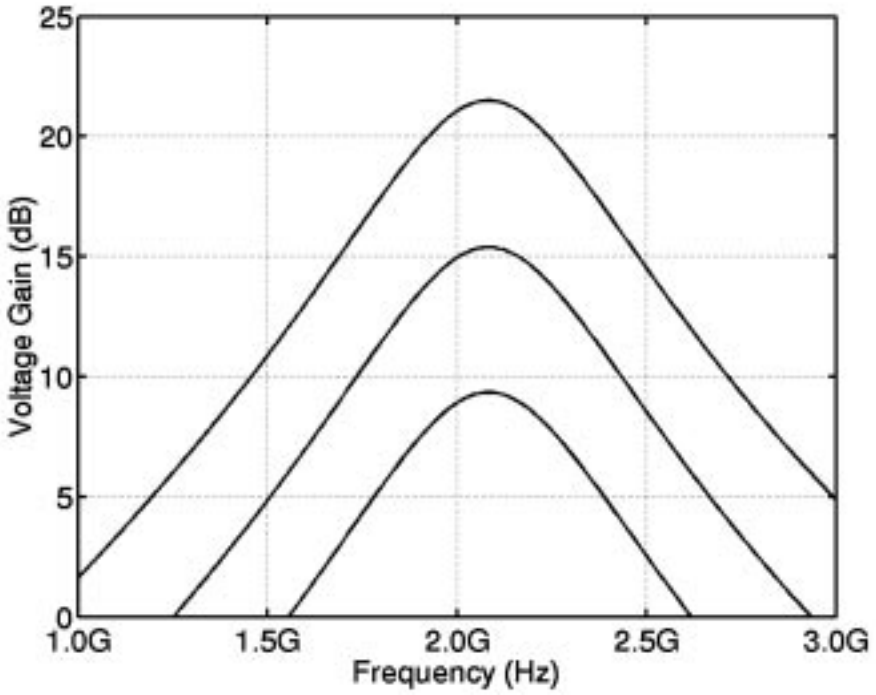

Figure 5.8. Voltage gain of an inductively-degenerated LNA using digitally-controlled current steering for gain adjustment.

Comparing analog and digital current steering, analog steering has less effect on LNA performance at maximum gain if an appropriate control voltage can be produced. In analog current steering there are a minimum number of additional devices connected to the emitter of the cascode transistor, which can degrade LNA performance. Figure 5.9 shows an example of the performance degradation of an inductively-degenerated LNA as the number of gain steps is added to the digital current steering. The LNA is simulated using similar models as in the experimental circuits and it achieves 20dB voltage gain and 1.45 dB NF at 2GHz. The NF degradation caused by the additional gain step is simulated by adding additional transistor pairs in parallel with the cascode transistor. The additional pairs are biased to conduct signals to the LNA output. Thus, it can be observed that the NF at maximum gain degrades as the number of gain steps is increased, as explained in Chapter 3.2. In practice, the usability and number of gain steps using digital current steering must be checked using a circuit simulator.

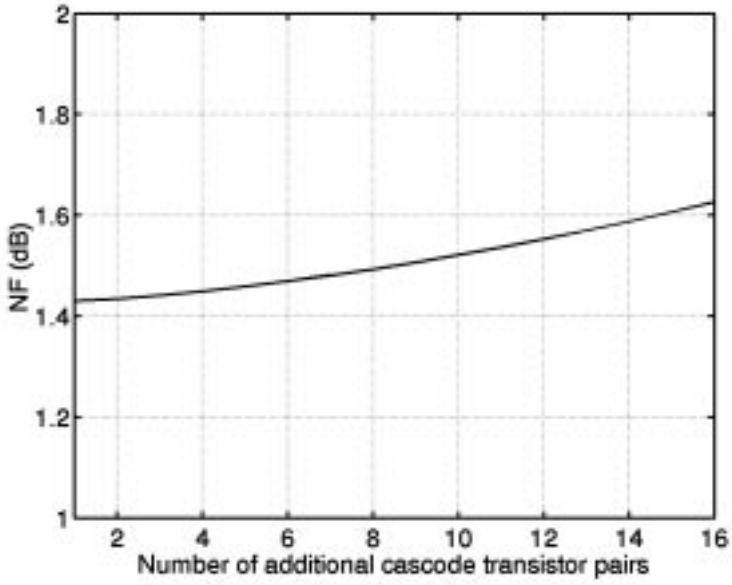

Figure 5.9. NF degradation of an inductively-degenerated LNA at 2GHz caused by additional cascode transistor pairs.

5.2.3 Variable gain using resistor chain

A different type of gain control, which is based both on digital current steering and load tuning, is shown in Figure 5.10. The gain control is based on the ratio of the resistor values in the resistor string (R1-R3)[5]. At maximum gain, the cascode transistor Qc1 steers the signal to the load, which is a damped parallel resonator. The LNA gain is lowered by biasing the transistor Qc1 off and having one of the transistors Qc2 or Qc3 on. The gain reduction depends on the ratio between R1, R2, and R3. For example, if the transistor Qc2 is biased on and the resistor R1:R2:R3 ratios are 2:1:1, the voltage gain is reduced by 6dB compared to maximum gain. The benefit of this gain control is that the gain reduction depends on the ratios between the resistors. Thus, the process variations do not alter the gain step. However, this configuration suffers from a few drawbacks. The gain control is sensitive to parasitic capacitances in the resistor chain [5]. In addition, when the gain is lowered, the DC current must go through the resistors in the chain, which decreases the DC voltage in the collectors of Qc2 and Qc3. Therefore, the resistor values have a maximum usable value for the proper operation of the transistors Qc2 and Qc3. The minimum value of the resistor is limited by the maximum gain setting, since too-low resistor values decrease the maximum LNA gain [6].

5.2.4 Variable gain using separate signal paths

LNA gain can be adjusted by using separate signal paths at different gain settings. Figure 5.11 (a) illustrates an inductively-degenerated cascode LNA in which an alternative signal path can be used for different gain settings. For a signal which is close to the sensitivity level the inductively-degenerated LNA is biased on as the other stage is off. When the signal level at the receiver input increases above a certain threshold level, the alternative stage is biased on and the

inductively-degenerated stage is turned off. Figure 5.11 (b) shows an example of the alternative stage. A similar structure is used in the experimental circuits and in [5]. For proper performance the additional signal path must have a high input impedance when the inductively-degenerated LNA is used. When the additional signal path is used, the input matching must meet the same performance requirement as in the maximum gain mode. Otherwise, the performance of the pre-select filter may be degraded and thus the reception is corrupted. The input impedance of the LNA which has the alternative signal path biased on and the inductively-degenerated LNA off is

$$Z_{in} = j\omega Lb1 + Z2 \left\| \left(\frac{1}{j\omega C_{\pi}} + j\omega Le1 \right) \right. , \tag{5. 4}$$

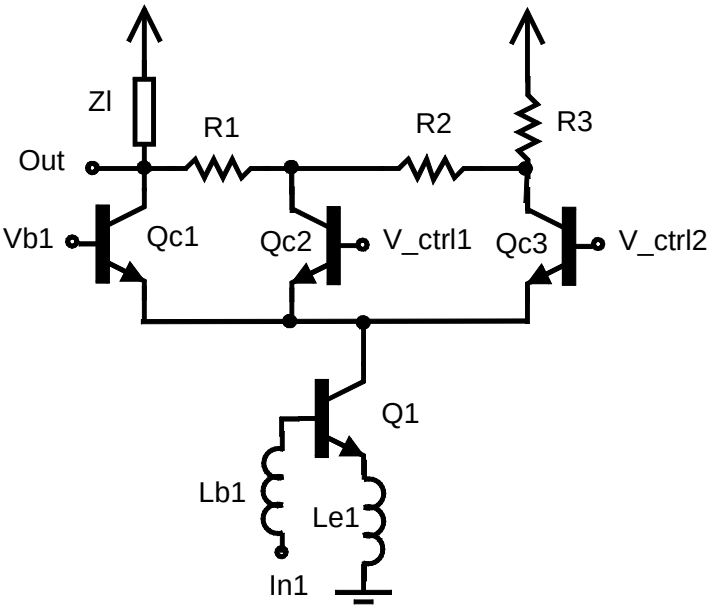

Figure 5.10. LNA using a resistor chain for variable gain [5].

where C_{π} is the base-emitter capacitance of the transistor Q1 and Z2 is the input impedance of the additional stage. If the additional stage uses a similar configuration as in Figure 5.11 (b), the input impedance of this stage can be estimated as

$$Z2 = R2 + \frac{1}{g_{m2}} + \frac{1}{j\omega C2} = R_{in2} + \frac{1}{j\omega C2} , \tag{5. 5}$$

where g_{m2} is the transconductance of Q2 and R_{in2} is the sum of the resistor, R2, and transconductor, g_{m2}. In most cases, the base inductor dominates the inductive part of the matching in inductively-degenerated LNAs. Therefore it can be assumed that

$$\frac{1}{j\omega C_{\pi}} + j\omega Le1 \approx \frac{1}{j\omega C_{\pi}} . \tag{5. 6}$$

Thus, the input matching in Equation (5.4) reduces to

$$Z_{in} = j\omega Lb1 + Z2 \left\| \frac{1}{j\omega C_{\pi}} \right. . \tag{5. 7}$$

In addition, if the capacitor C2 is designed to be much larger than C_{π}, the input matching can be estimated as

$$Z_{in} \approx j\omega Lb1 + \frac{R_{in2}^2 \omega C_{\pi} + 1/\omega C2}{j\left(R_{in2}^2 \omega^2 C_{\pi}^2 + 1\right)} + \frac{R_{in2} - R_{in2} \dfrac{C_{\pi}}{C2}}{R_{in2}^2 \omega^2 C_{\pi}^2 + 1} . \tag{5. 8}$$

From Equation (5.8) it can be observed that appropriate matching can be achieved compared to the case when the inductively-degenerated LNA is biased on.

The implementation of the multi-stage gain control using separate signal paths is difficult, since a change in g_{m2} or R2 also changes the input matching. In addition, the use of multiple parallel stages increases the parasitic components at the LNA input, which always degrades the performance of the inductively-degenerated LNA. The number of gain steps can be increased by connecting the alternative signal path between the base and collector of the transistor Q1 and using digital current steering in the cascode transistor. Another example of an alternative signal path can be found, for example, in [7] and [8], where the bipolar transistor Q2 and resistor R2 in Figure 5.11 (b) are replaced with a MOS switch.

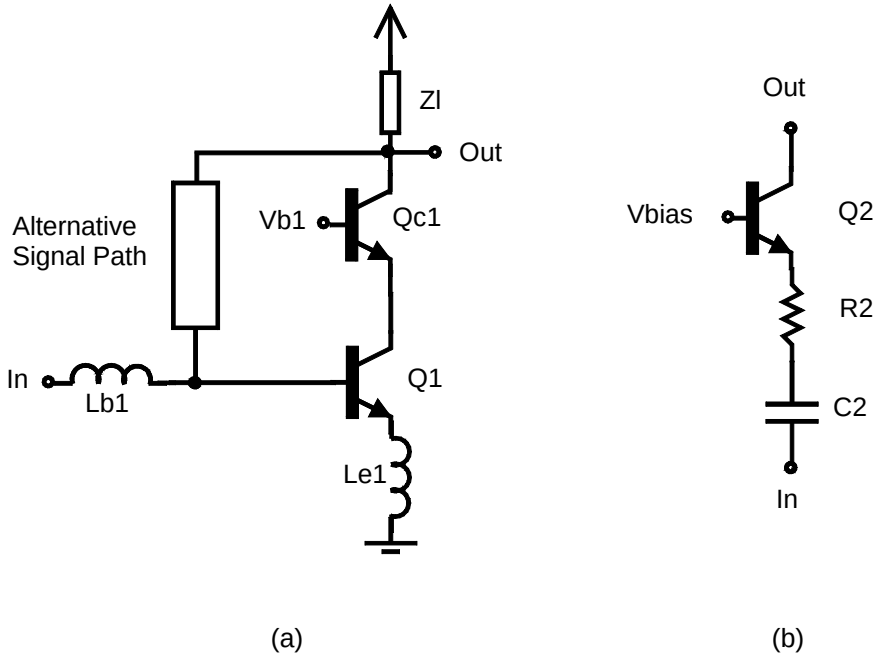

Figure 5.11.(a) LNA with an alternative signal path for low-gain mode. (b) An example of the schematic of the alternative path.

5.2.5 Comparison of gain control methods of inductively-degenerated LNA

Table 5.1 shows a comparison between the different methods described in this section. The gain range, step accuracy, and control implementation describe how easily it is achieved. The effect on LNA performance describes how the performance of the inductively-degenerated LNA without gain control is decreased. The plus (+) sign indicates that LNA performance is only slightly degraded compared to an LNA without gain control. As can be observed, it is possible to use all control methods except G_m tuning in inductively-degenerated LNAs.

In general, all of these methods increase the IIP3 of the receiver. This is because, as the LNA gain decreases, the stages following the LNA have less effect on the total IIP3 of the receiver, as described in Chapter 2.5.2. In DCRs the IIP3 of the receiver is usually limited by the mixers, and therefore the LNA gain control has a significant effect on the receiver IIP3. The effect of the gain control on the IIP3 of the LNA depends on the implementation of the gain control. If the gain control affects the LNA input stage the IIP3 of the LNA is changed. Thus, the IIP3 remains constant in all the methods presented except in G_m tuning and in the alternative signal path. The IIP3 of the LNA using G_m tuning or an alternative signal path is increased by increasing the degeneration of the input stage. However, since the value of the gain step and the input matching determine the values for these components, the IIP3 of the LNA cannot be significantly changed. In addition, by adding the programmable gain to the LNA the need for the programmable gain is reduced in the stages following the LNA, i.e. in the baseband.

The choice of the correct method depends on the design approach. For example, does the analog baseband have tunable gain and how is it implemented? How much can the LNA performance be degraded by variable gain? All gain control methods can be implemented on with multi-mode LNAs described in the previous chapter. The possibilities of using these methods are shown in the following chapter, which describes the experimental circuits.

Table 5.1 Comparison of implementation methods for variable gain in inductively-degenerated LNAs

	Gain range	Step accuracy	Control implementation	Effect on LNA performance
G_m tuning	-	-	-	-
R tuning	+/-	+	+	+/-
RLC tuning	+/-	+/-	+	+
Digital current steering	+	+	+	+/-
Analog current steering	+	+	-	+
Resistor chain	+	+/-	+	+/-
Alternative signal path	+/-	+/-	+/-	+/-

5.3 Transients in DCRs caused by programmable gain in RF front-end

The gain has to change during reception in continuously-receiving systems, such as direct-sequence CDMA. Hence, in order for reception to be achieved with an acceptable bit-error rate, the gain adjustment has to be carried out without significant transients in the baseband signal, which, typically, will be strongly amplified in the analog baseband before A/D conversion.

The benefit from the gain adjustment in the RF front-end is that the tuning transients from the RF circuitry do not fall into baseband frequencies. The low frequency transients are upconverted in the mixers to RF frequencies and then filtered out by the baseband channel-select filter. However, if the gain adjustment circuit is at RF but DC-coupled to the mixer output, the RF gain control may abruptly change the DC offset at the mixer output, thus producing transients in the baseband. This can occur, for example, when the gain adjustment is implemented at the input transistors of a Gilbert cell-type mixer.

In Chapter 2 the problems caused by LO selfmixing in DCRs were discussed. However, a new problem arises from the RF gain adjustment in a DCR resulting from LO leakage, which is shown in Figure 5.12. The local oscillator (LO) operates at the reception frequency. In DCR, a part of the LO signal power leaks to the RF input. This signal is then fed back to the mixer input and downconverted with the same LO signal, producing a DC offset at the mixer output. When the gain of the RF front-end is fixed, the DC-offset from the LO selfmixing remains constant as long as the LO leakage in the receiver remains constant. This constant DC offset can be filtered out with various techniques. The options that can be used to remove the offset depend on the system specifications. In some cases, highpass filtering is suitable; this can be implemented using, for example, AC coupling or a DC feedback loop, i.e. a servo [4].

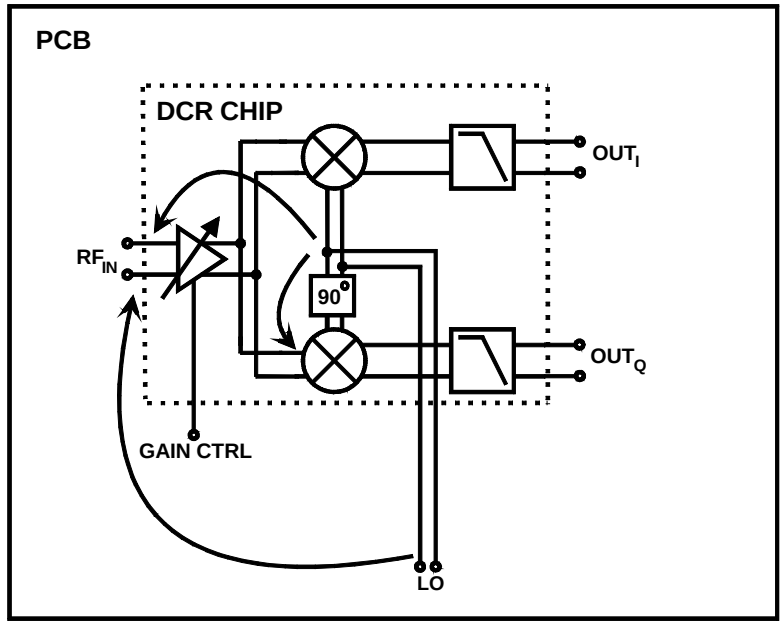

Figure 5.12. Coupling paths of the LO signal, which can produce DC offset because of selfmixing.

A new problem arises when the RF gain is changed abruptly with digitally-controlled steps. After the change in the gain, the leaked LO signal passes through the LNA to the mixer input

with a different gain. In association with the gain change, the selfmixed DC offset at the mixer output is changed as well. This is usually a rapid change, thus producing a transient to the mixer output. These transients can be much higher than the desired signal and hence they must be removed. The selfmixed LO power at the mixer output, which is due to LO leakage to the RF input, can be estimated as

$$P_{1,2} = P_{LO} - L_{LOtoRF,1,2} + G_{RF,1,2} \tag{5. 9}$$

where P_{LO} is the local oscillator power (dBm), $L_{LOtoRF,1,2}$ are the LO attenuations to the RF port (dB), and $G_{RF,1,2}$ are the front-end gains from the RF input to the mixer output with different gain settings (dB). When the gain is changed in the LNA, the value of the DC offset change can be calculated as

$$V_{offset,rms} = \sqrt{0.05 \cdot 10^{\frac{P_1}{10}}} \mp \sqrt{0.05 \cdot 10^{\frac{P_2}{10}}}. \tag{5. 10}$$

Here P_1 and P_2 are the powers in the 50 Ω environment with different RF front-end gains at the output of the mixer as a result of the LO selfmixing. These equations give a worst-case DC offset change, if it is assumed that the DC offset is mainly dominated by the LNA gain change. The minus (-) sign is applied when LO selfmixing happens in-phase and the gain change does not change the signal phase at the mixer input. The plus (+) sign is used when the selfmixing happens in-phase and the signal phase changes by 180° when the gain is changed. For example, the minus sign can be applied when the LNA uses current steering for gain control, since it does not affect the signal phase. However, LO leakage to the mixer input may change with different LNA gain settings and thus produce an additional DC offset change. Therefore, these equations only estimate the DC offset change.

In the published DCRs, the typical LO power at the RF input is between –100dBm and –60dBm [4], [9], [10], [11]. Figure 5.13 illustrates the calculated DC offset change as a function of LO-power leakage to the LNA input, as the RF front-end gain is lowered by 3 dB and the signal phase to the mixer input is not changed between different gain settings. This change is shown with four different RF front-end gain values. It can be seen that the offset change is easily in the range of several mV. If the gain steps are larger at the RF front-end then a larger offset change is obviously observed. Figure 5.14 shows measured and calculated DC offset changes at the mixer output for the direct conversion receiver presented in Chapter 6.2. The calculated result was obtained with the following procedure. First, the gain of the RF front-end was measured with different LO powers and gain settings. Then the LO power at the RF input was measured and the offset change was calculated using Equation (5.10). The plus sign in Equation (5.10) was applied because the gain alternation changes the signal phase at the mixer input. In order to minimize the number of bits required in the A/D converter and the power consumption of this receiver, baseband circuitry with a maximum voltage gain of 66 dB follows the RF front-end. A change in the offset of a few millivolts after the downconversion with that baseband gain is enough to produce an offset change of a few volts at the input of an A/D converter, which corrupts reception.

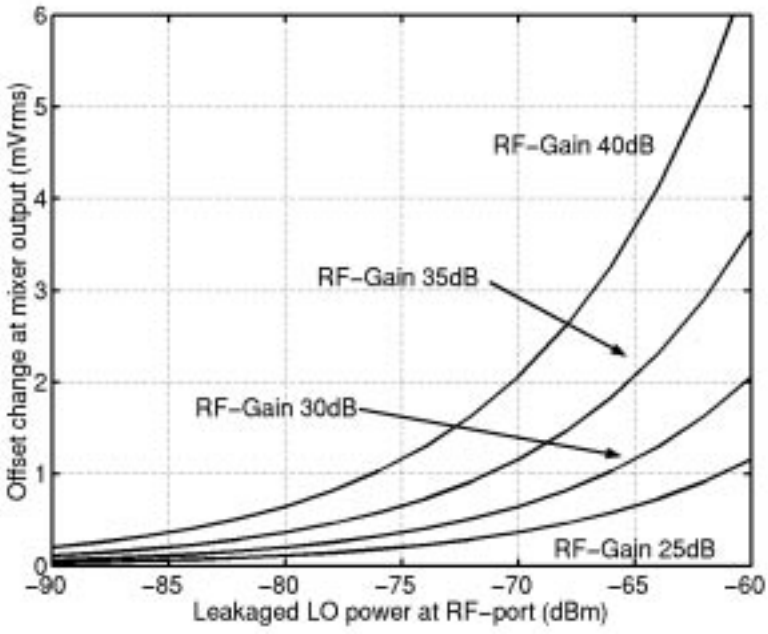

Figure 5.13. Calculated DC offset change at the mixer output as a function of the LO power leakage to the LNA input, when the RF front-end gain is lowered by 3 dB. The signal phase is assumed to be constant between different gain settings.

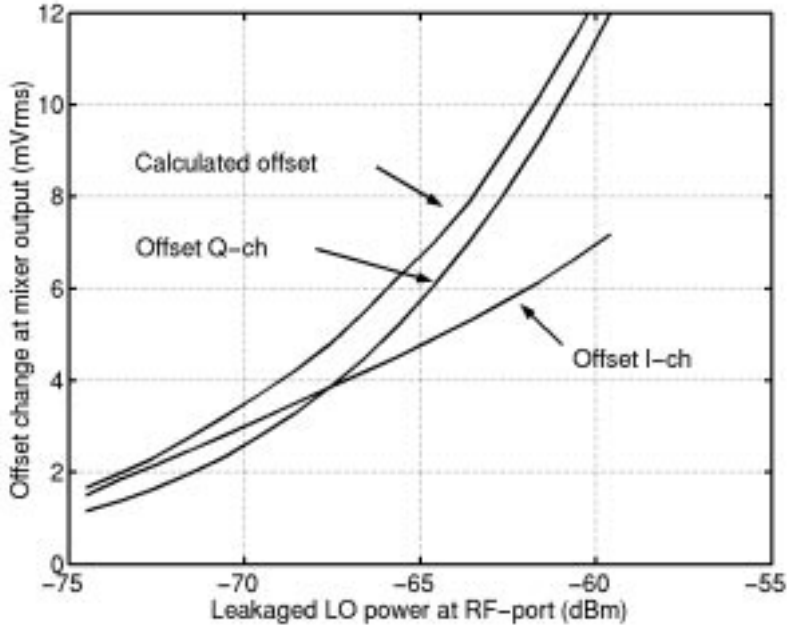

Figure 5.14. Measured and calculated DC offset change when the RF voltage gain is changed by 20dB. Calculated values assume a 180° signal phase change between the different gain settings.

The problem arising from the RF gain-control transients can be solved using two different approaches. In the first approach, a DC offset change of a few mV is accepted at the mixer output. In this case, to minimize the effect of the DC offset change, the RF gain is adjusted when the power of the desired signal is much higher than the DC offset change. Thus, if the RF gain control produces unacceptable large transients when the signal is close to the sensitivity level, the gain adjustment for small signal levels must be implemented in the baseband circuits. In this case, the variable gain in the baseband is not allowed to produce transients, which could cause the signal quality to deteriorate. In the second solution, the DC offset change at the mixer output is decreased to a level at which it is always much smaller than the actual signal. This requires strong LO signal suppression at the LNA input and is discussed below.

A lot of the LO power may leak to the RF input through the PCB and bond wires. Therefore, special attention must be paid to the design of the PCB. For example, the use of orthogonal LO and RF signal wiring, both on-chip and PCB, reduce the LO power leakage. Furthermore, using on-chip LO driver amplifiers, or placing VCO on the same chip, minimizes the LO power off-chip. Hence, only locally on-chip generated LO can couple to the RF input. As an additional solution, the off-chip LO power at the RF frequency can be minimized using a double-frequency LO. This solution obviously requires an on-chip divide-by-two circuit. However, the divide-by-two circuit can be used to produce a 90° phase shift between the I and Q mixers, instead of using RC or polyphase-type passive structures. The limiting factor for a divide-by-two circuit is usually the frequency band used. In current technologies, with a reasonable current consumption, a 5-GHz input frequency is easily achieved. This is enough to cover most current wireless telecommunication systems. Therefore, the divider shown in Figure 5.15, was implemented in the next receiver designed. In addition, compared to the previous mixer, which is presented in detail in Chapter 6.2, the mixer shown in Figure 5.16 was used to further reduce the LO leakage. The reverse isolation of the mixer in Figure 5.16 is improved by 11 dB, according to simulations, because of the cascode transistor between the LO switches and the input transistor. In the measurements, the LO power at the RF input was decreased from –68 dBm to –75 dBm, compared to the previous design. Figure 5.17 and Figure 5.18 illustrate the transients of this circuit when the LNA gain is changed by 5 dB and 10 dB, respectively. According to Equation (5.10), 55 mV and 152 mV transients should be observed at the baseband output when the LNA gain is changed in 5 dB and 10 dB steps, respectively. The minus (-) sign was applied in this case, since the LNA uses current steering for variable gain. The measured and calculated values match well for the 5 dB step but with the 10 dB step a larger difference is observed between the calculated and measured values. As previously explained, these types of changes are expected, because Equation (5.10) gives a worst-case estimation with the limitations previously explained. The baseband used similar high pass filtering as in [12]. The effect of the highpass filters at the baseband can be clearly observed in these figures.

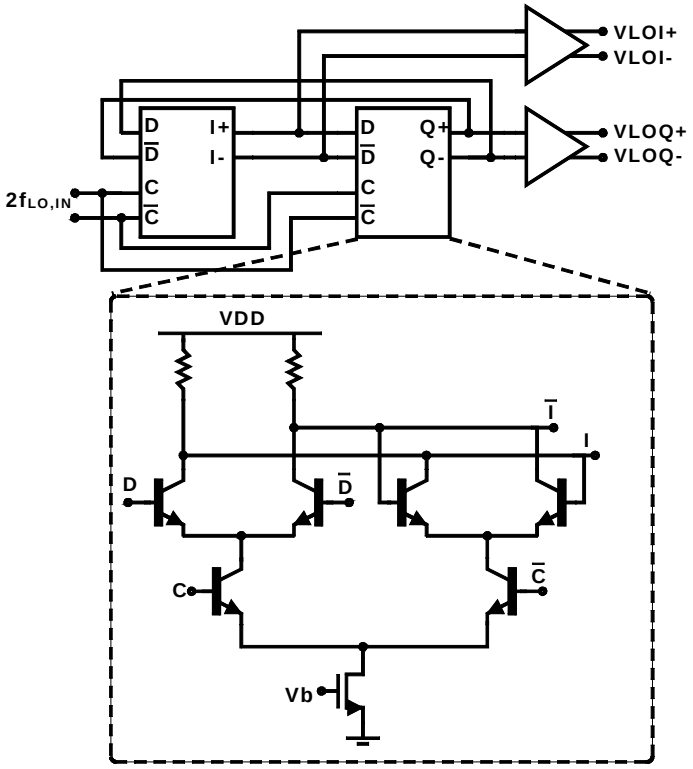

Figure 5.15. Schematic of the LO divider.

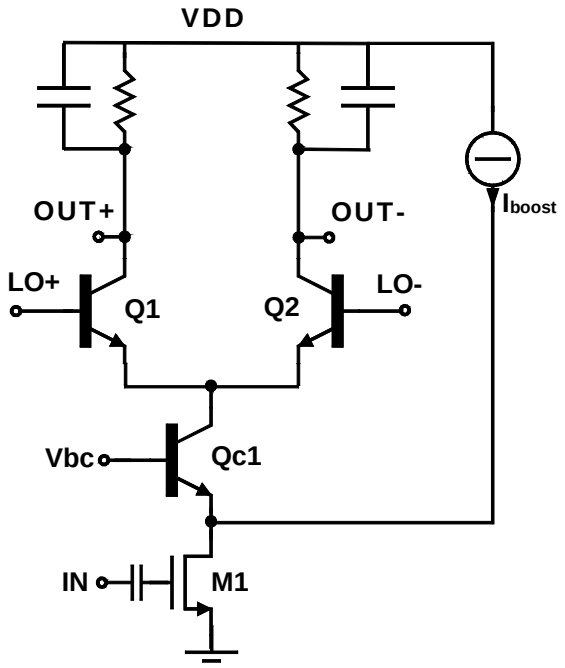

Figure 5.16. Schematic of the mixer used.

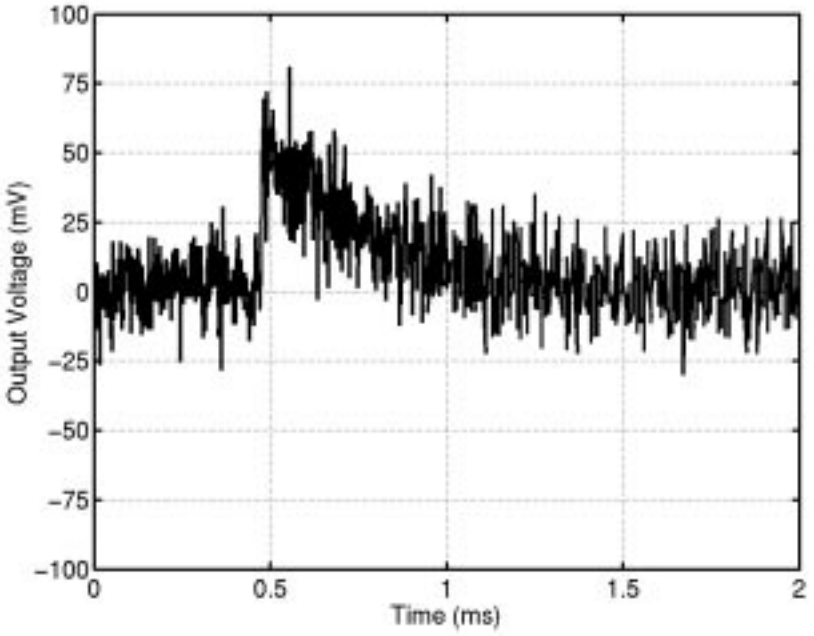

Figure 5.17. Transient at the baseband output when the LNA gain is increased by 5 dB.

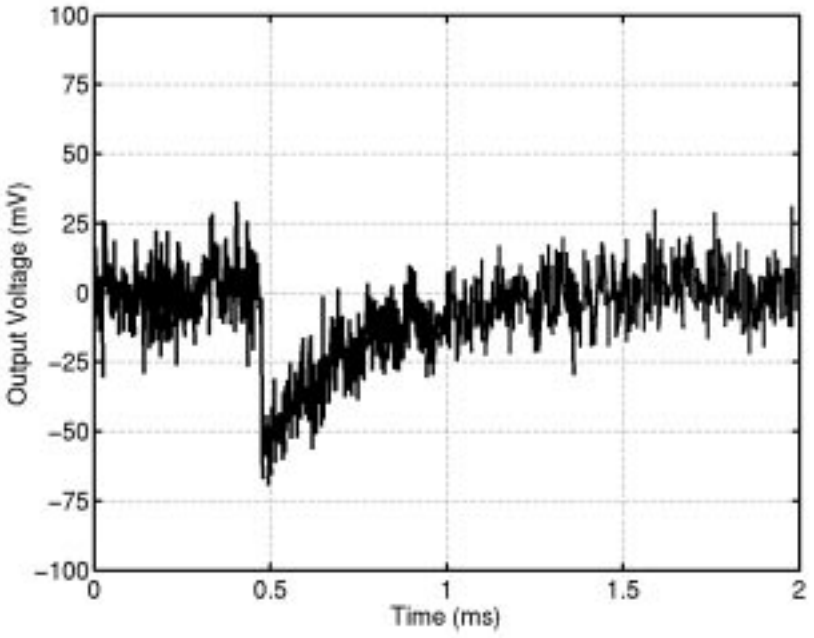

Figure 5.18. Transient at the baseband output when LNA gain is decreased by 10 dB.

To further decrease LO leakage, modifications were made in the implementation of the next receiver. This receiver is described in detail in Chapter 6.4. In this chip, the modifications were mainly made to the layout. The limiting LO buffers, which are located between the divider and

mixers, were previously located close to the divider. These were now moved to between the I and Q mixers and very close to the LO switches. The motivation for this was to minimize the LO signal routing path length at the same frequency as RF and also to reduce the length of the high-power LO signal. Furthermore, a part of the on-chip supply capacitor was placed close to the divider. In the measurements, the LO power at the RF input was below –98 dBm. With this low LO power it becomes difficult to distinguish transients from the noise at the baseband output, which is associated with the DC offset change described above. However, transients could be observed at the baseband output when the noise was removed from the results by averaging the output signal, which is shown in Figure 5.19. The average value is obtained by calculating a mean of 50 points from the original data. The baseband voltage gain of this receiver is 64 dB.

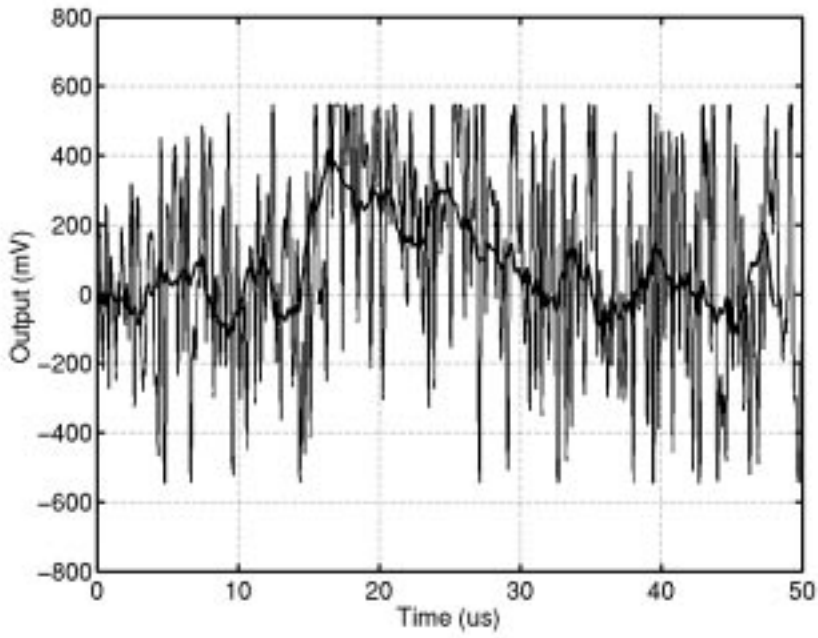

Figure 5.19. The transient at baseband output when LNA gain is decreased by 12 dB. The thick line is the averaged signal from the original narrow signal.

5.4 References

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6 Experimental circuits

This chapter describes two RF front-ends and two DCRs, which were designed and measured for this thesis. The description of all the chips includes details of the whole receiver. The details are included because the author was involved in the partitioning of the whole receiver. In addition, most of the measurement results are from the whole RF front-end or receiver. Without the description of the whole design the results are incomplete. Furthermore, the main focus was on the operation of the whole receiver. Thus, the test outputs were used only when the receiver performance did not suffer because of these outputs. The placement and design of the test outputs is not optimal for individual blocks. Detailed issues concerning the baseband and A/D converters are left out since they do not fall either within the scope of this thesis or the field of expertise of the author. The author's contribution to these circuits is explained in detail in Chapter 1. In general, the author was responsible for the design of the LNA and LNA-mixer interfaces and receiver partitioning, and for performing the measurements of the circuitry.

The first two implementations are intended for single-system applications and the other two for multi-mode applications. The RF front-end which is described in Section 6.1 is designed for a WCDMA direct-conversion receiver. This circuit is included in the thesis since it was part of the first published WCDMA receiver and it includes a different way to implement the emitter inductor compared to the other experimental circuits in this thesis. In addition, it was the starting-point for the other publications. This circuit is published in references [1], [2], and [3]. In addition, practically the same circuitry is included in [4]; only slight modifications were made to the LNA load resonator. The DCR in Section 6.2 is intended for the same system as the previous RF front-end. It includes an RF front-end and baseband filters with programmable gain. The goal in this receiver is to meet the specifications when a disturbing A/D converter is implemented on the same chip as the sensitive RF blocks. In addition, this chip has programmable gain implemented in the LNA. The circuit is published in [5] and [6]. The LNAs in both chips use circuit structures which are described and analyzed in Chapters 2 and 3. In addition, the gain control circuitry used in the DCR is described in Chapter 5.

The RF front-end in Section 6.3 is targeted for WCDMA and GSM900 applications. The supply voltage of the RF front-end is 1.8V, which is the lowest of those found in the experimental circuits in this chapter. In addition, the LNA uses a different type of programmable gain from the other LNAs in this chapter. In addition, the RF front-end includes a single-ended-to-differential converter, which is based on a circuit described in Chapter 3, to combine the two single-ended LNA outputs to a double-balanced mixer. This RF front-end is published in [7] and [8]. The multi-mode DCR in Section 6.4 is designed for GSM900, DCS1800, PCS1900, and WCDMA systems. The LNA in this chip uses only four on-chip inductors and has a different type of programmable gain compared to the other circuits. The LNA drives the single-ended input of the mixers directly. This type of interface was developed for this receiver in order to make possible the combination of two LNA outputs to a single mixer, and it was introduced in Section 4.3. This receiver is published in [9]. The circuit solutions in these multi-mode chips are mainly based on the issues analyzed in Chapters 4. In addition, the gain control in both chips is based on circuits described in Chapter 5. However, both gain control methods exploit the additional multi-mode circuitry.

The results for gain control transients, analyzed in Section 5.3, are measured from the receivers which are introduced in Sections 6.2 and 6.4. The transients are decreased in the multi-mode receiver, in Section 6.4, to a level where it becomes difficult to observe these without averaging the output signal.

6.1 RF front-end for direct-conversion WCDMA receiver

A direct-conversion RF front-end receiver chip which can be used in third generation mobile communications is described in this section. The RF front-end has a 27.5-dB voltage gain, 4-dB NF(DSB), -9-dBm IIP3, and +43-dBm IIP2. It draws 41 mA from a 2.7-V supply. The RF chip that was designed to operate as part of a WCDMA receiver which includes an analog baseband and A/D converter chips [1]. The block diagram of the RF front-end is shown in Figure 6.1. The RF chip consists of an LNA, quadrature mixers, and a 90° LO phase shift network, and uses a 25-GHz f_t BiCMOS process with a 0.35-µm MOS minimum gate length. External components were used only for input matching.

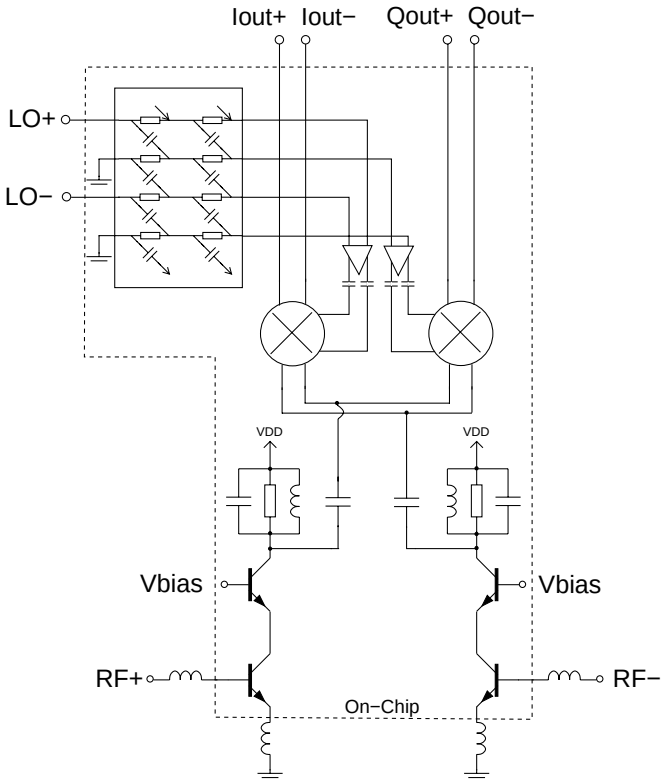

Figure 6.1. Schematics of the RF front-end.

6.1.1 LNA design

A fully-differential inductively-degenerated cascode LNA is used. Differential structures are used because of their immunity to common-mode distortion through the substrate. In addition, the mixer is designed for a balanced input signal. The load for the LNA is a damped resonator. This resonator uses parallel resistors giving a 500-MHz bandwidth, which allows the receiver to operate both in mobile terminals and base stations. The resistor value trades off between the gain, bandwidth, noise figure, and sensitivity to component values. The LNA, with a 20-dB voltage gain, drives the capacitive input of the quadrature mixers directly.

The input matching inductors were realized by using bond wires. Because of the small value of the emitter inductors (0.6 nH), they were realized using three bond wires, as shown in Figure 6.2. An additional bond wire was added between the two emitters. The advantages are larger inductor values, which can be realized more easily, and a better virtual ground in the middle of the pad-to-pad bonding. The input matching in Figure 6.3 shows that the measured and simulated values are close to each other. The problem in this implementation is the shared emitter bonding pads, which are used both by the common-mode inductor, Lcm, and the ground inductors, Le1 or Le2. For a greater reliability, parallel bonding pads should be used for Lcm. In addition, alternative ways to implement the emitter inductor were considered. In Figure 6.4 (a), the emitter inductor is realized using a single bonding wire from the emitter to the ground, and in Figure 6.4 (b), the emitter inductor is realized using on-chip bonding from the emitter to the chip ground. The configuration in Figure 6.4 (a) was excluded because of its low inductor value, which would have led to a short bonding wire. In practice, it would have been too difficult to implement the wire. The configuration in Figure 6.4 (b) was excluded because it would have required two on-chip bonding wires. In addition, it would require accurate modeling of the inductance between the ground and chip-ground. This was considered too complicated because the number and location of the ground bonding pads were not fully known before the final layout.

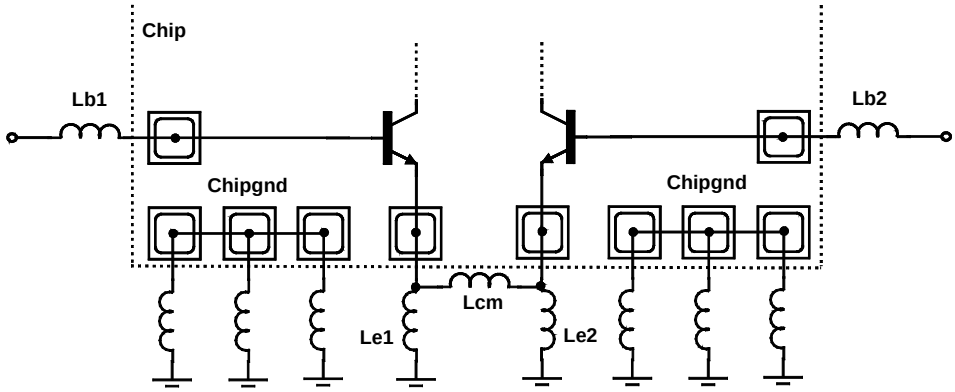

Figure 6.2. The input-matching network.

6.1.2 Mixer design

The double-balanced modified Gilbert cell mixer in Figure 6.5 optimizes the RF front-end gain and dynamic range requirements. The NMOS transistors are applied to the RF input because of their higher linearity, and the npn transistors in the LO switches are required because of their lower 1/f noise. The flicker noise in the RF input is upconverted. The mixer drives the baseband circuit, which has a variable input impedance as a result of the gain control. The buffers needed to drive the baseband use 35% of the total RF front-end supply current. The DC level at the mixer output is adjusted by a common-mode feedback (CMFB). The CMFB loop in Figure 6.6 is a two-stage amplifier which compares the reference voltage to the mixer output voltage and adjusts the DC current through the load resistors.

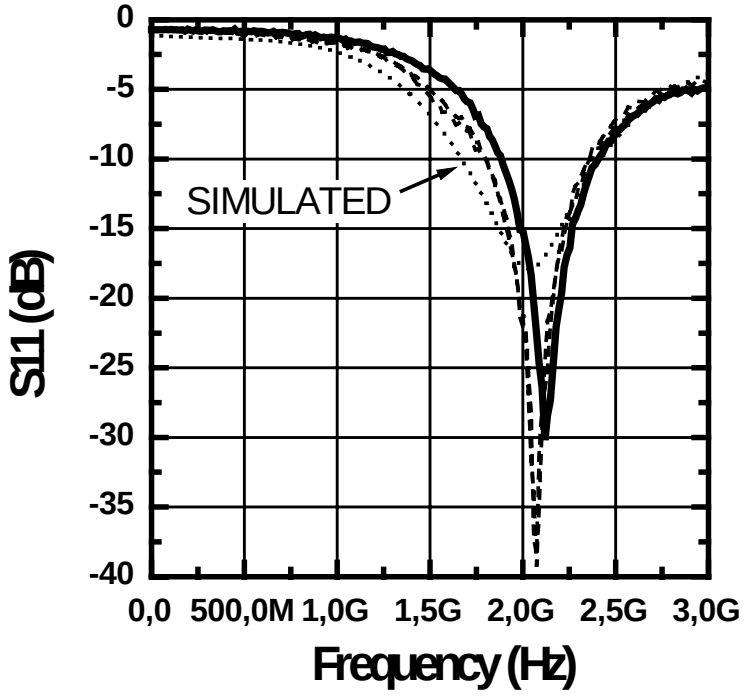

Figure 6.3. Simulated and measured S11. The dashed lines are single-ended s-parameters for the input.

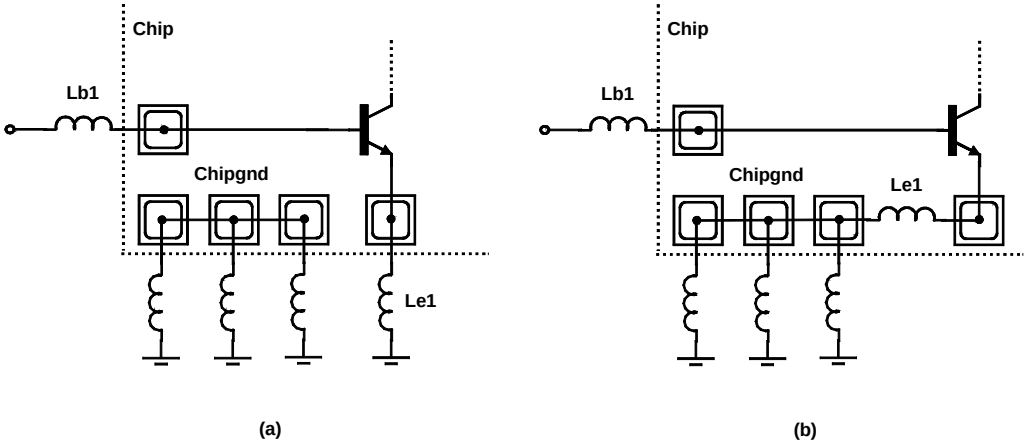

Figure 6.4. Alternative ways to implement the emitter inductor using a bonding wire: (a) uses a single bonding wire from the emitter of the input transistor to the ground: (b) uses on-chip bonding from the emitter of the input transistor to the chip-ground.

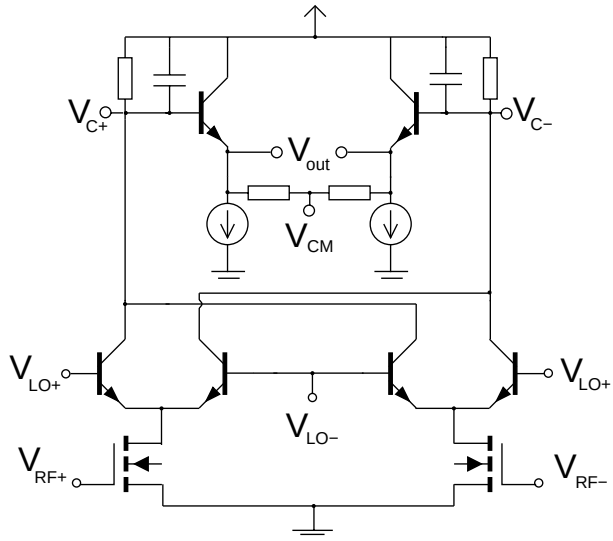

Figure 6.5. Mixer schematics including the output buffer.

A two-stage polyphase filter generates the quadrature LO signals. An accurate phase shift can be performed with a polyphase filter, but in theory it suffers from a 3-dB loss per stage. This loss was compensated by using a differential amplifier in front of the mixer. The LO and RF lines were drawn orthogonally in order to minimize the LO-to-RF leakage [10].

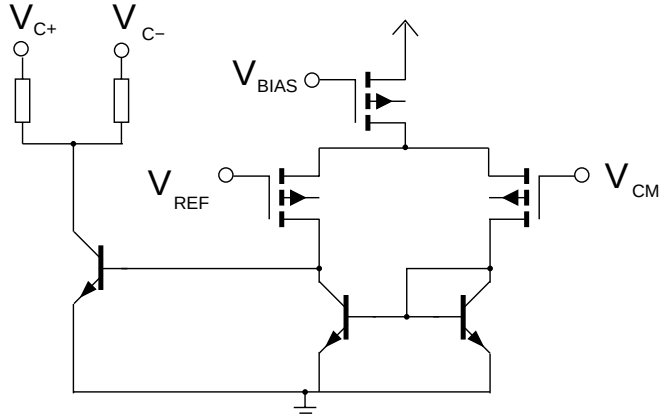

Figure 6.6. Schematics of the two-stage amplifier in CMFB.

In differential circuits, mismatches between the transistors and asymmetry in the layout damage immunity to second-order effects in balanced circuits. Therefore, ultimate symmetry in the layout design is obeyed.

6.1.3 Measurements

The performance of the RF front-end is summarized in Table 6.1. Separate LNA or mixer measurements cannot be made for this circuit because no additional measurement buffers, which could have degraded RF front-end performance, were implemented between the LNA and mixers. The measured RF response in Figure 6.7 shows a 300-MHz shift in the load

resonance from the designed 2.05 GHz. This was due to the models used for passive components and parasitic effects in the resonator. The input impedance of the baseband block varies according to the gain control setting and the mixers have to drive the load with only slight changes in the gain. The drop in the gain, shown in Figure 6.8, is only 0.5 dB to the minimum load impedance (460Ω, differential), which has a negligible effect on system performance. Two capacitors at the output of the mixer produce a pole at 6 MHz in Figure 6.9. The pole relaxes the linearity requirements of the baseband block. The IIP3, IIP2 and compression point in Figure 6.10 were measured in the passband using a 2 GHz f_{LO} and RF inputs at 2.003 and 2.00425 GHz.

Table 6.1. The summarized performance of the RF front-end.

NF(DSB) integrated from 100kHz to 2 MHz	[dB]	4.0
Voltage gain max.	[dB]	27.5
IIP3	[dBm]	-9
IIP2	[dBm]	+43
-1 dB compression	[dBm]	-25
LO-to-RF isolation	[dB]	>66
I/Q gain imbalance	[dB]	< 0.6
I/Q phase imbalance	[deg]	< 1°
P(LO)	[dBm]	-5
S11	[dB]	< -10
Idd (LNA)	[mA]	4
Idd (mixer)	[mA]	4
Idd (with biasing and buffering)	[mA]	41
Supply	[V]	2.75
Active area	[mm^2]	1.2×1.7

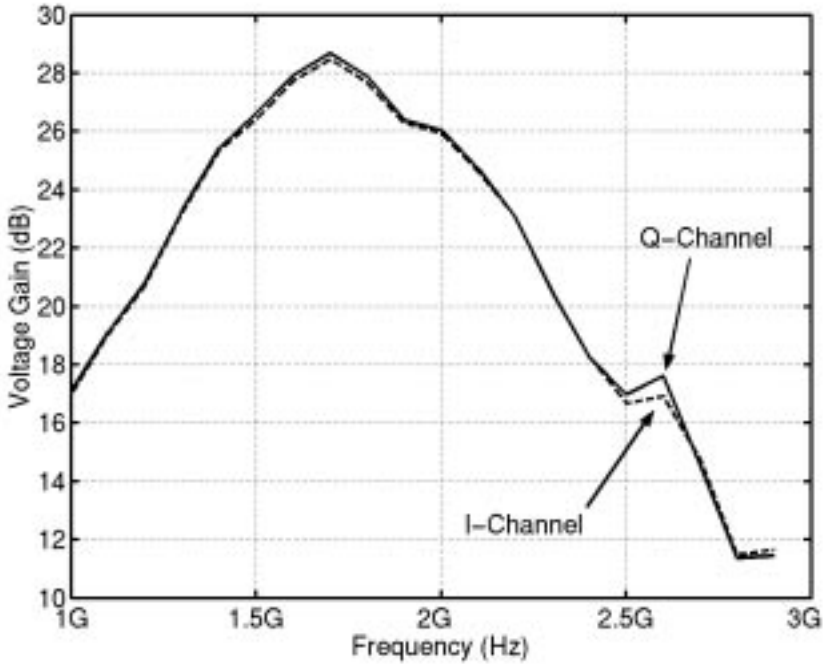

Figure 6.7. The measured RF response in the I and Q channels with a fixed IF of 200 kHz.

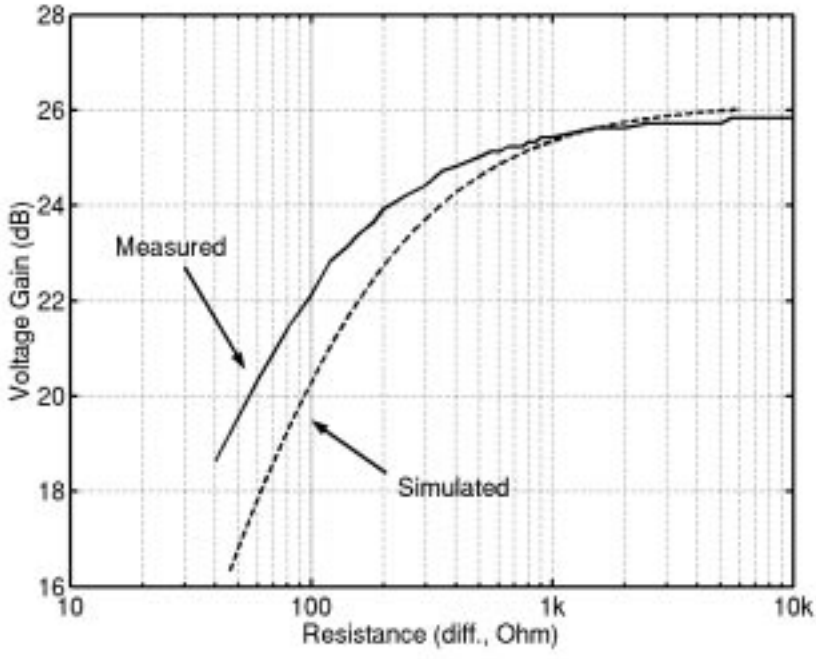

Figure 6.8. Driving capability of the mixer output. The minimum input resistance of the following baseband circuit is 460 Ω.

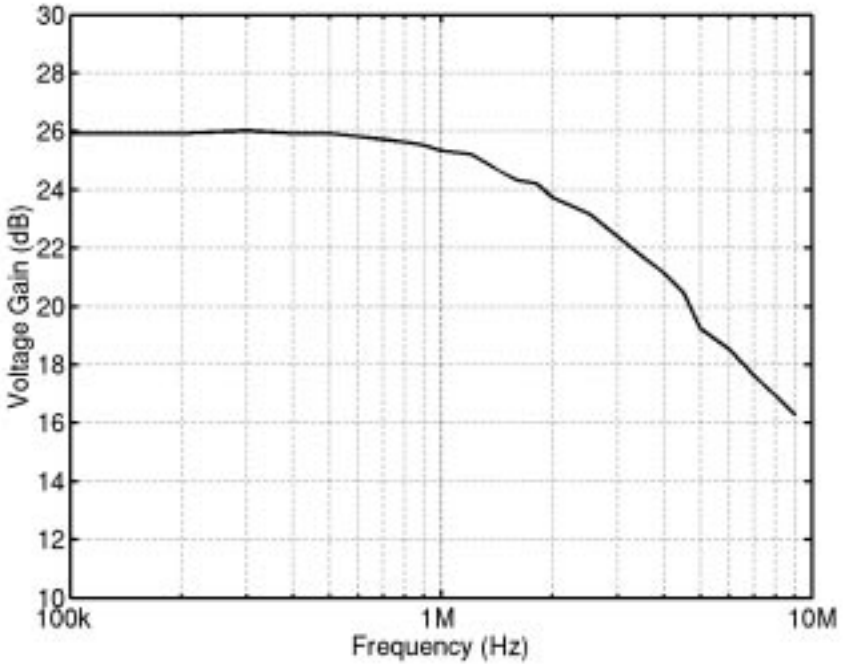

Figure 6.9. IF response of the front-end showing the effect of the mixer pole (f_{LO}=2 GHz).

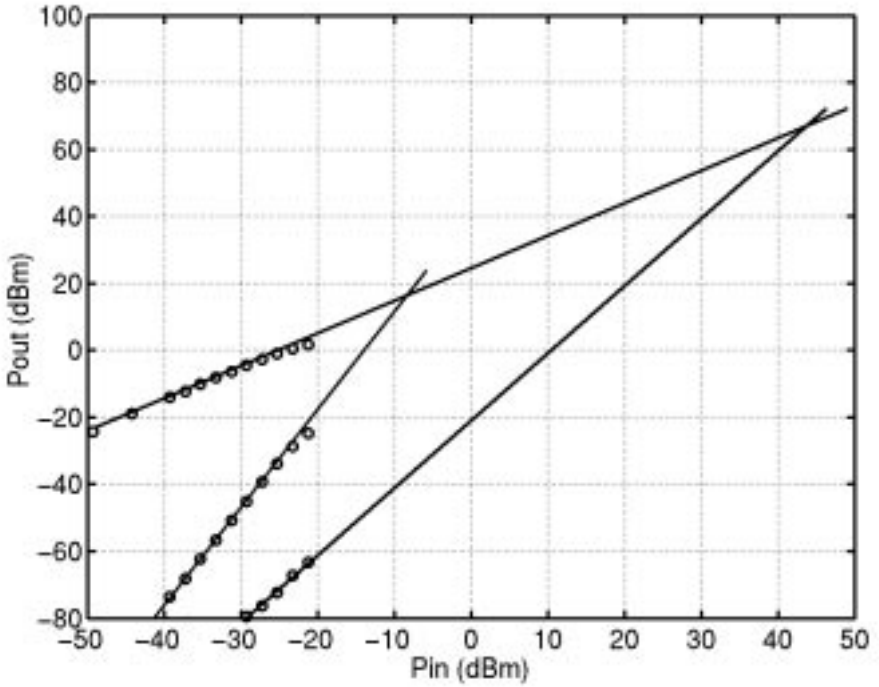

Figure 6.10. RF front-end linearity (f_{RF1}=2.003, f_{RF2} =2.0045 GHz, f_{LO}=2.000 GHz).

The performance of the chip was also measured with a supply voltage of 2.1 V. This had a negligible effect on gain and linearity. Only the DC-level at the mixer output shifted for the designed value. A microphotograph of the chip is shown in Figure 6.11.

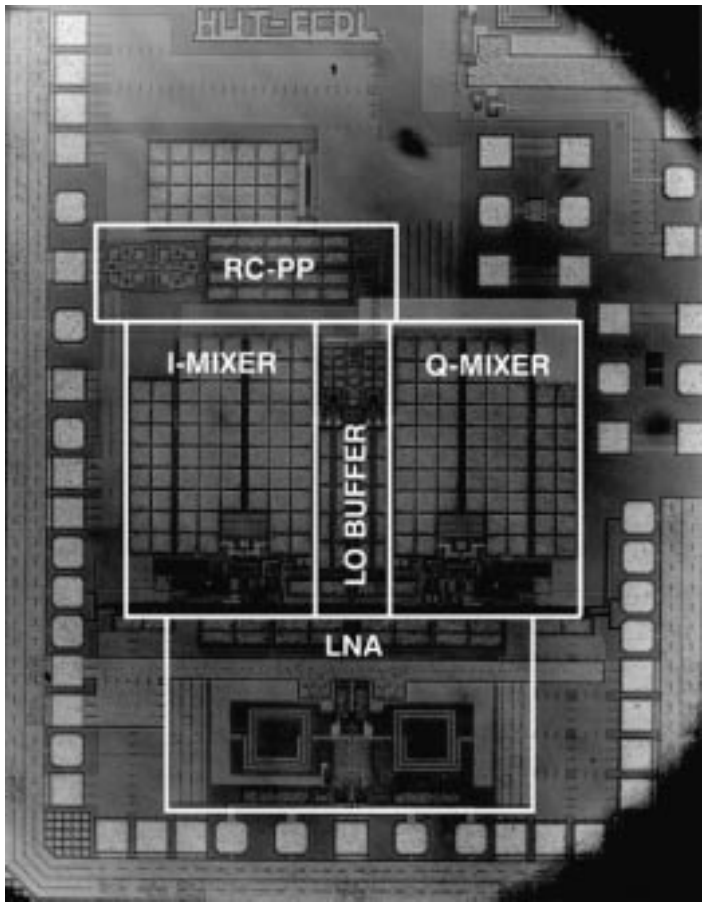

Figure 6.11. Microphotograph of the chip.

6.2 22-mA, 3.0-dB NF direct-conversion receiver for 3G WCDMA

A 2-GHz single-chip direct-conversion receiver including on-chip A/D converters achieves a 3.0-dB NF(DSB) and –14-dBm IIP3 with 60-mW power consumption from a 2.7-V supply. The receiver was designed according to the UTRA/FDD specification proposal [11]. The low power consumption was achieved with proper partitioning and by avoiding buffering between blocks. In the differential RF front-end, current-boosted quadrature mixers follow the programmable-gain low-noise amplifier. In the baseband, on-chip AC-coupled highpass filters are utilized to implement amplification with a programmable gain having small transients related to gain steps. The outputs of the fifth-order analog channel-select filters, which achieve 36-dB adjacent-channel attenuation, are sampled directly by the two single-amplifier 6-bit pipeline A/D converters. The block diagram of the chip, which was fabricated with a 0.35-μm 45-GHz f_T SiGe BiCMOS process, is shown in Figure 6.12.

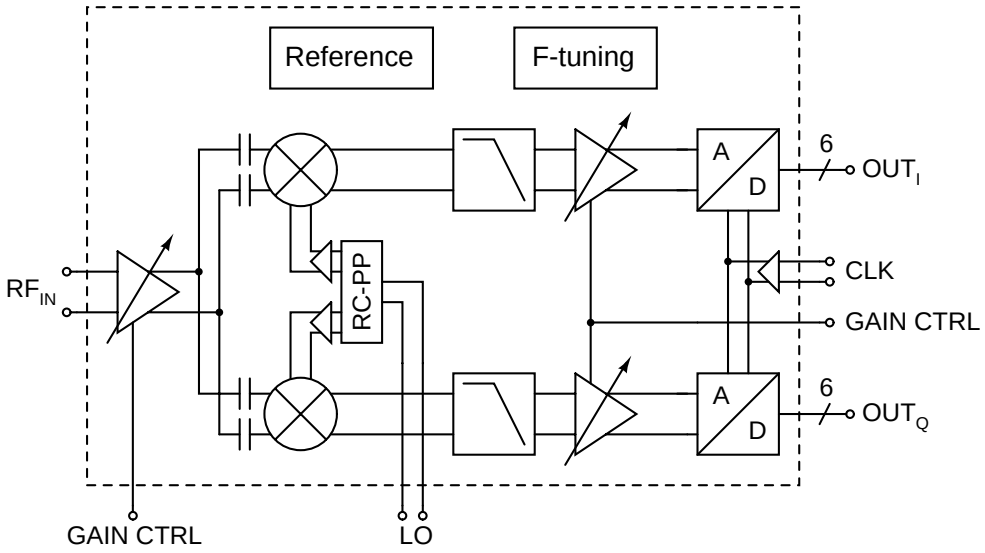

Figure 6.12. Receiver block diagram.

When an RF input signal is converted to digital form on the same chip as sensitive RF circuits the feedthrough of the clock harmonics to the RF input creates spurious tones, which can fall into the band of the desired channel, thus decreasing the SNR [4]. Although wide-band CDMA systems are less sensitive to downconverted clock harmonics, extremely good isolation is still required between the analog and digital blocks. Only a few millivolts of clock distortion can be allowed at the output of a WCDMA receiver that has a voltage gain of almost 100 dB.

6.2.1 LNA

A differential inductively-degenerated LNA was chosen because of the presence of digital circuits on the same chip. The bipolar LNA has two modes, with a 21-dB difference in the gain. A single branch of the LNA switched into high-gain mode is shown in Figure 6.13. In this mode, the transistors Q1 and Q2 operate as a cascode common-emitter LNA. In low-gain mode, Q1 is turned off and Q3 is operating in a common-base configuration [12]. With a resistive degeneration the linearity is improved by 17 dB, compared to high-gain mode with an equal supply current. In the high gain mode, the base inductance is reduced to a realizable value using the capacitor C1. The resonator load is damped with parallel resistors. Hence, a sufficient bandwidth and tolerance against device parameter deviations are achieved without a significant increase in the noise figure (NF). The base inductors of the LNA are implemented with bonding wires, while the other matching elements are placed on the chip. The AC-coupled interface with the quadrature mixers filters out the wide-spread envelope beat around the DC, which is generated in the LNA. The LNA draws 3.0 mA from a 2.7-V supply. According to simulations the voltage gain, NF, and IIP3 of the LNA are 23.1 dB, 1.35 dB, and –10.2 dBm, respectively. In addition, the main contributors to the LNA output noise power are the input transistors (50%), biasing (15%), and the emitter inductors (8%).

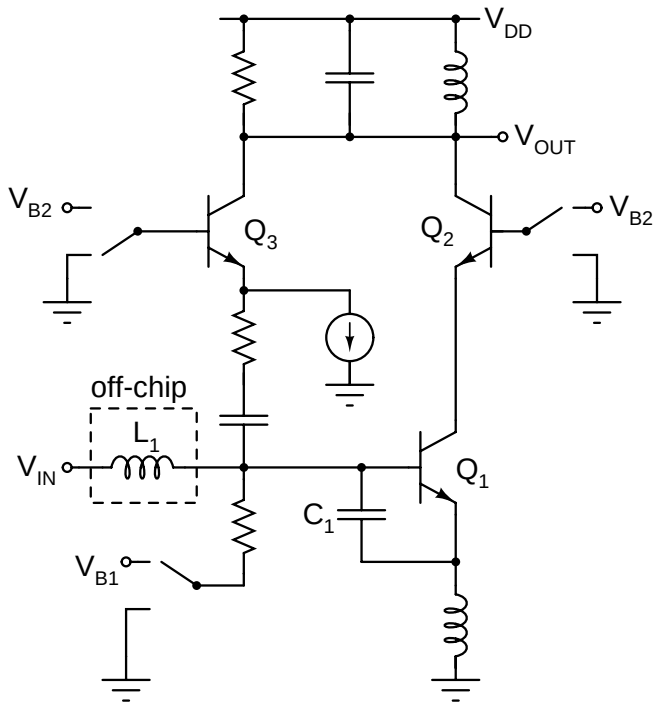

Figure 6.13. Single branch of the LNA in high-gain mode.

6.2.2 Downconversion mixer

The downconversion mixer in Figure 6.14 uses a modified Gilbert cell topology. NMOS input transistors are used because of their better linearity. The bipolar switching transistors create a lower flicker noise and perform proper switching with a smaller LO signal swing than MOS devices. The current boosting of the input stage in the modified Gilbert cell mixer ensures a sufficient gain from a low supply voltage, since the load resistors can be enlarged without lowering the output DC voltage, as the supply current through them is reduced [13]. It also conserves the third-order linearity performance as the current through the input transistors, which limits the mixer IIP3, does not need to be reduced. The current boosting adds new noise sources to the mixer. However, the voltages at the drains of the input transistors are far below the positive supply voltage and therefore the current source PMOS transistors can be designed to have a small g_m and thus a low noise. The current boosting decreases the noise contribution of the bipolar commutating switches without causing their linearity to deteriorate. As a consequence, the total NF of the mixer is decreased. Each mixer consumes 2.8 mA.

An external LO signal is brought through a two-stage RC polyphase filter. The input of the two-stage polyphase filter is matched by bonding wires to 50 Ω. The loss of the filter is compensated with limiting LO-driving buffers, which are resistively-degenerated bipolar differential pairs with resistor loads. A single buffer consumes 0.8 mA. The acceptable LO input power range is from -10 dBm to 0 dBm.

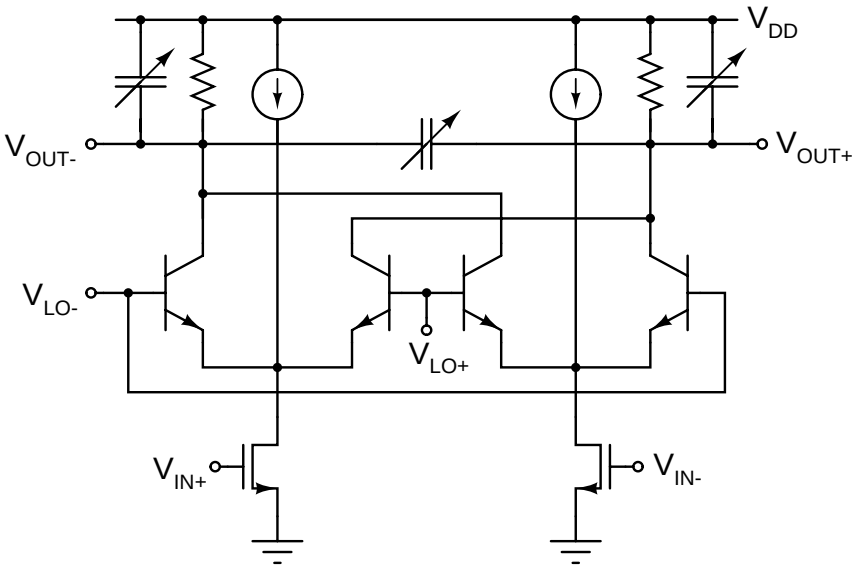

Figure 6.14. Downconversion mixer.

The mixer load is an on-chip RC structure forming the real pole of the odd-order lowpass filter used for the channel selection [14]. Since the resistor values are in the order of 1 kΩ, the capacitor is implemented mostly as an unit capacitors connected between the mixer outputs so as to minimize the silicon area. The PMOS switches, which are used in the capacitor matrix to tune the time constant of the pole are so large that they do not cause any significant distortion.

6.2.3 Analog baseband circuit and A/D converters

The analog baseband circuit consists of two similar signal channels, a frequency tuning circuit and voltage and current references. One signal channel, shown in Figure 6.15, includes an analog channel-select filter, amplification with programmable gain, and three on-chip highpass filters (HPFs), which filter out offsets.

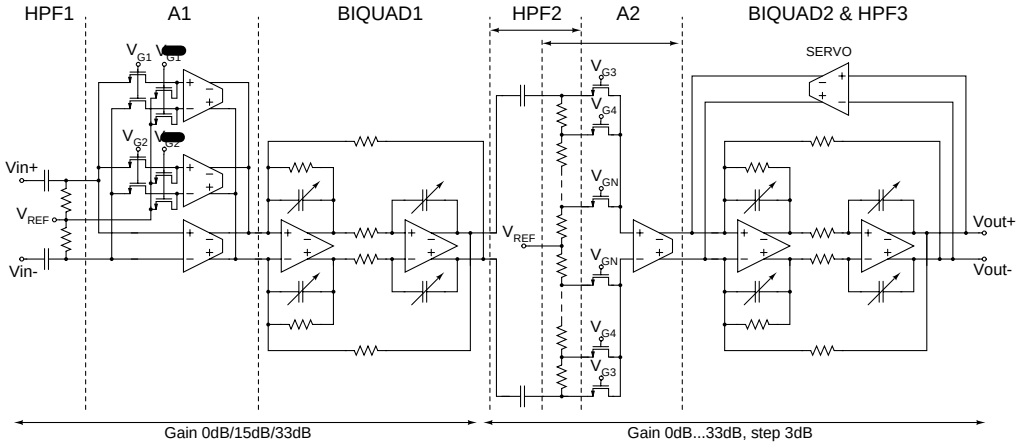

Figure 6.15. One signal channel of the analog baseband circuit.

The channel-select filter is a fifth-order Chebyshev lowpass filter with a 0.01-dB passband ripple and -3-dB frequency of 1.92 MHz. The filter approximates the root raised cosine filter with a 0.22 roll-off, thus realizing the channel-select filtering and chip shaping in the analog domain. Ideally, the adjacent channel attenuation of the channel-select filter is slightly over 36 dB with a 3.84-Mcps chip rate and 5-MHz channel spacing.

The real pole at the mixer output, which in this case is located at 1.2 MHz, increases the linearity considerably by attenuating the out-of-band signals before the signal processing with active devices. Here the pole is followed by a PMOS differential pair (A1) loaded with the first opamp-RC biquad. The HPF between the mixer output and differential pair (HPF1) prevents the offset at the mixer output from causing the balance of the differential pair to deteriorate and significantly decreasing the IIP2 of the analog baseband circuit. In this design, the adjustable gain, which ranges from 0 dB to 66 dB in 3-dB steps, is implemented with the inter-stage transconductors A1 and A2, shown in Figure 6.15. A1 is a parallel combination of three PMOS differential pairs. Transconductance (g_m) is decreased in two large steps by disconnecting the inputs of a transconductor from the signal path with V_{G1} and V_{G2}. In order to minimize the transients, the transconductor bias currents are not switched off. The differential pairs implementing the two smaller g_ms are resistively degenerated. In A2, the variable attenuation is implemented with a resistive voltage divider, controlled with V_{G3}…V_{GN} and followed by a resistively-degenerated PMOS differential pair with a fixed g_m.

The two 6-bit 15.36 MS/s pipeline ADCs directly sample the output of the continuous-time channel-select filter. The ADCs are implemented using two 2.5-bit stages followed by a 2-bit flash stage as indicated in the block diagram shown in Figure 6.16. Each 2.5-bit stage consists of a multiplying D/A converter (MDAC) and a six-level sub-ADC with a small decoding logic [15]. The properly-delayed output bits of each stage are fed to a redundant sign digit (RSD) correction circuitry [16] and finally buffered out of the chip in parallel. The current consumption of the ADC reduced by alternating a single opamp between the two consecutive stages, exploiting the property of successive stages working in opposite clock phases.

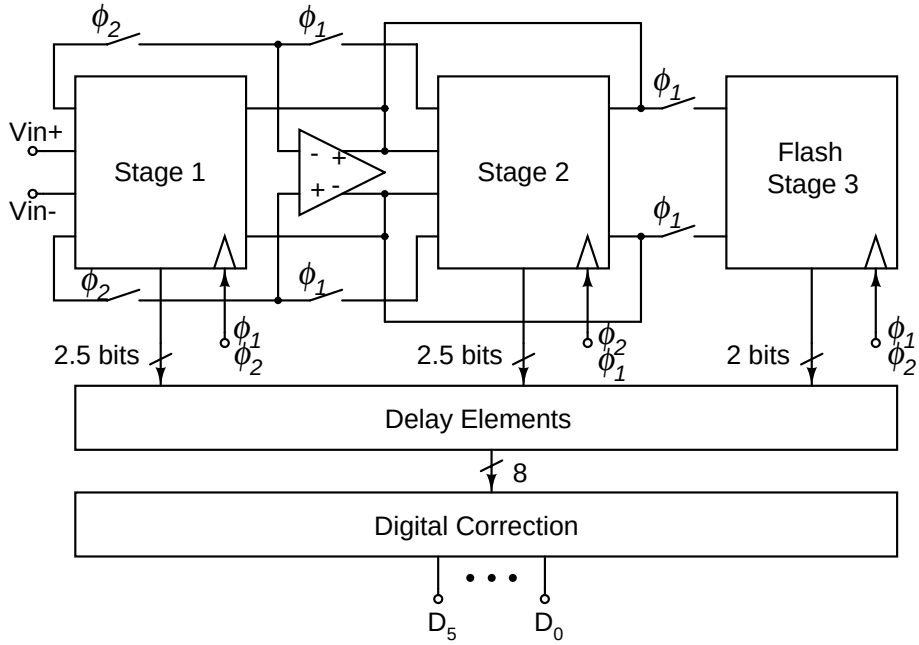

Figure 6.16. A/D converter block diagram.

The coupling of the clock signal into the sensitive RF input is the key issue in single-chip receivers [4]. A high level of isolation is achieved by separating the digital parts into an isolated p-well in the BiCMOS process. The contribution of the ADC clock to the substrate noise is reduced by using a differential sinusoidal clock input with low amplitude, which is amplified on-chip into a sharp rail-to-rail clock signal. In addition, the output buffers are designed to have slow rise and fall times and on-chip decoupling capacitors are used in the supply voltage lines of the ADCs and RF front-end.

6.2.4 Experimental results

The receiver is fabricated with a 0.35-μm 45-GHz f_T SiGe BiCMOS process. The measured performance parameters of the receiver are given in Table 6.2. The chip area is 10.3 mm^2, including the bonding pads. The receiver is mounted and bonded directly on a printed circuit board (PCB). Although separate supplies are used on the chip a single supply is used on the PCB. All bonding pads are ESD-protected. External baluns are used at the RF and LO inputs. An external –3-dBm 2.0-GHz LO was used for the measurements unless otherwise mentioned. A microphotograph of the receiver is shown in Figure 6.17.

Table 6.2. Summarized performance of the receiver.

Supply voltage	[V]	2.7
Current consumption	[mA]	22
Voltage gain	[dB]	12…99
NF (DSB)	[dB]	3.0
Out-of-band IIP3 (high / low RF gain)	[dBm]	-14 / +3
Out-of-band IIP2 (high / low RF gain)	[dBm]	+17 / +43
-1dB compression (high / low RF gain)	[dBm]	-27 / -7
LO-to-RF isolation	[dB]	> 65
S11 (high / low RF gain)	[dB]	< -11 / -13
Baseband gain range / step / step error	[dB]	66 / 3.0 / 0.4
Filter bandwidth imbalance	[%]	< 0.5
Adjacent channel attenuation	[dB]	36

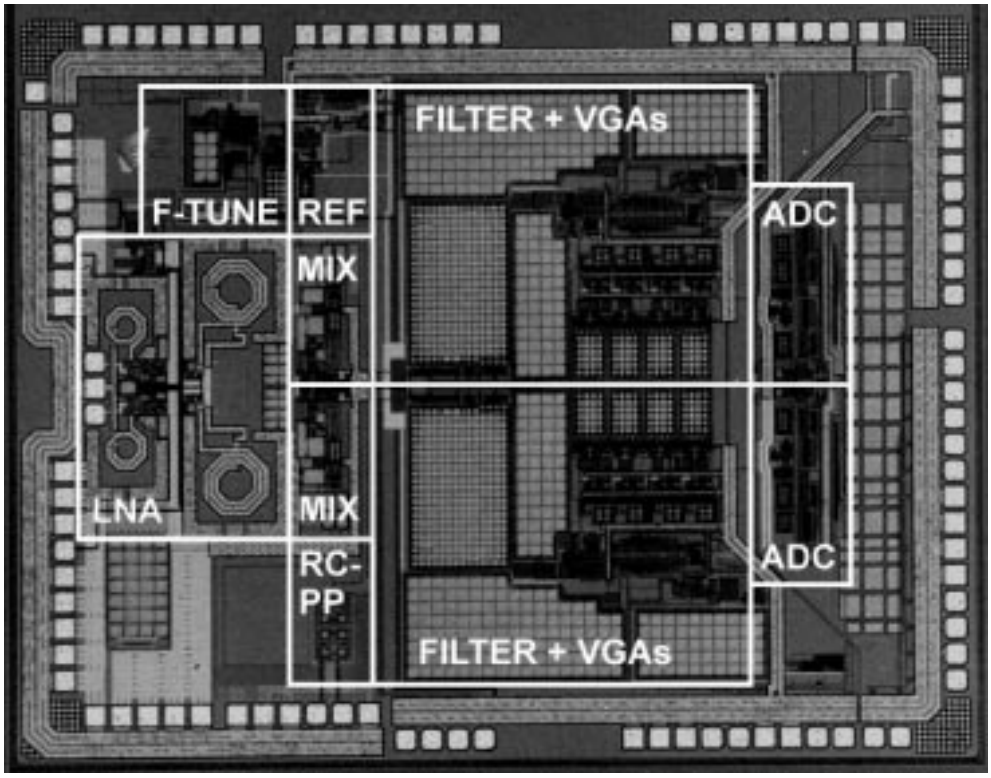

Figure 6.17. Chip microphotograph.

The receiver voltage gain at high and low RF gains is shown in Figure 6.18 as a function of the LO frequency. The gain at 2.0 GHz is 99 dB and the RF gain step, which is shown in Figure 6.19, is approximately 21 dB. The constant frequency offset between the LO and RF signals is 200 kHz. The baseband gain is at the maximum in both cases. The measured input matching of the LNA at the high and low RF gain values is shown in Figure 6.20. The S11 is better than –11 dB in both WCDMA bands at both gain settings. The notch at 2.7 GHz is not designed and comes from the PCB. The measured LO-to-RF isolation from the differential LO input to the differential RF-input is higher than 65 dB.

Receiver NF is measured at the ADC output. The equivalent noise bandwidth of the receiver, which must be used in the NF calculations, is derived from the measured frequency response of the channel-select filter. The receiver NF as a function of the LNA quiescent current is shown in Figure 6.21. The nominal LNA current is 3.0 mA. With a minor increase in the total current consumption the receiver NF can be decreased to 2.6 dB. The contribution of different building blocks to the noise power generated in the receiver at the maximum gain is approximately 50 % in the LNA, 40-% in the downconversion mixers, and 10 % in the analog baseband circuit. The noise generated in the mixer load resistors and ADC is included in the noise of the analog baseband circuit. With the maximum gain, the input-referred noise of the analog baseband circuit corresponds to 12 nV/√Hz. With the low RF and maximum baseband gain the receiver NF is 20 dB.

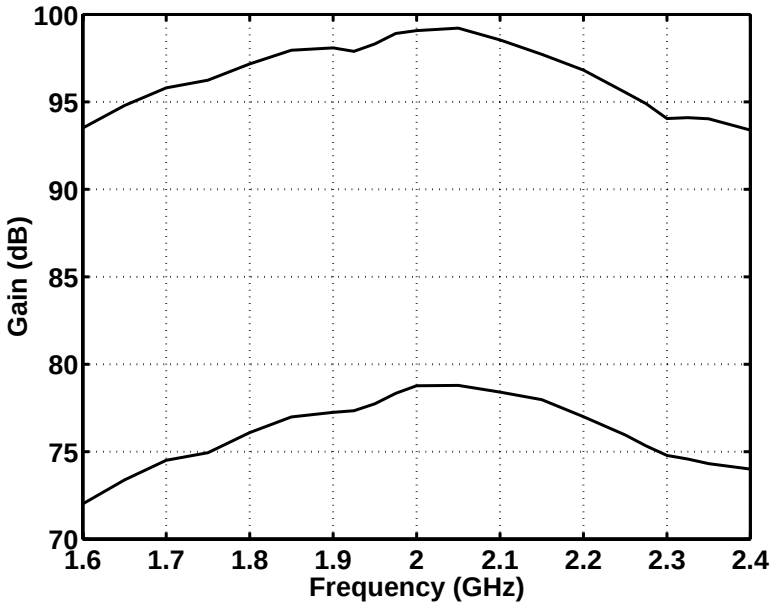

Figure 6.18. Receiver voltage gain at high and low RF gains. The baseband gain is at the maximum.

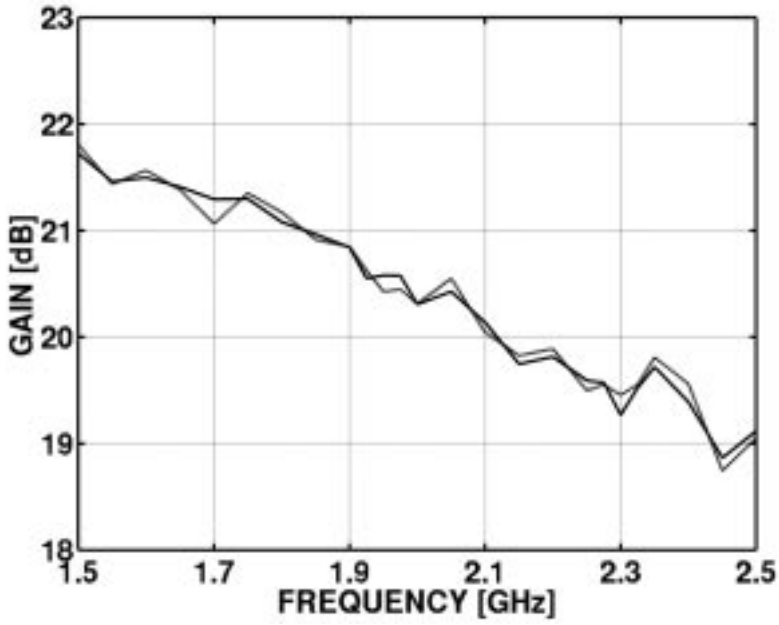

Figure 6.19. RF gain step of I- (solid line) and Q-channels (dashed line) as a function of LO frequency.

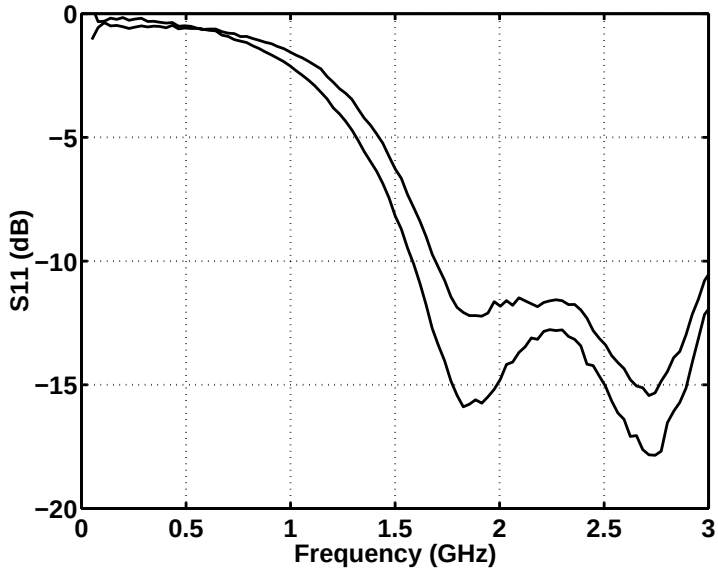

Figure 6.20. Input matching of the LNA at high (upper curve) and low RF gains.

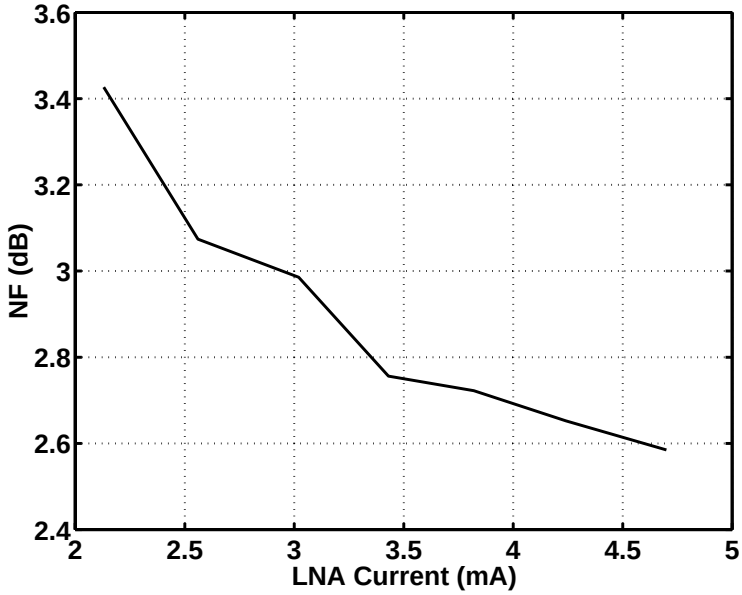

Figure 6.21. Receiver NF as a function of LNA quiescent current.

The IIP3 and IIP2 of the receiver are measured with 10-MHz + 20.2-MHz and 10-MHz + 10.2-MHz downconverted signals, respectively. The +17-dBm IIP2 with the high RF gain is the worst case out of several measured samples. The highest measured IIP2 value with the high RF gain is +34 dBm. An example of the two-tone test spectrum in the IIP3 measurement is shown in Figure 6.22. The tone at 40 kHz comes from the measurement setup. With –48-dBm test signals at the input and a 99-dB voltage gain the IIP3 is –14 dBm. The input power is referred

to 100 Ω because of the differential input. The expected IIP2 of the analog baseband circuit with 10-MHz + 10.2-MHz test signals is over +75 dBV [17]. With a 33-dB RF voltage gain the simulated IIP3 of the analog baseband circuit with 10-MHz + 20.2-MHz test signals corresponds to +2 dBm at the receiver input and does not limit the performance. The effect of the analog baseband circuit on the linearity of the whole receiver was found out by increasing the frequencies of the test signals. The RF front-end limits the IIP3 and IIP2 since a change in the frequencies of the test signals did not affect the results. The blocking performance is defined using a blocker at a 15-MHz offset from LO and measuring the compression of a small in-band signal. The in-band signal compressed with a –27-dBm blocker at the maximum receiver gain, as shown in Table 6.2.

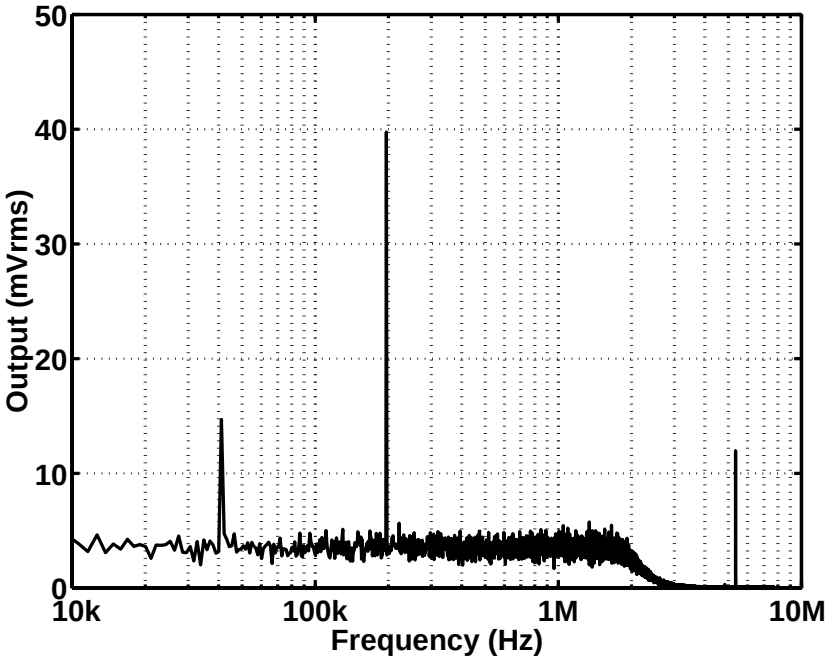

Figure 6.22. IIP3 test at the maximum receiver gain. With –48-dBm input signals at 10.0-MHz and 20.2-MHz offsets from the LO the 40-mV_{RMS} distortion component at the output corresponds to –14-dBm IIP3.

The measured frequency response of the channel selection filter at low RF and maximum baseband gain is shown in Figure 6.23. A good matching between the simulated and measured frequency responses is achieved, although cascaded filter sections are used. The adjacent channel attenuation was measured using a modulated WCDMA channel at a 5-MHz offset from the LO. The attenuation, compared to a WCDMA channel at the LO frequency, is over 36 dB when the –3-dB frequency of the filter is 1.92 MHz. The measured current consumption of the whole analog baseband circuit is 7.5 mA.

The differential nonlinearity (DNL) and integral nonlinearity (INL) of the A/D-converter were found by means of the code density test to be 0.27 LSB and 0.18 LSB, respectively. The signal-to-noise and distortion ratio (SNDR) was also estimated from the code density test and is at least 35.6 dB, which corresponds to an effective number of bits (ENOB) of 5.6 bits (7.12-MHz input signal). The SFDR of the converter was measured with the fast Fourier transformation characterization. The SFDR is limited by the third-order distortion and is more than 50 dB over

the whole Nyquist band. The two ADCs draw a supply current of 4.5 mA including the output buffers. The current consumption of the twelve output buffers is included in the 22-mA current consumption of the whole receiver.

The spurious tone due to the feedthrough of clock harmonics to the RF input is measured using a 15.36-MS/s sample rate in the ADCs. The magnitude of the tone is measured as a function of the LO frequency over a 300-MHz band around 2 GHz. The LO frequencies are chosen in such a way that the downconverted spurious tone is located at 200 kHz. The worst clock spurious is smaller than 20 mV at the output, causing degradation of less than 0.1 dB in the 3.0-dB total NF.

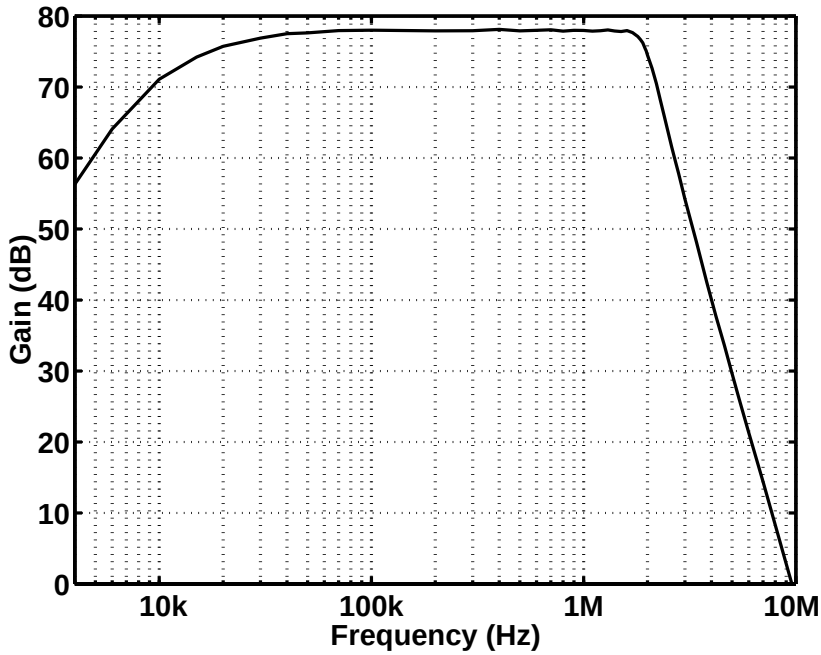

Figure 6.23. Measured filter frequency response at low RF gain and maximum baseband gain.

6.3 Dual-band RF front-end for WCDMA and GSM applications

An RF front-end for dual-band, dual-mode operation is presented in this section. The front-end consumes 22.5 mW from a 1.8-V supply and is designed to be used in a direct conversion WCDMA and GSM receiver. The front-end was fabricated in a 0.35-μm BiCMOS process and, in both modes, can use the same devices in the signal path except the LNA input transistors. The front-end has a 27-dB gain control range, which is divided between the LNA and quadrature mixers. The measured NF (DSB) and voltage gain are 2.3 dB and 39.5 dB for GSM, and 4.3 dB and 33 dB for WCDMA, respectively. The linearity parameters IIP3 and IIP2 are -19 dBm and +35 dBm for GSM, and –14.5 dBm and +34 dBm for WCDMA, respectively.

The RF front-end is intended for GSM and third-generation WCDMA applications and designed using specifications related to these standards [11], [18]. The main characteristics of

the two systems are shown in Table 6.3. The challenges for an RF designer set by the standards are related to the different reception bands. GSM operates at 900 MHz, while the WCDMA bands are around 2 GHz. In addition, the two systems have a different channel spacing and symbol rate. This clearly affects the channel-select filtering but the 1/f-noise can cause significant degradation in noise performance, particularly in the case of direct-conversion receivers with a narrow channel bandwidth [19], such as GSM.

Table 6.3. WCDMA and GSM system characteristics.

	WCDMA	GSM
Main application	Data	Voice
Access method	DS-CDMA	TDMA
Duplexing	FDD	TDD/FDD
Modulation	QPSK	GMSK
Receive bands		
Base station [MHz]	1920-1980	880-915
Mobile station [MHz]	2110-2170	925-960
Channel spacing	5 MHz	200 kHz

6.3.1 RF front-end for direct-conversion receivers

A block diagram of the RF front-end that was designed is shown in Figure 6.24. It has two separate single-ended inputs, one input for each standard. The separate inputs are used to make separate pre-select filters possible. Furthermore, if the two reception bands were connected simultaneously to the same input, the spurious responses could corrupt the reception. With the exception of the input transistors and matching inductors of the LNA, all on-chip devices are utilized in both modes. The single-ended-to-differential conversion is performed before the signal downconversion, thus making possible a double-balanced mixer topology. The single-ended-to-differential converter additionally improves the LO-to-RF isolation and separates the two differently-sized resonators of the LNA from the mixer. The RF front-end requires only one differential LO port because one mode is selected to be operational at a time. If the receiver had two LO signals, spurious tones could corrupt the reception, particularly if the A/D converters were implemented on the same chip [4]. The LO is external and the 90° phase shift is performed off-chip. In multi-band receivers, it is impractical to perform the quadrature generation with poly-phase filters. Each standard at a different frequency band would require its own filter structure, thus leading to parallel filters and a very complicated interface design. A possible solution generating quadrature LO would be to use divide-by-two circuits.

The signal paths between the different blocks are AC-coupled with 10-pF on-chip capacitors. Hence, the low-frequency distortion components generated by the second-order nonlinearities in the LNA and single-ended-to-differential converter are filtered out before downconversion. Otherwise, they could partly leak through the mixer to the output. A fully-differential signal path could also be used throughout the front-end to reduce the effect of common-mode distortion and noise [20]. However, it would double the power consumption of the LNA, increase the chip area, and require a balun in front of the LNA, thus increasing the loss between

the antenna and the receiver. The front-end has a tunable gain in order to relax the baseband linearity and gain control requirements. The gain control is divided between the mixer and the LNA. The combined current consumption of the LNA and single-ended-to-differential converter is 6.6 mA in GSM and 6.1 mA in WCDMA mode. A single mixer uses 3 mA.

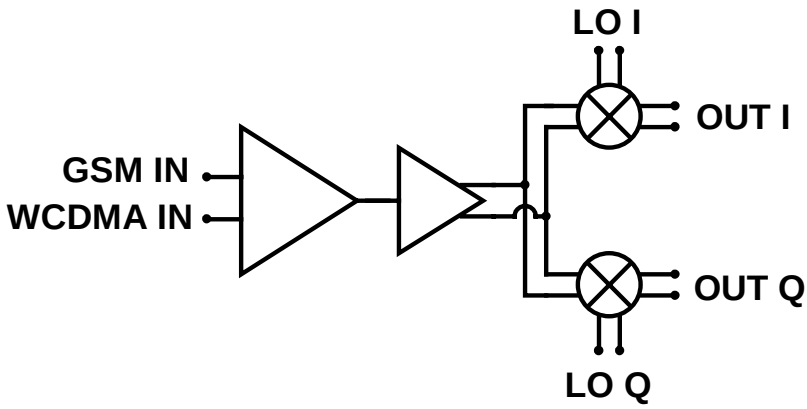

Figure 6.24. Block diagram of the RF front-end.

6.3.2 LNA

The schematic of the LNA operating in WCDMA mode with the maximum gain is shown in Figure 6.25. The LNA uses a conventional common-emitter topology with cascode transistors at all gain and mode settings to achieve a good reverse isolation with high gain and low NF. The transistors Q1 and Q2 are used as the input transistors for different modes. The base and emitter inductors of the transistors Q1 and Q2 are used for matching. In GSM mode, the capacitor, Cm, is also added between the base and emitter of Q2 to reduce the value of the base inductor, Lb2, to a realizable value. Depending on whether the LNA is used in WCDMA or in GSM mode, one of the input transistors is biased on, while the other is off. The transistor, which is turned off, has a negligible effect on the NF and the signals coming to the base of this transistor are shunted to chip ground. Therefore, the signals which pass through the non-operational pre-select filter cannot desensitize the LNA. The LNA has two damped resonators, which are used as loads in different modes. The resonance frequencies are 950 MHz and 2.1 GHz, respectively. The damping resistors RL1 (250 Ω) and RL2 (150 Ω) give a sufficient bandwidth for both mobile terminal and base station usage and tolerance against different process variations without causing the noise performance of the LNA to deteriorate significantly. The –1 dB bandwidths are 350 MHz and 150 MHz for WCDMA and GSM resonators, respectively. The active output port and the load resonator of the LNA are selected with the biasing of the cascode transistors.

The LNA has two gain steps in both modes, which are implemented in the following manner. At the maximum gain, the LNA uses the damped resonator of the appropriate mode as a load. For example, in WCDMA mode, Q1 acts as an input transistor, Q3 as a cascode, and RL1, C1, and L1 as the load. Depending on the standard chosen, the first gain step is realized by connecting another resistor in parallel with the resonator by closing the PMOS switch S1 or S2 so as to reduce the Q value of the resonator. The sizing of the switch constitutes a trade-off between the on-resistance and parasitic capacitance, which both affect damping and resonant frequencies. The gain step is 3.2 dB in GSM mode and 2.8 dB in WCDMA mode at the resonant frequency. A larger LNA gain step is performed by connecting the resonator tuned for

the other mode as a load. In that case, the LNA does not operate at the resonance frequency and the gain is lowered by over 12 dB compared to the maximum. For example, in WCDMA mode, this gain step is performed by connecting Q3 to the chip ground and using Q4 as a cascode. In that case, the LNA uses the resonator L2, C2 and RL2 as the load and OUT2 instead of OUT1. The gain and mode control in the LNA are implemented using MOS switches, which steer the biasing of Q1-Q4, turning off the biasing of the unused devices. The input transistors are biased using current mirrors, while the cascode transistors use V_{be} multipliers. The use of two stacked diode-connected bipolar transistors in the biasing of the LNA cascode is not possible because of the low supply voltage. The LNA drives an AC-coupled single-ended-to-differential converter.

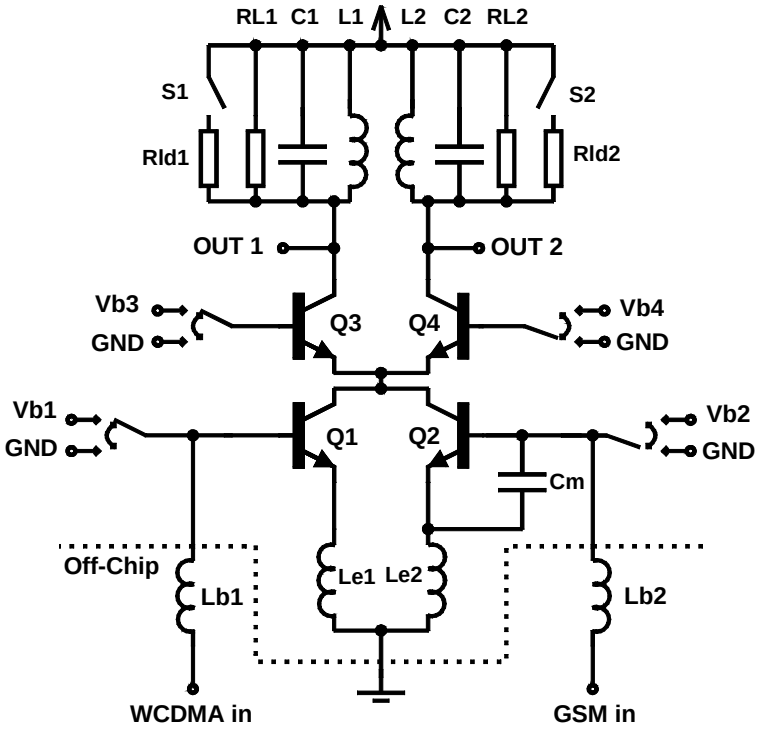

Figure 6.25. Schematics of the LNA.

6.3.3 Single-ended-to-differential converter

The single-ended-to-differential converter makes possible the use of double-balanced mixers and isolates the LNA load resonators. The schematic of the single-ended-to-differential converter is shown in Figure 6.26. The conversion is performed with either transistor Q5 or Q6 depending on the LNA resonator chosen. This kind of structure has some benefits compared to passive baluns or differential pair converters. Integrated passive baluns are not feasible because they require a large area and can only be used through part of the frequency band from 900 MHz to 2.2 GHz. A differential pair, on the other hand, cannot fulfill the high linearity requirements with a low supply and low current.

The converter has a 3-dB voltage gain when connected to the front-end. The maximum voltage gain to a high impedance load is 6 dB for this type of a converter. In order for a good balance to

be achieved, the load impedances seen from the emitter and collector of Q5 and Q6 must match well. Therefore, the supply inductances, L1 and L2, should also be equal. This was solved by using separate supply pads in the converter to ensure equal lengths and an equal number of bond wires. In addition, a dummy transistor Q7 is added to compensate for the effect of the collector capacitances of Q5 and Q6 [21]. According to simulations, the phase and gain errors are less than 4° and 0.2 dB over the operation range from 800 MHz to 2.2 GHz, respectively.

The single-ended LNA and the single-ended-to-differential converter are sensitive to supply noise. Therefore, an on-chip decoupling 100-pF capacitor with a small series resistor provides efficient damping without there being susceptibility to unwanted resonances.

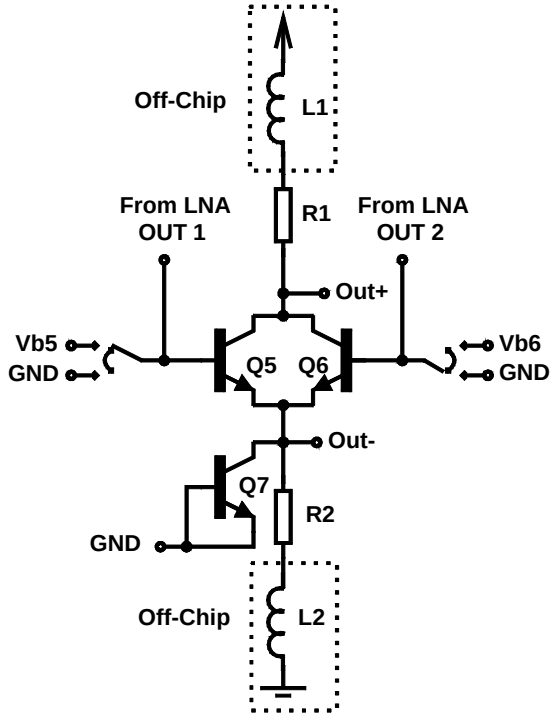

Figure 6.26. Schematics of the single-ended-to-differential converter.

6.3.4 Mixer

The mixer that was designed, shown in Figure 6.27, is basically a double-balanced cross-coupled Gilbert mixer. It utilizes NMOS transistors in its input stage with bipolar LO switches [1]. The advantage of using MOS transconductors (M1-M2), rather than bipolar ones, is in their better linearity performance. In addition, the mixer topology is current-boosted in order better to relax the lower supply voltage conditions [13]. The boosting makes possible the utilization of higher mixer conversion gain by allowing larger resistive loading in the mixer output. By current boosting, a lower mixer noise figure is achieved without the third-order linearity performance deteriorating. In this type of mixer without current boosting, the linearity and noise performance always trade off against each other. The linearity of the input transconductor can be maintained, since the drain currents through the input devices do not need to be lowered. The additional DC currents are fed through resistively-degenerated long-channel PMOS transistors.

The bipolar switching transistors (Q1-Q4) are used as the functional mixer core instead of the respective NMOS transistors because of their lower flicker noise. In addition, the bipolar transistors provide a higher f_T, which is required in order to achieve on-off switching that is as symmetrical as possible. Thus, the second-order distortion caused by the non-ideal LO signal duty-cycle is minimized. In addition, MOS switches typically require a larger swing in order to exhibit complete switching compared to bipolar ones. This relaxes the LO cross-coupling and isolation performance. The mixers provide adjustable-voltage conversion gain with three 4-dB gain control steps. The maximum voltage conversion gain is 14 dB. The gain control is implemented by switching additional resistor pairs between the mixer output terminals. The mixer has an RC lowpass pole at the output in order to relax the out-of-band linearity requirements of the following baseband stages and it is designed to drive a circuit, as in [17].

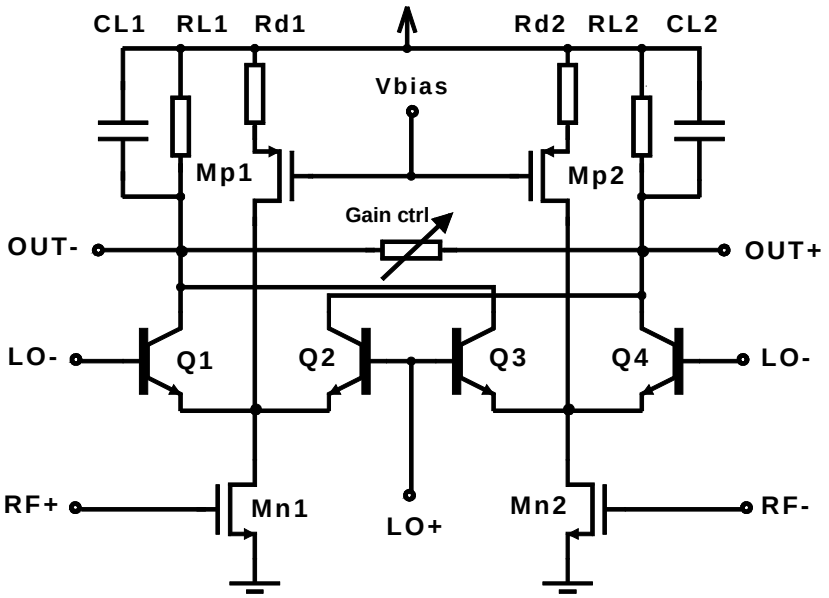

Figure 6.27. Schematics of the quadrature mixer.

The mixer was not implemented and measured as a stand-alone circuit because of the uncertainties in the linearity measurements of a single direct-conversion mixer without an LNA and on-chip LO buffers [22]. Nevertheless, the comparison between the stand-alone simulations of the mixer and the measurements of the whole front-end matches very well. The simulated IIP3 of the mixer is +10 dBm and +8 dBm for WCDMA and GSM, respectively. The simulated NF(DSB) is 9.5 dB at both bands.

6.3.5 Layout

A microphotograph of the circuit is shown in Figure 6.28. The designed front-end is implemented using a 25-GHz f_T BiCMOS process with a 0.35-μm minimum MOS gate length. The chip area is 3.5 mm^2, including the bonding pads. The two RF input pads are brought as close as possible to the LNA input transistors in order to minimize the wiring parasitics, which would affect NF and input matching. The LO and RF wiring are brought orthogonally to each other and grounded properly on both sides in order to achieve good LO-to-RF isolation. Also, the LO and RF wiring do not overlap even in the commutating switches. The balanced mixers are made as symmetrical as possible in order to minimize the second-order distortion.

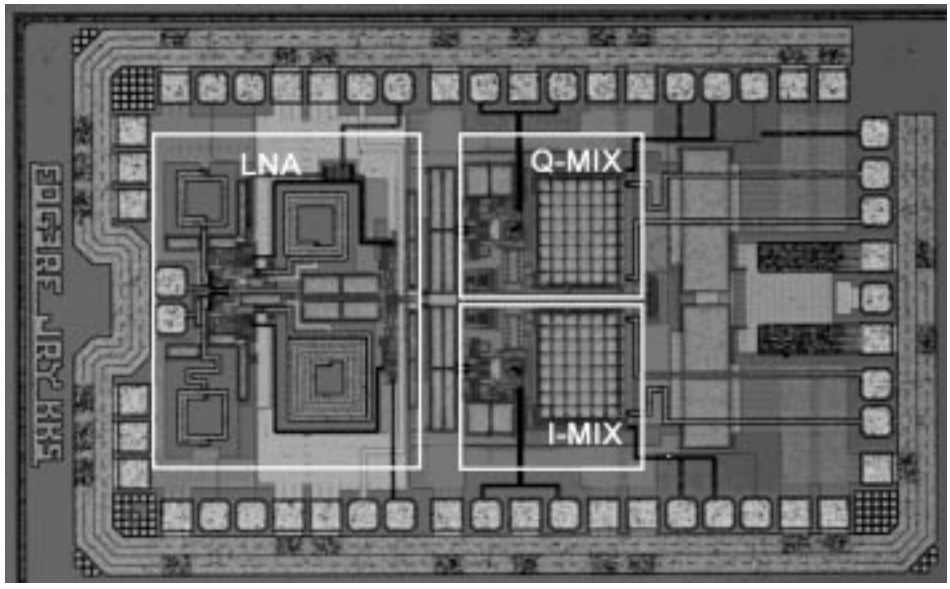

Figure 6.28. Chip microphotograph.

6.3.6 Experimental results

In direct-conversion receivers, the mixer output does not need to drive a 50-Ω impedance [23]. However, an external instrumentation buffer with a high input impedance was used to drive the 50-Ω measurement equipment. The front-end chip was bonded directly on a high-frequency ceramic PCB (RO4350); this is a compatible material with the standard FR4. All measurement results presented in this paper include the PCB. The main benefit of using RO4350 material compared to FR4 is its lower dissipation factor (0.0040), which has the effect of reducing input losses.

The measured performance of the RF front-end is summarized in Table 6.4. The RF responses of both modes at the maximum gain settings are shown in Figure 6.29. The simulated maximum gain was 39 dB in both modes. In GSM mode, this gain was achieved, while in the WCDMA mode the maximum gain was only 33 dB. Thus, the NF in WCDMA mode was also higher than expected according to the simulations. The difference between the simulated and measured gains in WCDMA mode was due to inaccurate transistor models at higher frequencies. Otherwise, all the other values measured matched to the simulations very well. Figure 6.30 illustrates all 12 possible gain values that can be achieved in WCDMA mode, while Figure 6.31 shows the RF responses of six different gain settings in GSM mode. In Figure 6.31, Curve A illustrates the maximum gain setting. Curves B-D show the mixer gain steps when the LNA gain is at maximum. Curves E, F present the LNA gain steps when the mixer is at minimum gain. The total gain control range is 27 dB for both modes. The variation in the gain between the mobile station reception and base station reception bands resulting from the RF response is less than 1 dB at all settings. The input matching in Figure 6.32 is independent of the front-end gain because the biasing of the input transistor remains the same with different gain settings. The reported S11 values for GSM and WCDMA cover both mobile station and base station reception bands.

Table 6.4. Measured performance in WCDMA and GSM modes.

		WCDMA	GSM
NF(DSB) @max gain	[dB]	4.3	2.3
NF(DSB) @min gain	[dB]	15.9	12.3
Voltage gain max	[dB]	33	39.5
Voltage gain min	[dB]	6.5	12
IIP3 @max gain	[dBm]	-14.5	-19
IIP3 @min gain	[dBm]	-7	-7.5
IIP2 @max gain	[dBm]	+34	+35
IIP2 @min gain	[dBm]	+32	+34
ICP –1dB @max gain	[dBm]	-25	-29
ICP –1dB @min gain	[dBm]	-20	-23
LO-to-RF isolation	[dB]	>58	>68
S11	[dB]	<-18	<-12
P(LO)	[dBm]	-10	-10
Power dissipation	[mW]	22.5	21.5
Supply voltage	[V]	1.8	1.8
Chip area	[mm^2]	3.5	3.5

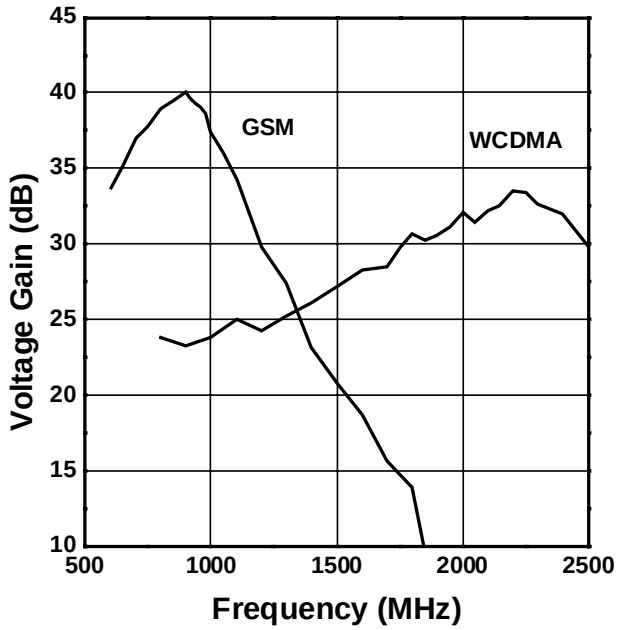

Figure 6.29. Maximum gain responses in both modes.

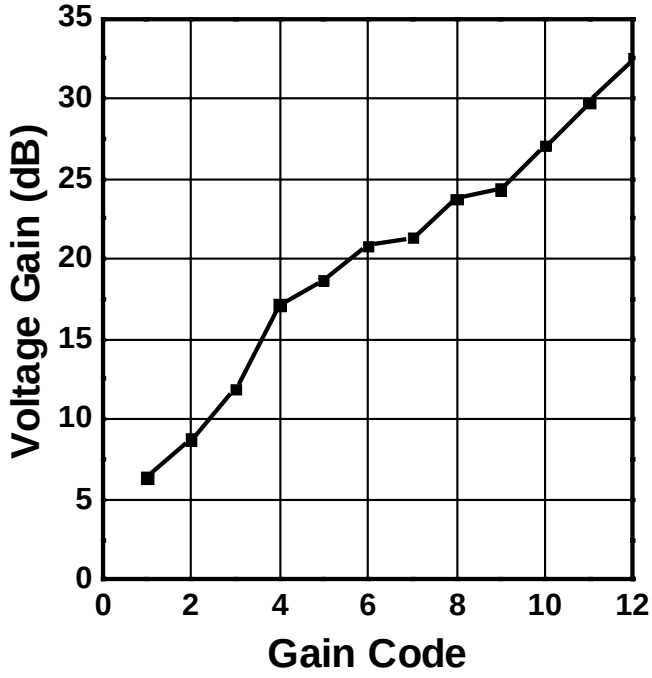

Figure 6.30. Gain in WCDMA mode at different tuning codes.

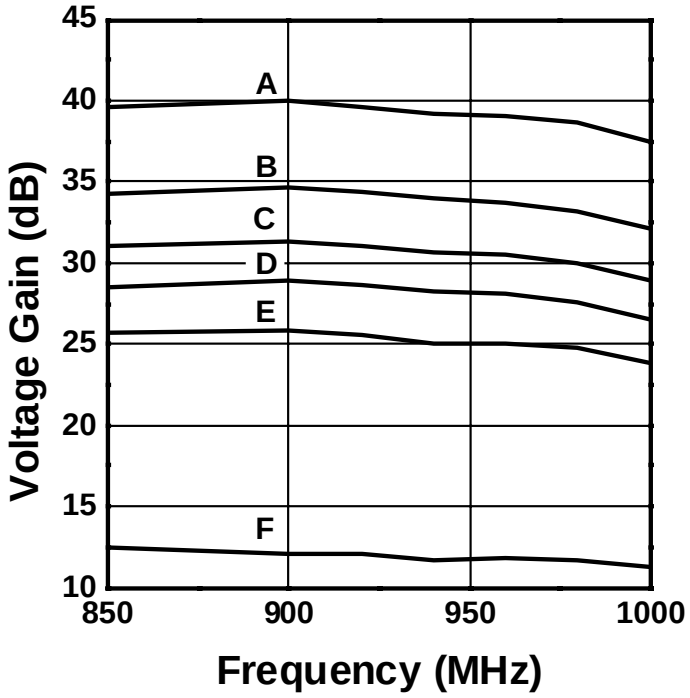

Figure 6.31. RF response with six different gain settings in GSM mode.

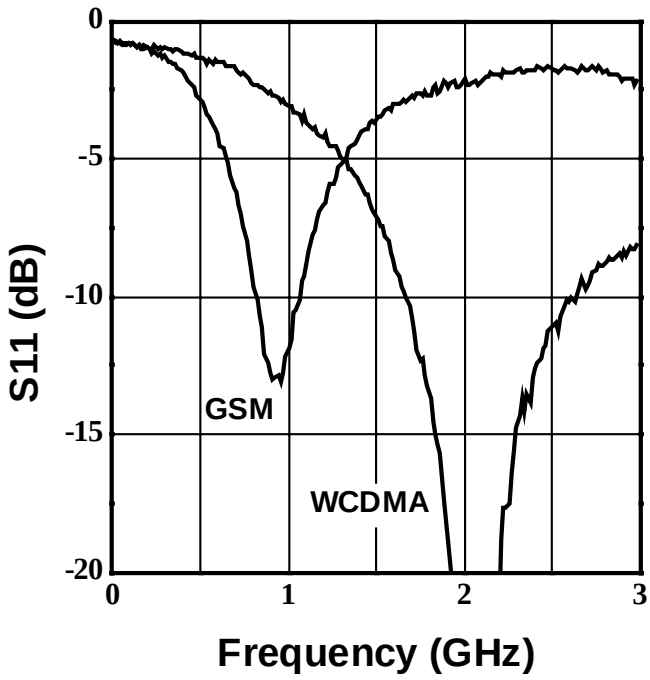

Figure 6.32. Input matching in both bands.

Figure 6.33 illustrates the spectrum of the output noise with maximum gain in both modes. The NF is 2.3 dB and 4.3 dB for GSM and WCDMA, respectively. The low flicker noise corner was achieved with bipolar LO-switching transistors and with a sufficient gain in the front-end. The contribution of the flicker noise to the total NF is almost negligible, even in GSM mode. The measured NF in GSM mode, when integrated from 200 Hz to 100 kHz, increases only by 0.2 dB compared to the case where only white noise is present. In WCDMA, the flicker noise is insignificant.

Several samples were measured in order to achieve better reliability in the measurement results. Altough the noise, gain, and third-order linearity performance remain almost equal from sample to sample, some variations in the second-order characteristics can be found. This obviously indicates a dependence on the circuit balance, i.e. device mismatch and layout symmetry. However, the worst IIP2 values, regardless of the mode, were found to be +32 dBm, while the highest were above +45 dBm. Figure 6.34 illustrates the linearity of the front-end in WCDMA mode at the maximum gain. The effects of the supply voltage on voltage gain, IIP2, and IIP3 are illustrated in Figure 6.35 and Figure 6.36 for GSM and WCDMA, respectively. To get some perspective of the front-end blocking performance, several tests with a large blocker were applied in both modes. The gain of the small desired signal is compressed by 1 dB with a blocker of -32 dBm at 600/1600/3000-kHz offset and -27 dBm at 10/15-MHz offset from the desired signal in GSM and WCDMA modes, respectively. A comparison of the results with the specifications reveals that the 3-MHz in-band GSM test blocker would probably fail. When comparing the results to specifications, it should be noted that the measurements do not include the preselection filter. The passband loss of the pre-select filter must be added to the results and the test should be performed with modulated signals.

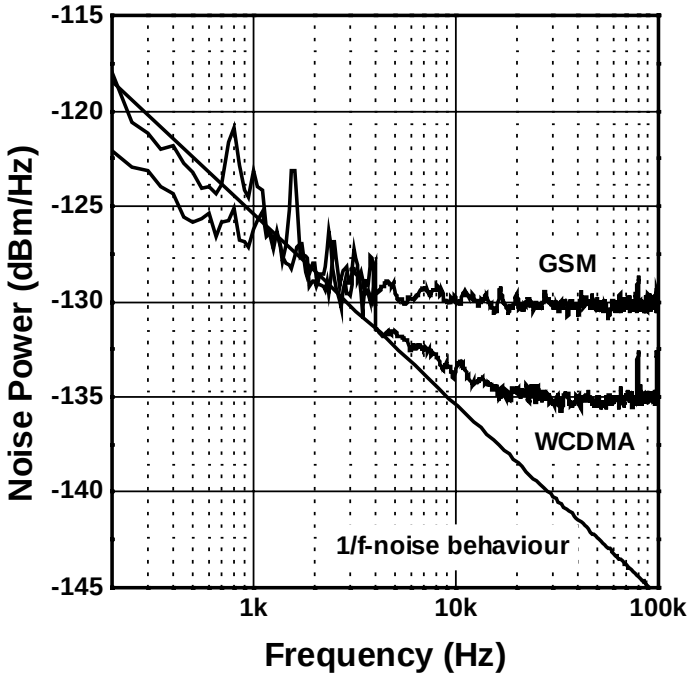

Figure 6.33. Output noise power at WCDMA and GSM maximum gain settings.

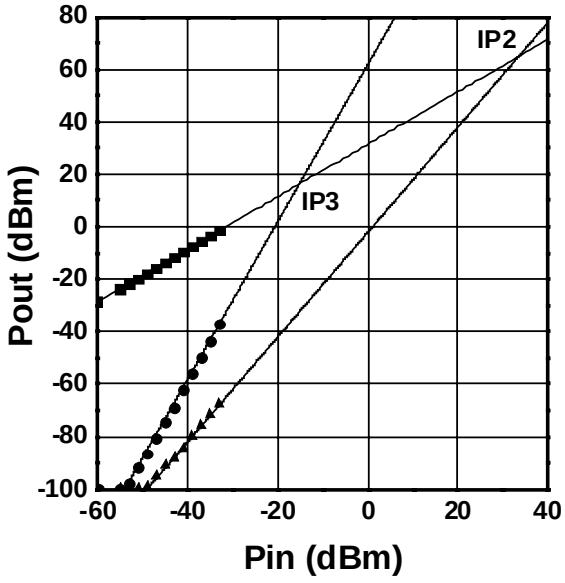

Figure 6.34. Linearity of the RF front-end in WCDMA maximum gain mode.

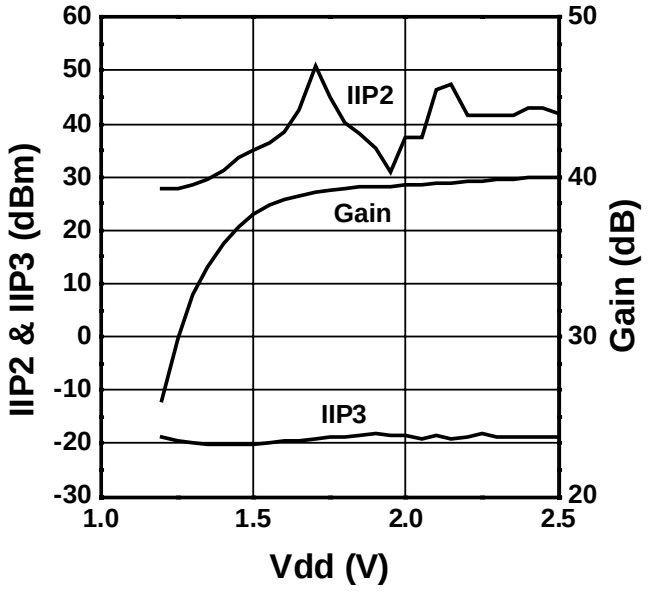

Figure 6.35. Voltage gain, IIP2, and IIP3 as a function of the supply voltage in GSM mode.

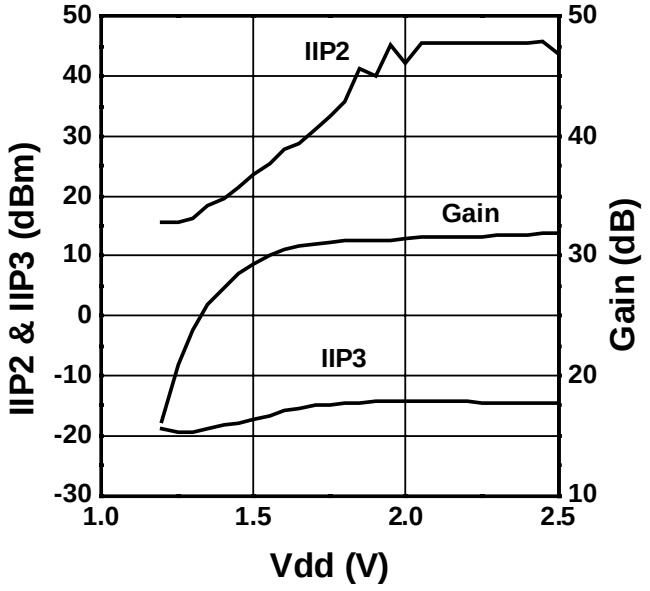

Figure 6.36. Voltage gain, IIP2, and IIP3 as a function of the supply voltage in WCDMA mode.

A large input signal from the unselected system can also desensitize the reception. This can happen when the signal from the other system is mixed with the spurious and harmonic tones of the operating standard. This can cause problems, particularly if the front-end has a single input for both standards, i.e., if there were a dual-band pre-selection filter. A situation in which the two standards selected can desensitize the front-end is illustrated in Figure 6.37. It is assumed that the handset is operating in GSM mode. It is connected to the highest GSM band and receiving at a frequency of 959.9 MHz. Simultaneously, there is a nearby mobile station connected to the lowest WCDMA band, transmitting at the 1922.5 MHz center frequency. This channel can be strong and mix with the second harmonic of the LO signal, causing an unwanted harmonic in the reception band, thus desensitizing signal reception. The out-of-band blocker can be as high as 0 dBm, according to the GSM specifications [18]. No effect on the desired GSM signal was measured with a –15 dBm input blocking signal. Thus, if the out-of-band attenuation of the WCDMA pre-selection filter in the reception band of the mobile station is 30 dB the front-end would tolerate a blocker of more than +15 dBm. Hence, the problem is insignificant in this case.

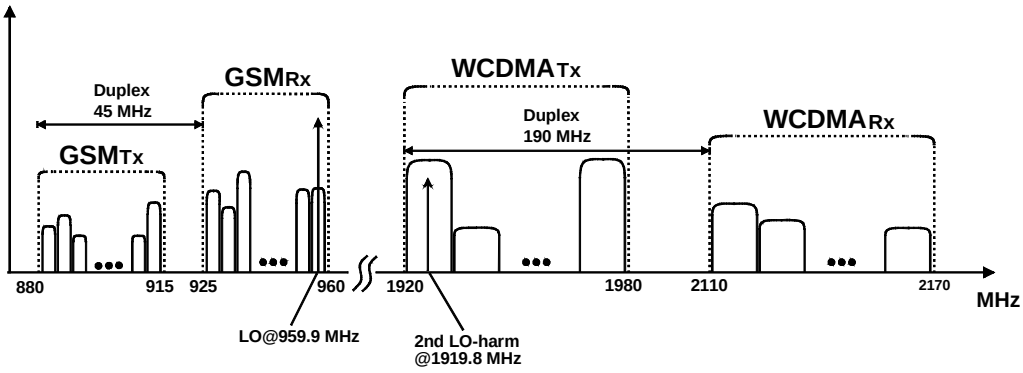

Figure 6.37. Frequency bands of GSM and WCDMA, showing possible mixing between the two bands.

6.4 Multi-mode receiver for GSM900, DCS1800, PCS1900, and WCDMA

A single-chip, multi-mode receiver for GSM900, DCS1800, PCS1900, and UTRA/FDD WCDMA is introduced in this section. Hence, the receiver operates at four different RF frequencies and with two different baseband bandwidths. The chip presented, which consists of a low-noise amplifier, downconversion mixers with on-chip LO I/Q generation, channel-select filters, and programmable-gain amplifiers, uses a direct-conversion architecture. Altough there are four reception bands, only four on-chip inductors are used in the single-ended low-noise amplifier. The repeatable receiver IIP2, with over +42dBm, is achieved with mixer linearization circuitry together with baseband circuitry having approximately +100-dBV out-of-band IIP2. The NF of the SiGe BiCMOS receiver is less than 4.8dB in all GSM modes, and 3.5dB in WCDMA. The power consumption from a 2.7-V supply in all GSM modes and in WCDMA mode is 42mW and 50mW, respectively. The silicon area is 9.8mm^2, including the bonding pads.

The direct conversion receiver (DCR), shown in Figure 6.38, is designed according to the UTRA/FDD WCDMA, GSM900, DCS1800, and PCS1900 system specifications [24], [18]. Each of the four systems in this receiver can be activated by means of externally-supplied

digital control. Thus, no hardware modifications, such as changes in the PCB, are required. The aim was to share as many receiver building blocks as possible without degrading the performance compared to single-system receivers. In addition, the multi-band interface between the LNA and mixers is designed to avoid buffering and single-ended-to-differential converters, which would increase power consumption [8]. If this multi-mode receiver is compared to the earlier single-system DCR described in Section 6.2, it has a comparable performance with only a 20% increment in the chip area, excluding the A/D converters. The increase in the chip area is mainly because of channel-select filters, which require large on-chip RC time constants in GSM mode. Furthermore, this receiver provides solutions for the well-known IIP2 problem of DCR in both the RF and baseband circuits.

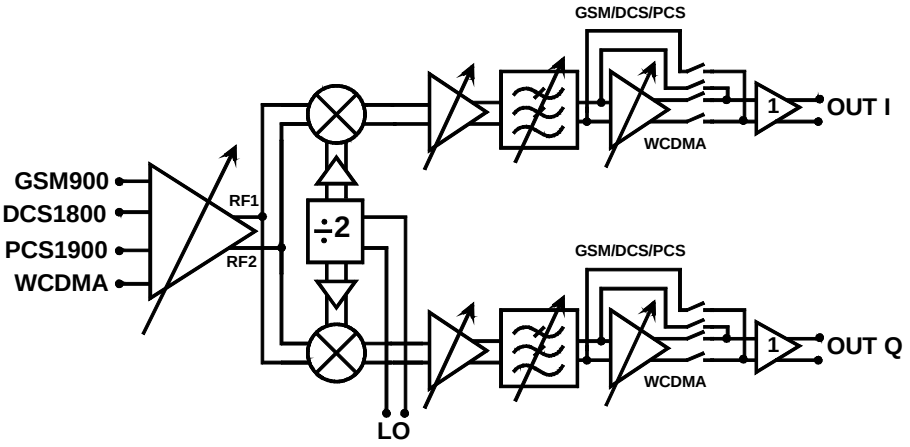

Figure 6.38. Block diagram of the receiver.

6.4.1 LNA

The LNA shown in Figure 6.39 uses single-ended topology to reduce the number of on-chip inductors and eliminates the need for an off-chip balun, unlike in balanced structures. In addition, the single-ended topology has lower power consumption compared to balanced structures [23]. However, the single-ended structure is more sensitive to substrate noise and other on-chip interferes. To decrease this effect, the LNA was placed as far away from the interfering blocks as possible. This design also benefits from the highly-resistive BiCMOS substrate. Depending on the mode selected, one of the four inputs is activated, while the other inputs are connected to ground, which reduces interference from the non-operational systems. Hence, all inputs can be separately matched and optimized. In high-gain mode, the active system uses one of the common-emitter transistors Q1-Q4 as an input transistor. Alternatively, to improve linearity at high signal levels, the LNA gain can be lowered by approximately 30dB, using a resistively-degenerated common-base stage, shown in Figure 6.40(a) [12]. The biasing arrangement of the four input transistors Q1-Q4 in GSM900 high-gain mode is shown in Figure 6.40(b). When the common-base stage is used in GSM900, the switch S9 is closed instead of S8 being closed, since S9 biases off the input transistor but does not steer the RF signal to ground. In addition to using the common-base configuration, the LNA gain can be controlled with the cascode transistor pairs Q51-Q72, which perform two 6-dB gain steps by steering part of the signal current to the non-operational output, as shown in Figure 6.39. Thus, in all modes, six gains can be selected in the LNA.

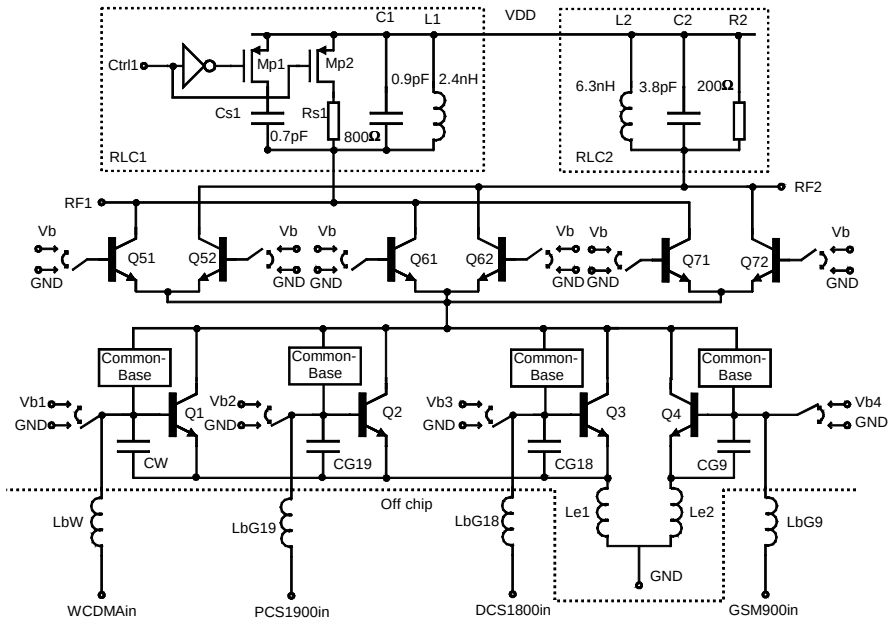

Figure 6.39. Multi-mode LNA. GSM900 mode at maximum gain is selected.

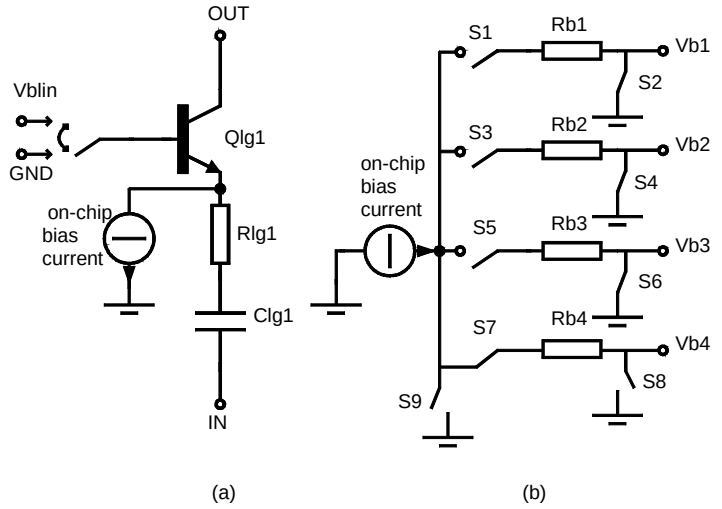

Figure 6.40. (a) One LNA common-base stage. (b) LNA input transistor biasing (in GSM900 high gain mode).

In WCDMA, PCS1900, and DCS1800 modes, the LNA uses the resonator RLC1 as the load and RF1 as the signal output. In GSM900 mode, RLC2 and RF2 operate as the load and signal outputs, respectively. The resonance frequency for RLC1 can be lowered for DCS1800 and PCS1900 systems by adding a capacitor, Cs1, with switch Mp1. In addition, the switch Mp2 is

opened, which compensates for the Q-value reduction caused by Mp1 and increases the LNA gain to an acceptable level. Altogether, only four on-chip inductors were used, which was made possible by sharing the matching and load inductors in the WCDMA, PCS1900, and DCS1800 systems. Thus, four on-chip inductors can be removed, compared to a multi-band receiver with parallel LNAs [25], [26]. The two single-ended LNA outputs (RF1, RF2) are capacitively ac-coupled to the mixer inputs in order to filter out the low-frequency second-order distortion generated in the LNA [27]. All LNA components except the input bond wires are on-chip, including switches, biases, and a current reference. The simulated LNA performance is shown in Table 6.5 and the power consumption in all modes is 8.6mW, including the biases and reference.

Table 6.5. Simulated LNA performance at maximum gain.

		GSM900	DCS1800	PCS1900	WCDMA
Voltage Gain	[dB]	24.6	26.0	26.2	26.2
NF	[dB]	1.4	1.9	1.9	2.0
IIP3	[dBm]	-15.8	-13.7	-13.4	-12.9
S11	[dB]	-23	-16	-18.8	-19

6.4.2 Downconversion mixer

The double-balanced mixer, which is driven by the single-ended LNA, is shown in Figure 6.41. The LNA and mixer share two separate interfaces, the LNA outputs RF1 and RF2, one of which can be selected at a time. The other mixer input branch is always shunted to chip ground while in the off state. Thus, when the LNA gain is decreased by steering part of the signal current to the non-operational resonator, it is shunted to ground in the mixer input. By way of illustration, if the mixer uses RF1 as its input, the transconductor M1 is biased on while the gate of the transconductor M2 is connected to ground. An additional current Iboost is fed to the drain of the transconductor M1. The cascode device Qc1 is biased on while the base of the cascode transistor Qc2 is shunted to ground and isolated from the biasing node Vbc. In addition to band-selection, the cascode transistors are used to improve the LO-to-RF isolation. According to simulations, the mixer reverse isolation is improved by over 11dB when the cascodes are used. The current consumption is reduced in the single-endedly driven double-balanced mixer since current injection is not used to boost the shunted transconductor M3. The injection current is about 70% of the total bias current through the transconductor M1/M2. The W/L ratios of the transconductors M1/M2 and M3 are equally scaled according to their bias currents.

A technique to reduce the even-order distortion is used in the mixer. The IIP2 characteristics are improved by inserting a controllable additional resistive load in parallel with the positive and negative load resistors. Thus, a controllable mismatch linearizes the mixer with respect to the even-order distortion, with negligible effect on the other essential performance parameters, such as noise, gain, and IIP3. The additional load consists of binary-weighted large resistor fingers with a 5-bit control. The adjustment has a ±10% tuning range. Both the I and Q channels are adjusted separately, because they exhibit different asymmetry performance. Figure 6.42 illustrates the IIP2 of several samples as a function of the trimming range. The improved receiver IIP2 is at least +42dBm in each characterized sample. This means an IIP2 of approximately +65-dBm referred to the input of the downconversion mixers. The minimum dc offset at the mixer output does not necessarily indicate the best IIP2 characteristics, as shown in

[28]. Therefore, in certain cases the arrangement used increases the dc offset in the mixer output, as the second-order intermodulation rejection is improved. The mixer is followed by a baseband transconductor, which tolerates dc offsets without degrading the performance. In addition, dc offset is cancelled at the mixer output.

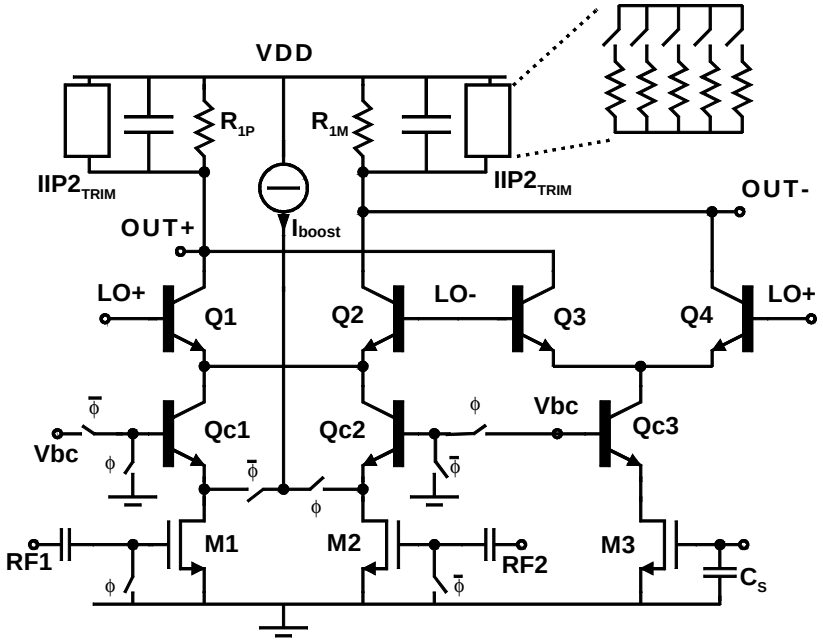

Figure 6.41. Downconversion mixer with IIP2 enhancement circuitry.

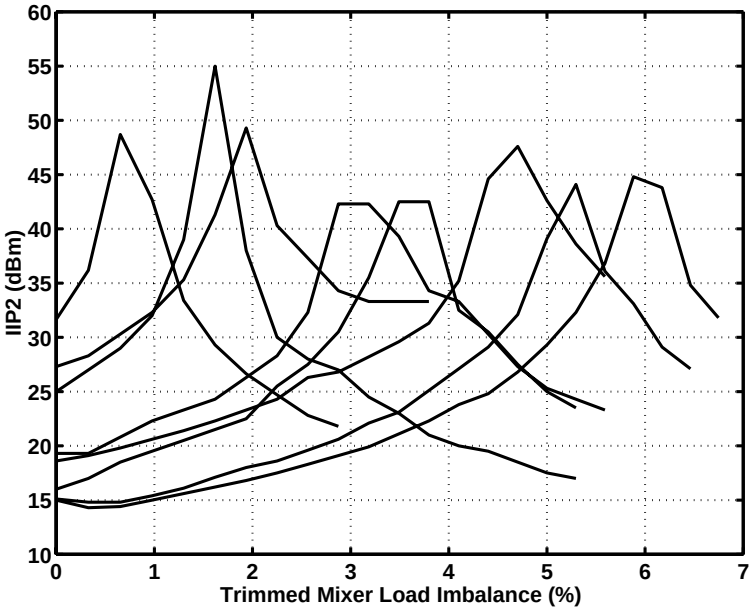

Figure 6.42. Receiver IIP2 of several samples.

Because of the RC pole at the mixer output, resistor tuning makes the IIP2 improvement frequency dependent in the baseband. Figure 6.43 illustrates the frequency dispersion along the downconverted channel once the mixer has been trimmed at a fixed downconversion test frequency. In GSM mode, the input-referred distortion component of the DCR of –125dBm between 40kHz and 100kHz corresponds to an IIP2 of +45dBm measured with –40-dBm input tones. In WCDMA mode, the –137-dBm IMD2 at 200kHz corresponds to an IIP2 of +57dBm with –40-dBm input tones at 10MHz and 10.2MHz. When the baseband is in GSM mode, the switches in parallel with resistors R2P and R2M, shown in Figure 6.44, are open. Since the resistors R2P and R2M are approximately 13 times larger than the mixer load resistors R1P and R1M, the effect of the mixer load trimming in the pole frequency is insignificant. In WCDMA mode, the switches are closed, and thus the trimming may considerably shift the pole frequency in the trimmed branch in the channel. This makes the trimming in WCDMA mode frequency-dependent. The shift in the pole frequency should be compensated capacitively in order to keep the pole frequencies in both branches equal. In addition, the problem could be mitigated by shifting the pole in WCDMA mode to a higher frequency. The shifting of the pole to higher frequencies would significantly increase the linearity requirements of the following stage and was therefore omitted.

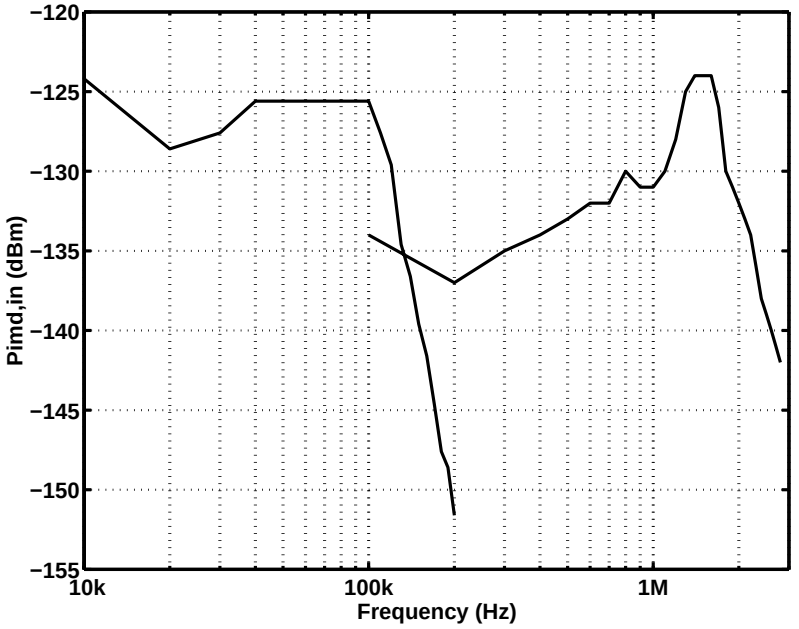

Figure 6.43. Sensitivity of trimmed IIP2 along the downconversion channel, in GSM and WCDMA modes. The measured input-referred IMD2 component is shown on the y-axis.

6.4.3 Analog baseband circuit

The analog baseband circuit consists of two similar channels that contain channel-select filtering and amplification with a programmable gain. The baseband circuit has two operation modes, one for WCDMA and the other for the different GSM systems. The channel-select filter is implemented with the opamp-RC technique. The RC structure at the mixer output, which forms the real pole of the odd-order prototype [29], is followed by a transconductor, Gm1 in

WCDMA and Gm2 in GSM mode, as shown in Figure 6.44. A fourth-order leapfrog filter common to both WCDMA and GSM follows the transconductor Gm1 or Gm2 [30].

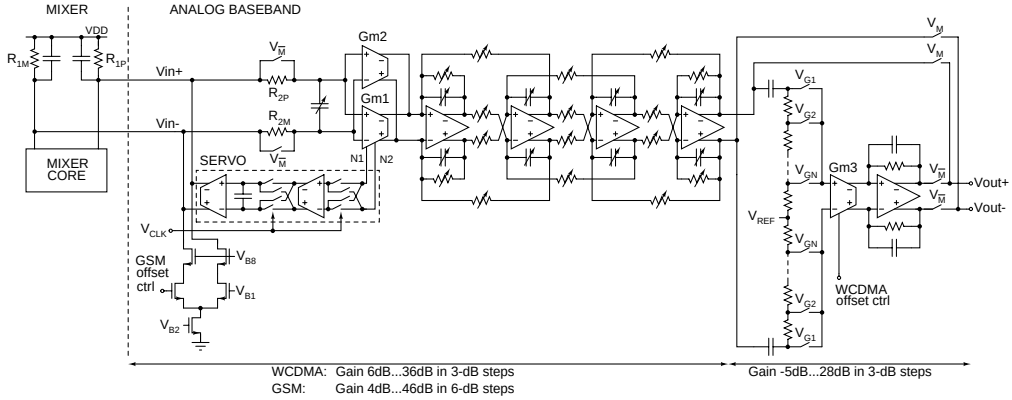

Figure 6.44. One signal channel of the analog baseband circuit (V_M is the mode select signal).

In GSM modes, the channel-select filter prototype is fifth-order Butterworth and in WCDMA fifth-order Chebyshev with 0.01-dB passband ripple [6]. The two complex conjugate pole pairs are implemented as a fourth-order leapfrog structure. All capacitor matrices in the leapfrog filter are identical. In WCDMA mode, the capacitor sizes are decreased to one third that of GSM mode and the remaining capacitors are used in the servo loop to push the –3-dB frequency of this highpass filter to lower frequencies.

In WCDMA mode, the baseband gain can be varied from 1dB to 64dB in 3-dB steps. The programmable gain is implemented with switched resistors in Gm1 and a programmable attenuator loss after the leapfrog structure [6]. On-chip offset removal in WCDMA mode consists of a servo with chopper stabilization and ac coupling. With on-chip passives the –3-dB frequencies of the servo feedback loop and ac coupling are 1kHz and 13kHz, respectively. The offset at the baseband output changes slowly as a result of aging and variations in the temperature and supply voltage. Therefore, the static offset voltage at the baseband output is cancelled with an off-chip control in the transconductor Gm3.

The analog baseband block is designed to drive 8-bit ADCs in both modes. The dynamic range of 8-bit ADCs with a sample rate of approximately 1MS/s is higher than required to detect data in GSM systems, since channel selection filtering precedes the ADC. Therefore, the additional dynamic range decreases the required maximum gain and programmable gain range in GSM mode, compared to WCDMA. A maximum DCR voltage gain of about 80dB is sufficient in GSM mode. In GSM mode, the baseband gain can be varied from 4dB to 46dB in 6-dB steps. The programmable gain is mostly realized in Gm2 and two steps are implemented in the leapfrog filter using switched resistors, which is possible in TDMA systems which have idle time slots. The amplifier following the leapfrog filter is switched off in this mode. Because of the high maximum baseband gain the offset voltage at the baseband output is controlled at the mixer output with an additional NMOS differential pair with an off-chip control. Methods for the implementation of an automatic feedback for the compensation of DC offsets in burst mode systems are discussed, for example, in [33], [34].

6.4.4 Experimental results

The receiver was fabricated with a 0.35-μm 45-GHz f_T SiGe BiCMOS process and mounted directly on a PCB by wire bonding. The measured performance of the receiver is summarized in Table 6.6. The input matching with maximum LNA gain and in linear modes are illustrated in Figure 6.45 and Figure 6.46, respectively. The measured voltage gain at all LNA gain settings in GSM900 mode and WCDMA mode are shown in Figure 6.47 and Figure 6.48, respectively. The maximum voltage gain of the DCR in all modes is illustrated in Figure 6.49. The voltage gain drop at 2.2GHz is due to the limited operation bandwidth of the LO generation circuit. However, the operation band covers the upper WCDMA band in all the measured samples. The parasitic capacitances, together with the resistive loading, limit the usable frequency range of the divider at a constant bias current. The equivalent noise bandwidth of the DCR, which is used in the NF calculations, was derived from the measured frequency response of the analog channel-select filter. The DSB NF is 3.5dB in WCDMA and less than 4.8dB in all GSM modes. In all GSM modes, the baseband circuit produces approximately half of the noise generated in the receiver. In WCDMA mode, the RF front-end dominates the noise generated in the receiver. The noise spectrum at the receiver output in WCDMA and DCS1800 modes at maximum gain is illustrated in Figure 6.50. The chip area of the prototype receiver in Figure 6.51 is 9.8mm^2.

Table 6.6. Summarized performance of the receiver.

		GSM	DCS1800	PCS1900	WCDMA
Supply voltage	[V]	2.7			
Power consumption*	[mW]	42			50
Voltage gain	[dB]	0…82	-6…79	-4…79	-6...99
Baseband gain step	[dB]	6			3
NF (DSB)	[dB]	3.8	4.6	4.8	3.5
IIP3	[dBm]	-20	-21	-21	-21
Calibrated IIP2	[dBm]	+42	+42	+42	+47
IIP2 without calibration	[dBm]	+14	+16	+18	+18
-1dB compression	[dBm]	-35	-34	-34	-34
I/Q gain imbalance	[dB]	0.4	0.7	0.8	0.5
LO@ RF input	[dBm]	-88	-92	-96	-98
S11	[dB]	-13	-10	-11	-14

* Excluding measurement buffers

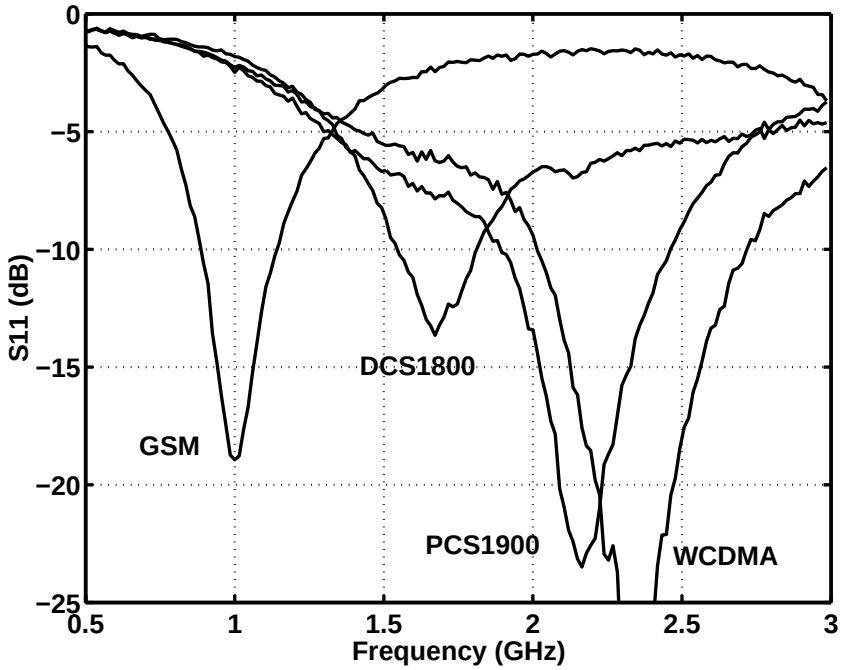

Figure 6.45. Input matching of the LNA in all four different modes. LNA gain at maximum.

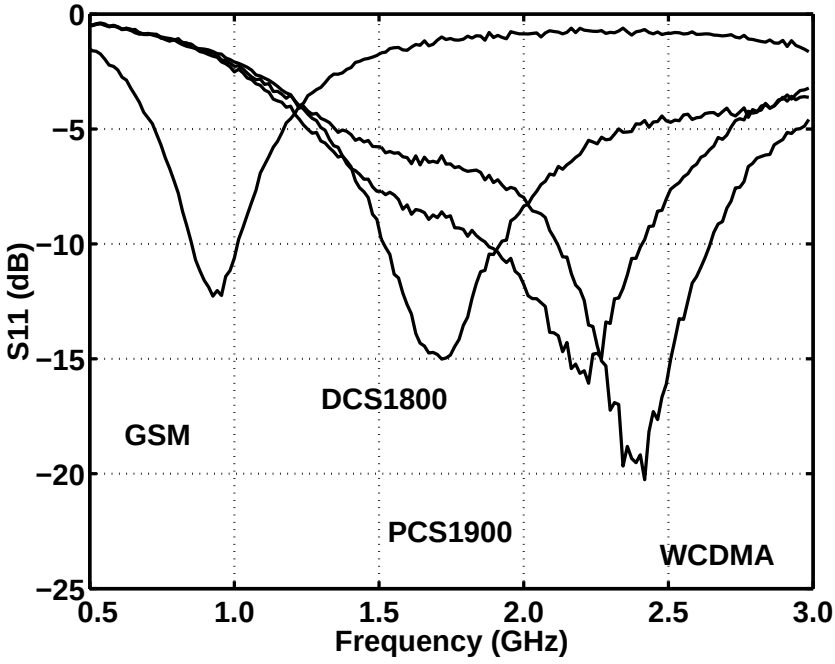

Figure 6.46. Input matching of the LNA in all four different modes. LNA is using resistively-degenerated stage.

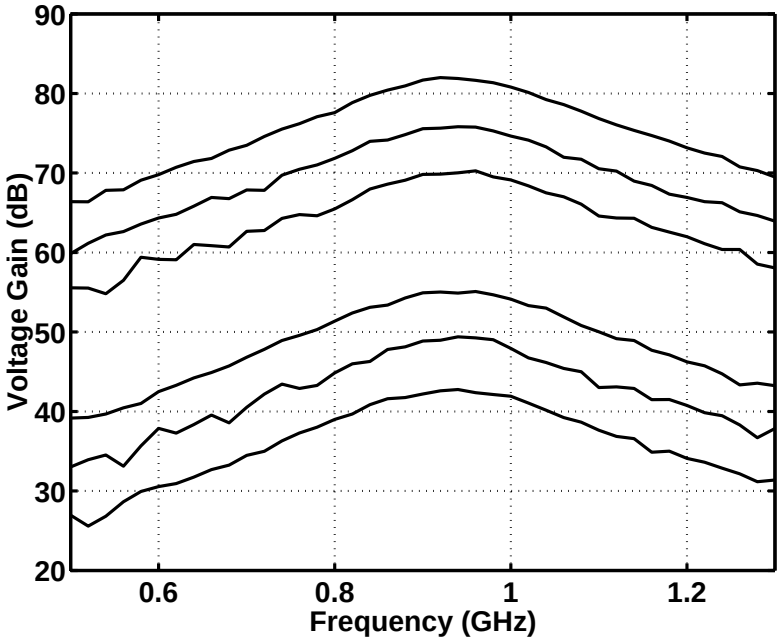

Figure 6.47. Measured DCR voltage gain at GSM900 mode at all LNA gain settings.

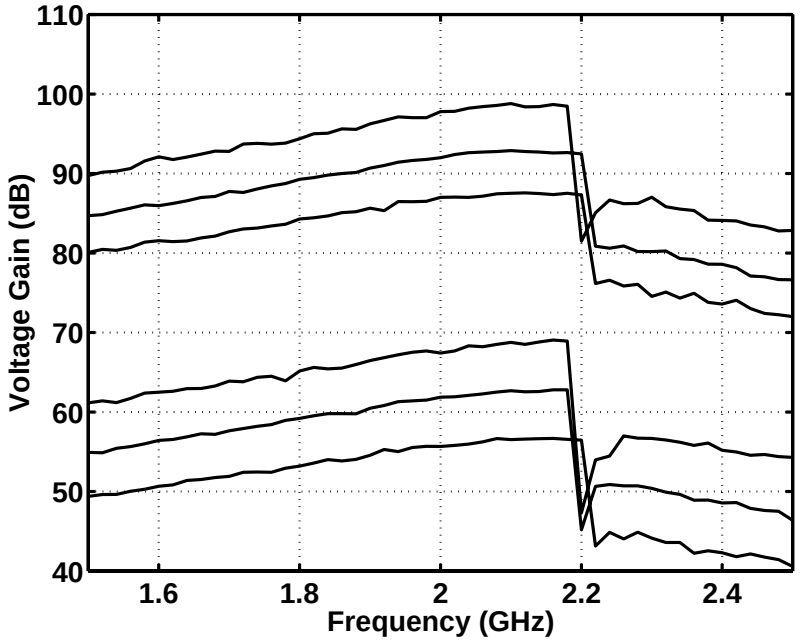

Figure 6.48. Measured DCR voltage gain at WCDMA mode at all LNA gain settings.

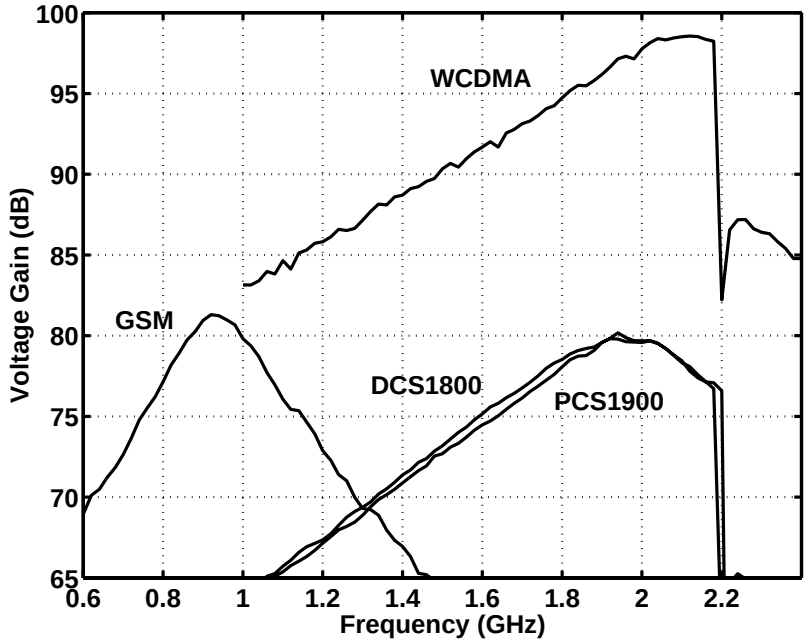

Figure 6.49. Measured maximum DCR voltage gain in all four modes.

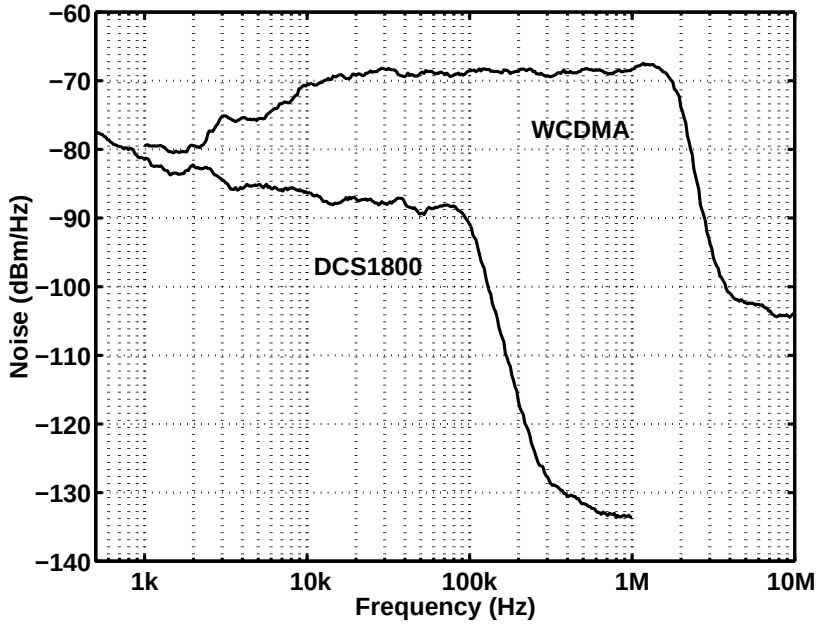

Figure 6.50. Noise spectrum in WCDMA and DCS1800 modes.

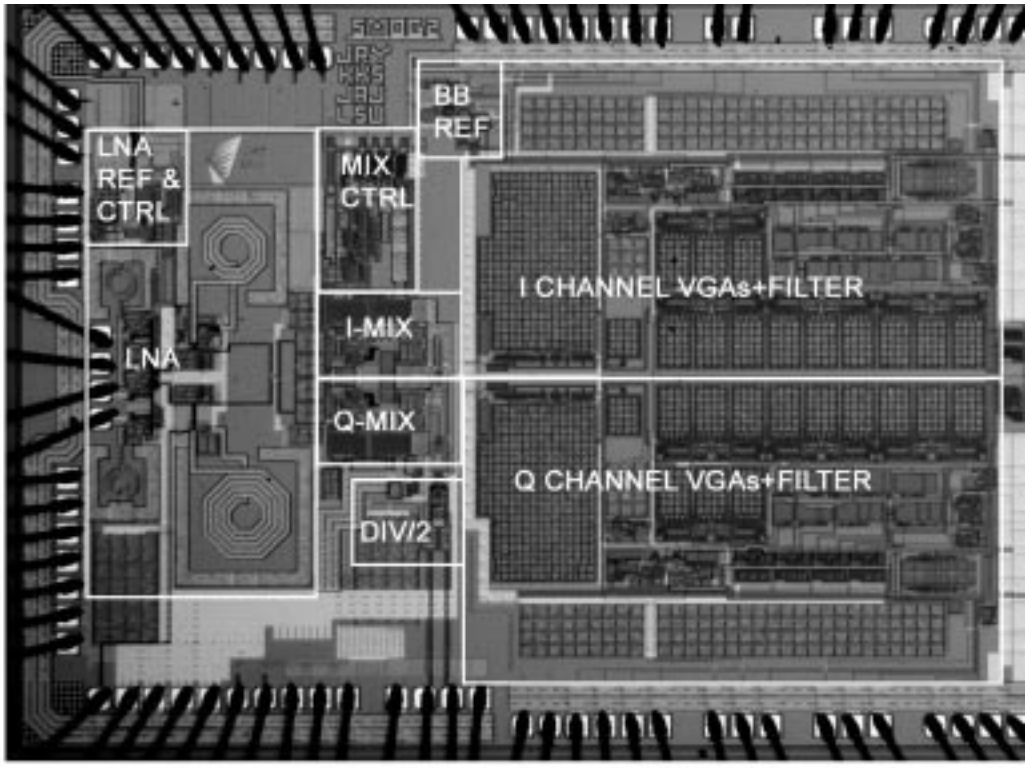

Figure 6.51. Chip microphotograph.

In WCDMA mode, the compression of a small in-band signal is defined using a downconverted 15-MHz blocker, and the IIP3 and IIP2 are measured with 10-MHz & 20.2-MHz and 10-MHz & 10.2-MHz downconverted signals, respectively. In all GSM modes, compression is defined using a downconverted 0.6/1.6/3.0-MHz blocker, and the IIP3 and IIP2 are measured with 800-kHz & 1.6-MHz and 800-kHz & 820-kHz downconverted signals, respectively. In all modes, the RF front-end limits receiver linearity. The IIP3 was slightly lower than expected and is limited by the mixer, probably because the mixer biasing had shifted considerably from the simulated values. The receiver IIP3 depends on the pre-select filter passband loss and increases by the amount of the pre-select filter loss compared to the receiver IIP3 at the LNA input, even though the pre-select filter does not decrease the power of the in-band blockers, compared to the desired signal. However, the GSM/DCS1800/PCS1900 intermodulation test and tolerance test against a high blocker probably fail as a result of the low IIP3.

The measured power consumption of the analog baseband circuit including two channels without output buffers in GSM and WCDMA modes, is 3.9mW and 12.7mW, respectively. The two output buffers, which are used for measurement purposes at the baseband output, consume altogether 3.7mW in both modes since they are over-designed so as to provide a sufficient bandwidth in the measurements. The measured frequency responses of the channel selection filter in GSM and WCDMA modes with the maximum DCR gains are shown in Figure 6.52. Both responses are a combination of separate curves. A test signal with higher power was used in the stopband to expand the dynamic range of this measurement. The peaks in the WCDMA response at frequencies higher than 40MHz are the harmonics of the clock signal used to chop the servo amplifier.

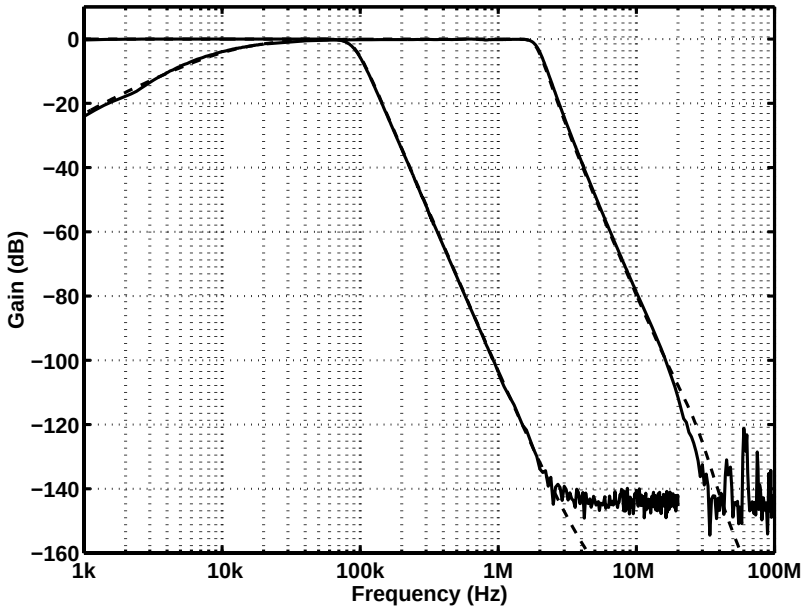

Figure 6.52. Measured and simulated nominal (dashed line) frequency responses of channel-select filter in GSM and WCDMA modes.

In multi-band receivers, the interference from a non-operational system can corrupt the reception. Large interference at the input of a non-operational system and its harmonics can compress the small desired signal, as in the blocking test. Furthermore, in multi-system receivers, the mixing product of an unwanted signal may lie directly in the passband of the channel-select filter. Thus, it may considerably decrease the signal-to-noise ratio. In this receiver, the two additional bands increase the number of possible interferers already discussed in Section 6.3. The most challenging systems are GSM900 and DCS1800, since the second harmonic in the GSM900 reception band maps directly on to the DCS1800 reception band. Hence, these signals are not suppressed by the pre-select filter, as in the RF front-end described in the previous section. In order to discover the receiver performance in these two systems, two different measurements were applied. In the first case, the receiver operated in GSM900 mode, and the interference was injected to the non-operational DCS1800 input. The desired signal was mixed down to 20kHz. The DCS1800 interfering input signal mixes down with the second LO harmonic or the off-chip double frequency LO. In the measurements, the DCS1800 signal was selected to produce a 12-kHz interferer. No gain compression of the wanted signal was observed. Furthermore, the interference at the output at 12kHz was 16dB below the wanted signal when +3-dBm and –99-dBm input powers were applied to DCS1800 and GSM900 inputs, respectively. Hence, the receiver should operate properly in this mode. In the second measurement, the receiver operated in DCS1800 mode, and the interference was injected to the non-operational GSM900 input. The desired signal was again placed at 20kHz after downconversion. In this case, the second harmonic of the GSM900 signal was mixed with the fundamental LO. The desired signal compressed 1dB when a –6-dBm interference was injected to the GSM900 input. Hence, the gain compression is not a problem. However, with an input power of –99dBm at the DCS1800 input, the desired signal is 1.2dB higher than the interfering passband signal with –23-dBm power at the non-operational GSM900 input. Thus, this effect corrupts reception as a result of a low signal-to-noise ratio. The GSM900 signal probably leaks to the DCS1800 input already at PCB where the two inputs are located close to each other. The second harmonic of the GSM900 signal is then generated in the LNA or mixer. Therefore, in order to ensure proper reception, additional separation between these two systems is required.

Hence, switched structures in the pre-select filters or antennas may be required to achieve sufficient performance.

6.5 Conclusions to experimental circuits

In Sections 6.1 and 6.2, circuits, which are intended for a single-system WCDMA direct-conversion receiver were presented. The RF front-end in Section 6.1 was a part of the first WCDMA receiver published. The first version of the RF front-end was implemented on a separate chip and the second version was on the same chip as the baseband circuit and A/D converters. The LNA in these circuits is a standard inductively-degenerated LNA without any gain control. In Section 6.2, a low-noise, low-power single-chip direct-conversion receiver for the UTRA/FDD WCDMA cellular system was described. A low current consumption of 22 mA was achieved in a wide-band system, although the receiver includes on-chip ADC's. Compared to the receiver in [4], the problems related to clock feedthrough are mitigated. In this design degradation of sensitivity of less than 0.1-dB is observed in the worst case, although the total NF is only 3.0 dB. The low NF verifies the appropriacy of the partitioning and shows that the noise from the baseband can be almost negligible, even in direct-conversion architecture, together with sufficient linearity and low power. In this receiver, the LNA had a low gain mode, which was implemented by using a separate signal path. However, this design had a problem with RF gain transients, which was analyzed in Chapter 5. Thus, the gain can be changed only at high input signal levels without significant transients.

In Sections 6.3 and 6.4, circuits which are targeted for multi-mode DCRs were described. The RF front-end in Section 6.3 is applicable to WCDMA and GSM direct-conversion receivers. With the exception of the LNA input transistors and matching inductors, all on-chip devices are utilized in both modes. An on-chip active balun permits the use of a single-ended RF input and double-balanced mixers. The balun provides a single-ended-to-differential conversion over the large frequency range required in multi-band receiver with high linearity and acceptable noise levels. The converter uses a common-emitter and common-collector structure with a dummy transistor and separate supply pads to guarantee symmetrical output loads. Current boosting in quadrature mixers makes possible low-voltage operation with sufficient gain, linearity, and noise. The power consumption of the RF front-end from a single 1.8 V supply is 22.5 mW. The 27-dB gain control range is divided between the LNA and the mixers.

In Section 6.4, a low-power, low-noise, single-chip radio receiver for the GSM900, DCS1800, PCS1900, and UTRA/FDD WCDMA systems was introduced. This is the first published multi-mode DCR operating in four different reception bands and two different channel bandwidths. Off-chip components were not used in the signal path of this DCR, excluding the input bond wires. Component sharing was optimized by taking into account the need to minimize the silicon area and power consumption and to avoid performance degradation compared to corresponding single-system receivers. For example, only four on-chip inductors are used in the LNA. The IIP2 of the receiver can be improved repeatedly to over +42dBm by controlling the mismatching of the mixer load resistors. The analog baseband circuit achieves approximately +100-dBV out-of-band IIP2, which does not limit receiver performance. The problems related to gain changes in discrete steps at RF in a DCR were significantly reduced. This problem and the results were analyzed in Chapter 5.

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7 Conclusions

During the last few years the design driver has shifted towards fast data applications instead of speech. In addition, the different systems may have a limited coverage, for example, limited to urban areas only. Thus, the receiver should be able to use different systems depending on the required solution or location of the receiver. This thesis concentrates on the design and implementation of single-chip LNAs for this type of DCRs. The focus has been on implementing programmable gain and multi-band operation with an inductively-degenerated LNA.

In the first part of this thesis, the requirements for the LNA were described. The analog receiver specifications were estimated from system specifications, and the LNA requirements were derived from these figures of merit. The different receiver architectures were briefly described and the rationale for the use of direct-conversion architecture was given. In addition, issues related to multi-system receivers were addressed and differences from single-system receivers were described. After the system level design of the LNA was described, the design of a single-system inductively-degenerated LNA was described in detail. The different elements and their limitations were described and analyzed. In addition, different types of LNAs were compared to an inductively-degenerated cascode LNA in order to justify why this topology was selected as the basis for all the experimental circuits. Since the focus is on DCR design, issues connected with the LNA mixer interface were also given and analyzed.

One of the most essential parts of this thesis is the provision of circuit solutions in the design of a multi-mode LNA. These circuit solutions were developed to share some of the devices already in the LNA in order to reduce the chip area compared to the traditional approach, which uses parallel structures. The usability of these circuits depends on the receiver architecture and the systems chosen for the receiver. The circuits in this thesis were developed for a multi-mode receiver, where only one system is activated at a time. In addition, several methods for the implementation of a programmable gain in the LNA were described and analyzed. Issues related to gain control transients in DCRs operating in continuous time systems, such as WCDMA, were also described and analyzed.

The experimental circuits demonstrate the usability of the circuit structures discussed. The first two experimental ICs demonstrate that an inductively-degenerated LNA can be used in a single-system WCDMA receiver. In the second WCDMA receiver the A/D converter is implemented on the same chip, without LNA performance being significantly degraded. In the last two experimental circuits, the use of the inductively-degenerated LNA in a multi-system receiver is demonstrated. To the author's knowledge, this last multi-mode receiver is the first published complete multi-mode DCR which includes four different reception bands and two different channel bandwidths. The results show clearly that this type of LNA is feasible in a multi-system environment. In addition, the experimental circuits demonstrate that although four different systems are implemented on the single chip, the chip area does not increase linearly as the number of systems increases, and the performance of the individual systems is not significantly degraded compared to a single-system receiver.

Only a few publications exist which analyze or implement circuits which are particularly designed for multi-mode receivers. However, the need in the future for receivers of this type is evident and therefore research must be conducted in this field. This thesis introduces new circuit solutions for multi-mode receivers, concentrating on the multi-mode LNA. The development of future systems and technologies will define the usability of and need for these specific circuit solutions.

Appendix 1: Table of recently published LNAs

Ref	f_{RF} [GHz]	Gain [dB]	NF [dB]	IIP3 [dBm]	Pd [mW]	Vdd [V]	Idd [mA]	# of stages	Bias on-chip
[1]	2	21	1.85	-9	na	2.8	na	1	na
[2]	5.75	14.2	0.9	0.9	16	1	16	1	no
[2]	5.75	14.1	1.8	4.2	21.6	1.8	12	1	no
[3]	2.1	12	2.8	4	15	3	5	1	na
[4]	2	14.5	1.6	5	24.8	2.85	8.702	1	no
[5]	0.88	16.3	1.5	12.2	23.1	3	7.7	1	yes*
[6]	8	13.5	3.2	na	22.4	1	22.4	1-2	no
[7]	2	14	1.6	-4.5	30	3	10	1	na
[7]	5	14.3	3.2	-2	39	3	13	1	na
[8]	2.14	25.2	2.3	-13.1	na *	na	12.2	2	yes
[9]	5	17	2.3	-7	13	3.3	3.939	1	yes
[10]	5.8	7.2	3.2	6.7	20	1.3	15.38	2	no
[11]	2.4	12	3.2	-5	7	1.75	4	1	na
[12]	1.9	21	1.5	-5	na	2.6	na	1	na
[13]	2.14	14.9	1.6	9.1	23.1	3	7.7	1	yes*
[14]	1.57	16.5	1.3	-5	9	1.5	6	1	na
[15]	2.46	14	2.36	-2.2	4.65	1.5	3.1	1	yes
[16]	5.2	19.3	2.45	-6.1	26.4	3.3	8	1	na
[17]	1.9	12.5	1	8	na*	na	5	na	na
[18]	1.9	15.5	1.8	3	na*	na	7	1	na
[19]	0.9	20	4.2	-2	na	2.1	na	1	na
[20]	0.9	15.3	1.4	1.6	16.52	2.8	5.9	1	yes
[21]	2	14.8	2	0.2	na*	na	6.2	1	yes
[22]	1.95	15	1.4	2	36	3	12	1	yes
[23]	2.4	14.9	1.8	-14	5.1	3	1.7	2	yes
[24]	2.1	13	1.65	3	14.58	2.7	5.4	1	yes
[25]	2.4	8.9	3.2	-5.5	3.87	1.8	2.15	1	yes
[26]	2.45	15.1	2.88	2.2	na	na	8.1	1	yes
[26]	2.45	15.9	2.86	-2.6	na	na	7	1	yes
[27]	0.9	15.5	2.8	18	45	3	15	1	na
[28]	2	12.5	3.1	na	5.5	1	5.5	1	na
[29]	1.2	20	0.79	-10.8	9	1.5	6	1	na
[30]	1.8	11.3	1.9	3.7	32.1	3	10.7	1	yes
[31]	1.8	17	1.3	-2	12.15	2.7	4.5	1	na
[32]	1.96	15.3	1.9	7.6	17.55	2.7	6.5	2	yes
[33]	1.9	15	1.5	-4.5	13.5	2.7	5	1	yes
[34]	0.9	16.5	1.05	0	27	2.7	10	1	yes
[35]	2.4	19	2.4	1.5	26.4	3.3	8	1	no
[36]	0.9	10	1.75	3	na	na	10	1	yes
[37]	0.9	22	2	-3	21.6	2.7	8	2	yes
[38]	5.25	15.5	4.5	5.6	10	2.5	4	1	na
[39]	5.2	11	2.17	0.3	10	2	5	1	na

Other blocks on-chip	offchip lin	Differential	Topology	Technology	Ref
yes	no	no	CE+cas	SiGe BiCMOS	[1]
no	no	yes	CE	0.18um CMOS	[2]
no	no	yes	CE+cas	0.18um CMOS	[2]
yes*	no	no	CE+cas	0.25um CMOS	[3]
yes	no	no	CE+FB	0.25 SiGe BiCMOS	[4]
yes*	yes	no	CE	0.5 SiGe BiCMOS	[5]
no	no	no	folded CE	0.18um CMOS	[6]
no	no	yes	CE+cas+FB	0.25 SiGe BiCMOS	[7]
no	no	yes	CE+cas+FB	0.25 SiGe BiCMOS	[7]
yes*	no	no	CE	0.5 SiGe HBT	[8]
no	no	no	CE+cas	0.35 SiGe BiCMOS	[9]
no	yes	no	CS+CS	0.35 um CMOS	[10]
yes	no	yes	CE+resfb	0.18um CMOS	[11]
yes	no	yes	CE+cas	SiGe BiCMOS	[12]
yes	yes	no	CE	0.5 SiGe BiCMOS	[13]
no	no	no	CS+cas	0.25um CMOS	[14]
no	no	no	CS+cas	0.15um CMOS	[15]
no	no	no	CS+2cas	0.35 um CMOS	[16]
yes	no	no	na	0.4um PHEMT	[17]
yes	yes	no	CE	BiCMOS	[18]
yes	no	yes	CG	0.25um CMOS	[19]
no	yes	no	CE+cas+FB	0.25 SiGe BiCMOS	[20]
no	no	no	CE	SiGe	[21]
no	no	no	CE	InGaP HBT	[22]
no	no	no	CS+CD+FB	0.5um PHEMT	[23]
no	no	no	CE+cas+FB	0.35 SiGe BiCMOS	[24]
no	no	yes	CS+cas	0.18um CMOS	[25]
no	no	no	CS +cas	0.25um CMOS	[26]
no	no	no	CE+cas	SiGe BiCMOS	[26]
no	no	yes	CS+cas	0.35 um CMOS	[27]
yes	no	no	CS+cas	.2 um CMOS/SIMOX	[28]
no	no	no	CS+cas	na	[29]
yes	no	no	CE	0.25um BiCMOS	[30]
yes	no	no	CE+cas	30GHz SiGe	[31]
no	yes	no	CE+CE	SiGe	[32]
no	no	no	CE+cas	75GHz SIGe	[33]
no	yes	no	CS+cas	0.35 SiGe BiCMOS	[34]
yes	no	no	CS+cas	0.6um CMOS	[35]
no	yes	no	CS+cas	0.35 BiCMOS	[36]
no	no	yes	CS complem	0.35 um CMOS	[37]
no	no	no	CS+cas	0.35 BiCMOS	[38]
no	no	no	CS+cas	0.25um CMOS	[39]

CE is common emitter
CS is common source
CG is common gase
FB is feedback
cas is cascode

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