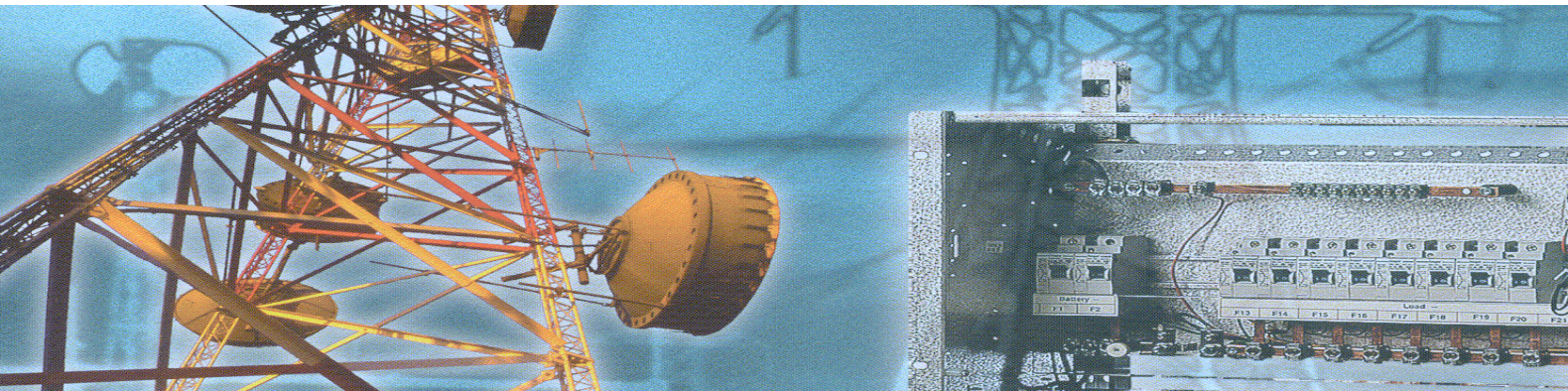


DESIGN OF ROBUST CONTROLLERS FOR TELECOM POWER SUPPLIES

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Abstract

A Telecom power supply is studied and analyzed from control system viewpoint. It consists of three stages: AC/DC rectifier, a backup battery, and a Telecom load. The AC/DC rectifier stage can be composed of paralleled DC/DC converters preceded by paralleled AC/DC converters. However, paralleled DC/DC converters are only considered in this thesis because they constitute the main dynamics in practice. A system of paralleled DC/DC converters operating in continuous inductor current mode with either voltage mode control or peak current mode control are modeled and analyzed using state-space representation. The \mathcal{H}_∞ control design is used in order to guarantee the robust stability and robust performance of the system in spite of different uncertainties. Also the \mathcal{H}_∞ loop-shaping design is used to design robust controllers in the presence of uncertainties. μ -analysis is used to evaluate the robustness of the system. Simulation results are presented to demonstrate the control design procedure and to compare between the two approaches presented.

A Telecom power system can be composed of voltage-loop and current-loop subsystems. The multi-input-multi-output proportional-integral-derivative (PID) controller is first designed achieving robust stability and robust performance of the voltage-loop. Then, the multi-input-multi-output proportional-integral (PI) controller for current-loop is designed to achieve robust stability and robust performance of the overall system. μ -analysis is used to evaluate the robustness of PID and PI controllers. Simulation results are also presented to demonstrate and validate the control design.

The required output characteristic of a Telecom power system contains three modes of operation: constant-voltage, modified constant-power, and constant-current modes. This nonlinear operation can be achieved by using the fuzzy-logic approach. A fuzzy PID-like controller is implemented to achieve the robust output voltage in spite of load disturbances. A fuzzy PI-like controller is implemented to ensure the overload protection reaching the optimal output characteristic of a Telecom power system. Also the internal-model control (IMC) method is applied to basic DC/DC converters: buck, boost, and buck-boost converters. IMC scheme is used to improve the dynamic performance of basic converters by achieving a robust output voltage against line and load disturbances. Simulations show good dynamic performance of the IMC controller.

Key Words

Telecom power supply, \mathcal{H}_∞ control, PID-control, fuzzy-logic control, internal-model control.

To my father, Abdulla, hope that he will find
a joy in this humble achievement.

Idris A. Gadoura

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“One crowded hour of glorious life is worth an age without a name”
Mordaunt, English Poet (1730-1809)

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Idris A. Gadoura

Espoo, Finland
01.04.2002

List of Publications

The text of this thesis is based on the following publications, which are referred to as P1, P2, P3, P4, P5, P6, P7, and P8 in the text.

- [P1] Gadoura, I., T. Suntio, and K. Zenger, “Robust Control Design for Paralleled DC/DC Converters With Current Sharing”, *Proc. of the 15th IFAC World Congress on Automatic Control*, July 21-26, 2002 in Barcelona, Spain, 6p, CD-ROM.
- [P2] Gadoura, I., T. Suntio, and K. Zenger, “Dynamic System Modeling and Analysis for Multiloop Operation of Paralleled DC/DC Converters”, *Proc. of the Int. Con. on Power Electronics and Intelligent Motion*, June 19-21, 2001 in Nuremberg, Germany, pp. 443-448.
- [P3] Gadoura, I., T. Suntio, and K. Zenger, “Model Uncertainty and Robust Control of Paralleled DC/DC Converters”, *Proc. of the IEE Int. Con. of Power Electronics, Machines, and Drives*, April 16-18, 2002 in Bath, UK, pp. 74-79.
- [P4] Gadoura, I., T. Suntio, and K. Zenger, “Practical Robust Control Design for Paralleled DC/DC Converters Using \mathcal{H}_∞ Loop-Shaping Techniques”, *Proc. of the Int. Con. on Power Electronics and Intelligent Motion*, May 14-16, 2002 in Nuremberg, Germany, pp. 335-340.
- [P5] Suntio T., I. Gadoura, J. Lempinen, and K. Zenger, “Practical Design Issues of Multi-loop Controller for a Telecom Rectifier”, *Proc. of the IEEE Int. Telecommunications Energy Special Conference*, May 07-10, 2000 in Dresden, Germany, pp. 197-201.
- [P6] Gadoura, I. and T. Suntio, “Implementation of Optimal Output Characteristic for a Telecom Power Supply: Fuzzy-logic Approach”, *International Journal of Control and Intelligent Systems*, 2002. (*In press*)
- [P7] Gadoura, I., T. Suntio, K. Zenger, and P. Vallittu, “Internal Model Control for DC/DC Converters”, *Proc. of the 8th European Con. on Power Electronics and Applications*, September 7-9, 1999, Lausanne, Switzerland, 7p, CD-ROM.
- [P8] Gadoura, I., T. Suntio, and K. Zenger, “Improved Stability Properties of Boost and Buck-boost Converters Using IMC-based Controller”, *Proc. of the Int. Con. on Power Electronics and Intelligent Motion*, June 19-21, 2001 in Nuremberg, Germany, pp. 527-532.

Publications [P1-P4] and [P6-P8] were mainly contributed by the author of this thesis. In [P5], the author's contribution is shared with the other authors.

List of Notations, Symbols, and Abbreviations

1. NOTATIONS

(A, B, C, D)	State-space realization of a linear system
\mathcal{C}	Field of complex numbers
\mathcal{C}_+	Closed right hand plane of \mathcal{C} , $\{x \in \mathcal{C} \mid \operatorname{Re}(x) \geq 0\}$
\mathcal{C}^n	Linear space of ordered n -tuples in \mathcal{C} , i.e., space of all n -dimensional complex vectors
$\mathcal{C}^{n \times m}$	Ring of complex matrices with n rows and m columns
$\operatorname{diag}(A, B, C)$	Block-diagonal matrix with diagonal entries A , B , and C , i.e., $\operatorname{diag}(A, B, C) = \begin{bmatrix} A & 0 & 0 \\ 0 & B & 0 \\ 0 & 0 & C \end{bmatrix}$
$\mathcal{F}_l(A, B)$	Lower linear fractional transformation defined by $\mathcal{F}_l(A, B) := A_{11} + A_{12}B(I - A_{22}B)^{-1}A_{21}$ where A and B are linear operators. A is partitioned into 2×2 blocks $A = \left[\begin{array}{c c} A_{11} & A_{12} \\ \hline A_{21} & A_{22} \end{array} \right]$ such that the lower right part A_{22} is compatible in size with B .
$\mathcal{F}_u(A, B)$	Upper linear fractional transformation defined by $\mathcal{F}_u(A, B) := A_{22} + A_{21}B(I - A_{11}B)^{-1}A_{12}$ where A and B are linear operators. A is partitioned into 2×2 blocks $A = \left[\begin{array}{c c} A_{11} & A_{12} \\ \hline A_{21} & A_{22} \end{array} \right]$ such that the upper right part A_{11} is compatible in size with B .
$G := \left[\begin{array}{c c} A & B \\ \hline C & D \end{array} \right]$	Packed notation of the transfer function associated with a linear system
(A, B, C, D)	
$\ G\ _\infty$	Norm of $G \in \mathcal{RH}^\infty$ which is called \mathcal{H}_∞ -norm. $\ G\ _\infty := \sup_{\omega \in \mathcal{R}} \bar{\sigma}(G(j\omega))$

\mathcal{G}	An entire set of perturbed models, which must be suitably controlled by the robust controller.
	$\mathcal{G} = \{G(I_n + \Delta W_i) : \Delta \text{ is stable and } \ \Delta\ _\infty \leq 1\}$
\mathcal{G}_ε	The class of perturbed models is given by the family
	$\mathcal{G}_\varepsilon = \left\{ (\tilde{M} + \Delta_M)^{-1} (\tilde{N} + \Delta_N) : [\Delta_M, \Delta_N] \in \mathcal{RH}_\infty, \ \Delta_M, \Delta_N\ _\infty < \varepsilon \right\}$
I_n	$n \times n$ identity matrix
M^T	Transpose of $M \in \mathcal{C}^{n \times m}$
M^*	Complex-conjugate transpose of $M \in \mathcal{C}^{n \times m}$, or adjoint operator of M for a linear operator M
\mathcal{R}	Field of real numbers
\mathcal{R}_+	Set of nonnegative real numbers, $\{x \in \mathcal{R} \mid x \geq 0\}$
\mathcal{R}^n	Linear space of ordered n -tuples in \mathcal{R} , i.e., space of all n -dimensional real vectors
$\mathcal{R}^{n \times m}$	Ring of real matrices with n rows and m columns
\mathcal{RH}^∞	Space of all proper real-rational matrix-valued functions of $s \in \mathcal{C}$, which have no poles in \mathcal{C}_+ , for the continuous-time case.
$ x $	Absolute value of x in \mathcal{C} or \mathcal{R}
$\langle x \rangle$	Averaged value of x in \mathcal{C} or \mathcal{R}
$\ x\ $	Euclidean norm of x in \mathcal{R}^n or \mathcal{C}^n
$\ x\ _p$	Norm of $x = [x_1 \ x_2 \ \cdots \ x_n]^T$ in \mathcal{R}^n or \mathcal{C}^n defined by
	$\ x\ _p := \left(\sum_{i=1}^n x_i ^p \right)^{1/p} \text{ for } 1 \leq p < \infty$
	$\ x\ _\infty := \max_i x_i \text{ for } p = \infty$
\dot{x}	The differentiation of vector x , i.e. $\dot{x} = [\dot{x}_1 \ \dot{x}_2 \ \cdots \ \dot{x}_n]^T$
\hat{x}	The small-signal components of vector x , i.e. $\hat{x} = [\hat{x}_1 \ \hat{x}_2 \ \cdots \ \hat{x}_n]^T$
$\ \cdot\ _H$	The Hankel norm, which is a kind of induced norm from past inputs to future outputs.
	$\ G\ _H = \sqrt{\rho(\mathbb{C} \mathbb{O})}$, where \mathbb{C} is the controllability Gramian matrix and \mathbb{O} is the observability Gramian matrix.
$\bar{\sigma}(X)$	The maximum singular value of X in $\mathcal{C}^{n \times m}$
$\underline{\sigma}(X)$	The minimum singular value of X in $\mathcal{C}^{n \times m}$

γ	The robustness indicator that should be minimized in order to find a stabilizing controller.
ε	The stability margin that should be maximized, which is a problem of robust stabilization of normalized coprime factor plant descriptions. $\varepsilon = 1/\gamma$
ρ	The spectral radius, which is the magnitude of the largest eigenvalue of the matrix A . $\rho(A) = \max_i \lambda_i(A) $
Δ	A specific source of uncertainty, e.g. input uncertainty, output uncertainty, or parametric uncertainty.
$\mu(M)$	Structured singular value with underlying structure $\Delta \subset \mathcal{C}^{n \times m}$. It is defined by $\mu(M) := \left\{ \min \{ \bar{\sigma}(\Delta) : \Delta \in \Delta, \det(I - M\Delta) = 0 \} \right\}^{-1}$ unless no $\Delta \in \Delta$ makes $\det(I - M\Delta) = 0$, in which case $\mu(M) := 0$.

2. SYMBOLS

a_1	Input gains for proportional part of PID-like FLC
a_2	Input gains for proportional part of PI-like FLC
A	System matrix of the nominal system
A_{cl}	System matrix of the closed-loop system
A_K	System matrix of the feedback controller
A_p	System matrix of the perturbed system
A_{OFF}	System matrix of the nominal system when the switch is OFF.
A_{ON}	System matrix of the nominal system when the switch is ON.
b	Reference weight in PID formula
b_1	Input gains for derivative part of PID-like FLC
b_2	Input gains for derivative part of PD-like FLC
B	Input matrix of the nominal system
B_{cl}	Input matrix of the closed-loop system
B_K	Input matrix of the feedback controller
B_p	Input matrix of the perturbed system, i.e. $B_p = [B_{p1} \mid B_{p2}]$
c	Control command
\mathbf{c}	Control command vector
c_0	DC-value(s) of control command (vector)
c_1	Input gain for integral part of PID-like FLC
\mathbf{c}_{CM}	Control command vector in PCMC configuration
\mathbf{c}_i	Control commands vector of current-loop
c_j	Control command of 'j' converter
c_o	The output of PD-like FLC
\mathbf{c}_u	Control commands vector of voltage-loop

\mathbf{c}_{VM}	Control command vector in VMC configuration
\mathbf{c}_{Δ}	Input vector of plant uncertainty
$\mathbf{c}_{\Delta i}$	Input vector of plant uncertainty for current-loop
$\mathbf{c}_{\Delta u}$	Input vector of plant uncertainty for voltage-loop
ce_u	Voltage error change, which is a second input to PID-like FLC
ce_i	Current error change, which is a second input to PD-like FLC
C	Capacitor or capacitance
\mathbf{C}	Output matrix of the nominal system
\mathbf{C}_{cl}	Output matrix of the closed-loop system
\mathbf{C}_K	Output matrix of the feedback controller
\mathbf{C}_p	Output matrix of the perturbed system, i.e. $\mathbf{C}_p = [\mathbf{C}_{p1} \mid \mathbf{C}_{p2}]^T$
\mathbf{C}_{pi}	Output matrix of the perturbed system for current-loop
\mathbf{C}_{pu}	Output matrix of the perturbed system for voltage-loop
\mathbf{C}_{OFF}	Output matrix of the nominal system when the switch is OFF.
\mathbf{C}_{ON}	Output matrix of the nominal system when the switch is ON.
\mathbf{d}	Disturbance vector, e.g. $\mathbf{w} = [u_{in} \ i_g]^T$
d_1	Output gains of PID-like FLC
d_2	Output gains of PI-like FLC
\mathbf{d}_{Δ}	Input vector of disturbance uncertainty
D	Derivative gain of PD and PID controllers
\mathbf{D}	Input-output matrix of the nominal system
\mathbf{D}_{cl}	Input-output matrix of the closed-loop system
\mathbf{D}_K	Input-output matrix of the feedback controller
\mathbf{D}_p	Input-output matrix of the perturbed system, i.e. $\mathbf{D}_p = \left[\begin{array}{c c} \mathbf{D}_{p11} & \mathbf{D}_{p12} \\ \hline \mathbf{D}_{p21} & \mathbf{D}_{p22} \end{array} \right]$
\mathbf{e}	Error vector, i.e. $\mathbf{e} = [\mathbf{e}_u \mid \mathbf{e}_i]^T$
e_{uj}	Voltage error of 'j' converter, i.e. $e_{uj} = u_{ref} - u_j$
e_{ij}	Current error of 'j' converter, i.e. $e_{ij} = i_{ref} - i_{outj}$
\mathbf{e}_u	Voltage error vector, i.e. $\mathbf{e}_u = [e_{u1} \ e_{u2} \ \dots \ e_{un}]^T$
\mathbf{e}_i	Current error vector, i.e. $\mathbf{e}_i = [e_{i1} \ e_{i2} \ \dots \ e_{in}]^T$
\mathbf{E}	Disturbance matrix of the nominal system
\mathbf{E}_{OFF}	Disturbance matrix of the nominal system when the switch is OFF.
\mathbf{E}_{ON}	Disturbance matrix of the nominal system when the switch is ON.
f_s	Switching frequency
\mathbf{F}	Disturbance-output matrix of the nominal system
\mathbf{F}	The closed-loop system from \mathbf{w} to \mathbf{z} , i.e. $\mathbf{F} = \mathcal{F}_u(\mathbf{N}, \Delta)$
F_m	Gain
\mathbf{F}_m	Diagonal gain matrix
\mathbf{F}_{mq}	Diagonal gain matrix, i.e. $\mathbf{F}_{mq} = q \cdot \mathbf{F}_m$
\mathbf{F}_{OFF}	Disturbance-output matrix of the nominal system when the switch is OFF.
\mathbf{F}_{ON}	Disturbance-output matrix of the nominal system when the switch is ON.
\mathbf{F}_u	The closed-loop system from \mathbf{w}_u to \mathbf{z}_u , i.e. $\mathbf{F}_u = \mathcal{F}_u(\mathbf{N}_u, \Delta_{pu})$

\mathbf{G}	Perturbed system transfer matrix, i.e. $\mathbf{G} = \begin{bmatrix} \mathbf{G}_{11} & \mathbf{G}_{12} \\ \mathbf{G}_{21} & \mathbf{G}_{22} \end{bmatrix}$
G_{co}	Control-to-output voltage transfer function
$G_{co-i\ pq}$	Control of 'p' converter-to-output current of 'q' converter transfer function
$G_{co-u\ pq}$	Control of 'p' converter-to-output voltage of 'q' converter transfer function
G_c	Controller transfer function in IMC structure
\mathbf{G}_d	Nominal disturbance model
\mathbf{G}_{di}	Nominal disturbance model for current-loop
\mathbf{G}_{du}	Nominal disturbance model for voltage-loop
\mathbf{G}_{dd}	Perturbed disturbance model
G_f	Low-pass filter transfer function in IMC structure
G_{imc}	Internal model controller, i.e. $G_{imc} = G_f G_c$
G_{ip}	Load-to-output current of 'p' converter transfer function
G_{lo}	Line-to-output voltage transfer function
$G_{lo-i\ pq}$	Line of 'p' converter-to-output current of 'q' converter transfer function
$G_{lo-u\ pq}$	Line of 'p' converter-to-output voltage of 'q' converter transfer function
G_m	Internal model transfer function in IMC structure, which is factorized into all pass portion G_m^+ and a minimum phase portion G_m^- , i.e. $G_m = G_m^+ G_m^-$
\mathbf{G}_p	Nominal plant model
\mathbf{G}_{pi}	Nominal plant model for current-loop
\mathbf{G}_{pp}	Perturbed plant model
\mathbf{G}_{ps}	Shaped nominal plant model
\mathbf{G}_{pu}	Nominal plant model for voltage-loop
\mathbf{G}_u	Perturbed system transfer matrix of voltage-loop
h	The order of low-pass filter in IMC structure
i_c	Control command in PCMC configuration
i_C	Output capacitor current
i_g	Current source represents a load disturbance
i_L	Inductor current
\mathbf{i}_L	The vector of output inductor currents, i.e. $\mathbf{i}_L = [i_{L1} \ i_{L2} \ \dots \ i_{Ln}]^T$
$i_{L,0}$	DC-value of output inductor current
$i_{o\max,0}$	DC-value of maximum output current
i_{out}	Output current
$i_{out,0}$	DC-value of output current
\mathbf{i}_{out}	The vector of output currents, i.e. $\mathbf{i}_{out} = [i_{out1} \ i_{out2} \ \dots \ i_{outn}]^T$
i_{ref}	Reference current, i.e. DS $\Rightarrow i_{ref} = \frac{1}{n} \sum_{j=1}^n i_{out,j}$ and MS $\Rightarrow i_{ref} = i_{out,1}$
I	Integral gain of PI and PID controllers
j	A module number in parallel configuration of DC/DC converters
k	Sample number.
k_{ij}	Augmented current controller of 'j' converter, i.e. $k_{ij} = k_{uj} k_j$
k_j	Current controller of 'j' converter
k_{uj}	Voltage controller of 'j' converter

K	Feedback controller
\mathbf{K}	MIMO feedback controller, e.g. $\mathbf{K} = [\mathbf{K}_u \mid \mathbf{K}_i]$
\mathbf{K}_i	Diagonal current controller matrix, i.e. $\mathbf{K}_i = \text{diag}(k_{i1}, k_{i2}, \dots, k_{in})$
K_p	Proportional gain of PI and PID controllers
\mathbf{K}_s	\mathcal{H}_∞ LSD controller
\mathbf{K}_u	Diagonal voltage controller matrix, i.e. $\mathbf{K}_u = \text{diag}(k_{u1}, k_{u2}, \dots, k_{un})$
L	Inductor or inductance
m_1	Inductor ripple slope when the switch is ON
m_2	Inductor ripple slope when the switch is OFF
m_c	Artificial ramp slope
\mathbf{M}_{cf}	Left coprime factorization of nominal plant, i.e. $\mathbf{G}_p = \mathbf{M}_{cf}^{-1} \mathbf{N}_{cf}$
n	Number of dc-dc converters in parallel
\mathbf{n}	Measurement noise vector
\mathbf{n}_i	Measurement noise vector of current-loop
\mathbf{n}_v	Measurement noise vector of voltage-loop
N	Derivative weight in modified PID formula
N	The closed-loop system from $[\mathbf{v}_\Delta \ \mathbf{w}]^T$ to $[\mathbf{y}_\Delta \ \mathbf{z}]^T$, i.e. $N = \mathcal{F}_l(\mathbf{P}, \mathbf{K}) = \left[\begin{array}{c c} \mathbf{N}_{11} & \mathbf{N}_{12} \\ \hline \mathbf{N}_{21} & \mathbf{N}_{22} \end{array} \right]$
\mathbf{N}_{cf}	Left coprime factorization of nominal plant, i.e. $\mathbf{G}_p = \mathbf{M}_{cf}^{-1} \mathbf{N}_{cf}$
\mathbf{N}_u	The closed-loop system from $[\mathbf{u}_{\Delta u} \ \mathbf{w}_u]^T$ to $[\mathbf{y}_{cu} \ \mathbf{z}_u]^T$, i.e. $\mathbf{N}_u = \mathcal{F}_l(\mathbf{P}_u, \mathbf{K}_u) = \left[\begin{array}{c c} \mathbf{N}_{u11} & \mathbf{N}_{u12} \\ \hline \mathbf{N}_{u21} & \mathbf{N}_{u22} \end{array} \right]$
NB	Negative big membership function
NS	Negative small membership function
P	Proportional gain of P, PI, PD, and PID controllers
\mathbf{P}	Interconnection model transfer matrix
PB	Positive big membership function
P_o	Nominal output power
PS	Positive small membership function
\mathbf{P}_u	Interconnection model transfer matrix of voltage-loop
q	Gain
\mathbf{Q}	Gain matrix that specifies which scheme of current sharing is employed
r	Cable resistance
\mathbf{r}	Reference vector
r_C	Equivalent-series resistance of output capacitor
r_L	Equivalent-series resistance of output inductor
r_o	Cable resistance from DC-busbar to a Telecom load
r_p	Interconnection resistance
R	Resistive load
R_s	Resistor that is used to inject the inductor current into the control circuit in PCMC
S	Sensitivity function
\mathbf{S}_i	Input sensitivity transfer matrix
\mathbf{S}_o	Output sensitivity transfer matrix

t	Time in seconds
T	Complementary sensitivity function
T_d	Derivative time in PD and PID structures
T_i	Integral time in PI and PID structures
\mathbf{T}_i	Input complementary sensitivity transfer matrix
\mathbf{T}_o	Output complementary sensitivity transfer matrix
T_s	Switching time interval
\mathbf{T}_{zw}	The closed-loop transfer matrix from \mathbf{w} to \mathbf{z}
u_{ave}	Average of output voltage, i.e. $u_{ave} = (u_{1,0} + u_{2,0})/2$
u_c	Output of voltage controller
u_C	Output capacitor voltage
$u_{C,0}$	DC-value of output capacitor voltage
u_{CL}	Output of overload controller
u_{in}	Input voltage
$u_{in,0}$	DC-value of input voltage
u_j	Output voltage of ‘ j ’ converter, i.e. $u_j = u_{Cj} + r_{Cj} C_j du_{Cj}/dt$
u_o	Output of PID-like FLC
u_{out}	Output voltage
$u_{out,0}$	DC-value of output voltage
u_{ref}	Reference voltage
u_s	Switching voltage
u_Δ	Input vector of uncertainty
$u_{1,0}$	Maximum DC-value of output voltage
$u_{2,0}$	Minimum DC-value of output voltage
u_{BAT}	Battery voltage
u_{FC}	Float charging voltage
\mathbf{u}_C	The vector of output capacitor voltages, i.e. $\mathbf{u}_C = [u_{C1} \ u_{C2} \ \dots \ u_{Cn}]^T$
\mathbf{u}_{in}	The vector of input voltages, i.e. $\mathbf{u}_{in} = [u_{in1} \ u_{in2} \ \dots \ u_{inn}]^T$
u_{LVD}	LVD voltage, i.e., the LVD switch will turn ON when $u_{BAT} \geq u_{LVD}$
\mathbf{u}_{out}	The vector of output voltages, i.e. $\mathbf{u}_{out} = [u_{out1} \ u_{out2} \ \dots \ u_{outn}]^T$
\mathbf{u}_s	The vector of switching voltages, i.e. $\mathbf{u}_s = [u_{s1} \ u_{s2} \ \dots \ u_{sn}]^T$
U_m	Sawtooth waveform amplitude, i.e. PWM gain
U_s	The feedback signal of current-loop, i.e. $U_s = R_s i_L$
\mathbf{w}	Input vector, e.g. $\mathbf{w} = [\mathbf{r} \ \mathbf{d} \ \mathbf{n}]^T$.
\mathbf{w}_0	DC-values of disturbance vector
w_1	Pre-compensator transfer function.
w_i	Uncertainty weight
w_{id}	Uncertainty weight of disturbance model
w_{ip}	Uncertainty weight of plant model
w_p	Performance weight
\mathbf{w}_u	Input vector of voltage-loop, i.e. $\mathbf{w}_u = [\mathbf{r} \ \mathbf{d} \ \mathbf{n}_u]^T$
\mathbf{W}_1	Pre-compensator in LSD
\mathbf{W}_2	Post-compensator in LSD
\mathbf{W}_d	Disturbance scaling matrix
\mathbf{W}_{id}	Disturbance uncertainty weight transfer matrix

W_{ip}	Plant uncertainty weight transfer matrix
W_n	Measurement noise uncertainty weight transfer matrix
W_{ni}	Measurement noise uncertainty weight transfer matrix of current-loop
W_{nu}	Measurement noise uncertainty weight transfer matrix of voltage-loop
W_p	Performance weight transfer matrix
W_{pi}	Performance weight transfer matrix of current-loop
W_{pu}	Performance weight transfer matrix of voltage-loop
W_r	Reference scaling matrix
W_c	Control command weight transfer matrix
y	Output vector
y_0	DC-value(s) of output voltage(s and currents)
y_d	Output vector of disturbance uncertainty
y_i	Output vector of current-loop
y_m	Feedback signal
y_c	Output vector of plant uncertainty
y_{ci}	Output vector of plant uncertainty of current-loop
y_{cu}	Output vector of plant uncertainty of voltage-loop
y_u	Output vector of voltage-loop
y_Δ	Output vector of uncertainty
x	State-variable vector
x_K	State-variable vector of feedback controller
x_0	DC-values of state-variables vector
z	Output vector, i.e. $z = [z_1 \ z_2]^T$.
z_i	Output vector of current-loop
z_u	Output vector of voltage-loop
Z	Zero membership function
Z_{out}	Output impedance
α	Adjustable gain
β	Resistor gain
δ	The duty-cycle as a function of time, i.e. $\delta = \delta_0 + \hat{\delta}$
δ_0	DC-value of the duty-cycle
Δ_A	Parametric uncertainty of A -matrix
Δ_B	Parametric uncertainty of B -matrix
Δ_{Ci}	Parametric uncertainty of C -matrix for current-loop
Δ_{Cu}	Parametric uncertainty of C -matrix for voltage-loop
Δ_d	Disturbance uncertainty transfer matrix where $\ \Delta_d\ _\infty < 1$ for all ω
Δ_D	Parametric uncertainty of D -matrix
Δi_L	The difference between a peak inductor current and its averaged
$\Delta \langle i_L \rangle$	The change in averaged inductor current
Δ_p	Plant uncertainty transfer matrix where $\ \Delta_p\ _\infty < 1$ for all ω
Δ_{pi}	Plant uncertainty transfer matrix for current-loop where $\ \Delta_{pi}\ _\infty < 1$ for all ω
Δ_{pu}	Plant uncertainty transfer matrix for voltage-loop where $\ \Delta_{pu}\ _\infty < 1$ for all ω
Δu_{ref}	Output of PI-like FLC

Δ_N, Δ_M Left coprime factorization of uncertainty plant model where

$$\mathbf{G}_{pp} = (\mathbf{M}_{cf} + \Delta_M)^{-1} (\mathbf{N}_{cf} + \Delta_N)$$

$\hat{\mathbf{A}}$ Fictitious uncertainty transfer matrix representing the \mathcal{H}_∞ performance specification

ω Frequency in radians/second

λ Parameter that is used to tune the IMC controller

ϕ, Φ Crisp input vector to FLC and its space

θ, Θ Crisp output vector from FLC and its space

3. ABBREVIATIONS

AC	Alternative current
AC/DC	AC to DC rectifier
ACMC	Average current-mode control
ADC	Analog-to-digital converter
ASIC	Application specific integrated circuit
CICM	Continuous inductor current mode
CMC	Current-mode control
CPC	Current programming control
CPL	Constant power load
DAC	Digital-to-analog converter
DC	Direct current
DC/DC	DC to DC converter
DICM	Discontinuous inductor current mode
DK	A method is used to minimize a given μ -condition
DS	Democratic scheme
DSP	Digital-signal processor
EMI	Electromagnetic interference
ESR	Equivalent series resistance
ETSI	European Telecommunications Standard Institute
FDLTI	Finite-dimensional, linear time-invariant
FL	Fuzzy-logic
FLC	Fuzzy-logic controller
GM	Gain margin
IC	Integrated circuit
IMC	Internal-model control
LCF	Left-coprime factorization
LFT	Linear fractional transformation
LHP	Left-hand plane
LQ	Linear quadratic
LSD	Loop-shaping design
LTI	Linear time-invariant
LVD	Low voltage disconnection
MIMO	Multi-input-multi-output
MS	Master-slave scheme

NP	Nominal performance
NS	Nominal stability
P	Proportional control
PCMC	Peak current-mode control
PD	Proportional-derivative control
PFC	Power factor correction
PI	Proportional-integral control
PID	Proportional-integral-derivative control
PM	Phase margin
POL	Point of load
PSU	Power supply unit
PUPS	Point of use power supply
PWM	Pulse-width modulator
RHP	Right-hand plane
RP	Robust performance
RS	Robust stability
SISO	Single-input-single-output
SMPS	Switching-mode power supply
UPS	Uninterruptible power supply
VMC	Voltage-mode control

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Chapter 1

Introduction

In this introduction, material is collected to facilitate understanding of the main components of this thesis. The main motivation is based on the contribution of this work in power electronics. A Telecom power supply operating in different modes is composed of three parts. Each part has its own characteristic. The first part, AC/DC rectifiers, is only considered in this thesis. A cascaded controller is considered necessary in the case of parallel-connected converters. A brief history of applied 'modern' control techniques in DC/DC converters gives a good insight and background to the work presented in the thesis.

1.1 Background and Motivation

"Information Super Highways" is a new terminology in the telecommunication industry referring to new digital infrastructures (Liu, 2000). These infrastructures will be capable of providing a platform of a wide range of voice, video and data information services. Nowadays the Internet is widely and exclusively used enlightening that these infrastructures are needed. When designing these systems, the basic requirements should be taken into account, such as high reliability, low cost, and low power consumption. Power electronics is a central part of these infrastructures and is required to meet the design requirements. A Telecom power system is an important part that needs to provide reliable and cost effective power solution to the information super highways.

A power supply that is used to power Telecom switching systems is typically an uninterruptible power supply system of DC-type composed of AC/DC rectifier stage and a backup battery as shown in Fig. 1.1. The backup battery is in parallel with the load so that when AC power from the mains fails, the load is powered by battery.

Due to the downtime for a Telecom power system, which is only a few minutes in its lifetime of 20 years, a Telecom power system is required to be high quality and high reliability (Liu, 2000). In addition to system redundancy arrangement, high quality for each subsystem is essentially required. The power converters are always at the top of the failed component list that has a very big impact on a Telecom power system. If the AC/DC rectifier

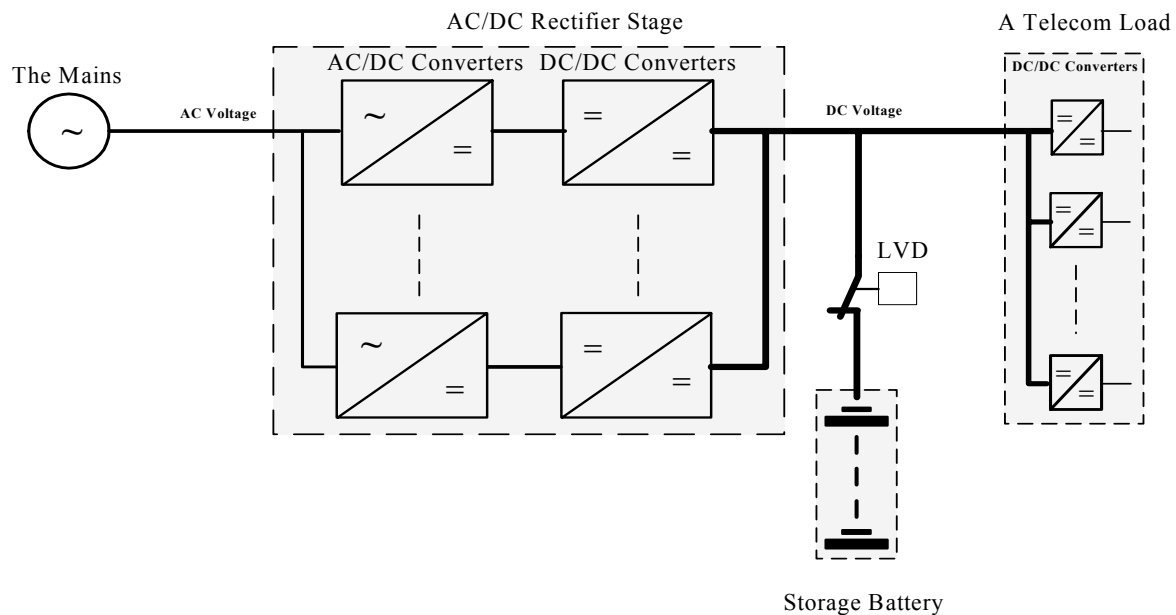


Fig. 1.1 - A typical Telecom power system that consists of three parts: AC/DC rectifier stage, storage battery, and a Telecom load.

stage fails, a large subset of a Telecom system will not function. The voice or data transmission capacity will be reduced significantly, although the battery will provide some back-up time at this condition. However, at a Telecom load, if the DC/DC power supply fails, the board will not function and, sometimes, the expensive digital ICs on the circuit board may be damaged. This causes local service disruption. At this point the necessity of protection system is raised in order to rescue the system when the failure occurs.

The required output characteristic of a Telecom power supply depicts that the control of a power supply is of nonlinear nature. In addition, the required performance must be maintained in the case of many converters operating in parallel. The noise specifications are stringent and stipulated by European Telecommunications Standard Institute (ETSI 300-132-2). All these add more performance objectives to the control design and emphasize that the control circuit should be optimum.

Nowadays the companies are focusing on producing high quality, reduced cost, and more compact products. Integration is a keyword meaning to use the ASIC technology both in power components and controlling/monitoring. Integration means less discrete components and results in less manufacturing cost as well as improved product reliability and quality. ASIC technology normally means use of mixed signal processes including DSP necessitating the adoption of a computer-controlled system. The application of fuzzy control to power electronics is an interesting topic of research. Many publications are dealing with designing of fuzzy-logic controllers for DC/DC converters. However, none of them gives appropriate results comparing with either analog or digital solutions that can achieve the desired output performance perfectly.

A Telecom power supply is a demanding object to be controlled because of its multivariable nature. Large and small signal modeling are used to study the dynamic performance of the power supply. Generally, the small signal models provide a good

accuracy up to 1/10 of the switching frequency, which is most often sufficient from the dynamic range of controlling. Also they can be used to design a proper control system, e.g., the \mathcal{H}_∞ optimal control design. The robustness of control is of prime concern and major problem in analog designs as argued in (Buso, 1999), (Escobar, *et al.*, 1999), (Ioannidis, *et al.*, 1998), and (Pujara, *et al.*, 1996). A model of a Telecom power supply can never be perfect, and as such it will always be an approximation of the real system. Often certain characteristics of a Telecom power system will not be modeled at all. This is either because their contribution to the overall behavior is small, e.g., the AC/DC rectifier preceding DC/DC converter in the AC/DC rectifier stage, or because they are not easily modeled, e.g. the time-delay among switches. Furthermore, the dynamics of a Telecom power system may change during long-term operation, e.g., because of power components' variations. To address the difference between modeled and true systems, various measures of robustness are used. A controller is said to exhibit good robust stability if it remains stable for all variations in plant behavior, which are reasonably expected to occur. Similarly a controller is said to exhibit good robust performance if it continues to perform satisfactorily for all encountered plant variations.

The different control configurations of fuzzy-logic control (FLC), internal-model control (IMC), \mathcal{H}_∞ control, and \mathcal{H}_∞ loop-shaping design (\mathcal{H}_∞ LSD) are adopted into DC/DC converters, and studied and analyzed in order to achieve robust output in spite of different uncertainties. Modeling uncertainties is a key point of designing a proper robust control system. Comparing different control designs gives a good insight into the usability of \mathcal{H}_∞ control in DC/DC converters' field. This thesis aims at providing a wide comparison among different robust control techniques, which are recently applied by the author and his group to either single DC/DC converter or n -paralleled DC/DC converters, in order to reach optimum robust solutions to many problems in reality.

1.2 A Telecom Power Supply

1.2.1 Basic Configuration of a Telecom Power System

A typical Telecom power system is shown in Fig. 1.1. It consists of two parts. One part is the AC/DC rectifier stage that converts the AC line voltage into a DC bus. This DC bus is distributed over the entire Telecom power system. For critical power systems, battery back up is usually required. In this case, the AC/DC rectifier stage should also be able to charge the battery when needed. The other part is DC/DC power supplies that convert the intermediate DC voltage into logic voltage for the Telecom switching system, which is the Telecom load.

1.2.2 Operation Modes

A typical Telecom power system operates in three modes that can be described as follows. The AC/DC rectifier stage supply the load power and maintain the storage battery at fully charged state during the normal mode of operation called constant-voltage mode or float

charging in Fig. 1.2. To ensure maximal reliability performance, the load share between the parallel-connected DC/DC converters should be equal, i.e., fault detection, necessitating the use of active load share controller in each parallel operating units as presented in (Gadoura, *et al.*, 1999a) and (Suntio and Suur-Askola, 1997).

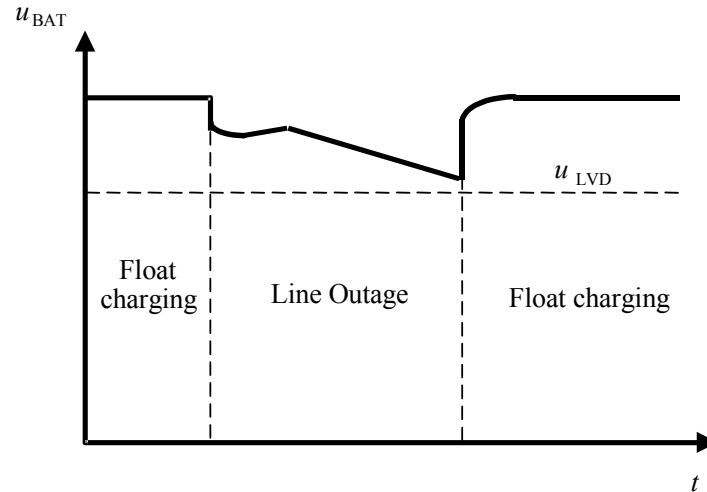


Fig. 1.2 - System operating modes; float charging when the battery is full, line outage when the mains fails and the battery starts powering a Telecom load, float charging when the battery is recharging.

When the mains are interrupted, the battery will discharge, i.e., line outage in Fig. 1.2, and supply the Telecom load. When the mains are restored, the rectifiers will start up and recharge the storage battery as well as supply the Telecom load, i.e., battery recharging in Fig. 1.2.

Telecom systems are very often equipped with low voltage disconnection (LVD) circuitry by means of which the battery will be disconnected from the power system in the case of extremely long line outage in order to prevent it from deep discharging. The LVD facility can be connected either to disconnect the storage battery or the load as shown in Fig. 1.1. To maximize the system reliability performance, see (Suntio and Suur-Askola, 1997), the LVD facility is recommended to be connected at battery side. This will, however, mean that the rectifiers have to start up and power the Telecom load without parallel-connected battery. It will affect significantly the sizing of the units in respect to the load power and to the defining of optimum output characteristics, as shown in (Gadoura, *et al.*, 1999a) and (Suntio, *et al.*, 1996), as well as the stability considerations, as shown in (Gadoura, *et al.*, 1998a) and (Gadoura, *et al.*, 1999b).

1.2.3 AC/DC Rectifier Stage

The AC/DC rectifier stage converts the AC voltage into the DC bus. From technical point of view, the main requirements are high efficiency, low EMI and high power factor or low harmonic distortion at the AC side. Also from both cost and performance point of view, the AC/DC rectifier stage consists of two parts, as shown in Fig. 1.1, is the preferred choice for

high output power application (Liu, 2000). One part is the AC/DC converter that converts the AC line voltage into an intermediate DC voltage. Power factor correction (PFC) is achieved. Boost converter is usually used in this part, because it is easier for input current shaping and it is suitable for high DC output voltage. The other part is the DC/DC converter that converts the intermediate DC voltage to the output DC voltage. Electrical isolation is provided at this stage. A buck-derived converter is usually used for high power application, e.g., forward converter. Now and then, we will only consider the DC/DC converters part of AC/DC rectifier stage for modeling and control design. In practice, the output impedance of an AC/DC converter is almost equal to zero, so that it has no effect on the output load. Consequently, it is sufficient to study the DC/DC converter part when studying the output behavior of the whole system.

1.2.4 A Telecom Load: DC/DC Converters Stage

The DC/DC converters convert the intermediate DC bus voltage into lower voltage to power the logic circuits, as shown in Fig. 1.1. As presented in (Liu, 2000) there are two basic powering architecture options at the DC/DC conversion stage. One is called shelf power and the other is called distributed power. In case of the shelf converter powering options, the power supply unit (PSU) provides the power for all the equipment cards in the shelf. In this scheme, the power supply has multiple outputs to power different types of loads. Because the total output power of the power supply is relatively large, duplicated power supply units are connected in parallel to provide redundancy. The main advantage of this scheme is lower overall cost for the system. It also provides well-controlled voltage profiles among each output. However, it usually requires custom design for the power supply unit. In addition, once the system is designed, it is very difficult to change and upgrade the power system.

Another power option is called distributed power. In this case, the power module is mounted directly on the equipment card. This kind of power module is sometimes called on-board power module, Point of Use Power Supply (PUPS), or Point of Load (POL) power supply (Liu, 2000). In almost all the cases, the on-board power module provides only one output voltage. The trend is to use distributed power option. The main reason is flexibility and shorter time to market. The idea is to buy the power module off the shelf and stick into the board. There is no need for custom design, which is usually the case for shelf converter. Other advantages of this arrangement are low initial system cost and improved reliability. In some cases, only the on-board power module can meet the load transient and voltage regulation requirement. With the output voltage becomes lower and lower, it becomes more and more important to reduce the distance between the power supply and its load. The distributed power option fits in this situation quite well. The main requirements for the DC/DC converters are: high efficiency, low EMI, self-protection, small footprint and low height. It should be noted that for the distributed power architecture, the EMI filtering should be provided somewhere in the system to meet regulatory requirement and to ensure power system stability. Another desirable feature for the on-board power module is surface mountable. The reason behind this is that most of the integrated circuit on the board is surface-mounted. It will reduce assembly cost and to improve reliability if the power module is also surface-mounted.

Also note that a Telecom load is of constant-power type loads (CPL) from DC UPS systems viewpoint due to the internal DC/DC converters, see (Kislovski and Olsson, 1994) and (Suntio, *et al.*, 1996). Also the effect of an ideal CPL, parasitic elements of power components, and backup battery on the system's dynamics is previously studied and analyzed in (Gadoura, *et al.*, 1998a), (Gadoura, 1999), (Zenger, *et al.*, 1999), and (Zenger, *et al.*, 2000).

1.2.5 Output Characteristic of a Telecom Rectifier

Overload protection can be implemented by using either a constant-current limiting or combination of constant-power and constant-current limiting as discussed explicitly in [P5]. In order to utilize maximally the power supplying capacity of a rectifier without extra cost penalties, constant-power/constant-current scheme is preferred. A perfect constant-power limiting is difficult from controlling viewpoint. This is because of the nonlinearity imposed by a product-type control variable of two entities. To overcome this problem, the overload protection can be implemented by using a modified constant-power/constant-current limiting as shown in Fig. 1.3. The governing equations presenting the maximum output current during overload protection are as follows (P_o = nominal output power):

$$u_{2,0} \leq u_{out,0} \leq u_{1,0} : \quad i_{omax,0} \geq \left[(u_{1,0} + u_{2,0} - u_{out,0}) / (u_{1,0} \times u_{2,0}) \right] \times P_o \quad (1.1)$$

$$u_{out,0} \leq u_{2,0} : \quad i_{omax,0} \geq P_o / u_{2,0} \quad (1.2)$$

The encircled points in Fig. 1.3, where the mode change has to be carried out, are difficult from stability viewpoint. That is true especially when a storage battery is connected in parallel to the system rectifiers due to low internal resistance and high capacitance. This means also that special methods have to be used to stabilize the system.

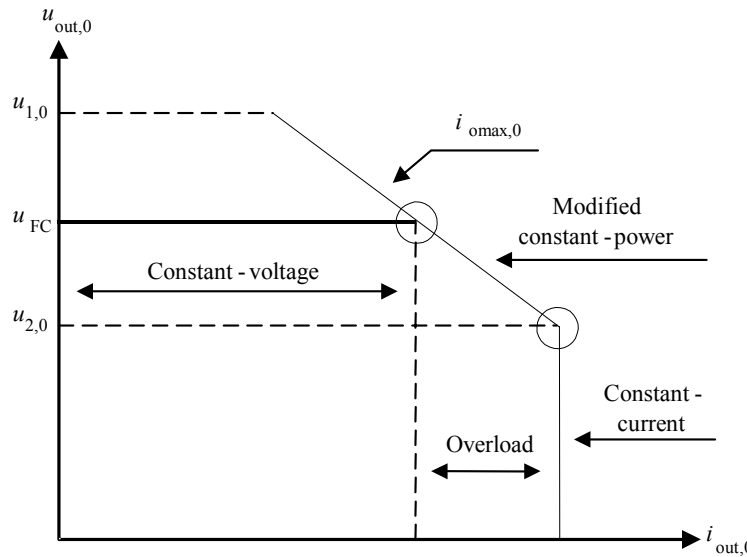


Fig. 1.3 – The recommended output characteristics that should be implemented to ensure an overload protection

1.3 Control Design

1.3.1 Control Configuration of DC/DC Converter

A. Voltage-Mode Control

Many textbooks, see (Krein, 1998), (Mitchell, 1992), (Mohan, *et al.*, 1995), and (Severns and Bloom, 1985), describe voltage-mode control (VMC) as the easiest solution to implement, although it has the disadvantage that it cannot correct any disturbance or change until it is detected at the output. The output voltage is regulated by closing a feedback loop between the output voltage and the duty-cycle. As seen in Fig. 1.4, the output voltage is compared to a reference voltage, $u_{\text{ref}}(t)$ to form an error signal that can be passed through the controller to generate the control signal, which is compared to a sawtooth waveform to finally control the transistor.

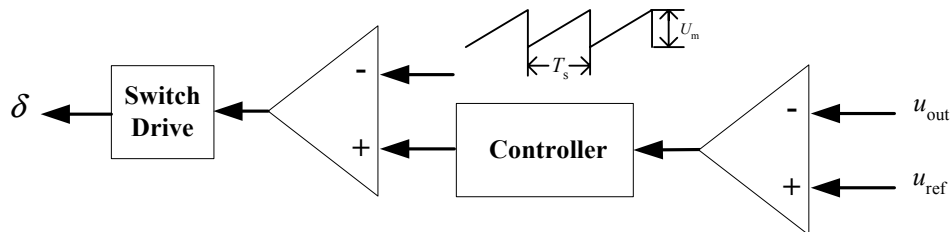


Fig. 1.4 – The voltage-mode control configuration, which is commonly used to regulate most DC/DC converters.

B. Current-Mode Control

Generally, if the current information is added to design a controller, the system dynamics will be significantly improved. This can be seen, e.g., in (Ioannidis, *et al.*, 1998). The inductor current waveform is chosen to illustrate the operation of the control loop, as shown in Fig. 1.5. The transistor is switched on at the start of each cycle by a clock pulse, which sets the output of the latch. The transistor current rises linearly while the device is conducting. The current is fed back as signal $i_L(t)$ and is compared to a reference signal $i_c(t)$. When the peak of $i_L(t)$ is equal to the reference, the comparator output switches low resetting the latch and turning the transistor OFF, representing a *peak current-mode control* (PCMC). Alternatively, when the average of $i_L(t)$ is equal to the reference, the comparator output switches low resetting the latch and turning the transistor OFF, representing an *average current-mode control* (ACMC). To this end the configuration of Fig. 1.5 should be modified. In both cases, the reference signal for the comparator is formed by an output voltage feedback loop produced by the controller. An artificial ramp can be added if the duty-cycle is greater than 0.5 from stabilization viewpoint as emphasized, for example in (Erickson and Maksimovic, 2001) and (Krein, 1998). New results on PCMC and ACMC are presented in (Suntio, *et al.*, 2000b) and (Suntio, *et al.*, 2001), respectively.

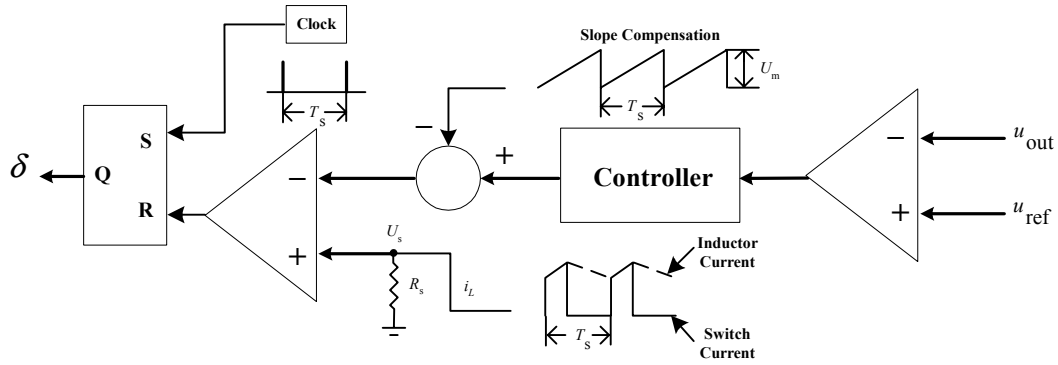


Fig. 1.5 - The current-mode control configuration including the inductor current information to improve the dynamic performance.

1.3.2 Cascaded Controller Structure for Paralleled DC/DC Converters

The paralleled DC/DC converters require a categorical current sharing mechanism to ensure proper operation. The main advantage of using parallel converters configuration with current sharing control is to increase the power process capability that improves a reliability of the overall system, i.e., redundancy. The current sharing scheme can be achieved by injecting a signal proportional to the desired converter output current into the voltage loop. The increased voltage loop error signal forces the duty cycle and then the output current of the converter to increase. The cascaded controllers are used in order to achieve both control objectives as presented in (Panov, *et al.*, 1997), (Rajagopalan, *et al.*, 1996), (Siri, *et al.*, 1992), and (Thottuvelil and Verghese 1998).

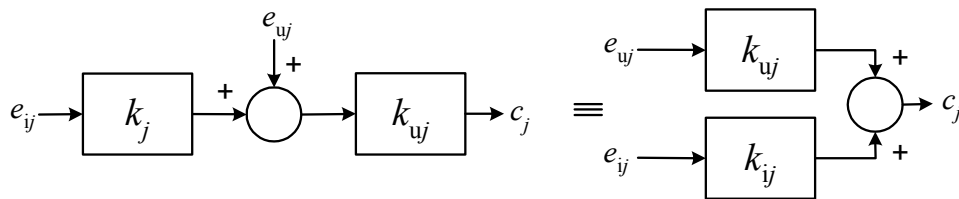


Fig. 1.6 - The cascaded controller configuration used to ensure robust output and to equalize the output currents. Note that $k_{ij} = k_{uj} \cdot k_j$, where $j = 1, 2, \dots, n$.

Also, from the reliability viewpoint, each converter must have its own control circuit. The control system of one converter is a voltage controller, k_{uj} , ensuring robust output voltage cascaded with current controller, k_j , ensuring current sharing as shown in Fig. 1.6.

$$\begin{aligned} c_j &= k_{uj} k_j e_{ij} + k_{uj} e_{uj} \\ &= k_{ij} e_{ij} + k_{uj} e_{uj} \end{aligned} \quad (1.3)$$

From the practical viewpoint, the controller structure of either voltage-loop or current-loop can be presented as a diagonal transfer matrix.

$$\mathbf{K}_u = \text{diag}(k_{u_1}, k_{u_2}, \dots, k_{u_n}) \quad (1.4)$$

$$\mathbf{K}_i = \text{diag}(k_{i_1}, k_{i_2}, \dots, k_{i_n}) \quad (1.5)$$

where \mathbf{K}_u and \mathbf{K}_i are used in control design. Then, the control vector can be written in general form as follows.

$$\mathbf{u} = \mathbf{K}_u \mathbf{e}_u + \mathbf{K}_i \mathbf{e}_i \quad (\text{Two-loop approach}) \quad (1.6)$$

$$\mathbf{u} = \mathbf{K}_u \mathbf{e}_u + \mathbf{K}_i \mathbf{e}_i = [\mathbf{K}_u \mid \mathbf{K}_i] \begin{bmatrix} \mathbf{e}_u \\ \mathbf{e}_i \end{bmatrix} = \mathbf{K} \mathbf{e} \quad (\text{Single-loop approach}) \quad (1.7)$$

where $\mathbf{e} = [\mathbf{e}_u \mid \mathbf{e}_i]^T$, \mathbf{e}_i is a vector of current error, and \mathbf{e}_u is a vector of voltage error.

1.3.3 Robust Control

In classical single-input single-output (SISO) control, gain and phase margins are used as measures of robustness as discussed in (Ogata, 1997) and (Skogestad and Postlethwaite, 1996). Loop shaping can be done in a very systematic way to attain good gain and phase margins, and to specify the desired closed-loop performance. If the plant has more than one output to control, then typically the loops are closed sequentially, i.e., a SISO controller is designed for one of the outputs using an appropriate actuator, that loop is then closed, and then another SISO controller is designed for the next output and so on. This is the so-called *loop-by-loop approach*. For example, for paralleled DC/DC converters the voltage-loop controller might be designed first using the output voltage feedback, and then the current-loop controller designed using the output current feedback as presented in [P5]. Extension of gain margin and phase margin to multivariable systems is a poor indicator of robustness primarily because it doesn't allow coupling between loops. An alternative uncertainty description, which does allow for coupling makes use of the maximum singular value of various closed-loop transfer functions to quantify robustness levels.

According to the small gain theorem, presented for example in (Zhou & Doyle, 1998), the closed loop is guaranteed to remain stable if the transfer function from inputs to outputs, \mathbf{T}_{zw} , is less than γ , where γ is the robustness indicator.

$$\|\mathbf{T}_{zw}\|_\infty < \gamma \quad (1.8)$$

where $\|\mathbf{T}_{zw}\|_\infty$ is the \mathcal{H}_∞ norm and can be defined as

$$\|\mathbf{T}_{zw}\|_\infty := \sup_{\omega} \bar{\sigma}(\mathbf{T}_{zw}(j\omega)) \quad (1.9)$$

A design objective might be to find a \mathbf{K} stabilizing the closed-loop system for a particular uncertainty description. In \mathcal{H}_∞ control law synthesis, the \mathcal{H}_∞ norm of a collection of transfer functions is minimized.

The theory of \mathcal{H}_∞ optimal control originated with G. Zames in 1981. It is firstly developed for input-output systems (Zames, 1981). The state-space solution to \mathcal{H}_∞ control problem is presented in (Doyle, *et al.*, 1989). This approach involves solving only two Riccati equations, and results in a controller of state dimension no higher than that of the weighted plant. This is the solution method used in the designs presented in this thesis. The advent of this reliable solution technique has made the \mathcal{H}_∞ problem formulation a very attractive design approach. As the emphasis of this thesis is that of the practicalities of applying \mathcal{H}_∞ control to a Telecom power supply, the controller equations are not presented here. However, they can be found in robust control textbooks, such as (Skogestad and Postlethwaite, 1996), (Zhou and Doyle, 1998), and (Dullerud and Paganini, 2000).

1.4 Applied Control Techniques in a Telecom Power Supply

DC/DC converters are classified as non-linear systems, which need to be averaged and linearized to obtain a linear time-invariant model. The controller is designed to ensure the stability of the closed-loop system, but also to minimize sensitivity to load changes and to attenuate input-output transmission that is required over large bandwidth. Most designs of feedback loops in DC/DC converters are based on frequency-domain analysis (Erickson and Maksimovic, 2001). A major problem comes into control system design when the transfer function of control-to-output voltage has a RHP-zero. RHP-zero contributes additional phase lag to the system restricting the closed-loop bandwidth. The power system for some applications, e.g. telecommunication equipment, is required to be robust and to operate without instability under a variety of operation conditions. Different control algorithms are applied to regulate DC/DC converters to achieve a robust output voltage. The design of a control system for the buck converter by using pole-placement technique is presented in (Ioannidis, *et al.*, 1998). The simulation and experimental results show fast transient response and good disturbance rejection. In (Escobar, *et al.*, 1999), the experimental result of different nonlinear control algorithms on a boost DC/DC converter including sliding mode control are presented and good comparison among them is carried out. It is concluded that the sliding mode control can provide robust output voltage against line-changes but it is very sensitive to load-changes. The robust stability analysis is done in (Pujara, *et al.*, 1996) by using the Kharitonov theorem and the Segment lemma. Also optimal control theory provides some methods that can be utilized to analyze robust stability.

Due to the wide research of efficient control algorithms, which can be implemented by digital signal processors (DSPs), fuzzy-logic-based controllers are an attractive topic to both academia and industry. They provide a means of converting a linguistic control strategy based on expert knowledge into a feedback control system. A good survey of fuzzy-logic controllers is presented in (Lee, 1990). In the field of designing switching-mode power supplies, the use of fuzzy controllers is quite limited because the conventional controller can carry out the task satisfactorily. The literature on the design of fuzzy controllers for DC/DC converters has been increasing in recent few years, but they cannot present a systematic way to design and tune a fuzzy controller that improves either a small signal or a large-signal response. In (Gadoura, *et al.*, 1998b) the fuzzy controller is designed with an advantage over

the conventional controller because it provides a good transient response although it is not very fast. A similar observation has been reported in (Wang and Lee, 1995). On the other hand, the conventional controller has better disturbance rejection capability than the fuzzy controller has. The derivation of fuzzy PD-like controller for regulating DC/DC converters and its implementation in a digital signal processor is presented in (So, *et al.*, 1996). The output voltage error and its derivative are used as the inputs and the duty cycle as the output of the fuzzy controller. Although they used the crisp values to achieve the optimum output (duty cycle), the results show poor dynamic performance. In (Mattavelli, *et al.*, 1997) the proposed fuzzy controller has three inputs, the output voltage error, the inductor current error, and the inductor current, which is used for current limiting. The controller output is the duty cycle, which is the sum of the outputs of fuzzy P-like controller and fuzzy I-like controller. This structure helps to improve the dynamic performance of the system as shown by the results. However, two membership functions that are chosen to control the inductor current are not enough to ensure the overcurrent limiting. Different structures of fuzzy controller, e.g. fuzzy PD, fuzzy PI, etc. are presented in (Jantzen, 1998). It also includes a tuning procedure of fuzzy controllers by using PID gains. The design is easy but not applicable to all systems. The implementation of a fuzzy-logic control algorithm into a microcontroller is presented in (Gupta, *et al.*, 1997). The experimental results show poor load disturbance capability for fuzzy controlled-buck converter.

The internal model control (IMC) structure, introduced by Garcia and Morari in 1982, makes use of a model in the parallel path of the plant in the equivalent control structure. The IMC structure provides a suitable background to analyze stability conditions. Control design is based on an assumed process model and a low-pass filter is included to improve the robustness of the design. The principles of IMC scheme are introduced in (Morari and Zafriou, 1989). Application of robust control theory to buck-boost converter is presented in (Buso, 1999). The uncertainties of parameters and line/load variations are considered to evaluate the relative errors between nominal and perturbed models then to choose uncertainty weights. A conventional PI-controller has been designed in the worst-case where line/load changes are minimum and parameters variations are maximum. Although the PI-controller can guarantee nominal performance and robust stability, robust performance cannot be achieved. The DK-iteration has been used to achieve robust performance. Also application to Ćuk converter is presented in (Tymerski, 1996). The perturbation block has been modeled as a diagonal matrix presenting different uncertainties: components uncertainties, load uncertainties, and worst-case phase/gain margin. Robust stability is tested using μ -analysis, however robust performance is not tested although it is important in practice. In (Wallis and Tymerski, 2000) the same modeling procedure has been applied to boost converter with both unstructured and structured uncertainties. Control design guarantees nominal and robust performances with respect to uncertainties of power converter components. Good comparison among controllers of \mathcal{H}_∞ , voltage-mode, voltage-mode with input voltage feed-forward, and current-mode has been presented in (Naim, *et al.*, 1997) showing the best capability of \mathcal{H}_∞ -controller over others. However, uncertainties have been excluded. \mathcal{H}_∞ loop-shaping controllers with/without current feedback, and LQ-controller have been designed for buck converter as presented in (Ioannidis and Manias, 1999). Nominal and robust stability and

performance are tested using μ -analysis. The simulation and experimental results show the potentiality of \mathcal{H}_∞ loop-shaping controller.

An excessive work has been done in the field of modeling, analysis, and control design of parallel-connected DC/DC converters. Previous studies on parallel-connected DC/DC converters have not fully addressed the effect of cable resistances and the interactions among converters (Garabandic and Petrovic, 1995) and (Rajagopalan, *et al.*, 1996). Most current-loop controllers are designed separately to ensure stability. However, the interactions affect the stability properties and the dynamic performance has not been studied. Also some modeling problems have been raised when Thévenin circuits are considered to model paralleled converters. These include complexity and mistreatment of interactions. Models of parallel-connected DC/DC converters, which are presented in (Siri and Banda, 1995) and (Thottuvelil and Verghese, 1998) can never be perfect because certain characteristics were not modeled at all, e.g., variations of power stage components, changes of operating points, load alterations, etc. The uncertainties cannot easily be modeled, however they must be included in the analysis. Various measures of robustness can be used; robust stability and robust performance guarantee that the system performs well in spite of disturbances and model uncertainties. Previous studies emphasized the applications of robust control theory to DC/DC converters but never tried to utilize theory in practical issues. Application of robust control theory to two-buck converters in parallel is presented in (Garabandic and Petrovic, 1995) where the nominal stability and robust stability in terms of singular values have been ensured. The simulation results show good dynamic performance of the system. The work has been extended to design robust decentralized control including both structured and unstructured uncertainties as presented in (Garabandic, *et al.*, 1998). The simulation results show good disturbances rejection capabilities. The necessity of a reliable control system that offers robust stability for the overall system and robust performance for its dynamics in presence of uncertainties is highly recommended to guarantee that a Telecom power supply is robustly uninterruptible. The \mathcal{H}_∞ control is one optimal solution used to achieve the robustness issues for a Telecom power supply. However, the selection of weighting functions in \mathcal{H}_∞ control design is non-trivial and invariably incorporates an iterative procedure where the weights are modified in the case of the resulting system failing to meet design specifications. Overcoming this difficulty the \mathcal{H}_∞ loop-shaping design, which combines classical loop shaping ideas with \mathcal{H}_∞ robust stabilization is suggested where the weighting functions are selected to shape the singular values of the nominal model as explicitly presented in (McFarlane and Glover, 1990) and (Feng, 1995). After all, the constraints of \mathcal{H}_∞ control have made its application in DC/DC converters very limited and raised the necessity of use the non-conservative approach that may be more flexible to reach good results. However, the design of \mathcal{H}_∞ controller for DC/DC converters is achieved by injecting the current information into the control circuit, which is well-known in practice, i.e., wherever the current information has been used as a control parameter, the control design is quite flexible.

1.5 Outline of the Thesis

This thesis consists of six chapters including the Introduction. The following chapters are outlined below:

Chapter 2: Modeling of DC/DC Converters.

The aim of this chapter is to utilize the modeling techniques that are used in power electronics in order to model DC/DC converters. In the beginning the author has assumed that the system operates in CICM with VMC. The state-space averaging and linearization are used with the purpose of deriving a linear system representation in either a state-space form or transfer function. The multiloop operation model of paralleled converters is also considered using the same techniques approaching a linearized system. The control system block diagrams are presented that help to formulate the control objectives.

Chapter 3: Uncertainty Models and Robustness.

In this chapter, some sets of perturbed models that are used to design robust controllers are generated. The structured and unstructured uncertainties are used, however, only the parameter variations are considered in both cases. The graphical presentation of uncertainties helps to understand the constraints of the use of robust control methods. The controller analysis and synthesis for DC/DC converters are also included in order to evaluate the control design in the next chapter.

Chapter 4: Controller Design.

This chapter presents the analogue design of PID controller for overload protection. The practical validation of the design is presented in [P5]. Also the PID-like FLC for overload protection is explicitly presented. The key issue is that the cascaded controller should be implemented. A constant-voltage controller is designed to ensure robust output and an overload controller to protect the converter when it runs overload. Also the control design procedures that are based on IMC, for one-unit converter, and \mathcal{H}_∞ & \mathcal{H}_∞ LSD, for parallel-connected converters, are presented.

Chapter 5: Design Examples.

The simulation results are presented in this chapter, which is actually a utilization stand of previous chapters. It includes FLC and IMC simulation for one-unit converter and PI/PID, \mathcal{H}_∞ , and \mathcal{H}_∞ LSD simulation for parallel-connected converters. The selection of weights is a crucial stage to achieve good results. The μ -analysis is also included as a tool of examining NS, NP, RS, and RP.

Chapter 6: Conclusions.

This chapter includes a summary that gives important issues discussed in the publications included in this thesis. Concluding remarks give an overview of the thesis. Author's contribution is given in separate section emphasizing the merit of this work. Also the future trends from the author's viewpoint are remarked.

Appendices: Appendix A presents the procedure that is used to model a multiplicative uncertainty in this thesis. Appendix B gives some Matlab™ codes and Simulink™ models that have been used to generate the results included in this thesis. Appendix C is a glossary that belongs to power electronics field. Appendix D is a collection of eight publications that this thesis is based on.

Chapter 2

Modeling of DC/DC Converters

Averaged models are usually used to represent power electronic systems (Krein, 1998). These averaged models are not necessarily linear, so they have to be linearized according to conventional methods for nonlinear systems. Linearized models support control design methods based on linear systems. This chapter aims to derive the linear models of one-unit converter and parallel-connected converters operating in CICM with VMC and PCMC.

2.1 State-Space Averaging Technique

In DC/DC converters, the functional relationships between sources, outputs, and control parameters are explored through the use of averaging. The basic DC/DC converters are two-switched network converters when operated in CICM, in that the system is switched back and forth between two linear systems under the control of duty-cycle. In each of the two positions of the switch, the system is linear. The dynamic equations of buck converter in Fig. 2.1 can be written as

$$\frac{di_L(t)}{dt} = -\frac{r_C R + r_L R + r_C r_L}{L(R + r_C)} i_L(t) - \frac{R}{L(R + r_C)} u_C(t) + \frac{1}{L} u_s(t) + \frac{r_C R}{L(R + r_C)} i_g(t) \quad (2.1-a)$$

$$\frac{du_C(t)}{dt} = \frac{R}{C(R + r_C)} i_L(t) - \frac{1}{C(R + r_C)} u_C(t) - \frac{R}{C(R + r_C)} i_g(t) \quad (2.1-b)$$

$$u_{out}(t) = \frac{r_C R}{R + r_C} i_L(t) + \frac{R}{R + r_C} u_C(t) - \frac{r_C R}{R + r_C} i_g(t) \quad (2.1-c)$$

where $u_s(t) = \begin{cases} u_{in}(t), & \text{when the switch is ON} \\ 0, & \text{when the switch is OFF} \end{cases}$

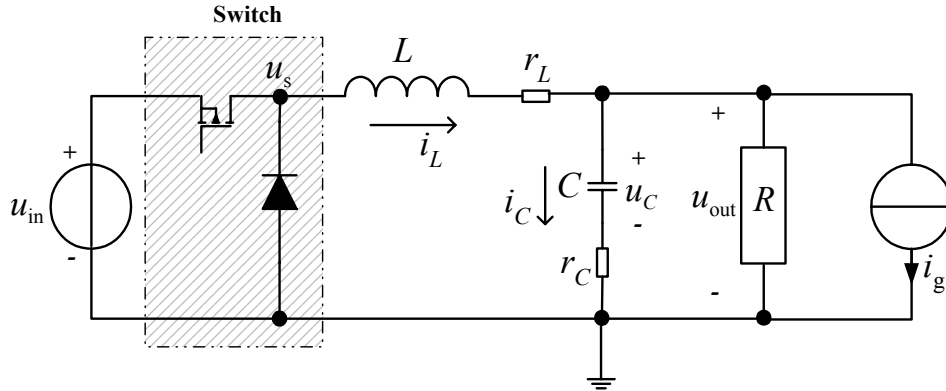


Fig. 2.1 – A simple buck converter feeding a resistive load only considered in simulations. However, a real Telecom load is more close to a constant-power load.

The averaged state-space equations can be represented as follows.

$$\langle \dot{\mathbf{x}} \rangle = \mathbf{A} \langle \mathbf{x} \rangle + \mathbf{E} \langle \mathbf{d} \rangle \quad (2.2-a)$$

$$\langle \mathbf{y} \rangle = \mathbf{C} \langle \mathbf{x} \rangle + \mathbf{F} \langle \mathbf{d} \rangle \quad (2.2-b)$$

where $\langle \mathbf{x} \rangle = [\langle i_L \rangle \quad \langle u_C \rangle]^T$, $\langle \mathbf{d} \rangle = [\langle u_{in} \rangle \quad \langle i_g \rangle]^T$, $\langle \mathbf{y} \rangle = \langle u_{out} \rangle$

$$\mathbf{A} = \mathbf{A}_{ON} \delta + \mathbf{A}_{OFF} (1 - \delta) = \begin{bmatrix} -\frac{r_C R + r_L R + r_C r_L}{L(R + r_C)} & -\frac{R}{L(R + r_C)} \\ \frac{R}{C(R + r_C)} & -\frac{1}{C(R + r_C)} \end{bmatrix}$$

$$\mathbf{E} = \mathbf{E}_{ON} \delta + \mathbf{E}_{OFF} (1 - \delta) = \begin{bmatrix} \frac{\delta}{L} & \frac{r_C R}{L(R + r_C)} \\ 0 & -\frac{R}{C(R + r_C)} \end{bmatrix}$$

$$\mathbf{C} = \mathbf{C}_{ON} \delta + \mathbf{C}_{OFF} (1 - \delta) = \begin{bmatrix} \frac{r_C R}{R + r_C} & \frac{R}{R + r_C} \end{bmatrix}, \text{ and } \mathbf{F} = \mathbf{F}_{ON} \delta + \mathbf{F}_{OFF} (1 - \delta) = \begin{bmatrix} 0 & -\frac{r_C R}{R + r_C} \end{bmatrix}$$

2.2 AC-Small Signal Model

A small signal model gives insight into the dynamic properties of the averaged variables in a converter. The small signal model can be derived by linearizing the nonlinear equations (2.2). Note that the nonlinearity of equations (2.2) is caused by the product of $\delta(t)$ $u_{in}(t)$.

Consider the following nonlinear system

$$\langle \mathbf{y} \rangle = f(\langle x_1 \rangle, \langle x_2 \rangle, \dots, \langle x_n \rangle) \quad (2.3)$$

The linearization procedure presented in (Ogata, 1997) is based on the expansion of the nonlinear function into a Taylor series about the operating points and the retention of only the linear terms. The linear mathematical model of equation (2.3) near the operating conditions is given by

$$\hat{y} = \left. \frac{df}{d\langle x_1 \rangle} \right|_{\substack{x_1=x_{1,0} \\ \vdots \\ x_n=x_{n,0}}} \hat{x}_1 + \left. \frac{df}{d\langle x_2 \rangle} \right|_{\substack{x_1=x_{1,0} \\ \vdots \\ x_n=x_{n,0}}} \hat{x}_2 + \dots + \left. \frac{df}{d\langle x_n \rangle} \right|_{\substack{x_1=x_{1,0} \\ \vdots \\ x_n=x_{n,0}}} \hat{x}_n \quad (2.4)$$

Therefore, the small signal model can be obtained by using equation (2.4) and can be rewritten as follows

$$\hat{\mathbf{x}} = \mathbf{A} \hat{\mathbf{x}} + \mathbf{B} \hat{c} + \mathbf{E} \hat{d} \quad (2.5-a)$$

$$\hat{y} = \mathbf{C} \hat{\mathbf{x}} + \mathbf{F} \hat{d} \quad (2.5-b)$$

$$\hat{\mathbf{x}} = \begin{bmatrix} -\frac{r_c R + r_L R + r_c r_L}{L(R+r_c)} & -\frac{R}{L(R+r_c)} \\ \frac{R}{C(R+r_c)} & -\frac{1}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{u}_C(t) \end{bmatrix} + \begin{bmatrix} \frac{u_{in,0}}{L} \\ 0 \end{bmatrix} \hat{\delta}(t) + \begin{bmatrix} \frac{\delta_0}{L} & \frac{r_c R}{L(R+r_c)} \\ 0 & -\frac{R}{C(R+r_c)} \end{bmatrix} \begin{bmatrix} \hat{u}_{in}(t) \\ \hat{i}_g(t) \end{bmatrix} \quad (2.6)$$

$$\hat{y}(t) = \begin{bmatrix} \frac{r_c R}{R+r_c} & \frac{R}{R+r_c} \end{bmatrix} \begin{bmatrix} \hat{i}_L(t) \\ \hat{u}_C(t) \end{bmatrix} + \begin{bmatrix} 0 & -\frac{r_c R}{R+r_c} \end{bmatrix} \begin{bmatrix} \hat{u}_{in}(t) \\ \hat{i}_g(t) \end{bmatrix} \quad (2.7)$$

The DC solution can be derived as

$$\mathbf{x}_0 = -\mathbf{A}^{-1} \mathbf{B} \delta_0 \text{ and } u_{out,0} = \mathbf{C} \mathbf{x}_0$$

$$\text{then } i_{L,0} = \frac{\delta_0 u_{in,0}}{R+r_L} \text{ and } u_{C,0} = \frac{R}{R+r_L} \delta_0 u_{in,0} = u_{out,0}$$

Also the transfer functions of the system, as indicated in Fig. 2.3(a), can be derived as follows.

$$\hat{y}(s) = \underbrace{\mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1} \mathbf{B}}_{G_{co}=G_p} \hat{c}(s) + \underbrace{\left[\mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1} \mathbf{E} + \mathbf{F} \right]}_{[G_{lo} \quad Z_{out}]=G_d} \hat{d}(s)$$

A small-signal representation of current-controlled buck converter is formed by considering the inductor current waveform, as shown in Fig. 2.2, under transient conditions as presented in (Schultz, 1993). The sampling of inductor current takes place when $t = (k + \delta)T_s$ and the duty-cycle constraints can, therefore, be written as

$$i_c(t) - m_c \delta(t) T_s = i_L(t) + \Delta i_L(t) \quad (2.8)$$

From Fig. 2.2, Δi_L can be derived by solving the following governing equations:

$$\Delta i_L + \delta \Delta \langle i_L \rangle / 2 = m_1 \delta T_s / 2 \quad (2.9a)$$

$$\Delta i_L - (1 - \delta) \Delta \langle i_L \rangle / 2 = m_2 (1 - \delta) T_s / 2 \quad (2.9b)$$

where $m_1 = (u_{in}(t) - u_{out}(t)) / L$ and $m_2 = (u_{out}(t)) / L$

$$\text{Then } \Delta i_L = \frac{\delta(1-\delta) T_s}{2L} u_{in}(t) \quad (2.10)$$

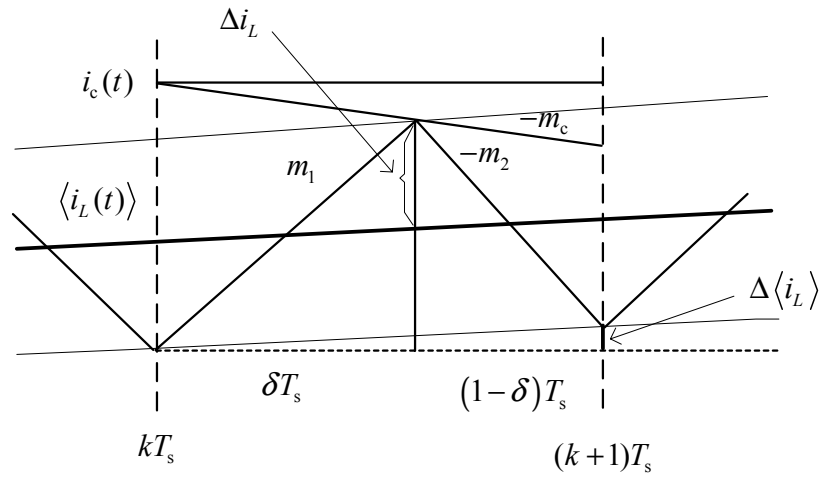


Fig. 2.2 - The waveform of the inductor current. It is used later to derive the control signal constraints of PCMC.

By substituting the equation (2.10) into (2.8), we can rewrite the duty-cycle constraints as

$$i_c(t) - m_c \delta(t) T_s = i_L(t) + \frac{\delta(1-\delta) T_s}{2L} u_{in}(t) \quad (2.11)$$

which is the same conclusion that has been reached in (Schultz, 1993) and (Suntio, 2002).

To derive the ac-small signal model, the linearization method in equation (2.4) should be applied to equation (2.11). Then the small signal of duty-cycle becomes

$$\hat{\delta}(t) = \frac{1}{m_c T_s + \frac{u_{in,0}}{2L} (1 - 2\delta_0) T_s} \left[\hat{i}_c(t) - \hat{i}_L(t) - \frac{T_s}{2L} \delta_0 (1 - \delta_0) \hat{u}_{in}(t) \right] \quad (2.12)$$

$$\hat{\delta}(t) = F_m \left[\hat{i}_c(t) - \hat{i}_L(t) - q \hat{u}_{in}(t) \right] \quad (2.13)$$

After substituting the equation (2.13) into the state-space representation of voltage-controlled buck converter, equation (2.2), a new state-space representation for the buck converter with PCMC will be obtained. Also new transfer functions can be derived.

The design of a control system begins with a model of a power converter, which is in general a finite dimensional approximation of the physical system. Although the linearized model approximates a real power converter quite well at low frequencies, all models are inadequate at higher frequencies. Differences between the model and the actual plant are treated as model uncertainty, as shown in Fig. 2.3(b).

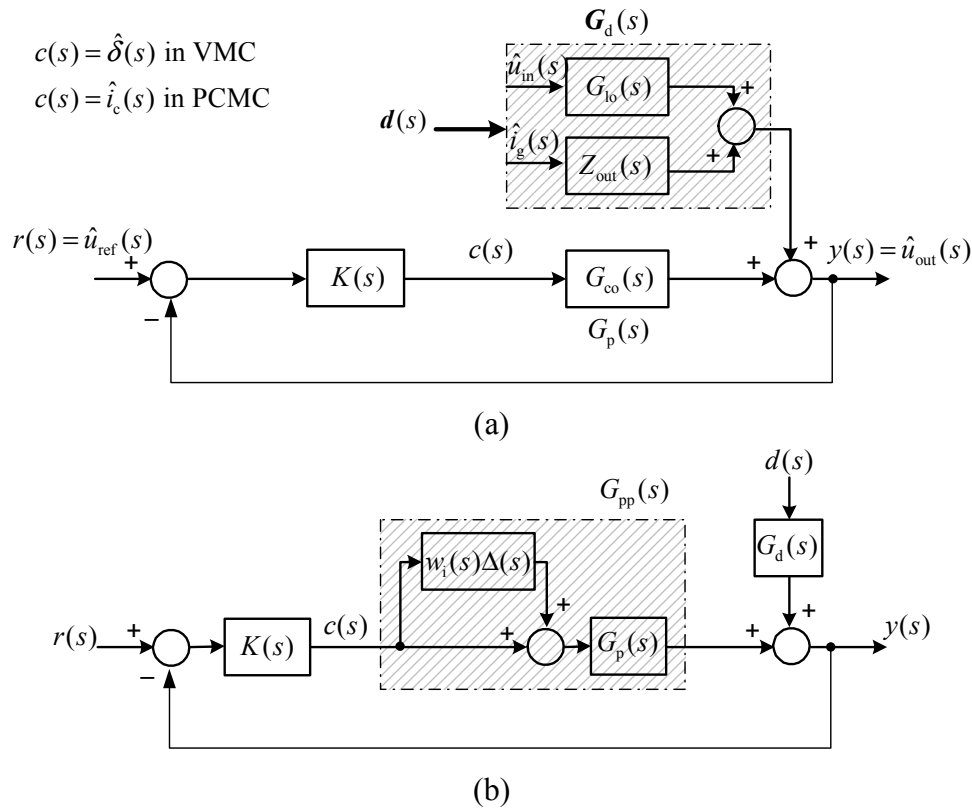


Fig. 2.3 - The classical feedback system that is commonly used in control design of DC/DC converters (a) and modern control system including uncertainty model (b).

2.3 Multiloop Operation of Paralleled DC/DC Converters

Current sharing among converters is the main control issue in parallel converters. The common reasons for paralleling power converters are either to increase the power output capability above the rating of a single module or to provide for redundancy so that a single module failure will not affect the system operation. Paralleling power converters adds complexity to the system and typically entails accepting some performance and cost compromises. In practice, the control is needed to ensure proper current sharing and many effective control schemes have been proposed in previous studies, such as (Choi, 1998), (Garabandic and Petrovic, 1995), (Perreault, *et al.*, 1999), and (Thottuvelil and Verghese,

1998). One common approach is to employ an active control scheme to force the currents in parallel converters to follow the reference current, which is an average current of converters. Such a scheme is commonly known as the democratic current sharing scheme (DS) as presented in (Jovanovic, *et al.*, 1996) and (Siri, *et al.*, 1992). If the reference current is the output current of one converter, such a scheme is known as the master-slave current sharing scheme (MS) as presented in (Panov, *et al.*, 1997), (Rajagopalan, *et al.*, 1996), and (Siri, *et al.*, 1992). The essence of an active control is to monitor the difference between the reference current and the output current of each converter and incorporate this information into the control of voltage-loop. The necessity of reliable control system that offers robust stability for the overall system and robust performance for its dynamics in presence of uncertainties is recommended, as presented in (Buso, 1999), (Garabandic and Petrovic, 1995), and (Tymerski, 1996). However only a single module has been considered. The procedure of designing a robust controller requires a model that takes the uncertainties of the system into consideration, as studied in (Skogestad and Postlethwaite, 1996).

2.3.1 Single-Loop Approach

In practice, parallel-connected DC/DC converters may be located far apart and may require unequal lengths of cable connecting them to bus bar where the load they share is connected to. The unequal cable lengths and interconnection points to bus bar between converters result in different impedances and contribute to the current-share distribution, as shown in Fig. 2.4. Concluding, all interconnection resistances should be included in the derived model. In (Siri and Banda, 1995) and (Thottuvelil and Verghese, 1998), the cable resistance has been taken into account when the comparison between different control techniques was carried out. The converter cable has significant impact on the performance of parallel-connected converters and, therefore, should be included in converter design. The state-space representation of averaged and linearized model that helps to derive all transfer functions of the system including interactions is presented in the next section.

A. State-Space Representation

According to Fig. 2.4 and after manipulating the dynamic equations that describe the system behavior, the state equations taking into account all interconnection resistances can be written as follows:

$$d\mathbf{i}_L/dt = \mathbf{M}_{in} \mathbf{u}_s - \mathbf{M}_{il} \mathbf{i}_L - \mathbf{M}_{ul} \mathbf{u}_C + \mathbf{M}_{gl} i_g \quad (2.14)$$

$$d\mathbf{u}_C/dt = \mathbf{M}_{ic} \mathbf{i}_L - \mathbf{M}_{uc} \mathbf{u}_C - \mathbf{M}_{gc} i_g \quad (2.15)$$

$$\text{where } \mathbf{i}_L = [i_{L_1} \ i_{L_2} \ \cdots \ i_{L_n}]^T, \quad \mathbf{u}_C = [u_{C_1} \ u_{C_2} \ \cdots \ u_{C_n}]^T, \quad \mathbf{u}_s = [u_{s_1} \ u_{s_2} \ \cdots \ u_{s_n}]^T,$$

$$\text{and } u_{s_j} = \begin{cases} u_{in_j}, & \text{when the switch is ON} \\ 0, & \text{when the switch is OFF} \end{cases}$$

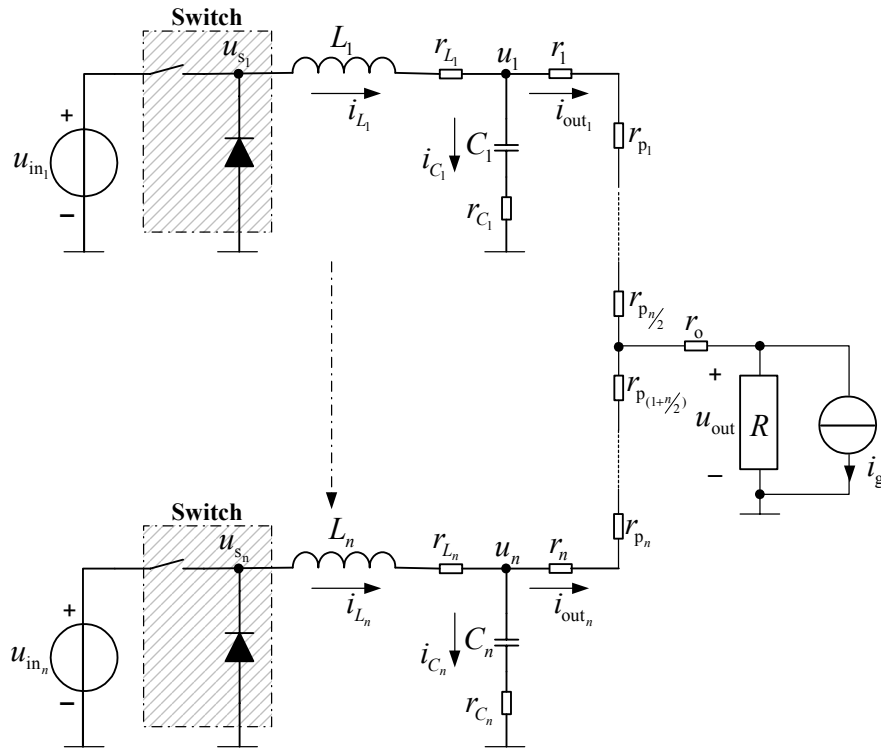


Fig. 2.4 – Parallel-connected DC/DC converters including all cable and interconnection resistances feeding a resistive load.

$$\mathbf{u}_{\text{out}} = \mathbf{M}_{\text{iu}} \mathbf{i}_L + \mathbf{M}_{\text{uu}} \mathbf{u}_C - \mathbf{M}_{\text{ug}} i_g \quad (2.16)$$

$$\mathbf{i}_{\text{out}} = \mathbf{M}_{\text{ii}} \mathbf{i}_L + \mathbf{M}_{\text{ui}} \mathbf{u}_C + \mathbf{M}_{\text{ig}} i_g \quad (2.17)$$

$$\mathbf{u}_{\text{out}} = [u_{\text{out}_1} \ u_{\text{out}_2} \ \cdots \ u_{\text{out}_n}]^T, \mathbf{i}_{\text{out}} = [i_{\text{out}_1} \ i_{\text{out}_2} \ \cdots \ i_{\text{out}_n}]^T$$

All matrices presented in equations (2.14) and (2.15) are dependent on the power stage components and obtained from the dynamic equations of multiloop operation of paralleled DC/DC converters.

$$\mathbf{M}_{\text{in}} = \text{diag}(1/L_1, 1/L_2, \cdots, 1/L_n)$$

$$\mathbf{M}_{\text{uc}}^{-1} = \text{diag}(C_1(r_{C_1} + r_1), C_2(r_{C_2} + r_2), \cdots, C_n(r_{C_n} + r_n)) + \mathbf{M}_p \text{diag}(C_1, C_2, \cdots, C_n)$$

$$\mathbf{M}_{\text{ic}} = \mathbf{M}_{\text{uc}} (\mathbf{M}_p + \text{diag}(r_1, r_2, \cdots, r_n))$$

$$\mathbf{M}_{\text{gc}} = \mathbf{M}_{\text{uc}} \mathbf{M}_r$$

$$\mathbf{M}_{\text{il}} = \text{diag}(r_{L_1}/L_1, r_{L_2}/L_2, \cdots, r_{L_n}/L_n) + \text{diag}(r_{C_1} C_1/L_1, r_{C_2} C_2/L_2, \cdots, r_{C_n} C_n/L_n) \mathbf{M}_{\text{ic}}$$

$$\mathbf{M}_{\text{ul}} = \text{diag}(1/L_1, 1/L_2, \cdots, 1/L_n) - \text{diag}(r_{C_1} C_1/L_1, r_{C_2} C_2/L_2, \cdots, r_{C_n} C_n/L_n) \mathbf{M}_{\text{uc}}$$

$$\mathbf{M}_{\text{gl}} = \text{diag}(r_{C_1} C_1/L_1, r_{C_2} C_2/L_2, \cdots, r_{C_n} C_n/L_n) \mathbf{M}_{\text{gc}}$$

$$\begin{aligned}
\mathbf{M}_{ii} &= \mathbf{I}_n - \text{diag}(C_1, C_2, \dots, C_n) \mathbf{M}_{ic} \\
\mathbf{M}_{ui} &= \text{diag}(C_1, C_2, \dots, C_n) \mathbf{M}_{uc} \\
\mathbf{M}_{ig} &= \text{diag}(C_1, C_2, \dots, C_n) \mathbf{M}_{gc} \\
\mathbf{M}_{iu} &= \text{diag}(r_{C_1}, r_{C_2}, \dots, r_{C_n}) (\mathbf{I}_n - \mathbf{M}_{ii}) \\
\mathbf{M}_{uu} &= \mathbf{I}_n - \text{diag}(r_{C_1}, r_{C_2}, \dots, r_{C_n}) \mathbf{M}_{ui} \\
\mathbf{M}_{ug} &= \text{diag}(r_{C_1}, r_{C_2}, \dots, r_{C_n}) \mathbf{M}_{ig} \\
\mathbf{M}_r &= [R \quad R \quad \dots \quad R]^T
\end{aligned}$$

$$\mathbf{M}_p = \left[\begin{array}{cccc|cccc}
R+r_o + \sum_{q=1}^{n/2} r_{p_q} & R+r_o + \sum_{q=2}^{n/2} r_{p_q} & \dots & R+r_o + r_{p_{n/2}} & R+r_o & R+r_o & \dots & R+r_o \\
R+r_o & R+r_o + \sum_{q=2}^{n/2} r_{p_q} & \dots & R+r_o + r_{p_{n/2}} & R+r_o & R+r_o & \dots & R+r_o \\
\vdots & \vdots & \ddots & \vdots & \vdots & \vdots & \ddots & \vdots \\
R+r_o & R+r_o & \dots & R+r_o + r_{p_{n/2}} & R+r_o & R+r_o & \dots & R+r_o \\
\hline
R+r_o & \dots & R+r_o & R+r_o & R+r_o + r_{p_{(n/2)+1}} & \dots & R+r_o & R+r_o \\
\vdots & \ddots & \vdots & \vdots & R+r_o + r_{p_{(n/2)+1}} & \ddots & \vdots & \vdots \\
R+r_o & \dots & R+r_o & R+r_o & \vdots & \dots & R+r_o + \sum_{q=(n/2)+2}^n r_{p_q} & R+r_o \\
R+r_o & \dots & R+r_o & R+r_o & R+r_o + r_{p_{(n/2)+1}} & \dots & R+r_o + \sum_{q=(n/2)+2}^n r_{p_q} & R+r_o + \sum_{q=(n/2)+1}^n r_{p_q}
\end{array} \right]$$

After averaging and linearization of the previous equations, a linear time-invariant system is realized and represented in state-space form.

$$\frac{d}{dt} \begin{bmatrix} \hat{\mathbf{i}}_L \\ \hat{\mathbf{u}}_C \end{bmatrix} = \left[\begin{array}{c|c} -\mathbf{M}_{il} & -\mathbf{M}_{ul} \\ \hline \mathbf{M}_{ic} & -\mathbf{M}_{uc} \end{array} \right] \begin{bmatrix} \hat{\mathbf{i}}_L \\ \hat{\mathbf{u}}_C \end{bmatrix} + \left[\begin{array}{c} \mathbf{M}_{in,u_{in,0}} \\ 0 \end{array} \right] \hat{\delta} + \left[\begin{array}{c|c} \mathbf{M}_{in,\delta_0} & \mathbf{M}_{gl} \\ \hline 0 & -\mathbf{M}_{gc} \end{array} \right] \begin{bmatrix} \hat{\mathbf{u}}_{in} \\ \hat{\mathbf{i}}_g \end{bmatrix}$$

$$\begin{bmatrix} \hat{\mathbf{u}}_{out} \\ \hat{\mathbf{i}}_{out} \end{bmatrix} = \left[\begin{array}{c|c} \mathbf{M}_{iu} & \mathbf{M}_{uu} \\ \hline \mathbf{M}_{ii} & \mathbf{M}_{ui} \end{array} \right] \begin{bmatrix} \hat{\mathbf{i}}_L \\ \hat{\mathbf{u}}_C \end{bmatrix} + \left[\begin{array}{c|c} 0 & -\mathbf{M}_{ug} \\ \hline 0 & \mathbf{M}_{ig} \end{array} \right] \begin{bmatrix} \hat{\mathbf{u}}_{in} \\ \hat{\mathbf{i}}_g \end{bmatrix}$$

$$\mathbf{M}_{in,\delta_0} = \mathbf{M}_{in} \text{diag}(\delta_{0_1}, \delta_{0_2}, \dots, \delta_{0_n})$$

$$\mathbf{M}_{in,u_{in,0}} = \mathbf{M}_{in} \text{diag}(u_{in,0_1}, u_{in,0_2}, \dots, u_{in,0_n})$$

$$\hat{\mathbf{x}} = \mathbf{A} \hat{\mathbf{x}} + \mathbf{B} \hat{\mathbf{c}}_{VM} + \mathbf{E} \hat{\mathbf{d}} \quad (2.18)$$

$$\hat{\mathbf{y}} = \mathbf{C} \hat{\mathbf{x}} + \mathbf{D} \hat{\mathbf{c}}_{VM} + \mathbf{F} \hat{\mathbf{d}} \text{ where } \mathbf{D} = [0] \quad (2.19)$$

In order to derive the AC-small-signal model in the state-space representation for paralleled DC/DC converters operating in CICM with PCMC, equation (2.13) is recalled

$$\hat{\delta} = F_m \left[\hat{i}_c - \hat{i}_L - q \hat{u}_{in} \right]$$

The matrix form of the previous equation can be written as

$$\hat{\delta} = F_m \hat{i}_c - F_m \hat{i}_L - F_{mq} \hat{u}_{in} \quad (2.20)$$

where $F_m = \text{diag}(F_{m_1}, F_{m_2}, \dots, F_{m_n})$ and $F_{mq} = \text{diag}(F_{m_1} q_1, F_{m_2} q_2, \dots, F_{m_n} q_n)$.

After substituting the equation (2.20) into equations (2.18) and (2.19), the ac-small-signal model can be derived.

$$\frac{d}{dt} \begin{bmatrix} \hat{i}_L \\ \hat{u}_C \end{bmatrix} = \begin{bmatrix} -M_{il} - M_{in,u_{in,0}} F_m & -M_{ul} \\ M_{ic} & -M_{uc} \end{bmatrix} \begin{bmatrix} \hat{i}_L \\ \hat{u}_C \end{bmatrix} + \begin{bmatrix} M_{in,u_{in,0}} F_m \\ 0 \end{bmatrix} \hat{i}_c + \begin{bmatrix} M_{in,\delta_0} - M_{in,u_{in,0}} F_{mq} & M_{gl} \\ 0 & -M_{gc} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_g \end{bmatrix}$$

$$\hat{\dot{x}} = A \hat{x} + B \hat{c}_{CM} + E \hat{d} \quad (2.21)$$

$$\hat{y} = C \hat{x} + D \hat{c}_{CM} + F \hat{d} \text{ where } D = [0] \quad (2.22)$$

B. Transfer Matrices

From the state-space representation, all transfer functions of the system including interactions can be derived as follows

$$\underbrace{\begin{bmatrix} \hat{u}_{out_1} \\ \hat{u}_{out_2} \\ \vdots \\ \hat{u}_{out_n} \\ \hat{i}_{out_1} \\ \hat{i}_{out_2} \\ \vdots \\ \hat{i}_{out_n} \end{bmatrix}}_{y(s)} = \underbrace{\begin{bmatrix} G_{co_u_{11}} & G_{co_u_{12}} & \cdots & G_{co_u_{1n}} \\ G_{co_u_{21}} & G_{co_u_{22}} & \cdots & G_{co_u_{2n}} \\ \vdots & \vdots & \ddots & \vdots \\ G_{co_u_{n1}} & G_{co_u_{n2}} & \cdots & G_{co_u_{nn}} \\ G_{co_i_{11}} & G_{co_i_{12}} & \cdots & G_{co_i_{1n}} \\ G_{co_i_{21}} & G_{co_i_{22}} & \cdots & G_{co_i_{2n}} \\ \vdots & \vdots & \ddots & \vdots \\ G_{co_i_{n1}} & G_{co_i_{n2}} & \cdots & G_{co_i_{nn}} \end{bmatrix}}_{G_p(s)} \underbrace{\begin{bmatrix} \hat{c}_1 \\ \hat{c}_2 \\ \vdots \\ \hat{c}_n \end{bmatrix}}_{c(s)} + \underbrace{\begin{bmatrix} G_{lo_u_{11}} & G_{lo_u_{12}} & \cdots & G_{lo_u_{1n}} & Z_{out_1} \\ G_{lo_u_{21}} & G_{lo_u_{22}} & \cdots & G_{lo_u_{2n}} & Z_{out_2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ G_{lo_u_{n1}} & G_{lo_u_{n2}} & \cdots & G_{lo_u_{nn}} & Z_{out_n} \\ G_{lo_i_{11}} & G_{lo_i_{12}} & \cdots & G_{lo_i_{1n}} & G_{i_1} \\ G_{lo_i_{21}} & G_{lo_i_{22}} & \cdots & G_{lo_i_{2n}} & G_{i_2} \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ G_{lo_i_{n1}} & G_{lo_i_{n2}} & \cdots & G_{lo_i_{nn}} & G_{i_n} \end{bmatrix}}_{G_d(s)} \underbrace{\begin{bmatrix} \hat{u}_{in_1} \\ \hat{u}_{in_2} \\ \vdots \\ \hat{u}_{in_n} \\ \hat{i}_g \end{bmatrix}}_{d(s)} \quad (2.23)$$

where $c(s)$ is $c_{VM}(s)$ in case of VMC and $c_{CM}(s)$ in case of PCMC. Also $G_{lo_u_{ji}}$ is the line-to-output voltage, $G_{co_u_{ji}}$ is the control-to-output voltage, Z_{out_j} is the load-to-output voltage, $G_{lo_i_{jq}}$ is the line-to-output current, $G_{co_i_{jq}}$ is the control-to-output current, G_{i_j} is the load-to-output current transfer functions. For simplicity equation (2.23) can be reformulated in general form with omitting hats as

$$y = G_p c + G_d d \quad (2.24)$$

where y is an output vector, c is a control vector, d is a disturbance vector, G_p is a plant model, and G_d is a disturbance model.

The closed-loop structure of paralleled DC/DC converters including uncertainty models and performance objectives is shown in Fig. 2.5 where the true paralleled DC/DC converters model is represented by dashed box. Note that W_{ip} and W_{id} are the uncertainty weights of plant and disturbance model, respectively. W_p is a performance weight, which is usually a low-pass filter used to achieve the desired closed-loop characteristic. W_n is a measurement noise weight, which is a high-pass filter. W_c is a control command weight. W_r and W_d are scaling matrices.

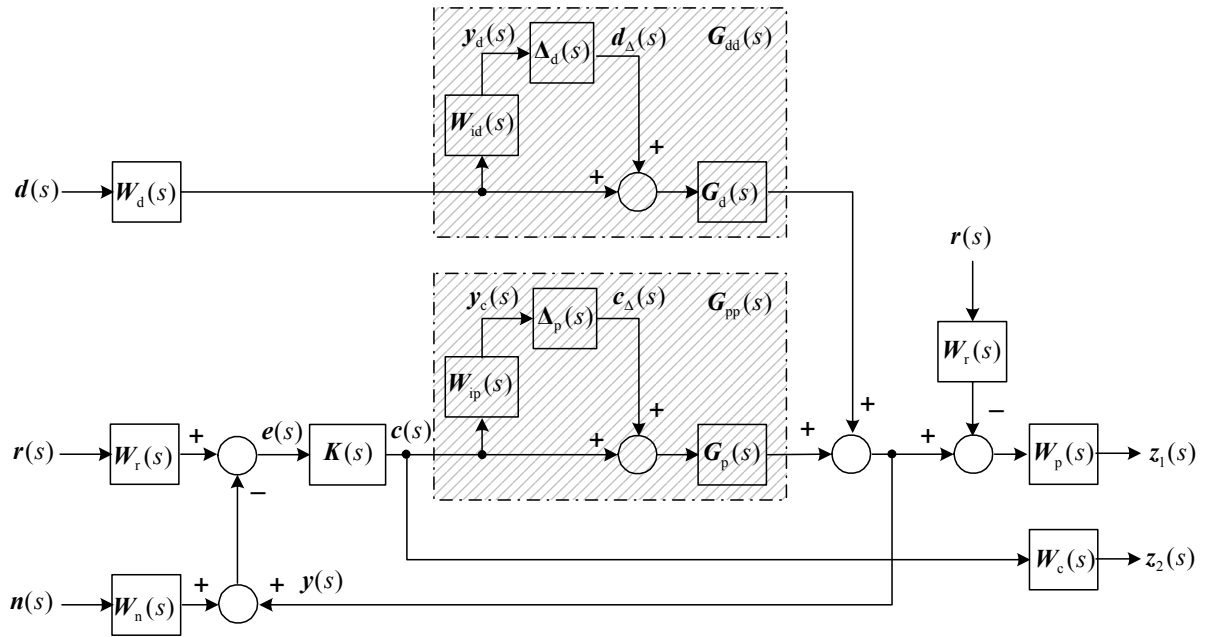


Fig. 2.5 – The control system of paralleled DC/DC converters including all uncertainties, which are presented as a multiplicative-input uncertainty.

2.3.2 Two-Loop Approach

In order to design a practical robust control of paralleled DC/DC converters, as shown in Fig. 2.4, the overall system is composed of two-MIMO subsystems, for voltage-loop and current-loop. The actual plant models consist of nominal plant models and uncertainty models.

$$\begin{bmatrix} y_u \\ y_i \end{bmatrix} = \begin{bmatrix} G_{pu} \\ G_{pi} \end{bmatrix} c + \begin{bmatrix} G_{du} \\ G_{di} \end{bmatrix} d \quad (2.23)$$

where the subscript “v” stands for voltage-loop subsystem and “i” for current-loop subsystem. The voltage-loop consists of n -SISO subsystems, where n is the number of converters in parallel that can be designed separately.

$$y_{u_j} = G_{p_{u_j}} c_j + G_{d_{u_j}} d_j, \text{ where } j = 1, 2, \dots, n \quad (2.24)$$

The voltage-loop design problem is illustrated in Fig. 2.6 when the disconnection at point “a” occurs. The design objective is to determine the controller parameters so that the system is robust with respect to changes in the line and load disturbances as well as in the plant model. Note that \mathbf{Q} -block in Fig. 2.6 is used to employ either master-slave current sharing scheme (MS) or democratic current sharing scheme (DS).

$$\mathbf{Q}_{MS} = \begin{bmatrix} 0 & 0 & 0 & \cdots & 0 \\ 1 & -1 & 0 & \cdots & 0 \\ 1 & 0 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 0 & 0 & \cdots & -1 \end{bmatrix} \text{ and } \mathbf{Q}_{DS} = \frac{1}{n} \begin{bmatrix} 1-n & 1 & \cdots & 1 \\ 1 & 1-n & \cdots & 1 \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1-n \end{bmatrix} \quad (2.25)$$

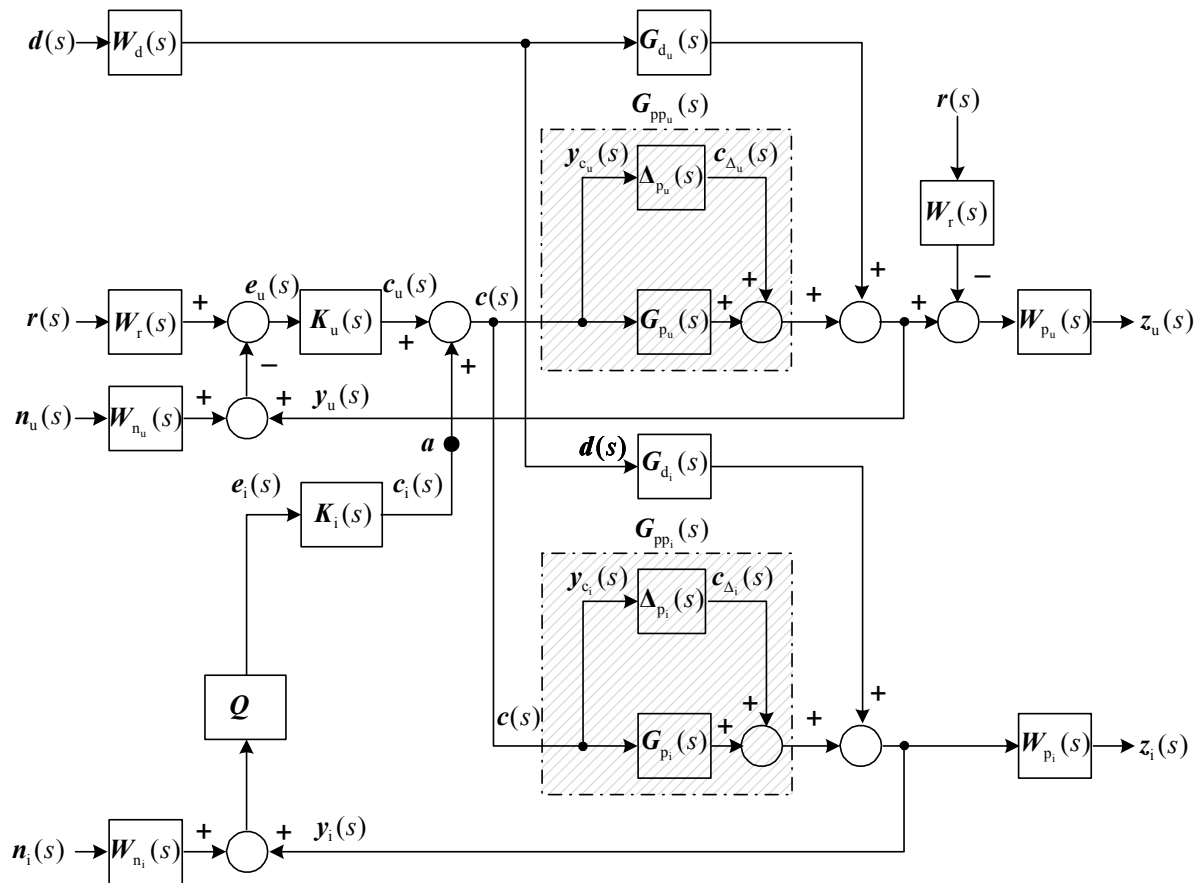


Fig. 2.6 - The control configuration of paralleled DC/DC converters including all uncertainties. The control of voltage-loop is considered when it is isolated from the current-loop by breaking the connection at point a .

Chapter 3

Uncertainty Models and Robustness

The term uncertainty refers to the differences or errors between models and real systems. Whatever methodology is used to present these errors will be called an uncertainty model. For the study of robust stability and robust performance, we assume that the actual plant is represented by a transfer matrix that belongs to an uncertainty model set.

3.1 Uncertainty Model

The uncertainty of the plant model may be due to many reasons, such as linearization, different operating conditions, and the variation in power stage components. The uncertainty may be represented in parametric form or in terms of gain and phase bounds. A family of plants may be represented by a nominal model and uncertainty bound. A set of parametric uncertainty models can be generated if we have taken the following parameter variations in consideration, as presented in [P1-P4]:

- Uncertainty in passive components, i.e., capacitors and inductors: According to manufacturer, the variation of L can be about $\pm 15\%$ of nominal value and of C about from -50% to $+20\%$. Note that, in the simulations, the variations of L were about $\pm 10\%$ and of C about $\pm 20\%$.
- Uncertainty in parasitic elements, i.e., ESR of L and C : They depend on manufacturing of L and C . The variations can reach to $+90\%$ of nominal values.
- Uncertainty in dynamic load, i.e., resistive load: The output power of a Telecom power system can be varied from 10% to 90% of its maximum.
- Uncertainty in line source, i.e., input voltage: Due to the utility supply discontinuity the variations of line source can be about $\pm 20\%$ of nominal value.
- Uncertainty in interconnection resistances, i.e., resistances of cable and interconnection

points between converters: The variations of these resistances can reach to +90% of nominal values.

When the voltage-mode control (VMC) is applied to two-buck converters connected in parallel, Fig. 3.1 shows the dominant parameters that affect considerably on the modeling of the uncertainty. When the \mathcal{H}_∞ norm of the relative error is more than one, the uncertain parameters present the worst-case situation that is extremely difficult to control. It is obvious that the inductors' values, L , have a big effect on the resulting relative errors. Also the capacitors' values, C , have a considerable effect. Therefore, in design level the output inductors should be selected with minimum tolerances as much as possible. As a matter of fact, the minimum tolerances of inductors that exist in market are $\pm 15\%$.

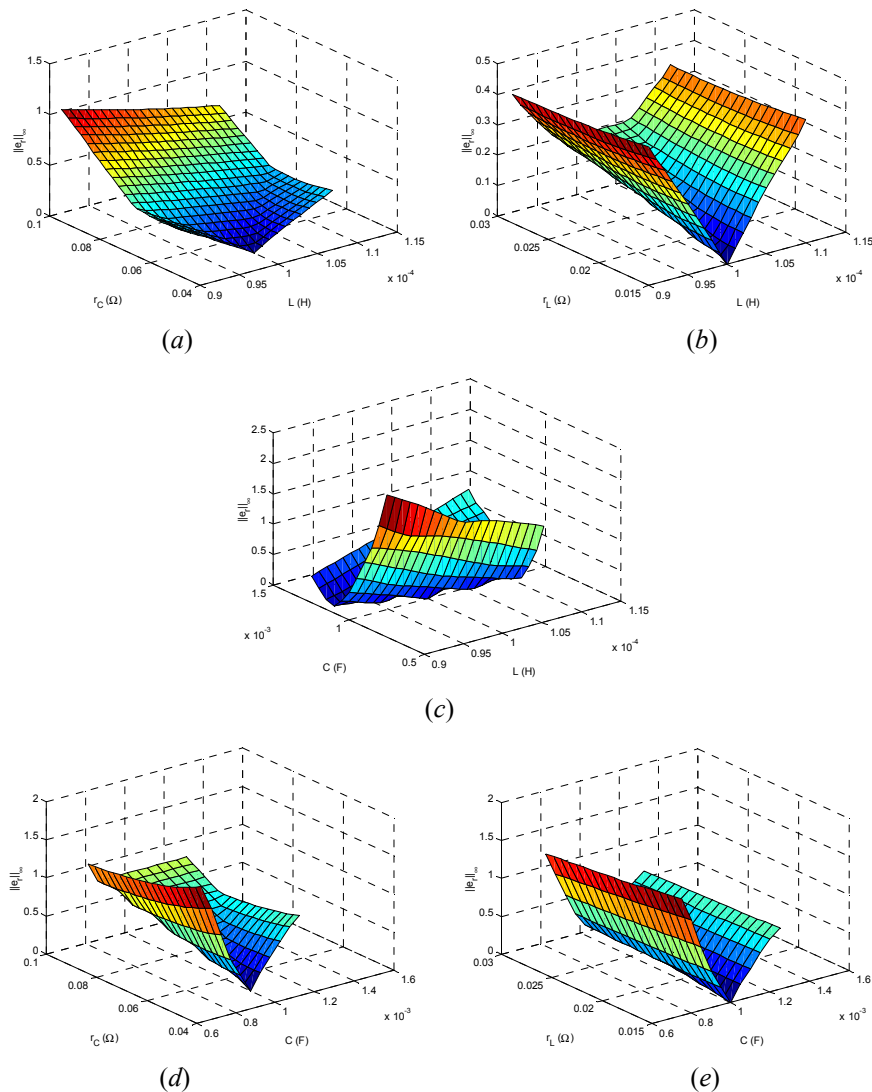


Fig. 3.1 – The \mathcal{H}_∞ -norm of the relative error between the perturbed, G_{pp} , and nominal, G_p , plant models. The worst-case is when the \mathcal{H}_∞ -norm goes over unity, (a) L vs. r_C , (b) L vs. r_L , (c) L vs. C , (d) C vs. r_C , and (e) C vs. r_L .

3.1.1 Structured Uncertainty

A general procedure to treat the parametric uncertainty is presented in, e.g., (Skogestad and Postlethwaite, 1996), (Tymerski, 1996). The structured uncertainty is here modeled by comparing the worst-case perturbed model to the nominal model. That worst-case model produces the largest peak of the relative errors when comparing to the nominal model.

Consider the perturbed plant models of equation (2.23) as shown in Fig. 2.6.

$$G_{ppu} = C_{pu} (sI - A_p)^{-1} B_p \quad (\text{For voltage-loop}) \quad (3.1)$$

$$G_{ppi} = C_{pi} (sI - A_p)^{-1} B_p \quad (\text{For current-loop}) \quad (3.2)$$

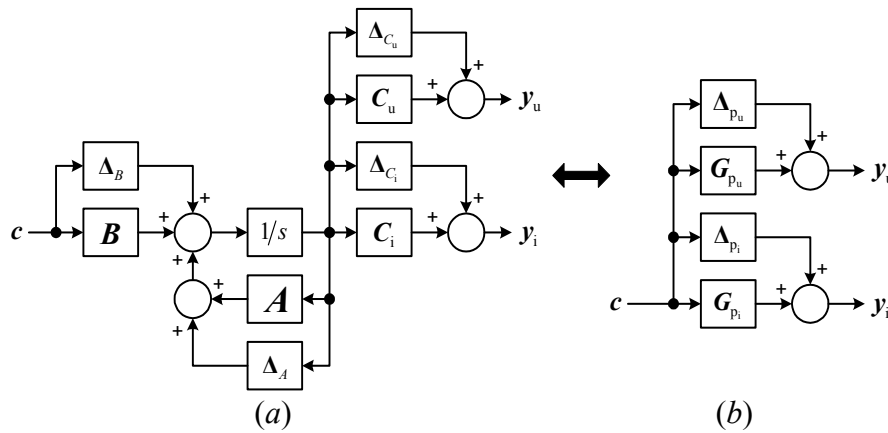


Fig. 3.2 - The parametric uncertainty in state-space representation, (a), and its equivalent, (b) that inserts into the control system of Fig. 2.6.

These transfer matrices can be presented as a perturbed state-space model as follows.

$$\begin{aligned} \dot{x} &= A_p x + B_p u \\ y_u &= C_{pu} x \quad \text{and} \quad y_i = C_{pi} x \end{aligned} \quad (3.3)$$

The perturbed state-space matrices can be realized as shown in Fig. 3.2(a), and Fig. 3.2(b) shows how to adapt the uncertainty model into Fig. 2.6.

$$A_p = A + \Delta_A, \quad B_p = B + \Delta_B, \quad C_{pi} = C_i + \Delta_{Ci}, \quad \text{and} \quad C_{pu} = C_u + \Delta_{Cu}$$

where A , B , C_i , and C_u model the nominal system, Δ_A , Δ_B , Δ_{Ci} , and Δ_{Cu} model the uncertainty, i.e., the real parameter variations in power components of converters. The uncertain perturbations are chosen into a block-diagonal matrix as follows.

$$\Delta_{pu} = \text{diag}(\Delta_A, \Delta_B, \Delta_{Cu}) \quad (3.4)$$

$$\Delta_{pi} = \text{diag}(\Delta_A, \Delta_B, \Delta_{Ci}) \quad (3.5)$$

3.1.2 Unstructured Uncertainty

The unstructured uncertainty can be represented using additive uncertainty or inverse additive uncertainty, multiplicative input uncertainty or inverse multiplicative input uncertainty, and multiplicative output uncertainty or inverse multiplicative output uncertainty, for more details see (Skogestad and Postlethwaite, 1996). However, in this text the multiplicative input uncertainty is used because other uncertainty representations cannot give better results. For SISO systems, the multiplicative uncertainty bound in which the family of the plant is defined as

$$\mathcal{G} = \left\{ G_{pp} : \frac{|G_{pp} - G_p|}{|G_p|} \leq |w_{ip}| \right\} \quad (3.6)$$

where G_{pp} , G_p , and $|w_{ip}|$, represent the actual plant, nominal model, and multiplicative uncertainty bounds, respectively. Thus any member of \mathcal{G} satisfies

$$G_{pp} = G_p (1 + w_{ip} \Delta_p), \text{ where } |\Delta_p| \leq 1 \quad \forall \omega \quad (3.7)$$

For MIMO systems, the multiplicative input uncertainty is used to represent the model uncertainty. The performance objective is that the ∞ -norm of transfer function from w to z be small for all possible uncertainty transfer functions Δ . These uncertainties have been lumped together into one block uncertainty at the input of a nominal model, as shown in Fig. 2.5. The nominal plant G_p and the uncertainty weight W_{ip} parameterize an entire set of plants, \mathcal{G} , which must be suitably controlled by the robust controller K .

$$\mathcal{G} = \left\{ G_p (I_n + \Delta_p W_{ip}) : \Delta_p \text{ is stable and } \|\Delta_p\|_{\infty} \leq 1 \right\} \quad (3.8)$$

The unknown transfer function $\Delta_p(s)$ is used to parameterize the difference between the nominal model G_p and the actual behavior of real system, G_{pp} . To do this, the weight W_{ip} should be chosen so that the normalized perturbation satisfies

$$\max_{G_{pp} \in \mathcal{G}} \bar{\sigma} \left\{ G_p^{-1} (G_{pp} - G_p) \right\} \leq |w_{ip}| \quad \forall \omega, \quad \text{where } W_{ip} = w_{ip} I_n \quad (3.9)$$

Also the weight W_{id} should be chosen so that the normalized perturbation satisfies

$$\max_{G_{dd} \in \mathcal{G}} \bar{\sigma} \left\{ G_d^{-1} (G_{dd} - G_d) \right\} \leq |w_{id}| \quad \forall \omega, \quad \text{where } W_{id} = w_{id} I_n \quad (3.10)$$

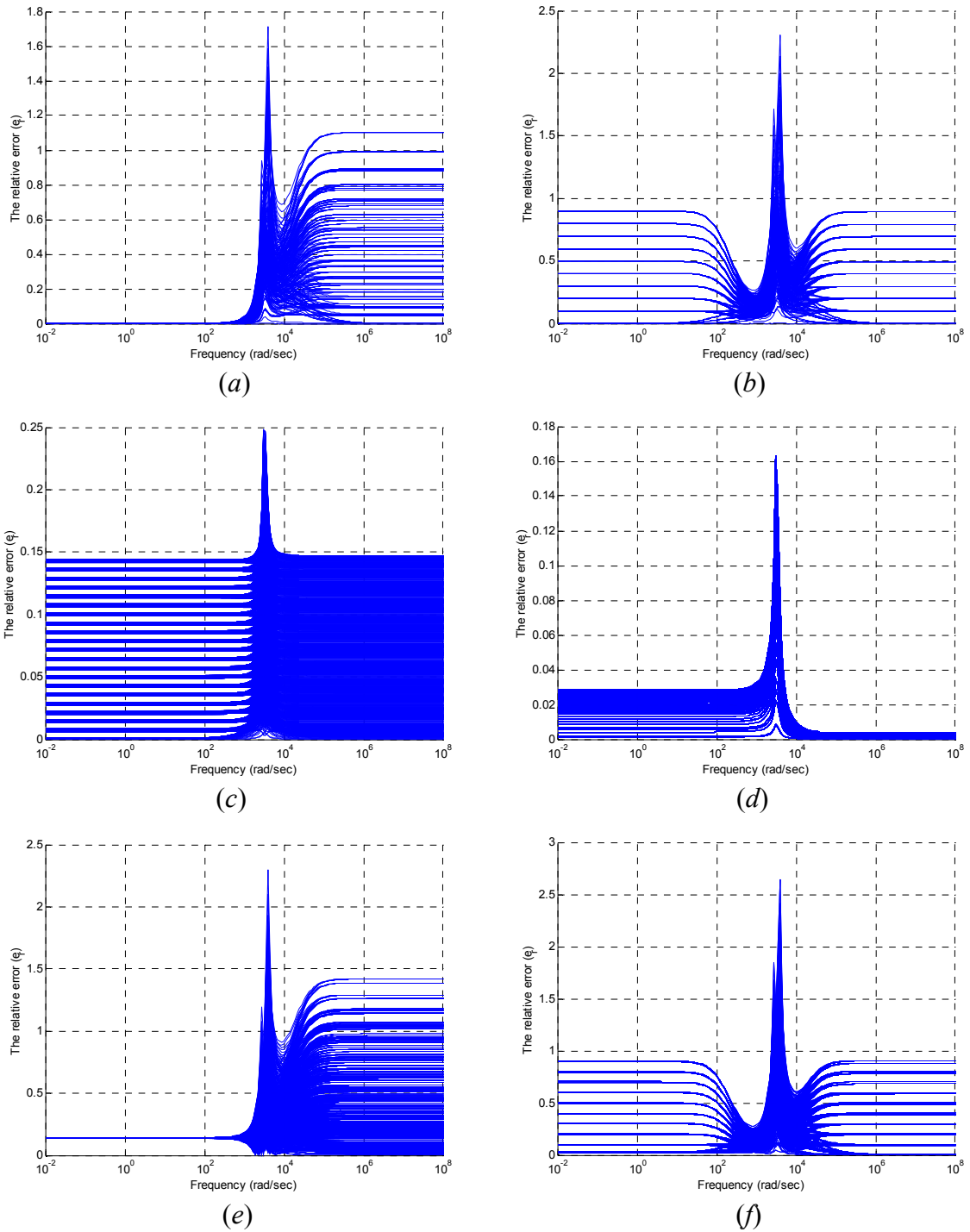


Fig. 3.3 – The relative errors' plots for a single buck converter operating in CICM with VMC (a) variations in power components for G_p , (b) for G_d , (c) variations in line source and load for G_p , (d) for G_d , (e) variations in power components, line source, and load for G_p , (f) for G_d .

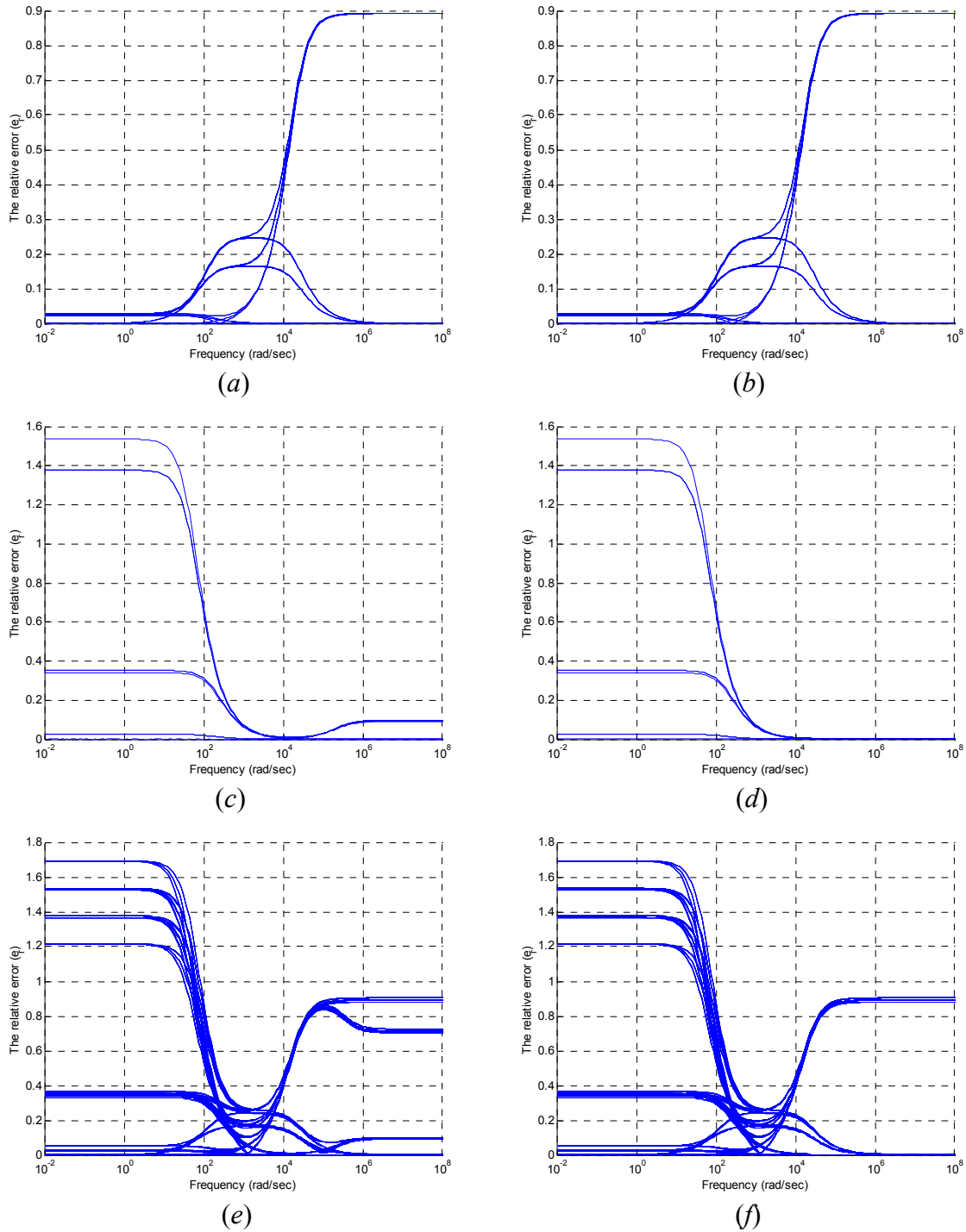


Fig. 3.4 – The relative errors' plots for a single buck converter operating in CICM with PCMC (a) variations in power components for G_p , (b) for G_d , (c) variations in line source and load for G_p , (d) for G_d , (e) variations in power components, line source, and load for G_p , (f) for G_d .

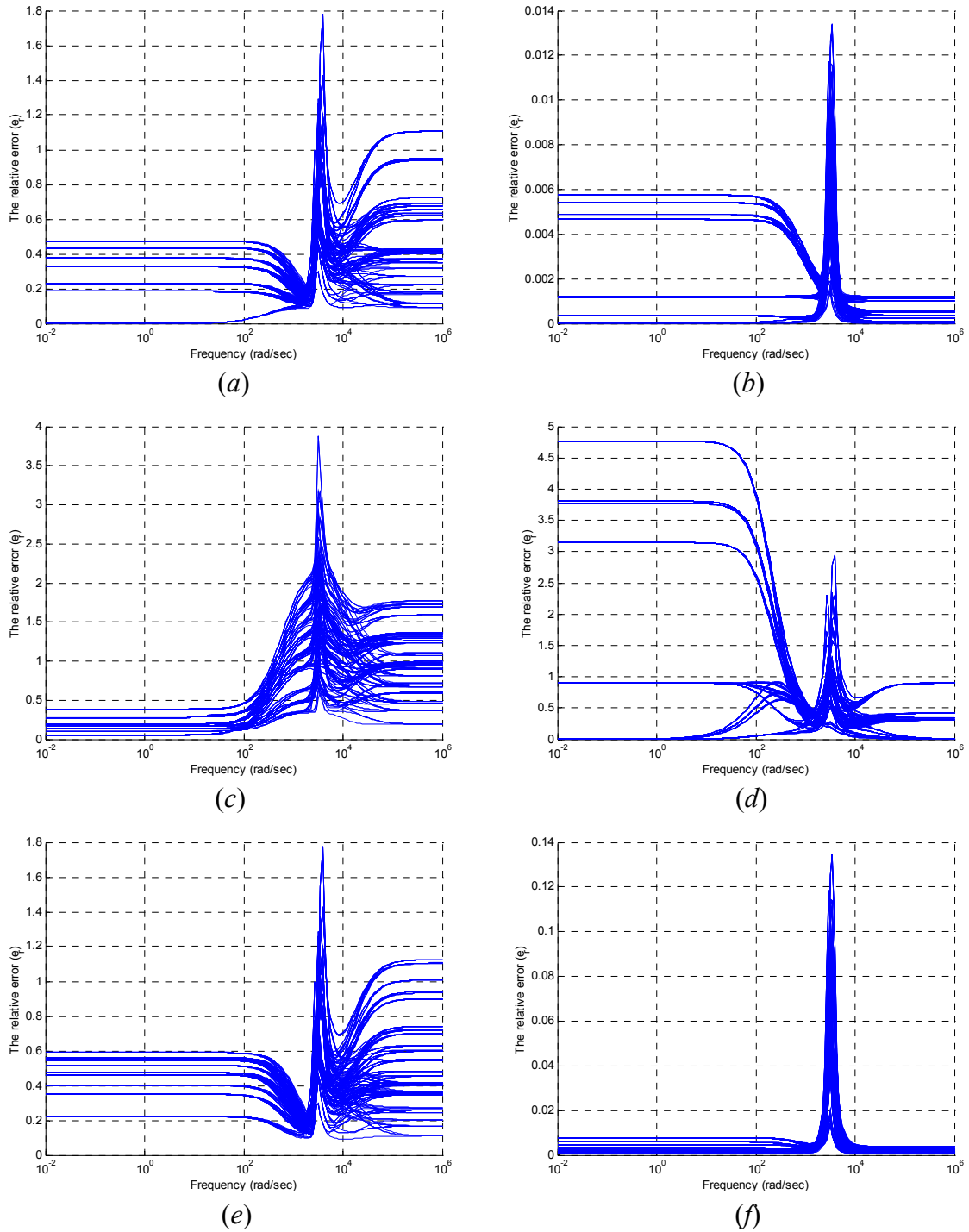


Fig. 3.5 – The relative errors' plots for two-buck converters connected in parallel and operating in CICM with VMC. The variations are only in power components, (a) for G_p , (b) for G_d , (c) for G_{pu} , (d) for G_{du} , (e) for G_{pi} , (f) for G_{di} .

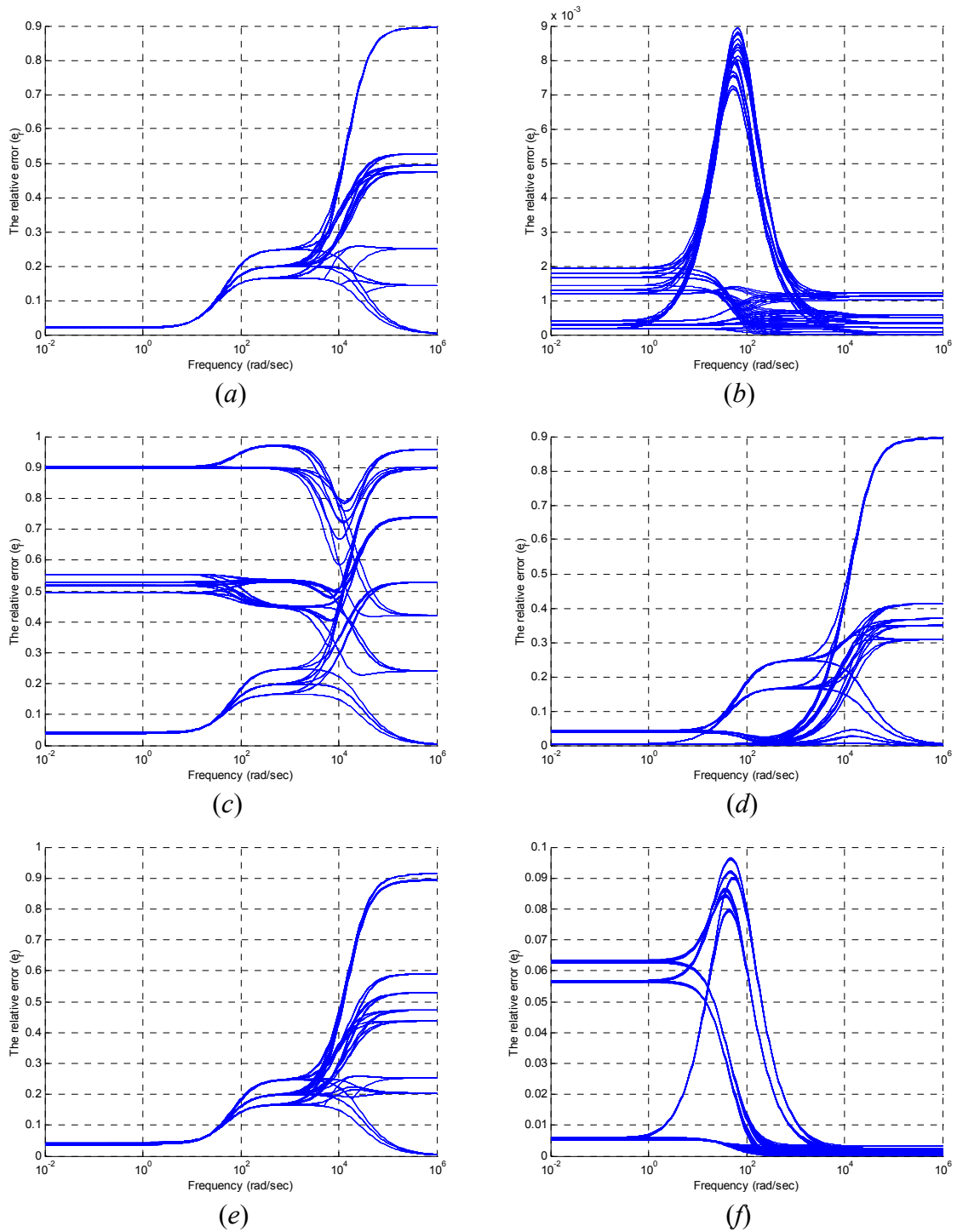


Fig. 3.6 – The relative errors' plots for two-buck converters connected in parallel and operating in CICM with PCMC. The variations are only in power components, (a) for G_p , (b) for G_d , (c) for G_{pu} , (d) for G_{du} , (e) for G_{pi} , (f) for G_{di} .

The graphical representations of uncertainties are presented in Fig. 3.3 and Fig. 3.4 for a single-buck converter with VMC and PCMC, respectively, and in Fig. 3.5 and Fig. 3.6 for two-buck converters with VMC and PCMC, respectively. If the \mathcal{H}_∞ -norm of relative error is more than unity, the influence of uncertain parameters on the system is greater than the nominal ones. From these graphs we can conclude the following remarks:

- The uncertain plant models' variations of a single-buck converter can be the same as of two-buck converters in parallel. However it is not for the uncertain disturbance models due to the common load that is used in both cases.
- The line source and load variations for a voltage-controlled-buck converter are much less than for a current-controlled buck converter and vice versa for the variations of power components. This is a consequence of the feed forward of input/inductor current, i_L , into the control circuit.
- In parallel-connected configuration, the uncertainty considering the variations of power components is much less when PCMC is used than when VMC, as can be seen by comparing Fig. 3.5 with Fig. 3.6. The reason is that the converters with VMC have been presented as a resonant system.
- In the case of two-loop approach, the voltage-loop is very sensitive to power component variations and more than in the single-loop approach.

3.2 Control Issues

3.2.1 Single Converter

The objective of the controller design is the robust stability for all members of the family of plants \mathcal{G} . Performance of the controller should also include set-point tracking, disturbance rejection, and suppression of measurement noise. It is well understood that the designer has to make a basic trade-off between the objectives of tracking and noise suppression. The performance of a closed loop system can be judged by its sensitivity and complementary sensitivity functions. The sensitivity function $S(s)$ relates the disturbances to the output, and the complementary sensitivity function $T(s)$ relates the set point to the output.

Considering the closed loop classical feedback system, as shown in Fig. 2.3, the sensitivity and complementary functions are defined as

$$S(s) = \frac{1}{1 + G_p K} \quad \text{and} \quad T(s) = \frac{G_p K}{1 + G_p K} \quad (3.11)$$

The \mathcal{H}_∞ optimal controller minimizes the ∞ -norm of the sensitivity function $S(s)$ weighted by $w_p(s)$.

$$\min_K \|S w_p\|_\infty = \min_K \sup_{\omega} |S w_p| \quad (3.12)$$

If the optimal controller K is designed with a particular $w_p(s)$, the sensitivity function bound should satisfy the following constraint.

$$|S(j\omega)| < |w_p(j\omega)|^{-1}, \quad \forall \omega \quad (3.13)$$

The bound $|w_p(j\omega)|^{-1}$ forces the sensitivity function to be small in the frequency range where large disturbances are anticipated. The nominal performance will be achieved, if $\|S w_p\|_\infty < 1$ for all ω . For robust stability, the complementary sensitivity $T(s)$ should be small in the frequency range where the model uncertainty measured by $w_i(s)$ is large, i.e., $\|T w_i\|_\infty < 1$ for all ω . Robust performance is achieved by satisfying both nominal performance and robust stability with some margin, i.e.,

$$|T w_i| + |S w_p| < 1 \text{ for all } \omega \quad (3.14)$$

3.2.2 Paralleled DC/DC Converters

A. For Single-Loop Approach

According to Fig. 2.5, the interconnection system transfer matrix from $[v_\Delta \ w \ c]^T$ to $[y_\Delta \ z \ e]^T$ can be written as

$$P(s) = \begin{bmatrix} P_{11} & P_{12} \\ P_{21} & P_{22} \end{bmatrix} = \left[\begin{array}{cc|c} P_{11_{11}} & P_{11_{12}} & P_{12_1} \\ P_{11_{21}} & P_{11_{22}} & P_{12_2} \\ \hline P_{21_1} & P_{21_2} & P_{22} \end{array} \right] \quad (3.15)$$

The general control configuration in Fig. 3.7(b), which is used for analysis procedure, is obtained by using a lower LFT (linear fractional transformation) of Fig. 3.7(a). The closed-loop transfer matrix from $[v_\Delta \ w]^T$ to $[y_\Delta \ z]^T$ can be written as

$$\begin{aligned} N = \mathcal{F}_l(P, K) &= P_{11} + P_{12} K (I - P_{22} K)^{-1} P_{21} \\ &= \begin{bmatrix} N_{11} & N_{12} \\ N_{21} & N_{22} \end{bmatrix} \end{aligned} \quad (3.16)$$

where $v_\Delta = [c_\Delta \ d_\Delta]^T$, $w = [r \ d \ n]^T$, $y_\Delta = [y_c \ y_d]^T$, and $z = [z_1 \ z_2]^T = [W_p(y - W_r r) \ W_u c]^T$.

To ensure good performance with a small input usage, i.e., z is small, we would like to have $\|N_{22}\|_\infty$ small, i.e., all the MIMO transfer function in equation (3.16) are small. The \mathcal{H}_∞ -

norm is defined as the maximum singular value over all frequencies, i.e., $\|\bullet\|_\infty = \sup_{\omega} \sigma_{\max} |\bullet|$.

The uncertain closed-loop transfer matrix F from w to z , which is presented in Fig. 2.5, is obtained by using an upper LFT

$$\begin{aligned} F &= \mathcal{F}_u(N, \Delta) = N_{22} + N_{21}\Delta(I - N_{11}\Delta)^{-1}N_{12} \\ &= \begin{bmatrix} -W_p S_o W_r & W_p S_o G_{dd} W_d & -W_p T_i W_n \\ W_c S_i K W_r & -W_c S_i K G_{dd} W_d & -W_c S_i K W_n \end{bmatrix} \end{aligned} \quad (3.17)$$

where the sensitivity and the complementary sensitivity matrices of the perturbed system are defined as

$$S_o = (I + G_{pp}K)^{-1} \text{ and } S_i = (I + KG_{pp})^{-1} \quad (3.18)$$

$$T_o = G_{pp}K(I + G_{pp}K)^{-1} \text{ and } T_i = (I + KG_{pp})^{-1}KG_{pp} \quad (3.19)$$

For robust stability, the system must remain stable for all plants in the uncertainty set. This should satisfy that $F(s)$ is stable for all Δ where $\|\Delta\|_\infty \leq 1$, which is equivalent to

$$\|N_{11}\|_\infty < 1 \text{ for all } \omega \quad (3.20)$$

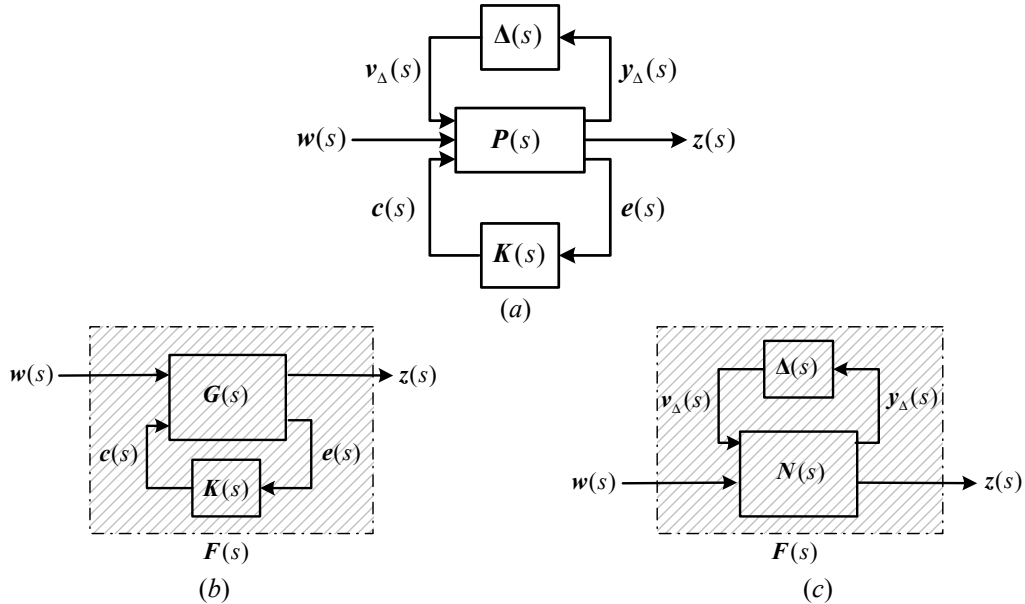


Fig. 3.7 – Configurations of control system. The general control system is used to design the controller and analyze the system in the presence of uncertainty (a). In designing of feedback controller we have to use the perturbed model (b), however, in analysis we have to consider the uncertainty for testing (c).

Robust performance is achieved if robust stability is satisfied and the transfer matrix from \mathbf{w} to \mathbf{z} is small for all plants in the uncertainty set, i.e.,

$$\|\mathbf{F}\|_{\infty} < 1 \text{ for all } \Delta \text{ where } \|\Delta\|_{\infty} \leq 1 \quad (3.21)$$

B. For Two-Loop Approach

According to Fig. 2.6, the control design procedure is first to design the voltage-loop and then the current-loop. Here we will design and analyze the robust control of the closed-loop system in Fig. 3.9, i.e., current-loop design. However, the same procedure has been applied to the closed-loop system in Fig 3.8, i.e., voltage-loop design.

From Fig. 3.9(a), \mathbf{P} is the nominal system, \mathbf{K}_u is the voltage-loop controller, \mathbf{K}_i is the current-loop controller, and the Δ is the uncertainty, which is presented as

$$\Delta \in \Delta \equiv \left\{ \Delta : \Delta = \text{diag} \{ \Delta_{p_u}, \Delta_{p_i} \}, \|\Delta\|_{\infty} \leq 1 \right\} \quad (3.22)$$

Using upper linear fractional transformation (upper-LFT), the system may be represented as in Fig. 3.9(b), where \mathbf{G} is the perturbed transfer matrix from \mathbf{w} and \mathbf{c} to \mathbf{z} and \mathbf{e} . This configuration is used to design the controller that stabilizes the system in presence of uncertainty. The closed-loop transfer matrix from $[\mathbf{v}_{\Delta} \ \mathbf{w}]^T$ to $[\mathbf{y}_{\Delta} \ \mathbf{z}]^T$ can be written in the form of a lower LFT, which is used to analyze the overall system.

$$\begin{aligned} \mathbf{N} = \mathcal{F}_l(\mathbf{P}, \mathbf{K}) &= \mathbf{P}_{11} + \mathbf{P}_{12} \mathbf{K} (\mathbf{I} - \mathbf{P}_{22} \mathbf{K})^{-1} \mathbf{P}_{21} \\ &= \begin{bmatrix} \mathbf{N}_{11} & \mathbf{N}_{12} \\ \mathbf{N}_{21} & \mathbf{N}_{22} \end{bmatrix} \end{aligned} \quad (3.23)$$

where $\mathbf{v}_{\Delta} = [\mathbf{c}_{\Delta_u} \ \mathbf{c}_{\Delta_i}]^T$, $\mathbf{w} = [\mathbf{r} \ \mathbf{d} \ \mathbf{n}_u \ \mathbf{n}_i]^T$, $\mathbf{y}_{\Delta} = [\mathbf{y}_{c_u} \ \mathbf{y}_{c_i}]^T$, and $\mathbf{z} = [\mathbf{z}_u \ \mathbf{z}_i]^T$.

To ensure good performance, we would like to have $\|\mathbf{N}_{22}\|_{\infty}$ small. The uncertain closed-loop transfer matrix $\mathbf{F}(s)$ from \mathbf{w} to \mathbf{z} is obtained by using an upper LFT

$$\mathbf{F} = \mathcal{F}_u(\mathbf{N}, \Delta) = \mathbf{N}_{22} + \mathbf{N}_{21} \Delta (\mathbf{I} - \mathbf{N}_{11} \Delta)^{-1} \mathbf{N}_{12} \quad (3.24)$$

For robust stability, the system must remain stable for all plants in the uncertainty set. This should satisfy that $\mathbf{F}(s)$ is stable for all Δ where $\|\Delta\|_{\infty} \leq 1$. Robust performance is achieved if robust stability is satisfied and the transfer matrix from \mathbf{w} to \mathbf{z} is small for all plants in the uncertainty set.

$$\|\mathbf{F}(s)\|_{\infty} < 1 \text{ for all } \Delta \text{ where } \|\Delta\|_{\infty} \leq 1 \quad (3.25)$$

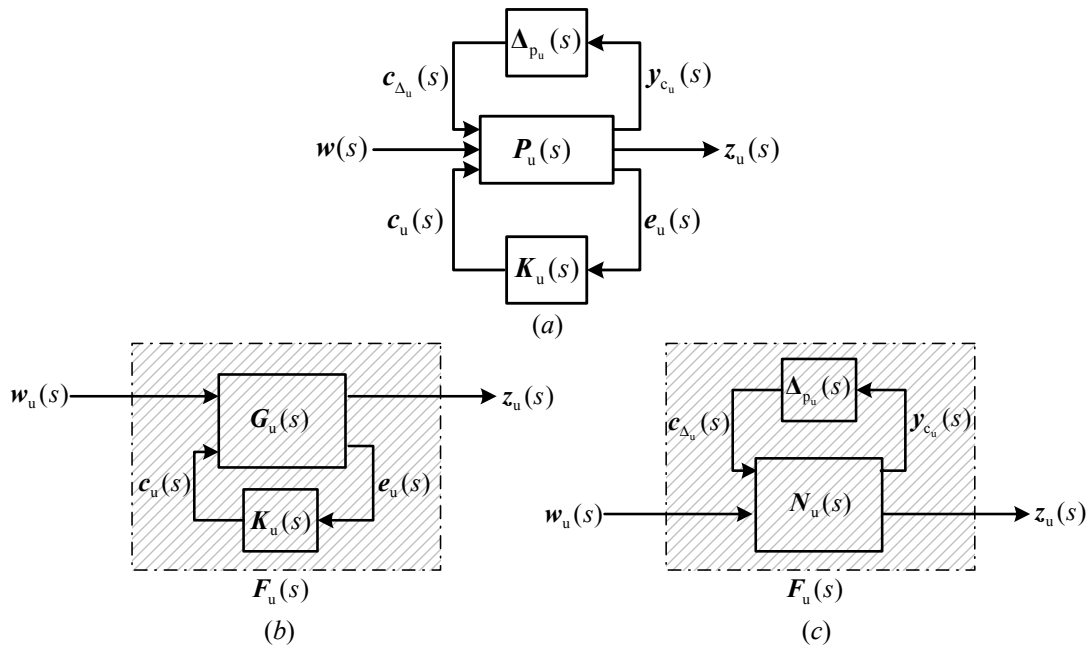


Fig. 3.8 - The general configurations are considered to design and analysis the voltage-loop control of paralleled DC/DC converters in the presence of uncertainty, (a) the general control configuration, (b), the perturbed model that is used to design a voltage-loop controller, (c) the closed-loop system that is used to analyze the voltage-loop in the presence of uncertainties.

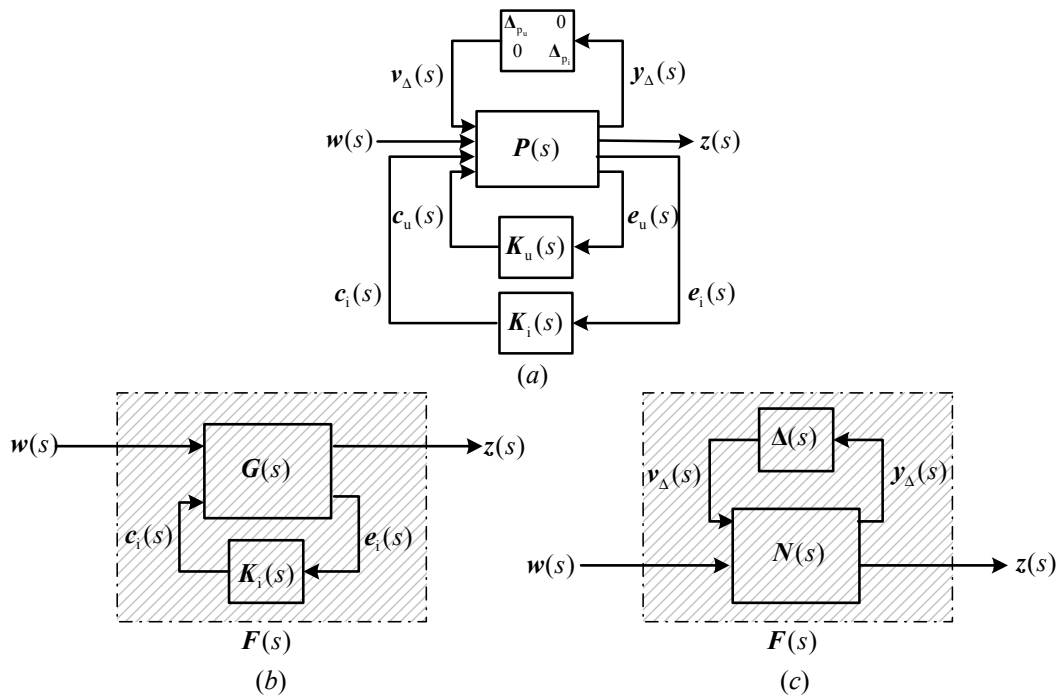


Fig. 3.9 - The general configurations are considered to design and analysis the current-loop control of paralleled DC/DC converters in the presence of uncertainty, (a) the general control configuration, (b) the perturbed model that is used to design a current-loop controller, (c) the closed-loop system that is used to analyze the overall system in the presence of uncertainties.

3.3 Quantitative Conversion of Power Electronics Specifications

In the next chapter the control design of DC/DC converters are developed under different specifications. The first part, i.e., when designing analogue and fuzzy overload controllers, can be quite understandable to power electronics designers due to using the specifications that are written in power electronics expressions. However, the last part, i.e., when using the robust control, may raise many questions, because the design specifications are expressed in robust control terms. In order to overcome these difficulties, the common specifications of power supply design in terms of robust control is presented in Table 3.1 where the contents is based on (Ridley, *et al.*, 1988) and (Skogestad and Postlethwaite, 1996).

TABLE 3.1 – The translation of power electronics specifications to robust control expressions

Power Electronics	▪ The power supply must be stable under all operating conditions of line and load			
Robust Control	SISO	$NS \Leftrightarrow S$ has all poles in LHP	MIMO	$NS \Leftrightarrow N$ has all poles in LHP (Internally stable)
Power Electronics	▪ Input-output noise transmission (audio susceptibility) must be less than a specified maximum. ▪ The settling time and peak overshoot of the dynamic response to a step-load change must be less than a specified maximum. ▪ The output must remain within a specified range for all operating conditions of line and load.			
Robust Control	SISO	$NP \Leftrightarrow w_p S < 1, \quad \forall \omega$	MIMO	$NP \Leftrightarrow \ N_{22}\ _\infty < 1, \quad \forall \omega$ and NS
Power Electronics	▪ The power supply must be stable under all operating conditions, with all possible component variations that may occur during the lifetime of the system.			
Robust Control	SISO	$RS \Leftrightarrow w_i T < 1, \quad \forall \omega$	MIMO	$RS \Leftrightarrow \ N_{11}\ _\infty < 1, \quad \forall \omega$ and NS
Power Electronics	▪ The output must remain within a specified range for all operating conditions, with all possible component variations that may occur during the lifetime of the system.			
Robust Control	SISO	$RP \Leftrightarrow w_p S + w_i T < 1, \quad \forall \omega$	MIMO	$RP \Leftrightarrow \ F\ _\infty < 1, \quad \forall \omega$ $\ \Delta\ _\infty < 1$ and $\ \hat{\Delta}\ _\infty < 1$ and NS

Chapter 4

Controller Design

4.1 PID-Control

In this section, the use of modified PID-algorithm to control DC/DC converters results in the desired output and provides satisfactory control. Modified PID controller is used to avoid the set-point kick phenomenon by applying the differentiation only on the output voltage but not on the reference voltage as described in (Åström and Hägglund, 1995) and (Ogata, 1997).

PID control is used in order to find the best control scheme that ensures the stability of the closed-loop system and at the same time satisfies the performance requirements. Additional information extracted from the simulation tools is exploited to securely tune the controller. The transfer function of the modified PID-controller can be written as

$$u_c(s) = K_p \left(bu_{\text{ref}}(s) - u_{\text{out}}(s) + \frac{1}{T_i s} (u_{\text{ref}}(s) - u_{\text{out}}(s)) - \frac{sT_d}{1 + sT_d/N} u_{\text{out}}(s) \right) \quad (4.1)$$

where the derivative part has been modified to prevent a large amplification of changes in the reference voltage.

A search for the best set of PID-parameters that gives the desired performance to the control loop is difficult and computationally expensive, see (Maffezzoni and Rocco, 1995). However, by achieving the performance requirements of the output voltage and inductor current, it is possible to find a set of PID-parameters that can be used as a first guess in optimization procedure in order to obtain optimum parameters for PID controller. This has been used in (Gadoura, *et al.*, 1998b) and (Gadoura, *et al.*, 1999b).

The optimal principle to control a Telecom rectifier is to use cascaded voltage/ current control as shown in Fig. 4.1 [P5], if the stringent noise requirements are to be met. The constant-voltage controller can be implemented by using ground referenced modified PID controller.

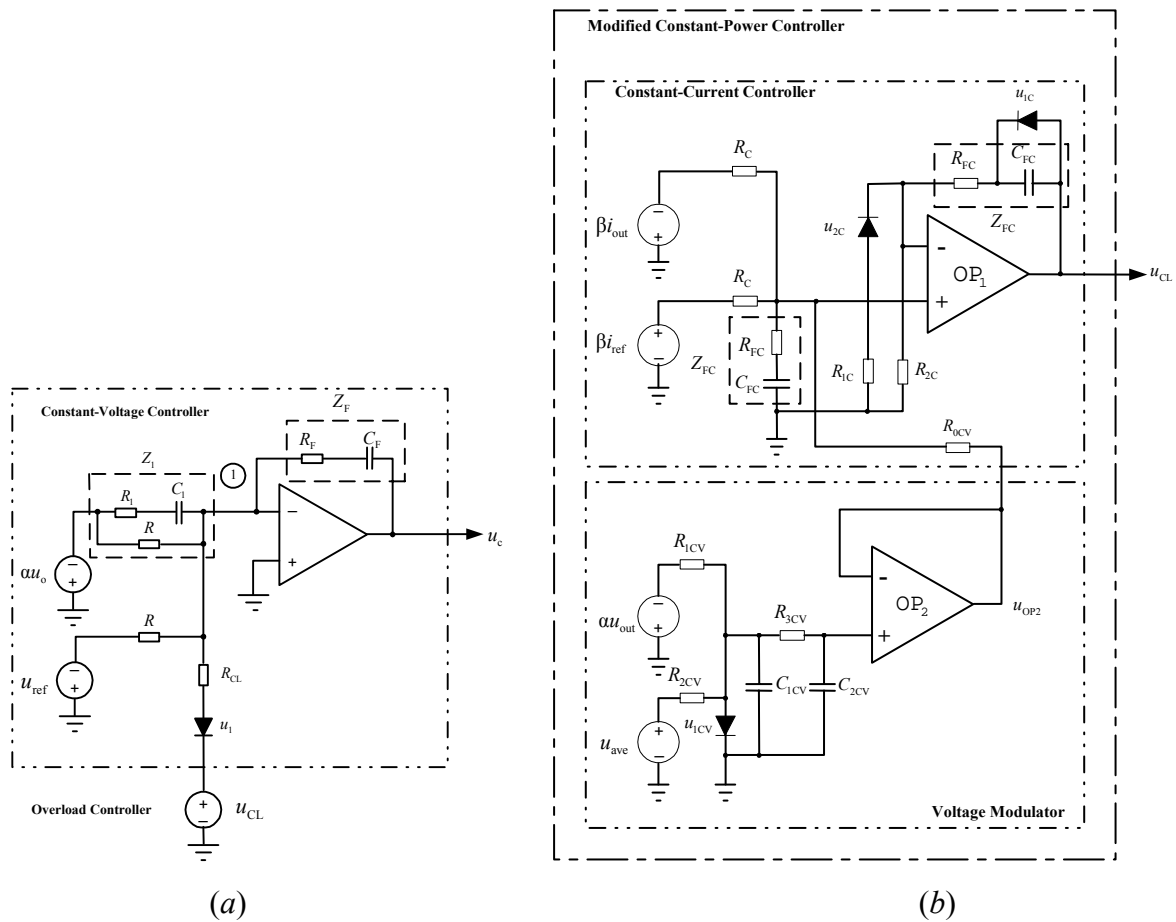


Fig. 4.1 – The practical analogue cascaded controller; (a) constant voltage controller, and (b) overload controller.

The modified derivative part is used to overcome the audio-susceptibility problems at CICM and DICM boundary and also to eliminate the overshoot when changing voltage reference. Because of the inverting amplifier principle of point 1, as shown in Fig. 4.1(a), it is easy to connect other controller actions to the constant-voltage controller in such a way that they are automatically called for or disconnected from the action by using a diode, e.g. u_1 , (Gadoura, *et al.*, 1999a).

The overload-protection controller can be implemented by using a constant-current controller, i.e. output current limiting, and voltage modulator as shown in Fig. 4.1(b). The modified output power limiting ($u_{out} \geq u_1$) is implemented by modulating the current reference by means of output voltage. The modulating signal must be filtered sufficiently to reduce the effect of positive feedback from output voltage.

The earlier mentioned mode-change points, Fig. 1.3, are stabilized by using a diode u_{2C} as shown in Fig. 4.1(b). The PI controller parameters are effectively modulated by the level of error signal. Integrating amplifiers tend to saturate when not at linear operating mode and cause delayed operation when called for action. This problem is corrected by changing the amplifier from PI to P mode by means a diode u_{1C} when the controller is not in active limiting

mode as shown in Fig. 4.1(b). The constant-current limiting ($u_{\text{out}} < u_2$) is implemented by saturating the modulation voltage u_{OP2} by means of diode $u_{1\text{CV}}$.

4.2 Fuzzy-Logic Control

Fuzzy-logic control (FLC) serves as an example of the more conventional controllers. The conventional controllers manage a complex control surface by reading sensor information, executing a mathematical model, and making changes to the device actuators. However, fuzzy-logic controllers manage this complex control surface through heuristics rather than a mathematical model (Cox, 1999). In addition, a fuzzy system is able to approximate, to any level of precision, any continuous linear or nonlinear function. FLC employs fuzzy sets to represent the semantic properties of each control and solution variable, and processes its input and output by using a set of fuzzy IF-THEN rules that associate an input value, through a collection of fuzzy sets, into a new output representation, (Wang, 1997).

4.2.1 Principles

The basic configuration of a fuzzy-logic controller (FLC) is shown in Fig. 4.2. The fuzzifier transforms a real-valued variable into a fuzzy set and the defuzzifier transforms a fuzzy set into a real-valued variable. The fuzzy rule base represents the collection of fuzzy IF-THEN rules. The fuzzy inference engine combines these fuzzy IF-THEN rules into a mapping from fuzzy sets in the input space Φ to fuzzy sets in the output space Θ based on fuzzy logic principles, (Reznik, 1997)

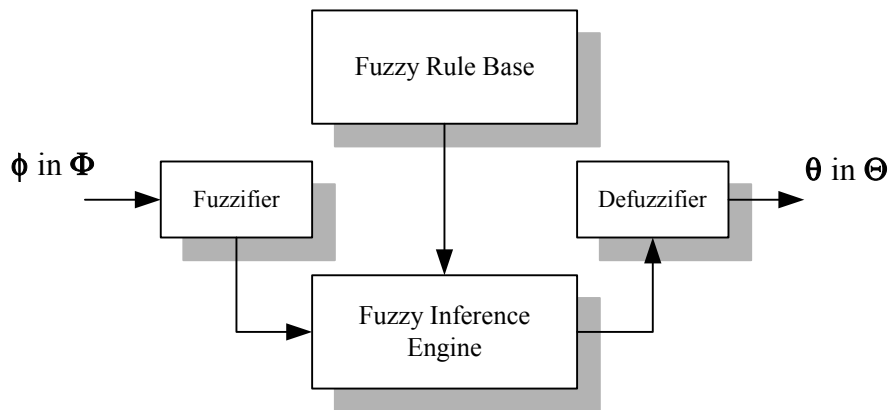


Fig. 4.2 - The basic configuration of fuzzy-logic controller that consists of three parts: fuzzifier converting the input to fuzzy sets, defuzzifier producing the crisp output, and fuzzy inference engine governing by fuzzy rules.

In the case of DC/DC converters, the derivation of the fuzzy rules is considered to improve the converter performances in terms of dynamic response and robustness and is based on the following criteria as partly presented in (Mattavelli, *et al.*, 1997) and (So, *et al.*, 1996):

1. When the output of the converter is far from the reference voltage, the change of control signal must be large to bring the output to the reference quickly.
2. When the output of the converter is moving closer the reference, the change of control signal is small.
3. When the output of the converter is near the reference and is moving closer to it rapidly, the control signal must be kept constant to prevent overshoot.
4. When the reference voltage is reached and the output voltage is still changing, the change of control signal is very small preventing the output from moving away.
5. When the reference voltage is reached and the output voltage is steady, the control signal is constant.
6. When the output voltage is above the reference voltage, the sign of the change of control signal must be negative and vice versa.

4.2.2 Constant Voltage Controller

The layout structure of fuzzy voltage controller is shown in Fig. 4.3, which is appropriate in order to avoid the difficulty of writing fuzzy rules for the integral part, (Jantzen, 1998) and (Yen and Langari, 1999).

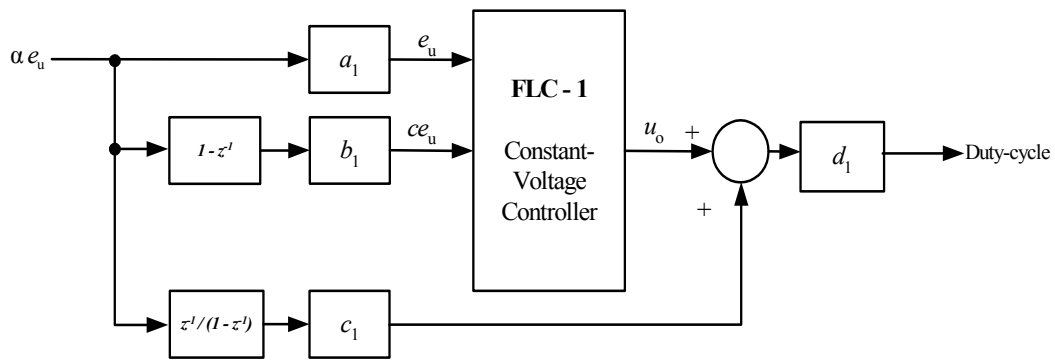


Fig. 4.3 - The structure of practical PID-like FLC. FLC-1 has two inputs; the error and its change. The output is added to the integral part.

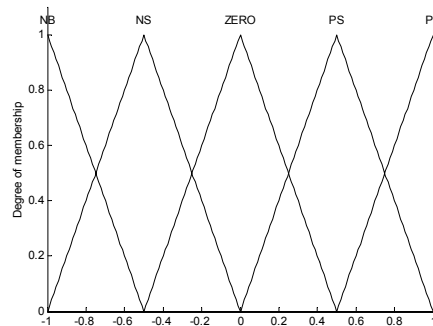


Fig. 4.4 - The membership functions of the inputs, e_u , e_i , ce_u , ce_i , and outputs, u_o , c_o , of both PID-like FLC and PI-like FLC.

The controller inputs are the output voltage error ' e_u ' and its derivative ' ce_u ' with gains a_1 , and b_1 , respectively. The integral part with gain c_1 is added to the controller output ' u_o ' with gain d_1 to generate the duty cycle that controls the operation of buck converter. As shown in Fig. 4.4, the fuzzy sets are defined for each input and output variable. Five linguistic terms, positive big, positive small, zero, negative small, and negative big, have been chosen for input and output variables in order to smooth the control action. By using scaling factors the value of each input and output variable is normalized in $[-1,1]$. The fuzzy rules can be derived in order to improve the converter performances in terms of dynamic response and robustness as shown in Table 4.1. The inferred output of each rule is generated using Mamdani's min fuzzy implication. The defuzzification operation is performed to obtain a crisp result from inferred results of all involved rules using the center of gravity method. Fig. 4.5 gives a graphical representation of Table 4.1.

TABLE 4.1 – The fuzzy rules of FLC that are used in both PID-like FLC and PI-like FLC

	ce					
e		PB	PS	Z	NS	NB
	PB	PB	PB	PB	Z	NS
	PS	PB	PS	PS	Z	NS
	Z	PS	Z	Z	Z	NS
	NS	PS	Z	NS	SN	NB
	NB	PS	Z	NB	NB	NB

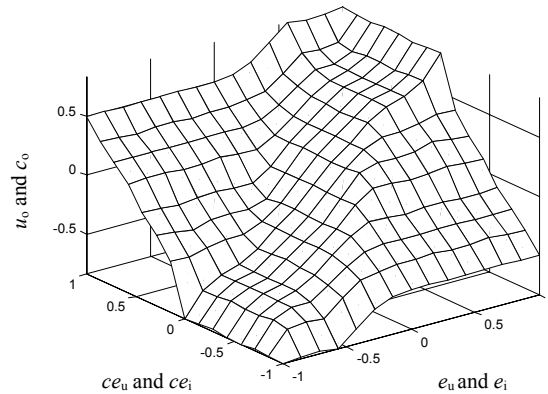


Fig. 4.5 – Graphical representation of Table 4.1. The output action (control command) shows to be smooth when the inputs change.

4.2.3 Overload Controller

The implemented structure of PI-like FLC is shown in Fig. 4.6. The controller inputs are modified output current error ' e_i ' and its change ' ce_i ' with gains a_2 and b_2 , respectively. The integration of the controller output ' c_o ' with gain d_2 will yield ' Δu_{ref} ', which is the required change at output voltage reference to follow the presented output characteristics, Fig. 1.3, at

overload. Fuzzy sets are defined for each input and output variable. Five linguistic terms are chosen as in the case of constant-voltage controller. The input variables are scaled to $[-1,1]$ by means of gains a_2 and b_2 . The output variable is limited to $[0,-60]$ in order to ensure operation down to short circuit. Also the fuzzy rules are the same as those have been used in constant-voltage controller. The PI-like FLC in Fig. 4.6 is almost the same configuration of PD-like FLC except for the integrator on the output, (Jantzen, 1998).

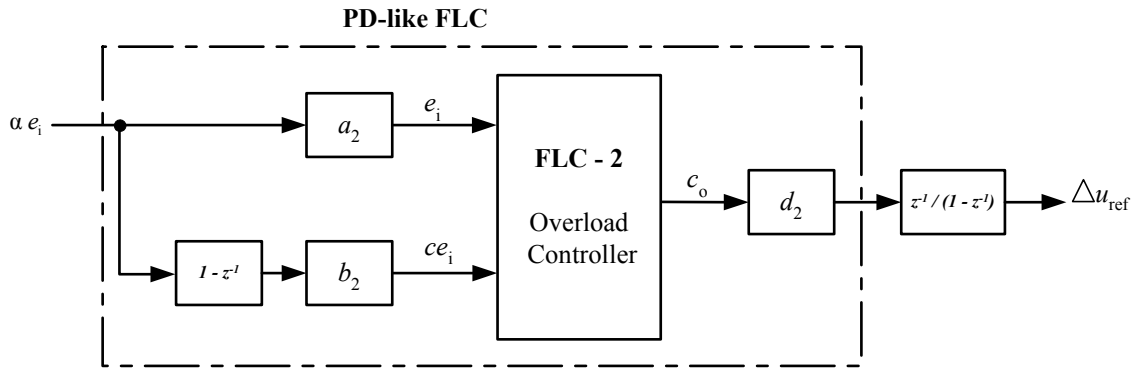


Fig. 4.6 - The structure of fuzzy overload controller, which is a PD-like FLC with an integrator on its output.

4.2.4 Tuning Procedure of PID-like FLC

The tuning procedure of PID-like FLC that is used in [P6] can be simplified as follows, as proposed in (Jantzen, 1998):

1. Use the PID parameters that are obtained by using Kappa-Tau tuning rules as presented in (Gadoura, *et al.*, 1999b).
2. Replace the summation in PID-controller, as shown in Fig. 4.3, by fuzzy controller, which has the following structure:
 - It has two inputs that are an error and change in error, and one output.
 - Five memberships are chosen for input and output variables, PB, PS, Z, NS, and NB, in order to smooth the control action.
 - Create the fuzzy rules, as shown in Table 4.1, in order to improve the converter output performance and based on the criteria that is presented in Section 4.2.1.
3. Normalize all values of input and output variables by using the gains, a_1 , b_1 , c_1 , and d_1 .
 - $a_1 d_1 = P = K_p$, so that $d_1 = \frac{K_p}{a_1}$.
 - $b_1 d_1 = D = K_p T_d$, so that $b_1 = a_1 T_d$.
 - $c_1 d_1 = I = \frac{K_p}{T_i}$, so that $c_1 = \frac{a_1}{T_i}$.
4. The same procedure can be utilized to tune PI-like FLC, which is shown in Fig. 4.6.

4.3 Internal-Model Control

4.3.1 Principles

The simplicity of the IMC controller structure depends on two assumptions, as presented in (Morari and Zafiriou, 1989). Firstly, the relationship between the conventional feedback control structure and IMC structure can be defined as

$$K(s) = \frac{G_f(s)G_c(s)}{1 - G_f(s)G_c(s)G_m(s)} = \frac{G_{imc}(s)}{1 - G_{imc}(s)G_m(s)} \quad (4.2)$$

which is inside the dashed line in Fig. 4.7. Secondly, we can assume that the internal model transfer function $G_m(s)$ is equal to the control-to-output transfer function $G_p(s)$, which is the case of a perfect model. Therefore, the closed-loop transfer function can be defined as

$$u_{out}(s) = G_f(s)G_c(s)G_p(s) u_{ref}(s) \quad (4.3)$$

The model shall be factorized into an all-pass portion $G_m^+(s)$ and a minimum-phase portion $G_m^-(s)$, i.e. $G_m(s) = G_m^+(s) G_m^-(s)$. $G_m^+(s)$ includes the right half-plane zero, in the case of boost and buck-boost converters, and is equal to one, in the case of the buck converter. The controller shall be defined as $G_f(s)G_c(s) = G_f(s)G_m^{-1}(s)$, where $G_f(s)$ is a low-pass filter and, in general, has the form $G_f(s) = 1/(\lambda s + 1)^h$, where h is an integer to guarantee that the controller $G_f(s)G_c(s)$ is proper, and λ is a tuning parameter that is used to ensure the stability condition of the system, (Rivera, *et al.*, 1986)

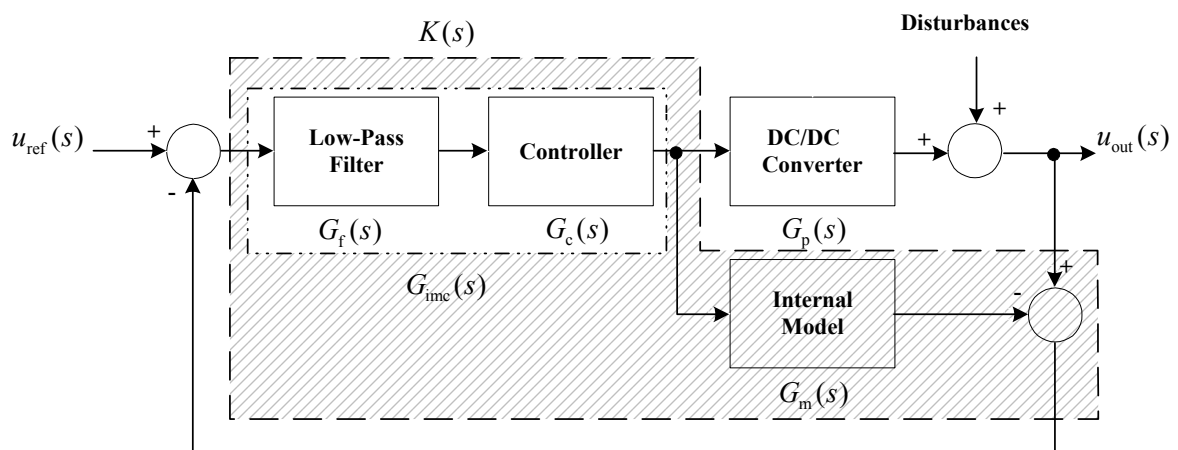


Fig. 4.7 - The internal-model control scheme for DC/DC converter and its equivalent in classical feedback control. $G_p(s)$ is usually $G_{co}(s)$.

4.3.2 Design Procedure

The IMC controller for DC/DC converter can be summarized as follows.

1. Let $G_m(s) = G_p(s)$, which means that the model is perfect.
2. Factorize the internal model as $G_m(s) = G_m^+(s) G_m^-(s)$. For example the control-to-output transfer function of the buck converter is of a minimum phase then $G_m^+(s) = 1$ and $G_m^-(s) = G_p(s)$.
3. Specify the controller as $G_c(s) = G_m^{-1}(s) = G_p^{-1}(s)$.
4. The simple filter design $G_f(s) = 1/(\lambda s + 1)$ can be used, which is enough to guarantee that $G_f(s) G_c(s)$ is proper.

Also we can obtain a digital IMC-based controller that can be implemented on digital signal processors (DSPs), by discretizing the transfer functions of internal model controller in Fig. 4.7 using one of suitable approximation methods, see (Åström and Wittenmark, 1997) and (Ogata, 1987).

4.3.3 \mathcal{H}_∞ Control Ensuring RS & RP

In this section, the design procedure based on \mathcal{H}_∞ optimization criterion to achieve robust performance and robust stability using the IMC structure is presented. The controller design steps are derived on the basis of the stability and performance objectives discussed in the previous section.

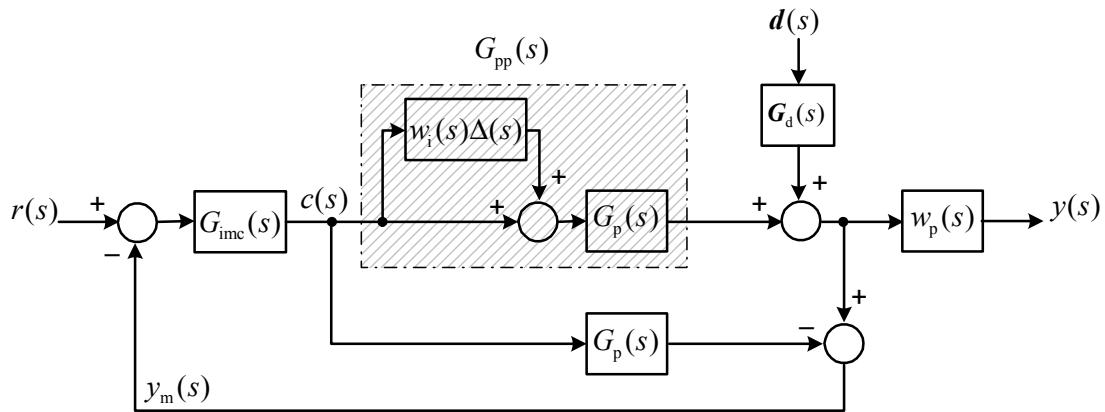


Fig. 4.8 - The IMC structure including uncertainty model. The internal model $G_m(s)$ is assumed to be the same as the nominal plant model $G_p(s)$.

A. The IMC Structure

The IMC structure is shown in the block diagram of Fig. 4.8 where $G_{pp}(s)$ denotes the perturbed plant model, $G_p(s)$ is the nominal model, and $G_{imc}(s)$ is the IMC controller. The feedback signal for this case is given as

$$y_m = (G_{pp}(s) - G_p(s))c + G_d(s)d \quad (4.4)$$

If the model is exact and there is no disturbance, then there is no feedback. Intuitively, with perfect modeling and no disturbance, an open loop system will perform well. The feedback signal y_m expresses the plant uncertainty and disturbances. The IMC structure can provide a feed-forward type of control when there is perfect modeling and will also handle disturbances and uncertainties through feedback.

The IMC structure is internally stable if and only if both plant $G_p(s)$ and controller $G_{imc}(s)$ are stable when the model is perfect, (Morari and Zafiriou, 1989).

B. Performance of IMC

For the IMC structure shown in Fig. 4.8, the input-output relation is given as

$$y = \underbrace{\frac{G_{imc} G_{pp}}{1 + G_{imc} (G_{pp} - G_p)}}_{T(s)} r + \underbrace{\frac{1 - G_{imc} G_p}{1 + G_{imc} (G_{pp} - G_p)}}_{S(s)} G_d d \quad (4.5)$$

When the plant model is exact, S and T reduce to

$$S(s) = 1 - G_{imc} G_p \text{ and } T(s) = G_{imc} G_p \quad (4.6)$$

The sensitivity function is a direct indicator of performance. This can be made zero by choosing the controller $G_{imc}(s) = G_p^{-1}(s)$. This would imply the perfect control. However, from the equivalent classical controller, $K(s) = \infty$, which implies that perfect control is practically impossible.

C. IMC Design Procedure

The design procedure is a two-step approach, which has no inherent optimality characteristics but should provide a good engineering approximation to the optimal solution.

\Rightarrow *Nominal Performance:*

The controller $G_{imc}(s)$ is first selected to yield a good system response for the inputs of interest for the case when $G_{pp} = G_p$. Generally $G_{imc}(s)$ is designed by minimizing

$$\|S w_p\|_{\infty} = \|(1 - G_{imc} G_p) w_p\|_{\infty} < 1 \text{ for all } \omega \quad (4.7)$$

\Rightarrow *Robust Stability and Performance:*

At high frequencies when the multiplicative uncertainty bound $|w_i|$ exceeds unity, $T(s)$ has to be rolled off. Therefore $G_c(s)$ is augmented by a low pass filter $G_f(s)$. The order of $G_f(s)$ is

such that $G_{\text{imc}}(s)$ becomes proper and its roll-off frequency is low enough to satisfy the robust stability constraint

$$\|T w_i\|_{\infty} = \|G_{\text{imc}} G_p w_i\|_{\infty} < 1 \text{ for all } \omega \quad (4.8)$$

The controller parameter is selected to meet the following performance specification:

$$|T w_i| + |S w_p| < 1 \text{ for all } \omega \quad (4.9)$$

Note that the nominal model of either boost or buck-boost converter is factorized into all pass portion G_p^+ and a minimum phase portion G_p^- , i.e. $G_p = G_p^+ G_p^-$. All pass portion includes a RHP-zero of the nominal model where $|G_p^+| = 1$ for all ω .

$$G_p^+(s) = \frac{-s + z}{s + z^H} \quad (4.10)$$

where the superscript H denotes complex conjugate. The controller $G_{\text{imc}}(s)$ can be written as

$$G_{\text{imc}}(s) = G_f(s) G_c(s) = G_f(s) G_p^-(s) \quad (4.11)$$

In case of single unit of buck, boost, or buck-boost converter, a first-order filter is quite enough ($h = 1$). The filter parameter λ is adjusted to meet robust stability and robust performance.

4.4 FEEDBACK CONTROL for Paralleled DC/DC Converters

There are many reasons to use feedback control. By designing a feedback controller, the effect of noise and disturbances can be reduced. Also the command signal tracking can be improved. Another use of feedback control is the reduction of the effects of plant uncertainty. The mathematical models that are used to describe the plant dynamics are “*never*” perfect. A feedback controller can be designed to maintain stability of the closed-loop system, i.e., robust stability, and to achieve an acceptable level of performance in the presence of uncertainties in the plant description, i.e., robust performance.

4.4.1 PI/PID Control

A. Voltage-Loop Design

The PID controller has been chosen to regulate the voltage-loop in order to achieve robust output voltage in spite of line and load disturbances. Recalling equation (2.23) each voltage-loop of each converter can be designed separately, which means that the control design of one-buck converter, as presented explicitly in (Gadoura, 1999), can be utilized in this stage.

As long as the paralleled buck converters are identical, the control design procedure of one-buck converter can be duplicated for other converters. In general, a good literature of the tuning rules of PID controller are studied and discussed in (Åström and Häggglund, 1995). The PID controllers are designed to achieve the robust stability and robust performance of the voltage-loop that should, according to Fig. 2.6 and Fig. 3.8, satisfy the following:

$$\text{RS} \Leftrightarrow F_u(s) \text{ is internally stable} \quad (4.12)$$

$$\text{RP} \Leftrightarrow \|F_u(s)\|_\infty < 1 \text{ for all } \Delta_{p_u} \text{ where } \|\Delta_{p_u}\|_\infty \leq 1 \quad (4.13)$$

B. Current-Loop Design

The PI controller, which is k_j in equation (1.3), has been selected to equalize the output current of each converter to the current reference. After designing the voltage-loop of each converter and according to Fig. 3.9, the PI controllers are tuned to achieve the robust stability and robust performance of the overall system.

$$\text{RS} \Leftrightarrow F(s) \text{ is internally stable} \quad (4.14)$$

$$\text{RP} \Leftrightarrow \|F(s)\|_\infty < 1 \text{ for all } \Delta \text{ where } \|\Delta\|_\infty \leq 1 \quad (4.15)$$

4.4.2 \mathcal{H}_∞ Optimal Control

Consider the standard setup of Fig. 3.7(b) for synthesis procedure, which is obtained by using an upper LFT of Fig. 3.7(a) as follows.

$$\begin{aligned} G = \mathcal{F}_u(P, \Delta) &= P_{22} + P_{21}\Delta(I - P_{11}\Delta)^{-1}P_{12} \\ &= \begin{bmatrix} G_{11} & G_{12} \\ G_{21} & G_{22} \end{bmatrix} \end{aligned} \quad (4.16)$$

where $G_{22}(s)$ is the transfer matrix from c to e , i.e., the nominal plant model. The minimal realization of $G(s)$ can be written as follows.

$$\dot{x} = A_p x + B_{p1} w + B_{p2} c, \quad y = C_{p2} x + D_{p21} w + D_{p22} c, \quad \text{and} \quad z = C_{p1} x + D_{p11} w + D_{p12} c$$

$$G(s) = \left[\begin{array}{c|c} A_p & B_p \\ \hline C_p & D_p \end{array} \right] = \left[\begin{array}{c|cc} A_p & B_{p1} & B_{p2} \\ \hline C_{p1} & D_{p11} & D_{p12} \\ C_{p2} & D_{p21} & D_{p22} \end{array} \right] \quad (4.17)$$

Also the minimal realization of a stabilizing controller can be written as follows

$$\dot{x}_K = A_K x_K + B_K y \quad \text{and} \quad c = C_K x_K + D_K y$$

$$\mathbf{K}(s) = \left[\begin{array}{c|c} \mathbf{A}_K & \mathbf{B}_K \\ \hline \mathbf{C}_K & \mathbf{D}_K \end{array} \right] \quad (4.18)$$

It can be concluded from the previous equations that the state-space representation of the controlled system can be defined as:

$$\begin{bmatrix} \dot{\mathbf{x}} \\ \dot{\mathbf{x}}_K \end{bmatrix} = \mathbf{A}_{cl} \begin{bmatrix} \mathbf{x} \\ \mathbf{x}_K \end{bmatrix} + \mathbf{B}_{cl} \mathbf{w} \quad \text{and} \quad \mathbf{z} = \mathbf{C}_{cl} \begin{bmatrix} \mathbf{x} \\ \mathbf{x}_K \end{bmatrix} + \mathbf{D}_{cl} \mathbf{w}$$

$$\text{where } \mathbf{A}_{cl} = \left[\begin{array}{c|c} \mathbf{A}_p + \mathbf{B}_{p2} \mathbf{D}_K (\mathbf{I} - \mathbf{D}_{p22} \mathbf{D}_K)^{-1} \mathbf{C}_{p2} & \mathbf{B}_{p2} \mathbf{C}_K + \mathbf{B}_{p2} \mathbf{D}_K (\mathbf{I} - \mathbf{D}_{p22} \mathbf{D}_K)^{-1} \mathbf{D}_{p22} \mathbf{C}_K \\ \hline \mathbf{B}_K (\mathbf{I} - \mathbf{D}_{p22} \mathbf{D}_K)^{-1} \mathbf{C}_{p2} & \mathbf{A}_K + \mathbf{B}_K (\mathbf{I} - \mathbf{D}_{p22} \mathbf{D}_K)^{-1} \mathbf{D}_{p22} \mathbf{C}_K \end{array} \right]$$

Closed-loop \mathbf{A} -matrix

(4.19)

By setting $\mathbf{w} = 0$ and assuming that either $\mathbf{D}_{p22} = 0$ or $\mathbf{D}_K = 0$, i.e., \mathbf{G}_{22} or \mathbf{K} is strictly proper, the interconnection in Fig. 3.7(c) is well posed, (Dullerud and Paganini, 2000). Therefore, the state-space representation of the controlled system can be reduced to:

$$\begin{bmatrix} \dot{\mathbf{x}} \\ \dot{\mathbf{x}}_K \end{bmatrix} = \underbrace{\left[\begin{array}{c|c} \mathbf{A}_p + \mathbf{B}_{p2} \mathbf{D}_K \mathbf{C}_{p2} & \mathbf{B}_{p2} \mathbf{C}_K \\ \hline \mathbf{B}_K \mathbf{C}_{p2} & \mathbf{A}_K \end{array} \right]}_{\text{Closed-loop } \mathbf{A}\text{-matrix}} \begin{bmatrix} \mathbf{x} \\ \mathbf{x}_K \end{bmatrix} \quad (4.20)$$

The closed-loop system is said to be internally stable if $(\mathbf{I} - \mathbf{D}_{p22} \mathbf{D}_K)$ is invertible and the closed-loop \mathbf{A} -matrix is stable, i.e., all its eigenvalues have negative real part, (Dullerud and Paganini, 2000). The \mathcal{H}_∞ -optimal control problem is to compute an internally stabilizing controller \mathbf{K} that minimizes $\|\mathbf{G}\|_\infty$. The following conditions guarantee the existence of an optimal controller \mathbf{K} , (Skogestad and Postlethwaite, 1998) and (Zhou and Doyle, 1998):

- $(\mathbf{A}_p, \mathbf{B}_{p2})$ is stabilizable and $(\mathbf{C}_{p2}, \mathbf{A}_p)$ is detectable. This is necessary and sufficient for existence of an internally stabilizing controller.
- \mathbf{D}_{p12} has full column rank to ensure that the control signal \mathbf{c} is fully weighted in the output \mathbf{z} . And \mathbf{D}_{p21} has full row rank to ensure that the input signal \mathbf{w} fully corrupts the measured signal \mathbf{e} .
- $\left[\begin{array}{c|c} \mathbf{A}_p - j\omega \mathbf{I} & \mathbf{B}_{p2} \\ \hline \mathbf{C}_{p1} & \mathbf{D}_{p12} \end{array} \right], \left[\begin{array}{c|c} \mathbf{A}_p - j\omega \mathbf{I} & \mathbf{B}_{p1} \\ \hline \mathbf{C}_{p2} & \mathbf{D}_{p21} \end{array} \right]$ have full column and row rank, respectively for all ω that means there are no imaginary axis zeros in the cross systems from \mathbf{c} to \mathbf{z} and from \mathbf{w} to \mathbf{e} .

Under these assumptions, the MatlabTM command *hinfsyn* computes the optimal controller searching for minimum γ that guarantees the existence of a controller, i.e., $\|G\|_\infty < \gamma$, see (Balas, *et al.*, 1998). Once more the \mathcal{H}_∞ controller equations are not presented here, however, the reader is referred to, e.g., (Skogestad and Postlethwaite, 1996).

4.4.3 \mathcal{H}_∞ Loop Shaping Design

According to Fig. 4.9, the stabilization problem of a perturbed plant G_{pp} is clearly declared in terms of a normalized left coprime factorization.

$$G_{pp} = (M_{cf} + \Delta_M)^{-1} (N_{cf} + \Delta_N) \quad (4.21)$$

where Δ_M and Δ_N are stable transfer matrices, which represent the uncertainty in the nominal plant model G_p . In addition, $G_p = M_{cf}^{-1} N_{cf}$.

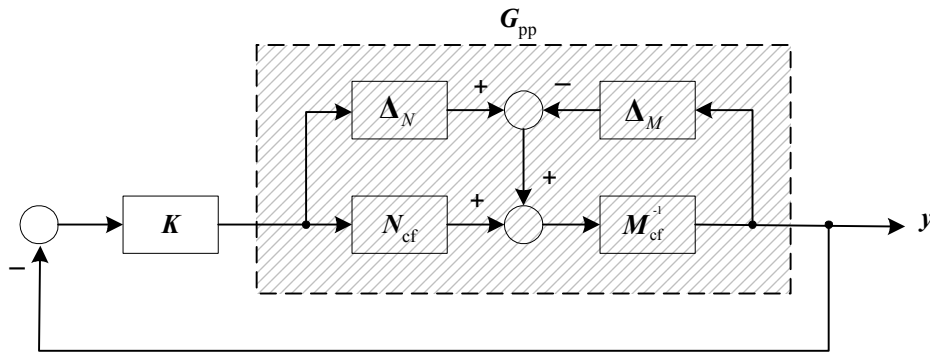


Fig. 4.9 – The left coprime factorization of the perturbed plant model G_{pp} . It is used to ensure the robust stabilization of the system.

The main objective of robust stabilization is to stabilize a class of perturbed plant model defined by

$$\mathcal{G}_\varepsilon = \left\{ (M_{cf} + \Delta_M)^{-1} (N_{cf} + \Delta_N) : [\Delta_M \quad \Delta_N] \in \mathcal{RH}^\infty, \left\| [\Delta_M \quad \Delta_N] \right\|_\infty < \varepsilon \right\} \quad (4.22)$$

where $\varepsilon > 0$ is the stability margin. The robust stability of the perturbed system is guaranteed with lowest achievable value of γ_{\min} , if and only if the nominal system is stable and

$$\gamma_{\min} = \left\| \begin{bmatrix} K \\ I \end{bmatrix} (I - G_p K)^{-1} M_{cf}^{-1} \right\|_\infty = 1/\varepsilon_{\max} \quad (4.23)$$

It is shown in (McFarlane and Glover, 1990) and (Skogestad and Postlethwaite, 1996) that this problem reduces to Nehari extension problem

$$\gamma_{\min} = \left\{ I - \left\| \begin{bmatrix} N_{cf} & M_{cf} \end{bmatrix} \right\|_H^2 \right\}^{-1/2} = (I + \rho(XZ))^{1/2} \quad (4.24)$$

where $\| \cdot \|_H$ denotes Hankel norm, ρ denotes the spectral radius, and Z and X are the unique positive definite solutions of two algebraic Riccati equations for minimal state-space realization of G_{pp} . It is important to emphasize that since we can compute γ_{\min} by solving just two Riccati equations, the γ -iteration can be avoided to solve the \mathcal{H}_∞ problem.

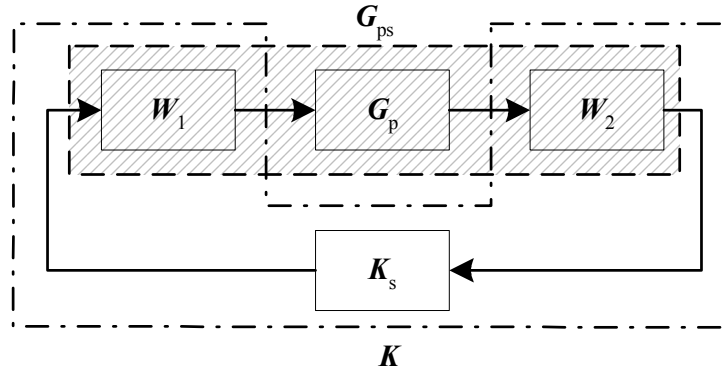


Fig. 4.10 – The shaped plant that is used to synthesis to find an optimal \mathcal{H}_∞ controller, K_s . The weights should be compensated with the \mathcal{H}_∞ controller to result the final controller, K .

In practice solving robust stabilization alone cannot specify the performance requirements as mentioned in (Skogestad and Postlethwaite, 1996). However the pre- and post-compensators are used to shape the open-loop singular values of the plant prior to robust stabilization the shaped plant.

$$G_{ps} = W_2 G_p W_1 \quad (4.25)$$

where W_1 and W_2 are the pre- and post-weighting functions respectively as shown in Fig. 4.9. The controller K_s is synthesized by solving the robust stabilization problem for the shaped plant G_{ps} with a normalized left coprime factorization. The final controller for the perturbed plant model G_{pp} can be obtained.

$$K = W_1 K_s W_2 \quad (4.26)$$

Finally the \mathcal{H}_∞ loop-shaping design procedure offers some advantages. The \mathcal{H}_∞ loop-shaping design is based on classical loop-shaping ideas that made it easy to use. Also it gives the closed formula of the \mathcal{H}_∞ optimal cost, γ_{\min} , that corresponds to a maximum stability margin, ε_{\max} , where the γ -iteration is not needed in the solution.

Chapter 5

Design Examples

Different design examples are discussed in this chapter to verify the control design procedures presented in the thesis. The Matlab™/Simulink™ is used as a setup platform for simulation. Especially the Control System Toolbox™, Fuzzy Logic Toolbox™, and μ -Analysis and Synthesis Toolbox™ have been used in the control design.

5.1 One-unit Configuration

Occasionally, a one-unit DC/DC converter is treated as a SISO system when a classical control design, such as PID control, is used. However, it has a multivariable nature due to the external inputs, so that it should be considered as a MIMO system in order to design modern (robust) control algorithm for it.

5.1.1 Fuzzy-logic Control Design

Considering the following specifications of a buck converter: input voltage $u_{in,0} = 140$ V, output voltage $u_{out,0} = 54$ V, max. output power $P_o = 500$ W, switching frequency $f_s = 100$ kHz, inductance $L = 100$ μ H, capacitance $C = 1000$ μ F, output resistance $R = 11$ Ω , equivalent series resistance of capacitor $r_C = 50$ m Ω , equivalent series resistance of inductor $r_L = 15$ m Ω . The PID-controller parameters are $K_p = 12.665$, $T_i = 7.49 \times 10^{-4}$ s, $T_d = 1.69 \times 10^{-4}$ s, $N = 4$, $b = 0.573$ and the PI-controller parameters $K_p = 0.02$, $T_i = 2 \times 10^{-6}$ s. These parameters are taken from (Gadoura, *et al.*, 1999a) in order to obtain the scalar gains of Fig. 4.3 and Fig. 4.6.

Fig. 5.1 shows the dynamic performance of the output voltage against step-changes in output power using fuzzy controllers. The fuzzy controllers have the advantage of better transient response and improved large signal over conventional controllers, as presented in [P6]. Fig. 5.2 shows the resulting output characteristic of the DC/DC converter. When the output current increases above the nominal value, the output voltage starts decreasing until the minimum value is achieved. If the output current continues to increase, the output voltage will cut off (Gadoura, *et al.*, 1999a).

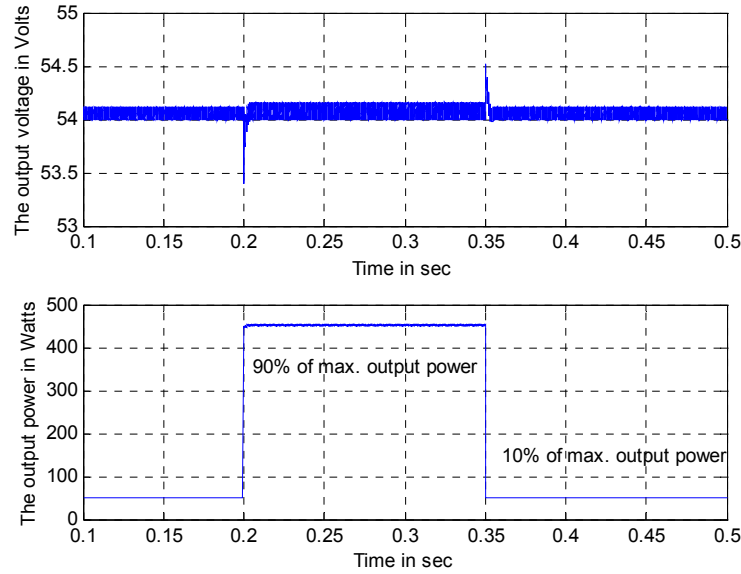


Fig. 5.1 - The output voltage with step-changes in output power using PID-like FLC.

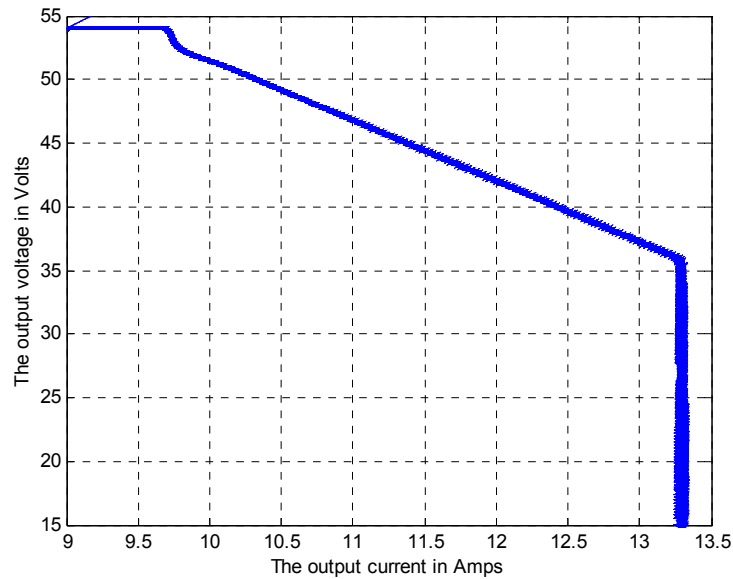


Fig. 5.2 - The output characteristic of a Telecom power supply using PI-like FLC.

5.1.2 Internal Model Control Design

The boost and buck-boost converters supplying a resistive load are implemented and simulated using MatlabTM/SimulinkTM to verify the validity of control design. The specifications are given as follows. The input voltage $u_{in,0} = 12$ V, output voltage $u_{out,0} = 24$ V, max. output power $P_o = 25$ W, switching frequency $f_s = 240$ kHz, inductance $L = 200$ μ H, capacitance $C = 220$ μ F, output resistance $R = 44$ Ω , equivalent series resistance of capacitor $r_C = 0.2$ Ω , equivalent series resistance of inductor $r_L = 0.1$ Ω .

The performance weights $w_p(j\omega)$ for boost and buck-boost converters that can be adopted into Fig. 4.8 have been chosen as

$$w_p(j\omega) = \frac{1/1.25 s + 1000}{s + 1000 \times 10^{-6}} \quad (\text{Boost converter}) \quad (5.1)$$

$$w_p(j\omega) = \frac{1/1.27 s + 1000}{s + 1000 \times 10^{-6}} \quad (\text{Buck-boost converter}) \quad (5.2)$$

From Fig. 5.3, the uncertainty weights $w_i(j\omega)$ for boost and buck-boost converters can be obtained as an upper bound of relative errors.

$$w_i(j\omega) = 1.04 \frac{s + 1.7 \times 10^4}{s + 4.5 \times 10^4} \quad (5.3)$$

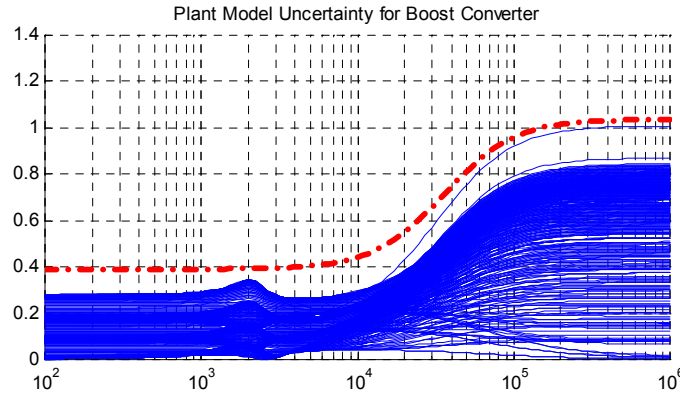


Fig. 5.3 – The relative errors and uncertainty bound of both boost and buck-boost converters

In Fig. 5.4, nominal performance (NP) test of equation (4.8), robust stability (RS) test of equation (4.9), and robust performance (RP) test of equation (4.11) are carried out for boost converter, on the left, and for buck-boost converter, on the right with different values of λ , $\lambda = 0.5$ ms (solid-line) & 0.3 ms (dashed-line). Obviously, robust performance can't be guaranteed with $\lambda = 0.3$ ms. However, nominal performance and robust stability are ensured.

In Fig. 5.5 and Fig. 5.6, the simulation results of output voltage of boost and buck-boost converters show good rejection to line ($\pm 20\%$ of input voltage) and load ($+10\%$ to $+90\%$ of maximum output power) disturbances. Fig. 5.5 and Fig. 5.6 demonstrate the effectiveness of the control design.

The method only requires the tuning of a single parameter, which has been selected by solving the \mathcal{H}_∞ -optimal control criterion. The stability properties have been improved as shown in Fig. 5.7 and Fig. 5.8. For boost converter, the gain and phase margin are improved from 18 dB and 4.5° for uncompensated system to 28 dB and 85.5° for compensated system. For buck-boost converter, the uncompensated system is shown to be unstable in closed-loop, however, for the compensated system the gain and phase margins are 26.1 dB and 84.6° . The

bandwidths are restricted due to their RHP-zeros. From the simulation results, it can be seen that the use of IMC-based controller provides good tracking performance and disturbance rejection capability. Also it provides robust stability and robust performance in the presence of uncertainties.

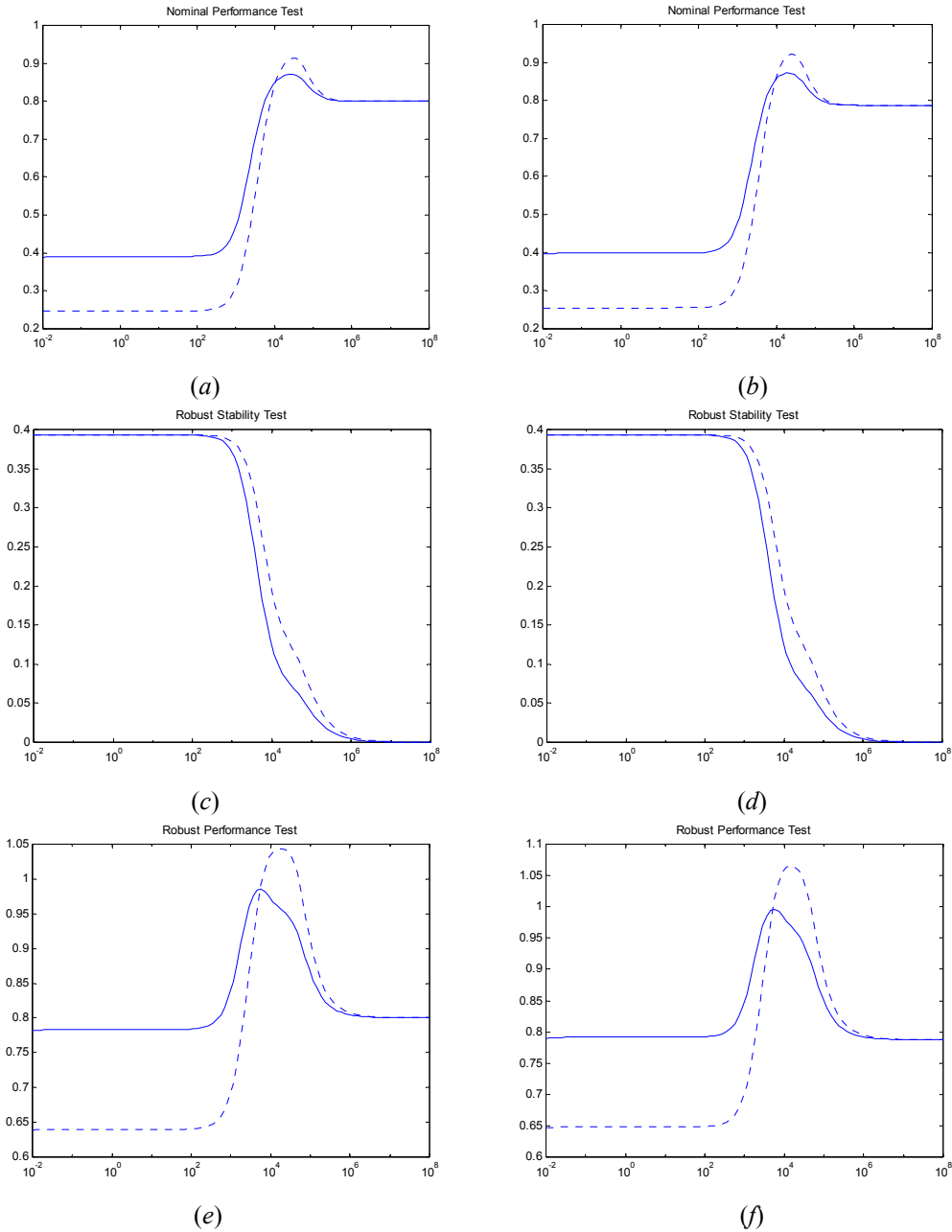


Fig. 5.4 – The nominal performance NP, robust stability RS, and robust performance RP bounds for boost converter, (a), (c), and (e), respectively, and for buck-boost converter, (b), (d), and (f), respectively, using IMC-based controller with different values of λ . $\lambda = 0.5$ ms (solid-line) & 0.3 ms (dashed-line).

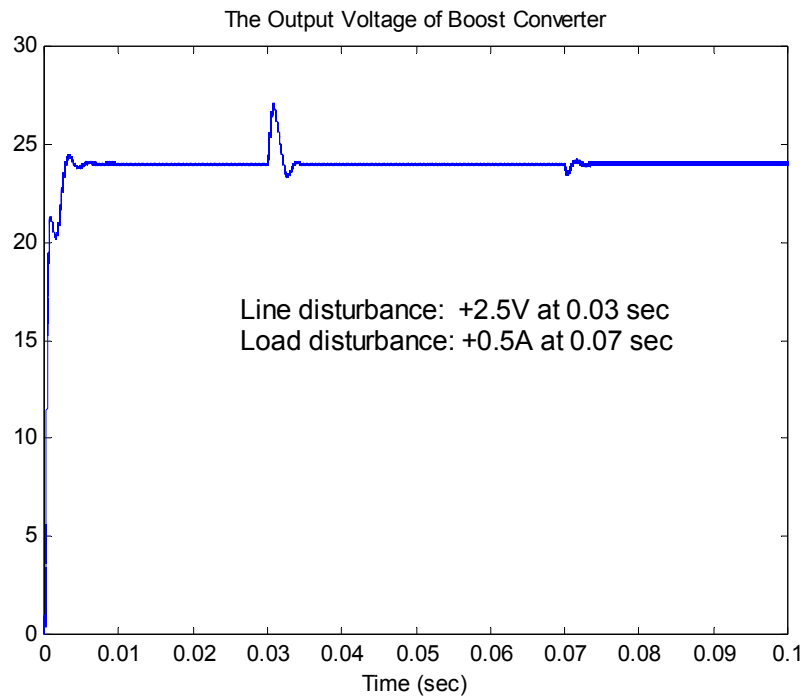


Fig. 5.5 - The output voltage of boost converter shows good transient response when line and load disturbances are applied. Also it is robust in spite of the variations of power components.

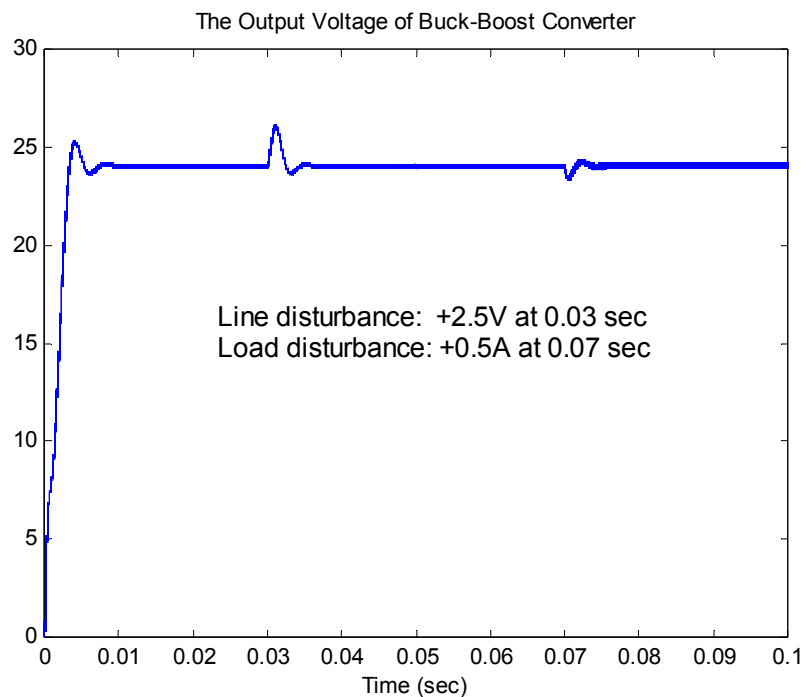


Fig. 5.6 - The output voltage of buck-boost converters shows good transient response when line and load disturbances are applied. Also it is robust in spite of the variations of power components.

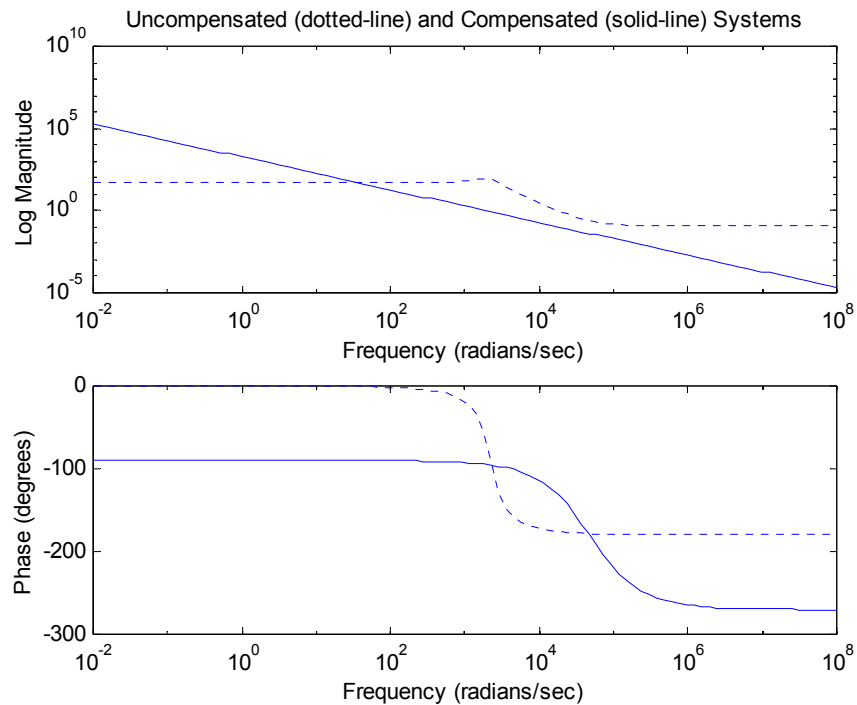


Fig. 5.7 - The bode plots of boost converter with and without compensation. The gain and phase margin are improved from 18 dB and 4.5° for uncompensated system to 28 dB and 85.5° for compensated system.

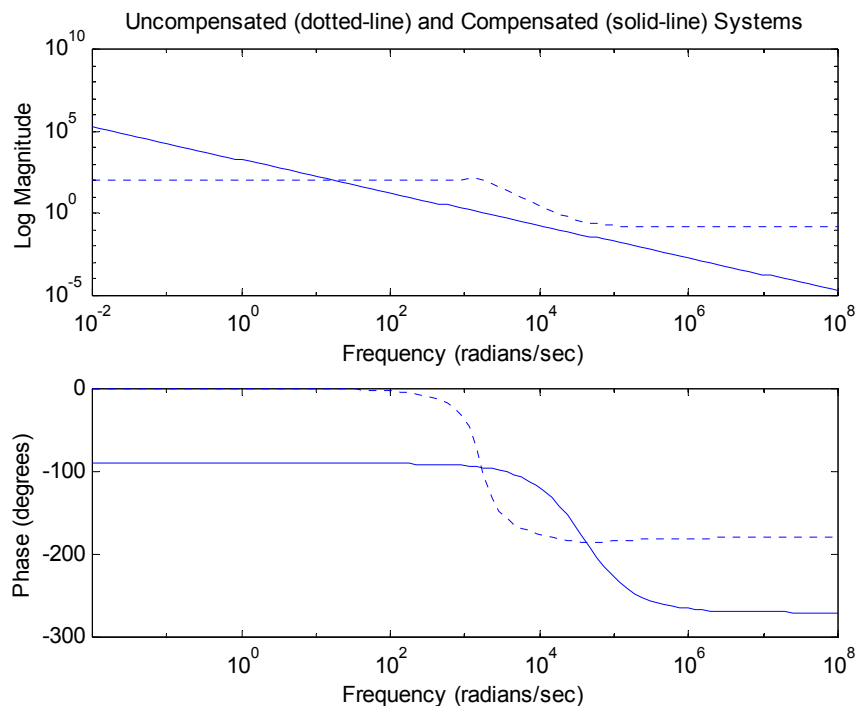


Fig. 5.8 - The bode plots of buck-boost converter with and without compensation. The uncompensated system is shown to be unstable in closed-loop, however, for the compensated system the gain and phase margins are 26.1 dB and 84.6° .

5.2 Parallel-connected Configuration

The configuration of two-identical parallel-connected buck converters is considered to verify the control design procedure. The specifications are given as follows. The input voltage $u_{in,0} = 140$ V, output voltage $u_{out,0} = 54$ V, max. output power $P_o = 500$ W, switching frequency $f_s = 100$ kHz, inductance $L = 100$ μ H, capacitance $C = 1000$ μ F, output resistance $R = 11$ Ω , equivalent series resistance of capacitor $r_C = 50$ m Ω , equivalent series resistance of inductor $r_L = 15$ m Ω , interconnection resistance $r_p = 10$ m Ω , cable resistance $r = 20$ m Ω .

5.2.1 PI/PID Control Design

The cascaded PI/PID controllers as shown in Fig. 1.6 are used to ensure robust output and to share the current load. The controllers are identical for both converters and have the following parameters. PID-controller: $K_p = 22.665$, $T_i = 0.745$ ms, $T_d = 0.169$ ms, $N = 4$, and $b = 0.573$. PI-controller: $K_p = 2$ and $T_i = 0.2$ ms. The formulas of PI and PID controllers can be written as follows.

$$c_{i_j} = K_{p_j} \left(1 + \frac{1}{T_{i_j} s} \right) (i_{ref_j} - i_{out_j}) \quad (5.4)$$

$$c_{u_j} = K_{p_j} \left(b_j (u_{ref_j} + c_{i_j}) - u_j + \frac{1}{T_{i_j} s} (u_{ref_j} + c_{i_j} - u_j) - \frac{T_{d_j}}{T_{d_j}/N_j s + 1} u_j \right) \quad (5.5)$$

where $j = 1, 2, \dots, n$ and n is a number of converters connected in parallel.

From Fig. 2.6, the high-pass filter matrices, $W_{nu}(s)$ and $W_{ni}(s)$, are designed to attenuate the measurement noise, which is ignored (i.e., $\mathbf{n}_u = \mathbf{n}_i = 0$) in the simulation. Also we assumed that the interconnection resistance $r_p = 0$. The low-pass filter matrices, $W_{pu}(s)$ and $W_{pi}(s)$, are designed to reduce the ripples in the output currents and voltages in order to study the disturbance rejection capability of the system. Also $W_d(s)$ and $W_r(s)$ are scaling matrices.

In Fig. 5.9, nominal performance (NP) and nominal stability (NS) of the voltage-loop are achieved where the maximum singular value is less than 1 and all the poles are located in LHP, respectively. Also the robust performance (RP) and robust stability (RS) of the voltage-loop are achieved as shown in Fig. 5.10. In Fig. 5.11 and Fig. 5.12, NP, NS, RP, and RS of the overall system are achieved where γ is equal to 1.27, which is violating the robust performance of the overall system. However the simulation results of the worst-case show that the system is robustly performed and stable as shown in Fig. 5.14 and Fig. 5.15. Note that few poles those are very large are not seen in the pole-zero maps because of figure scales.

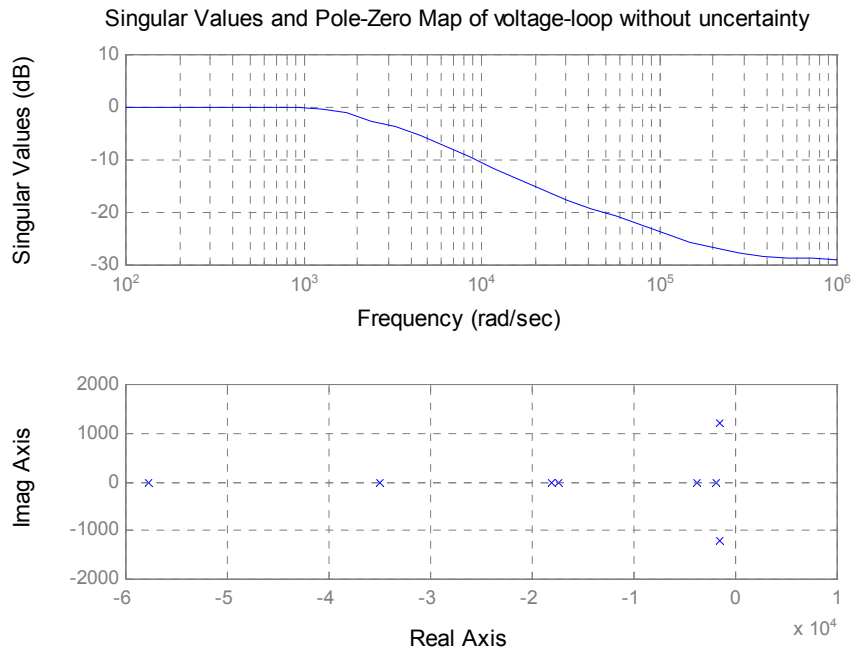


Fig. 5.9 - The nominal performance and nominal stability tests for voltage-loop, i.e., $\bar{\sigma}(N_{u_{11}}) < 1$ for all ω and N_u has all poles in LHP.

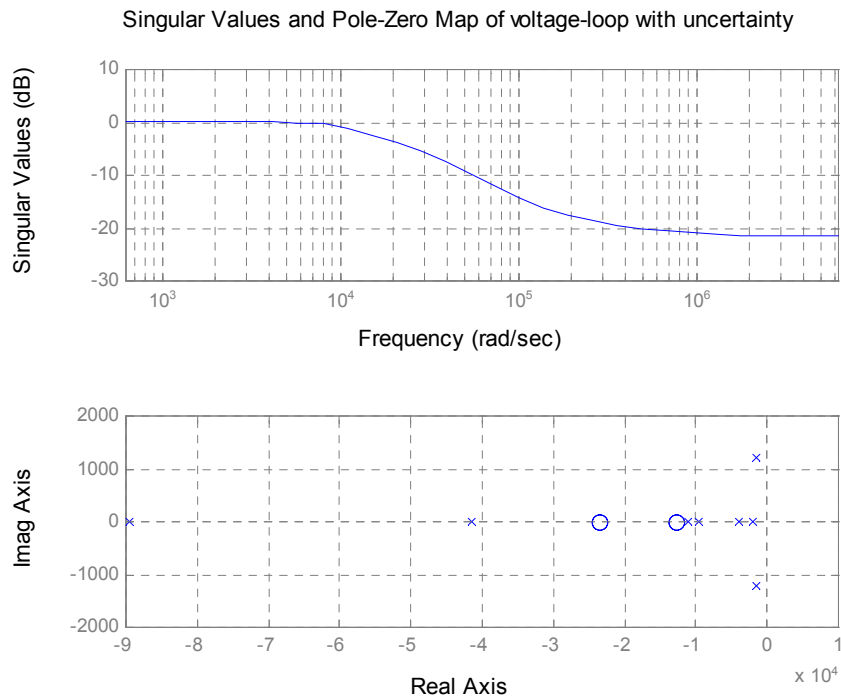


Fig. 5.10 - The robust performance and robust stability tests for uncertain voltage-loop, i.e., $\bar{\sigma}(F_u) < 1$ for all ω and F_u has all poles in LHP

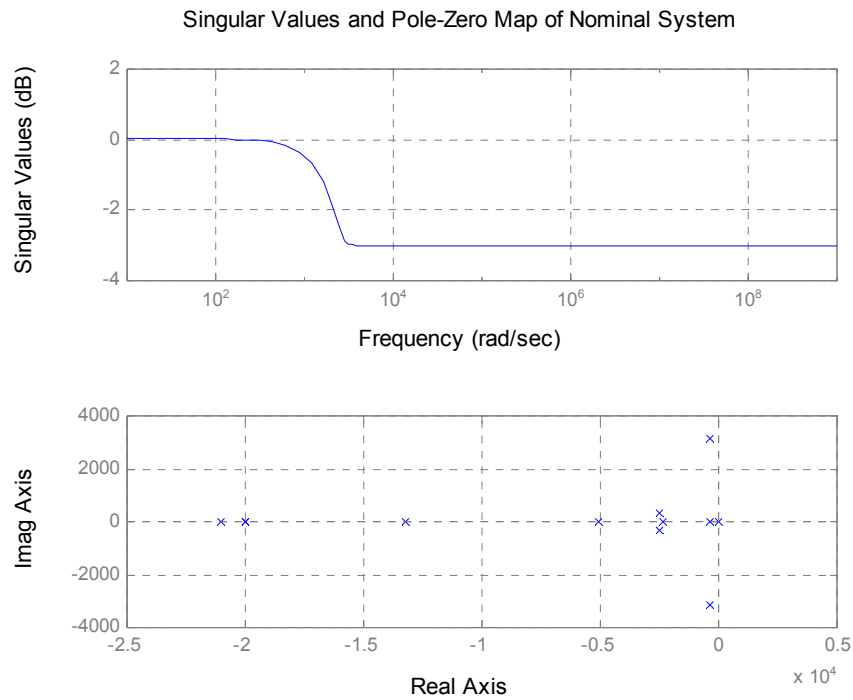


Fig. 5.11 - The nominal performance and nominal stability tests for the overall system, i.e., $\bar{\sigma}(N_{11}) < \gamma$ for all ω and N has all poles in LHP.

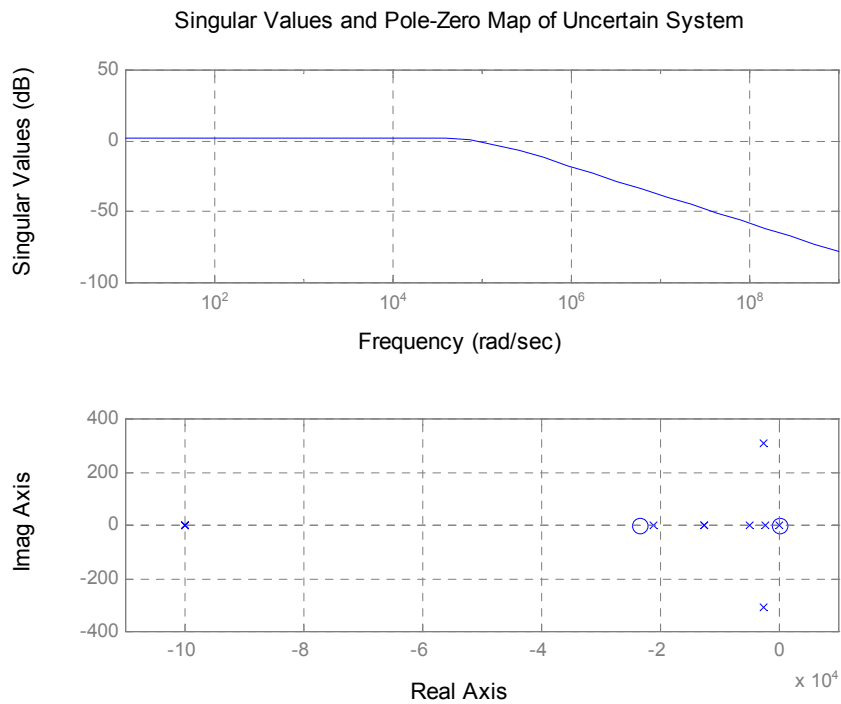


Fig. 5.12 - The robust performance and robust stability tests for uncertain system, i.e., $\bar{\sigma}(F) < \gamma$ for all ω and F has all poles in LHP.

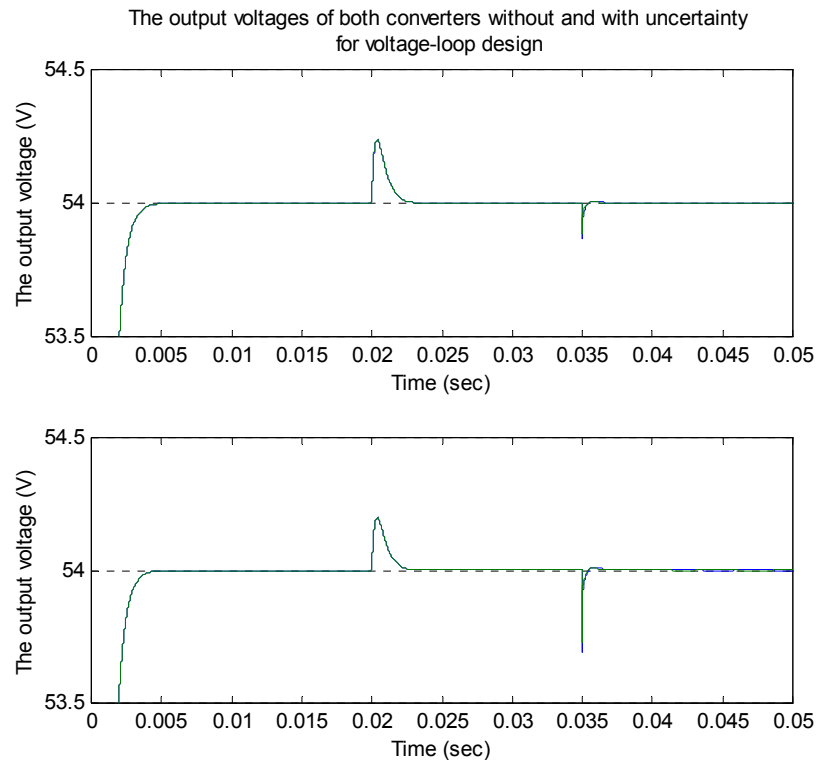


Fig. 5.13 - The steady state and transient behavior of the output voltages of the voltage-loop in the presence of line & load disturbances without (upper) and with uncertainty (lower).

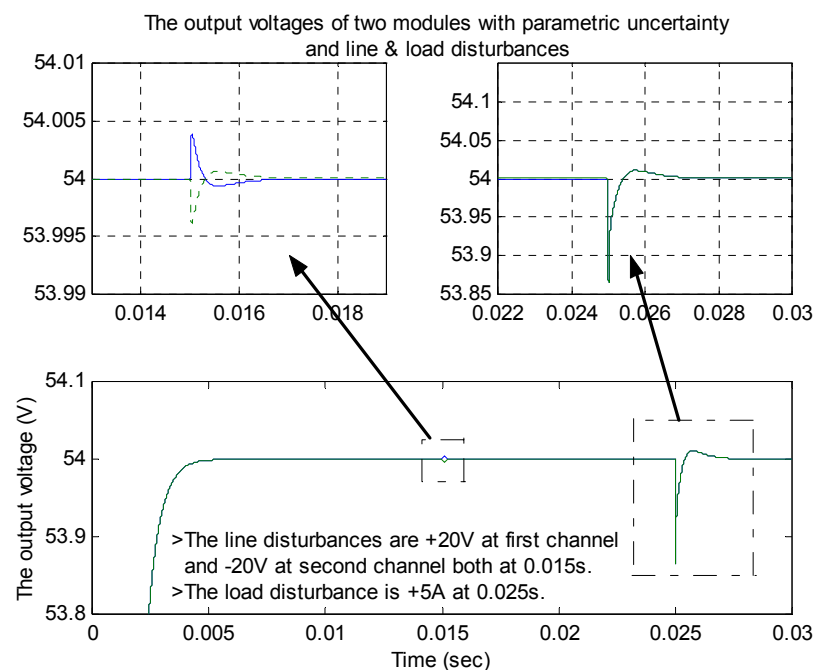


Fig. 5.14 - The steady state and transient behavior of the output voltages in the presence of line & load disturbances with uncertainty.

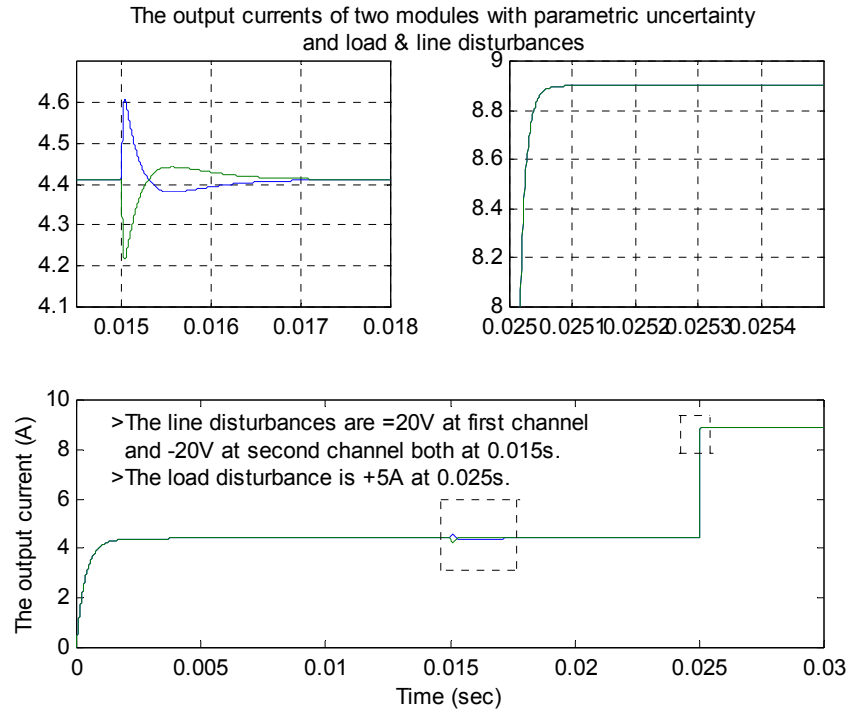


Fig. 5.15. The steady state and transient behavior of the output currents in the presence of line & load disturbances with uncertainty.

5.2.2 \mathcal{H}_∞ Control Design

A. Voltage Mode Control

From Fig. 2.5, the performance weight $w_p(j\omega)$ for two-identical paralleled buck converters has been chosen with very small gain that has been compensated with final controller.

$$w_p(j\omega) = 9 \times 10^{-8} \frac{0.83s + 1000}{s + 1} \quad (5.6)$$

where $\mathbf{W}_p = w_p \mathbf{I}_4$.

The measurement noise has been modeled to avoid some difficulties in the synthesis procedure. The noise weight $w_n(j\omega)$ for two-identical paralleled buck converters has been chosen as a high-pass filter.

$$w_n(j\omega) = \frac{2s + 10^5}{s + 1.1 \times 10^5} \quad (5.7)$$

where $\mathbf{W}_n = w_n \mathbf{I}_4$.

The uncertainties weights, as shown in Fig. 5.16, are derived by using equations (3.9) and (3.10).

$$w_{ip} = 0.97 \frac{s^2 + 1 \times 10^4 s + 1 \times 10^8}{s^2 + 5463 s + 2.9 \times 10^7} \quad (5.8)$$

$$w_{id} = 6.8 \times 10^{-3} \frac{s^2 + 3.36 \times 10^4 s + 9.93 \times 10^8}{s^2 + 6894 s + 4.02 \times 10^7} \quad (5.9)$$

$$W_{ip} = w_{ip} I_2 \text{ and } W_{id} = w_{id} I_3$$

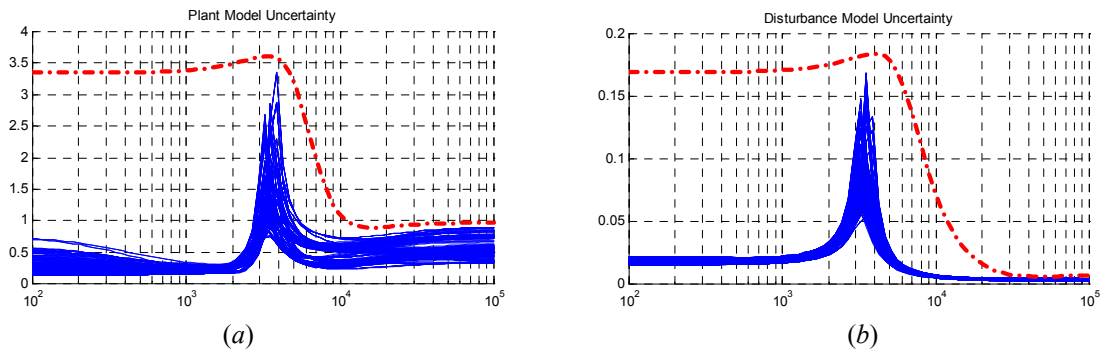


Fig. 5.16 – The uncertainties bounds (dash-dotted line) of the plant model uncertainty (a), and the disturbance model uncertainty (b). Plotting the relative errors between the nominal model and the perturbed models has produced the uncertainties bounds, which are the upper bounds of the relative errors plots.

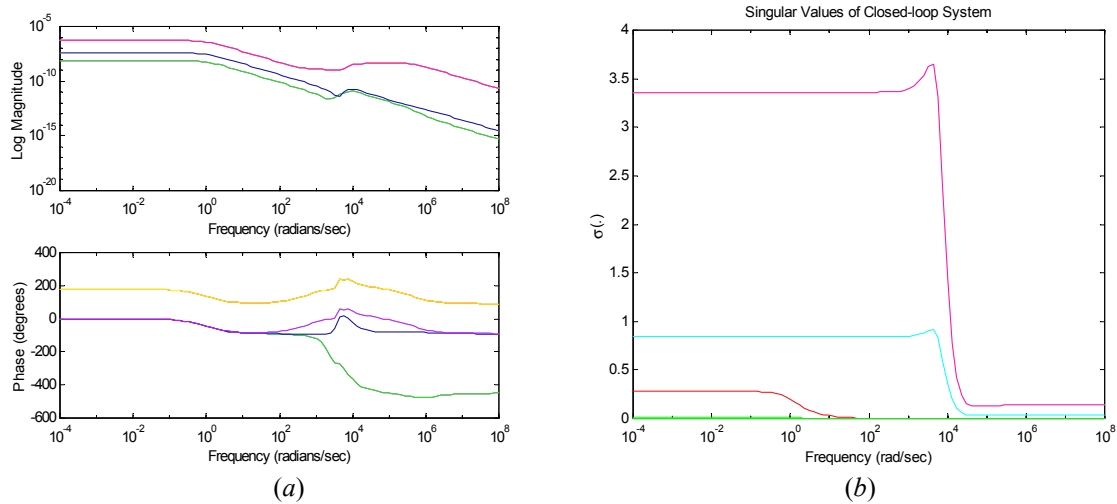


Fig. 5.17 – The bode plots of \mathcal{H}_∞ -robust controller that is synthesized using “*hinfsyn*” command in Matlab™ (a), and the singular values of the closed-loop system where the maximum singular value is greater than 1, which indicates that the noise/disturbance signals are not completely attenuated (b).

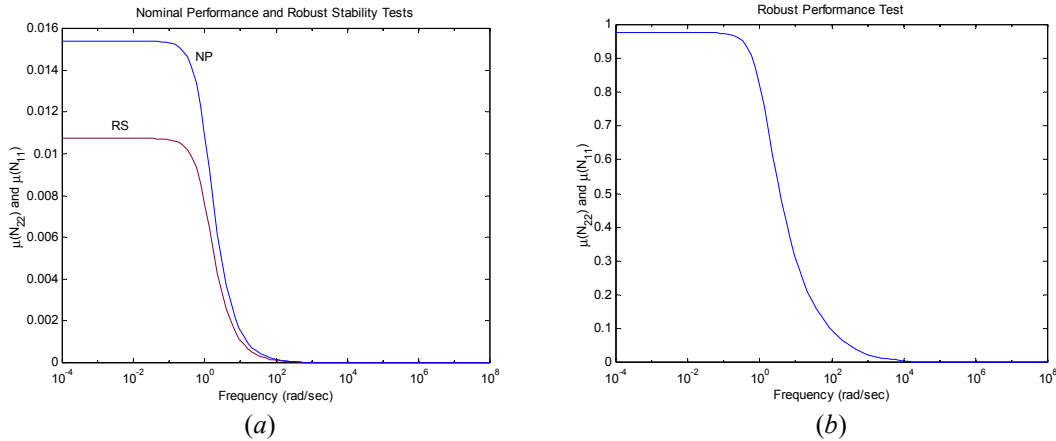


Fig. 5.18– The nominal performance NP and robust stability RS bounds (a), and robust performance RP bound (b), of two-identical-buck converters connected in parallel with \mathcal{H}_∞ controller.

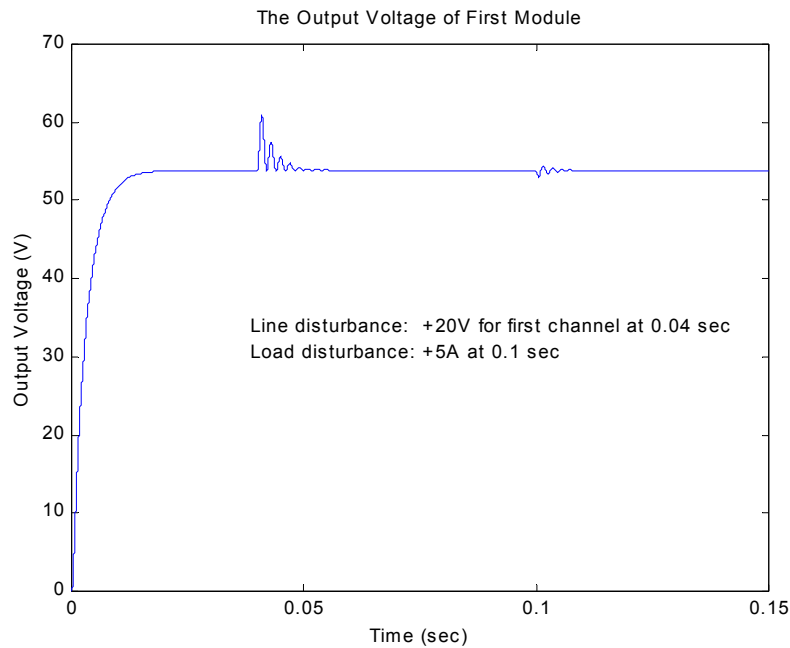


Fig. 5.19 - The output voltage of first converter. When the line and load disturbances are applied the oscillation is clearly seen because of big peaks at resonance frequency.

From Fig. 5.17(a), the \mathcal{H}_∞ -controller appears to be stable although its gain is small. However, it will be increased when compensated with the performance weight gain. Fig. 5.17(b) shows the singular values of the closed-loop system. The maximum singular values of the resulting closed-loop system (14-inputs and 11-outputs) has rank equal to 3.7, hence the rest of its singular values are less than 1. The controlled system achieves nominal performance, robust stability, and robust performance, as shown in Fig. 5.18. In Fig. 5.19, the simulation results of

output voltage of two-buck converters in parallel show good rejection to line and load disturbances. Also the output currents of two modules are shown in Fig. 5.20.

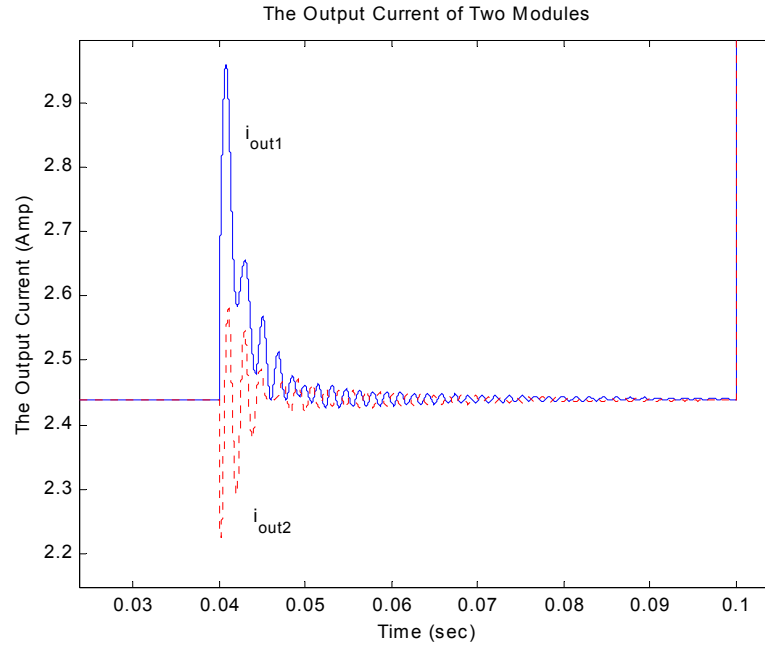


Fig. 5.20 - The output currents when line disturbance is applied. The signals are oscillatory.

B. Current Mode Control

The performance weight $w_p(j\omega)$ has been chosen as a low-pass filter.

$$w_p(j\omega) = \frac{0.67s + 100}{s + 10} \quad (5.10)$$

where $\mathbf{W}_p = w_p \mathbf{I}_4$.

The noise weight $w_n(j\omega)$ for two-identical paralleled buck converters has been chosen as a high-pass filter.

$$w_n(j\omega) = \frac{1.11s + 1000}{s + 10000} \quad (5.11)$$

where $\mathbf{W}_n = w_n \mathbf{I}_4$. Also the control weight $w_c(j\omega)$ has been chosen as a high-pass filter.

$$w_c(j\omega) = \frac{1.11s + 10000}{s + 20000} \quad (5.12)$$

where $\mathbf{W}_c = w_c \mathbf{I}_2$. \mathbf{W}_r and \mathbf{W}_d are scaling matrices.

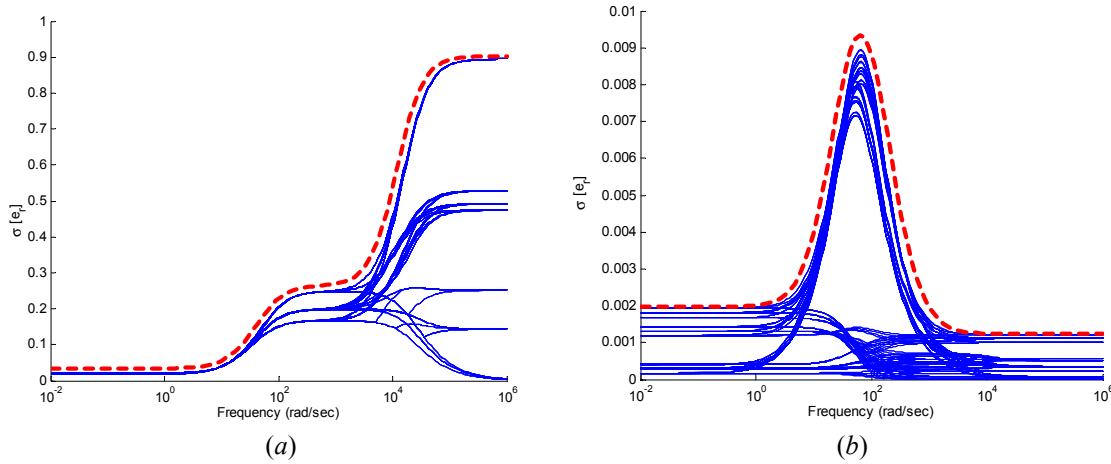


Fig. 5.21 – The uncertainty bounds (dashed line) of plant model uncertainty (a), and disturbance model uncertainty (b). The uncertainties bounds are the upper bounds of relative errors plots between the nominal model and the perturbed models.

The uncertainties weights, as shown in Fig. 5.21, are also derived by using equations (3.9) and (3.10).

$$w_{ip} = 0.92 \frac{(s + 4.54 \times 10^3)(s + 7.6)}{(s + 1.55 \times 10^4)(s + 58)} \quad (5.13)$$

$$w_{id} = 0.0012 \frac{(s + 1.26 \times 10^3)(s + 5.3)}{(s + 136.85)(s + 30.7)} \quad (5.14)$$

$$\mathbf{W}_{ip} = w_{ip} \mathbf{I}_2 \text{ and } \mathbf{W}_{id} = w_{id} \mathbf{I}_3$$

The Matlab™ function “*hinfsyn*” is used to synthesize the \mathcal{H}_∞ controller by selecting a value of γ that determines if there exists a controller \mathbf{K} such that

$$\|\mathbf{F}\|_\infty = \|\mathcal{F}_1(\mathbf{G}, \mathbf{K})\|_\infty < \gamma, \text{ where } \mathbf{G} = \mathcal{F}_u(\mathbf{P}, \Delta) \quad (5.15)$$

This value of γ is minimized numerically by using a modified bisection algorithm, called γ -iteration. It is repeated until the magnitude of the difference between the smallest γ value that has passed and the largest γ value that has failed is small, see (Balas, *et al.*, 1997). The achieved γ is 1.0006 as shown in Fig. 5.22(b) describing singular values of the closed-loop system. From Fig. 5.22(a), the \mathcal{H}_∞ controller shows to be stable, however it has an order of 28 that makes it very difficult to implement in reality. Model reduction techniques can be applied to reduce the 28th-order controller to 2nd-order controller without losing the robustness properties. The balanced realization of the system that helps to remove all unobservable and/or uncontrollable modes, and the Hankel norm approximation are used to

produce a low-order controller. The MatlabTM functions “*sysbal*” and “*hankmr*” are performed to achieve a second-order controller that is used in simulation of Fig. 5.24 and Fig. 5.25.

The controlled system achieves nominal performance and robust stability, as shown in Fig. 5.23(a). Also the robust performance is achieved as shown in Fig. 5.23(b). In Fig. 5.24, the simulation results of output voltage of two-buck converters in parallel show good rejection to line and load disturbances. Also the output currents of two modules are shown in Fig. 5.25, however both responses are somewhat slow.

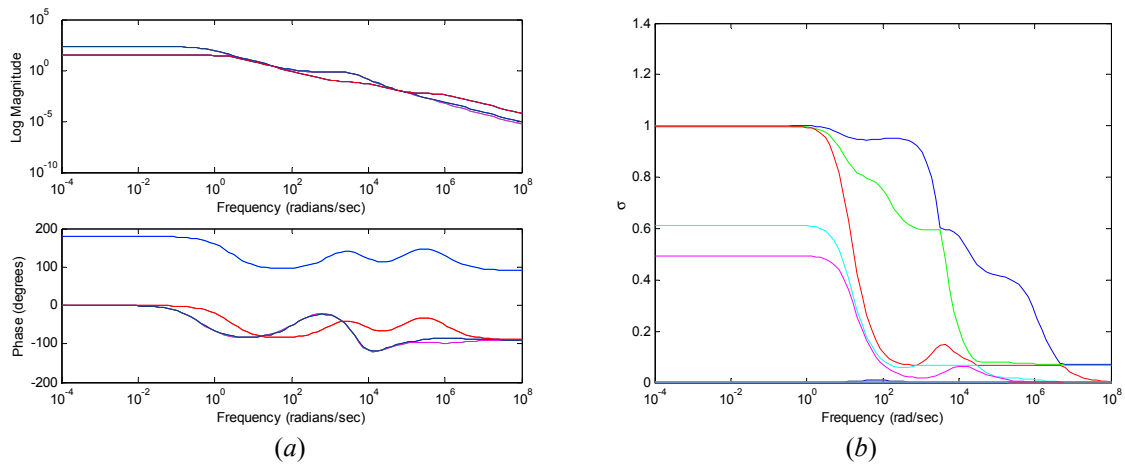


Fig. 5.22 – The bode plots of \mathcal{H}_∞ robust controller (a), and the singular values of the closed-loop system with \mathcal{H}_∞ robust controller (b).

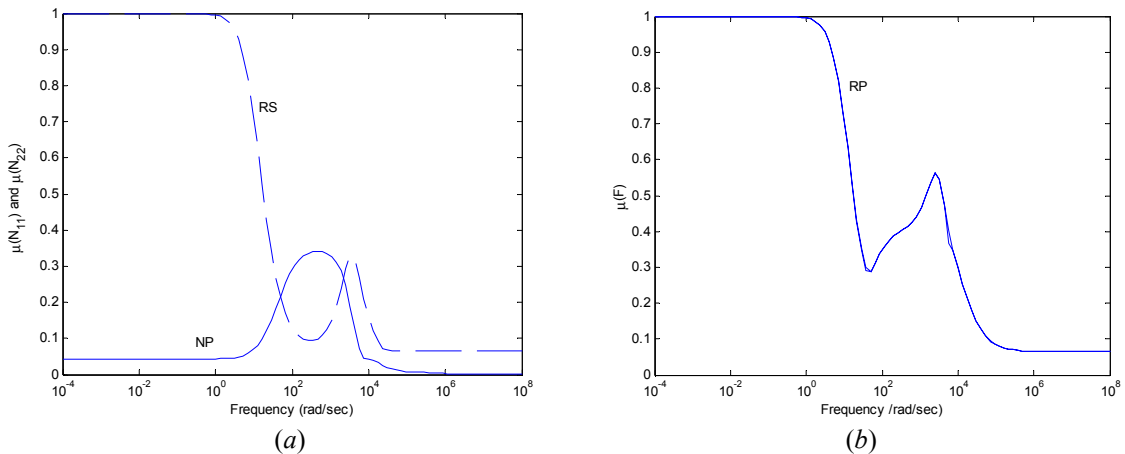


Fig. 5.23 – The μ -evaluations for nominal performance NP and robust stability RS bounds (a), and robust performance RP bound (b).

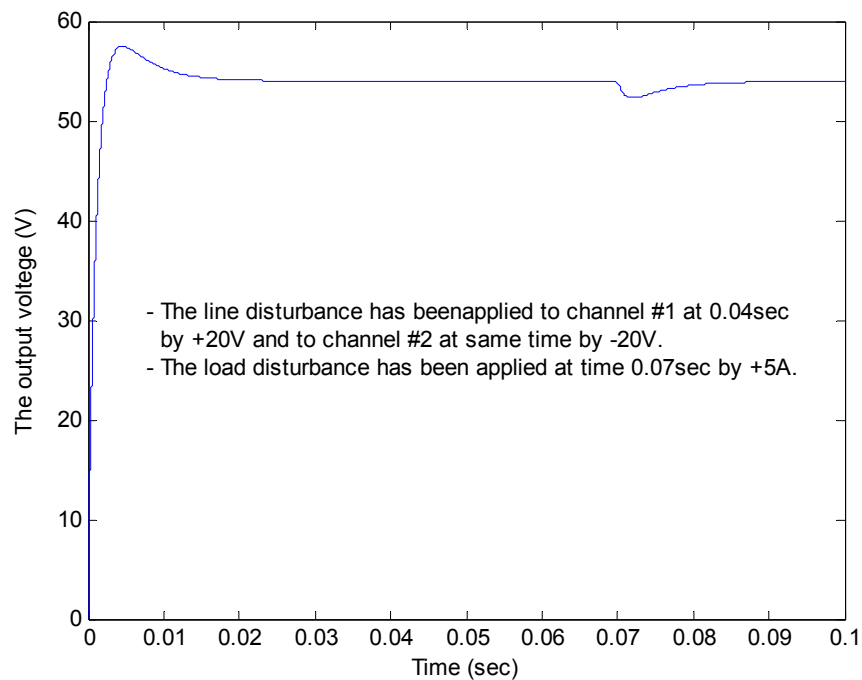


Fig. 5.24 – The output voltage of first converter when the line and load disturbances are applied. The response is robust in spite of the variations of power components.

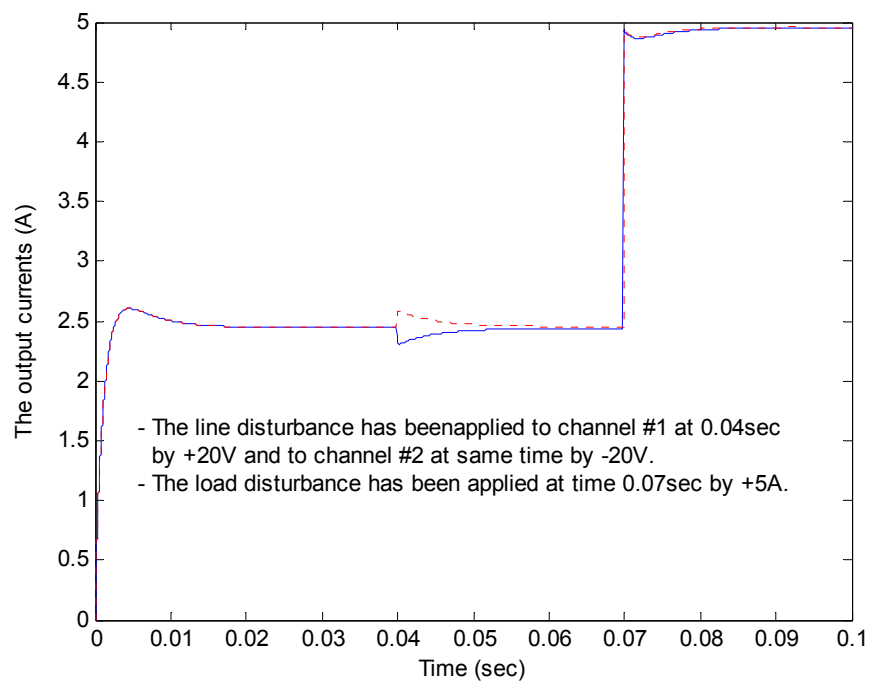


Fig. 5.25 – The output currents when the line and load disturbances are applied. Also it is robust in spite of the variations of power components.

5.2.3 \mathcal{H}_∞ Loop-Shaping Control Design

The interconnection model that used in the \mathcal{H}_∞ LSD procedure includes the performance and uncertainty weights that were expressed in equations (5.10-5.14). The \mathcal{H}_∞ LSD procedure starts by shaping the nominal plant model by pre- and post-plant weighting functions.

$$w_1 = 0.3 \frac{s+10000}{s}, \quad W_1 = w_1 I_2 \quad (5.16)$$

and $W_2 = I_4$

A good shape would normally be high gain at low frequencies, low gain at high frequencies, and roll-off rates of approximately 20 dB/decade at the desired bandwidth, with higher rates at high frequencies. The singular value plots should also be quite close to each other at the desired bandwidth. The post-plant weighting function W_2 is usually chosen as a constant, reflecting the relative importance of the outputs to be controlled and the other measurements being fed back to the controller. The pre-plant weighting function W_1 contains the dynamic shaping. Integral action, for low frequency performance, phase-advance for reducing the roll-off rates at crossover, and phase-lag to increase the roll-off rates at high frequencies should all be placed in W_1 , if desired. The weights should be chosen so that no unstable hidden modes are created in G_{ps} . Fig. 5.27 shows that the plant model is well shaped. The Matlab™ function “ncfsyn” is used to synthesize the \mathcal{H}_∞ controller. The value of γ is determined by equation (4.24), so that the γ -iteration is not needed. Once the controller K_s that robustly stabilizes the shaped plant model is achieved, the final controller K can be obtained by absorbing the weighting functions, W_1 and W_2 into K_s , i.e., $K = W_1 K_s W_2$.

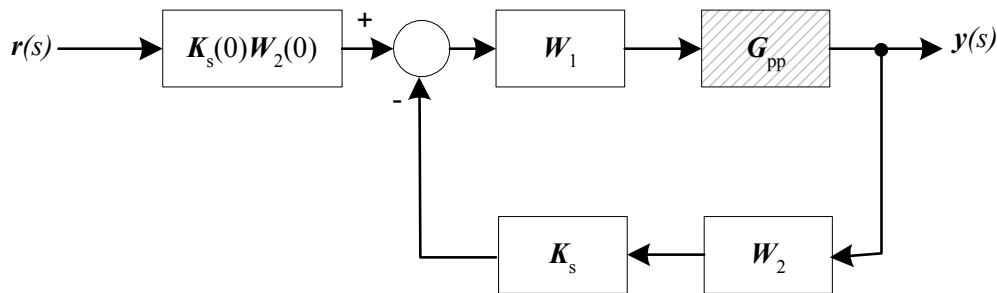


Fig. 5.26 – A practical implementation of \mathcal{H}_∞ LSD controller to avoid the set point kick phenomenon.

For tracking problems, the reference signal is generally fed between K_s and W_1 as shown in Fig. 5.26. This helps that the references do not directly excite the dynamics of K_s , which can result in large amounts of overshoot (classical derivative kick). The constant pre-filter ensures a steady state gain of unity between the references and the measurements, assuming integral action in W_1 .

The controlled system achieves nominal performance and robust stability, as shown in Fig. 5.28(a). Also the robust performance is achieved as shown in Fig 5.28(b). In Fig. 5.29, the simulation results of output voltage of two-buck converters in parallel show good rejection to line and load disturbances. Also the output currents of two modules are shown in Fig. 5.30, however the load disturbance yields a bit large peak.

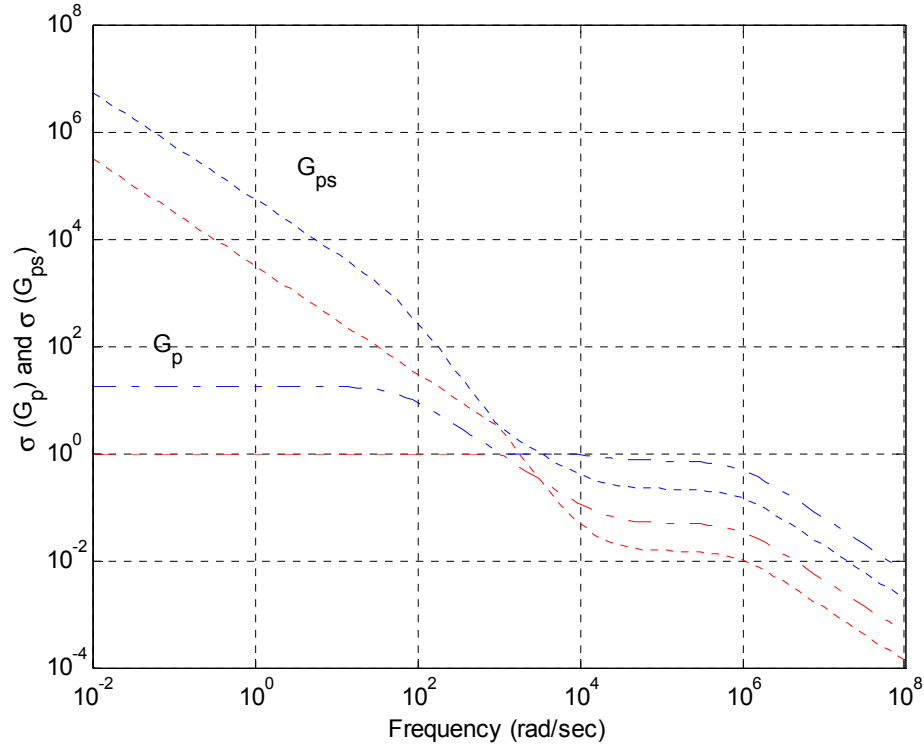


Fig. 5.27 – The singular values of the nominal plant and the shaped plant model.

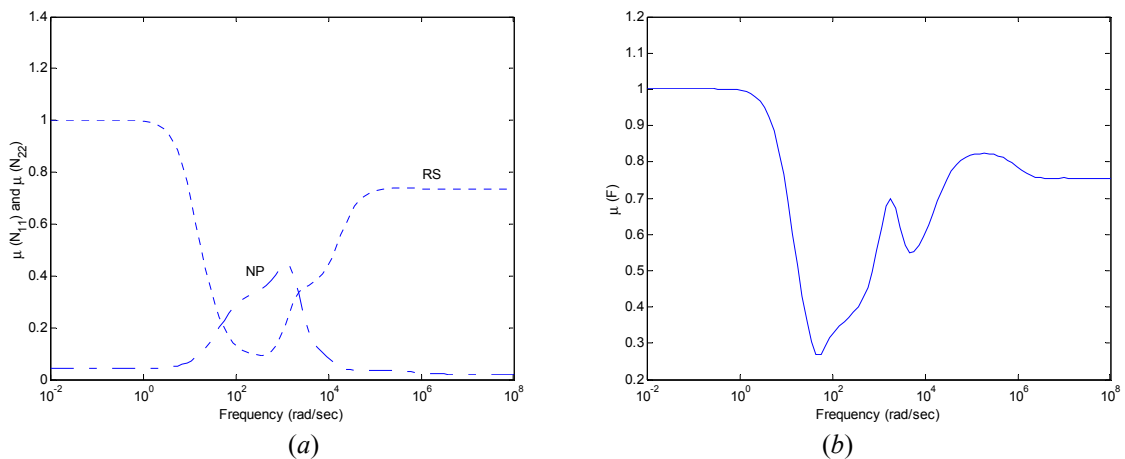


Fig. 5.28 – The μ -evaluations for nominal performance NP and robust stability RS bounds (a), and robust performance RP bound (b).

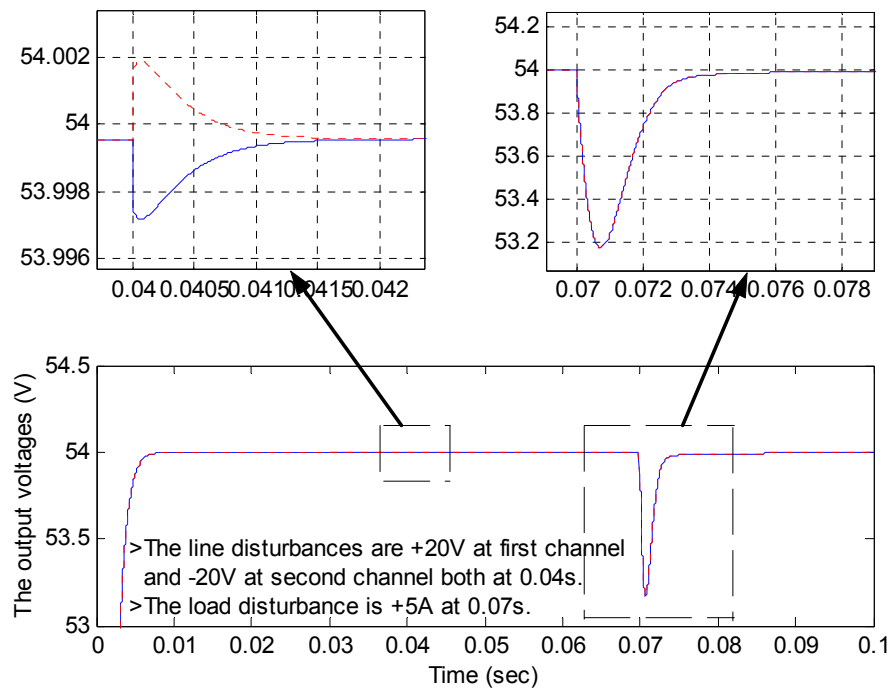


Fig. 5.29 – The output voltage of first module when the line and load disturbances are applied. Also it is robust in spite of the variations of power components.

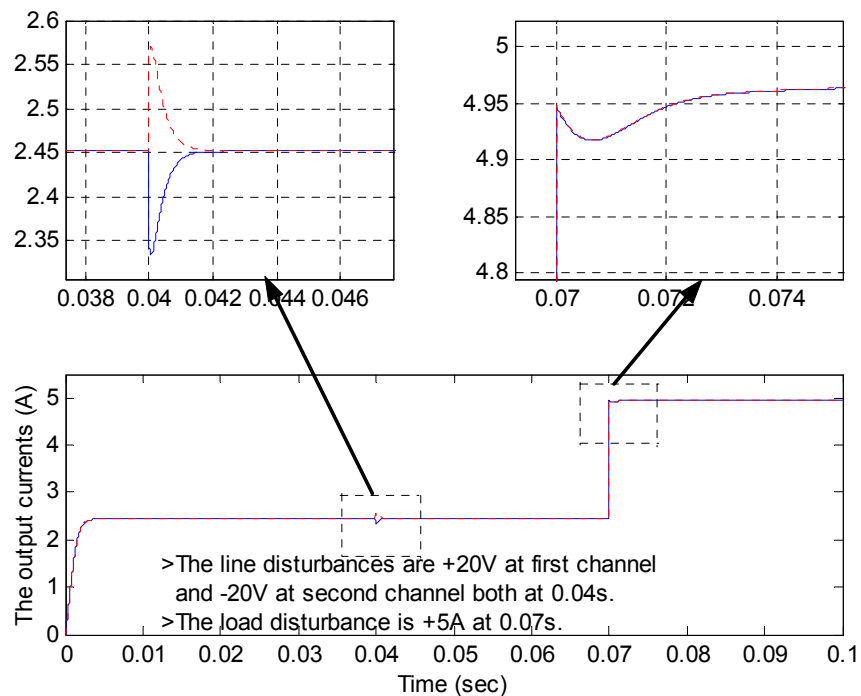


Fig. 5.30 – The output currents when the line and load disturbances are applied. Also it is robust in spite of the variations of power components.

5.3 Discussion on Applied Control Methods in Paralleled DC/DC Converters

This discussion is based on the results presented in [P1-P4]. Some of the key points have been discussed in this chapter.

TABLE 5.1 – Summary of applied robust control in two-identical buck converters connected in parallel

PI/PID Control	VMC	<ul style="list-style-type: none"> ▪ The nominal performance (NP), nominal stability (NS), robust performance (RP), and robust stability (RS) of the voltage-loop are achieved. ▪ The NP, NS, and RS of the overall system are achieved. ▪ The peak of maximum singular value of $F(s)$ is equal to 1.27, which is violating the robust performance of the overall system. ▪ The simulation results of the worst-case show that the system is robustly performed and stable.
\mathcal{H}_∞ Control	VMC	<ul style="list-style-type: none"> ▪ The \mathcal{H}_∞-controller stabilizes the system although its gain is small. However, it will be increased when compensated with the performance weight gain. ▪ The maximum singular value of the resulting closed-loop system has rank equal to 3.7, which means that the disturbance from input to output is not completely attenuated. ▪ The controlled system achieves nominal performance, robust stability, and robust performance.
	PCMC	<ul style="list-style-type: none"> ▪ The maximum singular value of the resulting closed-loop system has rank equal to 1.0006. ▪ The \mathcal{H}_∞ controller has an order of 28 that makes it very difficult to implement in reality. ▪ Model reduction techniques can be applied to reduce the 28th-order controller to 2nd-order controller without losing the robustness properties. ▪ The controlled system achieves nominal performance, robust stability, and robust performance. However output voltages and currents responses are a bit slow.
\mathcal{H}_∞ LSD Control	VMC	<ul style="list-style-type: none"> ▪ The LSD is straightforward approach, which is easy to implement in practice. ▪ The nominal performance is achieved. ▪ The voltage-controlled system, which is a resonant system, can achieve neither the robust stability nor the robust performance.
	PCMC	<ul style="list-style-type: none"> ▪ The nominal performance, robust stability, and robust performance are achieved. ▪ The \mathcal{H}_∞ loop-shaping controller attains the robust stability and robust performance of the system in the presence of uncertainty and shows good tracking performance and disturbance rejection capability.

Chapter 6

Conclusion

6.1 Summary of Papers

[P1] A practical robust control design of paralleled DC/DC converters in the presence of uncertainties is introduced in this paper. The overall system is composed of two-MIMO subsystems, for voltage-loop and current-loop. The voltage-loop consists of n -SISO subsystems, where n is the number of converters in parallel that can be designed separately. The actual plant models consist of nominal plant models and uncertainty models. Parametric uncertainty is modeled where the structure of the model is known, but some of the parameters are uncertain. Robust PID and PI controllers are proposed to achieve robust stability and robust performance for voltage-loop and current-loop respectively. Also the μ -analysis is used to evaluate the robustness of both controllers. The control design procedure presented is verified by simulation of two 500W-buck converters connected in parallel.

[P2] The model of parallel-connected DC/DC converters including all interconnection resistances is presented in state-space form that helps to analyze the system. The uncertainties, components of power converters, operating points, and load changes, are considered in order to design a robust controller that guarantees robust stability and performance of the system. Uncertainty models for plant and disturbance models are obtained as multiplicative input uncertainties. The \mathcal{H}_∞ optimal control is introduced and analyzed in order to design a stabilizing controller that can achieve robust stability and robust performance. The modeling, analysis and control design procedure presented is verified by simulation results on two 500W-buck converters connected in parallel and operated in CICM with VMC.

[P3] In [P2] the \mathcal{H}_∞ control design is applied to the system of paralleled DC/DC converters operating in continuous conduction mode (CICM) with voltage-mode control (VMC), however, in this paper, the peak-current-mode control (PCMC) configuration is used instead. The modeling procedure is carried out to present the system in the state-space form. The

uncertainties, components of power converters, are considered in order to design a robust controller that guarantees robust stability and performance of the system. The uncertainty models for the plant and disturbance models are obtained as a multiplicative input uncertainty. The \mathcal{H}_∞ optimal control is introduced and analyzed in order to design a stabilizing controller that can achieve robust stability and robust performance in spite of different uncertainties. The μ -analysis is used to evaluate the robustness of the system. Simulation results are presented to demonstrate the control design procedure.

[P4] In this paper a robust controller design of paralleled DC/DC converters using the \mathcal{H}_∞ loop-shaping techniques is considered. The \mathcal{H}_∞ loop-shaping design, which combines classical loop shaping ideas with \mathcal{H}_∞ robust stabilization, is suggested. The weights are selected to shape the singular values of the nominal model. The actual plant and disturbance models consist of nominal models and uncertainty. A multiplicative-input uncertainty is considered to represent the uncertainty caused by the variations of power components. The \mathcal{H}_∞ loop-shaping control is used to design stabilizing controllers that can achieve robust stability and robust performance. The same design procedure that used in [P2] is here exploited too. The μ -analysis is used to evaluate the robustness of LSD controller. A design example is presented to demonstrate the control design procedure.

[P5] In this paper, the analogue design of constant-voltage controller and overload protection controller are presented and their tasks are clearly stated. The controller design principles are discussed and the essential control-to-output transfer functions of buck converter operating either in CICM or DICM with VMC and PCMC are derived in order to analyze the system and to meet the control objectives. The cascaded controller implementation results in excellent performance both in small and large signal sense, and it is proven by experiment that both controllers can ensure the robust output and achieve the output characteristic of a Telecom power supply.

[P6] This paper is a fuzzy-logic application to regulate a voltage-controlled DC/DC converter against variations in output load improving the system stability and dynamic performance. The fuzzy-logic technique is also used to achieve the optimal output characteristic of a Telecom power system that operates in three modes. The definition and the function of output characteristic including the stability constraints are based on the operation modes. The goals of control design are to achieve robust output voltage and to ensure overload protection. The fuzzy controllers for voltage-loop and current-loop are designed based on a criterion that guarantees good dynamic performance and robustness. The tuning procedure is simple and easy to follow and apply. A design example of a buck converter is used to demonstrate the fuzzy-logic control system design. The results are satisfactorily good and highly promising when compared to the results of digital control design presented in (Gadoura, *et al.*, 1999a).

[P7] The current-mode-controlled buck converter model is presented and the control current-to-output voltage transfer function, which is based of the inductor current waveform, is obtained because it will be used in derivation of internal-model control transfer functions. The principles of internal-model control (IMC) are given in the beginning. The procedure to design an IMC-based controller for current-mode-controlled buck converter is given in

details and the simulation results show good rejection capability against step-load changes. The IMC-based controller has one tuning parameter that is used to enhance the dynamic performance of the system. Afterward, it has been noticed that the behavior of the inductor current must be as shown in Fig. 2.2, as shown also in (Schultz, 1993) and (Suntio, 2002). The transfer functions of current-mode-controlled DC/DC buck converter that are derived in [P7] are based on the inductor current waveform of Fig. (2) in [P7].

[P8] The application of internal model control to regulate boost and buck-boost converters improving their stability properties is presented in this paper. The \mathcal{H}_∞ optimal control is used to find a proper solution to design a filter in order to achieve robust stability and robust performance. The transfer functions of voltage-controlled boost and buck-boost converters are derived that are used in our analysis and control design. The model uncertainty is obtained by taking an upper bound of the relative errors that are produced by comparing the perturbed models with the nominal model. The performance objectives in addition to RS and RP are set point tracking, disturbance rejection, and suppression of measurement noise. The IMC-based controller is introduced and analyzed using the \mathcal{H}_∞ optimal control design. Design examples show that the IMC design achieves all performance objectives.

6.2 Concluding Remarks

A typical Telecom power supply in parallel configuration is introduced to study the operation modes of the system. The constant-power nature of a Telecom system and the necessity of cost-effective design stipulate the use of special output characteristic. This characteristic specifies the operation modes of the system as presented in (Gadoura, *et al.*, 1999a). Three operation modes are recommended to achieve regulated output voltage and overload protection. The first mode is the constant-voltage mode, which is achieved by voltage controller. The second and third modes are the constant-power and constant-current modes, which are achieved by an overload controller. The nonlinearity of the modified-constant-power mode operation raises some difficulties in control design of the system. The fuzzy controllers are proposed for both loops: PID FLC for voltage-loop and PI FLC for current-loop. The fuzzy-logic controllers are designed in a simple way but with special structures. Although the analog control system based on cascaded approach is well proven in practice and shows excellent performance, the fuzzy-logic solution gives the same performance as analog design and has an advantage in DSP implementation. The practical analogue constant-voltage controller and overload protection controller are designed and it is experimentally proven that they ensure the stability and proper dynamics of operation. In addition, the simulation results show the potentialities of fuzzy-logic approach.

Also the IMC scheme is applied to regulate voltage-controlled-buck converter in order to achieve robust output voltage. The IMC structure has been obtained using the control-to-output transfer function, which is derived by using a small-signal model. The filter parameter is tuned to improve the dynamic performance of the system that can be selected according to the bandwidth of the closed-loop response. The IMC leads to a controller with a simple structure. In designing the IMC controller for voltage-controlled boost and buck-boost converters, the tuning of a single parameter has been selected by solving \mathcal{H}_∞ optimal control

criterion. The bandwidths are restricted due to their RHP-zeros. The stability properties have been clearly improved in terms of PM and GM. From the simulation results, it can be seen that the use of IMC controller provides good tracking performance and disturbance rejection capability. Also it provides robust stability and robust performance in the presence of uncertainties.

In parallel-connected configuration, the system of two-buck converters operating in CICM is considered in this thesis. However, the model is quite flexible to include n -buck converters connected in parallel. Also the same procedure can be followed to derive models of paralleled boost or buck-boost converters. The state-space representation of paralleled buck converters operating in CICM with VMC has been presented and analyzed. By defining the control constraint of PCMC, a new state-space representation of paralleled buck converters operating in CICM with PCMC is obtained. By presenting the system in state-space form, the system can be analyzed easily, i.e., controllability, observability, etc. The uncertainties for both plant and disturbance models are attained by determining the upper boundary of the relative errors that are produced by comparing every member of the perturbed model set to the nominal model. Whether the unstructured or structured uncertainty is used, the uncertainty model is only represented by the parameter variations of the system. The unstructured uncertainty has been represented using the multiplicative-input uncertainty that leads to better results than others, e.g., the additive uncertainty, the multiplicative-output uncertainty, etc. On the other hand, the structured uncertainty is modeled by comparing the most worst-case perturbed model to the nominal model. The worst-case can be defined as the perturbed model that produces the largest peak of the relative errors when comparing to the nominal model. These can clearly be seen in the graphical representations of the uncertainty. The \mathcal{H}_∞ controller is designed in order to achieve robust stability and robust performance. Also the \mathcal{H}_∞ LSD controller is designed based on McFarlane-Glover method presented in (McFarlane and Glover, 1989). The RS and RP are achieved when the two-paralleled-buck converters are in PCMC. However they are not ensured with VMC because of the extreme resonant peaks that cannot be treated. The simulation results demonstrate the effectiveness of \mathcal{H}_∞ controller and \mathcal{H}_∞ LSD controller that provide robust stability and robust performance and show good tracking performance and disturbance rejection capability in the presence of uncertainties.

A procedure to split the system of paralleled DC/DC converters into two subsystems, voltage-loop and current-loop is proposed and studied in order to reduce the controller order when synthesizing and to match the practical proven method of tuning the controllers. The voltage-loop consists of n subsystems that help to design each one separately. The PID controllers are designed to regulate the voltage-loop and to achieve the robust performance and robust stability in the presence of the uncertainty. The MIMO PI controller is designed to regulate the current-loop of the system where the outputs are injected into their voltage-loops. The decentralized MIMO PI controller is succeeded to achieve the robust performance and robust stability of the current-loop. The overall system has good rejection ability of line and load disturbances with zero steady-state error, small peaks, and fast recovery time. This procedure can be used to design the \mathcal{H}_∞ controllers for both loops. However the uncertainty models for voltage-loop have larger peaks that make the controller synthesis very difficult, if possible.

According to the simulation results of the output voltages and currents, the PI/PID controllers give the best results comparing with other techniques. However, the description of the uncertainty that is used in order to design robust PI/PID controllers is less conservative than others. The better results are, therefore, expected.

6.3 Author's Contribution

This work is actually an extended version of previous work reported in (Gadoura, 1999). The main contribution in this thesis can be summarized in the following points:

- The fuzzy-logic controllers that are used to ensure a robust output and to achieve an output characteristic of a Telecom power supply are successfully implemented and tested.
- A novel application of IMC to DC/DC converters is presented and examined for basic converters: buck, boost, buck-boost. The simulation results show the suitability of IMC to power converters.
- The state-space representation of paralleled DC/DC converters operating in CICM is derived for VMC and PCMC configurations. The analysis and control design are quite straightforward utilizing available techniques for state-space model. Also the interactions are treated in proper way.
- The \mathcal{H}_∞ and \mathcal{H}_2 loop-shaping control are effectively applied to paralleled DC/DC converters. The uncertainty representation plays the main key point in designing the robust controllers. By analyzing the uncertainty models, some constraints in designing and controlling of power converters are raised.

6.4 Future Trends

More research work should be done in modeling and control design of paralleled DC/DC converters. In modeling, the input filter should be included due to its effect on the stability properties of the system as proven in (Suntio, *et al.*, 2000a) and (Suntio, *et al.*, 2002). In control design, the non-conservative robust control should be applied in order to achieve better dynamic performance than conservative control presented in this thesis. Also the decentralized controller is only used in practice where each module has its own control circuit increasing the system's reliability. The decentralized \mathcal{H}_∞ control should be utilized and applied. It should also be compared with the existing controllers that are presented in [P1] and used in reality.

Due to DSP implementation, the sampled-data version of robust controller should be designed. Also the model reduction that is used in [P3] to reduce the controller's order should be studied in order to reduce the order of closed-loop system maintaining the robustness issues.

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Appendix A

Multiplicative Uncertainty Model Procedure

Consider a finite dimensional linear time-invariant system (FDLTI) modeled by the state-space representation

$$\begin{aligned}\dot{\mathbf{x}}(t) &= \mathbf{A} \mathbf{x}(t) + \mathbf{B} \mathbf{c}(t) \\ \mathbf{y}(t) &= \mathbf{C} \mathbf{x}(t) + \mathbf{D} \mathbf{c}(t)\end{aligned}\tag{A1}$$

where $\mathbf{x}(t) \in \mathcal{R}^n$, $\mathbf{c}(t) \in \mathcal{R}^m$, and $\mathbf{y}(t) \in \mathcal{R}^p$. The corresponding transfer matrix from $\mathbf{c}(t)$ to $\mathbf{y}(t)$ is defined by using *Laplace* transformation as

$$\mathbf{y}(s) = \mathbf{G}(s) \mathbf{c}(s)\tag{A2}$$

where $\mathbf{G}(s) = \mathbf{D} + \mathbf{C}(s\mathbf{I} - \mathbf{A})^{-1} \mathbf{B}$ and $\mathbf{x}(0) = [0]$. Also the transfer matrix can be put in the following notation:

$$\mathbf{G}(s) := \left[\begin{array}{c|c} \mathbf{A} & \mathbf{B} \\ \hline \mathbf{C} & \mathbf{D} \end{array} \right]\tag{A3}$$

The inverse of transfer matrix $\mathbf{G}(s)$ can be derived by using the well-known matrix inversion lemma, i.e., $(\mathbf{A}_1 + \mathbf{A}_2 \mathbf{A}_3 \mathbf{A}_4)^{-1} = \mathbf{A}_1^{-1} - \mathbf{A}_1^{-1} \mathbf{A}_2 (\mathbf{A}_4 \mathbf{A}_1^{-1} \mathbf{A}_2 + \mathbf{A}_3^{-1})^{-1} \mathbf{A}_4 \mathbf{A}_1^{-1}$.

$$\begin{aligned}\mathbf{G}^{-1}(s) &= \mathbf{D}^{-1} - \mathbf{D}^{-1} \mathbf{C} (\mathbf{B} \mathbf{D}^{-1} \mathbf{C} + s\mathbf{I} - \mathbf{A})^{-1} \mathbf{B} \mathbf{D}^{-1} \\ &= \mathbf{D}^{-1} - \mathbf{D}^{-1} \mathbf{C} (s\mathbf{I} - (\mathbf{A} - \mathbf{B} \mathbf{D}^{-1} \mathbf{C}))^{-1} \mathbf{B} \mathbf{D}^{-1}\end{aligned}\tag{A4}$$

$$\mathbf{G}^{-1}(s) := \left[\begin{array}{c|c} \mathbf{A} - \mathbf{B}\mathbf{D}^{-1}\mathbf{C} & -\mathbf{B}\mathbf{D}^{-1} \\ \hline \mathbf{D}^{-1}\mathbf{C} & \mathbf{D}^{-1} \end{array} \right] \quad (\text{A5})$$

Also the equation (A5) has been presented in (Zhou and Doyle, 1998). If \mathbf{D} is not a squared matrix, the pseudo-inverse is used to obtain \mathbf{D}^{-1} .

Remark 1: If the system is strictly proper, i.e., $\mathbf{D} = [0]$, the state-space representation of its inverse cannot be realized. To overcome this problem, the output equation should be differentiated, i.e., an extra pole should be added to the inverse of the system that will be proper, then the state-space representation is realized.

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{A} \mathbf{x}(t) + \mathbf{B} \mathbf{c}(t) \\ \mathbf{y}(t) &= \mathbf{C} \mathbf{x}(t) \Rightarrow \dot{\mathbf{y}}(t) = \mathbf{C} \dot{\mathbf{x}}(t) = \mathbf{C}\mathbf{A} \mathbf{x}(t) + \mathbf{C}\mathbf{B} \mathbf{c}(t) \end{aligned} \quad (\text{A6})$$

The transfer matrix can be written as

$$\tilde{\mathbf{G}}(s) = \mathbf{C}\mathbf{B} + \mathbf{C}\mathbf{A}(s\mathbf{I} - \mathbf{A})^{-1} \mathbf{B} \quad (\text{A7})$$

$$\tilde{\mathbf{G}}(s) := \left[\begin{array}{c|c} \mathbf{A} & \mathbf{B} \\ \hline \mathbf{C}\mathbf{A} & \mathbf{C}\mathbf{B} \end{array} \right] \quad (\text{A8})$$

Once more, by using the matrix inversion lemma, the inverse of transfer matrix $\tilde{\mathbf{G}}(s)$ can be obtained as:

$$\begin{aligned} \tilde{\mathbf{G}}^{-1}(s) &= (\mathbf{C}\mathbf{B})^{-1} - (\mathbf{C}\mathbf{B})^{-1} \mathbf{C}\mathbf{A} \left(\mathbf{B}(\mathbf{C}\mathbf{B})^{-1} \mathbf{C}\mathbf{A} + s\mathbf{I} - \mathbf{A} \right)^{-1} \mathbf{B}(\mathbf{C}\mathbf{B})^{-1} \\ &= (\mathbf{C}\mathbf{B})^{-1} - (\mathbf{C}\mathbf{B})^{-1} \mathbf{C}\mathbf{A} \left(s\mathbf{I} - \left(\mathbf{A} - \mathbf{B}(\mathbf{C}\mathbf{B})^{-1} \mathbf{C}\mathbf{A} \right) \right)^{-1} \mathbf{B}(\mathbf{C}\mathbf{B})^{-1} \end{aligned} \quad (\text{A9})$$

$$\tilde{\mathbf{G}}^{-1}(s) := \left[\begin{array}{c|c} \mathbf{A} - \mathbf{B}(\mathbf{C}\mathbf{B})^{-1} \mathbf{C}\mathbf{A} & -\mathbf{B}(\mathbf{C}\mathbf{B})^{-1} \\ \hline (\mathbf{C}\mathbf{B})^{-1} \mathbf{C}\mathbf{A} & (\mathbf{C}\mathbf{B})^{-1} \end{array} \right] \quad (\text{A10})$$

Also note that if $\mathbf{C}\mathbf{B}$ is not a squared matrix, the pseudo-inverse is used to obtain $(\mathbf{C}\mathbf{B})^{-1}$.

Remark 2: According to Remark 1, the multiplicative-input uncertainty can be derived by defining the upper boundary of all possible relative errors between the perturbed plant $\mathbf{G}_p(s)$ and the nominal model $\mathbf{G}(s)$, which is used to model uncertainty presented in [P2-P4,P8].

$$\left\| \mathbf{G}^{-1}(s) [\mathbf{G}_p(s) - \mathbf{G}(s)] \right\|_{\infty} \leq |\mathbf{w}_i(s)| \quad (\text{A11})$$

Since \mathbf{G}^{-1} is not realized, $\tilde{\mathbf{G}}^{-1}$ should be used instead. However, $\tilde{\mathbf{G}}_p$ should be used as well.

$$\tilde{\mathbf{G}}_p(s) := \left[\begin{array}{c|c} \mathbf{A}_p & \mathbf{B}_p \\ \hline \mathbf{C}_p \mathbf{A}_p & \mathbf{C}_p \mathbf{B}_p \end{array} \right] \quad (\text{A12})$$

which leads to conclude that

$$\tilde{\mathbf{G}}^{-1}(s) [\tilde{\mathbf{G}}_p(s) - \tilde{\mathbf{G}}(s)] = \mathbf{G}^{-1}(s) [\mathbf{G}_p(s) - \mathbf{G}(s)] \quad (\text{A13})$$

Note that it is also the same for multiplicative-output uncertainty.

$$[\tilde{\mathbf{G}}_p(s) - \tilde{\mathbf{G}}(s)] \tilde{\mathbf{G}}^{-1}(s) = [\mathbf{G}_p(s) - \mathbf{G}(s)] \mathbf{G}^{-1}(s) \quad (\text{A14})$$

Appendix B

MATLAB™/SIMULINK™ Simulation Setup

B.1 How to Model Uncertainty?

In order to model uncertainty, we have implemented the state-space model with nominal parameters that is used to express the transfer matrices of the system. All possible perturbed models have been generated by constructing number of inner loops that depend on number of uncertain components. For each loop, the \mathcal{H}_∞ norm of the relative errors is plotted. In modeling of unstructured uncertainty, we have to obtain the transfer function of an upper bound of the relative errors' plots, e.g., as shown in Fig. 5.16, which is implemented into Fig. 2.5 as a diagonal matrix as a multiplicative-input uncertainty. In modeling of structure uncertainty, we have to obtain the state-space representation of worst-case, if we admit that the worst-case that gives the largest peak in the relative errors' plots. Then, the perturbed model will be compared with the nominal model to derive the uncertainty model.

B.1.1 Single-Loop Approach

```
1 % 1.Consider two-buck converters connected in parallel and feeding
2 % common load, which is here a resistive load. However, in reality,
3 % a Telecom load is a constant-power load due to its nature.
4 % 2.This code will generate 2^11=2048 perturbed model that can be
5 % compared to the nominal model in order to model the uncertainty.
6 % 3.We assume that the system operates in CICM with VMC, however, the
7 % code is applicable to the system with PCMC as well.
8 %
9 R_L=11; %The resistive load
10 r_L=20e-3; %A cable resistance from bus-bar to load
11 Ts=1/100e3; %The switching time interval
12 Vref=54; %The reference voltage
13 %
14 % The parameters of first module
15 %
16 L1=100e-6;
17 C1=1000e-6;
```

```

18 rC1=50e-3;
19 rL1=15e-3;
20 Vin1=140;
21 D1=Vref/Vin1;
22 r1=20e-3;
23 rp1=10e-3;
24 %
25 % The parameters of second module
26 %
27 L2=100e-6;
28 C2=1000e-6;
29 rC2=50e-3;
30 rL2=15e-3;
31 Vin2=140;
32 D2=Vref/Vin2;
33 r2=20e-3;
34 rp2=10e-3;
35 %
36 % Generate the "M" matrices of nominal model that are presented in
37 % Chapter 2
38 %
39 Mp=[R_L+r_L+rp1 R_L+r_L;R_L+r_L R_L+r_L+rp2];
40 Mvc_1=diag([C1*(rC1+r1),C2*(rC2+r2)])+Mp*diag([C1,C2]);
41 Mr=[R_L R_L]';
42 Mvc=inv(Mvc_1);
43 Mic=Mvc*Mp+Mvc*diag([r1,r2]);
44 Mgc=Mvc*Mr;
45 Min=diag([1/L1,1/L2]);
46 Min_D=Min*diag([D1,D2]);
47 Min_V=Min*diag([Vin1,Vin2]);
48 Mil=diag([rL1/L1,rL2/L2])+diag([rC1*C1/L1,rC2*C2/L2])*Mic;
49 Mvl=Min-dia([rC1*C1/L1,rC2*C2/L2])*Mvc;
50 Mgl=diag([rC1*C1/L1,rC2*C2/L2])*Mgc;
51 Mii=eye(2)-diag([C1,C2])*Mic;
52 Mvi=diag([C1,C2])*Mvc;
53 Mig=diag([C1,C2])*Mgc;
54 %
55 % The feedback voltage (v_j)
56 %
57 Miv=diag([rC1,rC2])-diag([rC1,rC2])*Mii;
58 Mvv=eye(2)-diag([rC1,rC2])*Mvi;
59 Mvg=-diag([rC1,rC2])*Mig;
60 %
61 % The state-space representation of nominal model
62 %
63 A=[-Mil -Mvl;Mic -Mvc];
64 B=[Min_V;zeros(2)];
65 E=[Min_D Mgl;zeros(2) -Mgc];
66 C=[Miv Mvv;Mii Mvi];
67 F=[zeros(2) Mvg;zeros(2) Mig];
68 %
69 % The transfer matrices
70 %
71 Gp=pck(A,B,C*A,C*B);
72 Gd=pck(A,E,C,F);
73 %
74 % The inverse transfer matrices
75 %
76 CB_inv=pinv(C*B);
77 Gp_inv=pck(A-B*CB_inv*C*A,-B*CB_inv,CB_inv*C*A,CB_inv);
78 F_inv=pinv(F);
79 Gd_inv=pck(A-E*F_inv*C,-E*F_inv,F_inv*C,F_inv);

```

```

80 %
81 omega=logspace(-2,6,200);
82 figure(1)
83 hold
84 figure(2)
85 hold
86 %
87 % A Telecom load changed from 10% to 90% of full load (P_out_max =
88 % 500W). As a resistive load, which is proposed for simulation, 10% of
89 % P_out_max leads to R_L = 58ohms and 90% of P_out_max leads to R_L =
90 % 6.5ohms
91 %
92 for Q_R_L = [6.5 58];
93     R_L=Q_R_L;
94     for Q_L1 = [-0.1 0.1]
95         L1=100e-6;
96         L1=L1*(1+Q_L1);
97         for Q_C1 = [-0.2 0.1]
98             C1=1000e-6;
99             C1=C1*(1+Q_C1);
100             for Q_esr1 = [-0.5 0.5]
101                 rC1=50e-3;
102                 rL1=15e-3;
103                 rL1=rL1*(1+Q_esr1);
104                 rC1=rC1*(1+Q_esr1);
105                 for Q_Vin1 = [-20 20]
106                     Vin1=140;
107                     Vin1=Vin1+Q_Vin1;
108                     D1=Vref/Vin1;
109                     for Q_r1 = [-0.25 0.25]
110                         r1=20e-3;
111                         rp1=10e-3;
112                         r1=r1*(1+Q_r1);
113                         rp1=rp1*(1+Q_r1);
114                         for Q_L2 = [-0.1 0.1]
115                             L2=100e-6;
116                             L2=L2*(1+Q_L2);
117                             for Q_C2 = [-0.2 0.2]
118                                 C2=1000e-6;
119                                 C2=C2*(1+Q_C2);
120                                 for Q_esr2 = [-0.5 0.5]
121                                     rC2=50e-3;
122                                     rL2=15e-3;
123                                     rL2=rL2*(1+Q_esr2);
124                                     rC2=rC2*(1+Q_esr2);
125                                     for Q_Vin2 = [-20 20]
126                                         Vin2=140;
127                                         Vin2=Vin2+Q_Vin2;
128                                         D2=Vref/Vin2;
129                                         for Q_r2 = [-0.25 0.25]
130                                             r2=20e-3;
131                                             rp2=10e-3;
132                                             r2=r2*(1+Q_r2);
133                                             rp2=rp2*(1+Q_r2);
134                                         %
135                                         % Generate the "M" matrices of
136                                         % perturbed model
137                                         %
138                                         Mp=[R_L+r_L+rp1 R_L+r_L;R_L+r_L
139                                              R_L+r_L+rp2];
140                                         Mvc_1=diag([C1*(rC1+r1),C2*(rC2+r2)])
141                                         +Mp*diag([C1,C2]);

```

```

142 Mr=[R_L R_L]';
143 Mvc=inv(Mvc_1);
144 Mic=Mvc*Mp+Mvc*diag([r1,r2]);
145 Mgc=Mvc*Mr;
146 Min=diag([1/L1,1/L2]);
147 Min_D=Min*diag([D1,D2]);
148 Min_V=Min*diag([Vin1,Vin2]);
149 Mil=diag([rL1/L1,rL2/L2])
150 +diag([rC1*C1/L1,rC2*C2/L2])*Mic;
151 Mvl=Min-diag([rC1*C1/L1,rC2*C2/L2])
152 *Mvc;
153 Mgl=diag([rC1*C1/L1,rC2*C2/L2])*Mgc;
154 Mii=eye(2)-diag([C1,C2])*Mic;
155 Mvi=diag([C1,C2])*Mvc;
156 Mig=diag([C1,C2])*Mgc;
157 %
158 % The feedback voltage (v_j)
159 %
160 Miv=diag([rC1,rC2])
161 -diag([rC1,rC2])*Mii;
162 Mvv=eye(2)-diag([rC1,rC2])*Mvi;
163 Mvg=-diag([rC1,rC2])*Mig;
164 %
165 % The state-space representation of
166 % perturbed model
167 %
168 A_1=[-Mil -Mvl;Mic -Mvc];
169 B_1=[Min_V;zeros(2)];
170 E_1=[Min_D Mgl;zeros(2) -Mgc];
171 C_1=[Miv Mvv;Mii Mvi];
172 F_1=[zeros(2) Mvg;zeros(2) Mig];
173 %
174 % The transfer matrices and their
175 % inverses of perturbed model
176 %
177 Gpp=pck(A_1,B_1,C_1*A_1,C_1*B_1);
178 figure(1)
179 GGp=mmult(Gp_inv,msub(Gpp,Gp));
180 GGp_frq=frsp(GGp,omega);
181 vplot('liv,m',vnorm(GGp_frq));
182 %
183 Gdd=pck(A_1,E_1,C_1,F_1);
184 figure(2)
185 GGd=mmult(Gd_inv,msub(Gdd,Gd));
186 GGd_frq=frsp(GGd,omega);
187 vplot('liv,m',vnorm(GGd_frq));
188 end;
189 end;
190 end;
191 end;
192 end;
193 end;
194 end;
195 end;
196 end;
197 end;
198 end;

```


B.1.2 Two-Loop Approach

The uncertainty model can be obtained by using the same Matlab™-code that is used in previous section with some changes: use code (a) instead of lines (69-79) and use code (b) instead of lines (174-187).

```

1  % Code (a)
2  % Partition the plant model Gp = [Gpv | Gpi]'
3  % Partition the disturbance model Gd = [Gdv | Gdi]'
4  %
5  Gp=pck(A,B,C*A,C*B);
6  Gpv=sel(Gp,1:2,:);
7  [a_pv,b_pv,c_pv,d_pv]=unpck(Gpv);
8  Gpi=sel(Gp,3:4,:);
9  [a_pi,b_pi,c_pi,d_pi]=unpck(Gpi);
10 %
11 Gpv_inv=minv(Gpv);
12 Gpi_inv=minv(Gpi);
13 %
14 Gd=pck(A,E,C,F);
15 Gdv=sel(Gd,1:2,:);
16 [a_dv,b_dv,c_dv,d_dv]=unpck(Gdv);
17 Gdi=sel(Gd,3:4,:);
18 [a_di,b_di,c_di,d_di]=unpck(Gdi);
19 %
20 d_dv_inv=pinv(d_dv);
21 Gdv_inv=pck(a_dv-b_dv*d_dv_inv*c_dv,
22             -b_dv*d_dv_inv,d_dv_inv*c_dv,d_dv_inv);
23 d_di_inv=pinv(d_di);
24 Gdi_inv=pck(a_di-b_di*d_di_inv*c_di,
25             -b_di*d_di_inv,d_di_inv*c_di,d_di_inv);

1  % Code (b)
2  % The transfer matrices and their
3  % inverses of perturbed model
4  %
5  Gpp=pck(A_1,B_1,C_1*A_1,C_1*B_1);
6  Gppv=sel(Gpp,1:2,:);
7  Gppi=sel(Gpp,3:4,:);
8  figure(1)
9  GGpv=mmult(Gpv_inv,msub(Gppv,Gpv));
10 GGpv_frq=frsp(GGpv,omega);
11 vplot('liv,m',vnorm(GGpv_frq));
12 figure(2)
13 GGpi=mmult(Gpi_inv,msub(Gppi,Gpi));
14 GGpi_frq=frsp(GGpi,omega);
15 vplot('liv,m',vnorm(GGpi_frq));
16 %
17 Gdd=pck(A_1,E_1,C_1,F_1);
18 Gddv=sel(Gdd,1:2,:);
19 Gddi=sel(Gdd,3:4,:);
20 figure(3)
21 GGdv=mmult(Gdv_inv,msub(Gddv,Gdv));
22 GGdv_frq=frsp(GGdv,omega);
23 vplot('liv,m',vnorm(GGdv_frq));
24 figure(4)
25 GGdi=mmult(Gdi_inv,msub(Gddi,Gdi));
26 vplot('liv,m',vnorm(GGdi_frq));

```

B.2 How to Create the Interconnection Structure?

The system that is to be controlled, commonly referred to as the plant, may itself be the result of interconnecting various sorts of subsystems in series, in parallel, and in feedback. In addition, the plant is interfaced with sensors, actuators, and control system. Our model for the overall system represents all of these components in nominal form and will include components introduced to represent uncertainties. Simulink model, as shown in Fig. B.1, is used to present the interconnection model of the system. The Matlab files are used to derive the state-space representation of the interconnection model.

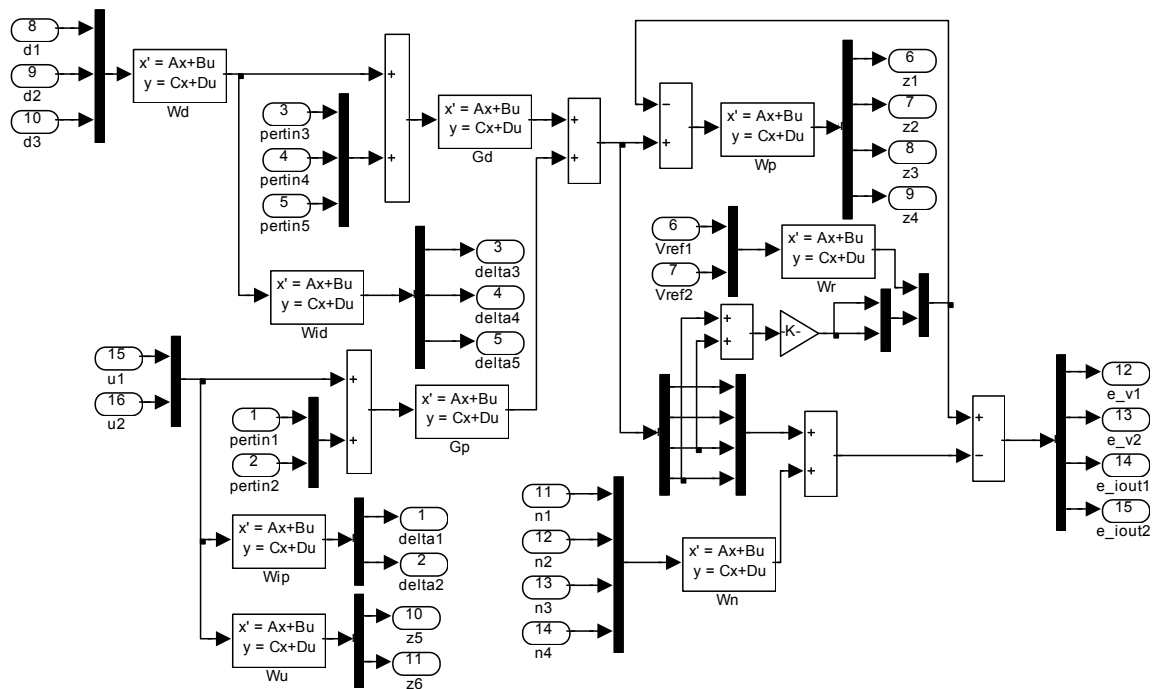


Fig. B.1 – The interconnection model P of Fig. 3.7(a). The state-space representation is derived using “*linmod*” command of Matlab.

B.2.1 Single-Loop Approach

```

1  Gp=pck(A,B,C,D);      %The nominal plant model
2  Gd=pck(A,E,C,F);      %The nominal disturbance model
3  %
4  % The uncertainty weights of plant model 'Wip' and of disturbance
5  % model 'Wid'
6  %
7  wip=nd2sys([1 1e4 1e8],[1 5463 2.9e7],0.97);
8  Wip=daug(wip,wip);
9  [Aip,Bip,Cip,Dip]=unpck(Wip);
10 %
11 wid=nd2sys([1 3.36e4 9.93e8],[1 6894 4.02e7],0.0068);
12 Wid=daug(wid,wid,wid);

```

```

13 [Aid,Bid,Cid,Did]=unpck(Wid);
14 %
15 % Perturbed models
16 %
17 Gpp=mmult(Gp,madd(eye(2),Wip)); %The perturbed plant model
18 [App,Bpp,Cpp,Dpp]=unpck(Gpp);
19 %
20 Gdd=mmult(Gd,madd(eye(3),Wid)); %The perturbed disturbance model
21 [Add,Bdd,Cdd,Ddd]=unpck(Gdd);
22 %
23 % The performance weight matrix 'Wp'
24 %
25 mp=2.5; ap=2e-1; wbp=1e3; np=1;
26 wpp1=nd2sys([1 wbp*(mp^(1/np))],[1 wbp*(ap^(1/np))],[1e-4/mp]^(1/np));
27 wpl=wpp1; %mmult(wpp1,wpp1,wpp1);
28 Wp=daug(wpl,wpl,wpl,wpl);
29 [Ap,Bp,Cp,Dp]=unpck(Wp);
30 %
31 %The noise weight matrix 'Wn'
32 %
33 mn=0.9; an=10; wbn=1e3; nn=1;
34 wnn=nd2sys([1 wbn*(mn^(1/nn))],[1 wbn*(an^(1/nn))],[1/mn]^(1/nn));
35 wn=wnn; %mmult(wnn,wnn,wnn);
36 Wn=daug(wn,wn,wn,wn);
37 [An,Bn,Cn,Dn]=unpck(Wn);
38 %
39 %The control command weight matrix 'Wu'
40 %
41 muu=0.9; au=2; wbu=1e5; nuu=1;
42 wuu=nd2sys([1 wbu*(muu^(1/nuu))],[1 wbu*(au^(1/nuu))],[1/muu]^(1/nuu));
43 [1 wbu*(au^(1/nuu))],[1/muu]^(1/nuu));
44 wu=wuu;%mmult(wuu,wuu,wuu);
45 Wu=daug(1,1); %daug(wu,wu);
46 [Au,Bu,Cu,Du]=unpck(Wu);
47 %
48 % Scaling matrices
49 %
50 Wr=daug(54,54); %The reference voltage scaling matrix
51 [Ar,Br,Cr,Dr]=unpck(Wr);
52 %
53 Wd=daug(20e-3,20e-3,5e-3); %The disturbance scaling matrix
54 [Ad,Bd,Cd,Dd]=unpck(Wd);
55 %
56 % The interconnection model 'Gp_ic'
57 %
58 [Aic,Bic,Cic,Dic]=linmod('P_ic');
59 Gp_ic=pck(Aic,Bic,Cic,Dic);

```

B.2.2. Two-Loop Approach

```

1 Gp=pck(A,B,C,D);
2 Gpv=sel(Gp,1:2,:); %The nominal plant model for VL
3 [a_pv,b_pv,c_pv,d_pv]=unpck(Gpv);
4 Gpi=sel(Gp,3:4,:); %The nominal disturbance model for VL
5 [a_pi,b_pi,c_pi,d_pi]=unpck(Gpi);
6 %
7 Gd=pck(A,E,C,F);
8 Gdv=sel(Gd,1:2,:); %The nominal plant model for CL
9 Gdv_hat=sbs(mscl(madd(sel(Gdv,:,1),sel(Gdv,:,2)),0.5),sel(Gdv,:,3));
10 [a_dv,b_dv,c_dv,d_dv]=unpck(Gdv);
11 Gdi=sel(Gd,3:4,:); %The nominal disturbance model for CL

```

```

12 Gdi_hat=sbs(mscl(madd(sel(Gdi,:),1),sel(Gdi,:),2)),0.5),sel(Gdi,:),3));
13 [a_di,b_di,c_di,d_di]=unpck(Gdi);
14 %
60 % The uncertainty weights of plant model 'Wipv' and of disturbance
15 % model 'Widv' for VL
16 %
17 wipv=nd2sys([1 5163 5.9168e6],[1 1226 1.277e7],0.85632);
18 Wipv=daug(wipv,wipv);
19 [Aipv,Bipv,Cipv,Dipv]=unpck(Wipv);
20 %
21 widv=mmult(nd2sys([1 1.889e4],[1 139.1],0.49494),
22            nd2sys([1 2054 1.642e6],[1 1913 1.405e7],1));
23 Widv=daug(widv,widv,widv);
24 [Aidv,Bidv,Cidv,Didv]=unpck(Widv);
25 %
61 % The uncertainty weights of plant model 'Wipi' and of disturbance
26 % model 'Widi' for CL
27 %
28 wipi=nd2sys([1 4040 7.824e6],[1 1349 1.297e7],2.1054);
29 Wipi=daug(wipi,wipi);
30 [Aipi,Bipi,Cipi,Dipi]=unpck(Wipi);
31 %
32 widi=mmult(nd2sys([1 1339 1.148e6],[1 2771 6.303e6],0.017243),
33            nd2sys([1 2.073e4 1.285e8],[1 1818 1.329e7],1));
34 Widi=daug(widi,widi,widi);
35 [Aidi,Bidi,Cidi,Didi]=unpck(Widi);
36 %
37 % The performance weight matrix 'Wpv' for VL
38 %
39 mpv=1.2; apv=1e-3; wbpv=1e3; npv=1;
40 wppv1=nd2sys([1 wbpv*(mpv^(1/npv))],[1 wbpv*(apv^(1/npv))],
41             (1e-5/mpv)^(1/npv));
42 wpv1=wppv1;%mmult(wppv1,wppv1);
43 Wpv= daug(wpv1,wpv1);
44 [Apv,Bpv,Cpv,Dpv]=unpck(Wpv);
45 %
46 % The noise weight matrix 'Wnv' for VL
47 %
48 mnv=0.5; anv=1.1; wbnv=1e5; nnv=1;
49 wnnv=nd2sys([1 wbnv*(mnv^(1/nnv))],
50            [1 wbnv*(anv^(1/nnv))],(1/mnv)^(1/nnv));
51 wnv=wnnv;%mmult(wnnv,wnnv,wnnv);
52 Wnv=daug(wnv,wnv);
53 [Anv,Bnv,Cnv,Dnv]=unpck(Wnv);
54 %
55 % The performance weight matrix 'Wni' for CL
56 %
57 mpi=1.2; api=1e-3; wbpi=1e3; npi=1;
58 wppil=nd2sys([1 wbpi*(mpi^(1/npi))],
59            [1 wbpi*(api^(1/npi))],(1/mpi)^(1/npi));
60 wpil=wppil;%mmult(wppil,wppil,wppil);
61 Wpi= daug(wpil,wpil);
62 [Api,Bpi,Cpi,Dpi]=unpck(Wpi);
63 %
64 % The noise weight matrix 'Wni' for CL
65 %
66 mni=0.5; ani=1.1; wbni=1e5; nni=1;
67 wnni=nd2sys([1 wbni*(mni^(1/nni))],
68            [1 wbni*(ani^(1/nni))],(1/mni)^(1/nni));
69 wni=wnni;%mmult(wnni,wnni,wnni);
70 Wni=daug(wni,wni);
71 [Ani,Bni,Cni,Dni]=unpck(Wni);

```

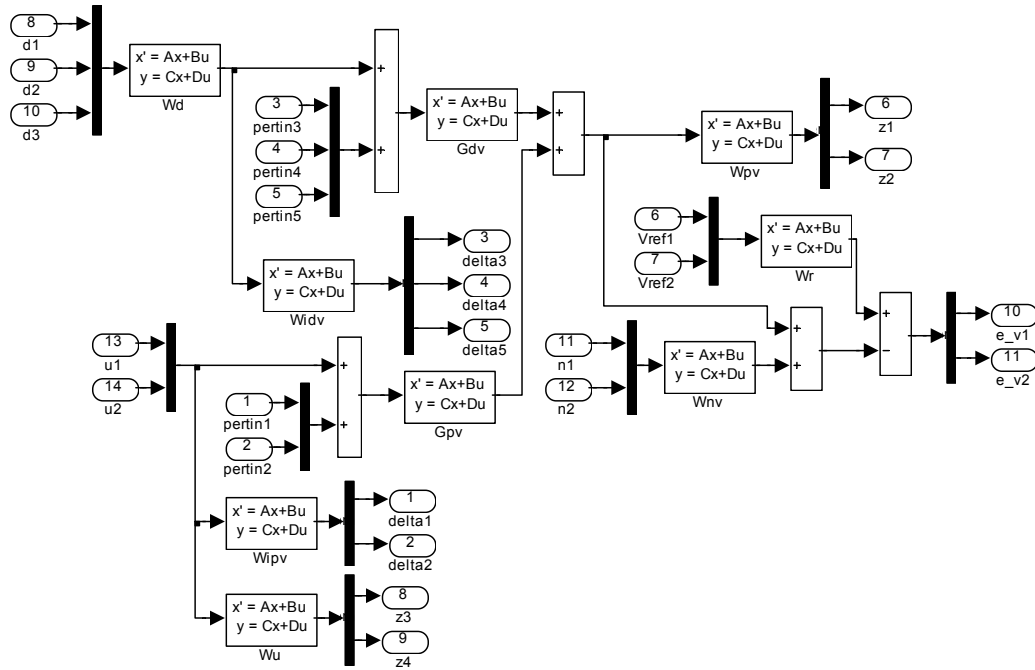


Fig. B.2 – The interconnection model P_u of Fig. 3.8(a) that is used to design a stabilizing controller of voltage-loop.

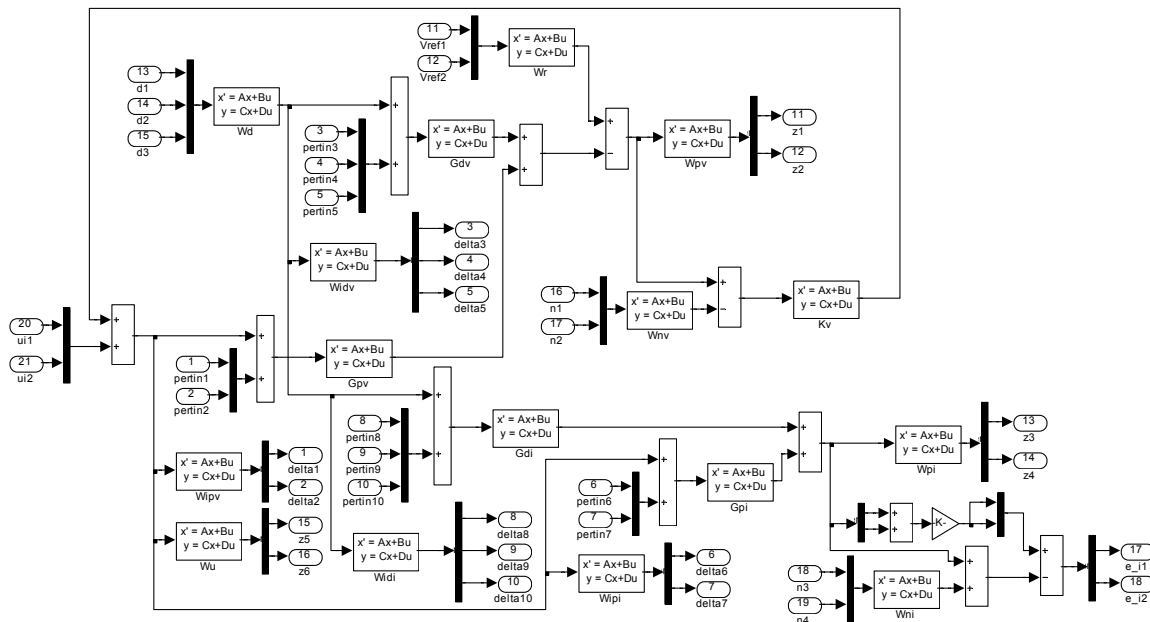


Fig. B.3 – The interconnection model P of Fig. 3.9(a) that is used to design a stabilizing controller of current-loop.

```

72 %
73 % The control command weight matrix 'Wu'
74 %
75 muu=0.1; au=3; wbu=1e6; nuu=1;
76 wu=nd2sys([1 wbu*(muu^(1/nuu))],
77           [1 wbu*(au^(1/nuu))],(1/muu)^(1/nuu));
78 Wu=daug(wu,wu);
79 [Au,Bu,Cu,Du]=unpck(Wu);
80 %
81 % Scaling matrices
82 %
83 Wr=daug(54,54); %The reference voltage scaling matrix
84 [Ar,Br,Cr,Dr]=unpck(Wr);
85 %
86 Wd=daug(20e-3,20e-3,5e-3); %The disturbance scaling matrix
87 [Ad,Bd,Cd,Dd]=unpck(Wd);
88 %
89 % The interconnection model for VL 'P_ic_VoltageLoop'
90 %
91 [Aicv,Bicv,Cicv,Dicv]=linmod('P_ic_VoltageLoop');
92 P_ic_VoltageLoop=pck(Aicv,Bicv,Cicv,Dicv);
93 %
94 % The interconnection model for CL 'P_ic_CurrentLoop'
95 %
96 [Aici,Bici,Cici,Dici]=linmod('P_ic_CurrentLoop');
97 P_ic_CurrentLoop=pck(Aici,Bici,Cici,Dici);

```

B.3. \mathcal{H}_∞ Controller with μ Plots Evaluation

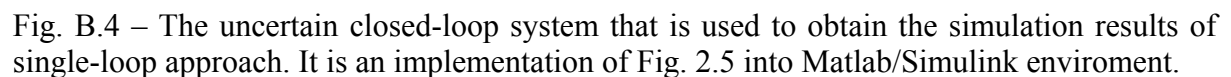
The following Matlab™ files and Simulink™ models are used to design a stabilizing \mathcal{H}_∞ controller and to use μ -analysis to evaluate the control design.

B.3.1. Single-Loop Approach

```

1  [K_H_inf,CL_H_inf]=hinfsyn(Gp_ic,4,2,1,10,0.001,2);
2  omega=logspace(-4,8,100);
3  %
4  K_H_inf_fr=frsp(K_H_inf,omega); %The H_inf controller frq. resp.
5  figure(1)
6  vplot('bode',K_H_inf_fr);
7  %
8  CL_H_inf_fr=frsp(CL_H_inf,omega); %The closed-loop frq. resp.
9  figure(2)
10 vplot('liv,m',vsvd(CL_H_inf_fr));
11 %
12 % Examine the nominal performance NP and the robust stability RS
13 %
14 rs_H_inf=sel(CL_H_inf_fr,1:5,1:5); %For RS
15 np_H_inf=sel(CL_H_inf_fr,6:11,6:14); %For NP
16 figure(3)
17 vplot('liv,m',vnorm(rs_H_inf),vnorm(np_H_inf));
18 %
19 % Examine the robust performance RP
20 %
21 bnds_rp=mu(CL_H_inf_fr,[5 5;9 6]); %For RP
22 figure(4)
23 vplot('liv,m',bnds_rp);

```



A. For Voltage-Loop

A14

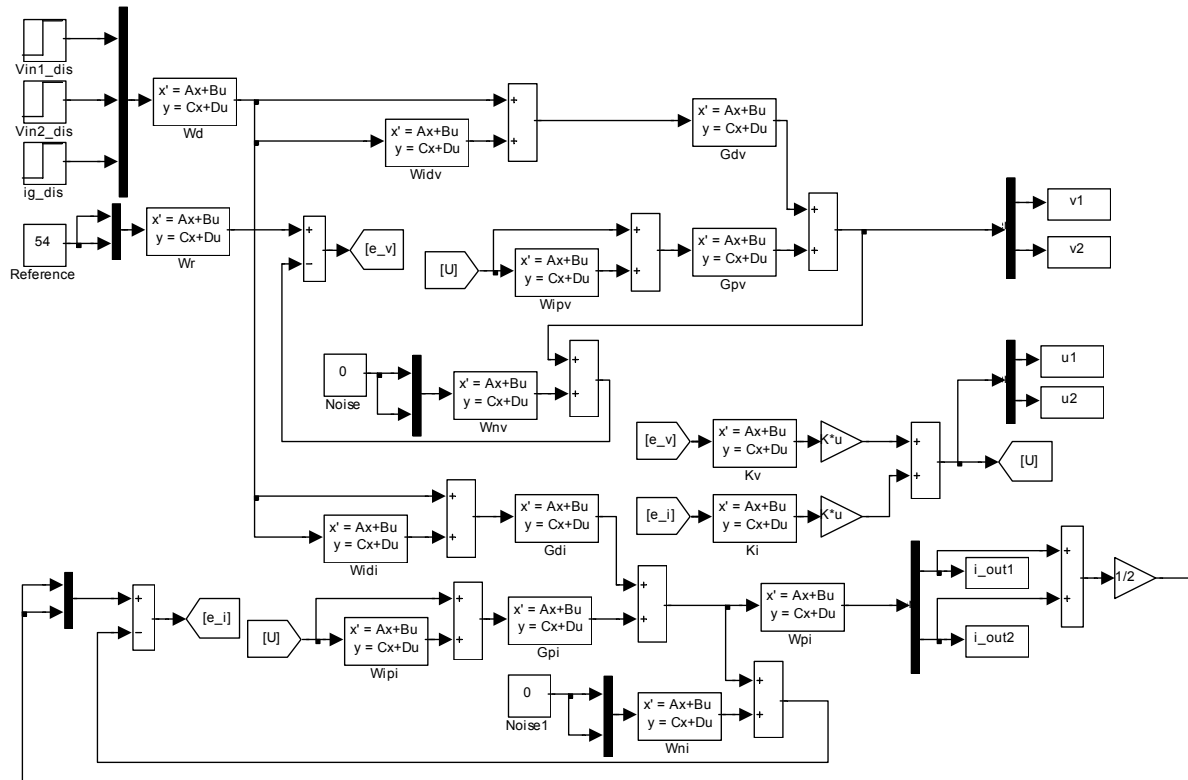


Fig. B.5 – The uncertain closed-loop system that is used to obtain the simulation results of two-loop approach. The multiplicative-input uncertainty is used.

```
28 figure(4)
29 vplot('liv,m',bnds_rpv);
```

B. For Current-Loop

```
1 % The interconnection model for CL 'P_ic_CurrentLoop'
2 %
3 [Aicvd,Bicvd,Cicvd,Dicvd]=linmod('P_ic_CurrentLoop ');
4 G_ic_CurrentLoop =pck(Aicvd,Bicvd,Cicvd,Dicvd);
5 %
6 % H_inf controller synthesis
7 %
8 [Kd_H_inf,CLd_H_inf]=hinfsyn(G_ic_CurrentLoop,2,2,1,10,0.001,2);
9 omega=logspace(-4,8,100);
10 Kd_H_inf_fr=frsp(Kd_H_inf,omega); %The H_inf controller frq. resp.
11 figure(1)
12 vplot('bode',Kd_H_inf_fr);
13 %
14 CLd_H_inf_fr=frsp(CLd_H_inf,omega); %The closed-loop frq. resp.
15 figure(2)
16 vplot('liv,m',vsvd(CLd_H_inf_fr));
17 %
18 % Examine the nominal performance NP and the robust stability RS
19 %
20 rsd_H_inf=sel(CLd_H_inf_fr,1:10,1:10); %For RS
21 npd_H_inf=sel(CLd_H_inf_fr,11:16,11:19); %For NP
```



```

22 figure(3)
23 vplot('liv,m',vnorm(rsd_H_inf),vnorm(npd_H_inf));
24 %
25 % Examine the robust performance RP
26 %
27 bnds_rpd=mu(Cld_H_inf_fr,[10 10;9 6]); %For RP
28 figure(4)
29 vplot('liv,m',bnds_rpd);

```

B.4 \mathcal{H}_∞ LSD Controller with μ Plots Evaluation

The following Matlab™ files and Simulink™ models are used to design the \mathcal{H}_∞ LSD controller and to use μ -analysis to evaluate the control design.

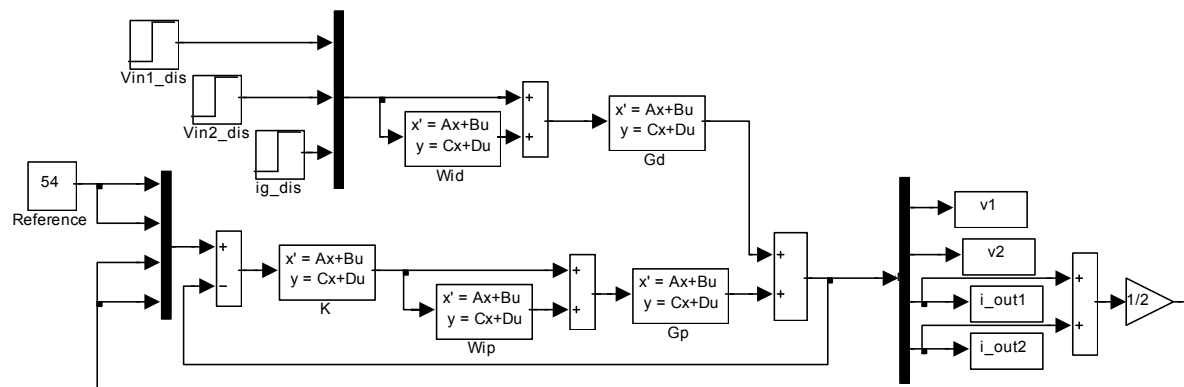


Fig. B.6 – The uncertain closed-loop system that is used to obtain the simulation results of \mathcal{H}_∞ LSD controller. The multiplicative-input uncertainty is used.

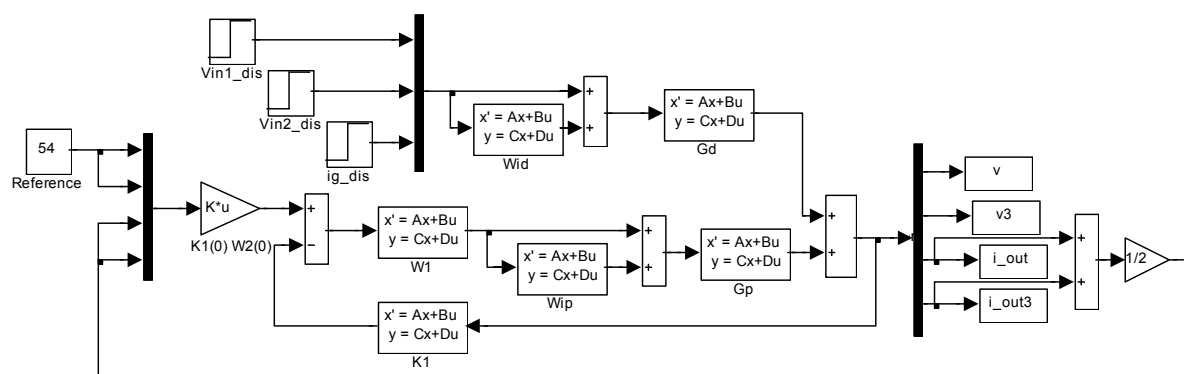


Fig. B.7 – The special arrangement of Fig B.6 that is used to reduce overshooting when designing the \mathcal{H}_∞ LSD controller.

```

1  omega=logspace(-2,8,100);
2  Gp_fr=frsp(Gp,omega);           %The nominal plant freq. resp.
3  %
4  % The interconnection model 'P_ic' for loop-shaping design
5  %
6  [Aic,Bic,Cic,Dic]=linmod('P_ic');
7  G_ic=pck(Aic,Bic,Cic,Dic);
8  %
9  % Shaped plant by defining weihgts
10 % W_1= 0.3*[(s+10000)/s].*I2 and W_2 = I4
11 %
12 w_1=nd2sys([1 1e4],[1 0],0.3);
13 W_1=daug(w_1,w_1);
14 [aw1,bw1,cw1,dw1]=unpck(W_1);
15 W_2=daug(1,1,1,1);
16 Gps=sel(G_ic,12:15,15:16);
17 Gp_shaped=mmult(W_2,Gps,W_1);    %The shaped nominal plant
18 Gp_shaped_fr=frsp(Gp_shaped,omega);
19 figure(1)
20 vplot('liv,lm',vsvd(Gp_fr),'-.',vsvd(Gp_shaped_fr),':');
21 %
22 % H_inf loopshaping controller
23 %
24 [K1,e_max]=ncfsyn(Gp_shaped,1);
25 display(['e_max = 'num2str(e_max)]);
26 [ak1,bk1,ck1,dk1]=unpck(K1);
27 K1_dcgain=dcgain(ss(ak1,bk1,ck1,dk1));
28 K=mmult(W_1,K1,W_2);            %The shaped controller
29 figure(2)
30 K_frq=frsp(K,omega);
31 vplot('liv,lm',vsvd(K_frq));
32 [Ak,Bk,Ck,Dk]=unpck(K);
33 cl_hls=starp(G_ic,K,4,2);
34 %
35 % Examine the nominal performance NP and the robust stability RS
36 %
37 rs_hls=sel(cl_hls,1:5,1:5);
38 np_hls=sel(cl_hls,6:11,6:14);
39 rs_hls_fr=frsp(rs_hls,omega);    %For RS
40 np_hls_fr=frsp(np_hls,omega);   %For NP
41 figure(3)
42 vplot('liv,m',vnorm(np_hls_fr),':',vnorm(rs_hls_fr),'-');
43 %
44 % Examine the robust performance RP
45 %
46 cl_hls_fr=frsp(cl_hls,omega);
47 bnds_rp=mu(cl_hls_fr,[5 5;9 6]); %For RP
48 figure(4)
49 vplot('liv,m',bnds_rp,':');

```

B.5 PID/PI Controllers With μ Plots Evaluation

We have used the following Simulink models to design and analyze the control system. The *Linear Analysis Tool*, which is available when using Simulink, is used in analysis.

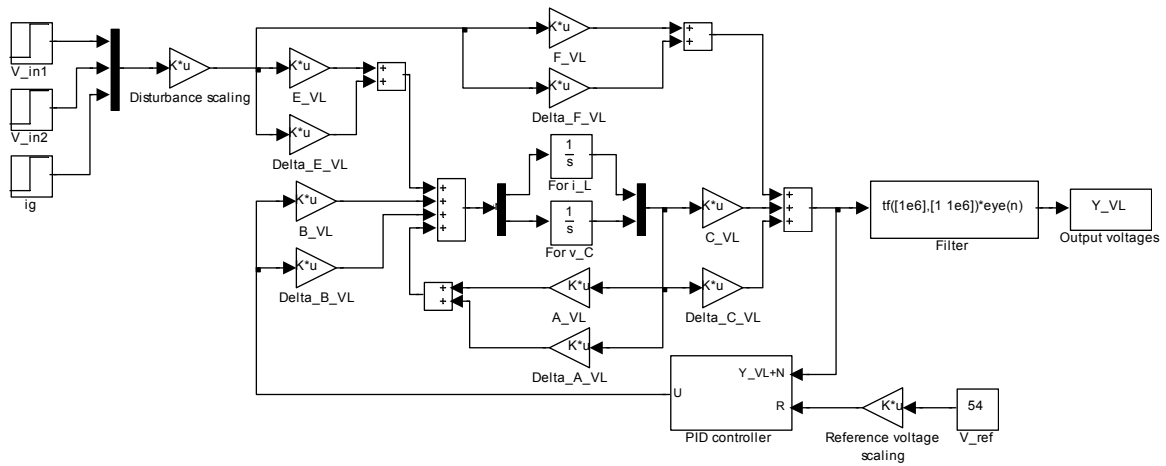


Fig. B.8 – The uncertain closed-loop system that is used to analyze and simulate the voltage-loop. The additive uncertainty is used.

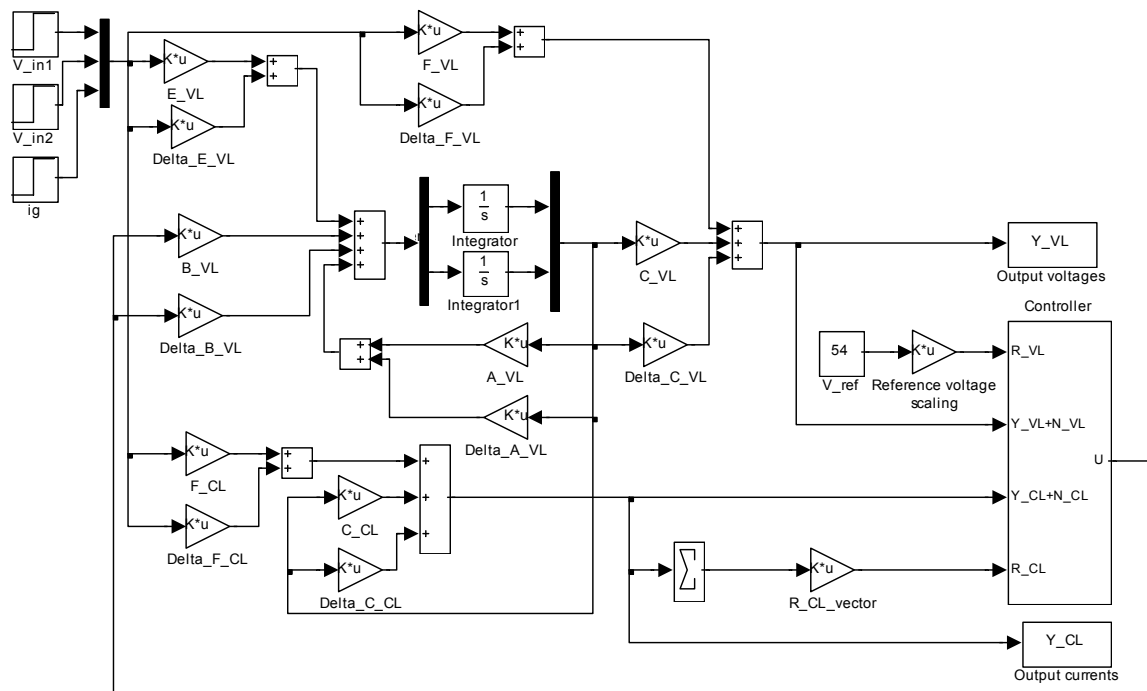


Fig. B.9 – The uncertain closed-loop system that is used to design the MIMO PI controller of current-loop and to analyze the overall system.

Appendix C

Glossary of Power Conversion Terms*

BACKUP BATTERY. One stage of a Telecom power supply, which is in parallel with a Telecom load powering it when AC power from the mains fails.

BANDWIDTH. A range of frequencies represents the highest frequency of disturbances at which there is enough overall gain to correct the error.

BODE PLOT. A graphic plot of gain versus frequency for a control loop, typically used to verify control loop stability, including phase margin.

BOOST CONVERTER. The step-up converter is another switching converter that has the same components as the buck converter, but this converter produces an output voltage greater than the source.

BUCK CONVERTER. The step-down converter can also be called a switch mode regulator. It generates an output voltage, which is greater than the input voltage.

BUCK-BOOST CONVERTER. The output voltage can be less than, or greater than the input voltage, however, the output polarity is opposite to the input polarity.

CONSTANT CURRENT POWER SUPPLY. A power supply designed to regulate the output current for changes in line, load, ambient temperature, and drift resulting from time.

CONSTANT VOLTAGE POWER SUPPLY. A power supply designed to regulate the output voltage for changes in line, load, ambient temperature, and drift resulting from time.

*This Glossary is collected from the web site of Power-One, Inc., <http://www.power-one.com>. Also some of them are from (Krien, 1998).

CONTROL CIRCUIT. A circuit in a closed-loop system, typically containing an error amplifier, which controls the operation of the system to achieve regulation.

CONVERTER. An electrical circuit, which accepts a DC, input and generates a DC output of a different voltage, usually achieved by high frequency switching action employing inductive and capacitive filter elements.

CURRENT PROGRAMMED CONTROL. The converter output is controlled by inserting a feedback of inductor current into a control circuit. The transistor switches on and off by such that the peak inductor current follows the control input signal.

CURRENT LIMITING. An overload protection circuit that limits the maximum output; current of a power supply in order to protect the load and/or the power supply.

CURRENT MODE. A control method for switch-mode converters where the converter adjusts its regulating pulse width in response to measured inductor current and output voltage, using a dual loop control circuit.

EFFICIENCY. The ratio of total output power to input power expressed as a percentage. Normally specified at full load and nominal input voltage.

EMI. Abbreviation for Electromagnetic Interference, which is the generation of unwanted noise during the operation of a power supply or other electrical or electronic equipment.

ESR. Equivalent Series Resistance. The value of resistance in series with an ideal capacitor, which duplicates the performance characteristics of a real capacitor.

FET. Field Effect Transistor, a majority carrier voltage controlled transistor.

FILTER. A frequency-sensitive network that attenuates unwanted noise and ripple components of a rectified output.

GAIN MARGIN. The inverse of the open loop gain magnitude at the frequency where the phase angle is 180° .

GROUND. An electrical connection to earth or some other conductor that is connected to earth. Sometimes the term "ground" is used in place of "common," but such usage is not correct unless the connection is also connected to earth.

INPUT FILTER. An internally or externally mounted low-pass or band-reject filter at the power supply input which reduces the noise fed into the power supply.

ISOLATION. Two circuits that are completely electrically separated with respect to DC potentials, and almost always also AC potentials. In power supplies, it is defined as the electrical separation of the input and output via the transformer.

LINE REGULATION. The change in output voltage when the AC input voltage is changed from minimum to maximum specified. It is usually a small value, and may be near zero with current mode control.

LOAD REGULATION. The change in output voltage when the load on the output is changed.

STABILITY. A system is said to be stable if it returns to the original operating conditions after being disturbed or altered.

MAINS. The utility AC power distribution wires.

MAXIMUM OUTPUT POWER. The absolute maximum output power that a power supply can produce without immediate damage.

MINIMUM LOAD. The minimum load current/power that must be drawn from the power supply in order for the supply to meet its performance specifications. Less frequently, a minimum load is required to prevent the power from failing.

OUTPUT IMPEDANCE. The ratio of change in output voltage to change in load current.

OUTPUT NOISE. The AC component that may be present on the DC output of a power supply. Switch-mode power supply output noise has two components: a lower frequency component at the switching frequency of the converter and a high frequency component due to fast edges of the converter switching transitions.

OVERLOAD PROTECTION. A power supply protection circuit that limits the output current under overload conditions.

OVERSHOOT. A transient output voltage change, which exceeds the high limit of the voltage accuracy specification and is caused by turning the power supply on or off, or abruptly changing line or load conditions.

PARALLEL OPERATION. Connecting the outputs of two or more power supplies with the same output voltage for the purpose of obtaining a higher output current. This requires power supplies specially designed for load sharing.

PHASE MARGIN. The difference angle $180^\circ - \varphi$, where φ is the phase of the transfer function at the crossover frequency.

POWER FACTOR. The ratio of true power to apparent power in an AC circuit. In power conversion technology, power factor is used in conjunction with describing the AC input current to the power supply.

POWER FAIL. A power supply interface signal, which gives a warning that the input voltage will no longer sustain full power, regulated output.

PULSE WIDTH MODULATION. A switching power conversion technique where the width of a duty cycles is modulated to control power transfer for regulating power supply outputs.

RECTIFIER. An electrical circuit, which accepts an AC input and generates a DC output voltage, usually achieved by employing diode elements.

REFLECTED RIPPLE CURRENT. The RMS or peak-to-peak AC current present at the input of the power supply, which is a result of the switching frequency of the converter.

REGULATION. The ability of a power supply to maintain an output voltage within a specified tolerance as referenced to changing conditions of input voltage and/or load.

RIPPLE AND NOISE. The amplitude of the AC component on the DC output of a power supply usually expressed in millivolts peak-to-peak. For a switching power supply, it is usually the switching frequency of the converter stage.

SWITCHING FREQUENCY. The rate at which the DC voltage is switched on and off during the pulse width modulation process in a switching power supply.

TOPOLOGY. The design type of a converter, indicative of the configuration of switching transistors, utilization of the transformer, and type of filtering. Examples of topologies are the buck, Boost, and Buck-Boost.

TRANSIENT RECOVERY TIME. The time required for an output voltage to be within specified accuracy limits after a step change in line or load conditions.

UNDERSHOOT. A transient output voltage change, which does not meet the low limit of the voltage accuracy specification and is caused by turning the power supply on or off, or abruptly changing line or load conditions.

UPS. A power supply, which continues to supply power during a loss of input power. Two types are the stand-alone UPS, which is located external to the equipment being powered, and the battery back-up power supply, which is embedded in the equipment being powered.

VOLTAGE MODE. A method of closed loop control of a switching converter where the pulse width is varied in response to changes in the output voltage to regulate the output.

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