HELSINKI UNIVERSITY OF TECHNOLOGY
Department of Electrical and Communication Engineering
Optoelectronics Laboratory
Espoo, Finland 2003

Defect and Yield Analysis of Semiconductor Components and Integrated Circuits

Mika Karilahti

Dissertation for the degree of Doctor of Science in Technology to be presented with due permission for public examination and debate in Auditorium S4 of the Department of Electrical and Communications Engineering at Helsinki University of Technology (Espoo, Finland) on the 14th of February, 2003, at 12 o'clock noon.

Helsinki University of Technology
Department of Electrical and Communications Engineering
Optoelectronics Laboratory
P.O. Box 3500
FIN-02015 HUT Espoo
Tel. +358-9-4511
Fax. +358-9-4513128

Contact information:
Email: mika.karilahti@hut.fi , mika@karilahti.com , URL: http://www.karilahti.com ,
Tel: +358-40-5487656

ISBN 951-22-6368-8 (Printed)
ISBN 951-22-6370-X (PDF)

Picaset Oy
Espoo, Finland 2003

Abstract

Semiconductors were studied from the point of material, component, electrical and functional properties. Several methods were used to accomplish this, e.g. X-ray topography, etch pit analysis, statistical methods, and neural nets.

The compound semiconductor components, i.e. GaAs varactor diodes, AlGaAs/InGaAs p-HEMTs, and LEDs (GaAs/AlGaAs and GaPN) were studied using the method of synchrotron X-ray topography.

First, the silicon wafers studied were selected from fully processed lots with varying, though, low yields. The electrical circuits were fabricated with a CMOS (Complementary Metal-Oxide Semiconductor) process, well suited for mixed-signal applications.

Then, synchrotron X-ray topographs and etch pit micrographs of the wafers were analyzed with an image processing software, written entirely for this study, to quantify the strain and defects present in the images. This information was then correlated with electrical parameters previously measured from the wafers, including the yield.

Several of the parameters quantified from the synchrotron X-ray images show a strong correlation with certain measured parameters, e.g. PMOS transistor threshold voltage, polysilicon sheet resistance, N- sheet contact chain resistance. Then, some parameters practically do not correlate, e.g. NMOS breakdown voltage. A strong correlation of device yield with near-surface strain measured by synchrotron X-ray topography is found.

Finally, the method of self-organizing map (SOM) neural net was applied to analyze a heartbeat rate monitor integrated circuit (IC) yield dependence on CMOS process control monitoring (PCM) data. The SOM efficiently reduces the PCM parameter space dimensions and helps in visualizing the different parameter relations. This makes it possible to identify the most probable PCM parameters affecting the yield. Those were found out to be NMOS transistor drain current and aluminum sheet resistance.

Keywords: semiconductor, compound semiconductor, wafer, component, part, device, measurement, synchrotron, x-ray, topography, etch pit, neural net, self-organizing map, SOM, integrated circuit, IC, CMOS, yield, process control monitoring, PCM, semiconductor process.

Preface

The work presented in this thesis has been carried out at the Optoelectronics Laboratory of Helsinki University of Technology in collaboration with Microelectronics Research Laboratory in Dublin, Institut in Freiburg, Germany, during 1993-2002. The synchrotron X-ray topography measurements were carried out at the Hamburger Synchrotronstrahlungslabor (HASYLAB) at the Deutches Elektronen-Synchrotron (DESY) in Hamburg, Germany. I want to thank all institutes for the facilities, resources, and services they have been able to provide, and all the very helpful people there.

I wish to express my gratitude to my thesis supervisor Professor Turkka Tuomi for his support and patience with my post-graduate studies, Dr. Patrick McNally for his ideas, Professor Olli Simula for his advices, all my past and present colleagues at the Optoelectronics Laboratory, especially Dr. Markku Sopanen and Professor Harri Lipsanen.

The warmest thanks to my father Thure and mother Auli for them supporting and encouraging me with my studies from the comprehensive school through to the University.

I also want to thank my friends for their advices and help, also Markku Tilli from Okmetic for arranging the etch pit images, Kari Kivisalo for tifftopnm UNIX issues, and Anne Korkalainen for acquiring a collection of papers on gettering.

To the persons, who are, or are not mentioned here - I want to thank you for all your help!

Espoo, 16 December, 2002 Mika Karilahti

Contact information:
Email: mika.karilahti@hut.fi , mika@karilahti.com
URL: http://www.karilahti.com
Tel: +358-40-5487656

List of Publications

This thesis consists of an overview and the following publications:

I. P.J. McNally, P.A.F. Herbert, T. Tuomi, **M. Karilahti**, J.A. Higgins, *Analysis of the impact of dislocation distribution on the breakdown voltage of GaAs-based power varactor diodes,* **Journal of Applied Physics, 79, 8294-8297 (1996)**

II. P.J. McNally, T. Tuomi, P.A.F. Herbert, A. Baric, P. Äyräs, **M. Karilahti**, H. Lipsanen, and M. Tromby, *Synchrotron X-Ray Topographic Analysis of the Impact of Processing Steps on the Fabrication of AlGaAs/InGaAs p-HEMT's,* **IEEE Transactions on Electron Devices, Vol. 43, 1085-1091 (1996)**

III. **M. Karilahti**, T. Tuomi, M. Taskinen, J. Tulkki, H. Lipsanen, P.J. McNally, *Synchrotron X-ray topographic study of strain in silicon wafers with integrated circuits,* **Il Nuovo Cimento, 19 D, 181-184 (1997)**

IV. D. Lowney, P.J. McNally, M. O´Hare, P.A.F. Herbert, T. Perova, T. Tuomi, R. Rantamäki, **M. Karilahti** and A.N. Danilewsky, *Examination of the structural and optical failure of ultra bright LEDs under varying degrees of electrical stress using synchrotron x-ray topography and optical emission spectroscopy,* **J.Mater.Sci.:Materials in Electronics 12, 249-253 (2001)**

V. **M. Karilahti**, T. Tuomi, and P.J. McNally, *Integrated circuit process control monitoring (PCM) data and wafer yield analyzed by using synchrotron X-ray topographic measurements,* **Semiconductor Science and Technology 18, 45-55 (2003).**

VI. **M. Karilahti**, *Neural Net Analysis of Integrated Circuit Yield Dependence on CMOS Process Control Parameters*, **Microelectronics Reliability 43, 117-121 (2003).**

Author's Contribution

The author has participated in the measurements and the reviewing of the conclusions for publications I, II, IV.

The author has had a major role in the preparation of manuscript for the publication III.

The author has performed the critical measurements, analyzed the results, and derived the conclusions for the publication V.

The author has been solely responsible for the publication VI.

Contents

List of Abbreviations & Vocabulary

AFM – Atomic Force Microscope

ATE – Automated Test Equipment

CL – Cathodoluminescence

CMP – Chemical Mechanical Polishing

CMOS – Complementary MOS (combining PMOS and NMOS transistor structures)

CVD – Chemical Vapor Deposition

CZ – Czochralski (production method to grow ingots)

Device – semiconductor component (diced / not diced / packaged / not packaged)

DIP – Dual in-line package (IC package), sometimes DIL

DUT – Device Under Test

EBIC – Electron Beam Induced Current

EDX – Energy Dispersive X-ray analysis

ELO – Epitaxial Lateral Overgrowth

Fab – Semiconductor Fabrication Facility

FEM – Finite Element Method

HEMT – High Electron Mobility Transistor

IC – Integrated Circuit

LEC – Liquid Encapsulated Czochralski (older GaAs ingot manufacturing method)

LPCVD – Low Pressure CVD

LTPD – Lot Tolerance Percent Defective

MOS – Metal Oxide Semiconductor (semiconductor transistor structure)

MOVPE – Metal-Organic Vapor Phase Epitaxy

OES – Optical Emission Spectroscopy

PCM – Process control monitoring (semiconductor process parameters)

PL – Photoluminescence

PSG – Phosphosilicate glass

RTP – Rapid Thermal Processing (single-wafer at a time thermal processing)

SB – side braced (ceramic IC package)

SO – Small outline package (IC package)

SOM – Self-organizing map neural net

SPM – Scanning Probe Microscopy

STEM – Spectroscopic TEM

STM – Scanning Tunneling Microsope

SXRT – synchrotron X-ray topography

TEM – Transmission Electron Microscopy

VGF – Vertical Gradient Freeze (GaAs ingot manufacturing method)

1 Introduction

The studies examine how manufacturing process-induced strain and device operational strain, precipitates, and defects in semiconductor components and in integrated circuits, relate to device functionality, processing, and yield. Let us first have a look at the analysis methods that we were able to apply in the study of the semiconductor components and integrated circuits. We used synchrotron X-ray topography (SXRT) to measure strain in the compound semiconductor components. Then, SXRT and etch pit micrographs of integrated circuits were correlated against the process control monitoring (PCM) data and the yield information, in order to determine their relationships. Finally, self-organizing neural net was used to find dependencies between yield and semiconductor manufacturing process variables.

Synchrotron X-ray topography [1] is a high-resolution imaging technique based on X-ray diffraction. It has successfully been used in the section geometry mode for the observation of oxygen-induced precipitates and stacking faults inside silicon wafers [2], and for investigating wafer process simulations [3]. The advantages of the method are that it is fast and non-destructive. The inherent property of the X-ray topography is its extreme sensitivity to lattice strain, strain gradient and tilt, when using the continuous spectrum (white beam) of synchrotron radiation for imaging.

Etch pit images are used for identifying oxygen-induced precipitates and stacking faults extremely well, and the method is applied here in parallel with synchrotron X-ray topographic analysis to complement the analysis. The method of using etch pits has especially been favored by the researchers in Japan.

Process control monitoring (PCM) data is routinely collected from silicon wafers in semiconductor fabrication facility (Fab), by making the wafers undergo electrical and optical measurements to determine after the process steps to see how well the process parameters were within the allowed limits. This information is used in the Fab to decide if some wafer process layers need to be re-worked and if the devices should be tested by a special characterisation at the back end of the line to make certain that their electrical operating values meet the a priori specifications, e.g. temperature range, durability, speed, etc.

The wafer device yield plays a very important role in cost-effectiveness for Integrated Circuit (IC) manufacturers. Various models [4] have been constructed for estimating the device yield of a wafer - usually based on the die size, process linewidth, and particle accumulation. The yield is determined by the outcome of the wafer probing by using testers, and is carried out before wafer dicing. The functional testing of mixed-signal devices is very thorough, and much information can be acquired about circuit failure blocks and mechanisms based on these test results. The simplest form of information is aggregate pass / fail statistics of the device, where the yield is usually expressed as the percentage, i.e. good dice per all dice on a wafer, to make process and product comparisons easier. We have used here the absolute number of good dice, because that information was directly available from the databases.

A self-organizing map neural net was finally applied to the PCM and yield data collected from another wafer set, a heartbeat rate monitor IC. The aim was to find out

possible reasons for low yield by identifying process parameters related to the low yield.

As a summary, this study successfully utilizes all the previously mentioned measurement techniques, and links together material properties to electrical performance.

2 Imaging of Defects and Strain

2.1 Semiconductor Defects

Defects, Impurities and Contaminants

Semiconductor manufacturing and processing into electronic and optoelectronic components is a huge business. Semiconductor Industry Association (www.sia-online.org) publishes sales numbers of the consortium, where the annual sales today exceed 100 billion USD, and are growing. Various bulk semiconductor materials are the basis for all components. The quality and processing of that material is extremely important to improve the component yield, i.e. lowering the manufacturing costs.

Semiconductor material is manufactured with various methods. All of the methods are based on solidifying liquid or gas, e.g. silicon ingots are grown by the former method, and silicon carbide by the latter one. Crystal defects always get incorporated into the material in the growth process. These defects have an effect on the electrical properties and further processing of the material. This has a later effect on the component performance and yield.

As a peculiarity, on some instances defects will all the time be appearing and disappearing in material, depending on the material itself and the temperature, e.g. Cadmium develops increasing dislocation density in air at room temperature ([5] p.122), and Indium on the other hand achieves diminishing dislocation density in air at room temperature ([5] p.121). Some specific materials may retain their average dislocation density, but dislocation configuration could be changing constantly ([5] p.120). In this study the main interest is for semiconductor materials, whose dislocations forming temperature is several hundreds of degrees centigrade higher than room temperature, which is generally rated as 300K in the industry.

Within semiconductor materials the main defect types are structural inhomogeneities, such as microtwins (crystal consisting of two parts as mirror images, ASTM F1241), stacking faults, climb and screw dislocations, helical dislocations, dislocation loops and oxygen precipitates, swirl defects, defects caused by temperature and material gradients (e.g. in silicon), micropipes (e.g. in SiC), cellular structures (e.g. in LEC grown GaAs), and grain boundary dislocations. Also, when the material is not pure or is a compound, then chemical inhomogeneities can be formed. Crystal growth can cause particles originating from the growth crucible and voids to be trapped into the crystal.

A standard fabrication process of silicon integrated circuits includes more than two hundred process steps or stages, and usually takes 6-8 weeks to complete. For the actual processing, the thermal budget increases up to the gate oxidation stage, and then starts to decrease. Generally speaking, the whole thermal history of a wafer affects its defect and precipitate concentration [6], [7], [8].

Oxygen, is the most common impurity (with Carbon and Nitrogen) in commercial Czochralski grown silicon, and forms many electrically active defects, which can seriously degrade device performance. With high-temperature treatment of a wafer, oxygen forms clusters and interstitial dislocation loops, thus disrupting the lattice, and

causing defect states in the silicon. At lower annealing temperatures it can form thermal donors. These defects lower electrical mobility and cause unstable operation in the transistors. The main defects in silicon are based on precipitation and secondary defects, such as stacking faults and dislocations [9], [10].

The most serious contaminants in silicon are transitional interstitial metal atoms, especially Fe, Ni, Cu (and less Cr, Ag, Zn, Au). Their devastating effect for the yield is due to their high diffusivity and solubility at elevated temperatures, combined with electrical activity of the metals and their complexes [11]. Iron especially is known to degrade gate oxide integrity at the Si/SiO_2 interface as precipitate to change the electric field strength, and by acting as a trap in the oxide layer, thus assisting in charge tunneling through the oxide. In general, the metal contaminants have an effect on the electrical properties of the semiconductor material by forming deep level traps, i.e. electron / hole recombination centers, and also affect thermal properties by binding to precipitates. The recombination centers cause instability in transistors, and are extremely harmful in high-voltage and photovoltaic devices. The contaminants are originating from the raw material manufacturing process and the crucible, where the ingots have been grown from.

Silicon also contains As, Sb, and Sn, which do not introduce deep level traps in silicon, and so have little effect on carrier lifetime.

With integrated circuits, there is also a factor of alkali ions (Na+, K+), which are accumulated into the wafer surface (not inner) layers from the residues of various process chemicals. These ions are quite mobile, and seriously affect the electrical performance of the devices, e.g. biasing the threshold voltages of the transistors. The ions bind to mechanical defects (to precipitates and in the Si/SiO_2 interface to the trap states) and chemical bonds.

Reducing the Effects of Defects, Impurities and Contaminants

Gettering is about reducing defects, impurities and contaminants in the active device region by localizing and isolating them into a separate non-active region of the wafer. There are several possibilities to accomplish this, extrinsic and intrinsic gettering [11]:

a) Wafer backside damaging with e.g. back grinding, sandblasting, or laser melting, in order to create dislocations to bind contaminants, and subsequent heat treatment for enabling their diffusion into the region.

b) Increasing wafer backside strain by depositing amorphous or polycrystalline polysilicon films, on the backside.

c) Placing a layer of liquid aluminum to the wafer backside.

d) Gettering by phosphorus diffusion to create a higher equilibrium solubility to attract the contaminants.

e) Internal gettering by temperature treatment to make oxygen to precipitate, and thus bind the contaminants.

f) Implantation induced backside damage.

g) Gettering by Fermi-level effect and iron pairing in heavily doped substrates of epitaxial wafers.

The silicon wafers studied here, were processed through the “three-phase thermal cycle”, which was originally developed in the industry to produce a defect-free denuded zone in the wafer surface region [12], [13]. The first phase is out-diffusion of oxygen to reduce the total oxygen content of the wafer. The second phase is nucleation, wherein oxygen-based precipitates are enlarged in the interior part of the wafer; i.e. internal gettering [14]. Finally, the third phase is annealing, and is required to repair the structural damage caused by the heat treatment, as the objective has been to form a denuded zone right beneath the wafer surface [15], [16]. This zone is almost defect-free, and has a perfect crystal structure, but was not visible in the examined wafers.

The main idea is to reduce the concentration of impurities (oxygen, carbon and nitrogen) and to possibly use them (oxygen) to bind contaminants while taking care not to create any precipitates in the active electronic area.

Alkali ions in the top layers are handled with placing a polysilicon glass (PSG) layer as one of the topmost layers on the wafer. It is composed of P_2O_5/SiO_2 (usually 5% of phosphor) and deposited with CVD or LPCVD. PSG forms a stable complex that is able to bind Na^+ and K^+ ions, which are very mobile in room temperature, and are easily diffused into the PSG layer. The phosphorus concentration has to be kept low to prevent moisture absorption causing corrosion in aluminum lines.

2.2 Preferential Etching and Etch Pit Microscopy

Structural defects such as dislocations, stacking faults, precipitates, point defects, and microtwins have an effect on the mechanical, electrical and optical properties of single crystal and polycrystalline materials. By using preferential (or selective) etching, it is possible to make these defects visible for optical microscopy.

Preferential etching is one of the simplest and most common techniques for evaluating defects in silicon wafers due to its easy sample preparation and low cost. Other benefits are that it is sensitive and can be applied to large areas and does not need any expensive equipment. The drawback is that the results require interpretation and are not systematic for different materials and temperatures. Also, the detection limit is not specific.

The procedure for preferential etching is relatively simple. First, chemical mechanical polishing (CMP) is applied to remove any specific layer, and to flatten the surface. Next, etching is performed with a solution that dissolves the material faster at the defects than the perfect regions, and makes the defects visible as etch pits. Various solutions are used for various purposes. One of the first defect etchants developed, was the so-called Dash etch [17]. It was not optimal in terms of selectivity and sensitivity and in producing etch features that allowed distinguishing between certain types of defects, and required 4-16 hours for etching. The next approach was the "Sirtl etch" [18], and it works well only on {111} surfaces. Another very similar is the Seiter etch [19], which etches defects very well but only on {100} surfaces. A very common etch used by many researchers is the Wright etch [20], because it shows both line and point defects as pits. Finally, the Secco etch [21] etches defect on all surfaces. The "Schimmel" etch is an improved version Secco etch. Yang solution [22] is used to develop elongated rectangular, ellipsoid or circular etch pits in the {100} surface structure, or the pits of triangular pyramids on {111} surface.

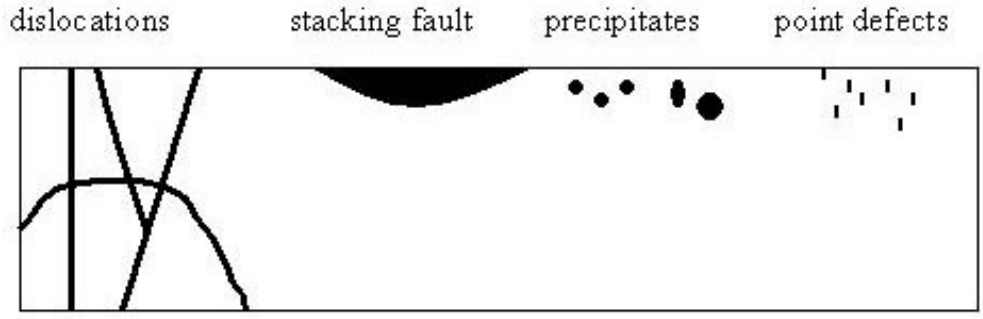


Figure 1(a). Wafer surface before etching.

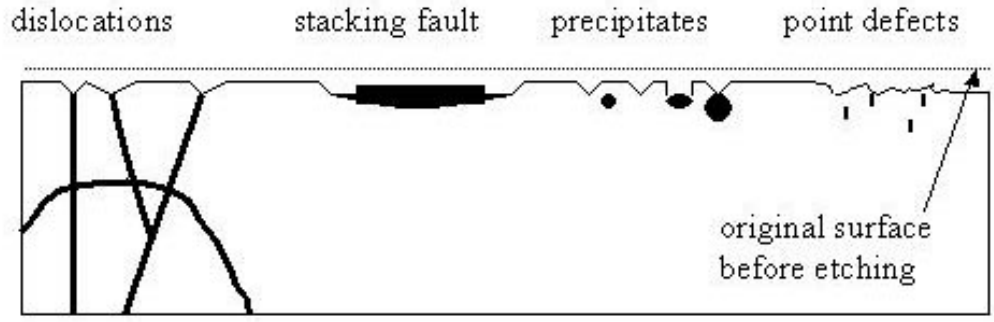


Figure 1(b). Wafer surface after applying an etchant.

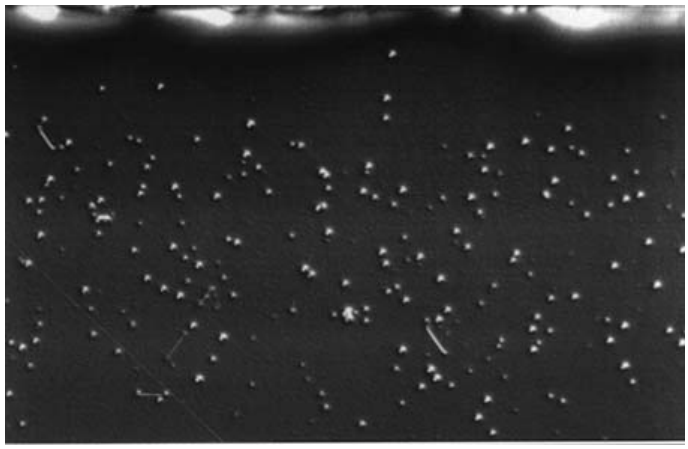


Figure 1(c). Etch pit micograph, i.e. the top view of Fig.1(b).

The procedure begins with the original sample in Fig. 1(a). After applying CMP and etching, we obtain the surface in Fig. 1(b), whose top layer is shown as the final etch pit micrograph in Fig. 1(c), where the one streak stretching from mid-left to 1/3rd lower left of the image is a polishing sreak, and the dots represent dislocations and precipitates, and the streaks connecting some of the dots are indicating a stacking fault.

The count of the microscopically visible pits provides information about the defect density present in the crystal, especially visible are stacking faults and microtwins as

streaks, dislocations as dots, and precipitates as small dots and pattern. Also, the CMP-caused streaks are visible, and they can be distinguished from the much shorter streaked stacking faults and microtwins, which also are dependent on the viewing direction. CMP-streaks usually extend over the whole image.

The drawback of the method is that it is difficult to distinguish between cracks and dislocations. Also, information can be obtained only of a specific layer. If the damage information of different layers is needed, step etching can be used.

In this study the etch pit images are made by sectioning the wafers, applying mechanical-chemical polishing to flatten the cross-section surface, and finally using a hydrofluoric based etch solution, actually the Wright etch, to reveal the defects. This method can be used to identify oxygen-induced precipitates and stacking faults extremely well [23].

In some instances, especially with SiC, it is necessary to apply anodic dissolution under bias voltage or electrochemical etching [24] to reveal electrically active defects (defects that generate carriers). Also, ultrasonic grinding methods have been experimented [25].

2.3 Synchrotron X-ray Topography

Background [26], [27], [28]

X-rays are convenient for studying single crystals. The crystal lattice acts as a Bragg grating for the X-rays, which are intensified by constructive interference in the directions matching the Bragg criterion (1), where d is the spacing of the lattice planes, θ is the Bragg angle, and λ is the wavelength,

$$2\,d \sin\theta = \lambda \quad . \tag{1}$$

Conventional X-ray sources have been the X-ray tubes, which are commonly used in small laboratories and facilities. The main reason for using synchrotron X-ray radiation is the continuous radiation spectrum (white beam), allowing more flexibility for the alignment of the sample, because there always exist several wavelengths that match the Bragg criterion. Therefore, by using white beam synchrotron X-rays, several usable topographs are obtained on the same film (Laue pattern) with a single exposure, as shown in Fig. 2. With X-ray tubes, the spectrum would be composed of only brehmstralung and K_α (and L_α) wavelengths depending on the anode material Cr, Fe, Co, Ni, Cu, Mo, Ag, W, or Au ([5] p.314). In addition, the high X-ray intensity of the synchrotron allows much shorter exposure times than conventional X-ray laboratory sources do.

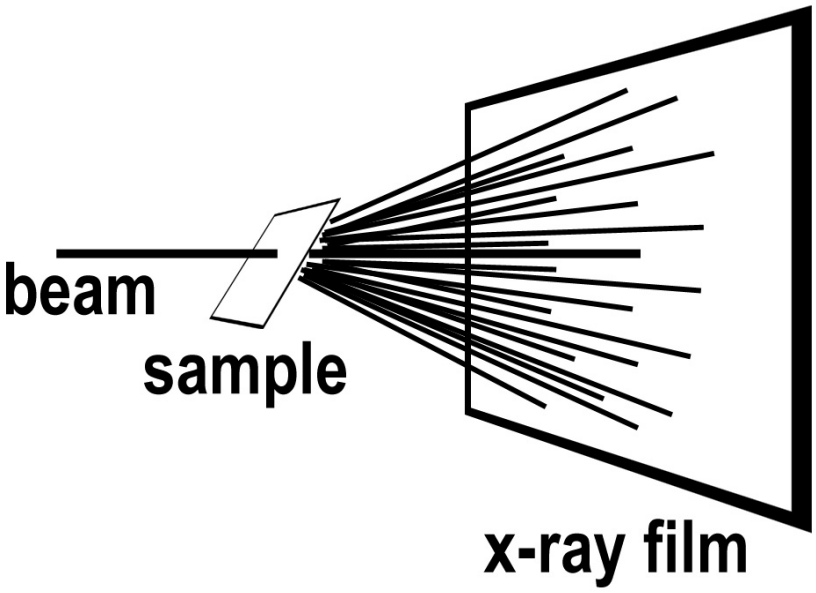


Figure 2. Several usable topographs are obtained by using white beam synchrotron X-rays.

It is customary to place the studied sample surface to the exiting X-ray beam in order to reduce noise in the topographs, and in a similar fashion, to place the film emulsion towards the incoming X-ray beam.

Summarizing, the advantage of using synchrotron X-rays is that the beam is white (has a wide spectrum of wavelengths) and collimated. The white beam brings several advantages: sample orientation is not necessary, several reflections with one exposure, all crystal parts simultaneously visible, large diffracted intensity, and good geometrical resolution. On the other hand, the drawbacks are: sensitivity to heat load, higher harmonics images overlap, and limited sensitivity to weak distortions.

Image Contrast ([28] p.77-89)

There are three types of image contrasts with X-ray topography: orientational, kinematical, and dynamical.

The *orientational contrast* is observed because of the continuous spectrum of the incident synchrotron beam; the misorientated lattice planes in Fig. 3(b) diffract a beam having a wavelength available in the polychromatic (white) spectrum according to Bragg's law. Fig. 3(a) shows a case of monochromatic beam not having a suitable wavelength to diffract.

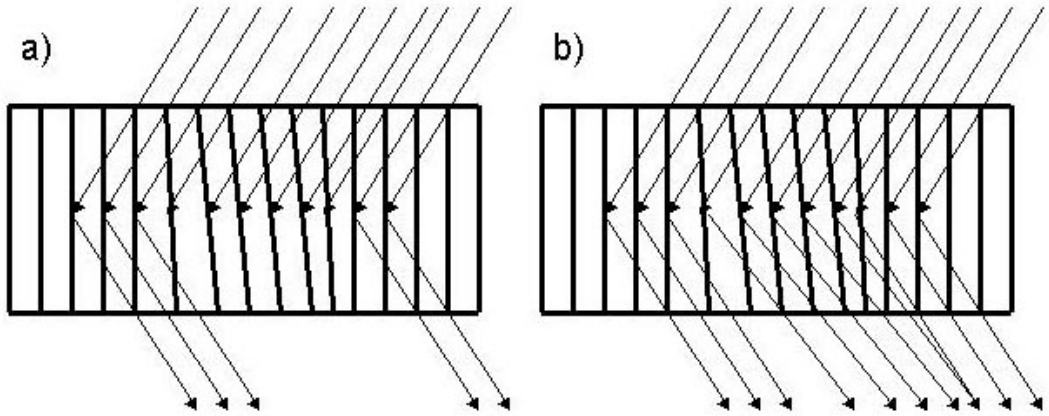


Figure 3. Orientational contrast with (a) monochromatic and (b) white beam diffracting from lattice with some of the planes tilted in the center part of the block.

The *kinematical contrast* (or extinction contrast, or direct image) is observed as an enhanced diffracted beam intensity when $\mu t < 2\ldots3$, where μ is the linear absorption coefficient, and t is the sample thickness [29], [30], governing the intensity in the absorption equation of the Beer-Lambert law

$$I = I_0 \, e^{-\mu t} \, . \qquad (2)$$

This type of contrast is observed as a series of dark dots in the interior part of the wafer. It also contributes to the dark part of the images near the surface. The corresponding μt values are 0.42, 0.15 and 0.06 for the 440, 660 and 880 reflection of the 220 section topograph of silicon, respectively. For the 220 reflection of silicon, $\mu t = 3.2$. The 220 section topographs show therefore kinematical (or direct) images of the cross section of the sample without any significant dynamical image contribution. An imperfect part of the crystal diffracts more strongly than the surrounding nearly perfect crystal. The intensity of the diffracted beam from the imperfect part is proportional to the square of the structure factor, whereas that of the nearly perfect part is proportional to the magnitude of the structure factor [31].

The *dynamical image* contrast is commonly observed in nearly perfect single crystals, if μt is larger than 6 or 8 [30]. These dynamical images appear as white images, i.e. they correspond to areas of decreased X-ray intensity, the defects, in effect causing shadows in the diffracted beam. The interference pattern, i.e. Pendellösung fringes observed in the section topographs of nearly perfect crystals are also explained by the dynamical theory of X-ray diffraction.

We regard the deformed region near the surface to be caused mainly due to strain between the oxide and the substrate with the silicon studies. In the bulk the defect images originate from oxygen-induced stacking faults and silicon-oxygen precipitates. The increased diffracted X-ray intensity is taken as a measure of lattice distortion. Sometimes only strong doping itself is able to cause lattice mismatch and strain [16]. The silicon-oxide interface produces strain [32], which can lead to the formation of defects, dislocations and stacking faults near the wafer surface. The darkening is due to an increased strain gradient, because the X-ray intensity is proportional to the strain gradient in the first approximation of the extinction contrast [33].

Imaging Geometries [34], [35], [36], [37]

Synchrotron X-rays are polychromatic (white), and this makes it possible to obtain several diffraction images onto the X-ray detection film with a single exposure.

There exist several imaging geometries, of which we have mainly applied the section transmission (Laue) and large-area back reflection (Bragg) geometries.

Large-area topographs (transmission geometry) are obtained by placing the sample into a wide (e.g. 3 mm by 3 mm beam), and exposing the film, as sketched in Fig. 2, except that the sample stays upright, and the topograph images are a representation of the whole sample thickness, accumulating intensity variations from the defects through the sample.

Fig. 4 shows the Laue pattern of the exposed and developed film of a GaAs wafer. The upper three round markings are from a film drying clip, and the exposure number, 96 is marked into the upper right corner in the dark room before exposing the film. The light rectangular in the center is due to a piece of lead (Pb) used for blocking the excess radiation.

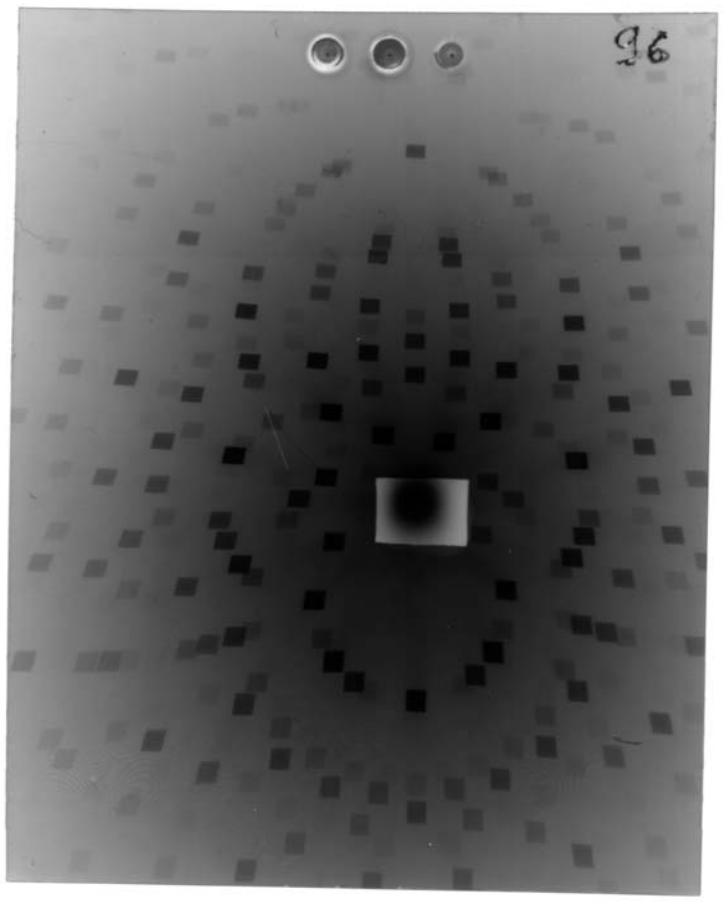


Figure 4. Laue pattern of the exposed and developed film of the large-area topograph setup (GaAs wafer). Film size is 10 cm by 10 cm.

Enlargement of a topographic projection details the defects of GaAs wafer grown with the Vertical Gradient Freeze (VGF) process. Fig. 5 clearly shows the dislocation loops in the material as dark threads.

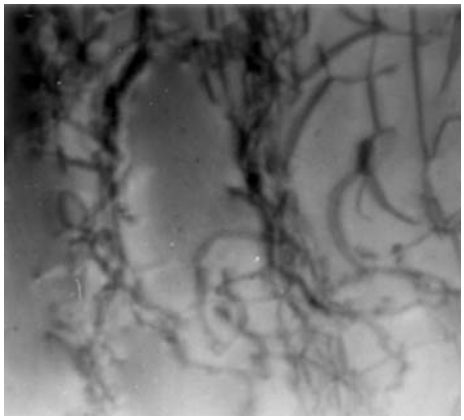


Figure 5. Large-area topograph (1 mm by 1 mm) of a VGF grown GaAs wafer.

It is possible to take a large-area topograph from an integrated circuit. One such exposure is shown in Fig. 6, which should not be confused with optical microscopy, and the dark areas in the synchrotron topograph indicate stronger strain or strain gradient, and the light ones less so.

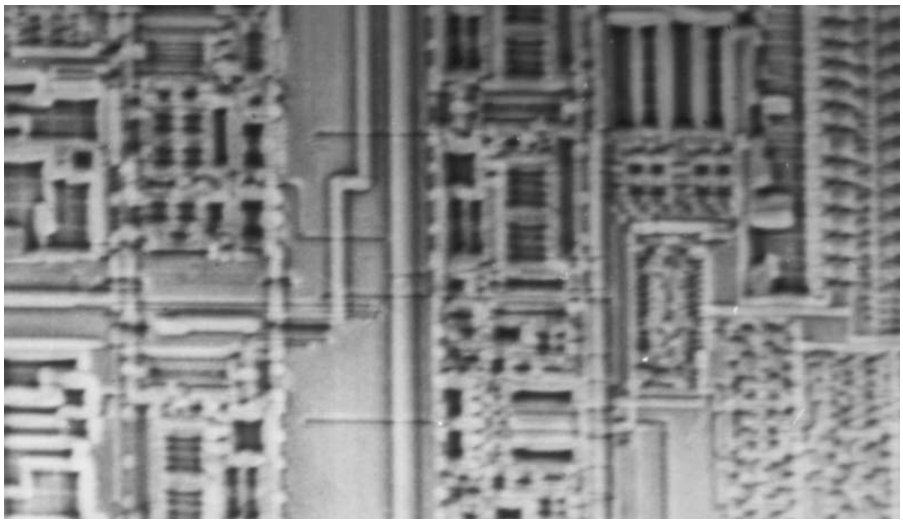


Figure 6. Large-area topograph shows a part of an IC from a silicon wafer. The image width is 0.3 mm.

Section geometry is used for obtaining topographs from the interior part of the sample without any slicing of the sample. Figure 7 shows a schematical setup for acquiring the images. A vertical slit of 15 μm is placed in front of the wafer, whose normal makes an a small angle (about 18°) to the incident beam and the wafer (001) surface, with the IC surface facing away from the beam to achieve less image noise. A typical width of the beam is 5 mm. The distance from the film to the sample should be convenient for obtaining all the relevant topographs in the Laue pattern onto the film. Typical distance between a silicon sample and a film is 35 mm. The synchrotron topograph is then a mapping of the projected wafer cross-section.

Pendellösung fringes [38] are caused by an X-ray interference pattern from an almost perfect crystal due to the dynamical image contrast. They are best seen in section topographs, but were not observed in the topographs of this study probably because of the distortion the silicon wafers exhibited due to thermal and mechanical processing they had experienced.

The section topography setup in Fig. 7 produces on the film the Laue pattern shown in Fig. 8, when examining (001) orientated silicon. A micrograph of a topograph is shown in figure 9. The strain field is visible as dark contrast underneath the IC structures on the top.

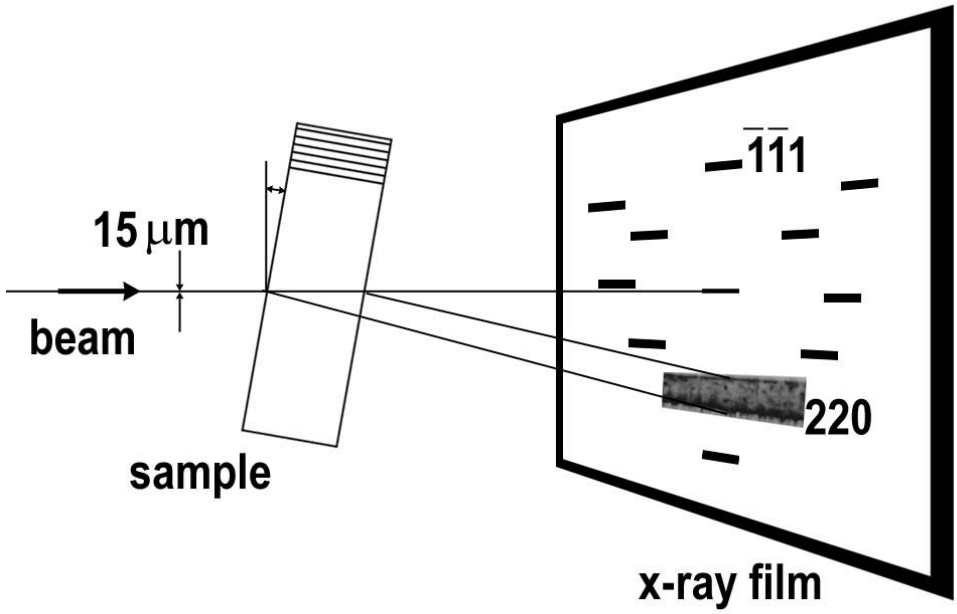


Figure 7. Experiment setup for obtaining synchrotron X-ray section topographs of a silicon wafer. The planes (110) are the diffracting ones, and some have been made visible in the sample.

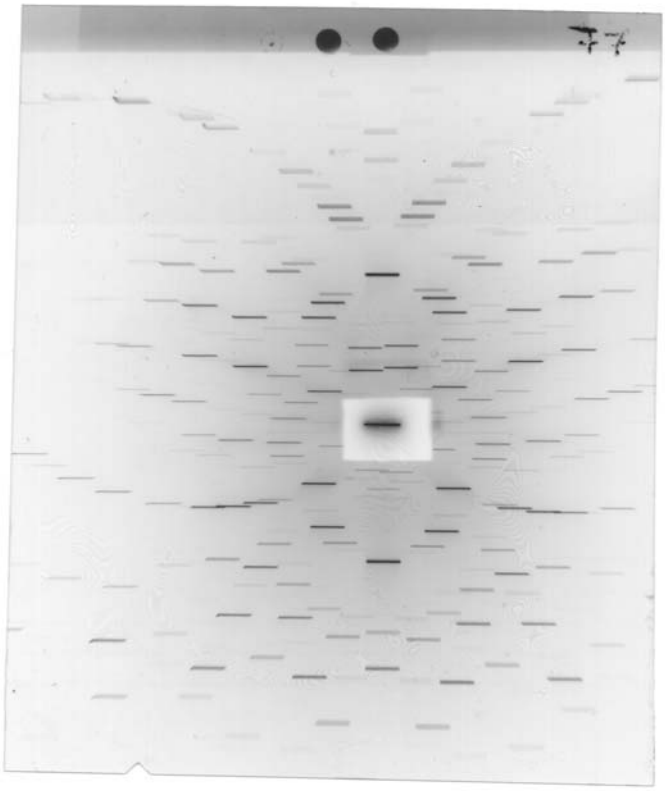


Figure 8. Laue pattern of the exposed and developed film of the section topograph setup (silicon wafer). Film size is 10 cm by 10 cm.

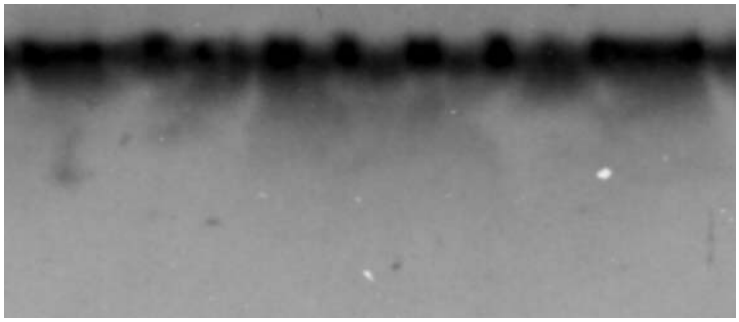


Figure 9. Section topograph shows a part of an integrated circuit from a silicon wafer surface. The image width is 2 mm.

Pinhole topography is a rare setup, where two limited (some micrometers) beams are used in parallel to expose the film.

Back reflection geometry is mainly used for orienting the crystal, and for some specific studies, schematically shown in Fig. 10. It has been very important for the micropipe studies of SiC. This setup only produces images of the surface layers, because of the limited penetration depth of the main wavelengths. The main setup has been the back

reflection large-area beam, but can be used in section mode, too. This way it is possible to create section images of the surface.

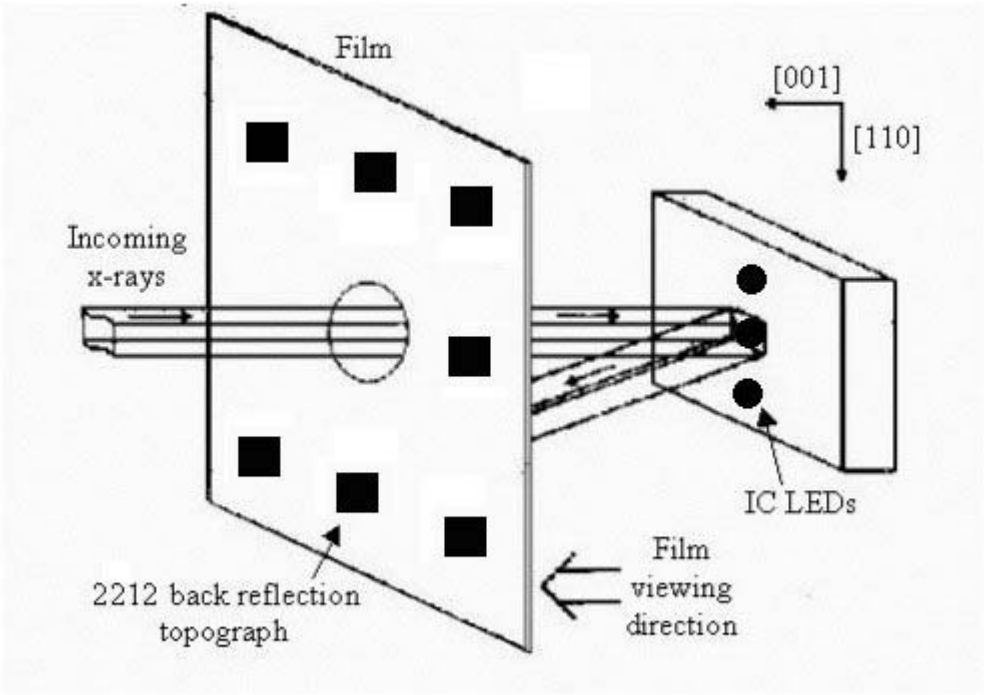


Figure 10. Setup of large-area back reflection topography.

Grazing incidence (Bragg-Laue) geometry is used with modifying the incidence angle to attain certain X-ray penetration depth, e.g. to do depth profiling of the samples. Here the large-area beam hits the sample first, and is then deflected with a very large angle, some degrees below 180° to the film.

Double crystal topography setup is used when strain sensitivity should be enhanced, and background from radiation in the image should be suppressed. It is possible to use two- or more-crystal arrangements in topography, and the setup is similar to diffractometry and spectroscopy, and the two basic groups are non-dispersive and dispersive settings. In the non-dispersive setting the front-crystal is identical to the sample crystal and the same reflection is used on both. For the dispersive crystal setting, the front-crystal may differ from the sample crystal, and different reflections may be used for each crystal. The advantage with the multi-crystal topography is improved imaging resolution.

2.4 Other Imaging Methods for Semiconductors

Transmission Electron Microscopy (TEM) [39], [40]

Electrons are accelerated to high energies and focused on a material by using magnetic lenses. The electrons can then scatter or backscatter elastically or inelastically, or produce X-rays, Auger and secondary electrons, light, and lattice vibrations. The samples are prepared for analysis by extracting thin (60 nm) slices from the specimen for TEM observations. The TEM can be extended to do spectroscopy (STEM). Hence, the signatures of the elements can be detected from the X-rays, whose energy corresponds to the K_α electron energy.

Scanning Electron Microscopy (SEM) [39]

In the primary electron imaging, electrons from the beam interact with the nuclei in the sample. The coulomb attraction deflects the paths of the electrons, the event being called Rutherford elastic scattering. The electrons back-scattering from the sample surface can be used to attain topological and compositional information of the sample. The most widely used SEM mode is based on the detection of secondary electrons. These are loosely bound conduction band electrons in the immediate sample surface, having a range of a few nm, and are able to escape from the sample, and can be detected. The enegy-dispersive X-ray (EDX) analysis is based on the same method as described in conjunction with TEM. The vacant K_α electron position in the sample becomes filled by an outer electron, and the energy is released as an Auger electron or X-ray, which photon energy can be detected to analyze the material decomposition. When the electron beam is probing a semiconductor sample, the primary electrons promote valence band electrons to the conduction band. The created electron-hole pair recombines, and emits a photon in the visible or near-visible range. These photons can be detected, and this method is called cathodoluminescence (CL) [41]. This method can be used to analyze the crystal structure, including impurities, lattice defects and distortion. Alternatively, the electron-hole pairs can be separated by a voltage potential, and detected as electron beam induced current (EBIC).

Photoluminescence (PL) [41], [42], [43]

Photons are used to excite electrons in a semiconductor valence band into the conduction band with some kinetic energy remaining, and also creating a hole. The electron-hole pairs recombine, and emit the energy as photons. The emitted photon energy is at or near the semiconductor bandgap energy. There are several possible energy transitions, e.g. band-to-band recombination, exciton recombination, conduction band to acceptor state transition, etc. Temperature affects the recombination process, and a cryostat is used for cooling down the temperature of the sample.

Raman Microscopy [43], [44]

Raman Microscopy is based on the principle of monochromatic (laser) light interacting with phonons (lattice vibrations) in the material under study. The back-scattered light is able to either gain energy by absorbing a phonon, or loose energy by creating a phonon. This causes a shift in the back-scattered light frequency, which can be detected. The use

of visible light makes it possible to examine the surface parts of the semiconductors [45], [46], because their transparency (bandgap energy) is in the infrared area, e.g. silicon and GaAs. The advantage of the visible light is that better than 1 μm resolution can be achieved with ordinary microscope based technology. The phonon population is very temperature-dependent, and will have to be compensated for in the measurements.

Scanning Probe Microscopy (SPM) [47], [48]

The first microscope in this category was the introduction of the Scanning Tunneling Microscope (STM) in 1982 by Binnig and Rohrer at the IBM Research Laboratory in Zürich, Switzerland. This technique is based on the principle of moving a fine metallic tip with piezoelectric actuators above an electrically conducting sample, maintaining a constant tunneling current between the tip and the sample. The X-Y-Z positioning of the tip creates the map of the surface. An improvement came in 1986 with the invention of the Atomic Force Microscope (AFM), which is able to map non-conducting materials, also. There, the tip is taken to a close proximity with the surface. The tip experiences an attractive force until it comes into a very close distance (0.3 nm) of the surface. Then, the force becomes repulsive, and grows very steeply with the decreasing distance. The force detection is delicate, so the sample is moved as with piezoelectric actuators. Another variation of the technique is the Thermal Scanning Microscope (TSM), which senses the thermal conductivity of the surface with a resistive tip that acts as a tiny resistance thermometer.

3 Experimental Results on Silicon Integrated Circuits

Publication III examines wafers, which have gone through a real IC manufacturing process. The synchrotron X-ray topographic study is supplemented with etch pit micrograph and computational strain analysis of the silicon and oxide interface. Fig. 11 shows a 220 section topograph of a fully processed silicon wafer. The strain below the surface is visible as dark image due to the orientational (extinction) contrast. The dark spots inside the wafer originate from the strain caused by oxygen-induced precipitates.

The etch pit micrograph of the same wafer is shown in Fig. 12, which shows precipitates as black dots. The surface part exhibits similar structures as the synchrotron X-ray topograph, but to a lesser extent. The IC's and the pad areas are visible in both Fig. 11 and Fig. 12. The etch pit concentration appears low, most possibly due to insufficient etching.

The effect of strain is numerically computed in Fig. 13. In the computer simulation, an oxide disc (actually half) is grown on top of silicon, and the resulting strain is computed assuming circular symmetry.

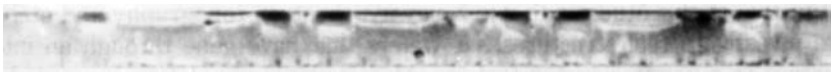


Figure 11. Synchrotron X-ray topograph of the wafer with integrated circuits. The wafer surface is on top and the image width is 7 mm.

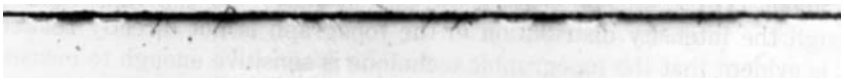


Figure 12. Etch pit micrograph of the wafer with integrated circuits. The wafer surface is on top and the image width is 15 mm.

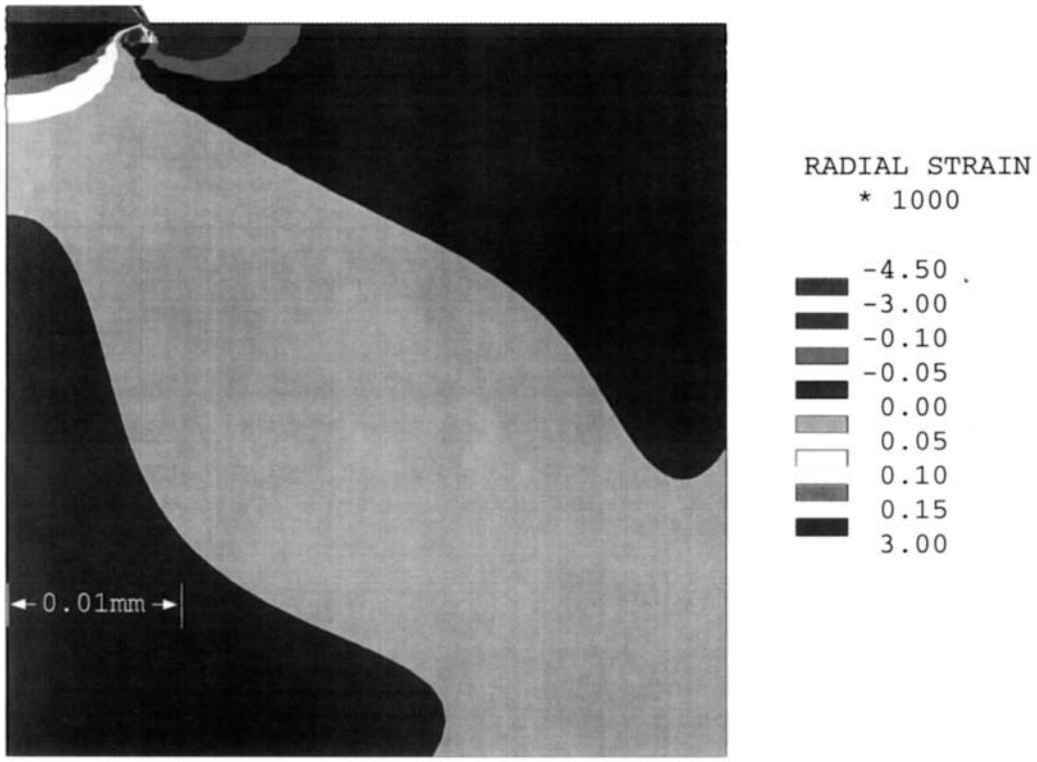


Figure 13. Computational strain of an oxide disc half located on silicon in the upper left corner, wafer surface is on top.

New results based on etch pit micrographs, this information not existing in any of the publications, will be presented in this chapter. Parameter extraction is very similar to the methods described in the publication V. Presenting comparative results requires repeating the contents from that publication.

One objective of the study was to correlate wafer cross-section defect image data against PCM parameters and device yield. In order to evaluate the defect count and concentration of the wafers, the synchrotron X-ray topographs and etch pit micrographs were first measured, and then digitally processed with digital image processing software, written entirely for the study. After retrieving characteristic image feature parameters, a correlation was then computed between those parameters and the electrically measured PCM parameters and the yield. The results are evaluated in-depth for the device, which is an analog audio codec processor used in mobile phones some time ago.

As the result, positive correlation between good device yield and strong near-surface strain gradient is found by synchrotron X-ray topography. Unexpectedly, computed from the etch pit micrographs, the yield correlates very poorly to the defect-free zone depth of the wafer surface. The results suggest that strain has more impact on the operation of the electronic device than precipitates solely would have.

3.1 Sample preparation

All the wafers for this study were chosen from several production lots processed with a Complementary Semiconductor Metal-Oxide (CMOS) process adapted for mixed-signal products. The common factor for all the chosen wafers is that the yield varies significantly across the lots.

The wafers in this study were first subjected to temperatures of 965°C for 18 min, then 850°C for 5 min, then 900°C for 41 min, then 1000°C for 14 min, then 784°C for 6 min, and finally 730°C for 35 min. Many of the steps are carried out separately, so the actual temperature approaches the room temperature on occasion. The simplified thermal cycle is shown in Fig. 14. A standard fabrication process includes more than two hunderd process steps, and usually takes 6-8 weeks to complete. For the actual processing, the thermal budget increases up to gate oxidation, and then starts to decrease. This means that p+ predeposition, skin oxidation, n+ pre-deposition, and gate oxidation each make their contribution the crystal defect generation.

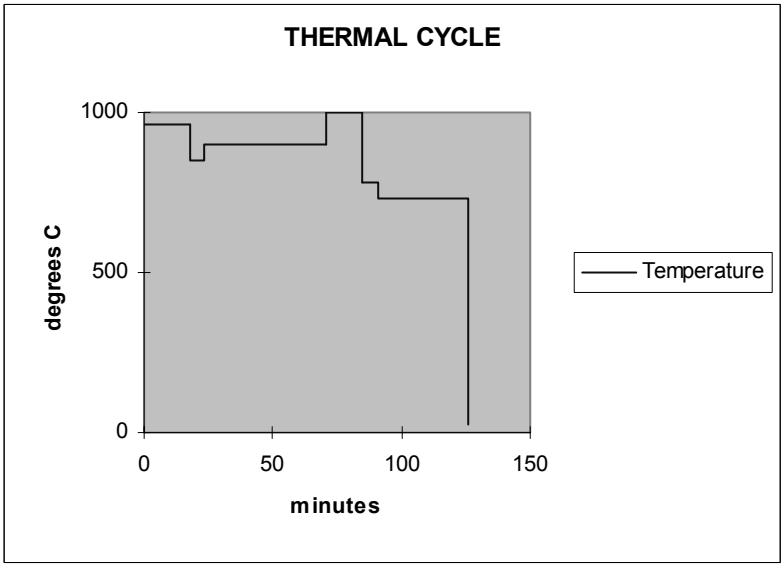


Figure 14. Simplified thermal cycle of the IC manufacturing process

Before processing commenced in the fab, the oxygen concentration of the wafers in this study was in the range of 13-16 ppm measured according to the new standard [49] of the American Society for Testing and Materials (ASTM).

The fab is using the "three-phase thermal cycle" (described previously), where the first phase is out-diffusion of oxygen to reduce the total oxygen content of the wafer. The second phase is nucleation, wherein oxygen-based precipitates are enlarged in the interior part of the wafer; this is called internal gettering [14]. Finally, the third phase is annealing, and is used to repair structural damage caused by the heat treatment, as the objective in process simulations is to form a denuded zone right beneath the wafer surface [15], [16]. The zone is almost defect-free, and has a perfect crystal structure.

During the processing, many parameters are measured optically and by other means to verify that layer thicknesses, etch depths, etc. are within the allowed limits. After completing the processing of a given lot, the electrical PCM parameters are measured.

The test structures have been designed so that the effect of various process variables can be electrically measured. After this the wafers are tested functionally, also called wafer probing, to determine device functionality, thus the yield. Finally, backside grinding is applied to the wafers.

The already probed wafers were then exposed to aluminum removal to prevent X-ray induced fluorescent radiation from the metal. Later it was determined that the large streaks and enhanced intensity observed in the X-ray synchrotron images were actually not due to fluorescence, rather due to strain and orientational (extinction) contrast of the kinematical diffraction theory [32], [50], which can cause images to be mapped even outside of the physical area of a wafer [51], [52]. The silicon and oxide interface produces strain, which can lead to the formation of defects, dislocations and stacking faults near the wafer surface.

The wafers were then sliced in half: The other of the halves was used for synchrotron imaging, and the other for etch pit imaging. All the wafers for this study were chosen from several production lots processed with a 2 μm linewidth Complementary Semiconductor Metal-Oxide (CMOS) process adapted for mixed signal products. The common factor for all the chosen wafers is that the yield of each lot varies significantly.

3.2 Experimental Techniques: Synchrotron X-ray Topographs and Etch Pit Micrographs

Synchrotron X-ray topographic images

The synchrotron X-ray experiments were performed at Hamburger Synchrotronstrahlungslabor am Deutschen Elektronen-Synchrotron (HASYLAB-DESY), Hamburg, with the DORIS III positron storage ring having a particle momentum of 4.43 GeV / c and typical beam currents of 70 mA [53]. Fig.15 shows the experimental setup for section topographic imaging. A vertical slit of 15 μm is placed in front of the wafer, whose normal makes an angle of approximately 18° to the incident beam and the wafer (001) surface, with the IC surface facing away from the beam to achieve less image noise. The distance from the film to the sample was 35 mm. The synchrotron image is now a mapping of the projected wafer cross-section, i.e. 0.525 mm / cos(18°), where the thickness of the unprocessed wafer is 0.525 mm. The horizontal beam width is 5 mm and the beam height 15 μm, hence the volume imaged is about 4.1x10-11 m3.

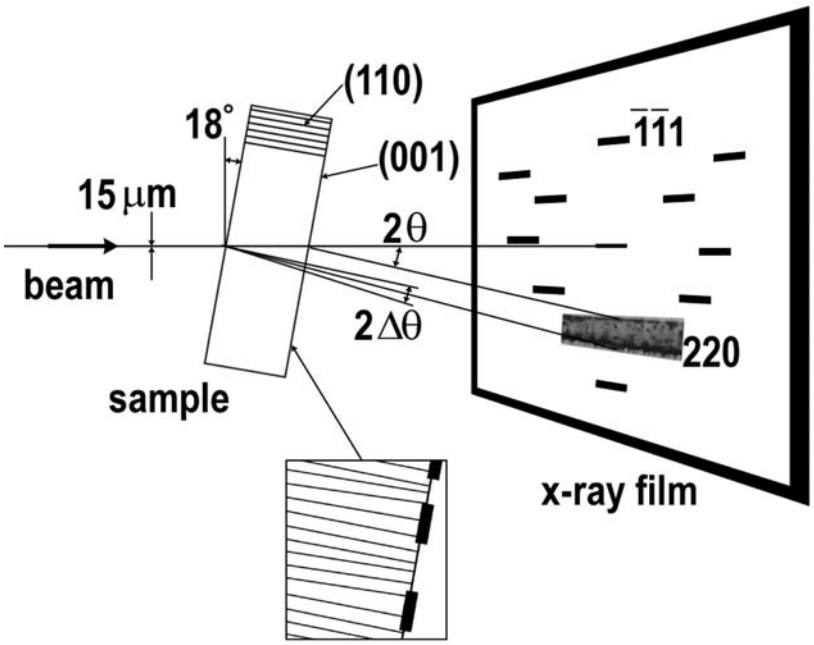


Figure 15. Experiment setup used for obtaining the synchrotron X-ray images. Enlargement of the wafer surface shows how the oxide deforms the (110) planes.

The Laue patterns of topographs were recorded on Kodak High Resolution SO-343 films. The 220 section topographs were enlarged from the film with a microscope. They were transferred into digital form with a CCD camera mounted on the microscope. The original CCD images are 855 x 652 pixels with 256 gray levels. The CCD images of the wafers occupy only about 30% of the X-ray topograph image area.

All the section topographs of this study are defined as 220 topographs, because it is the first structure factor permitted Bragg reflection from the (110) lattice planes of silicon. However, the dominant wavelengths contributing to this 220 topograph (wavelength λ=166 pm, E=7.5 keV) are the 440 reflection (λ=83 pm, E=15 keV), the 660 reflection (λ=56 pm, E=22 keV), and the 880 reflection (λ=30 pm, E=42 keV). Contributions from reflections higher than 880 are negligible because of the small intensity of the incident radiation from the bending magnet source and of the decreased sensitivity of the recording medium, the X-ray film, at the corresponding large photon energies.

The main reason for using synchrotron X-ray radiation is the continuous radiation spectrum, which mitigates the requirement for exact alignment of the sample. In addition, the high X-ray intensity allows much shorter exposure times than for conventional X-rays laboratory sources. When using synchrotron X-ray, several usable topographs are obtained on the same film with a single exposure as shown schematically in Fig. 15. In this work only the most representative reflections, i.e. 220, were selected for further study.

Although the average lattice parameter in the (001) plane is the same throughout the whole wafer, there is local strain variation in the silicon and oxide interface as shown in the lower part of Fig. 15. Consequently, this strain causes diffraction intensity variation due to lattice distortion. All strained locations appear darker than their surroundings; this contrast is explained by the kinematical diffraction theory.

Image contrast considerations

When applying synchrotron radiation to section topography, three types of image contrast are commonly observed: orientational, kinematical and dynamical. The image contrast issue was detailed out in the previous chapters.

The dark contrast in the X-ray synchrotron images is caused by strain and strain gradient, and reveals the existence of precipitates, stacking faults, and other strain-related defects. The dark streaks in the images extending out from the wafer area were first assumed to be caused by diffraction from the aluminum wires and contacts, however, later it was determined to be caused by strain.

As far as all the synchrotron X-ray topographs are concerned, we assume that the deformed region near the surface is mainly due to strain between the oxide and the substrate. In the bulk the defect images originate from oxygen-induced stacking faults and silicon-oxygen precipitates. The increased diffracted X-ray intensity is taken as a measure of lattice distortion. Based on this relationship the feature extraction and analysis of the X-ray synchrotron images is justifiable when determining the yield and PCM parameter dependence of the strain gradient. In both cases (kinematical and orientational contrast) the diffracted intensity is proportional to the concentration of distorted regions. Sometimes only strong doping itself is able to cause lattice mismatch and strain [16]. The silicon-oxide interface produces strain [32], which can lead to the formation of defects, dislocations and stacking faults near the wafer surface. The synchrotron X-ray topographs on the left in Fig. 17 show the wafer without any Pendellösung fringes. The streaks imply a tilting of the lattice planes. The darkening is due to an increased strain gradient, because he X-ray intensity is proportional to the strain gradient in the first approximation of the extinction contrast [33]. Unfortunately, the film of 17(b) was poorly exposed, and could not be used in the analysis.

All wafers for this study were chosen from several production lots processed in a 2 μm line width Complementary Semiconductor Metal-Oxide (CMOS) process adapted for mixed-signal products. The common factor for all the chosen wafers is that the yield varies significantly across the lots. The wafers are measured electrically and optically throughout the wafer processing to verify at each stage that e.g. layer thicknesses, etch depths, etc. are within the allowed limits. After completing the processing of a given lot, the majority of the PCM parameters are measured. The electrical test structures have been designed so that the effect of various process variables can be electronically measured. After this the wafers are tested functionally, also called wafer probing, to determine yield. Finally, backside grinding is applied to the wafers to fit them into a low-profile package.

Etch pit images

In order to produce etch pit images, approximately 1 cm wide pieces were sliced from the remaining wafer halves. These were then stacked on top of each other, placing epoxy resin between the pieces. The pile was then placed sideways into a small plastic box, and filled with more epoxy. After the epoxy had solidified, the plastic box was removed from the epoxy block, now containing the stacked wafer slices. This block was then fastened under a stack of 2-3 blank wafers, all glued together with epoxy. The piece was placed into a wafer polish machine, and polished until the surface of the wafer stack was totally free of the epoxy. This first polishing stage took about 40 minutes. After that, the polishing sand paper was changed into a much finer one, and

polishing was continued for another 10 minutes. Then the piece was ready for chemical treatment. It was first rinsed in de-ionised water, then Wright etched [20] for 3 minutes, and then rinsed again in de-ionised water. If the etching were not sufficient, it would be repeated again with a shorter duration. The exposed visible etch pits were digitally photographed with a microscope CCD camera, and the pictures were printed out on a 600 dpi laser printer, the image size being 20 cm by 10 cm. The resulting images show stacking faults as lines on the right side pictures in Fig. 17.

The digitized size of these etch pit images after cropping is 450 x 250 pixels, with 256 gray levels. The 525 mm thick wafers do not fully fit into the images. This is not critical, as we are more interested in the upper half of the wafers, containing the electrical circuits.

The method of etch pit micrographs can be used to identify oxygen-induced precipitates and stacking faults extremely well [23].

Both the image types are placed next to each other for visual comparison in Fig. 17. Table 1 links together the topograph and micrograph locations on the wafer in Fig. 16 with the corresponding images in Fig. 17. Table 2 links together the actual lot and wafer numbers with the images in Fig. 17. Table 3 links together the images in Fig. 17 with the lot and wafer numbers and the measurement locations in Fig. 16.

Table 1. Corresponding wafer locations and images

Wafer location in fig.16	Images in fig. 17
A	Synchrotron (left) and etch (right): a, d, g, j, m, p
B	Synchrotron (left): b, e, h, k, n, q
C	Synchrotron (left) and etch (right): c, f, i, l, o, r
D	Etch (right): b, e, h, k, n, q

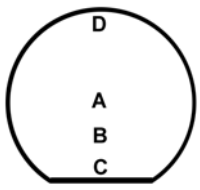


Figure 16. Locations of synchrotron X-ray topographs (A, B, C) and etch pit micrographs (D, A, C). The major wafer flat is nearest to the location C.

Table 2. Corresponding samples and images

Lot and wafer numbers	Images in fig. 17
19622, wafer # 20	Synchrotron (left) and etch (right): a, b, c
19631,wafer # 23	Synchrotron (left) and etch (right): d, e, f
20051, wafer # 37	Synchrotron (left) and etch (right): g, h, i
20116, wafer # 24	Synchrotron (left) and etch (right): j, k, l
20320, wafer # 9	Synchrotron (left) and etch (right): m, n, o
20321, wafer # 27	Synchrotron (left) and etch (right): p, q, r

Table 3. Corresponding image, lot number, wafer, and measurement location

Fig. 17	Lot#	Wafer#	Synchrotron image location in Fig. 16	Etch pit image location in Fig. 16
a	19622.1	20	A – Centre	A – Centre
b	19622.1	20	B – Middle	D – Arc
c	19622.1	20	C – Edge	C – Edge
d	19631.1	23	A – Centre	A – Centre
e	19631.1	23	B – Middle	D – Arc
f	19631.1	23	C – Edge	C – Edge
g	20051.1	37	A – Centre	A – Centre
h	20051.1	37	B – Middle	D – Arc
i	20051.1	37	C – Edge	C – Edge
j	20116.1	24	A – Centre	A – Centre
k	20116.1	24	B – Middle	D – Arc
l	20116.1	24	C – Edge	C – Edge
m	20320.1	9	A – Centre	A – Centre
n	20320.1	9	B – Middle	D – Arc
o	20320.1	9	C – Edge	C – Edge
p	20321.1	27	A – Centre	A – Centre
q	20321.1	27	B – Middle	D – Arc
r	20321.1	27	C – Edge	C – Edge

Fig. 17 shows the actual x-ray synchrotron images on the left and the etch pit micrographs on the right. Both are in the same scale, and the wafer height (thickness) in Fig. 17 (m),(n), and (o) is 525 μm. All the other wafers have been gone through the backgrinding stage, which is a standard procedure to make the wafer thinner by grinding its backside. Backgrinding is required for all the dice that are to be packaged in the small outline (SO) package to fit in. The standard wafer thickness is not a problem for the dice packaged in a dual in-line package (DIP) or side braced ceramic (SB) package.

It is important to notice that the synchrotron X-ray topographs and the etch pit micrographs of Fig. 17: b, e, h, k, n, q are not to be compared with each other, because the left side images are from the location B (table 3), when then right side images are from location D (table 3).

Visually comparing the synchrotron X-ray topographs on the left side, and the etch pit micrographs on the right side of the matching images in Fig. 17: a, c, d, f, g, i, j, l, m, o, p, r, clearly shows that the dark intensity (strain from precipitates) on the left side correlates with the white dot count (precipitates) on the right side.

The synchrotron image in Fig. 17(d), left side, shows a defect-free zone immediately below the integrated circuit structures of the wafer surface. The dark contrast on the surface is caused by the integrated circuits. However, that wafer is yielding only 23 dice when the best yield 73 dice is with the wafer in Fig. 17: m, n, o. Backgrinding is performed after the wafer yield probing, so it does not affect the yield. The integrated circuits are located on the surface of the wafer, and then, looking at the etch-pit micrographs of the same images, shows a distinct difference in the number of precipitates and stacking faults, visible as light-colored point defects and streaks respectively, streaks not to be mistaken for the polishing streak, e.g. seen in Fig. 17(l), right side, in the etch pit micrograph extending from the bottom to the top.

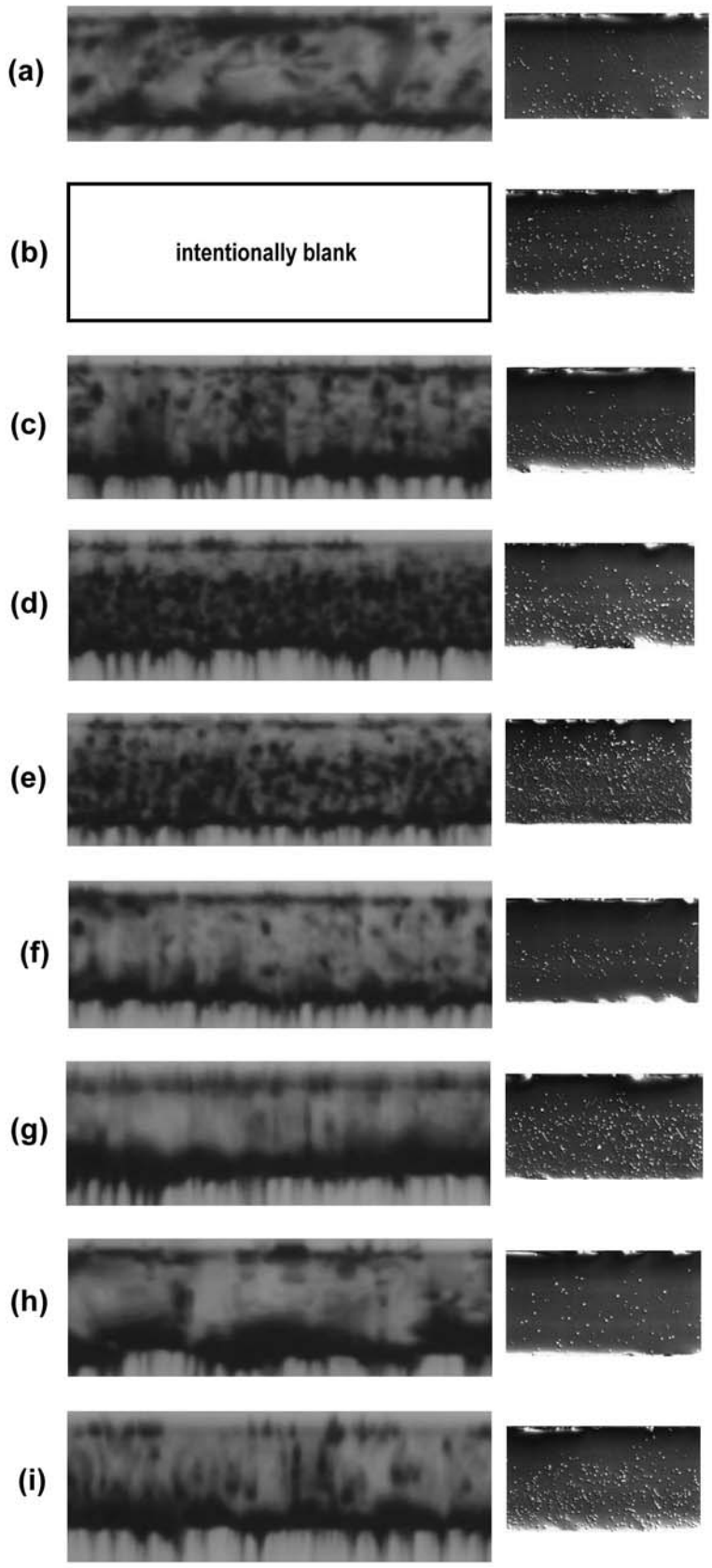


Figure 17 (a) - (i). Synchrotron topographs on the left, and corresponding etch pit micrographs on the right. The left and right side images are in scale. The width of the topographs is 2 mm. Poorly exposed X-ray topograph (b) is omitted.

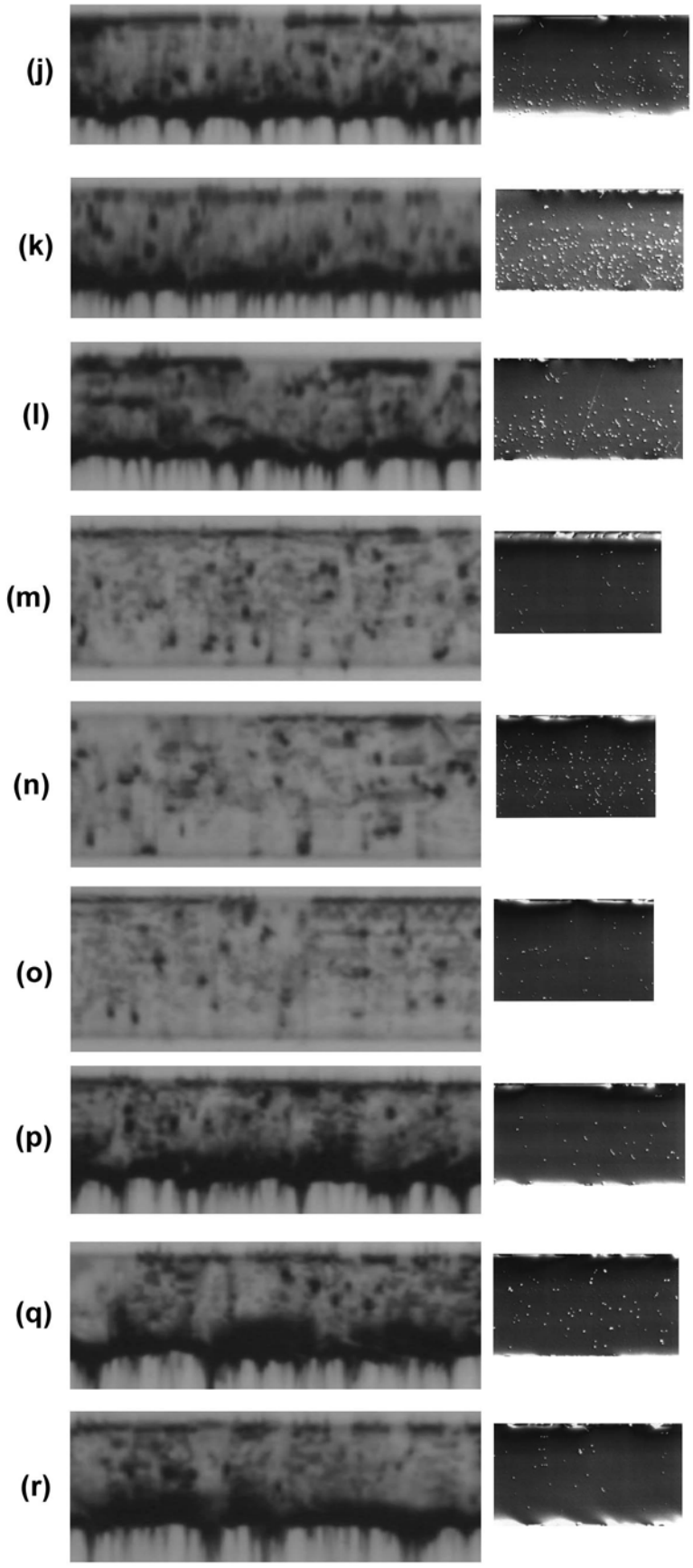


Figure 17 (j) - (r). Synchrotron topographs on the left, and corresponding etch pit micrographs on the right. The images are in scale. The width of the topographs is 2 mm.

3.3 Quality Control and Process Control Monitoring (PCM) data

Quality Control [54], [55]

Controlling the process quality is very important. Fabs try to keep up with constant quality by applying various methods to analyze their process. Some of the used quality control tools include, e.g. histograms, check sheets, pareto charts, cause and effect diagrams, defect concentration diagrams, scatter diagrams, control charts, and time series models. Additionally, statistical quality control tools, e.g. process capability (C_{pk}, P_{pk}, C_{pm}) indices, and time series can be used for triggering off automatic alarms.

Process control monitoring (PCM) data is required to be able to use these quality control tools. In the previous text the term PCM could also be interpreted as Product Control Monitoring as opposed to Process Control Monitoring, because the parameters are also used for monitoring the wafer component quality and reliability. Making decisions about if the product or process is acceptable, is by no means an easy task, e.g. if the process/product is in control and acceptable, or in control but unacceptable, or out of control but acceptable.

When uncertain, additional tests for the process and/or the product may be required for making the decision. When testing for acceptability, sufficient sampling must be determined, and a plan must be created. Very often in the semiconductor industry, LTPD (Lot Tolerance Percent Defective) level 5 is used. This means lots at or worse than the LTPD are accepted at most 5% of the time. In other words, defected lots are rejected at least 95% of the time.

Process Control Monitoring (PCM) data

Masks for wafers are generally designed so, that a wafer after being fully processed through the IC manufacturing process, will contain several test dice. The area consumed by a test die is usually quite large, i.e. sometimes comparable to several ordinary production dice. Measuring the electrical properties from the test dice gives an estimate of how good the lot processing has turned out to be, and if the devices need some special characterization to make sure they fulfill *a priori* specifications (e.g. temperature range, speed, lifetime), or if the wafers need to be re-worked (i.e. to remove some processed layers, and then re-process them back on).

Process control monitoring (PCM) parameters are routinely measured during and after the wafer processing. All wafers are equipped with test dice. These are specially constructed electrical structures to allow the measuring of electrical properties accumulated to the wafer during the integrated circuit processing. The impact of the process variations is measured from the test dice, which contain self-enhancing electrical structures (e.g. bridges).

A large number of electrical parameters are measured from the test dice. These measurements include MOS transistor threshold voltage, gate width, capacitor Q-value, contact chain resistance, thin-film resistor properties, and several others. Table 4 lists all the measured PCM parameters, and table 5 lists some of the parameters with their

typical values. Electrical values are measured from all the test dice on each wafer, and are called Process Control Monitoring (PCM) data. Finally the IC devices are tested for functionality at the block level in the wafer probing stage, and the yield of each wafer is appended to the data.

Table 4. Electrically and optically measured PCM parameters

Parameter shortname	Parameter description
NMOS Vt0	NMOS transistor threshold voltage
NMOS Beta	NMOS transistor current gain
NMOS IDS3	NMOS transistor drain to source current at 3V
NMOS breakdown voltage	NMOS transistor breakdown voltage
NMOS IDS	NMOS transistor drain to source current at 5V
PMOS IDS	PMOS transistor drain to source current at 5V
PMOS Vt0	PMOS transistor threshold voltage
PMOS Beta	PMOS transistor current gain
PMOS IDS3	PMOS transistor drain to source current at 3V
PMOS breakdown voltage	PMOS transistor breakdown voltage
N- bulk resistance	Wafer bulk resistance
P- sheet resistance	Sheet resistance of p-implanted well
PG sheet resistance	P-type guard area sheet resistance (resistivity / thickness)
NG sheet resistance	N-type guard area sheet resistance (resistivity / thickness)
PS sheet resistance	Polysilicon sheet resistance (resistivity / thickness)
Al/Metal Capacitance	Aluminum to metal area capacitance
Al/Metal C mDissipation	Aluminum to metal sheet capacitor dissipation x 1000 (= 1000 / Q)
Al/Metal C leak12V	Aluminum to metal capacitor leakage current at 12V
NS sheet resistance	N substrate sheet resistance
Metal/P- C leak20V	Metal to P- capacitor leakage current at 20V
Metal sheet resistance	Sheet resistance of metal
Metal 2u electrical linewidth	electrical linewidth of 2um metal
Metal 2u substrate leak	2um metal to substrate leakage current
Metal 2u optical linewidth	Optical linewidth of 2um metal
Al resistance	Aluminum resistance

Al sheet resistance	Aluminum sheet resistance
Al sheet leakage	Aluminum sheet leakage current
Metal contact(size1)	Resistance of aluminum to metal contact, size A
Metal contact(size2)	Resistance of aluminum to metal contact, size B
Metal contact(size2) chain	Resistance of aluminum to metal contact (size B) chain
P- sheet contact(size1) chain	Resistance of aluminum to P-doped well contact (size A) chain
P- sheet contact(size2) chain	Resistance of aluminum to P-doped well contact (size B) chain
N- sheet contact(size1) chain	Resistance of aluminum to N-doped well contact (size A) chain
N- sheet contact(size2) chain	Resistance of aluminum to N-doped well contact (size B) chain
Thin-film sheet resistance	Resistance of a sheet of thin-film layer
Thin-film leakage	Thin-film layer to aluminum leakage current
Thin-film resistance (width1)	Resistance of a sheet (width C) of thin-film layer
Thin-film resistance (width2)	Resistance of a sheet (width D) of thin-film layer
Thin-film R delta-length	Difference of vertical vs. horisontal resistance
Wafer yield	The number of good dice obtained from one wafer

Table 5. Typical measured values of the electrical PCM parameters

Parameter description	**Typical value**
NMOS transistor threshold voltage	0.659 V
Al-Metal1 Capacitor leakage at 12V	1.7 nA
Al to Metal contact chain resistance	0.217 ohm
Thin Film Resistance, nominal 20 k ohm	19200 ohm

3.4 Integrated Circuit Testing and Yield

Integrated circuit testing [56], [57], [58] is required for determining the functionality of the device under test (DUT), and based on the passed and failed functional tests also some process quality factors may be used.

The testing scheme should be based on fault modeling, because of the testing time minimization. The functional testing must be constructed from the viewpoint of the functional blocks in cooperation with the design department already from the design phase, because some blocks may require separate probing lines and design modifications to make some variables readable, e.g. on-chip amplifiers. Additionally, it is totally possible to have a separate test pin to activate the device into a special test mode, where some inputs and outputs are internally connected into various block inputs and outputs.

As an example, testing a memory block would require at least the following tests:

a) Making sure that no single bit is stuck to V_{SS} or V_{DD}. A sequential testing of 1's and 0's would cover this.

b) Making sure that not any address (or data) lines are cross-connected. Consecutive testing of alternating bit pattern matrices of 1's and 0's would cover this (first $55_{HEX}=01010101_{BIN}$ and then $AA_{HEX}=10101010_{BIN}$)

c) Making sure that the memory cells are not leaking to V_{SS} or V_{DD}. This would require a hold-time, where writing 1's into memory, it would be checked than none has changed into a 0, and then the other way around.

d) Making sure that no neighboring memory cells are leaking into each other. This would require an alternating bit pattern.

e) Making sure of the memory integrity. This could be tested with some preliminarily developed pseudo-random patterns.

In practice the test head of the probe stage, with tens to hundreds of needles is placed on the DUT pads the, and the automated test equipment (ATE) tests the device according to the test program. The tester creates suitable test patterns and connects signal generators and counters online. It digitizes the measurement signals, measures timings, and finally determines, according to the test limits, if the device performs acceptably or not. If not, the die is marked with ink to distinguish it as a non-working component.

Then, the wafer is diced, and the working dice are assembled into packages often in Far-East due to cost reasons. The components are then re-tested, usually in elevated temperature to make sure they are in spec.

As mentioned earlier with quality control, a suitable sampling plan can be created, so the testing of all devices is not necessary. Many fabs do not test all the dice of the wafer, rather test only few of them, to make certain that the product and process are in order. Some fabs skip some wafers in the lot, and some skip all the wafers in the lot for some products. The reason is that all wafer testing costs money. The testers are expensive, and testing takes time. Programming, operating and maintenance of the

equipment cost money. Also, the production cycle can be made considerably shorter by skipping most of the testing. All the IC manufacturers, however, do test devices after the packaging. Customers, i.e. electronics assembly companies, would not be willing to buy untested products, as this leads to increased rework and replacement work at their production line.

The device yield of wafers plays a very important role in cost-effectiveness for Integrated Circuit (IC) manufacturers. Various models have been constructed for estimating the device yield of a wafer - usually based on the die size, process linewidth, and particle accumulation. This study takes a new approach and examines how process-induced strain, precipitates, and stacking faults in the wafer correlate with the wafer device yield and Process Control Monitoring (PCM) data parameters.

Silicon wafers produced in a semiconductor fabrication facility routinely go through electrical and optical measurements to determine how well the electrical parameters fit within the allowed limits. The yield is determined by the outcome of the wafer probing (electrical testing), carried out before dicing. The simplest form of yield information is the aggregate pass/fail statistics of the device, where the yield is usually expressed as a percentage of good dice per all dice on the wafer.

In principle, yield loss can be caused by several factors, e.g. wafer defects and contamination, IC manufacturing process defects and contamination, process variations, packaging problems, and design errors or inconsiderate design implementations or methods. Constant testing in various stages is of utmost importance for minimizing costs and improving quality.

4 Analysis

The objective of this study is to correlate wafer cross-section defect image data against PCM parameters and device yield. In order to evaluate the defect count and concentration of the wafers, the synchrotron X-ray topographs and etch pit micrographs are first measured, and then digitally processed with digital image processing software. After retrieving characteristic image feature parameters, a correlation is then computed between those parameters and the electrically measured PCM parameters and the yield.

4.1 Visual

Precipitates have traditionally been manually counted from the synchrotron X-ray images and etch pit micrographs. The counting is done for a certain rectangular area in the image, and then extended to the 3rd dimension, as the visible image depth is known to be the slit width for the synchrotron x-ray images, and etch variation depth with etch pit micrographs.

As already mentioned previously, visually comparing the synchrotron X-ray topographs on the left side, and the etch pit micrographs on the right side of Fig. 17: a, c, d, f, g, i, j, l, m, o, p, r, shows that the dark intensity (strain from precipitates) on the left side correlates with the white dot count (precipitates) on the right side when observed visually. Counting the dots and evaluating the precipitate count; evaluating the image darkness and the strain; they are both tremendous undertakings. The problem needs to be transferred into a computational task, making it possible to retain constancy and independency in the analysis.

4.2 Image Features and Processing

Synchrotron X-ray Topographic Analysis

The synchrotron topographic images were collected from the X-ray film using a CCD camera mounted on a microscope. The images were then processed with a computer algorithm to extract image features. The algorithm first sorts the darkest pixel values to the left side and the lightest values will go to the right side of the images; the consecutive horizontal pixel rows are treated independently. Then the optical density (image darkness) is mapped into relative X-ray intensity using the equation [59], [60]

$$I = a + b\,10^{D}\,, \tag{3}$$

where D is the optical density, I is the original X-ray intensity, and a,b are constants. Finally a threshold function is imposed on the images, and the characteristic curve feature information is extracted as pixel coordinates and as the average area coverage between the pixel coordinates as follows.

Figure 18 shows the procedure in which the optical image density of the original image, Fig. 18(a) is sorted pixel by pixel, placing to the left side the darkest pixel values (stronger strain) and to the right the lightest ones (less strain). Then, the image is

converted from optical density (image darkness) into relative intensity using the equation (3), and the background intensity level is uniformly subtracted to remove any bias. Thereafter, the pixel values are scaled into the range of integer values 0...255 from dark to light respectively, producing fig. 18(b). Finally, a threshold function is carried out for the image with a cutoff of 50% of the full scale darkness, choosing only the darker values further for the analysis. A different threshold value could have been chosen, but this value is expected to best retain the maximum image dynamics, i.e. does not drop the essential features in the image and still filters out sufficiently of the excess noise.

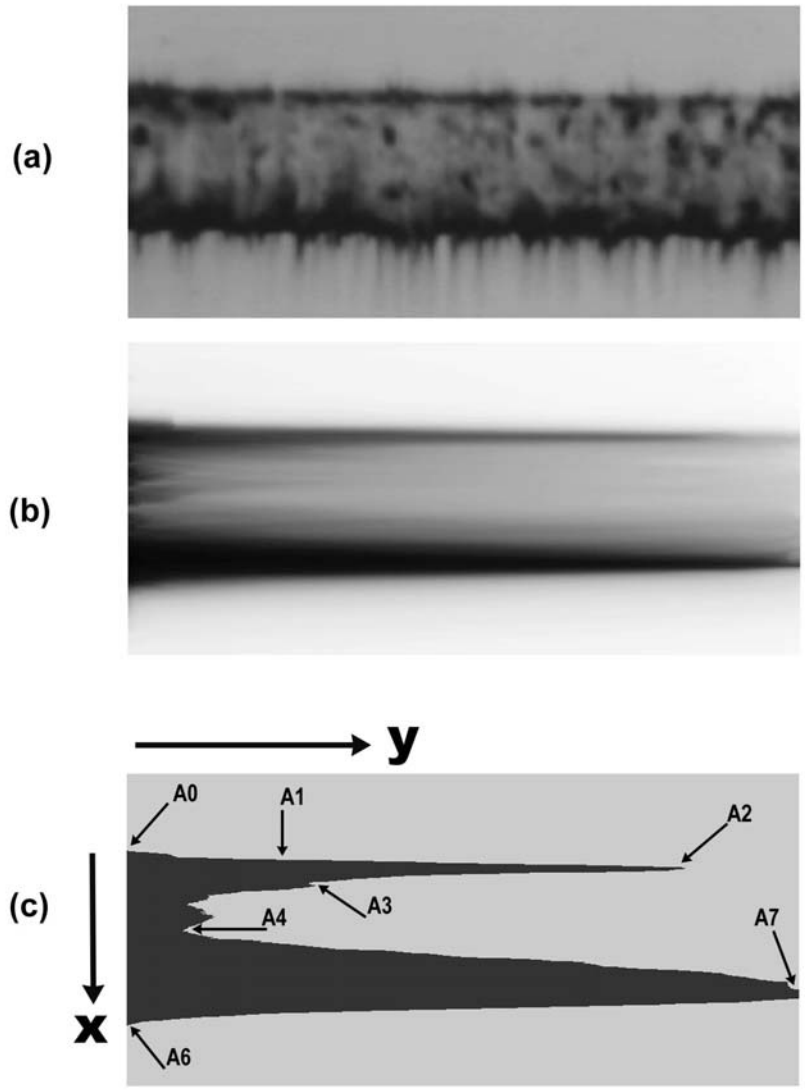


Figure 18. (a) 220 section topographs; (b) pixel-sorted image of Fig. (a) after converting from density to intensity and subtracting the backgound; (c) threshold applied to (b) to attain the image showing the extracted feature parameters to be used in correlation. The image size is about 850 x 650 pixels (width x height).

Finally, the result is available in Fig. 18(c), where the curve locations, A0, ..., A4, and A6, A7 are defined as the x-coordinate locations of the specific features existing in the curve coordinate (signal transition, accumulated contrast, etc.), i.e. x_{A0}, ... , x_{A4} and x_{A6}, x_{A7}. All the x-values are pixel indices from the digitised image. A0 (or x_{A0}) is the origin

of the parametric image data (or x-coordinate). A1 (or x_{A1}) is the x-coordinate value where the y-value of the curve has reached 20% of the first local y-maximum in y_{A2}. A2 (or x_{A2}) is the x-value of the first y-maximum of the curve, i.e. the highest density darkness y_{A2} near the wafer surface. A3 (or x_{A3}) is the x-coordinate value of the first local y-minimum yA3 of the curve immediately after the first local y-maximum, y_{A2}, of the curve. The x-coordinate value of the curve y-minimum y_{A4} in the wafer is A4 (or x_{A4}). The result of subtracting x_{A1} from x_{A4}, is A5 (or x_{A5}). The x-coordinate index value corresponding to the bottom of the wafer is A6 (or x_{A6}), which is only used for verifying manually that a good correlation is not coincidental. The x-axis value of the global y-maximum y_{A7}, is A7 (or x_{A7}) and is typically located near the bottom of the wafer, where the back grinding is the main cause of the darkness in the synchrotron X-ray topographic image derivatives. A8 denotes x_{A7} minus x_{A4}, A9 denotes x_{A6} minus x_{A7} and A10 denotes x_{A6} minus x_{A4}.

Then we have a y-coordinate series, where A11 (or $y_{A1...A2}$), represents the averaged y-coordinate from x_{A1} to x_{A2}. A12 (or $y_{A2...A3}$) is the average of y-coordinate from x_{A2} to x_{A3}. A13 (or $y_{A3...A6}$) is the average of y-coordinate from x_{A3} to x_{A6}. A14 (or $y_{A1...A3}$) is the average of y-coordinate from x_{A1} to x_{A3}. A15 (or $y_{A1...A6}$) is the average of y-coordinate from x_{A1} to x_{A6}. A16 (or $y_{A1...A4}$) is the average of y-coordinate from x_{A1} to x_{A4}. A17 (or $y_{A3...A4}$) is the average of y-coordinate from x_{A3} to x_{A4}. A18 (or $y_{A4...A6}$) is the average of y-coordinate from x_{A4} to x_{A6}. A19 (or $y_{A2...A4}$) is the average of y-coordinate from x_{A2} to x_{A4}. A20 (or $y_{A4...A7}$) is the average of y-coordinate across the range x_{A4} to x_{A7}. These are all listed in table 6.

Table 6. Coordinates analyzed from synchrotron x-ray topographic images.

Location of interest	Alternate notation	Explanation
A0	x_{A0}	Index origin
A1	x_{A1}	Intensity 20% rise point index (measured as 20% of y_{A2})
A2	x_{A2}	First y-maximum y_{A2} from origin
A3	x_{A3}	First local y-minimum y_{A3} from origin
A4	x_{A4}	Global y-minimum y_{A4}
A5	x_{A4-A1}	x_{A4} minus x_{A1}
A6	x_{A6}	Final coordinate index of image
A7	x_{A7}	Global y-maximum y_{A7}
A8	x_{A7-A4}	x_{A7} minus x_{A4}
A9	x_{A6-A7}	x_{A6} minus x_{A7}
A10	x_{A6-A4}	x_{A6} minus x_{A4}

A11	$y_{A1\ldots A2}$	Average of y-coordinate across the range x_{A1} to x_{A2}
A12	$y_{A2\ldots A3}$	Average of y-coordinate across the range x_{A2} to x_{A3}
A13	$y_{A3\ldots A6}$	Average of y-coordinate across the range x_{A3} to x_{A6}
A14	$y_{A1\ldots A3}$	Average of y-coordinate across the range x_{A1} to x_{A3}
A15	$y_{A1\ldots A6}$	Average of y-coordinate across the range x_{A1} to x_{A6}
A16	$y_{A1\ldots A4}$	Average of y-coordinate across the range x_{A1} to x_{A4}
A17	$y_{A3\ldots A4}$	Average of y-coordinate across the range x_{A3} to x_{A4}
A18	$y_{A4\ldots A6}$	Average of y-coordinate across the range x_{A4} to x_{A6}
A19	$y_{A2\ldots A4}$	Average of y-coordinate across the range x_{A2} to x_{A4}
A20	$y_{A4\ldots A7}$	Average of y-coordinate across the range x_{A4} to x_{A7}

The analysis of the etch pit micrographs should have a slightly different approach. The prints are scanned into the computer, then cropped to a size containing one wafer thickness at the most. The wafer 20320 did not go through backgrinding, so the etch pit images enclose only a part of the wafer, though most of the wafer.

Figure 19 shows the procedure, where the algorithm scans the image horizontally for darkness changes between neighboring pixels in Fig. 19(a). These locations, where dots represent defects and precipitates, and lines represent stacking faults, are visually enhanced until the next major pixel darkness changes occurs, and 19(b) is obtained. Several variations of the algorithm were tested to find a good threshold, wherein the pixel darkness change and the effect of neighboring pixels give the best results. After this the dark pixels are again sorted to the left side of the images to arrive to 19(c), and the characteristic curve information is extracted as pixel coordinates and used in the same manner as the coordinates in the synchrotron images, i.e. x_{B0}, ... , x_{B4} are projected on the vertical coordinate axis, and are taken as index values, i.e. pixel indices.

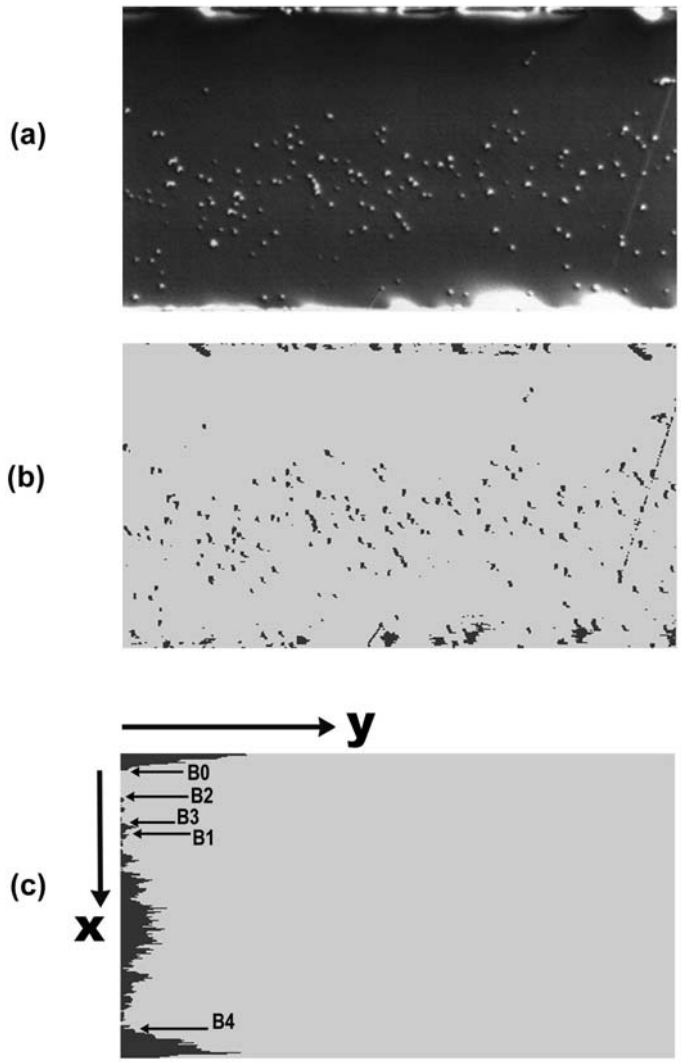


Figure 19. (a) etch pit micrograph; (b) image with enhanced precipitates and stacking faults before pixel-sorting; (c) pixel-sorted image of (b) also showing the extracted feature parameters. The image size is about 450 x 250 pixels (width x height).

The x-values of the specific features are denoted as x_{B0}, ... , x_{B4}. In the etch pit image derivative, B0 (or x_{B0}) is the origin of the parametric image data (or zero x-coordinate), B1 (x_{B1}) is the x-value where the y-value has reached 20% of its maximum height, cumulative pixels, in the image. B2 (x_{B2}) is the x-value of the end of a "clear zone" (or zone practically precipitate-free), thus indicating the third occurence of y-value exceeding 0.001 (= 0.1%) of the image maximum y-height. B3 (x_{B3}) is the x-coordinate value of the end of "small precipitates zone", i.e. the x-value, where the fifth occurence of y-value exceeding 0.01 (= 1%) takes place. Finally, B4 (x_{B4}) is at the bottom of the image, i.e. the x-value where the interpretable image ends, whereafter only noise and distortion is assumed to remain.

Additionally, y-coordinates, averaged and integrated image data were also combined into several parameters for correlation computations as B5 ($y_{B0...B1}$), B6 ($y_{B0...B2}$), B7 ($y_{B0...B3}$), B8 ($y_{B1...B2}$), B9 ($y_{B2...B3}$), B10 ($y_{B2...B4}$), B11 ($y_{B3...B4}$), B12 ($y_{B0...B4}$), B13 ($y_{B1...B3}$), B14 ($y_{B1...B4}$). These are all detailed out in Table 7.

Table 7. Etch pit imagedata coordinates.

Location of interest	Alternate notation	Explanation
B0	x_{B0}	Index origin
B1	x_{B1}	End of 20% cumulative precipitates
B2	x_{B2}	End of clear zone
B3	x_{B3}	End of small precipitate zone
B4	x_{B4}	Bottom of image
B5	$y_{B0...B1}$	Average y-coordiante of origin ... B1
B6	$y_{B0...B2}$	Average y-coordinate of origin ... B2
B7	$y_{B0...B3}$	Average y-coordinate of origin ... B3
B8	$y_{B1...B2}$	Average y-coordinate of B1 ... B2
B9	$y_{B2...B3}$	Average y-coordinate of B2 ... B3
B10	$y_{B2...B4}$	Average y-coordinate of B2 ... B4
B11	$y_{B3...B4}$	Average y-coordinate of B3 ... B4
B12	$y_{B0...B4}$	Average y-coordinate of origin ... B4
B13	$y_{B1...B3}$	Average y-coordinate of B1 ... B3
B14	$y_{B1...B4}$	Average y-coordinate of B1 ... B4

Integrated circuits are processed to the surface part of the wafer, and therefore the wafer defects detectable by the methods used here, do not necessarily predict the electrical properties of the final integrated circuits. Also, the electronic components processed onto the wafer surface parts, cause strain, which is visible in the surface part of the synchrotron images as darkness.

Both the coordinate index tables of the synchrotron X-ray topographs and etch pit micrographs produce vast amounts of data. Next, the most interesting matches are lined out.

4.3 Statistical Methods

The size of the data table becomes quite large, and ordinary Excel spreadsheet is the most convenient tool. The interest is in computing correlation coefficients to identify the relevant parameters (PCM & yield) affected by the strain and precipitates.

Linear least squares fitting is used to accomplish the linear regression, which is justifiable to be used for the derivates of the synchrotron X-ray topographic images,

because the darkness-to-intensity transformation, equation (2), has already been applied to the data. What actually took place in the study first, is that a transformation function was not initially used, and then any reasonable correlation did not exist.

With the derivatives of the etch pit micrographs, a linear relationship with the number of precipitates and stacking faults is anticipated, and no transformation there is expected to be required.

The PCM data contains some noise, and the exact locations of the test dice are not documented, so it is not reasonable to compute the correlations based on their locations on the wafers. Therefore, the PCM parameters are averaged for each wafer, and then correlated against the averaged extracted image feature parameters.

With the table in Excel and with the help of the functions available there, we obtain the correlation coefficients (also known as the product-moment coefficient of correlation, or Pearson's correlation). The result of synchrotron X-ray topographic data correlated against the PCM parameters & yield is shown in table 8.

Since there are only few correlation data points, we need to show that the obtained correlation coefficients (r) significantly differ from zero. Therefore, we use the hypothesis testing of discarding H_0: $r=0$ and accepting H_1: $r\neq0$ using the Student's t-distribution. The degrees of freedom used should be $n-2 = 6-2 = 4$, where n is the number of samples. The resulting confidence levels (significance) are shown in table 9.

Table 8. Pearson's correlation coefficients of synchrotron X-ray image parameters

PCM parameter	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20
NMOS Vt0	0.02	-0.14	-0.46	-0.07	-0.09	-0.42	-0.44	-0.55	0.29	-0.17	-0.19	-0.26	-0.02	-0.27	-0.05	-0.12	-0.27	0.06	-0.32	-0.05
NMOS Beta	-0.11	-0.19	-0.30	-0.24	-0.25	-0.18	-0.57	-0.65	0.45	0.05	-0.03	-0.38	-0.19	-0.30	-0.21	0.01	-0.49	-0.13	-0.43	-0.23
NMOS IDS3	-0.07	0.10	0.34	-0.22	-0.24	0.76	-0.28	-0.28	0.41	0.53	-0.05	-0.56	-0.55	-0.43	-0.56	-0.05	-0.37	-0.57	-0.48	-0.57
NMOS Vbreakdown	0.08	-0.08	-0.32	0.09	0.09	-0.76	0.02	-0.01	-0.18	-0.44	0.06	0.35	0.37	0.27	0.38	0.10	0.10	0.40	0.24	0.38
NMOS IDS	0.92	0.87	0.50	0.66	0.62	-0.33	0.33	0.17	-0.35	-0.57	-0.77	-0.46	0.18	-0.58	0.13	-0.70	0.51	0.21	-0.08	0.21
PMOS IDS	0.17	-0.03	-0.49	0.30	0.32	-0.36	-0.09	-0.24	0.00	-0.37	-0.54	-0.34	0.23	-0.41	0.18	-0.57	0.17	0.32	-0.14	0.19
PMOS Vt0	-0.48	-0.55	-0.75	-0.71	-0.73	0.50	-0.95	-0.96	0.92	0.69	0.01	-0.43	-0.80	-0.36	-0.81	0.17	-0.80	-0.75	-0.86	-0.82
PMOS Beta	0.14	0.02	-0.38	-0.13	-0.16	0.11	-0.64	-0.79	0.57	0.13	-0.51	-0.76	-0.46	-0.75	-0.50	-0.39	-0.39	-0.37	-0.78	-0.47
PMOS IDS3	0.13	0.23	0.59	0.40	0.43	-0.27	0.82	0.92	-0.76	-0.38	0.31	0.64	0.63	0.61	0.66	0.16	0.59	0.56	0.86	0.65
PMOS Vbreakdown	0.15	0.28	0.57	0.37	0.40	0.16	0.51	0.52	-0.41	-0.15	-0.05	-0.03	0.29	0.00	0.29	-0.21	0.37	0.26	0.36	0.28
N- bulk resistance	-0.39	-0.44	-0.67	-0.61	-0.63	0.69	-0.80	-0.80	0.84	0.73	-0.11	-0.44	-0.83	-0.41	-0.84	0.04	-0.63	-0.80	-0.83	-0.83
P- sheet resistance	-0.22	-0.05	0.23	-0.25	-0.25	0.83	-0.15	-0.10	0.31	0.58	0.06	-0.32	-0.48	-0.21	-0.48	0.04	-0.26	-0.52	-0.31	-0.49
PG sheet resistance	-0.34	-0.37	-0.08	-0.02	0.03	-0.65	0.36	0.48	-0.45	-0.32	0.69	0.91	0.64	0.91	0.69	0.57	0.16	0.61	0.80	0.63
NG sheet resistance	0.10	0.20	0.22	0.10	0.09	0.65	0.19	0.21	-0.02	0.28	-0.26	-0.22	-0.26	-0.24	-0.27	-0.27	0.20	-0.29	-0.13	-0.24
PS sheet resistance	-0.84	-0.87	-0.85	-0.88	-0.87	0.51	-0.78	-0.68	0.78	0.80	0.47	0.12	-0.66	0.20	-0.63	0.58	-0.77	-0.65	-0.49	-0.67
Al/Metal C	0.70	0.76	0.79	0.45	0.41	-0.34	0.37	0.30	-0.39	-0.45	-0.24	-0.15	0.21	-0.18	0.20	-0.21	0.33	0.20	0.14	0.25
Al/Metal C mDissipation	-0.74	-0.71	-0.55	-0.51	-0.47	0.55	-0.32	-0.22	0.40	0.60	0.37	0.15	-0.31	0.22	-0.28	0.32	-0.38	-0.32	-0.13	-0.34
Al/Metal C leak12V	0.48	0.56	0.57	0.18	0.14	-0.02	0.26	0.26	-0.23	-0.12	-0.11	0.02	-0.06	-0.03	-0.05	-0.01	0.23	-0.10	0.04	0.00
NS sheet resistance	-0.29	-0.46	-0.73	-0.31	-0.31	-0.23	-0.61	-0.67	0.47	0.07	-0.02	-0.19	-0.15	-0.17	-0.17	0.03	-0.45	-0.08	-0.39	-0.19
Metal/P- C leak20V	-0.36	-0.20	0.36	-0.27	-0.25	-0.01	0.23	0.40	-0.20	0.16	0.81	0.70	0.14	0.78	0.21	0.76	-0.10	0.06	0.51	0.15
Metal sheet resistance	0.10	-0.09	-0.40	0.15	0.16	-0.74	0.09	0.06	-0.24	-0.47	-0.02	0.37	0.41	0.26	0.41	0.01	0.22	0.44	0.27	0.42
Metal 2u electrical linewidth	0.04	0.24	0.55	-0.09	-0.11	0.52	0.22	0.33	-0.08	0.32	0.20	0.12	-0.25	0.15	-0.22	0.22	0.05	-0.33	0.06	-0.21
Metal 2u substrate leak	-0.39	-0.30	0.05	-0.36	-0.34	0.21	-0.36	-0.33	0.36	0.33	0.37	-0.16	-0.20	0.00	-0.19	0.31	-0.52	-0.20	-0.18	-0.25
Metal 2u optical linewidth	-0.34	-0.24	-0.07	-0.21	-0.19	0.68	-0.18	-0.15	0.30	0.48	0.01	-0.29	-0.33	-0.20	-0.34	-0.05	-0.23	-0.34	-0.26	-0.36
Al resistance	-0.34	-0.15	0.43	-0.16	-0.13	0.24	0.25	0.39	-0.16	0.22	0.60	0.39	0.10	0.50	0.14	0.48	-0.06	0.02	0.40	0.08
Al sheet resistance	-0.20	0.01	0.54	-0.11	-0.10	0.41	0.20	0.31	-0.08	0.28	0.41	0.14	-0.05	0.25	-0.02	0.32	-0.07	-0.12	0.21	-0.06
Al sheet leakage	-0.23	-0.21	-0.30	-0.66	-0.70	0.53	-0.79	-0.77	0.79	0.67	0.07	-0.37	-0.85	-0.30	-0.85	0.28	-0.72	-0.84	-0.80	-0.83
Metal contact(size1)	-0.03	-0.23	-0.51	0.15	0.17	-0.76	-0.01	-0.07	-0.16	-0.48	-0.03	0.24	0.47	0.17	0.46	-0.06	0.12	0.53	0.23	0.45
Metal contact(size2)	0.19	-0.02	-0.36	0.30	0.30	-0.83	0.13	0.06	-0.30	-0.61	-0.16	0.24	0.52	0.13	0.51	-0.16	0.29	0.57	0.28	0.52
Metal contact(size2) chain	0.20	0.01	-0.31	0.27	0.27	-0.82	0.15	0.10	-0.31	-0.59	-0.11	0.31	0.50	0.19	0.49	-0.09	0.29	0.54	0.31	0.50
P- sheet contact(size1) chain	-0.14	-0.03	0.00	-0.34	-0.36	0.96	-0.42	-0.42	0.57	0.70	-0.19	-0.59	-0.76	-0.51	-0.78	-0.12	-0.39	-0.77	-0.68	-0.76
P- sheet contact(size2) chain	0.20	0.28	0.15	-0.25	-0.30	0.68	-0.43	-0.47	0.52	0.50	-0.33	-0.63	-0.78	-0.60	-0.80	-0.16	-0.33	-0.78	-0.75	-0.74
N- sheet contact(size1) chain	-0.51	-0.31	0.29	-0.51	-0.50	0.38	-0.10	0.07	0.17	0.50	0.78	0.38	-0.22	0.53	-0.17	0.75	-0.42	-0.30	0.14	-0.23
N- sheet contact(size2) chain	-0.89	-0.86	-0.57	-0.91	-0.89	0.26	-0.60	-0.42	0.57	0.68	0.87	0.50	-0.42	0.61	-0.36	0.94	-0.76	-0.46	-0.13	-0.43
Thin-film sheet resistance	0.48	0.56	0.39	0.19	0.15	0.51	0.09	0.04	0.03	0.15	-0.52	-0.47	-0.39	-0.52	-0.41	-0.42	0.19	-0.41	-0.36	-0.34
Thin-film leakage	0.07	0.25	0.48	0.02	0.01	0.72	0.13	0.16	0.05	0.36	-0.11	-0.30	-0.32	-0.25	-0.32	-0.14	0.04	-0.37	-0.16	-0.31
Thin-film resistance (width1)	0.52	0.56	0.30	0.22	0.17	0.39	0.09	0.03	0.01	0.07	-0.56	-0.43	-0.34	-0.52	-0.37	-0.45	0.23	-0.35	-0.35	-0.29
Thin-film resistance (width2)	0.58	0.66	0.48	0.28	0.23	0.42	0.16	0.10	-0.05	0.05	-0.56	-0.48	-0.31	-0.54	-0.34	-0.47	0.26	-0.33	-0.31	-0.26
Thin-film R delta-length	0.51	0.69	0.82	0.29	0.26	0.44	0.27	0.24	-0.14	0.05	-0.34	-0.44	-0.20	-0.42	-0.22	-0.33	0.21	-0.24	-0.14	-0.17
Wafer yield	-0.45	-0.45	-0.34	-0.69	-0.71	0.03	-0.61	-0.53	0.53	0.43	0.54	0.20	-0.43	0.28	-0.40	0.68	-0.68	-0.44	-0.30	-0.43

Table 9. Confidence levels from the Student's t-test distribution of the synchrotron X-ray image parameters

PCM parameter	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20
NMOS Vt0	76%	82%	94%	78%	79%	93%	93%	96%	88%	83%	84%	87%	76%	87%	77%	81%	87%	78%	89%	77%
NMOS Beta	80%	84%	88%	86%	86%	83%	97%	98%	93%	77%	76%	91%	84%	88%	85%	76%	95%	81%	93%	85%
NMOS IDS3	78%	80%	90%	85%	86%	99%	88%	88%	92%	96%	77%	96%	96%	93%	96%	77%	91%	96%	94%	96%
NMOS Vbreakdown	79%	79%	89%	79%	79%	99%	76%	75%	83%	93%	78%	90%	91%	87%	91%	80%	80%	92%	86%	91%
NMOS IDS	100%	100%	95%	98%	97%	89%	89%	83%	90%	97%	99%	94%	83%	97%	81%	99%	95%	85%	79%	85%
PMOS IDS	83%	77%	95%	88%	89%	91%	79%	86%	75%	91%	96%	90%	85%	92%	83%	97%	83%	89%	82%	84%
PMOS Vt0	94%	96%	99%	99%	99%	95%	100%	100%	100%	99%	76%	93%	100%	90%	100%	83%	100%	99%	100%	100%
PMOS Beta	81%	76%	91%	81%	82%	80%	98%	100%	97%	81%	95%	99%	94%	99%	95%	91%	92%	91%	99%	94%
PMOS IDS3	81%	86%	97%	92%	93%	87%	100%	100%	99%	91%	88%	98%	98%	97%	98%	82%	97%	96%	100%	98%
PMOS Vbreakdown	82%	88%	96%	91%	92%	82%	95%	95%	92%	82%	77%	76%	88%	75%	88%	85%	91%	87%	90%	87%
N- bulk resistance	92%	93%	98%	97%	98%	99%	100%	100%	100%	99%	80%	93%	100%	92%	100%	77%	98%	100%	100%	100%
P- sheet resistance	85%	77%	86%	86%	86%	100%	82%	80%	89%	97%	78%	89%	94%	85%	94%	77%	87%	95%	89%	95%
PG sheet resistance	90%	91%	79%	76%	76%	98%	90%	94%	93%	89%	99%	100%	98%	100%	99%	97%	82%	97%	100%	98%
NG sheet resistance	79%	84%	85%	80%	79%	98%	84%	84%	76%	87%	87%	85%	86%	86%	87%	87%	84%	88%	81%	86%
PS sheet resistance	100%	100%	100%	100%	100%	95%	99%	98%	99%	100%	94%	81%	98%	84%	98%	97%	99%	98%	94%	98%
Al/Metal C	99%	99%	99%	93%	92%	90%	91%	88%	91%	93%	86%	82%	85%	83%	84%	85%	89%	84%	82%	86%
Al/Metal C mDissipation	99%	99%	96%	95%	94%	96%	89%	85%	92%	97%	91%	82%	89%	85%	88%	89%	91%	89%	81%	90%
Al/Metal C leak12V	94%	96%	97%	83%	81%	76%	87%	87%	85%	81%	80%	76%	78%	76%	77%	75%	85%	80%	77%	75%
NS sheet resistance	88%	94%	99%	89%	89%	86%	97%	98%	94%	78%	76%	84%	82%	83%	83%	77%	93%	79%	91%	84%
Metal/P- C leak20V	90%	84%	91%	87%	86%	76%	85%	92%	84%	82%	100%	99%	82%	99%	84%	99%	80%	78%	95%	82%
Metal sheet resistance	80%	79%	92%	82%	82%	99%	79%	78%	86%	94%	76%	91%	92%	87%	92%	75%	85%	93%	87%	93%
Metal 2u electrical linewidth	77%	86%	96%	79%	80%	95%	85%	89%	79%	89%	84%	81%	86%	82%	85%	85%	77%	89%	78%	85%
Metal 2u substrate leak	91%	88%	78%	90%	90%	85%	91%	90%	90%	89%	91%	83%	84%	75%	84%	89%	95%	84%	83%	86%
Metal 2u optical linewidth	90%	86%	78%	85%	84%	98%	83%	82%	88%	94%	76%	88%	90%	84%	90%	78%	85%	90%	86%	91%
Al resistance	90%	82%	93%	82%	81%	86%	86%	91%	82%	85%	97%	92%	79%	95%	81%	94%	78%	76%	92%	79%
Al sheet resistance	84%	76%	96%	80%	80%	92%	84%	88%	79%	87%	92%	82%	77%	86%	76%	89%	78%	80%	85%	78%
Al sheet leakage	86%	85%	88%	98%	99%	96%	100%	99%	100%	98%	78%	91%	100%	88%	100%	87%	99%	100%	100%	100%
Metal contact(size1)	76%	86%	95%	82%	83%	99%	76%	78%	82%	94%	77%	86%	94%	83%	94%	78%	80%	96%	86%	93%
Metal contact(size2)	84%	76%	91%	88%	88%	100%	81%	78%	88%	97%	82%	86%	95%	81%	95%	82%	88%	97%	88%	95%
Metal contact(size2) chain	84%	76%	89%	87%	87%	100%	82%	79%	89%	97%	80%	89%	95%	84%	95%	79%	88%	96%	88%	95%
P- sheet contact(size1) chain	82%	76%	75%	90%	90%	100%	93%	92%	97%	99%	84%	97%	99%	95%	99%	81%	91%	99%	98%	99%
P- sheet contact(size2) chain	84%	87%	82%	86%	88%	98%	93%	94%	95%	95%	89%	98%	99%	97%	100%	82%	89%	99%	99%	99%
N- sheet contact(size1) chain	95%	89%	88%	95%	95%	91%	80%	78%	83%	95%	99%	91%	85%	96%	83%	99%	92%	88%	81%	85%
N- sheet contact(size2) chain	100%	100%	96%	100%	100%	86%	97%	93%	96%	98%	100%	95%	93%	97%	91%	100%	99%	94%	81%	93%
Thin-film sheet resistance	94%	96%	92%	84%	82%	95%	79%	77%	77%	82%	95%	94%	91%	95%	92%	93%	84%	92%	91%	90%
Thin-film leakage	78%	86%	94%	76%	76%	99%	81%	82%	77%	90%	80%	88%	89%	86%	89%	81%	77%	91%	82%	89%
Thin-film resistance (width1)	95%	96%	88%	85%	83%	91%	79%	76%	75%	78%	96%	93%	90%	95%	91%	93%	85%	90%	90%	88%
Thin-film resistance (width2)	97%	98%	94%	87%	86%	92%	82%	80%	77%	77%	96%	94%	89%	96%	90%	94%	87%	89%	89%	87%
Thin-film R delta-length	95%	99%	100%	88%	87%	93%	87%	86%	81%	77%	90%	93%	84%	93%	85%	89%	85%	86%	82%	83%
Wafer yield	93%	93%	90%	99%	99%	77%	97%	96%	96%	93%	96%	84%	93%	88%	92%	98%	98%	93%	88%	93%

The most prominent results of the correlation analysis between the synchrotron X-ray topographs and the PCM data are going to be chosen for a detailed examination in Fig. 20.

Fig. 20(a) plots the aluminum-to-metal capacitor values as a function of x_{A2} image parameter, i.e. the x-coordinate of the first y-maximum of the curve, showing r=0.76 and a significance of 99.3%. Fig. 20(b) plots the N sheet contact chain resistance as a function of x_{A1} image parameter, i.e. the x-coordinate of the location where y-coordinate reaches 20% of the first y-maximum, showing r=-0.89 and a significance of 99.9%.

Fig. 20(c) plots the wafer yield as a function of the x_{A4} image parameter resulting with r=-0.69 and a significance of 98.5%. It is worth noting that such an inner location as x_{A4} would not necessarily be considered very relevant from the point of wafer manufacturing. One would expect the top surface to have more emphasis for the correlation, and not the inner region to this extent. The actual yield is marked as a number next to each plot point. Also, Fig. 20(d) shows a reasonable correlation of wafer yield as a function of $y_{A1...A4}$ image parameter, i.e. the averaged y-coordinate from A1 to A4, with r=0.68 and significance 98.5%.

Figs. 20(e) and 20(f), respectively, plot the PMOS and NMOS threshold voltages (V_{T0}) as a function of x_{A8} image parameter, i.e. x_{A7} minus x_{A4}. The NMOS voltage in Fig. 20(f) seems independent of the parameter, but the PMOS threshold voltage clearly correlates with r=-0.96 and a significance of 100.0% in Fig. 20(e). This suggests that a higher absolute value of the PMOS threshold voltage is attained with a smaller slope value from A4 to A7, i.e. smaller strain gradient on the backside of the wafer.

Figs. 20(g) and 20(h), respectively, plot the PMOS and NMOS I_{DS}, drain to source current at 3V. Again, the NMOS data is scattered, and the PMOS data correlates with r=0.92 and a significance of 100.0%. In this case the PMOS current should behave like this as it is also linked to the voltage correlation of Fig. 20(e).

One possible explaining factor for the PMOS and NMOS correlation difference is that all wafers are of n^- type, and thus NMOS transistors all have to be placed in a p-well, and this might hide the observability of the NMOS transistor parameter correlation.

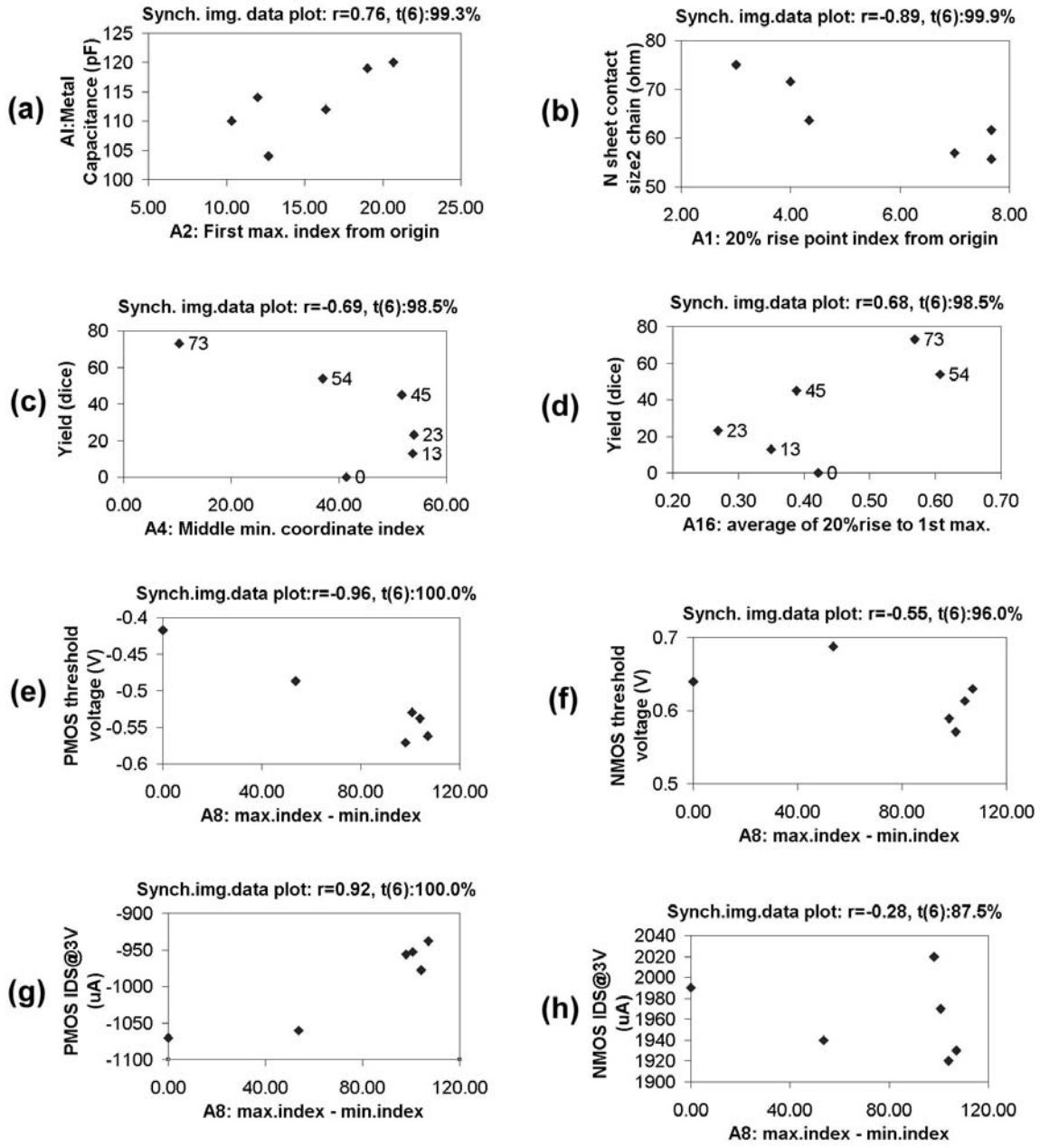


Figure 20. Plots of PCM parameters vs. synchrotron X-ray topographic feature values.

Now, to move from synchrotron X-ray topography to etch pit micrographic data, the result of correlating the etch pit micrographs and the electrical PCM data, is shown in table 10. Again, we use the hypothesis testing of discarding H_0: r=0 and accepting H_1: r≠0 using the Student's t-distribution. The resulting confidence levels (significance) are shown in table 11. The interests in certain parametric factors are all contributors to the selection criteria of the parameters for a closer inspection in Fig. 21.

Table 10. Pearson's correlation coefficients of etch pit image parameters.

PCM parameter	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14
NMOS Vt0	-0,23	0,29	-0,01	0,03	0,33	0,14	0,56	-0,34	0,82	0,46	0,46	0,47	-0,30	-0,30
NMOS Beta	0,04	0,69	0,25	-0,24	-0,01	-0,15	0,43	-0,35	0,83	0,49	0,50	0,48	-0,25	-0,25
NMOS IDS3	0,71	0,60	0,61	-0,55	-0,79	-0,37	-0,16	0,34	-0,37	-0,05	-0,03	-0,08	0,40	0,40
NMOS breakdownvoltage	-0,71	-0,28	-0,49	0,43	0,78	0,33	0,35	-0,48	0,66	0,27	0,26	0,30	-0,47	-0,47
NMOS IDS	-0,63	-0,35	-0,61	0,70	0,67	0,16	0,00	-0,25	-0,24	0,61	0,61	0,64	-0,38	-0,38
PMOS IDS	-0,04	0,06	-0,08	0,18	0,21	-0,04	0,22	-0,14	0,37	0,39	0,39	0,40	-0,25	-0,25
PMOS Vt0	0,57	0,22	0,75	-0,71	-0,43	0,59	0,93	0,59	0,38	-0,38	-0,36	-0,38	0,66	0,66
PMOS Beta	0,17	0,31	0,32	-0,21	-0,03	0,27	0,69	0,13	0,41	0,31	0,33	0,32	0,12	0,12
PMOS IDS3	-0,33	-0,26	-0,52	0,43	0,18	-0,46	-0,86	-0,34	-0,44	-0,02	-0,04	-0,03	-0,37	-0,37
PMOS breakdownvoltage	0,24	0,29	-0,04	0,07	-0,36	-0,79	-0,85	-0,14	-0,52	0,16	0,16	0,14	-0,17	-0,17
N- bulk resistance	0,66	-0,07	0,74	-0,67	-0,50	0,71	0,84	0,86	-0,02	-0,60	-0,58	-0,59	0,87	0,87
P- sheet resistance	0,79	0,34	0,61	-0,56	-0,86	-0,28	-0,24	0,54	-0,58	-0,36	-0,35	-0,39	0,56	0,56
PG sheet resistance	-0,45	-0,03	-0,39	0,24	0,35	-0,28	-0,35	-0,61	0,47	0,01	-0,01	0,00	-0,52	-0,52
NG sheet resistance	0,48	-0,33	0,22	-0,14	-0,46	0,09	-0,24	0,68	-0,92	-0,47	-0,47	-0,47	0,57	0,57
PS sheet resistance	0,61	0,00	0,75	-0,79	-0,52	0,62	0,76	0,68	0,29	-0,80	-0,79	-0,80	0,77	0,77
Al/Metal Capacitance	-0,67	-0,03	-0,57	0,57	0,56	-0,15	-0,26	-0,53	-0,09	0,62	0,62	0,63	-0,52	-0,52
Al/Metal C mDissipation	0,82	0,16	0,68	-0,69	-0,78	-0,02	0,06	0,58	-0,10	-0,69	-0,69	-0,71	0,61	0,61
Al/Metal C leak12V	-0,51	-0,49	-0,42	0,39	0,45	0,39	0,01	0,00	-0,39	0,02	0,02	0,05	-0,02	-0,02
NS sheet resistance	0,06	0,34	0,26	-0,25	0,06	0,19	0,65	-0,12	0,85	0,18	0,19	0,18	-0,06	-0,06
Metal/P- C leak20V	-0,11	0,10	-0,06	-0,09	-0,09	-0,26	-0,41	-0,24	-0,01	-0,25	-0,26	-0,27	-0,09	-0,09
Metal sheet resistance	-0,69	-0,47	-0,52	0,48	0,79	0,43	0,35	-0,35	0,52	0,16	0,14	0,19	-0,39	-0,39
Metal 2u electrical linewidth	0,14	-0,28	0,06	-0,09	-0,26	0,11	-0,28	0,39	-0,75	-0,44	-0,44	-0,45	0,40	0,40
Metal 2u substrate leak	0,46	0,98	0,51	-0,53	-0,58	-0,66	-0,15	-0,25	0,42	0,22	0,24	0,18	-0,09	-0,09
Metal 2u optical linewidth	0,86	0,41	0,64	-0,58	-0,87	-0,36	-0,22	0,48	-0,38	-0,32	-0,31	-0,35	0,48	0,48
Al resistance	0,28	0,37	0,16	-0,25	-0,48	-0,62	-0,65	-0,11	-0,23	-0,19	-0,19	-0,22	-0,01	-0,01
Al sheet resistance	0,38	0,41	0,24	-0,28	-0,56	-0,61	-0,63	0,00	-0,39	-0,14	-0,14	-0,17	0,09	0,09
Al sheet leakage	0,28	0,02	0,53	-0,53	-0,23	0,73	0,85	0,54	0,15	-0,36	-0,35	-0,35	0,63	0,63
Metal contact(size1)	-0,47	-0,03	-0,34	0,32	0,56	0,04	0,24	-0,51	0,76	0,36	0,35	0,38	-0,52	-0,52
Metal contact(size2)	-0,68	-0,28	-0,55	0,53	0,78	0,19	0,23	-0,51	0,60	0,39	0,38	0,42	-0,56	-0,56
Metal contact(size2) chain	-0,75	-0,38	-0,59	0,56	0,84	0,29	0,25	-0,48	0,56	0,33	0,31	0,36	-0,53	-0,53
P- sheet contact(size1) chain	0,82	0,15	0,71	-0,62	-0,79	0,17	0,20	0,82	-0,58	-0,46	-0,44	-0,47	0,81	0,81
P- sheet contact(size2) chain	0,30	-0,14	0,37	-0,29	-0,25	0,57	0,49	0,64	-0,44	-0,25	-0,23	-0,24	0,64	0,64
N- sheet contact(size1) chain	0,32	0,41	0,36	-0,47	-0,51	-0,31	-0,28	0,01	-0,03	-0,34	-0,34	-0,37	0,19	0,19
N- sheet contact(size2) chain	0,32	0,14	0,54	-0,67	-0,35	0,37	0,50	0,26	0,48	-0,67	-0,67	-0,68	0,45	0,45
Thin-film sheet resistance	0,10	-0,48	0,00	0,09	-0,06	0,43	0,07	0,58	-0,83	-0,21	-0,20	-0,19	0,46	0,46
Thin-film leakage	0,55	0,07	0,32	-0,27	-0,62	-0,23	-0,40	0,48	-0,82	-0,28	-0,27	-0,30	0,45	0,45
Thin-film resistance (width1)	-0,04	-0,60	-0,10	0,19	0,11	0,56	0,18	0,54	-0,75	-0,18	-0,18	-0,15	0,41	0,41
Thin-film resistance (width2)	-0,02	-0,47	-0,10	0,20	0,04	0,37	0,02	0,46	-0,81	-0,09	-0,08	-0,07	0,35	0,35
Thin-film R delta-length	0,10	0,02	-0,04	0,10	-0,20	-0,21	-0,41	0,16	-0,76	0,13	0,14	0,13	0,12	0,12
Wafer yield	-0,07	0,12	0,27	-0,37	0,05	0,50	0,67	0,02	0,61	-0,24	-0,24	-0,24	0,20	0,20

Table 11. Confidence levels from the Student's t-test distribution of the etch pit image parameters.

PCM parameter	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14
NMOS Vt0	85%	88%	75%	76%	89%	82%	96%	90%	100%	94%	94%	94%	88%	93%
NMOS Beta	77%	99%	86%	86%	75%	82%	93%	90%	100%	94%	95%	94%	86%	94%
NMOS IDS3	99%	97%	97%	96%	100%	91%	82%	90%	91%	78%	76%	79%	92%	76%
NMOS breakdownvoltage	99%	88%	95%	93%	99%	90%	90%	94%	98%	87%	87%	88%	94%	86%
NMOS IDS	98%	90%	97%	99%	98%	83%	75%	86%	86%	97%	97%	98%	91%	98%
PMOS IDS	77%	78%	79%	83%	84%	77%	85%	81%	91%	91%	91%	92%	86%	91%
PMOS Vt0	96%	85%	99%	99%	93%	97%	100%	97%	91%	91%	91%	91%	98%	91%
PMOS Beta	83%	89%	89%	85%	77%	87%	99%	81%	92%	89%	89%	89%	81%	89%
PMOS IDS3	90%	87%	95%	93%	83%	94%	100%	90%	93%	76%	77%	76%	91%	76%
PMOS breakdownvoltage	86%	88%	77%	78%	91%	100%	100%	81%	95%	83%	82%	81%	83%	83%
N- bulk resistance	98%	78%	99%	98%	95%	99%	100%	100%	76%	97%	97%	97%	100%	97%
P- sheet resistance	100%	90%	97%	96%	100%	87%	86%	96%	97%	91%	90%	91%	96%	90%
PG sheet resistance	94%	76%	92%	86%	90%	88%	90%	97%	94%	76%	75%	75%	95%	76%
NG sheet resistance	94%	90%	85%	82%	94%	79%	86%	98%	100%	94%	94%	94%	96%	94%
PS sheet resistance	97%	75%	99%	99%	95%	97%	99%	98%	88%	100%	100%	100%	99%	100%
Al/Metal Capacitance	98%	76%	97%	96%	96%	82%	86%	96%	79%	97%	97%	98%	95%	98%
Al/Metal C mDissipation	100%	82%	98%	99%	99%	76%	78%	97%	80%	99%	99%	99%	97%	99%
Al/Metal C leak12V	95%	95%	92%	92%	93%	91%	75%	75%	92%	76%	76%	77%	76%	77%
NS sheet resistance	78%	90%	87%	86%	78%	84%	98%	81%	100%	83%	84%	83%	78%	83%
Metal/P- C leak20V	80%	79%	78%	79%	79%	87%	92%	86%	75%	86%	87%	87%	79%	87%
Metal sheet resistance	99%	94%	95%	94%	100%	93%	90%	90%	95%	82%	82%	84%	91%	81%
Metal 2u electrical linewidth	82%	88%	78%	79%	87%	80%	88%	91%	99%	93%	93%	93%	92%	93%
Metal 2u substrate leak	94%	100%	95%	96%	97%	98%	82%	86%	93%	85%	86%	83%	79%	85%
Metal 2u optical linewidth	100%	92%	98%	97%	100%	91%	85%	94%	91%	89%	89%	90%	94%	89%
Al resistance	88%	91%	83%	86%	94%	97%	98%	80%	85%	84%	84%	85%	75%	84%
Al sheet resistance	91%	92%	86%	88%	96%	97%	98%	75%	91%	81%	81%	83%	79%	81%
Al sheet leakage	88%	76%	96%	96%	85%	99%	100%	96%	82%	91%	90%	90%	98%	90%
Metal contact(size1)	94%	76%	90%	89%	96%	77%	86%	95%	99%	91%	90%	91%	95%	90%
Metal contact(size2)	98%	88%	96%	96%	99%	84%	85%	95%	97%	92%	91%	92%	96%	91%
Metal contact(size2) chain	99%	91%	97%	96%	100%	88%	86%	94%	96%	89%	89%	90%	96%	89%
P- sheet contact(size1) chain	100%	82%	99%	97%	100%	83%	84%	100%	97%	94%	93%	94%	100%	93%
P- sheet contact(size2) chain	88%	81%	91%	88%	86%	96%	95%	98%	93%	86%	85%	86%	98%	85%
N- sheet contact(size1) chain	89%	92%	90%	94%	95%	89%	87%	75%	77%	90%	90%	91%	84%	90%
N- sheet contact(size2) chain	89%	82%	96%	98%	90%	91%	95%	87%	94%	98%	98%	98%	93%	98%
Thin-film sheet resistance	79%	94%	75%	79%	78%	93%	78%	97%	100%	84%	84%	84%	94%	83%
Thin-film leakage	96%	78%	89%	87%	97%	85%	92%	94%	100%	87%	87%	88%	93%	87%
Thin-film resistance (width1)	77%	97%	80%	84%	80%	96%	83%	96%	99%	83%	83%	82%	92%	82%
Thin-film resistance (width2)	76%	94%	80%	84%	77%	91%	76%	94%	100%	79%	79%	78%	90%	78%
Thin-film R delta-length	80%	76%	77%	80%	84%	85%	92%	82%	99%	81%	82%	81%	81%	82%
Wafer yield	78%	80%	87%	91%	78%	95%	98%	76%	97%	86%	86%	86%	84%	86%

Figure 21 shows the etch pit plots vs. various PCM parameters. Fig. 21(a) and (b) represent the NMOS I_{DS} (drain-to-source current) and PMOS I_{DS} plots respectively, having the cumulative precipitates count less than 20% of full scale (x_{B1}). Clearly the NMOS I_{DS} in Fig. 21(a) visually evaluated, appears to have a linear relationship (apart from one outlier), with r=0.71 and significance=98.8%. Apparently, the NMOS I_{DS} current is able to increase when the low-precipitate zone goes deeper. However, with PMOS I_{DS} plot in Fig. 21(b) there does not seem to be a clear dependence of the cumulative precipitates count below 20% of the full scale, also having r=-0.33 and significance=89.6%, representing very poor numbers.

Figure 21(c) shows the plot of N^- resistance vs. B7 ($y_{B0...B3}$) the average y-coordinate from the origin x_{B0} to x_{B3}, and it appears linear except for the one outlying data point. The correlation r=0.84 and the significance=99.8%. This would indicate that higher average cumulative precipitate count hints towards a higher N^- resistance. It would be required to analyze the absolute coordinates to make sure that this strange result were accurate.

Figure 21(d) has the Al/Mo capacitor dissipation factor vs. cumulative precipitates count less than 20% of full scale (x_{B1}). There is a reasonable linearity in the plot with r=0.82 and significance=99.7%. The more dissipation there is the deeper the 20% rise point goes.

Then, in Fig. 21(e) the Metal-to-substrate leakage current vs. B2 (x_{B2}) end of clear zone, shows extremely good correlation with r=0.98, and significance=100.0%. This would strangely state that the deeper the precipitates-free zone extends, the more there is leakage current from Metal into the substrate. There is not enough of information to explain the reason for this.

Figure 21(f) shows the yield vs. B2 (x_{B2}) end of clear zone, having a poor correlation r=0.12 and significance=80.5%. Practically, there is no real correlation. The numbers attached to the data points are the yield numbers of good dice, not percent.

Figure 21(g) presents the yield vs. B7 ($y_{B0...B3}$) the average y-coordinate from the origin x_{B0} and x_{B3}, there the linearity is much better with r=0.67 and significance=98.3% than in Fig. 21(f). The correlation here in Fig. 21(g) is not either on a very satisfactory level, but strangely indicates that higher precipitate count gives a better yield. There exists a possibility that the precipitates bind the contaminants, and in this way improve the performance of the electronics located on the wafers.

Then, Fig. 21(h) has the P^- sheet contact chain resistance vs. B1 (x_{B1}) the cumulative precipitates count less than 20% of full scale, with correlation coefficient r=0.82 and significance=99.7%. This result is in line with what would be expected, i.e. resistance slightly increases with increasing precipitate-free zone. Here the linearity looks very good, when we ignore the first data point as an outlier.

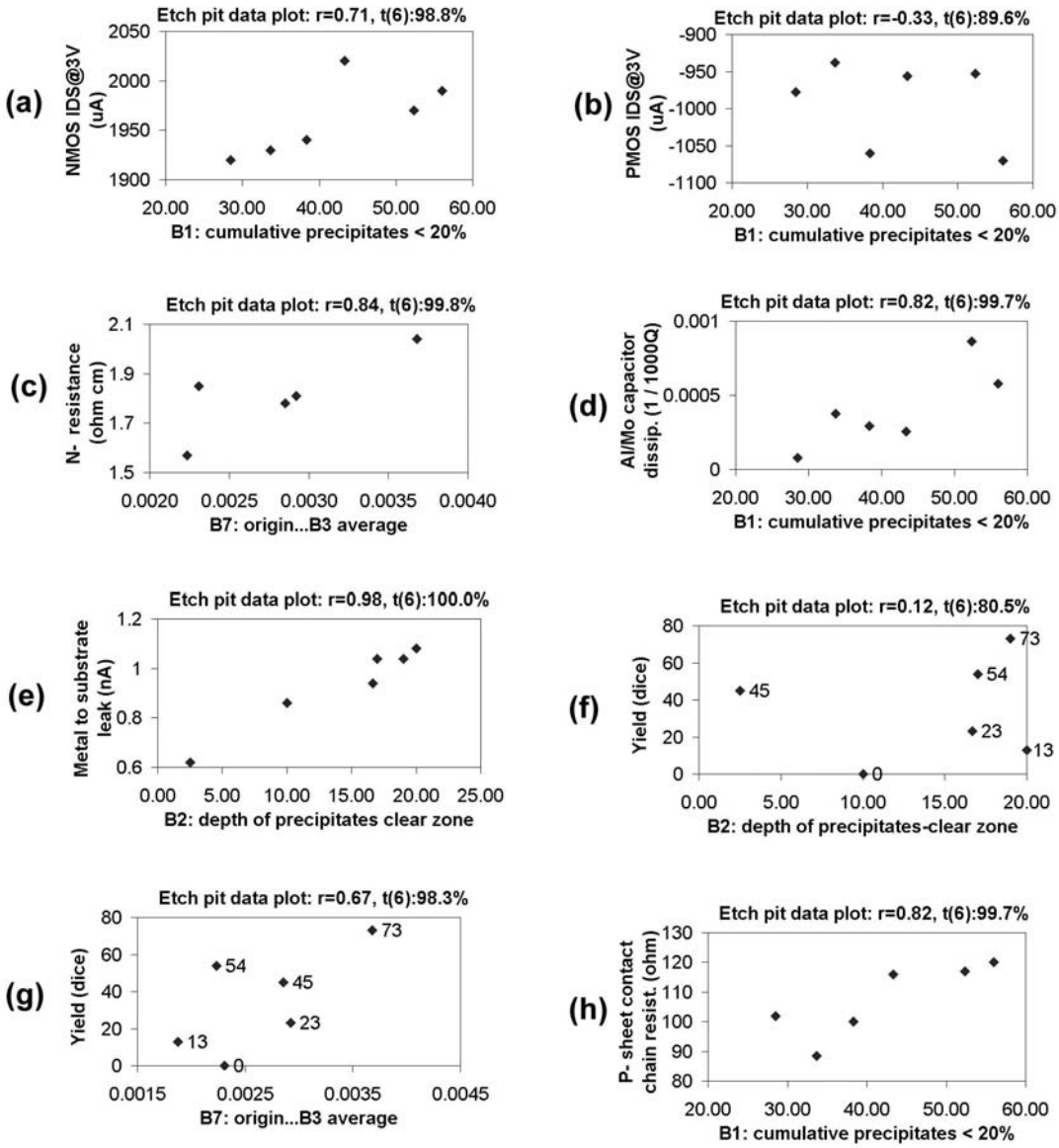


Figure 21. Plots of PCM parameters vs. etch pit micrograph feature values

There exist several studies attempting to correlate wafer quality with component properties [9], [10], [61]. This study combines X-ray synchrotron topographic and etch pit micrographic analysis data of wafer quality with various electrical PCM parameters obtained from five wafer locations from six wafers each by automatic wafer probing. The inherent property of X-ray topography is that it is able to visualize lattice strain gradient. The orientational X-ray contrast is a result of the lattice bending [51] i.e. stronger strain gradient, and therefore the stronger diffracted X-ray intensity results as darker film exposure. The strain in silicon is caused e.g. by lattice mismatch and bending, dislocations, and precipitates. The etch pit micrographs are especially useful for analyzing defects, precipitates and stacking faults.

The main results of this work state that wafer surface strain gradient and device functionality have positive correlation. This relationship may reflect a direct dependence between stronger diffracted X-ray intensity and better crystal quality [62], or the relationship may be indirect, e.g. stronger strain in the silicon and oxide interface,

forming trap states being able to bind alkali ions (Na+, K+), which are accumulated into the wafer surface layers from the residues of various process chemicals.

The relationship between the stronger strain gradient (most probably located in the silicon and oxide interface) in the wafer surface region and higher yield is apparent from the positive correlation coefficients of the surface region, yA1…A2, (r=0.54) and yA2…A3 (r=0.20) and yA1…A4 (r=0.68) vs. yield. On the other hand, in the interior part of the wafer, the negative correlation coefficients yA3…A6 (r=-0.43) and yA4…A6 (r=-0.44) vs. yield indicate a better yield with less internal strain (most probably originating from precipitates disrupting the crystal lattice). Also, the negative correlation coefficients of xA1 (r=-0.45) and xA2 (r=-0.45) and xA3 (r=-0.34) and xA4 (r=-0.69) and xA4-xA1 (r=-0.71) vs. yield, all indicate that the nearer the strain is located to the surface, the better the yield is.

Also, there is some indication from the etch pit micrograph analysis in Fig. 21(g), that the yield improves with higher precipitates concentration.

It would appear that after processing the electronic circuits onto the wafer, there remains no denuded zone below the active surface. It is possible that the strain in the interface of silicon and oxide, or some intermetallic structures contribute to the disappearance of the denuded zone, as none was observed in any of the images.

Previously, the author participated in a brief undocumented analysis, wherein ICs were processed on wafers in the same process, and these also revealed no denuded zone after the processing, even though the denuded zone constantly seems to appear in various process simulations [3], [4]. The brief analysis also dismissed the initial findings of stronger wafer surface strain gradient being linked to higher yield because of non-quantitative data and the lack of supporting studies [62] at the time.

The number of samples used in this study is relatively small. It is difficult to obtain a large series of wafers with PCM and yield data from a semiconductor fab, and then it takes an effort to use synchrotron facilities for X-ray topography to obtain good exposures for sufficient resolution. However, statistical analysis has been carried out using the Student's t-test for the correlation coefficients. There might also exist a possibility that some of the correlation is non-linear or exhibit co-dependence; therefore in addition to computing the correlation coefficients and the statistical confidence, the x-y plots were also visually checked for some manually chosen parameters, shown in Figs. 20 and 21. Most of the previously published articles have concentrated on process simulations, but here we have complicated integrated circuits processed on the wafer, and the conclusions are based on those results.

The results could indicate that the deep interior part of the wafer is not crucial, as might be expected, and that the regions adjacent to the electronic circuits, are important for the proper functionality of the electronic devices, e.g. the yield. Support for this comes from the absolute values of the correlation coefficients, e.g. yield correlating better against yA1...A4 with r=0.68 (surface) than against yA4...A6 with r=-0.44 (interior), when considering the absolute values only, hence dropping the sign of the value. Further statistical analysis would be required to substantiate this interpretation.

Usually in semiconductor industry, wafer backside gettering (intentional strain) and subsequent thermal annealing of the wafers is used for attracting precipitates [33]. Without diminishing the requirement for using gettering on the wafer backside (e.g. back grinding, sandblasting, ion implantation, laser melting, depositing amorphous or polycrystalline polysilicon films, or high-concentration backside phosphorous diffusion

and subsequent heat treatments) in order to create dislocation loops, grain boundaries, precipitates or other traps for metal atoms (Fe, Ni, Cu, Au) present in the substrate, this study indicates that good yield is especially exhibited by those wafers that show a higher strain gradient on the wafer front-side in the oxide-silicon interface than the others.

4.4 Self-Organizing Map Neural Net

This text covers the study done for paper VI. It is necessary to retain most of the text here, both to give the reader an understanding of the basics and the details about the analysis to substantiate the findings.

Introduction

The device yield factor is extremely important to semiconductor fabrication facilities (fab), as this directly translates into savings or costs. Various neural nets, including self-organizing maps (SOM) [63], have successfully been applied in the field of integrated circuit (IC) design modeling for yield optimization [64], spatial IC and wafer failure pattern analysis [65], [66], quality control [67], semiconductor process modeling [68], [69], [70], and functional yield and PCM analysis [71], [72], [73]. The main objective here is to analyze the yield dependence on various electrically and optically performed process control monitoring (PCM) measurements by using the SOM to identify the main factors for low yield of a heartbeat rate monitor IC device processed in a semiconductor fab. The high-dimensional parameter data probably contains non-linear dependencies, and ordinary linear regression methods will not be sufficient. Self-organizing maps (SOM) have shown their usefulness for analyzing yield and process control monitoring (PCM) data [71], [72], [73].

Simplified Principle of the Self-organizing Map

Figure 22 shows the structure of a 3 x 4 sized SOM vectors, thus each having 12 parameter (component) planes. The n-dimensional parameter space, which is represented by 12 map vectors $\underline{\mathbf{m}}_i = \{ \underline{\mathbf{A}}, \underline{\mathbf{B}}, \underline{\mathbf{C}}, \underline{\mathbf{D}}, \underline{\mathbf{E}}, \underline{\mathbf{F}}, \underline{\mathbf{G}}, \underline{\mathbf{H}}, \underline{\mathbf{I}}, \underline{\mathbf{J}}, \underline{\mathbf{K}}, \underline{\mathbf{L}} \}$ where the components of the vectors $\underline{\mathbf{A}}$, ..., $\underline{\mathbf{L}}$ range from 1 to n, representing the total map size of 3 x 4 x n components. Each of the neurons (vectors) initially contains a random value, and the map will be trained with q measurements, of which each one is n-dimensional, each dimension representing one measured parameter, and which are grouped together into a training data vector $\underline{\mathbf{x}}$. Training makes the map represent the measured data set more accurately, i.e. there will always be a single map vector, one of $\underline{\mathbf{m}}_i$, whose distance $||\underline{\mathbf{m}}_i - \underline{\mathbf{x}}||$ is the minimum (best match) and is denoted as $\underline{\mathbf{m}}^*_i$. The training is done by repeatedly sequencing through the set of measurement data vectors from 1 to q, finding the best matching vector $\underline{\mathbf{m}}^*_i$ from the map, and modifying its vector component values towards those of the training vector. Additionally, a small neighborhood around the best matching vector $\underline{\mathbf{m}}^*_i$ on the map is also modified towards the sample vector. All this is usually formulated for each i within the neighborhood as equation:

$$\underline{\mathbf{m}}_i (t + 1) = \underline{\mathbf{m}}_i (t) + \alpha_i (t) [c \, \underline{\mathbf{x}} (t) - \underline{\mathbf{m}}_i (t)] \qquad (4)$$

for one sequence, where α_i is the neighborhood kernel (or weight function, sometimes simplified to be the learning step size) decreasing from 1 down to 0 along with both increasing discrete time index *t*, and neighborhood distance on the map from the best matching vector $\underline{\mathbf{m}}^*_i$ (e.g. in fig. 22, **E** being the best matching vector, **H** is nearer in its neighborhood than **K**). After performing a sufficient number of training runs using the measurement vectors, the resulting map is assessed. One method of evaluating the quality of the map is to compute the average quantization error (expectation value) over the input samples, $E\{ \| \underline{\mathbf{x}} - \underline{\mathbf{m}}^*_i (x) \| \}$, where $\underline{\mathbf{m}}^*_i$ is the best matching map vector from the map for each measurement data vector $\underline{\mathbf{x}}$.

The idea and principle of the SOM are extensively handled in Kohonen's book [63].

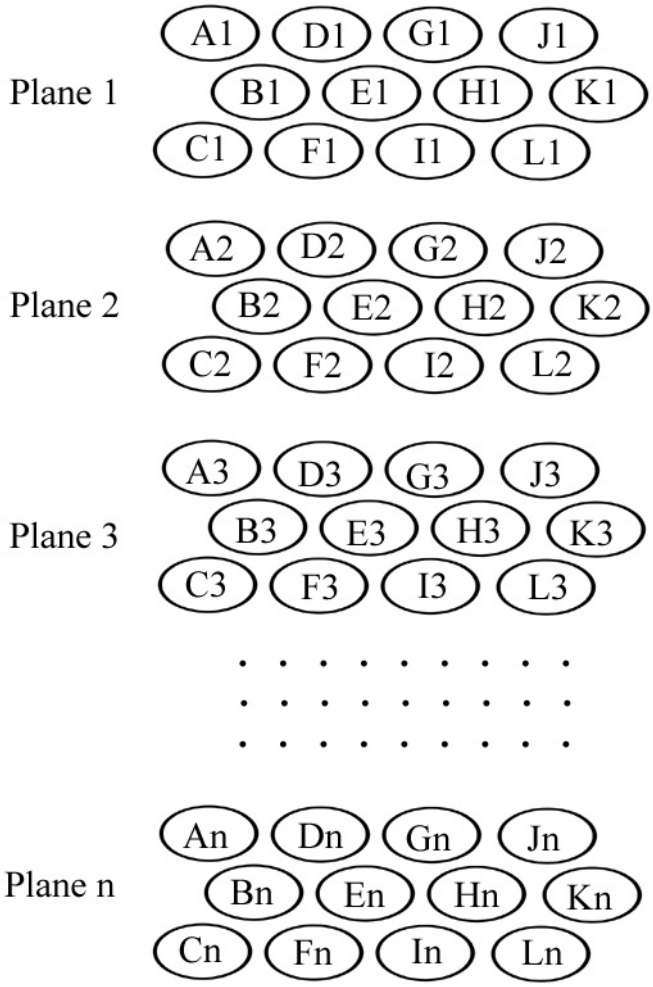


Figure 22. Component planes of a 3 x 4 self-organizing map, composed of n-dimensional vector space, representing a total of 3 x 4 x n components.

Analysis

The PCM data was collected from 17 production lots from a BiCMOS process during five months, and combined with the wafer yield and lot number information. Usually only a small number of the produced wafers are tested for PCM due to customer delivery urgency.

The data consists of 202 measured wafers, each with 5 test dices, accounting for a total of 1010 rows by 63 parameters (61 PCM & wafer yield & the lot number), e.g. transistor threshold and breakdown voltages, thin-film sheet resistances, gate linewidths, leakage currents, etc. The measurements were first checked for missing data and outliers, which were replaced by markers to instruct the SOM software [74] to ignore them. The method of SOM was then applied to reduce the high-dimensional data and create visibility for the parameter dependencies.

The training vectors should ideally be normalized not to give any single parameter plane too much of weight when training the map. However, caution should be used when doing the normalization, as one would have to know some background information about the parameters, which are ranging from nA to μm to V and kohm. For example, the current gain factor (about 500) should probably be considered at least as important as the transistor threshold voltage (about 0.55 V). Other parameters exhibit a similar range variation.

After careful consideration, each parameter was scaled by a simple division computation into the range of –20 to 0, or 0 to +20 depending on the parameter polarity. The yield was scaled to range from 0 to 100 to make it have more emphasis and control over the map convergence. This method is called supervised SOM ([63] p.161). Also, the lot numbers, carried along, were scaled to range from 0 to 0.1 in order to create a low-weighing tag to later allow lot region identification.

Decision about the map size to be used is by no means a simple choice. Reference [75] lists several studies using various map sizes and component plane dimensions. As an example, the number of training vectors used in ref. [76] was 208, while the map size was chosen as 10 x 10 neurons with 8 planes.

Intuitively, a large number of parameter planes can make it difficult for the map to attain independently trained category regions on the different planes, e.g. if the complex parameter space contains several co-dependent parameter planes, where the vectors are forced into the same region because of their dependency of such a parameter that is directing the map formation. Additionally, it is possible that some planes contain passenger nodes, which are not actually contributing to the map region classification.

Here, the SOM should now perform two functions: 1) the map size should be small, and still converge to represent the data set accurately, 2) the map should be large enough to reveal subtle relations between the parameters. While not directly translatable from the previous studies, the map size was chosen as 17 by 22, a total of 374 neurons. It is customary to leave randomly chosen 10% of the training vectors out of the training material, and use them for testing the map modeling performance. The main objective is to provide the semiconductor engineer with the most probable parameter candidates for the low yield, therefore it should be reasonably safe to use all the measurement vectors for training the map, as we are low on samples already. The map was initialized with random values.

After the training of the SOM, the average quantization error of the map per sample vector was found to be 2.72. Several algorithm variations were tested, and the one described in Table 12 procedure was found to result in the best performance. The quantization error is dependent on the map size, the initial values, and the training data. Table 13 lists the results of experimenting done on various sized maps.

Table 12. Algorithm for obtaining the best map (bubble neighborhood, hexagonal topology, linear alpha shrink, random initialization).

Run cycle	Training cycles	Alpha (neighborhood shrink)	Initial radius (neurons)	Average quantization error
1st	0	N/A	N/A	30.247436
2nd	10000	0.9	10	5.057104
3rd	100000	0.3	5	4.257122
4th	100000	0.2	0	2.718484

Table 13. Map size and the average quantization error per sample vector.

Map size (neurons)	Average quantization error
4 x 6 = 24	6.695118
6 x 6 = 26	5.841517
10 x 10 = 100	4.379018
10 x 12 = 120	4.087817
5 x 24 = 120	4.126108
17 x 22 = 374	***2.718484***
20 x 20 = 400	2.658164
10 x 40 = 400	2.706104
33 x 33 = 999	1.324180
10 x 100 = 1000	1.468767
20 x 50 = 1000	1.423114
40 x 40 = 1600	0.866286
100 x 100 = 10000	0.000005

The aim in this study is to use the self-organizing map in classification of PCM parameters & yield, to make it possible to identify yield-affecting factors, which the semiconductor engineer can experiment on and verify in the fab, e.g. to run experiment lots with specific parameter variations without too much of guessing. Therefore, the metrics of the map is chosen to be kept simple. In order to better understand the process parameter value relations, the map planes could be vectorized and run through a new SOM to see which planes become located closely together [77]. This might reveal process steps that cause co-dependence for certain parameters. To find out which parameters have a critical effect on the yield, all 63 map planes were visually inspected and compared to the yield plane Nr. 62.

Figure 23 shows (a) the yield from the plane number 62, (b) NMOS transistor drain current from the plane Nr. 49, (c) aluminum sheet resistance from the plane Nr. 35, (d)

metal layer 1 to metal layer 2 contact resistance from the plane Nr. 38, and (e) lot numbers from the plane Nr. 63.

In Fig. 23 the dark gray areas indicate a small parameter value, and light gray a large value. The yield in Fig. 23(a) is very low in the upper left corner and high in the upper right and lower left regions. The most likely parameter affecting the yield is the NMOS transistor drain current in Fig. 23(b), where the low current is located in the same region as the low yield in Fig. 23(a). Most of the discovered parameters have to do with NMOS transistors, and would need further investigation. The fab uses N-type wafers, and therefore the NMOS transistors have to be placed in a p-well, which process step might introduce additional impurities and cause bias to the operational characteristics of the NMOS transistors when compared to PMOS transistors.

The map plane of aluminum sheet resistance in Fig. 23(c) matches the good yield area, when the resistance value is in the region of intermediate range, i.e. the yield is not at its best if the aluminum sheet resistance is too small or too large. This result would not necessarily have been discovered with the procedure of re-applying the map to automatically categorize the SOM planes [77]. Also, the very low yield area in Fig. 23(a) seems to be related to the very high aluminum sheet resistance area in Fig. 23(c), an inversed relation, not detectable automatically. The metal layer 1 to metal layer 2 contact resistance SOM plane in Fig. 23(d) is shown only for a reference, as one cannot see there any relation to the yield. Fig. 23(e) contains the lot numbers, and interesting enough, the low yield apparently is a problem for the latest production lots, i.e. larger lot number, especially in the upper left corner.

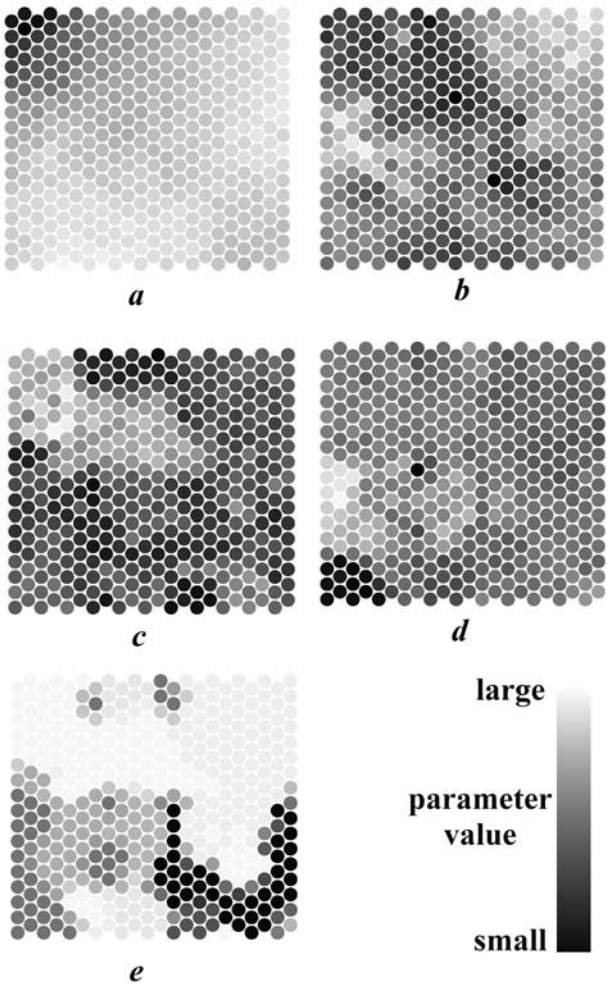


Figure 23. Component planes of the trained 17 x 22 self-organizing map, where dark gray relate to a small parameter value, light gray to a large value.

a Device yield

b NMOS transistor drain current

c Aluminum sheet resistance

d Metal layer 1 to metal layer 2 contact resistance

e Production lot numbers

The results show that the SOM type of neural net can effectively be applied to identify semiconductor process parameter relations. In this case the most likely causes for low yield turned out to be NMOS transistor drain current and aluminum sheet resistance. Supplied with this information the semiconductor engineer can plan lot run tests for performing process parameter variation to verify the findings. The analysis here could have improved by giving the yield more weight in the scaling, so that the lowest yield would have been located in the upper left corner and the highest yield in the lower right corner. Originally this was the situation, but improving the quantization error with a new random initialization, the map convergence was reduced from the viewpoint of yield.

5 Experiments on Compound Semiconductor Components: results and analysis

This section covers the publications I, II, and IV, which all handle compound semiconductors.

Publication I studies the breakdown voltage of GaAs based power varactor diodes. The breakdown should happen at about 40V, but the problem is that many of the diodes do not perform anywhere close to the spec. Varactor diodes are used as capacitors tunable by dc voltage, and GaAs based technology is necessary for high frequency applications. The studied diodes (see Fig. 24 for detailed structure) are fabricated on or near Liquid Encapsulated Czochralski (LEC) cellular dislocation networks in the substrate. The cell structure is known to be rich in As precipitates near the cell walls.

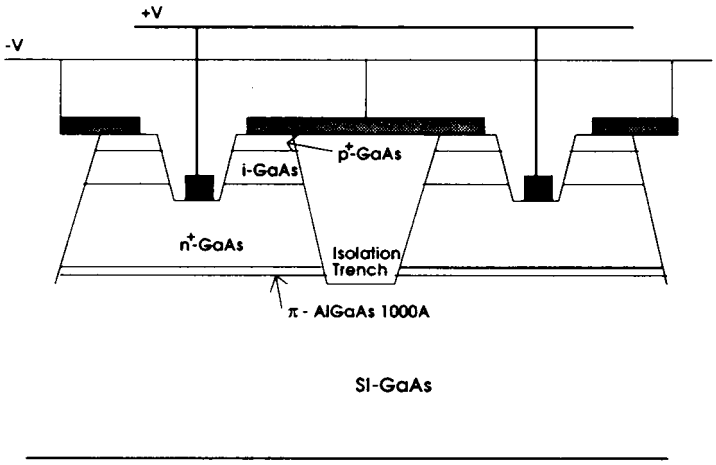


Figure 24. Structure of power varactor diodes in this study

The studied varactor diode stack is shown in Fig. 25. Each diode is sized 6300 μm x 100 μm. The nominal wafer thickness was 600 μm, though 200 μm was removed from the bottom to have better defect visibility, because GaAs is highly absorbent of X-rays. The numbering scheme of the diodes is shown in Fig. 26. Synchrotron X-ray topography is applied to the diode stack. Two geometry modes are used for the analysis.

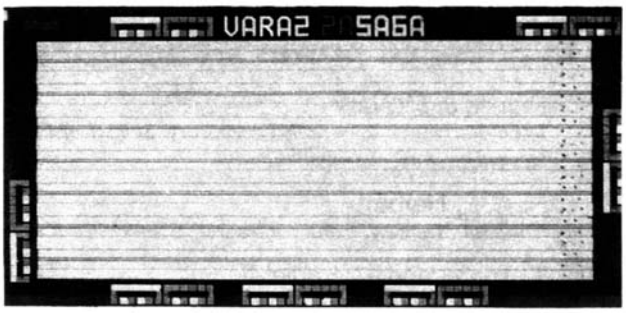


Figure 25. Micrograph of a stack containing 14 diodes.

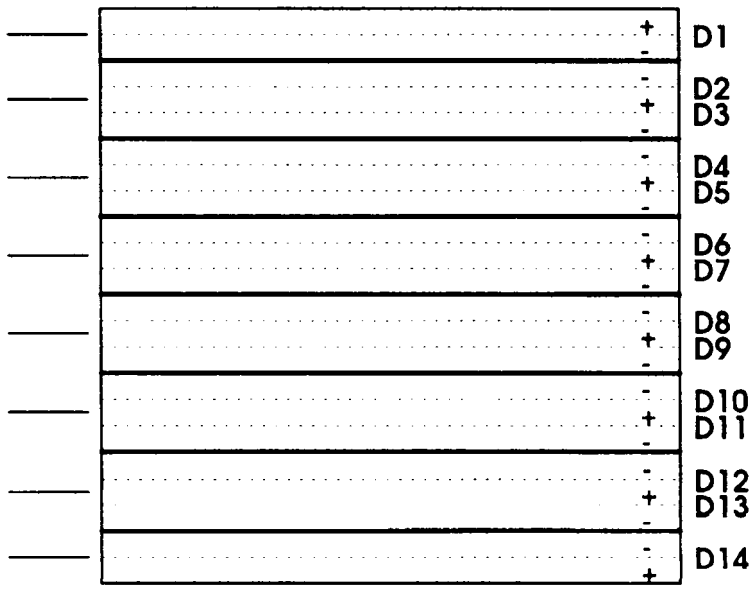


Figure 26. Numbering scheme used for each diode stack. The markers on the left identify the center of each p-n diode stack.

The large-area transmission topograph (geometry was described previously) is shown in Fig. 27. The cells are clearly visible in the image. There is a large dislocation line in an arc from D6 to D2. Also, there is a large concentration of defects and cells covering the diodes D2-D7, and a smaller concentration at D9-D13. From Fig. 28 it is evident that the breakdown voltage is actually better for the diodes D10-D13. The higher dislocation density at D2-D7 seems to correlate to the lower performance breakdown voltage.

Figure 27. Large-area topograph of the diode array. The image size is 3 mm x 3 mm.

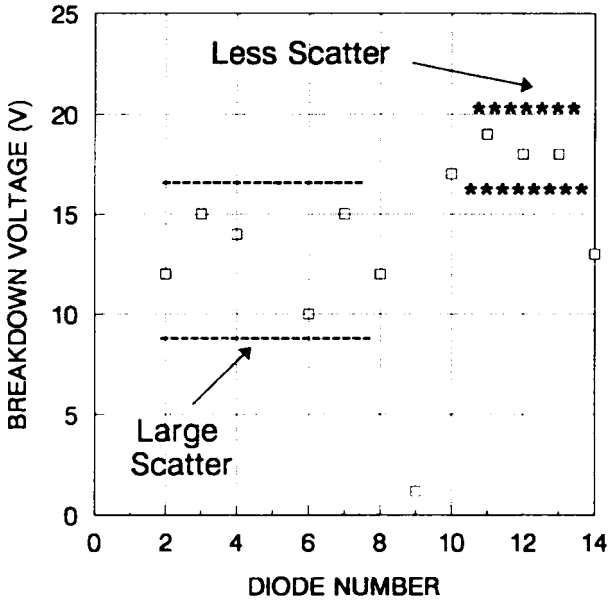


Figure 28. Breakdown voltage performance for a typical diode array.

The section transmission topograph (geometry was described previously) of the diode array is shown in Fig. 29. It is composed of two photographic enlargements, hence the abrupt change in the background darkness. The strain is clearly located in the upper part of the wafer.

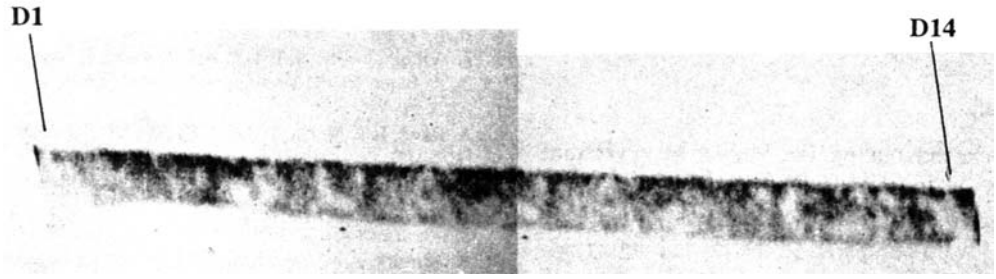


Figure 29. Section topograph of the diode array.

Publication II studies pseudomorpic HEMT's on epitaxial structures grown by low pressure MOVPE. Special attention is paid to the source/gate/drain metallization and the consequential stress generation, and the impact on the substrate of the deposition of the passivation dielectric overlayers. The dielectric overlayers can lead to large regions of piezoelectric charge in the active regions of a device, e.g. stress-induced transistor threshold voltages can shift 500 mV on some occations. They can also cause crystalline defects and dislocations.

Fig. 30 shows the structure of the p-HEMT used in this study, the image is not in scale. We have two sets of devices; HEMT-1 are the devices with source/gate/drain metallization, and another set, which went through Si_3N_4 deposition, shall be called HEMT-2. The schematic electrode configuration of the p-HEMT is shown in Fig. 31.

50nm	n^+ - GaAs cap layer ($4x10^{18} cm^{-3}$ Si)
25nm	$Al_{0.22}$ $Ga_{0.78}$ As gate contact layer (undoped)
	δ - doping ($3.6x10^{12}$ cm^{-2} Si)
3nm	$Al_{0.22}$ $Ga_{0.78}$ As spacer layer (undoped)
14nm	$In_{0.21}$ $Ga_{0.79}$ As channel layer (undoped)
0.5μm	GaAs buffer layer (undoped)
450 μm	SI GaAs SUBSTRATE

Figure 30. Vertical structure of the p-HEMT devices used in the study (not drawn to scale).

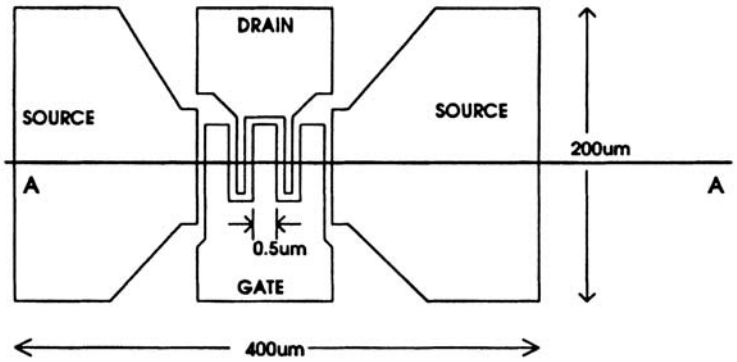
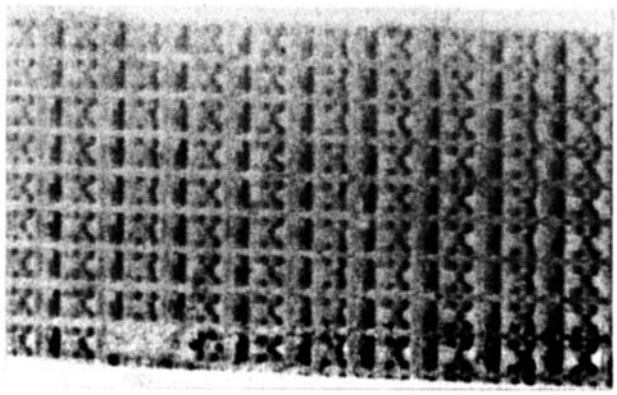


Figure 31. Schematic electrode configuration of the p-HEMT devices.

The large-area topograph of an array of 10 x 9 devices is shown in Fig. 32(a) of the HEMT-1 devices, and in Fig. 32(b) of the HEMT-2 devices. Clearly the strain for HEMT-2 is very strong, and the image in (b) is much more blurred than in (a), where there is no dielectric layer deposited. The arrow A in (b) marks one of the black streaky regions, apparently giving a rise to detrimental defect generation.

Section topographs of Fig. 33 section A-A are shown in Fig. 33(a) for HEMT-1, and Fig. 33(b) for HEMT-2 respectively. The strain is the strongest at the black bump marked as B, denoting the gate/drain region. Depositing a Si_3N_4 layer creates additional random strain and defects for the HEMT-2 array, and is clearly visible in (b) as distorted darkness distribution.

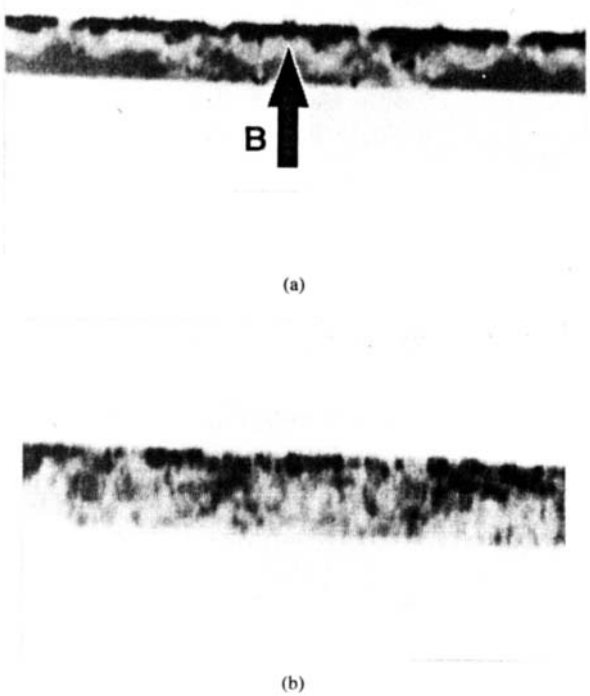
The introduction of severe stresses and defects/dislocations has implications for III-V device electrical performance. The dielectric materials are piezoelectric, and can cause deterioration to the device parameters, e.g. shift the transistor threshold voltages.



(a)

(b)

Figure 32. (a) large-area topograph of the HEMT-1 array with only metallization, and (b) HEMT-2 array with dielectric overlayer deposited.



(a)

(b)

Figure 33. (a) section topograph of the HEMT-1 array with metallization only, and (b) HEMT-2 array with dielectric overlayer deposited.

Publication IV handles failure analysis of ultra-bright LED Arrays under varying degrees of electrical stress was performed. Green (565 nm), Red (660 nm) and Infrared (890 nm) LEDs were subjected to currents between 0 and 1 A and voltages between 0 and 7 V. Using White Beam Synchrotron X-Ray Topography (SXRT) in back reflection large area and section modes, the failure modes of the devices were observed. As the power to each device was increased, a reduction in the definition of device lattice structure due to increased thermal stressing was observed. An increase in strain was witnessed in the devices as they were stressed to the point of near failure. It was noted that at or near failure, the strain fields in the ball-bonded regions of the device became anomalously large (0.08% for the Red LED (GaAs and AlGaAs epitaxial layers grown on a (001) GaAs substrate), 0.19% for the Green LED (nitrogen doped GaP as the active area) and 0.27% for the Infrared LED), as observed via orientational (extinction) contrast on the topographs. This contrast is most likely due to thermally induced damage. Onset of failure took place when the power supplied to each individual LED exceeded 600 mW in the case of the Green LEDs, 500 mW for the Red LEDs and 745 mW for the Infrared LEDs. Surprisingly, this is approximately 25 times greater than the nominal recommended supply for each LED array. This was confirmed by studying the current-voltage curve characteristics of the devices in conjunction with their emission spectra. As the power supplied to the devices was increased a narrowing of the radiative bandgap was witnessed in the Red and Green LEDs; whereas a broadening occurred in the Infrared LED. When complete failure occurred in the samples, it was observed that large lattice deformations of the original device structure took place. Optical micrographs indicated that the structure of the devices remains spatially unaltered although the gold bond wire became detached. This confirmed that the distortion observed in the x-ray topographs is mainly due to severe thermally induced lattice distortion. The induced lattice distortion is greatest for the Red LEDs; the sample appears to possess distinct and completely misorientated sub-grains. Large area and section geometry were both used in back-reflection mode.

The Red and Infrared LED active regions were constructed out of the III-V compound semiconductors GaAs and AlGaAs epitaxial layers grown on a (001) GaAs substrate. The active region of the Green LED was nitrogen doped GaP. The substrate of the device was attached to the IC package bulk using bonding glue.

Using a conventional laboratory power supply, the power supplied to each device was increased until failure occurred. The failure point was defined as the point where a sudden and complete loss in light occurred. Optical emission spectroscopy was also used to observe the failure of these devices via the change in output wavelength as a function of power supplied to the device. Plots of the relative output intensity versus wavelength were recorded.

Figure 34 depicts the failure of the Green (565 nm) LED via large area back reflection topography. Normal device operation (25 mW per device) is illustrated in Figure 34(a), which is a large area back reflection topograph. Figure 34(b) depicts a 3-D topographic image recorded from the reflection after cooling following device failure. In the *a priori* case – Figure 34(a) – the ball bond and accompanying gold wire are observed via absorption (reduced intensity, i.e. white contrast) of x-rays. The increase in intensity along the underside edges of the LED is related to the increase in stress due to the adhesion of the device substrate to the IC package bulk as indicated by the arrow X. Strain due to the metallization layers is present albeit difficult to observe as indicated by arrow Y. It was noticed that as the power supplied to the device was increased, the

consequent temperature rise and increased lattice vibration caused a reduction in the X-ray topographic definition of the strain induced by the metallization layers until failure occurred. Surprisingly, these devices continued to work at powers approximately 25 times greater than their maximum rated working power – 602 mW / device as opposed to 25 mW / device. Once catastrophic failure occurred, the topographic image of the LED became severely warped and distorted around the gold bond. The distortion is due to the build-up of large stresses, which are presumably related to the thermally induced lattice deformation. After failure, the device was allowed to cool. Upon cooling, large residual strain fields due to the thermal stressing remain. The strain due to the device attachment to the IC package bulk, metallization layers and heteroepitaxial interfaces have increased dramatically as arrows X, Y and Z portray respectively in Figure 34(b). Figures 34(a) and 34(b) were recorded from different reflections and hence different dimensions are marked on each image. The vector $\vec{g}$ shows the diffraction direction.

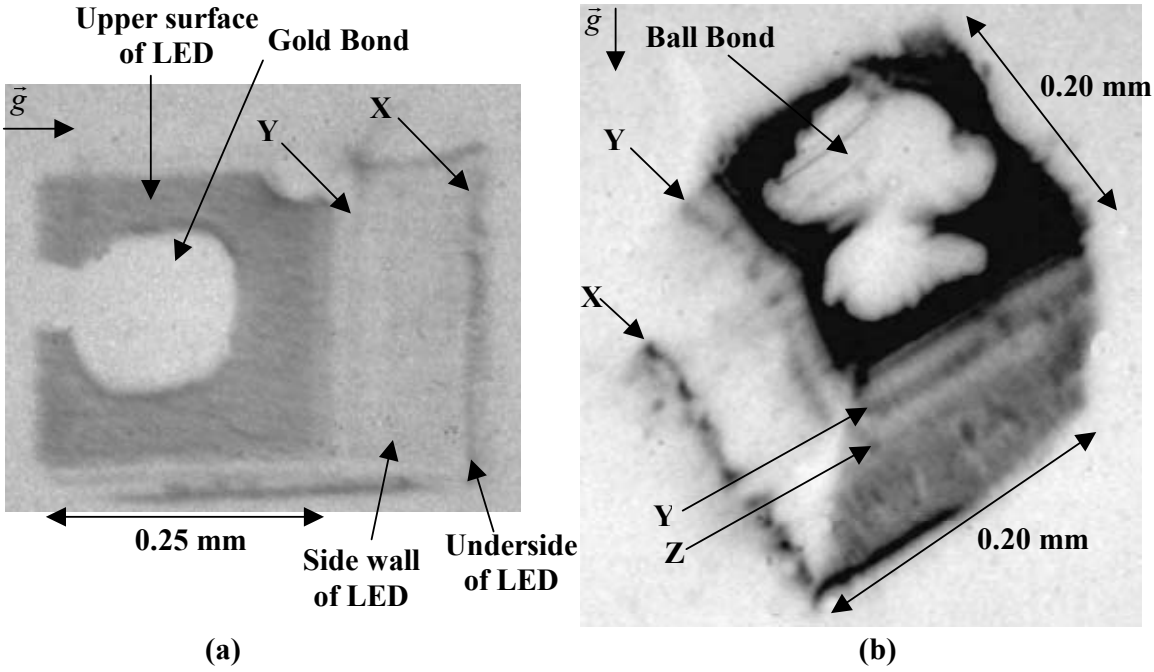


Figure 34. Back-reflection topographs of green LED (565 nm) (a) normal operation (25 mW / device) and (b) after cooling subsequent to failure

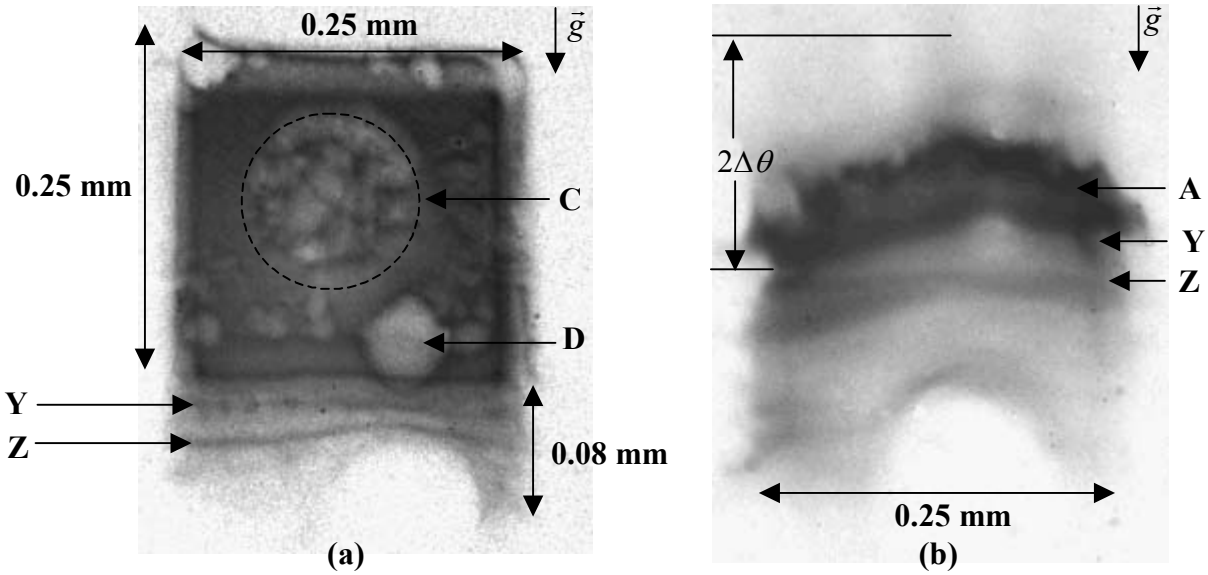


Figure 35. (a) Large-area back reflection topograph and (b) back reflection section topograph of Red (660 nm) LED after cooling subsequent to failure.

In Fig. 35(a) considerable strain fields due to the metallization layers are evident (arrows Y and Z). These lines arise most likely from the interfaces between the heteroepitaxial layers of the diode. Large localized leakage currents around the gold bond may have caused severe thermal lattice vibration and consequent surface damage (arrow D). Large strain fields are present in the active region A of Red LED after failure as conveyed by the back reflection section topograph in Fig. 35(b). Severe lattice deformation has occurred.

Measured optical emission spectra of the recombinative bandgap using Optical Emission Spectroscopy (OES) revealed a narrowing of the bandgap for the Green and Red LEDs as the power to and hence temperature of each device is increased; whereas a broadening occurred for the Infrared LED. Under normal operation the Red LED exhibited a distorted Gaussian spectrum centred at 649 nm. As the power was increased the peak wavelength changed to 741 nm with the introduction of a sidelobe at 715 nm. Conversely, under normal operation, the Green LED demonstrated a peak wavelength at 567 nm with a secondary peak at 561 nm. As the power was increased the presence of the secondary peak receded yielding a distorted Gaussian spectrum centered at 661 nm prior to failure.

The Infrared LED displayed the most unusual spectrum of all. Under normal operation, a dominant peak at 841 nm in concurrence with a tertiary peak at 810 nm was observed. At elevated powers (1.93 W per device) it was observed that the 810 nm peak had moved to 806 nm and dominated the 841 nm peak, which had shifted to 830 nm. This suggests that the high power induced damage is introducing the presence of a defect level within the band structure that provides for alternative radiative recombination paths. The possibility of such a level is not inconceivable considering post failure analysis of the device using back reflection section topography revealed large stresses.

6 Summary and Future Considerations

The yield, failure, and PCM data of compound semiconductors and IC wafer lots were analyzed by using a number of tools. They were synchrotron X-ray topography, etch pit micrographs, Finite Element Method (FEM) for computer strain simulations, and the self-organizing map neural net. Measurement results were extensively analyzed by using correlation and statistical principles.

With the compound semiconductor analysis, synchrotron X-ray topography was applied to the study of GaAs based power varactor diodes. The failures occur in the regions of strong strain shown in the topographs as a very dark area. GaAs is a very absorbent material for X-rays, and synchrotrons are few of the suitable sources for creating sufficient radiation flux to attain reasonable exposure time.

Pseudomorphic HEMT's on epitaxial structures were studied with synchrotron X-ray large-area and section topographs. The used Si_3N_4 overlayer is a piezoelectric material and can cause deterioration to the device parameters, e.g. shift the transistor threshold voltages. The topographs revealed that the overlayer caused the strain field to become heavily distorted.

Synchrotron X-ray topography was applied to the study of the failure of ultra-bright LEDs under varying degrees of electrical stress. With LEDs it was observed that the increased thermal load caused an increase in strain around the ball bond region of the devices as they are stressed to the point of near failure. When complete failure occurred in the samples, it was observed that large lattice deformations of the original device structure took place. Optical emission spectroscopy demonstrated a shift of the dominant peak towards long wavelengths for the Green and Red LEDs as applied power is increased.

The FEM-analysis showed that the growing of an oxide layer on top of a silicon layer creates strain and strain gradients.

The main results of the studies on the integrated circuits, state that wafer surface strain gradient and good device functionality have positive correlation. This relationship may reflect a direct dependence between stronger diffracted X-ray intensity and better crystal quality, or the relationship may be indirect, e.g. stronger strain in the silicon and oxide interface, forming trap states being able to bind alkali ions (Na+, K+), which are accumulated into the wafer surface layers from the residues of various process chemicals. There is also some indication from the etch pit micrographic analysis that the yield improves with higher precipitates concentration, which would need further investigation to justify the finding.

The SOM type of neural net can effectively be applied to identify semiconductor process parameter relations. In this case the most likely causes for low yield turned out to be NMOS transistor drain current and aluminum sheet resistance. The SOM could be utilized when transferring a process from one fab to another to speed up the process qualification by identifying the process parameters requiring attention. The SOM is especially well suited for solving process problems for IC's in pre-production stage, because there still exist process problems, and already sufficiently data for the analysis. Even though the SOM has not yet been widely adopted for everyday use in the semiconductor industry, this practical case study shows that the method is extremely efficient for analyzing certain semiconductor problems.

Future Considerations

Currently, most of the fabs are moving to single-wafer processing for the advantages of reduced risks, improved cycle times and shorter turnaround time. But as devices shrink, the technical reasons drive the tendency towards the Rapid Thermal Processing (RTP). RTP (single-wafer-at-a-time) thermal processing scheme increases the thermal variation when compared to the one-lot-at-a-time thermal processing scheme. This makes it more difficult to apply the previously described analysis methods for RTP wafers.

One of the latest developments is that in addition to having PCM test dice on wafers, there are specially assigned wafers in a process lot, allocated solely for testing purposes. They do not contain any production dice, only electrical test structures. This wafer-level testing allows the electrical testing of very detailed process events. Integrated circuit testing is becoming more complex and specialized. The number of transistors on a die is still increasing according to the Moore's law, and the used clock and operating frequencies are going up. This is becoming a serious challenge for the IC testing community.

References

[1] T.Tuomi, K.Naukkarinen, P.Rabe, *Phys stat. Solidi (a)* **25** (1974) 93.

[2] T.Tuomi, M.Tuominen, E.Prieur, J.Partanen, J.Lahtinen, J.Laakkonen, *J. Electrochem. Soc.* **142** (1995) 1699.

[3] J.Partanen, T.Tuomi, D.-Y.Yang, H.-G.Lee, O.H.Kim, S.Hahn, *J. Electrochem. Soc.* **139** (1992) 1431.

[4] J.A. Cunningham, *IEEE Trans. on Semicond. Manufacturing* **3** (1990) 60-71.

[5] Nato Advanced Study Institute on Characterization of Crystal Growth Defects by X-Ray Methods (eds. B.K.Tanner and D.K.Bowen), *Plenum Press* (1980)

[6] N.I.Puzanov and A.M.Eidenzon, The effect of thermal history during crystal growth on oxygen precipitation in Czochralski-grown silicon, *Semiconductor Science and Technology* **7** (1992) 406-413

[7] J.P. Joly and V.Robert, Influence of the first thermal cycles of an IC process on oxygen precipitation in CZ silicon wafers: a detailed analysis, *Semiconductor Science and Technology* **9** (1994) 105-111

[8] G.Kissinger, D.Gräf, U.Lambert, T.Grabolla and H.Richter, Key influence of the thermal history on process-induced defects in Czochralski silicon wafers, *Semiconductor Science and Technology* **12** (1997) 933-937

[9] T.Müller, G.Kissinger, A.C.Benkitsch, O.Brand, and H.Baltes, Assessment of Silicon Wafer Material for the Fabrication of Integrated Circuit Sensors, 1604 *Journal of The Electrochemical Society* 147 (4) 1604-1611 (2000)

[10] G.Kissinger, T.Grabolla, G.Morgenstern, H.Richter, D.Gräf, J.Vanhellemont, U.Lambert, and W.von Ammon, Grown-in Oxide Precipitate Nuclei in Czochralski Silicon Substrates and Their Role in Device Processing, *Journal of The Electrochemical Society* 146 (5) 1971-1976 (1999) 1971

[11] A.A.Istratov, H.Hieslmair, E.R.Weber, "Advanced Gettering Techniques in ULSI Technology", Materials Research Society: MRS Bulletin, June 2000, pp. 33-38.

[12] S.Hahn, C.Y.Tung, J.Lee, J.Partanen, T.Tuomi, Defect Control in Semiconductors*, Elsevier* 1990, p.627-631.

[13] B.O.Kolbesen, H.P.Strunk, VLSI Electronics: Microstructure Science*, Academic Press* **12** (1985) 143.

[14] G.A.Rozgonyi, C.W.Pearce, *Appl. Phys. Lett.* **31** (1977) 343.

[15] T.Tuomi, M.Tilli, O.Anttila, *Appl. Phys. Lett.* **57** (1985) 1384.

[16] T.Tuomi, S.Hahn, M.Tilli, C.-C.D.Wong, O.Borland, *Mat. Res. Soc. Symp. Proc.* **71** (1986) 47.

[17] W.C. Dash, *J. Appl. Phys.* **27** (1956) 1193

[18] E. Sirtl and Annemarie Adler, *Z. Metallkunde* **52** (1961) 529

[19] H. Seiter, in "Semiconductor Silicon 1977", ed. H. Huff, E. Sirtl; Electrochem. Soc. Proc. Series, p. 187

[20] Margarete Wright Jenkins, *J. Electrochem. Soc.* **124** (1977) 757

[21] F. Secco d'Aragona, *J. Electrochem. Soc.* **119** (1972) 948

[22] K. H. Yang, J. Electrochem. Soc., **131** (1984) 1140

[23] M.Futagami, *J. Appl. Phys.* **52** (1981) 5575.

[24] M.Kayambaki, K.Tsagaraki, V.Cimalla, K.Zekentes, R.Yakimova, Journal of the Electrochemical Society, **147** (7) 2744-2748 (2000)

[25] Pei, Z.J, and Ferreira, P.M., 1999, "An experimental investigation of rotary ultrasonic face milling," International Journal of Machine Tools and Manufacture, Vol. 39, No. 8, pp. 1327-1344

[26] B.K.Taner, X-Ray Diffraction Topography, Pergamon Press 1976

[27] D.K.Bowen and B.K.Tanner, High Resolution X-ray Diffractometry and Topography, Taylor & Francis 1998

[28] Applications of Synchrotron Radiation, Ed. H.Winick, D.Xian, M.Ye, and T.Huang, Gordon and Beach Science publishers 1989

[29] D.K. Bowen in Applications of Synchrotron Radiation (eds. H.Winick, D.Xian, M.-H. Ye and T. Huang), *Gordon and Breach Science Publishers* (1989) 77-89

[30] A.Authier, Dynamical Theory of X-Ray Diffraction, *Oxford University Press,* New York, 2001, p.527.

[31] B.E.Warren, *X*-Ray Diffraction*, Dover publications of Addison-Wesley,* 1969, p.331-333.

[32] M.Karilahti, T.Tuomi, M.Taskinen, J.Tulkki, H.Lipsanen, P.NcNally, *Il Nuovo Cimento* **19** (1997) 181.

[33] Z.H.Kalman, S.Weissman, *J.Appl.Cryst.* **12** (1979) 209-220

[34] R.Rantamäki, T.Tuomi, Z.R.Zytkiewicz, P.J.McNally, and A.N.Danilewsky, Comparative analysis of synchrotron X-ray transmission and reflection topography techniques applied to epitaxial laterally overgrown GaAs layers, Journal of X-ray Sc. and Tech. 8 (2000) 277-288

[35] E.Prieur, T.Tuomi, J.Partanen, E.Yli-Juuti, and M.Tilli, J. Cryst. Growth, 132 (1993) 599-605

[36] T.Tuomi, M.Juvonen, R.Rantamäki, K.Hjelt, M.Pavdaz, S.Nenonen, M-A.Gagliardi, P.J.McNally, A.N.Danilewsky, E.Prieur, M.Taskinen, M.Tuominen, Synchrotron X-ray topographic study of dislocations in GaAs detector crystals grown by vertical gradient freeze technique, Materials Research Society Symposia Proceedings 487 (1998) 459-464

[37] J-F.Pétroff, M.Sauvage, P.Riglet, H.Hashizume, Phil. Mag. A 42 (1980) 319-338

[38] J.Partanen and T.Tuomi, An experimental and theoretical study of Pendellösung fringes in sychrotron section topographs of silicon wafers, J. X-ray Sc. and Tech. 2 (1990) 165-171

[39] S.L.Flegler, J.W.Heckman, K.L.Klomparens, Scanning and Transmission Electron Microscopy: An Introduction, Oxford University Press; Reprint edition 1997

[40] D.B.Williams and C.B.Carter, Transmission Electron Microscopy: A Textbook for Materials Science, Kluwer Academic/Plenum Publishers 1996

[41] M.J.Weber (Ed.), Selected Papers on Phosphors, Light Emitting Diodes, and Scintillators: Applications of Photoluminescence, Cathodoluminescence, Electroluminescence, and Radioluminescence (Spie Milestone Series, Vol 151), Society of Photo-optical Instrumentation Engineers 1998

[42] K.D.Mielenz, Optical Radiation Measurements: Measurement of Photoluminescence , Academic Press 1982

[43] S.Perkowitz, Optical Characterization of Semiconductors: Infrared, Raman, and Photoluminescence Spectroscopy (Techniques of Physics, No 15), Academic Press 1993

[44] G.Turrell and J.Corset, Raman Microscopy: Developments and Applications, Academic Press 1996

[45] Y. Toda, S. Shinomori, K. Suzuki and Y. Arakawa // Appl. Phys. Lett. 73 (1998) 517.

[46] G. Wurtz, R. Bachelot and P. Royer // Eur. Phys. J. AP 5 (1999) 269.

[47] D.Bonnel, Scanning Probe Microscopy and Spectroscopy: Theory, Techniques, and Applications, John Wiley & Sons, 2nd ed. 2000

[48] A.Wiesenganger, Scanning Probe Microscopy and Spectroscopy : Methods and Applications, Cambridge University Press 1995

[49] Test Method F1239-94, Standard Test Methods for Oxygen Procipitation Characterization of Silicon Wafers by Measurement of Interstitial Oxygen Reduction, *American Society for Testing and Materials*, 1994.

[50] P.J.McNally, R.Rantamäki, T.Tuomi, A.N.Danilewsky, D.Lowney, J.C.Curley, P.A.F.Herbert, Mapping of Mechanical, Thermomechanical and Wire-Nond Strain Fields in Packaged Si Integrated Circuits Using Synchrotron White Beam X-Ray Topography, *IEEE Trans. On Comp. and Packaging Tech,* **24** (2001) 76-83

[51] R.Rantamäki, T.Tuomi, Z.R.Zytkiewicz, D.Dobosz, P.J.McNally, *J.Phys. D: Appl. Phys.* **32** (1999) A114-A118.

[52] J.Miltat, Characterization of Crystal Growth Defects, Eds. B.K.Tanner, D.K.Bowen, *Plenum Press,* New York and London, 1979, p.401-420

[53] T.Tuomi, Synchrotron X-Ray Topography of Electronic Materials, J. Synchrotron Rad. 9 (2002) 174-178

[54] D.C.Montgomery, Introduction to Statistical Quality Control, John Wiley & Sons 2000

[55] F.W.Brefogle III, Implementing Six Sigma: Smarter Solutions Using Statistical Methods, Wiley-Interscience 1999

[56] P.R.Shephard, Integrated Circuit: Design, Fabrication, and Test, McGraw-Hill Professional 1996

[57] P.K.Lala, Digital Circuit Testing and Testability, Academic Press 1997

[58] Mike Tien-Chien Lee, High-Level Test Synthesis of Digital VLSI Circuits, Artech House 1997

[59] B.D.Cullity, Elements of X-Ray Diffraction, *Addison-Wesley*, Reading, 1956, p.174.

[60] J.Miltat, Lecture Notes in Physics 112, Imaging Processes and Coherence in Physics, Proceedings, Les Houches 1979*, Springer-Verlag*, Berlin, Heidelberg, New York 1980 p.505.

[61] J.H.Matlock, Material Defect Factors Affecting MOS Device Performance, Silicon Processing, *ASTM STP 804, D.C.Gupta, Ed., American Society for Testing and Materials,* 1983, p.332-361.

[62] T.Shimura, H.Sensui, M.Umeno, Effects of the substrate crystals upon the structure of thermal oxide layers on Silicon, *Crystal Research and Technology* **33** issue 4 (1998) 637-642

[63] T.Kohonen, Self-organizing maps, Springer 1995, Berlin. (Second Extended Edition 1997).

[64] A.A.Ilumoka, A modular neural network approach to microelectronic circuit yield optimization. Microelectron. Reliab., 38 (1998) 571-580

[65] R.S.Collica, J.P.Card, W.Martin, SRAM bitmap shape recognition and sorting using neural networks. IEEE Trans. on Semiconductor Manuf., 8 (1995) 326-332.

[66] F-E.Chen, S-F.Liu, A neural-network approach to recognize defect spatial pattern in semiconductor fabrication. IEEE Trans. on Semiconductor Manuf., 13 (2000) 366-373.

[67] T.Stützle, A neural network approach to quality control charts. Proceedings of the International Workshop on Artificial Neural Networks (IWANN'95), Torremolinos, Spain. In: Mira J, Sandoval F, (Eds.), Lecture Notes in Computer Science Vol. 930, Springer Verlag, pp.1135-1141, 1995.

[68] E.A.Rietman, E.R.Lory, Use of neural networks in modeling semiconductor manufacturing processes: An Example for Plasma Etch Modeling. IEEE Trans. on Semiconductor Manuf., 6 (1993) 343-347.

[69] C.Bose, H.Lord, Neural network models in wafer fabrication. SPIE Proc. Applications of Artificial Neural Networks, 1965 (1993) 521-530.

[70] K.M.Marks, K.Goser, Analysis of VLSI process data based on self-organizing feature maps. Proceedings of Neuro-Nimes, France 15-17 Nov 1988, pp. 337-348.

[71] M.Gardner, J.Bieker, Data mining solves tough semiconductor manufacturing problems. KDD 2000 Boston, (2000) 376-383

[72] L.Ludwig, U.Epperlein, H.H.Kuge, P.Federl, B.Koppenhöfer, W.Rosenstiel, Classification of 'fingerprints' of process control monitoring-data with self-organizing maps. Proceedings of EANN '97, Stockholm, Sweden, pp. 107-111

[73] L.Ludwig, E.Pelz, M.Kessler, W.Sinderhauf, B.Koppenhoefer, W.Rosenstiel, Prediction of functional yield of chips in semiconductor industry applications. Proceedings of EANN '98, Gibraltar, UK, pp. 157-161, Turku, Finland 1998

[74] SOM_PAK software, SOM Programming Team of the Helsinki University of Technology, Laboratory of Computer and Information Science, ftp://www.cis.hut.fi/pub/som_pak/

[75] G.Myklebust, J.G.Solheim, Neural Networks, 1995, Proceedings., IEEE International Conference on., Vol. 2, 1995, pp.1054-1059.

[76] X.Luo, C.Singh, A.D.Patton, Loss-of-load state identification using self-organizing map, Power Engineering Society Summer Meeting, 1999. IEEE , Volume: 2 , 1999, pp. 670-675.

[77] J.Vesanto, J.Ahola, Hunting for correlations in data using the self-organizing map. International ICSC Symposium on Advances in Intelligent Data Analysis, Proc. of International (ICSC) Congress on Computational Intelligence Methods and Applications (CIMA'99), Rochester, New York, USA, June 22—25, ICSC Academic Press 1999, pp. 279-285