StatCom with Capacitive Energy Storage for Compensation of Cyclic Loads

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***Abstract*—Pulsating power consumption of a cyclic load may cause considerable disturbances in the voltage at the connection point. A StatCom can be employed to maintain the bus voltage level. With the integration of energy storage to the StatCom, the power quality at the connection point can be further improved by the additional active power compensation capability. This paper studies the control strategy for a StatCom with capacitive energy storage for compensation of a cyclic load. Simulations verify the proposed control scheme and show that both the phase jump and magnitude deviation of the bus voltage can be reduced by means of reactive and active power compensation.**

***Index Terms*—Active power compensation, energy storage, phase jump, StatCom, voltage source converter, VSC.**

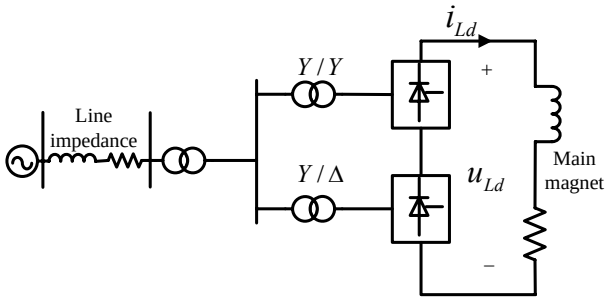

Fig. 1. Load model

I. Introduction

STatic synchronous compensators (StatComs) are widely used in power systems to provide voltage support by supplying reactive power. Integration of energy storage into the converter dc side makes it possible for a StatCom to provide also active power support to the network. Investigations have shown enhanced performance, regarding power oscillation damping [1] [2] and voltage sag mitigation [3] [4], by the integration of energy storage into Voltage Source Converters (VSC). Studies have also shown that active power compensation can mitigate disturbances related to phase jumps in a weak transmission system [5].

A particle accelerator is a typical cyclic load consuming pulsating reactive and active power with varying power factor. Fast magnetization and demagnetization of the main magnets require short rise and fall times of the power during each power cycle. The pulsating load power will create large fluctuations in the bus voltage at the connection point if there is no external voltage support device connected. In order to mitigate the voltage fluctuation, fast reactive power compensation is required. Studies in [6] have shown that, as a possibility, a Static Var Compensator (SVC) can serve this purpose. The reactive power can be almost fully compensated by the SVC, whereas the pulsating active power will be supplied by the network.

This work investigates the possible use of a StatCom with energy storage to improve the power quality at the point of common coupling (PCC) where the cyclic load is connected. A control strategy for StatComs with capacitive energy storage is proposed. Simulations have been performed with the power system simulation software PSCAD/EMTDC. The investigation shows that the phase jump and magnitude fluctuation in the PCC voltage can be reduced significantly by compensation of both the active and the reactive power.

A similar study has been carried out by Dragan Jovcic and Karsten Kahle [7]. A different control strategy is, however, proposed for compensation of particle accelerator load. In that study, the measured load power is taken as a feed-forward for ac voltage control, which in turn gives the d component of the converter reference voltage. Meanwhile, the load active power is controlled in an outer loop, delivering the reference dc voltage for the inner dc voltage control loop, which gives the q component of the converter reference voltage. Although different control approaches are utilized in these two studies, the results are in good agreement.

II. Load Model in PSCAD

The cyclic load simulated in PSCAD is a model of a particle accelerator main magnet supplied from a 12-pulse thyristor converter, as shown in Fig. 1. The accelerator consumes cyclic active and reactive power with a period of 2 seconds as shown in Fig. 2. Fast magnetization of the main magnet requires a short rise time of the load current (e.g., 650 ms). When the acceleration is finished, the main magnet should be demagnetized quickly, requiring a short fall time of the current (e.g., 550 ms). The load current is depicted in Fig 3.

The control system of the cyclic load implemented in PSCAD is shown in Fig 4. The outer loop controls the load current and gives the reference of the thyristor converter output dc voltage. The inner load voltage control loop controls the converter output voltage and delivers the command of the converter firing angle α.

This work is supported by the ELEKTRA research program, which is administered by ELFORSK AB, SE-101 53 Stockholm, Sweden.

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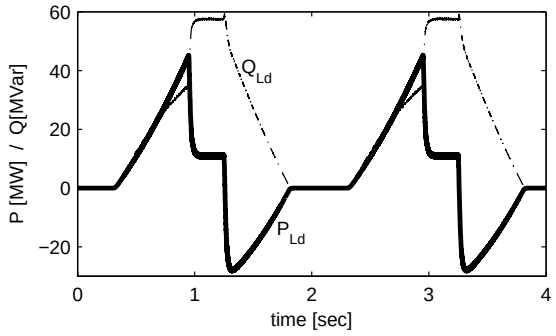

Fig. 2. Pulsating load power

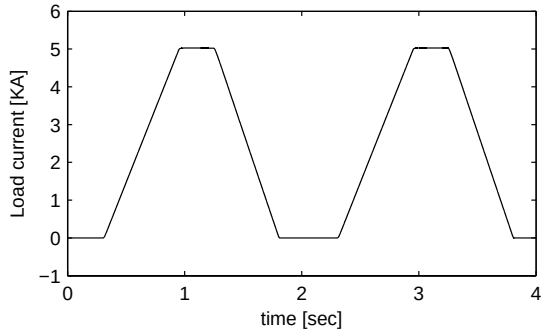

Fig. 3. Load current

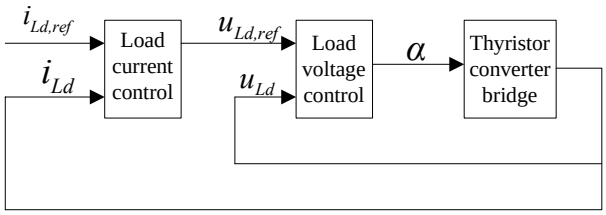

Fig. 4. Cyclic load control system

III. Converter Control

The VSC is connected to the PCC via a phase reactor, which has an inductance L_v and a resistance r_v, as shown in Fig. 5. The control system, which is depicted in the lower part of Fig. 5, consists of two loops. The inner loop employs deadbeat current control combined with a flux modulation scheme as suggested in [8]. The bus flux ψ_B is measured and resolved into a positive sequence, a negative sequence, and an offset component using the low-pass filter method described in [9], with a Phase Locked Loop (PLL) operating on the positive sequence component. The PLL operates in such a way that the d axis aligns with the bus flux vector in the rotating dq plane. The converter current is also separated into the same three components using the angle from the PLL. The deadbeat current control loop calculates the flux change for next sampling interval that is required to get the desired current. In calculation of the flux change, the bus flux with all components is used as a feed-forward signal. Then the flux modulator block generates the switching patterns that will deliver the required flux change in the upcoming

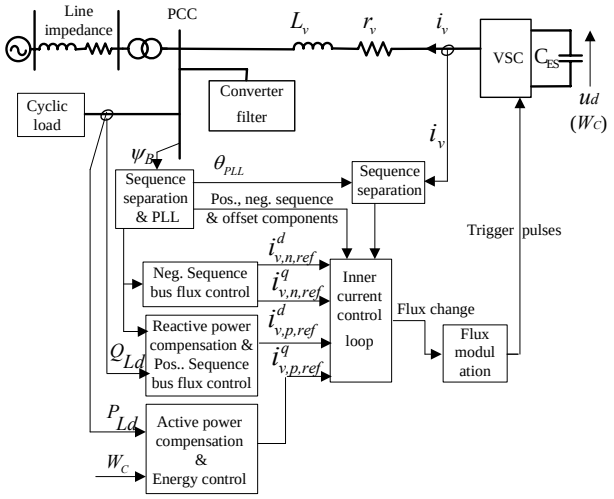

Fig. 5. System overview

sampling interval. The inner current control is implemented in the rotating dq reference frame (defined by the PLL). As all the controlled current components are dc quantities, there will be no steady-state tracking errors.

The references for the converter current components are given by the outer control loop. For the positive sequence, the active current (q component) reference is given by the dc voltage controller (here energy W_C is controlled instead) together with the active load power compensation block. The controller of the PCC flux magnitude together with the reactive load power compensation block provides the reactive current reference. The references for the negative sequence current (d and q components) are given by the corresponding negative sequence bus flux controller (d and q components). The references for the offset components of the converter current are set to zero as they are desired. All the controllers utilized in the outer control loop are of PI (proportional-integral) type. The load power compensation scheme will be described in next section.

IV. Compensation of the Cyclic Load

A. Reactive power compensation

The aim of reactive power compensation is to achieve a fast voltage control. For the general function of the StatCom, i.e., providing reactive power to the network to maintain the bus voltage level, the converter can be controlled only by the bus flux controller. However, the bus flux PI controller takes action only when bus flux deviations have been detected; and its control speed is limited. On the other hand, the load reactive power keeps changing during each load cycle. Hence, even though the bus voltage deviation can be controlled within a small range, the duration of the deviation can be quite long (85% of the load cycle as observed from the simulations). In order to obtain a faster voltage control, the pulsating reactive power should be compensated directly. The measured reactive power Q_{Ld} of the load can be taken as a feed-forward to command the required current and thus reactive power Q_v from the converter.

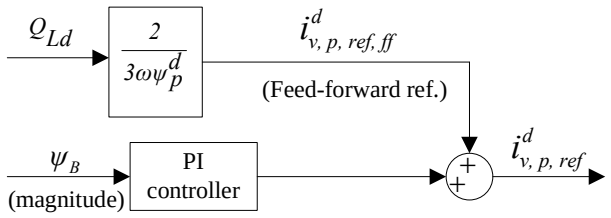

Fig. 6. Reactive power compensation and flux control

The reactive power provided by the converter is related to the converter current as shown in (1):

$$Q_v = \frac{3}{2}\omega(\psi_p^d i_{v,p}^d + \psi_p^q i_{v,p}^q) \tag{1}$$

where ψ_p^d and ψ_p^q are positive sequence dq components of the bus flux, $i_{v,p}^d$ and $i_{v,p}^q$ are the positive sequence components of the converter reactive and active current, and ω is the angular frequency of the bus flux.

Since the PLL locks on the positive sequence of the bus flux, ψ_p^q is very close to zero such that the converter reactive power can be approximated as:

$$Q_v = \frac{3}{2}\omega\psi_p^d i_{v,p}^d \tag{2}$$

Therefore, to directly compensate for the load reactive power, the required reactive current $i^d_{v,p,ref,ff}$, given in (3), should be added into the reference of the converter positive sequence reactive current.

$$i^d_{v,p,ref,ff} = \frac{2Q_{Ld}}{3\omega\psi_p^d} \tag{3}$$

Fig. 6 shows the reactive compensation and positive sequence flux magnitude control scheme.

B. Active power compensation

Although the voltage magnitude disturbance at the PCC is mainly caused by the pulsating reactive power, the active load power also plays a role. In addition to the magnitude disturbance, the pulsating active power also creates phase jumps in the voltage at the PCC, which might degrade the performance of other loads, especially phase sensitive loads, connected at the same point.

In order to mitigate the disturbances introduced by the pulsating active load, active power compensation can be utilized if energy storage devices are connected on the dc side of the converter. In this study, the energy storage device is supposed to be a large capacitor bank. The pulsating active power will be mainly exchanged between the cyclic load and the converter, while the network only needs to supply the average active power to the load. The active power compensation and energy control scheme is depicted in Fig. 7.

The active power that flows from the converter to the network is determined approximately by the converter current as in (4):

$$P_v = \frac{3}{2}\omega(\psi_p^d i_{v,p}^q - \psi_p^q i_{v,p}^d) \tag{4}$$

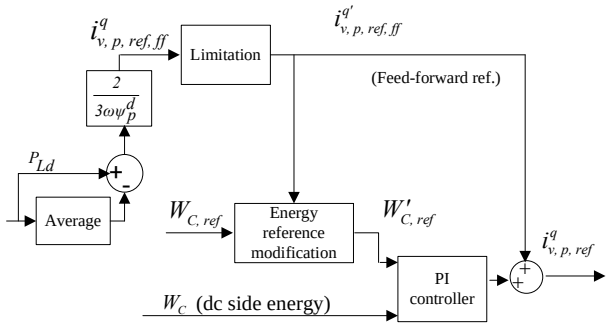

Fig. 7. Active power compensation and energy control

Since the PLL locks on the positive sequence component of the bus flux, ψ_p^q is very close to zero. Hence, the converter active power can be approximated as:

$$P_v = \frac{3}{2}\omega\psi_p^d i_{v,p}^q \tag{5}$$

To compensate for the pulsating part of the load active power P_{Ld}, the feed-forward converter active current reference is then given as:

$$i^q_{v,p,ref,ff} = \frac{2(P_{Ld} - P_{Ld,av})}{3\omega\psi_p^d} \tag{6}$$

where $P_{Ld,av}$ is the average active power of the load.

Since the energy that can be provided or absorbed by the capacitor bank is limited within a certain range, limitations must also be set on this calculated feed-forward reference active current of the converter.

When the feed-forward control commands active current from the converter, the energy stored in the capacitor bank will change accordingly, which in turn will cause the energy controller to react in a way counteracting the feed-forward control. For example, the feed-forward control commands a positive converter current (flowing out of the converter) when the load consumes active power. The converter then starts supplying active power immediately, which results in a drop in the stored energy. As soon as the energy controller detects the energy drop, a negative active converter current is ordered to try to keep the energy at the reference value. It should be noted that the feed-forward control is much faster than the energy controller because of the deadbeat control in the inner current control loop. The conflict between these two controls may be settled in favor of the feed-forward control since active power compensation is desired. The higher priority of the feed-forward control is kept by modifying the energy controller reference $W_{C,ref}$ into $W^{'}_{C,ref}$. A detailed description of the blocks 'Limitation' and 'Energy reference modification' is given below.

1) Limitation on the Feed Forward Current: Recognizing that only when the dc voltage is within the safe operation range the converter can provide or absorb active power, the feed forward reference current should be modified into $i^{q'}_{v,p,ref,ff}$ based on the energy stored on the dc side. A comparator can be employed to set the feed-forward reference to zero when the dc side stored energy is out of the safe operation range.

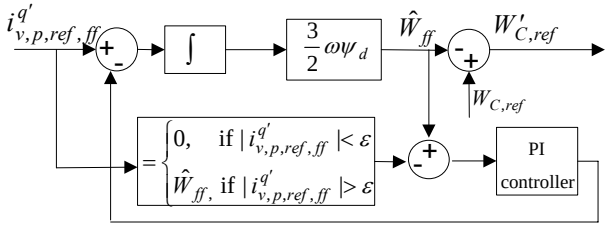

Fig. 8. Energy reference modification

TABLE I
SPECIFICATIONS OF THE SIMULATION SYSTEM[1]

Transformer primary side voltage	400 kV; line-line, rms
Transformer secondary side voltage	17.32 kV; line-line, rms
Converter rating	50 MVA
Filter capacitors	19 MVar
Lumped line impedance	5.5 mH (0.7pu)
Phase reactor	2.4 mH (0.15pu)
dc side capacitor	9376 μF
dc voltage	Maximum: 66 kV (4.7pu)
	Steady state: 33.9 kV (2.4pu)
	Minimum: 33.9 kV (2.4pu)
dc side energy	Maximum: 20.4MJ, $\tau = 0.408s$
	Steady state: 5.4MJ, $\tau = 0.108s$
	Minimum: 5.4MJ, $\tau = 0.108s$
VSC switching frequency	1350 HZ

2) Modification of the Energy Reference: As stated above, a PI energy controller is utilized to control the dc-side voltage and thus to control the energy for general purpose Var compensation. In case active power compensation is desired, a relatively large energy variation is inevitable. The reference for the energy controller should be modified as shown in (7):

$$W'_{C,ref} = W_{C,ref} - \hat{W}_{ff} \tag{7}$$

where $\hat{W}_{ff} = \int \frac{3}{2}\omega\psi^d_p i^{q'}_{v,p,ref,ff} dt$ is the estimated energy that the feed-forward control will take from the converter.

As indicated by (7), a mechanism is necessary to bring the energy reference back to its steady state, i.e., to bring $\hat{W}_{ff}$ back to zero at steady state, as shown in Fig. 8.

Obviously, the PI controller used to bring $\hat{W}_{ff}$ back to zero is active only when the feed-forward reference current is within a band of $\pm\epsilon$. Here ϵ is the threshold value to enable the active power compensation. As long as the active power compensation is in force, the input to this PI controller is zero.

V. SIMULATION RESULTS

Simulations have been performed in PSCAD to verify the proposed compensation strategy. The simulation system configuration is as shown in the upper part of Fig. 5. The specifications of the system are listed in Table I. The converter rating used is 50 MVA and the capacitors used for the converter filter provide additional 19 MVA reactive power.

[1]The specification of dc voltage rating and dc capacitor size in this table is just an example. No optimization has been done in this work.

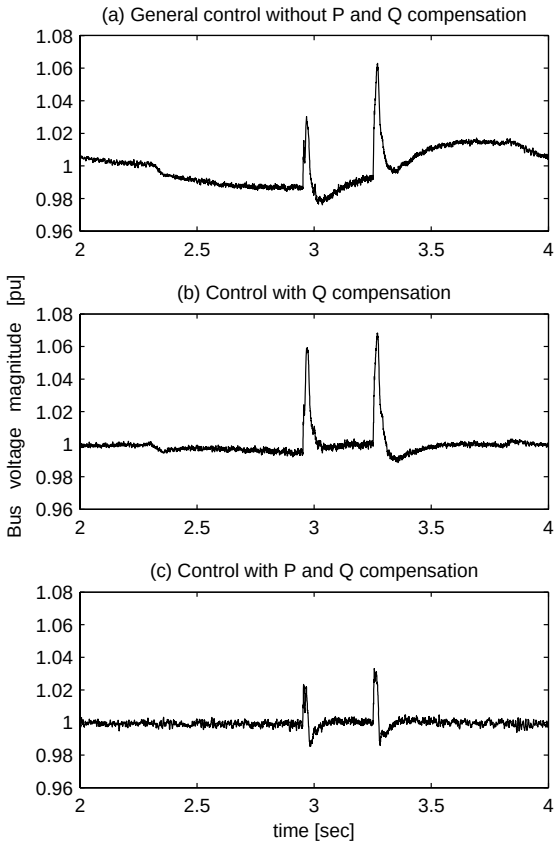

Fig. 9. Bus voltage magnitude

Since the power quality at the PCC is of great concern, the bus voltage was measured and the amplitude and the phase angle with respect to the infinite bus were extracted.

To see the impact of the active and reactive power compensation, the bus voltage magnitude and phase angle were recorded with different simulation conditions: general control without feed-forward active and reactive power compensation, with only reactive power compensation, with both active and reactive power compensation.

Fig. 9 shows the bus voltage magnitude during one load cycle under different compensation conditions. From the upper plot it can be seen that even without feed-forward active and reactive power compensation, the bus voltage could be kept within the range of 0.98pu-1.02pu except two spikes that occurred when the load active power changed abruptly. Although the voltage deviation was not very large, the duration was quite long (85% of the load cycle). The bus voltage magnitude was improved when the reactive power of the load was compensated directly by taking it as a feed-forward to the converter reactive power control, as shown in the middle plot. With feed-forward reactive power compensation, the reactive load power was almost completely provided by the StatCom (including the 19 MVA filter capacitor reactive power). As shown in Fig. 10, the network reactive power supply was almost zero for the whole load power cycle.

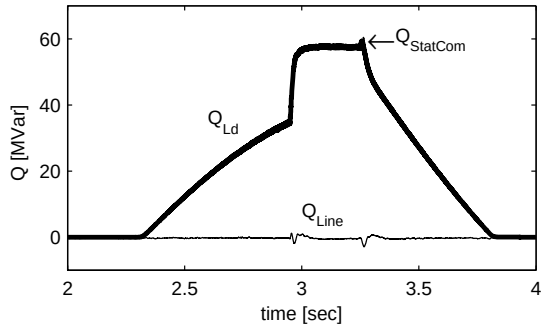

Fig. 10. Reactive power during one load cycle

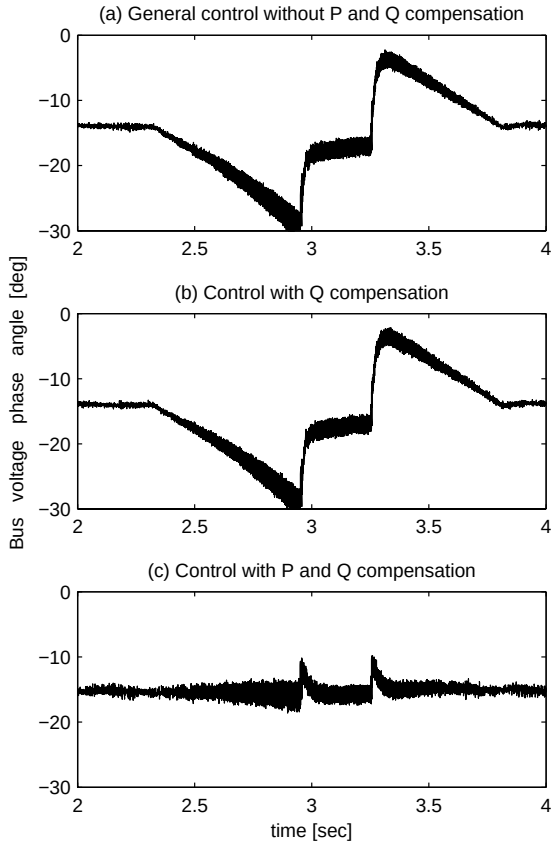

Fig. 11. Bus voltage phase angle

Even though the overall voltage magnitude was improved, the reactive power feed-forward control had hardly any impact on the voltage spikes. Moreover, the 2 upper plots in Fig. 11 show two phase jumps in the bus voltage. A large phase jump means big disturbance to other loads, especially phase sensitive loads such as ac motors, line commutated converters, etc.

When the converter had energy storage capability and the pulsating load active power was compensated by feed-forward active power control as described above, both the magnitude and the phase angle of the bus voltage were well controlled, as indicated by the lower plots of Fig. 9 and Fig. 11.

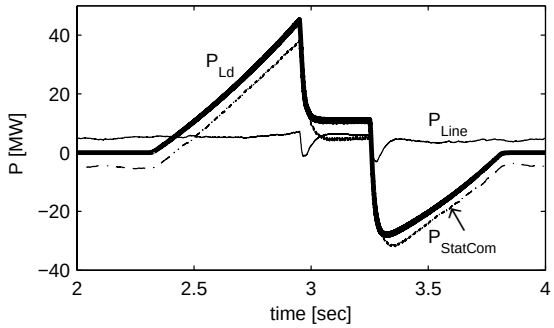

Fig. 12. Active power during one load cycle

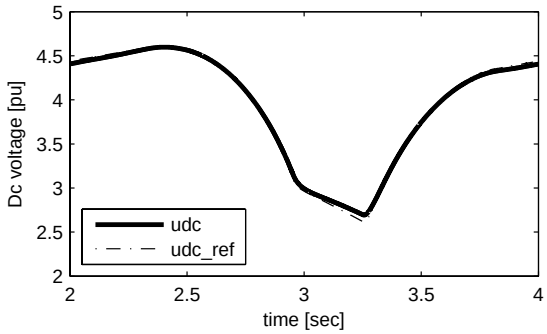

Fig. 13. Converter dc voltage

By utilization of load power feed-forward control, the pulsating part of the load active power was almost fully provided by the VSC, while the network only had to supply the average active power. This can be seen from Fig. 12, in which the load power, the power taken from the network and the power taken from the StatCom are plotted. Since the network only had to supply the average active power of the load, there was almost no phase shift in the bus voltage. Although there were two spikes accompanied by the phase jump occurring when the load active power changed abruptly, the magnitude was kept at a fairly low level of 3.2%. The phase jump was also reduced significantly due to the utilization of the active power compensation, which means reduced disturbance to phase sensitive loads.

Fig. 13 shows the variation of the dc voltage and its reference value during one load cycle.

VI. Conclusion

Cyclic loads may create severe disturbances in the network. Simulations have shown that a StatCom can provide fast reactive power support and thus can stabilize the bus voltage. Integration of energy storage with a StatCom can further mitigate the voltage magnitude disturbance. Additionally, the bus voltage phase jumps caused by the pulsating active power of the load can be reduced significantly.

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