High frequency winding design for planar switch mode transformers

André Büttner, Arne Nysveen and Magnar Hernes

***Abstract*—Switch mode power supplies as a mass produced article leave room for optimization especially at the voluminous magnetic components. Hereby planar component designs can reduce the overall height of the power supply and give it a more compact design. Since cores are available in standard sizes the optimal winding layout has to be found. Due to increased parasitic capacitance interleaving is not a good option to reduce losses in the windings at high frequency resonant power supplies.**

This article presents and evaluates different winding designs for resonant switch mode transformers operating in power supplies with frequencies larger than 500kHz. This article shows that the revolved parallel design performs best of the tested designs under the given conditions. In addition, the revolved design can compete with solutions as planar litz when it comes to value meaning cost and production complexity. Furthermore, the article shows the abilities of a heat measurement prototype.

***Index Terms*—Transformer windings, Switched mode power supplies, Electromagnetic analysis, Planar design, Thermal measurements**

I. INTRODUCTION

Switch mode power supplies (SMPS) are some of the most produced electric circuits worldwide. These devices power PCs, TVs, DVD players charge mobile phones and are consequently a mass-produced article. Therefore increasing the power density and reducing the cost are still the driving factors in designing SMPS. Magnetic components comprise a large amount of the volume in SMPS and therefore a size reduction and power density increase is beneficial. In the 1980s planar magnetic components were introduced, but they could not outperform the conventional wire wound components due to higher costs [1], [2]. Lower component height and better thermal management are advantages with the planar core design. In addition low controllable leakage inductance, very good repeatability and good adaptability for mass production are benefits in combination with printed circuit boards (PCB).

In order to minimize the effects of eddy currents, design guidelines have been established [3]. Unfortunately some are restricted to a certain frequency range. The rule of keeping the track width smaller than the double skin depth becomes impractical when the frequency exceeds 500kHz. This would result in a track width of 200µm, already small for cheap PCBs.

In order to achieve high currents, tracks are usually paralleled to increase the conductive area, [4]. Paralleling tracks may cause additional losses due to the proximity effect and circulating currents. These losses can be reduced by interleaving the primary and the secondary winding. Since high frequency designs above 500kHz are the field of resonant converter topologies, interleaving becomes problematic. Interleaving reduces the leakage inductance while increasing the parasitic capacitance. This capacitance interferes with the resonant circuit and needs special attention during the resonant design procedure. Therefore interleaving is not considered as an option in this article. The use of planar litz wires as presented in [5] seems expensive for a competitive design.

This article presents and evaluates different designs of transformer windings for resonant switch mode topologies operating higher than 500kHz, when interleaving becomes of limited use.

Design validations can be achieved by finite element analysis (FEA), analytic approaches and by measurements.

FEA makes it possible to solve complex problems with high accuracy. The accuracy can be improved by refining the mesh and hence increasing the number of elements. As a result the

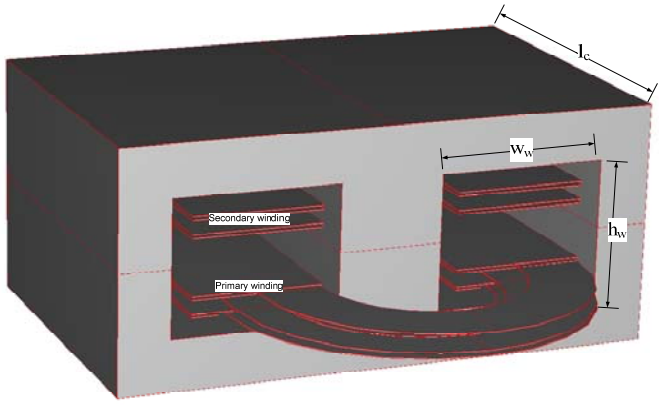


Fig. 1 3D outline of a EE43 core set with windings

The core set dimensions important for winding design are window width w_w=13.3mm, window height h_w=10.8mm, and core length l_c=28mm.

Manuscript received May 23, 2008. This work was supported in part by the Norwegian Research Council in Cooperation with SINTEF Energy Research

A. Büttner is with the Department of Electrical Power Engineering, Norwegian University of Science and Technology, Trondheim, Norway (e-mail: andre.buettner@elkraft.ntnu.no).

A. Nysveen is with the Department of Electrical Power Engineering, Norwegian University of Science and Technology, Trondheim, Norway (e-mail: arne.nysveen@elkraft.ntnu.no).

M. Hernes is with SINTEF Energy Research, Trondheim, Norway (e-mail: magnar.hernes@sintef.no).

equation system to solve increases and consequently the computational time too. In the 1990s some scientist [6] gave up on FEA due to lack of satisfactory results, long computation time and demand on the hardware. Further on the drawback long input and increased calculation time due to difficult geometry does not hold for the simple planar design. Nowadays it is not necessary to use a workstation, a dual core processor with 1GB RAM is sufficient to achieve proper results of a 2D planar model in seconds. Therefore FEA has become competitive to analytic design approaches particularly for planar objectives as already presented in [7]. Of further interest is the implementation into circuit modeling as presented by [8]. Still long computation time becomes a serious issue for 3-dimensional models.

Most of the existing analytic methods have been derived from applied theory mainly used for electric machines to one-dimensional problems in the transformer [9]. The one-dimensional solution cannot be applied to all applications. In [10] a method was introduced using a two-dimensional approach. The equations presented in [10] were used to give an estimation of the expected losses. The results of the estimations are presented in TABLE II at the end of the article.

As stated in several publications electric measurements tend to become inaccurate and thermal measurements are suggested [11]-[13]. In [12] was shown that the delay time of a 10cm cable is sufficient to cause a loss error of 10% at 500kHz and 4W estimated losses. At 1MHz and an estimated winding power loss lower than 2W, this results in an unacceptable error. Therefore calculating the loss components from the equivalent circuit using the classical no-load and short-circuit measurements are likely to fail.

II. Circuit Description and Design Proposals

In order to limit the amount of alternatives, only winding designs operating in a 1MHz resonant LLC full bridge converter were developed. The principle converter circuit is shown in Fig. 3. The additional inductance L for the circuit was implemented by using the larger leakage inductance of the non-interleaved design. In order to operate the converter stable a small airgap of 220µm was applied to the core set.

The chosen core set is a planar EE43 combination see Fig. 1, accommodating windings with a track thickness of 70µm copper and a transformation ratio of 10 to 2. Due to the 2 diode rectifier circuit, the number of tracks for the secondary winding becomes 4. Meaning 2 turns for each diode.

For a good comparison the designs were mounted in a plastic frame to assure the same distance between primary winding and secondary winding and core. The winding were designed with a clearance distance to the core of h_{clear}=1.5mm and a creepage distance between neighboring turns of d_{creep}=300µm. With a PCB thickness of h_{PCB}=1mm the leakage channel has a height of h_{leak}=5.8mm. The mean length turn for the E43 core set can be calculated using (1).

$$MLT = 2\left(l_c + w_{cl}\right) + 4\left(\sqrt{\frac{1}{2}w_w^{\,2}}\right) \tag{1}$$

The following four designs were designed and evaluated

A. Distributed winding design

The idea for this design is to counteract the losses close to the leakage channel by increasing the area in this position. This means the turns are distributed unequally between the layers, the first layer has 1 turn the second layer has 2 turns etc. The outline for 10 turns and 4 layers is shown Fig. 2 (b).

B. Split winding design

Fig. 2 (c) shows the split winding design. The turns are equally distributed over the layers resulting in a non-integer number of turns per layer.

C. Parallel track design

The parallel track design is shown in Fig. 2 (a). This design uses paralleling of tracks to increase the conductive area. The turns are laid out side by side in one layer and paralleled with the layer above and below.

D. Revolved parallel design

The revolved parallel design is inspired by the idea of the Roebel-bar [14]. The tracks of the winding take different positions during the 10 turns. The tracks are revolved at

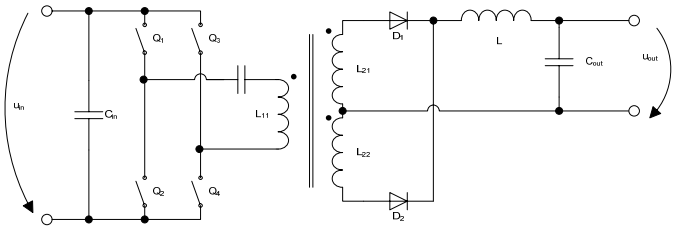
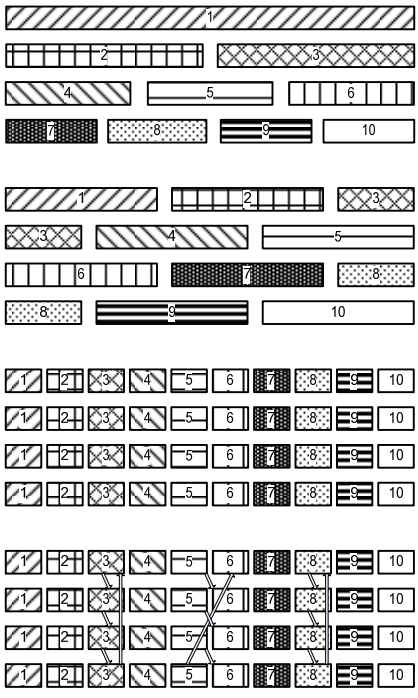


Fig. 3 Outline of the resonant full bridge converter with 2 diode rectification.



(a) *Distributed winding design* one track per turn but different track width

(b) *Split winding design* some turns consist of two tracks to fill the layer

(c) *Parallel track design* each turn is split in several tracks

(d) *Revolved parallel design* at 2.5, 5 and 7.5 turns the conductors are revolved

Fig. 2 Primary windings design proposals, leakage channel on top of each design

2.5turns at 5 turns and at 7.5turns as presented in Fig. 2 (d) thus reducing current imbalance.

III. Simulation and Measurement Setup

A. Finite Element Analysis

The program COMSOL Multiphysics [15] was used to simulate the candidate designs. To avoid long computation time and computation demands the presented FEA results are achieved by two-dimensional-simulations of the winding window only.

The relative permeability of the core is set to $\mu_r=\infty$. In addition only the total current of each turn is known. The resulting current density distribution over the tracks is calculated by the program.

The model parameters are: track thickness 70µm, the electric conductivity of the conductor is set to $\sigma_{Cu@25°C}=59.98\text{x}10^6$S/m, turn ratio 10:2. The primary current is a sinusoidal current with RMS value of I_{pri}=1.5A and the secondary current is a sinusoidal current with RMS value I_{sec}=7.5A.

B. Measurement setup

It is known that a 2-diode rectifier results in larger secondary winding losses than bridge rectifier topologies. Therefore the secondary winding was operated at 4 turns (instead of 2 by 2 center tapped) during the heat measurements. This reduces the effects caused by the secondary windings which were of lesser interest in this investigation. The transformer was operated in short circuit on the secondary side with a primary current of *Ipri*=1.5A. The frequency of the converter was adjusted to f_{meas}=833kHz during the measurements since this frequency gave the least overall oscillations for all designs under test, cf. Fig. 4. Due to the short-circuit setup the voltage driving the flux is low resulting in low core losses. Using (2) the peak value of the flux density results as B_p=5mT.

$$B_p = \frac{\Psi_{pp}}{2A_e N_1} = \frac{V_{in}}{4 f_{meas} A_e N_1} \qquad (2)$$

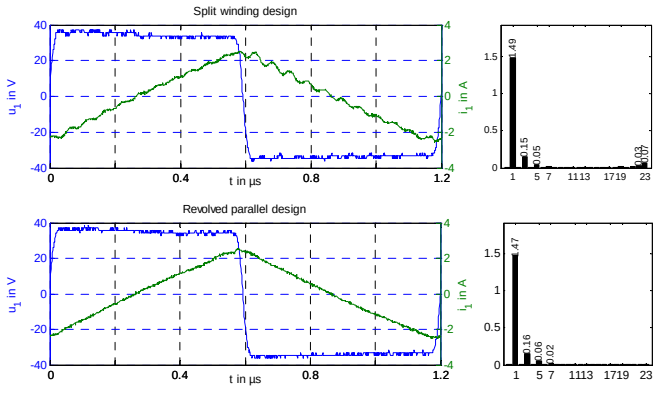


Fig. 4 Electrical measurements and Fourier analysis for two design proposals

The other two designs show similar electric results. The parallel track design shows no oscillation but the distributed winding design shows a 19th harmonic of 0.03A.

TABLE I
CONSTANTS AND VALUES FOR SIMULATION AND MEASUREMENTS

Symbol	Quantity	Value and unit [a]
lc	core length	28mm
w_w	width of the winding window	13.3mm
w_{cl}	width of the center leg	8.1mm
MLT	mean length turn	109.6mm
h_w	height of the winding window	10.8mm
h_{track}	track thickness	70µm
h_{clear}	Clearance distance to the core	1.5mm
h_{PCB}	thickness of the PCB	1mm
h_{leak}	height of the leakage channel	5.8mm
d_{creep}	creepage distance between neighboring tracks	300µm
Ipri	primary current RMS value	1.5A
Isec	secondary current RMS value	7.5A
Vin	primary voltage into the transformer	38V
f_{meas}	Measurement frequency	833kHz

Due to lack of data the core losses could not be obtained from the data sheet of the core material (3F4). However this does not mean that the core has no losses at this operation point as it will be shown later in the article.

The prototype of a heat measurement unit (G1) developed at SINTEF was used to conduct the heat measurements.

1) The heat measurement unit G1

The G1 is a kind of water based flow calorimeter. The basic scheme is shown in Fig. 5. The unit consists of a water tank with pump and a silicone pipe system. The unit is equipped with six water streamed probes. The water flow in each probe can be adjusted by the valves. The inlet and the outlet of the probes are equipped by thermocouples in T-type used as differential measurements. Type T (copper–constantan-copper) thermocouples are suitable for measurements in the −200 to 350 C range giving a sensitivity of about 43µV/°C. As both conductors are non-magnetic, type T thermocouples are appropriate for measurements involving magnetic fields. The probes consist of PMMA (polymethyl methacrylate) bonded on a ceramic base plate (aluminum ceramic substrate). This assures an equal spread of the heat over the probe and in

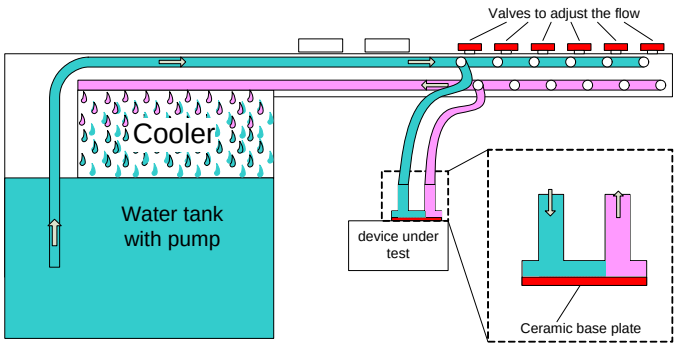


Fig. 5 Basic scheme of the G1 - heat measurement unit

The water is pumped through the pipes and the probe and heats up by the device under test. The thermocouples on the inlet and the outlet give a voltage in linear dependence to the heat emitted by the device under test. The heated water goes through the cooler dripping into the water tank.

addition guarantees a proper cooling to the point of interest.

The G1 measures the heat absorbed by the heat measurement probes. With the heat capacity to the circulating water the power can be calculated using the differential temperature increase connected to the thermoelectric voltage. The G1 is equipped with two calibration resistors with 1W and 10W. After calibration of the probes to 1W=0.1mV or 10W=0.1mV respectively the heat can be directly metered as a voltage. Since the expected losses are in the 1W area the probes were referenced with 1W calibration resistance. Using the 1W reference the sensitivity of the unit is good enough to meter the heat radiation of a bare hand (30mW) in proximity to the probe. The maximum power that can be metered is dependent on the water flow and the return temperature of the water since the water temperatures of tank and surrounding have to be equal. A maximum water temperature difference of ΔT=25K at 43µV/ C corresponds to 100W if 0.1mV=10W.

Since an exact adjustment of the probes to 0.1mV is very tedious and regarding the linear relation between voltage and temperature one can use the reference resistors to calculate scaling factors for each probe instead. An Agilent 34970a data acquisition switch unit logged the data.

2) Avoiding of error sources

As already stated, the water temperatures in the tank and the surrounding have to be equal to provide correct measurements. A higher water temperature would result in underestimated measurements and a lower water temperature would results in overestimated measurements respectively.

The device under test and the probes of the G1 were operated in an isolated housing of styrofoam with wall thickness of 6cm. This setup prevented influence due to heat sources in proximity of the probes i.e. solar radiation, opening door etc.

The use of a reference heat source for calibration removes the issue of accuracy in the thermocouples and in the flow regulation, as long as the flow is kept constant.

3) Measuring places and sequence

The probes were placed on the transformer at the plastic housing, the core, the secondary winding topside, and on the primary winding topside as it can be seen in the photograph in Fig. 6.

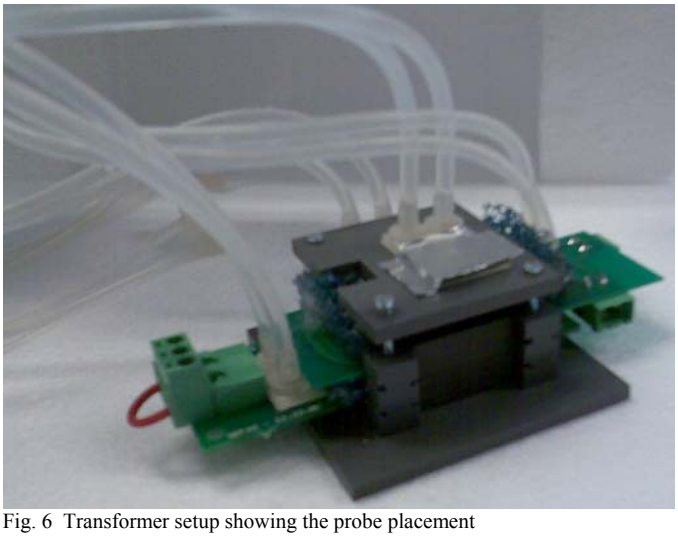


Fig. 6 Transformer setup showing the probe placement

The probe places are: secondary top-side, primary top-side, core, and plastic housing

The transformer was placed in the styrofoam housing with the heat measurement probes in place. Then the logger was started until the recorded voltages have settled (after approximately 5min). At that moment the converter was started supplying the transformer with the rectangular voltage assuring the primary current of *Ipri*=1.5A. After 10min the converter was turned off for 5min, and then turned on again for 5min and after that finally off.

IV. Simulation Results

All design proposals were simulated under the conditions and assumptions defined in Section III.A. In order to achieve plots showing the frequency dependence, the frequency was increased from 0 to 1MHz in logarithmic steps with 833kHz as an extra step to directly compare the measurement results later. The copper conductivity is chosen at 25ºC since the G1 measurement unit keeps the component at the ambient temperature.

The simulation results for the ratio R_{AC}/R_{DC} and the AC resistance R_{AC} are shown in Fig. 7. The *parallel track design* shows the largest losses even at low frequencies and is problematic without interleaving since the leakage field is forcing the current into the layer nearest to the leakage channel. This results in circulating currents between the parallel circuits. The losses for *distributed windings* are lower than for the parallel design since the copper area of the turn nearest to the leakage channel is increased considerably in comparison to the other designs. The distributed design would perform even better under higher temperature for the reason that the copper conductivity is reduced, giving less eddy currents in the turn close to the leakage channel. The *split winding design* has the lowest R_{AC} and can use the advantage of the larger copper area. In addition it benefits from the lower losses of the turns in the layers distant to the leakage channel.

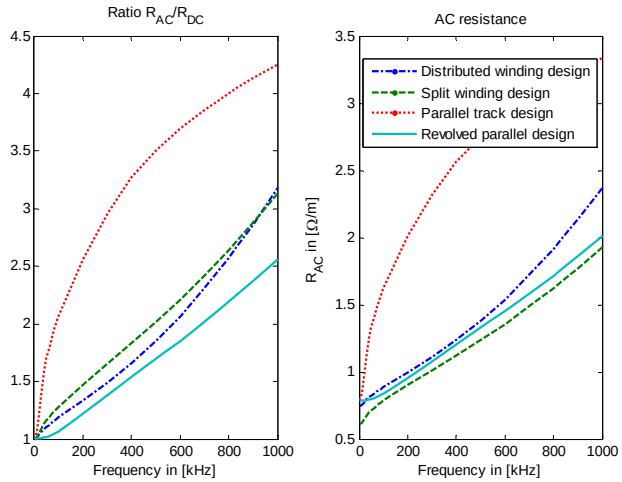


Fig. 7 Simulated ratio R_{AC}/R_{DC} and AC resistance R_{AC} in Ω/m for the design proposals

The revolved parallel design has the lowest R_{AC}/R_{DC} ratio of all compared designs but the split winding design has the lowest R_{AC}.

This can be seen in Fig. 8 were the distribution of the R_{AC} for the individual turns are shown. The *revolved parallel design* has the second lowest R_{AC} and the advantage of an even current distribution in each turn. This results in the lowest ratio R_{AC}/R_{DC} for the revolved parallel design as shown in Fig. 7.

The distribution of the losses in the winding gives indication of expected local heat sources and makes it possible to derive further optimized winding schemes. The distributed winding design operates well up to 400kHz. At larger frequencies the eddy current effect exceeds the effect of the large copper area close to the leakage channel, cf Fig. 8 (a) triangular markers. (turn 1). As Fig. 8 (b) shows the split winding design has the largest losses in turn 3 (circular

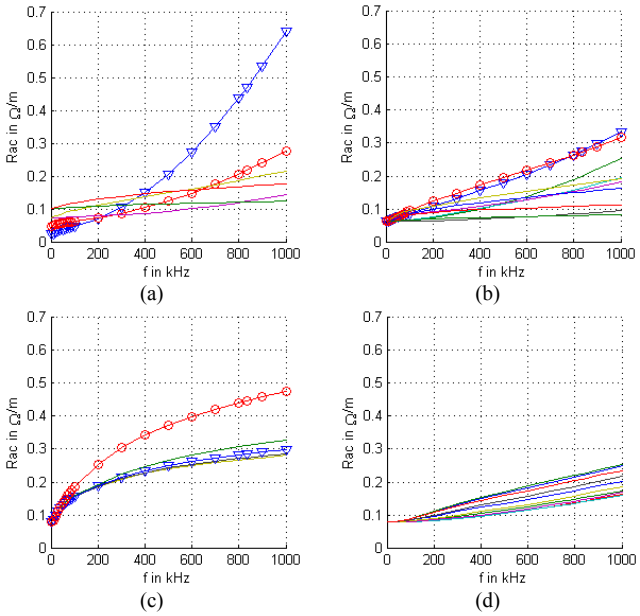


Fig. 8 Turn wise simulation results of losses for the primary winding designs
(a) Distributed winding design (b) Split winding design (c) Parallel track design (d) Revolved parallel design
Triangles indicate turn 1,circle indicate turn 3

markers) and in turn 1 (triangular markers). The parallel track design is unsuitable even for frequencies below 200kHz. The losses in the top layer are still dominant Fig. 8 (c) (circular marker). The limit for the revolved track design has not been reached at 1MHz. One has to keep in mind that the simulation presents ideal revolving (planar litz) which is difficult to achieve in a PCB design. In addition this might become impractical due to the amount of layer junctions.

V. Measurement Results

Regarding the high frequency the losses are metered using thermal measurements with the G1 as explained in Section III.B.1).

One example of a complete unfiltered measurement sequence for the distributed winding design is shown in Fig. 8. All designs were measured in the same way giving comparable results. The logged data was post processed using MATLAB/Simulink. Since the heat dissipation of the core affects the measurement of the winding heat dissipation, one

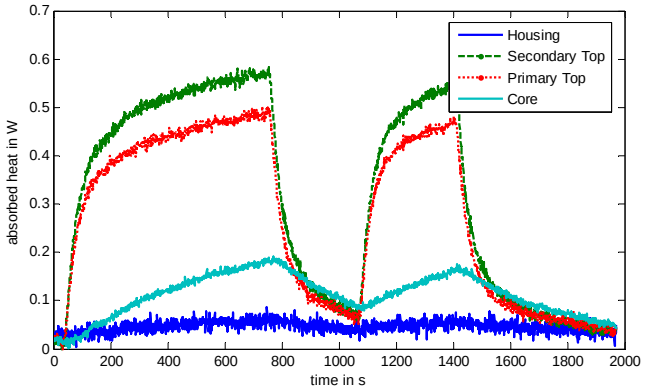


Fig. 9 Unfiltered scaled heat measurement sequence for the distributed winding design
The figure shows the heat coupling between core and winding. The windings reach the settle point at approx. 250s but continue to rise due to the heating of the core.

can subtract the temperature gradient of the core divided by the heat resistance to obtain the actual absorbed heat of the winding. The values achieved by this method are presented as Q_{meas} in TABLE II. However this practice would result in underestimated losses since not all heat can be absorbed by the probes.

Since the same secondary layout is used in all designs the losses in the secondary winding can be assumed to be the same. Therefore the ratio of the absorbed heat of primary and secondary Q_{pri}/Q_{sec} can present a qualitative result as shown in

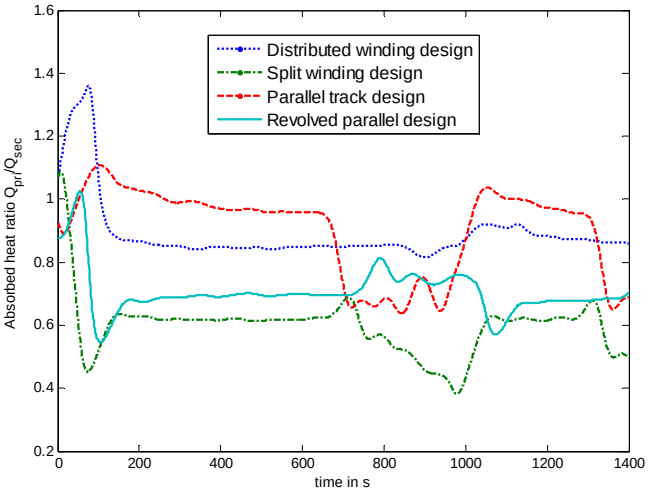


Fig. 10 Measured loss ratio Q_{pri}/Q_{sec} for the design proposals
The signals are filtered but not scaled and then divided. The flat areas (200..600s and 1100..1300s) present the stable operation point.

Fig. 10. Hereby the signals are filtered but not scaled and then divided giving the ratio. This eliminates influences due to all sources simultaneously affecting primary and secondary winding e.g. core heat dissipation.

VI. Result Summary and Discussion

Due to the PCB design process the conductive copper area is different for all designs. Of special importance are the creepage distance demands (clearance) between neighboring turns. Since the creepage distance is the same for all neighboring tracks, three tracks per layer result apparently in more copper cross sectional area than ten tracks per layer.

TABLE II
RESULT SUMMARY

	Distributed winding design	Split winding design	Parallel track design	Revolved parallel design
Primary Winding Results				
R_{DC} *in* $\frac{\Omega}{m}$	0.745	0.614	0.783	0.783
R_{AC} *in* $\frac{\Omega}{m}$	1.986	1.361	2.899	1.457
P_{sim1} *in W*	0.490	0.411	0.782	0.435
P_{est1} *in W*		0.223	0.338	
Q_{meas1} *in W*	0.35	0.25	0.38	0.27
Secondary Winding Results				
P_{sim2} *in W*	0.368	0.368	0.364	0.365
P_{est2} *in W*	0.215	0.215	0.215	0.215
Q_{meas2} *in W*	0.39	0.41	0.41	0.40
Total Results				
P_{sim} *in W*	0.859	0.780	1.146	0.800
P_{est} *in W*		0.437	0.552	
Q_{meas} *in W*	0.74	0.66	0.79	0.67

The frequency for all AC results is the measurement frequency f_{meas}=833kHz, the *MLT*=109.7mm

Knowing this puts the importance of the ratio plot of Fig. 7 into perspective to the R_{AC} plot of Fig. 7. This becomes more clear by comparing the values of R_{AC} at the measurement frequency of f_{meas}=833kHz as summarized in TABLE II. The mean length turn for the used E43 core is *MLT*=109.7mm giving losses for the designs as stated in TABLE II.

Regarding the prototype state of the G1 and comparing the simulation results with the heat measurements shows that the measurements are only comparable by means of quality but not by the values given in TABLE II. The value discrepancy can be a consequence from fact that the probe can not absorb all heat created by the winding. In addition the error can result from the difference of the current harmonics, the mean length turn of the designs and it can be the effect of the interconnection-wiring mandatory due to the PCB restricted to four layers. Since the error in the thermocouples is eliminated in comparing the ratio, cf. Fig. 10, gives trust worthy results.

The *split winding design* and the *revolved parallel design* perform best under the given conditions. The *distributed winding design* generates large losses in the layer close to the leakage channel, cf. Fig. 8 (a), and could not use the advantage of the large copper area at the frequency of 833kHz. The high frequency and the large winding width close the leakage field were not the best combination. The *parallel track design* is the worst design because only the layer close to the leakage channel conducts the current.

As stated in the beginning the reason for omitting interleaved design was the parasitic capacitance. The parasitic primary winding capacitance is also large in the distributed winding design and in the split winding design due to the combination of large areas with different potentials close to each other, cf. Fig. 4.

VII. CONCLUSION AND GUIDELINES

Planar litz is not an option due to the high cost. Therefore the revolved parallel design is regarded as the best option for planar transformers operating in resonant switch mode power supplies. The revolved parallel design with certain revolve points performs well enough and does not cost more than any other PCB with the same amount of layers. Due to the linear influence of the mean length turn, the windings have to be designed carefully. A sloppy design results in avoidable losses. The distributed winding design fails for frequencies above 450kHz. One advantage of the distributed winding design is the possibility to avoid an interconnection layer or interconnection wiring. It was the only design to get along with four layers. Turn dislocation in order to reduce the capacitance is a waste of copper area and should be avoided.

The G1 heat measurement unit provides interesting features for heat and loss measurements. However, since the G1 is a prototype the accuracy of the unit has to be verified in order to rely on the results given. Of special importance is the identification of heat leaking paths. These paths have to be eliminated, minimized or handled by calibration. Furthermore operating the unit below 1W seems not to be the optimal power area. Nevertheless, the qualitative results are good enough to compare the design proposal.

REFERENCES

[1] M.T. Quirke, J.J. Barrett, and M. Hayes, "Planar magnetic component technology-a review" in *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, 1992. **15**(5): p. 884-92.

[2] C. Quinn, K. Rinne, T. O'Donnell, M. Duffy, and C.O. Mathuna, "A review of planar magnetic techniques and technologies" in *16th Annual IEEE Applied Power Electronics Conference and Exposition*. 2001. Anaheim, CA, USA: IEEE.

[3] Ferroxcube, "Design of planar power transformers" Application Note 2001

[4] W. Chen, Y. Yan, Y. Hu, and Q. Lu, "Model and design of PCB parallel winding for planar transformer" *IEEE Transactions on Magnetics*, vol. 39 nr. 5, pp. 3202-3204, September 2003.

[5] S. Wang, M. A. de Rooij, W. G. Odendaal, J. D. van Wyk, and D. Boroyevich, "Reduction of High-Frequency Conduction Losses Using a Planar Litz Structure" in IEEE Transactions on power electronics, vol. 20, no. 2, pp 261-267, March 2005

[6] D. van der Linde, C. A. M. Boon, and J. B. Klaassens, "Design of a High-Frequency Planar Power Transformer in Multilayer Technology" in IEEE Transactions on industrial electronics vol. 38, no. 2, pp. 135-141, April 1991

[7] B. Ackermann and A. Lewalter, "Two-dimensional calculation of winding losses in planar magnetic components" in 4th IEEE International Conference on Power Electronics and Drive Systems, pp. 674-679 vol.2, 2001. Denpasar, Indonesia: IEEE.

[8] P. Zhou, W. N. Fu, D. Lin, S. Stanton, and Z. J. Cendes, "Numerical Modeling of Magnetic Devices" in IEEE Transactions on magnetics, vol. 40 no. 4, pp. 1803-1809, July 2004

[9] P.Dowell. "Effect of Eddy currents in transformer windings". Proc. IEE, vol. 113, pp 1387-1394, 1966.

[10] Drechsler, E. Calculation and optimization of switch mode magnetics. in 3rd International Telecommunications Energy Special Conference. 2000. Dresden, Germany: VDE-Verlag.

[11] O. Apeldoorn, K. Kriegel, " Optimal design for high-power high-frequency applications", in 6th European Conference on Power Electronics and Applications, pp 7-12 vol.1, 1995

[12] A. van den Boosche, V. Vlachev „ Inductors and transformers for power electronics", Boca Ranton CRC Press, pp 386-387, 2005

[13] Heinemann, L. Modelling and design of high frequency planar transformers. 1995. Atlanta, GA, USA: IEEE.

[14] W. Schuisky, "Berechnung elektrischer Maschinen", Springer-Verlag, Wien, p 236 1960

[15] COMSOL Multiphysics Version 3.4, COMSOL INC Stockholm 2008