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# Phase-change computing

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## ABSTRACT

Phase-change materials and devices are currently generating much interest for their potential to provide practicable alternatives to traditional von-Neumann computing (i.e. alternatives to computing in which memory and processing functions are carried out at physically separated locations). Indeed, many years after Ovshinsky and colleagues first showed the remarkable computing capabilities of phase-change devices (see for example [1-3]), other researchers have recently experimentally demonstrated the potential of phase-change devices to perform not only arithmetic computing [4], but also to provide hardware mimics of both synapses [5, 6] and neurons [4] (so opening the way to so-called bio-inspired or neuromorphic computing). We ourselves recently demonstrated reliable execution of the four basic arithmetic operations of addition, subtraction, multiplication and division using phase-change materials and micrometre-scale optical excitation with (groups of) femtosecond pulses [4]. In this paper however we demonstrate that this arithmetic capability is also accessible via the electrical domain and on the nanoscale.

The 'heart' of a phase-change arithmetic computer is a simple accumulator. With an accumulator we can perform all the basic arithmetic functions and, as we will show, also carry out complex arithmetic computations such as finding the prime factors of large numbers (furthermore we can do this latter task in a fast and efficient parallel fashion). To configure a phase-change device as an accumulator we tailor the input pulse amplitude and/or duration such that the SET state is reached (from the RESET state) not with a single pulse (as for normal binary memory operation) but with a pre-determined number of pulses. The number of pulses required to reach the SET state then provides the base for the computations to be performed using the accumulator (alternatively, for some algorithmic implementations, the number of pulses required to reach the SET state is determined by the specific computation being carried out).

We have implemented a base-10 phase-change accumulator using the pseudo device structure shown in Fig. 1(a). Here the top electrode is a combination of a lithographically defined contact pad and the tip of a conductive atomic force microscope (CAFM). The active layer in the device is $Ge_2Sb_2Te_5$ and the basic I-V switching curve is shown in Fig. 1(b). It can be seen that the threshold voltage for this particular configuration is around 3.7 V. If we apply input pulses with amplitude greater than this threshold (assuming typical pulse durations in the hundreds of

nanoseconds range), then the cell will switch into the SET state with a single pulse (as in normal binary memory operation). This is illustrated in Fig. 1(c). However, if we reduce the input pulse amplitude (while keeping the duration constant), then the number of pulses required to reach the SET state increases, as also shown in Fig. 1(c). By appropriate choice of the input pulse amplitude (and duration) we can thus tailor the number of pulses required for switching. In Fig 1(d) for example we show a case for which 10 pulses are required to reach the low resistance state. The response of Fig. 1(d) is in fact a base-10 accumulator and, in a similar manner to using an abacus, we can readily carry out base-10 arithmetic with this system, as we will show.

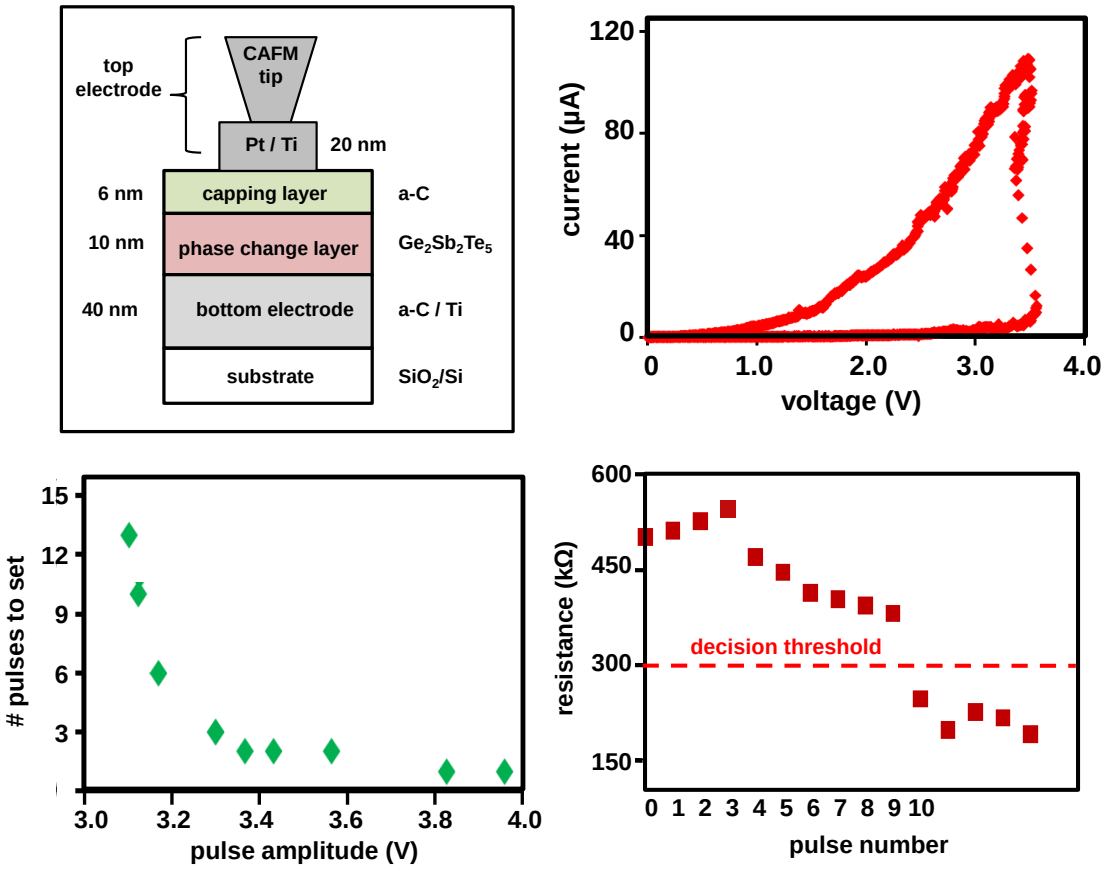


**Fig. 1** (a - top left) the pseudo device arrangement, (b - top right) I-V curve, (c - bottom left) number of pulses required to switch the cell versus pulse amplitude (200 ns duration pulse), (d- bottom right) the response of the base-10 accumulator system

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