Plasma Processing of III-V Materials for Energy Efficient Electronics Applications

Iain Thayne*, Xu Li, David Millar, Yen-Chun Fu, Uthayasankararan Peralagu
James Watt Nanofabrication Centre, School of Engineering,
University of Glasgow, Glasgow G12 8QQ, Scotland, UK

ABSTRACT

This paper reviews some recent activity at the James Watt Nanofabrication Centre in the University of Glasgow in the area of plasma processing for energy efficient compound semiconductor-based transistors. Atomic layer etching suitable for controllable recess etching in GaN power transistors will be discussed. In addition, plasma based surface passivation techniques will be reviewed for a variety of compound semiconductor materials ((100) and (110) oriented InGaAs and InGaSb).

Keywords: Compound semiconductors, atomic layer etching, plasma-based surface passivation

1. INTRODUCTION

The properties of compound semiconductor (III-V) materials make them highly attractive for improving the energy efficiency of contemporary and future electronic devices. The large bandgap, high breakdown field, high electron mobility and high saturation velocity of GaN-based materials are important enablers for high power and high frequency applications e.g. > 600 V power conversion and switching; and 5G RF and mm-wave transmitters. At the other "end" of the III-V materials spectrum, the low electron and hole effective masses, high saturation velocity and intriguing heterojunction band alignments of antimonide-based materials make them very compelling for high performance, sub 0.5 V CMOS logic and RF/mm-wave receiver applications.

With continued improvements in lithography, it is possible to define patterns with nanometric scale precision in resists and dielectrics. Similarly, contemporary atomic layer deposition techniques permit the conformal coating of dielectrics and metals with atomic layer precision. The ability to controllably etch with atomic scale precision is an important complementary capability, and is the scope of considerable activity in the mainstream semiconductor industry. The ability to undertake atomic layer etching (ALE) in compound semiconductor materials is also important for controlling threshold voltage in GaN-based power and RF transistors, and for the realization of non-planar narrow bandgap finfets and nanowires for continued CMOS scaling. Recent activity in the James Watt Nanofabrication Centre in the University of Glasgow (www.jwnc.gla.ac.uk) in atomic layer etching for these energy efficient electronics applications will be described in Section 2 of this paper.

To complement this etching work, Section 3 reports some developments in the use of post-etching in-situ plasma treatments for III-V materials before dielectric deposition – typical processes for advanced, non-planar devices. The impact of plasma processing on the etched surface can clearly be observed in the response of MOS capacitor structures using atomic layer deposited (ALD) dielectric stacks based on Al_2O_3 and HfO_2 deposited on InGaAs and GaInSb materials.

All of this work was undertaken in an Oxford Instruments Plasma Technology Ltd cluster tool where samples can be transferred between deposition and etch chambers without exposing processed surfaces to atmosphere.

Together these process modules are important additions to the palette of capabilities from which to select and determine process flows for optimizing the performance of advanced energy efficient transistors utilizing compound semiconductor materials.

*iain.thayne@glasgow.ac.uk; phone +44 (0)141 330 3859 ; fax +44 (0)141 330 6010; www.jwnc.gla.ac.uk

Advanced Etch Technology for Nanopatterning VI, edited by Sebastian U. Engelmann, Richard S. Wise,
Proc. of SPIE Vol. 10149, 101490R · © 2017 SPIE · CCC code: 0277-786X/17/$18 · doi: 10.1117/12.2257863

2. ATOMIC LAYER ETCHING OF III-V MATERIALS

2.1 Chlorine-based atomic layer etching

ALE (Atomic Layer Etching), a technique that removes very thin layers of material precisely using sequential self-limiting reactions has been considered one of the most promising techniques for achieving the low process variability necessary in the atomic-scale era [1].

For the last decade, AlGaN/GaN based HFETs have been intensely investigated as potential next generation power electronic device [2]. Emerging device topologies, e.g. the integrated cascode transistor, requires very precise control of gate recess eteching for the normally off device. [3]. Here, an ALE process for group III nitrides, based on a cycled procedure of Cl_2 chlorination and argon plasma removal of the chlorides is discussed.

The generic concept of ALE is shown in Figure 1, comprises a self-limiting plasma based modification of the material surface, followed by a plasma based self-limiting removal of the modified surface layer.

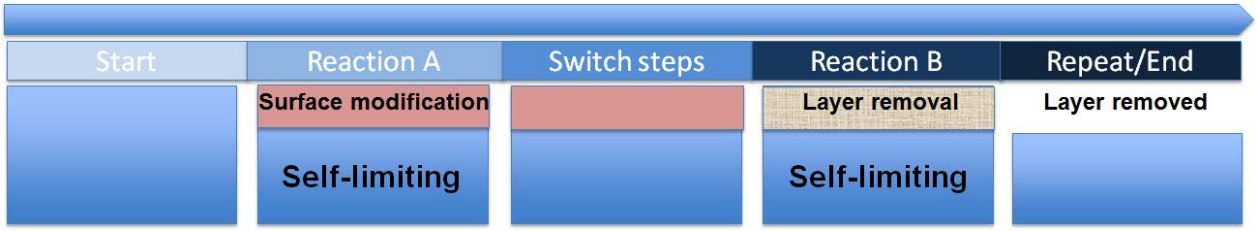

Figure 1. The ALE sequence which comprises a self-limiting surface modification process, followed by a self-limiting removal of the modified surface layer

Typical power device material structures used in this study are shown in Figure 2. The dual barrier structure is one which can be used for the realization of an integrated cascade device. The single barrier structure, is a more traditional AlGaN/GaN power device architecture.

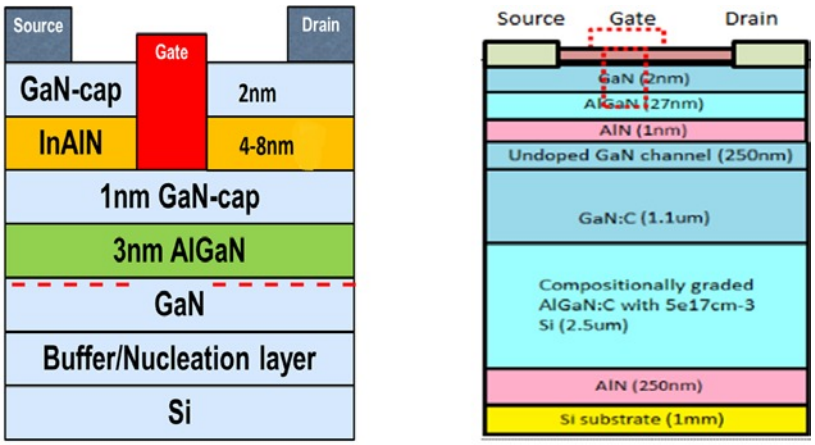

Figure 2. Left – a dual barrier GaN-based power device structure suitable for the realization of an integrated cascode transistor. Right – a more conventional single barrier GaN-based power device structure

An Oxford Instrument PlasmaLab Inductively Coupled Plasma (ICP) etching system with repeat loop function was used in this investigation. The etching chemistry was based on the formation of self-limited Al, Ga and In chlorides on the sample surface in Cl_2 gas or Cl_2 plasma and followed by a removal step using Ar plasma at an optimized RF power level at which the plasma removes only the surface chlorides.

Optimising the chlorination of the surface included comparing the use of Cl_2 plasma and simply flowing Cl_2 gas across the sample surface; time of chlorination; gas flow rate; gas concentration and chamber pressure. Optimisation of the Ar plasma removal step included an exploration of the impact of various parameters including RF power; chamber pressure and reaction time.

Figure 3 shows the effect of Ar plasma power on the etch rate of the chlorinated surface. For Ar plasma powers in the range 35- 45W, an "ALE window" is clearly seen. This data was obtained for 30 cycles of etching, with an etch depth of around 30 nm, which shows that the surface modification step is still too aggressive.

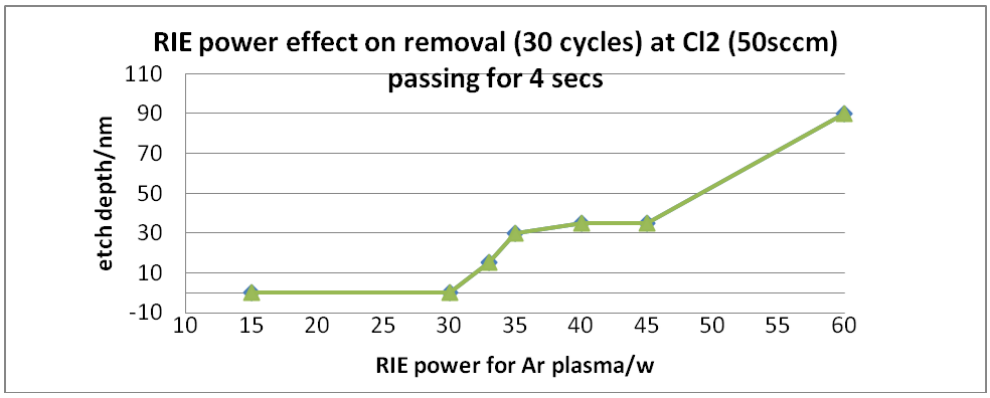

Figure 3. Effect of Ar power on etch depth for 30 cycles of the Cl-based ALE process at a given surface modification condition

By diluting the Cl_2 gas flow in Ar during the surface modification step, sub-nanometer per cycle etching can be achieved, as shown in Figure 4.

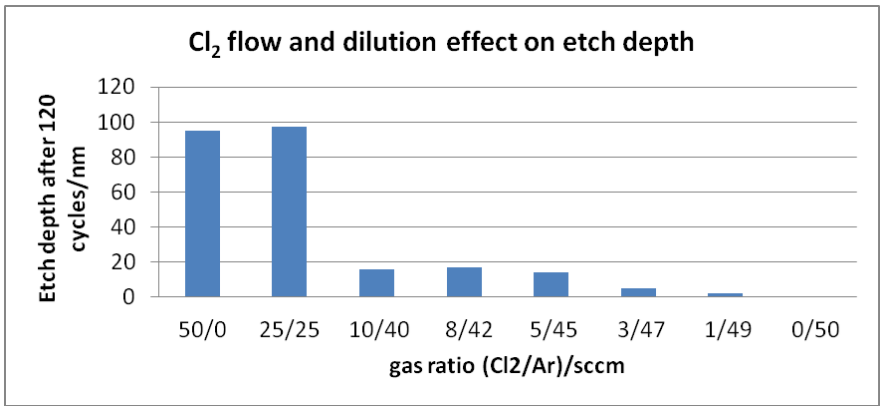

Figure 4. Effect of diluting Cl_2 gas with Ar during the surface modification step. Etch depths are determined from 120 cycles

This is confirmed in Figure 5, where a linear relation between etch depth and number of ALE cycles is clearly observed, with a removal rate of 0.13 nm per cycle.

One important aspect of any plasma based etch process in compound semiconductor devices, is the introduction of damage as a consequence of the interaction of energetic etch species with the underlying semiconductor materials. This is very important in the gate region of a transistor particularly if a plasma-based gate recess etch is being considered. Some of our very recent work [4], shows that with the optimized Cl_2/Ar ALE process described above, a 5 second Ar plasma exposure of a single barrier AlGaN/GaN structure at power levels in the "ALE window" can cause a 50% increase in sheet resistance as a consequence of a reduction in both electron mobility and channel carrier concentration. We have found however, that this can be mitigated by a post etch anneal process at temperatures which are compatible with the overall thermal budget of a GaN power transistor process flow.

An approach to further mitigate this damage induced effect is described in the next section.

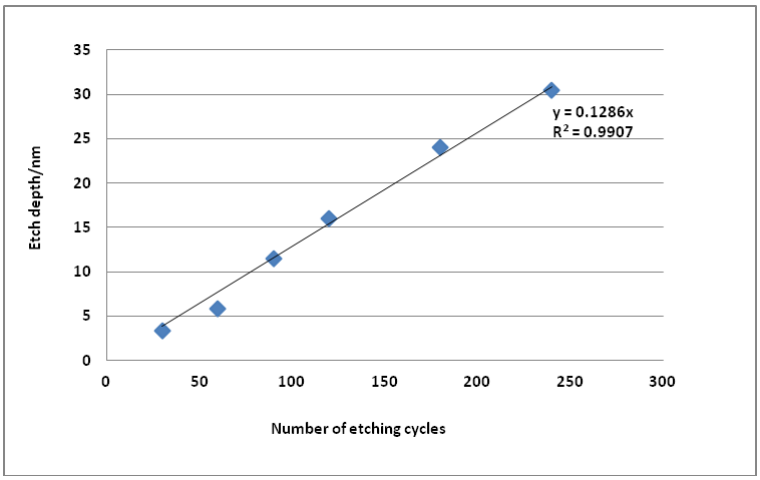

Figure 5. Etch depth as function of number of ALE cycles for the optimized process

2.2 Bromine-based atomic layer etching

As described above, an ALE window can be found for the controllable removal of III-N materials with etch rates of around 0.13 nm per cycle. However, the Ar plasma powers required introduce damage to the underlying materials. There is therefore a need to reduce the power of the plasma process step associated with the removal of the modified semiconductor surface. By considering volatility of the chemical species likely to be in the surface modified layer during ALE processes for compound semiconductor materials, the use of a bromine-based chemistry was explored.

The system configuration was identical to that described previously, and as before, the parameter space for both the surface modification and surface etch steps was evaluated. In the final optimised process, HBr diluted in Ar in a ratio 7:42 sccm flowed across the sample surface (no plasma was struck). This process enabled etching with an Ar plasma power of 20 W. As shown in Figure 6, for 160 cycles of this HBr:Ar ALE process, an etch depth of around 22 nm (0.13 nm/cycle etch rate) was obtained with rms surface roughness of 0.9 nm, similar to that before etching.

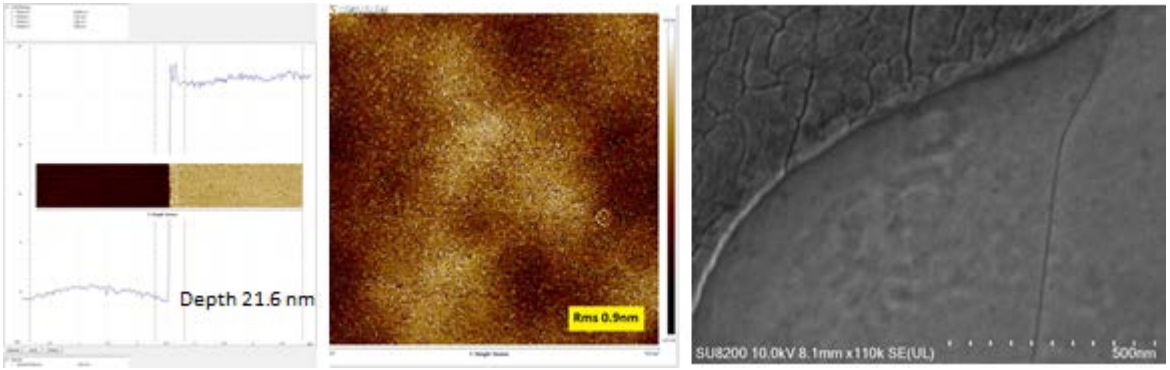

Figure 6. Etching depth by AFM (left); roughness of etching area (scan range 10x10 μm) by AFM (same as that before etching) (middle); SEM image of the etched step (right).

The ability to reduce the Ar plasma power to 20 W had a significant impact on the etch induced damage, as determined by van der Pauw measurement at room temperature. As shown in Figure 7, there is no modification to the electron mobility and carrier concentration and therefore sheet resistance of single barrier AlGaN/GaN structures as a consequence of 60 second exposure to Ar plasma powers of less than 25 W.

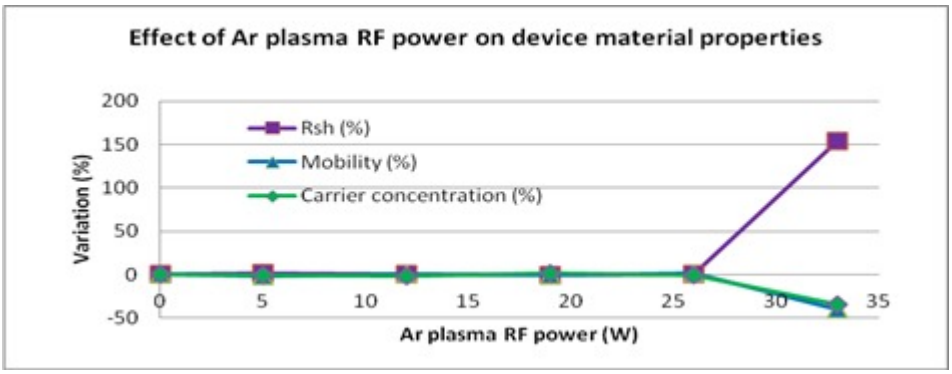

Figure 7. Impact of power of Ar plasma on electron mobility, carrier concentration and sheet resistance of single barrier AlGaN/GaN power device structure.

The HBr/Ar based ALE process therefore seems to be an encouraging one for controllable etching in the gate region of GaN-based power electronic devices, as etch rates of around 0.13 nm per cycle can be maintained but with minimal Ar plasma etch induced damage.

2.2 Plasma processes for InGaAs surfaces

A strength of the clustered plasma toolset is the ability to etch structures, then expose them to various plasma treatments in-situ before deposition of dielectrics. In this way, the etched surface chemistry should be controllable. This is very important for non-planar devices, and in particular compound semiconductor based finfets and nanowires where the impact of etch damage on the device performance is highly significant given the fins and wires have critical dimensions of 10's of nanometers. Described in this section are some findings from the first demonstration of the use of a cluster tool to explore the impact of the etch processes required for the formation of InGaAs finfets. The use of in-situ nitrogen and hydrogen plasmas on (100) and (110) oriented InGaAs surfaces subjected to a $Cl_2/CH_4/H_2$ etch chemistry prior to ALD deposition of a HfO_2 gate dielectric was evaluated using InGaAs MOS-capacitors.

Each plasma pre-treatment cycle comprised a plasma N_2 or H_2 pulse, a short TMA pulse, followed by an Ar gas draw/purge step and a plasma N_2 or H_2 pulse followed by 4 s of a N_2 or H_2 stabilization step. 25 cycles of plasma HfO_2 were then deposited at 300°C by ALD. MOS capacitors were then formed, using the process flow shown in Figure 8.

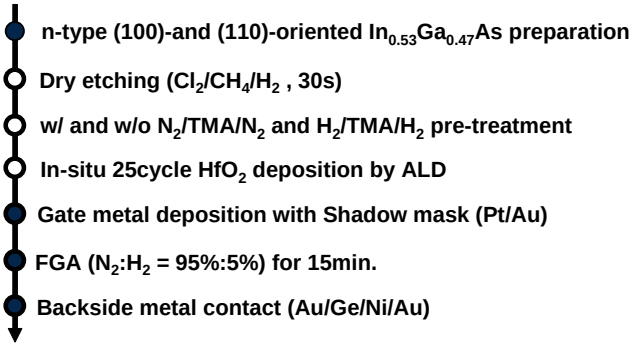

Figure 8. Process flow for MOS-capacitor fabrication with in-situ plasma processing and ALD on etched (100) and (110) oriented InGaAs

Based on frequency dependent room temperature C-V measurement, Figure 9, the control samples show the (110)-oriented layer has larger etch damage than the (100)-oriented layer. After cyclic plasma/TMA treatment, the in-situ etched (100)-oriented MOSCAPs (top row of Figure 9) have a slight reduction in frequency dispersion and bumps around mid-gap. Both parameters were improved significantly in the (110)-oriented MOSCAPs (bottom row of Figure 9) especially for plasma H_2.

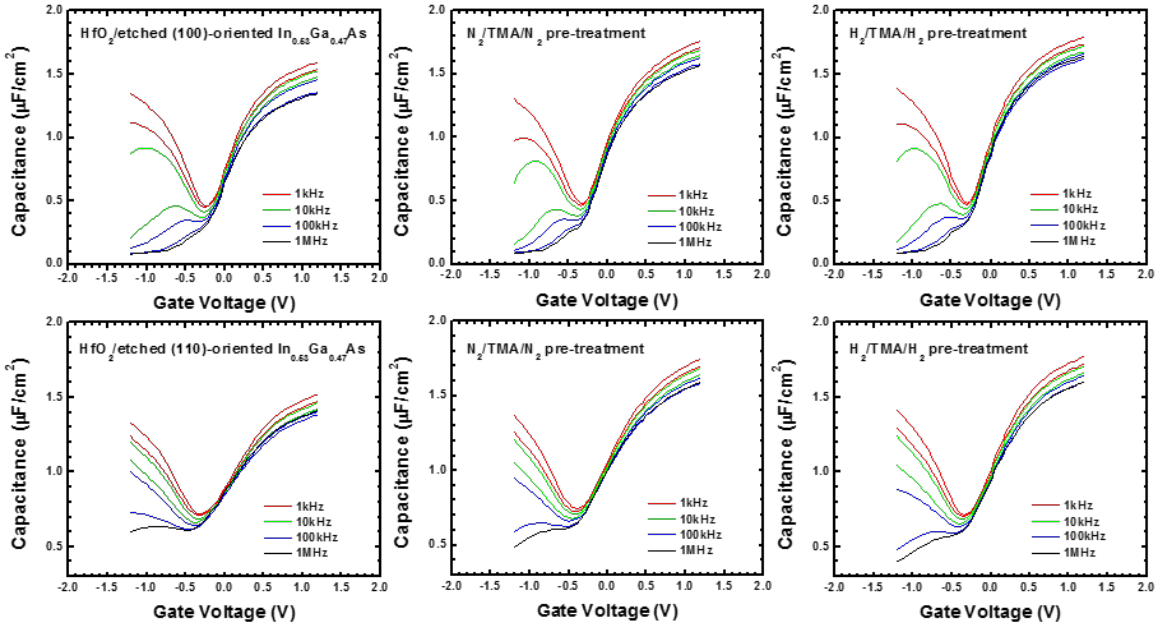

Figure 9. Room temperature C-V frequency variation of in-situ Au/Pt/HfO_2 (25cycle)/ etched (100)- and (110)-oriented n-$In_{0.53}Ga_{0.47}As$/InP MOS capacitors w/ FGA (top and bottom row) subjected to w/o and w/ 10cycle plasma N_2/TMA/plasma N_2 and plasma H_2/TMA/plasma H_2 pre-treatment.

The metrics of frequency dispersion in accumulation (C_{acc}), stretch-out (dC/dV) and hysteresis of all capacitors are captured in Table 1 which also reports the percentage variations of the metrics for control capacitors, w/ plasma N_2 and w/ plasma H_2. In relation to both control (100)-oriented and (110)-oriented samples, we observed ~17% and ~49% increase in dC/dV under plasma H_2 pre-treatment. On the other hand, both sample with plasma N_2 pre-treatment had ~5% and ~18% increase comparing to control samples.

Table 1. The analysis of frequency dispersion in accumulation (C_{acc}), stretch-out (dC/dV) and hysteresis of capacitors together with % variation of the metrics for plasma N_2/TMA/plasma N_2 and plasma H_2/TMA/plasma H_2 pre-treatment on (100)-oriented and (110)-oriented $In_{053}Ga_{0.47}As$ layers with respect to these control capacitors .

Capacitor	*C_{acc} (%dec)*		*dC/dV at 1kHz*		*Hysteresis at 1MHz*	
	%/dec	% variation	x 10^{-6} ($Fcm^{-2}V^{-1}$)	% variation	mV	% variation
(100)	5.21		1.87		68.5	
N_2/TMA/N_2	3.66	-29.7	1.95	+4.46	54.3	-20.8
H_2/TMA/H_2	2.78	-46.6	2.19	+17.0	65.1	-4.96
(110)	2.45		0.92		68.3	
N_2/TMA/N_2	3.00	+22.7	1.08	+17.5	45.9	-32.7
H_2/TMA/H_2	3.24	+32.3	1.37	+48.8	59.0	-13.7

This is similar to the observation in [5] where plasma H_2 is more effective in removing surface layers than N_2. It is assumed that there are more As-O bonds at the interface between HfO_2 and etched (110)-oriented layers when excluding the factor of native oxide left on etched interface. Therefore, plasma H_2 is more effective in mitigating etch damage.

2.3 Plasma processes for GaInSb surfaces

As described above, compound semiconductors may be an important enabling high mobility material to enable continued scaling of logic devices to supply voltages below 0.5 V. Antimonide based compound semiconductors (ABCS) are a particularly intriguing family of materials as they have excellent transport properties for both electrons and holes [2] and could therefore provide a solution for all III-V CMOS. $Ga_xIn_{1-x}Sb$ compounds offer the combined optimum performance for both n and p-type devices, and could facilitate the realisation of common channel inverters [2].

Described in this section are some findings from the first demonstration of the use of a clustered plasma tool to explore the effect of in situ H_2 plasma exposure, prior to high-k atomic layer deposition (ALD), on the p-$Ga_{0.7}In_{0.3}Sb$–Al_2O_3 interface.

The experimental matrix consisted of subjecting samples to variouos ICP power levels (150 W, 250 W) in the ICP-RIE chamber of the cluster tool as well as a control sample with no plasma exposure. Subsequent to plasma exposure, samples were transferred under vacuum to the ALD chamber, where 8 nm thermal Al_2O_3 was deposited at 200 °C, using TMA and H_2O. This experimental series was repeated with identical parameters, but additionally included a 600 ms TMA step (30 cycles, 20 ms TMA exposure, 3 s Ar purge), post plasma exposure, pre ALD.

Metal oxide semiconductor capacitors (MOSCAPs) were fabricated using the process flow shown in Figure 10.

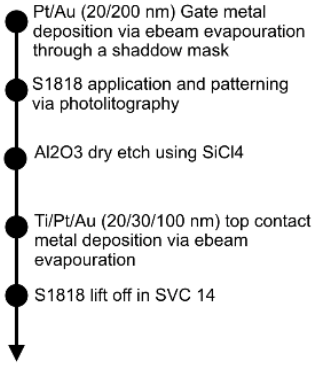

Figure 10. Process flow for MOS-capacitor fabrication

Figure 11 shows the results of frequency dependent capacitance-voltage (CV) measurements acquired at room temperature (RT) for samples treated with ICP powers up to 250 W, with and without pre ALD TMA exposure.

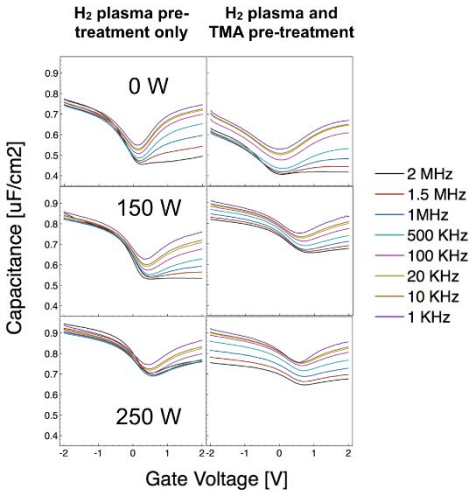

Figure 11. Room temp. frequency dependent CV measurements for samples with and without TMA pre-treatment, for control samples, and ICP powers of 150 and 250 W

These results were analysed qualitatively in terms of: capacitance modulation at 1 MHz, where $C_{mod} = C_{max}\text{-}C_{min}/C_{max}$; frequency dispersion in accumulation; and *dC/dV* at 1 kHz and are summarised in Table 2.

Table 2. Summary of capacitance modulation, frequency dispersion, and *dC/dV* for samples treated with H_2 plasma, with and without TMA exposure pre ALD. The results were acquired via room temperature, multi frequency CV measurements

Sample	ICP Power (W)	*Cmod* at 1 MHz (%)	Δ%	Freq. dispersion (1KHz to 1 MHz range)	Δ %	*dC/dV at 1kHz* (x 10^{-7} $Fcm^{-2}V^{-1}$)	Δ %
H_2 plasma only	0	36.29		1.18		3.18	
	150	33.29	-8.27	1.38	+16.95	2.37	-25.47
	250	23.84	-34.30	1.09	-7.63	1.78	-44.03
H_2 plasma / TMA	0	31.07	-14.38	5.1	+332.20	1.35	-57.55
	150	20.57	-43.32	2.37	+100.85	1.69	-46.86
	250	15.58	-57.07	3.82	+223.73	1.09	-65.72
	250 + FGA	45.3	+24.83	0.33	-72.03	4.62	+45.28

Prior to forming gas annealing, (FGA), none of the samples reached the theoretical minimum capacitance, indicating mid gap Fermi level pinning. Significant capacitance modulation was achieved however, with the control sample without pre ALD TMA exposure demonstrating a 36.29 % change. C_{mod} was found to degrade with H_2 plasma exposure for all powers investigated, and decrease with increasing ICP power. The other metrics did not show a distinct trend. The addition of the TMA exposure prior to ALD offered no improvement to any of the defined metrics, and substantially degraded the frequency dispersion in accumulation for all samples.

The RT frequency dependent CV data for the 250 W sample with pre ALD TMA exposure, post FGA, is shown in Figure 12. The FGA offered significant improvements with C_{mod} increasing by 190 %, the frequency dispersion reducing by 91 %, and the *dC/dV* slope increasing by 170 %.

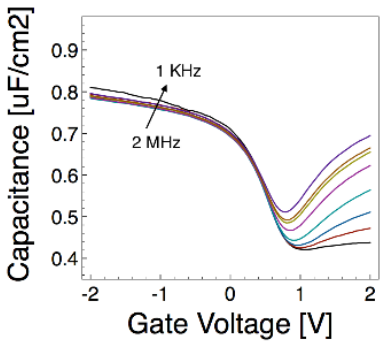

Figure 12. Multi frequency CV measurements of the 250 W sample, with TMA exposure, post 15 minute FGA at 350°C

This quality of MOS-capacitor response for a p-doped compound semiconductor material are high encouraging for common channel III-V CMOS in future, ultimately based around non-planar finfets or nanowires.

3. CONCLUSIONS

This paper shows how a set of clustered plasma deposition and etch tools enables optimization of processes for enhanced energy efficient compound semiconductor electronic devices.

Bromide-based atomic layer etching shows a great deal of promise for gate recess etching of GaN-based power electronic devices. The use of in-situ plasma processes after etching InGaAs and GaInSb materials for non-planar low voltage CMOS device realisation will likely be vital to optimization of these technologies for both logic and RF/mm-wave applications.

ACKNOWLEDGEMENTS

The work described in this paper was enabled by funding from the UK Engineering and Physical Sciences Research Council project EP/K014471/1 “Silicon Compatible GaN Power Electronics and the EU H2020 grant agreement 688684 “INSIGHT” consortium.

REFERENCES

[1] Kanarik K.J. et al., J. Vac. Sci. Technol. A 33(2), 020802, 2015
[2] Bright A.N. et al., J. Appl. Phys., 89, 3143, 2001
[3] Floros K., et al., Proc. 9th International Workshop on Nitride Semiconductors, (IWN 2016), 2016
[4] Li X. et al, to be presented at ISPlasma17, March 2017
[5] Yun Y. el al., J. Vac. Sci. Technol. A, 18, 2822, 2000
[6] Yuan Z. et al., Symposium of VLSI Technology, 96, pp185-186, 2012