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A Study of Recent Contributions on Simulation Tools for Network-on-Chip(NoC)

Muthana Saleh Alalaki, Michael Opoku Agyeman

Department of Computing and Immersive Technologies
The University of Northampton, UK
Michael.OpokuAgyeman@northampton.ac.uk

Abstract

The growth in the number of Intellectual Properties(IPs) or the number of cores on the same chip becomes a critical issue in System-on-Chip (SoC) due to the intra-communication problem between the chip elements. As a result, Network-on-Chip (NoC) has emerged as a new system architecture to overcome intra-communication issues. New approaches and methodologies have been developed by many researchers to improve NoC. Also, many NoC simulation tools have been proposed and adopted by both academia and industry. This paper presents a study of recent contributions on simulation tools for NoC. Furthermore, an overview of NoC is covered as well as a comparison between some NoC simulators to help facilitate research in on-chip communication.

Keywords: *Network-on-Chip(NoC), System-on-Chip(SoC), Embedded Systems, Computer Architecture.*

I. INTRODUCTION

The significant improvement in scaling and nano scale technologies will make it possible to build a System-On-Chips(SoCs) with billions of transistors and hundreds of cores [1][2][3][4]. Thus, a significant new application development in the field of consumer electronics, telecommunications, and system platforms are expected[5]. On the other hand, these systems will need powerful communication architectures in order to achieve different purposes. Moreover, these architectures should provide templates reusability to reduce the cost involving in design productivity [6]. The current SoCs, where the sustainable communication templates used, primarily depend on the bus approach which includes either a hierarchy of buses or a single shared bus [7].

On the other hand, this approach has faced additional constraints which restrain the future of SoCs.

Firstly, the operating frequency of buses reduces the growth in the number of cores connected. Secondly, low-level scalability with the system size when using a hierarchy of buses of a single shared bus. Thirdly, the energy consumption increases when the wire length increases with increase in circuit size. Finally, only one communication is allowed at a time by a bus or even in a hierarchic bus architecture [8].

To achieve the major requirements of future SoC such as scalability, reusability, parallelism while dealing with clock distribution and power constraints, a new paradigm, which is called Network-on-Chip(NoCs), has emerged[9]. It is a switching network which has been proposed as an alternative to interconnected cores in SoCs[10][11]. This paper conducts a study of recent contributions of simulation tools for NoC.

The rest of the paper is structured as follows: Section II provides an overview of the NoC concepts. Section III discusses the recently proposed simulation tools forNoCs, and Section IV concludes the paper.

II. NETWORK-ON-CHIP (NOC)

Network-on-Chip (also known as packet-switched on-chip interconnection networks) is one of the agitated approaches in on-chip communication. NoCs are multi-hop interconnections networks that are integrated on one single chip [12][13][14][15]. Table 1 shows a qualitative comparison between NoCs and conventional Buses. NoC consists of a number of routers which are structurally interconnected by point-to-point channels as shown in figure 1. Each of these routers is connected to its neighbor as well as a processing core using a set of ports (known as local ports or terminals) [1].

Table I: NoC and Buses Comparison [16]

NoCs	**Buses**
Upgrading is significant for designers to develop anew concept.	Simple and understandable concept.
The bandwidth increases with the network size	Limitation of bandwidth and all elements are sharing it.
Distributed routing decisions.	Blockages due to delays generated by arbitrations at the bus especially when the number of masters is significant.
Good and fast test coverage.	Slow and problematic regarding testing.
Delay transitions can be used by the data transfer because it has point-to-point connections.	Managing the time is difficult.
Point-to-point interconnections of each element for all sizes of the network and the local performance is not degraded when scaling.	Parasitic capacitance will be added by each item which increases the electrical performance degradation.

The model of communication in NoC is called message passing because each the processing cores connected to the network ports are communicating by exchanging messages and each of these messages consists of aheader, payload, and trailer.

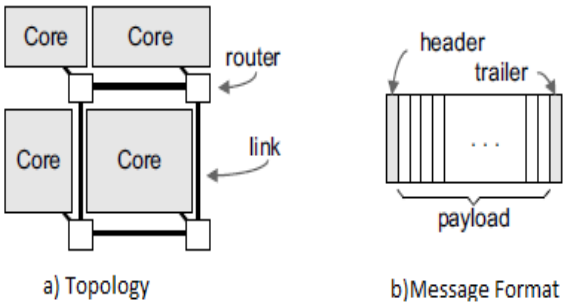

Figure 1: NoC Concepts [1]

NoC can be characterized by its topology as well as various strategies used for routing, switching, flow control, buffering and arbitration. The network topology describes how nodes and channels are arranged into agraph and the routing describes the process of choosing a path in the graph for each message. Flow control contends with the channel capacity, and switching is the technique of removing the data from the input channel to the output channel. The scheduling task of the use of channel is managed by the arbitration while the unscheduled messages are stored by the buffering task[17][18].

A. Topologies

The topologies of NoCs are significant when designing NoCs because the design of any router is based on it. Many topologies have been categorized into regular and irregular depending on the distribution process of routers within the network [9]. The most well-known topologies are mesh, torus, binary tree, ring, bus, butterfly, etc. (Figure 3)[19][20]:

a) ***Mesh***: it consists of a number of columns and rows where routers are located in the intersection between to links and the computational resources are close to the routers.

b) ***Torus***: it is a basic mesh network with some improvements where the heads and the tails of the columns are connected and the leftand right sides of the rows are connected as well. As a result, it requires more minimal routers and has better path diversity compared to themesh network.

c) ***Tree***: in this topology, nodes represent the routers and leaves represent the computational resources.

d) ***Butterfly***: it is a unidirectional (packets are routed from the left side which is the input to the right side which is the output) or bidirectional (all the inputs and outputs are located on the same side) and it uses a deterministic routing.

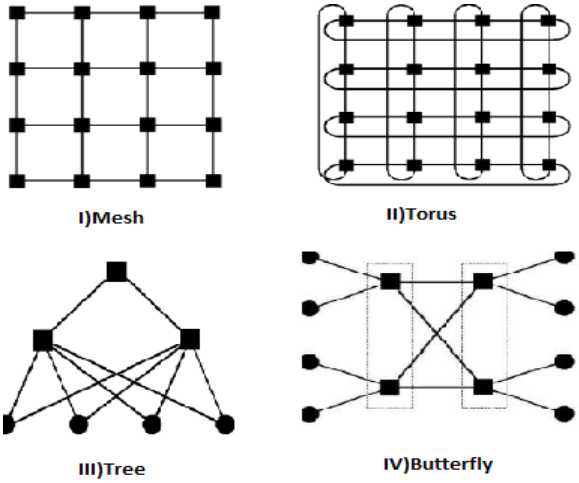

Figure 2: NoC Topologies

B. NoC Architecture

NoC normally consists of at least three fundamental elements [10][21]. Network adapters (known as Network Interface) are used to connect cores to the NoC and convert the bus protocol (used by Processing Elements) into network protocol (used by switches). Routing nodes are used to direct packets from source to destination based on the chosen protocol and they contain the routing strategies. Links which links the routing nodes and providing the bandwidth. They consist of one or more than one logical or physical channels for data transmission as well as connectivity between Network adapters and routing nodes and between the routing nodes themselves.

C. Routing

Routing is the transmission of data (packets) from source to destination using defined routing strategies. In literature, the routing schemes have been classified based on several criteria[22][23]. Source routing is a schema where the source node chooses the entire path before sending the packet to the destination. The main disadvantage of this approach is that the packet size will be increased because each one of the packets should carry the routing information through the transmission. Furthermore, the path cannot be updated or changed once the packet left the source. To solve this problem, Distributed routing is used where the routing table is accessed to determine the next hop(router) to forward the packet.

On the other hand, routing algorithms are also classified based on making the decision to choose certain paths among a set of available paths into deterministic, adaptive and oblivious. The source and destination address completely determine the path between which is the deterministic routing algorithm. The state of the network is important to make the routing decisions which is the adaptive routing algorithm. The better data flow can be achieved with this algorithm but it might generate complicated nodes[24][25]. In oblivious routing algorithm, the state of the network is not necessary to choose the route between the source and destination nodes. There are some other routing algorithms proposed in [26][27][28][29], but the main purpose of this paper is to present a study simulation tools, not the routing algorithms.

III. NoC SIMULATION TOOLS

The NoC design space is high dimensional and very large and includes topology optimization, congestion control methodologies, routing algorithms, thenumber of buffers, link capacities, and virtual channels per link, etc. In addition, the research area is expanding, which means more ideas, techniques as well as new architectures, are and will be proposed. Thus, the demand for simulation tools for evaluating different features of different NoCs proposals and designs increases. In this section, we have explained different simulation tools for NoC. Table II shows acomparison between these simulators and other well-known simulation tools.

A. BookSim

BookSim is a cycle-accurate and detailed simulator designed for NoCs as well as modeling interconnection networks for different systems. The first version of it is called BookSim1 which was a generic simulator and not designed for anon-chip environment in specific. It has been used to study different network designsincluding routing, topology, flow control, quality-of-services, router microarchitecture as well as some new technologies like nanophotonic[30][31]. In terms of system simulation, it provides the required flexibility in high-level simulation tools. With regard to network design, all key elements of a network router detailed modeling are provided by BookSim. Furthermore, it is intended to facilitate the modifications and addition of brand new network features. On the other hand, some of the topologies and advanced features proposed for on-chip networks are not supported by original BookSim. Thus, BookSim2 is developed to break the limitations as well as provides models of inter-router channel delay, traffic models, router microarchitecture, highly accurate network model and actual hardware behavior[32].

B. DARSIM

DARSIM is a cycle-level, parallel and a highly configurable simulator for Network-on-Chip as well as supports different virtual channel (VC) allocation and various routing algorithms due to its extremely parametrized table-based design. It can be driven by application traces or synthetic patterns or a built-in MIPS-based multicore simulator. Moreover, it is a parallel (multithreaded) simulation engine that split the tasks equally between the available processor cores as well as cycle accurate precision. Furthermore, it offers periodic synchronization and permitting tradeoffs between high speed and perfect accuracy. In addition, most of the hardware parameters can be configured including bandwidth, geometry, pipeline depth and crossbar dimensions[33].

C. Gem5

Gem5 is one of the emerged simulators that overcome most of thelimitations that faced the Computer architecture researchers. It is available for many researchers with a wide range of systems evaluation capabilities as well as clean interface and modularity commitment. In [34], its infrastructure is a combination of the best features of both GEMS [35] and M5 simulator[36]. That means it supports most the features of these two simulators such as multiple ISAs, highly configurable, diverse CPU models from M5 and flexible, detailed system, including multiple cache coherence protocols as well as interconnect models from GEMS. In addition, it supports various commercials ISAs (ALPHA, MUPS, ARM, SPARK, X86, and Power), involving booting Linux on ALPHA, x86, and ARM. Moreover, high level of collaboration is one the aspects of this simulator provided by thegem5 community because it is acommunity-led project and open source. Furthermore, additional features such as Parallelization and a first-class power model which might be added soon, many versions of Gem5 simulator have emerged such as gem5-gpu[37] and Gem5v [38].

D. NOXIM

Noxim simulator is developed using a C++ system description library called SystemC. The reason behind choosing SystemC is the essential aim of Noxim project which includes scalable performance and allowing expansion easiness while thecycle-accurate simulation is still maintained[39]. It also supports several parameters of the configuration space which are the workload, topology and structure, simulation and dynamic behavior. In addition, it is an open source simulator with the capabilities of cycle accurate platform, performance analysis and power figures of both emerging Wireless NoC (WiNoC) and conventional wired based NoC[40]. Although it only supports mesh topology, it supports various traffic patterns, different routing algorithm, hotspot injection, as well as

Simulator	Year	Benchmark	Framework	Open-source	Topologies	Heterogeneous support	GUI	Synchronous /asynchronous	Ref
BookSim	2010	-	C++	+	Many	-	-	Synchronous	[32]
DARSIM	2010	+	C++	+	All	-	-	Synchronous	[33]
Gem5v	2015	+	C++	+	Many	-	-	Synchronous	[38]
NOXIM	2010	-	SystemC	+	Mesh	+	-	Synchronous	[40]
HNOCS	2013	-	OMNet++	+	All	+	+	Both	[41]
Gpnocsim	2007	-	Java	+	All	-	-	Synchronous	[42]
gem5-gpu	2015	+	C++	+	All	+	-	Synchronous	[37]
AdapNoC	2016	-	C++	-	Mesh Torus (virtualized)	-	-	Synchronous	[43]
ENoCS	2015	-	Java	+	Many	+	+	Synchronous	[44]
MPSoCSim	2015	+	SystemC	+	Mesh	+	+	Synchronous	[45]
DART	2014	+	SystemC	+	All	+	+	Synchronous	[46]
Sniper	2015	+	SystemC	+	Many	+	+	Synchronous	[47]

simple source code[48]. In [40], A new version of this simulator has proposed which supports heterogeneous wired/wireless NoC architectures. Furthermore, Access Noxim is a modified version of the original NoC that supports 3D NoC system, Beltway routing, adaptive routing (Proactive thermal budget and Thermal-aware buffer allocation[49])[50].

E. HNOCS (Heterogeneous Network-on-Chip Simulator)

It is considered as the first introduced heterogeneous NoCs simulator to provide modeling of HNoCs with different link capacities as well as the number of virtual channels per unidirectional port and it is based on OMNeT++ [32]. This simulator supports parallelism (by changing the link to unidirectional), different Quality-of-Service (QoS) mechanisms, various arbitrary technologies, many routing protocols as well as power estimation. It supports three types of routers which are asynchronous, synchronous and synchronous virtual output queue (VoQ). In addition, it is open source, fully parameterized, scalable, modular and extendable for NoC. Moreover, sufficient set of statistical measurements is provided at the packet level and the flit such as throughput, end-to-end delay, transfer latencies, VC acquisition latencies, etc.[41].

F. Sniper

Sniper is one of the multi-core simulators based on Graphite simulation infrastructure and the interval core model. It is considered to become the next generation high speed, parallel and accurate X86 simulator for different heterogeneous and homogeneous multi-core architectures. The primary feature of this simulator is the core model which is depended on interval simulation. It is highly recommended for uncore as well as system-level studies which need more details compared to the traditional one-IPC models. SPLASH-2 benchmarks have been used to evaluate the performance and scalability of this simulator. As an added feature, it provides Python and SimAPI interfaces for controlling and monitoring its behavior at runtime[47].

IV. CONCLUSION

In this paper, we have presented an overview ofNoC concepts which is significant in SoCs design. Furthermore, a study of the key but recent simulation tools dedicated for NoC is provided. Particularly, the paper highlights a comparison of the simulation tools to help researchers and developers to decide on the most suitable simulation tool for their research proposals and designs.

REFERENCES

[1] C. Zeferino and A. Susin, "SoCIN: a parametric and scalable network-on-chip," in *Integrated Circuits and Systems Design, 2003. SBCCI 2003. Proceedings. 16th Symposium on*, Itajai, 2003.

[2] M. O. Agyeman, Q.-T. Vien, A. Ahmadinia, A. Yakovlev, K.-F. Tong and T. S. T. Mak, "A Resilient 2-D Waveguide Communication Fabric for Hybrid Wired-Wireless NoC Design.," *IEEE Trans. Parallel Distrib. Syst.*, vol. 28, no. 2, pp. 359-373, 2017.

[3] N. Genko, D. Atienza, G. D. Micheli, L. Benini, J. Mendias, R. Hermida and F. Catthoor, "A novel approach for network on chip emulation," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, Bologna, 2005.

[4] M. O. Agyeman, A. Ahmadinia and A. Shahrabi:, "Heterogeneous 3D Network-on-Chip Architectures: Area and Power Aware Design Techniques," *Journal of Circuits, Systems, and Computers*, vol. 22, no. 4, p. , 2013.

[5] P. C. Diniz, Reconfigurable Computing: Architectures, Tools and Applications, Mangaratiba: Springer Science & Business Media, 2007.

[6] S. Kumar, A. Jantsch, J.-P. Soininen, M. Forsell, M. Millberg, J. Oberg, K. Tiensyrja and A. Hemani, "A network on chip architecture and design methodology," in *VLSI, 2002. Proceedings. IEEE Computer Society Annual Symposium on*, Pittsburgh, 2002.

[7] E. Salminen, V. Lahtinen, K. Kuusilinna and T. Hamalainen, "Overview of bus-based system-on-chip interconnections," in *Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on*, Phoenix-Scottsdal, 2002.

[8] R. Hofmann and B. Drerup, "Next Generation CoreConnect (TM) Processor Local Bus architecture," in *Annual IEEE International ASIC/SOC Conference*, Rochester, 2002.

[9] M. O. Agyeman and A. Ahmadinia, "Power and area optimisation in heterogeneous 3D networks-on-chip architectures," *SIGARCH Computer Architecture News*, vol. 39, no. 4, p. , 2011.

[10] M. O. Agyeman, A. Ahmadinia and N. Bagherzadeh, "Performance and Energy Aware Inhomogeneous 3D Networks-on-Chip Architecture Generation," *IEEE Trans. Parallel Distrib. Syst.* , vol. 27, no. 6, pp. 1756-1769, 2016.

[11] M. O. Agyeman, A. Ahmadinia and A. Shahrabi, "Efficient routing techniques in heterogeneous 3D Networks-on-Chip," *Parallel Computing*, vol. 39, no. 9, 2013.

[12] J. Henkely, W. Wolfz and S. Chakradhary, "On-chip networks: A scalable, communication-centric embedded system design paradigm," in *VLSI Design, 2004. Proceedings. 17th International Conference on*, Princeton, 2004.

[13] L. Benini and D. Bertozzi, "Network-on-chip architectures and design methods," in *IEE Proceedings - Computers and Digital Techniques*, 2005.

[14] M. O. Agyeman, "A Study of Optimization Techniques for 3D Networks-on-Chip Architectures for Low Power and High Performance Applications," *International Journal of Computer Applications*, vol. 121, no. 6, 2015.

[15] M. O. Agyeman, "Michael Opoku Agyeman. Article: A Low Overhead Fault Reporting Scheme for Resilient 3D Network-on-Chip Applications," *Communications on Applied Electronics* , vol. 2, no. 4, pp. 43-48, 2015.

[16] P. Guerrier and A. Greiner, "A gentic architecture for on-chip packet-switched interconnections," in *Design, Automation, and Test in Europe*, New York, 2000.

[17] G. D. Micheli, C. Seiculescu, S. Murali, L. Benini, F. Angiolini and A. Pullini, "Networks on Chips: From research to products," in *Design Automation Conference (DAC), 2010 47th ACM/IEEE*, Lausanne, 2010.

[18] A. Agarwal, C. Iskander and R. Shankar, "Survey of Network on Chip (NoC) Architectures & Contributions," *Journal of Engineering,Computing and Architecture* , vol. 4, no. 1, 2009.

[19] N.Ashokkumar, P. Nagarajan and S.Ravanaraja3, "Survey Exploration of Network-on-Chip Architecture," Dindigul, 2009.

[20] G. D. Micheli and L. Benini, Networks on Chips: Technology and Tools, Academic Press, 2006.

[21] T. Bjerregaard and S. Mahadevan, "A survey of research and practices of Network-on-chip," *ACM Computing Surveys (CSUR)* , vol. 38, no. 1, 2006.

[22] G. Ascia, V. Catania, M. Palesi and D. Patti, "Implementation and Analysis of a New Selection Strategy for Adaptive Routing in Networks-on-Chip," in *IEEE TRANSACTIONS ON COMPUTERS*, 2008.

[23] P. Pande, C. Grecu, A. Ivanov, R. Saleh and G. D. Micheli, "Design, synthesis, and test of networks on chips," *IEEE Design & Test of Computers*, vol. 22, no. 5, pp. 404 - 413, 2005.

[24] A. B. Achballah and S. B. Saoud, "A Survey of Network-On-Chip Tools," *International Journal of Advanced Computer Science and Applications(IJACSA)*, vol. 4, no. 9, 2013.

[25] M. O. Agyeman and W. Zong, "An Efficient 2D Router Architecture for Extending the Performance of Inhomogeneous 3D NoC-Based Multi-Core Architectures," in *International Symposium*

on Computer Architecture and High Performance Computing Workshops (SBAC-PADW), 2016.

[26] G.-M. Chiu, "The Odd-Even Turn Model for Adaptive Routing," *IEEE TRANSACTIONS ON PARALLEL AND DISTRIBUTED SYSTEMS*, vol. 11, no. 7, pp. 729 - 738, 2000.

[27] B. B. Sayankar, P. Agrawal and S. S. Dorle, "Routing Algorithms for NoC Architecture: A Relative Analysis," in *6th International Conference on Emerging Trends in Engineering and Technology*, Nagpur, 2013.

[28] Y. Dong, Z. Lin and T. Watanabe, "An efficient hardware routing algorithms for NoC," in *IEEE Region 10 Conference*, Fukuoka, 2010.

[29] M. O. Agyeman and A. Ahmadinia, "An adaptive router architecture for heterogeneous 3D Networks-on-Chip," in *NORCHIP*, 2011.

[30] Y. Pan, P. Kumar, J. Kim, G. Memik, Y. Zhang and A. Choudhary, "Firefly: illuminating future network-on-chip with nanophotonics," in *Proceedings of the 36th International Symposium on Computer*, 2009.

[31] N. Jiang, J. Kim and W. J. Dally, "Indirect adaptive routing on large scale interconnection networks," in *Proceedings of the 36th International Symposium on Computer Architecture,*, 2009.

[32] N. Jiang, J. Balfour, D. U. Becker, B. Towles, W. J. Dally, G. Michelogiannakis and J. Kim, "A detailed and flexible cycle-accurate Network-on-Chip simulator," in *Performance Analysis of Systems and Software (ISPASS), 2013 IEEE International Symposium on*, Austin, 2013.

[33] M. Lis, K. S. Shim, M. H. Cho, P. Ren, O. Khan and S. Devadas, "DARSIM: a parallel cycle-level NoC simulator," in *IEEE Asian Solid-State Circuits Conference*, Saint Malo, 2010.

[34] N. Binkert, B. Beckmann, G. Black, S. K. Reinhardt, A. Saidi, A. Basu, J. Hestness, D. R. Hower, T. Krishna, S. Sardashti, R. Sen, K. Sewell, M. Shoaib, N. Vaish and D. A. Wood, "The gem5 Simulator," *ACM SIGARCH Computer Architecture News* , vol. 39, no. 2, pp. 1-7, 2011.

[35] D. J. S. B. M. B. M. R. M. M. X. A. R. A. K. E. M. M. D. H. a. D. A. W. Milo M.K. Martin, "Multifacet's General Execution-driven Multiprocessor Simulator (GEMS) Toolset," *Computer Architecture News (CAN)*, vol. 33, no. 4, pp. 92 - 99, 2005.

[36] N. L. Binkert, R. G. Dreslinski, L. R. H. K. T. Lim, A. G. Saidi and S. K. Reinhardt, "The M5 Simulator: Modeling Networked Systems," in *IEEE Micro*, 2006.

[37] J. Power, J. Hestness, M. S. Orr, M. D. Hill and D. A. Wood, "gem5-gpu: A Heterogeneous CPU-GPU Simulator," *IEEE Computer Architecture Letters*, vol. 14, no. 1, pp. 34 - 36, 2014.

[38] S. H. Nikounia and S. M. author, "Gem5v: a modified gem5 for simulating virtualized systems," *The Journal of Supercomputing*, vol. 71, no. 4, p. 1484–1504, 2015.

[39] M. Amoretti, "Modeling and Simulation of Network-on-Chip Systems with DEVS and DEUS," *ScientificWorldJournal*, 2014.

[40] V. Catania, A. Mineo, S. Monteleone, M. Palesi and D. Patti, "Noxim: An Open, Extensible and Cycle-accurate Network on Chip Simulator," in *Application-specific Systems, Architectures and Processors (ASAP), 2015 IEEE 26th International Conference on*, Toronto, 2015.

[41] Y. Ben-Itzhak, E. Zahavi, I. Cidon and A. Kolodny, "HNOCS: Modular open-source simulator for Heterogeneous NoCs," in *Embedded Computer Systems (SAMOS), 2012 International Conference on*, Samos, 2013.

[42] H. Hossain, M. Ahmed, A. Al-Nayeem, T. Z. Islam and M. M. Akbar, "Gpnocsim - A General Purpose Simulator for Network-On-Chip," in *Information and Communication Technology, 2007. ICICT '07. International Conference on*, Dhaka, 2008.

[43] P. W. Viglucci and A. Carpenter, "ENoCS: An Interactive Educational Network-on-Chip Simulator," in *ASEE Annual Conference & Exposition*, New Orleans, 2016.

[44] P. Wehner, J. Rettkowski, T. Kleinschmidt and D. Göhringe, "MPSoCSim: An extended OVP Simulator for Modeling and Evaluation of Network-on-Chip based heterogeneous MPSoCs," in *Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS)*, Samos, 2015.

[45] D. Wang, C. Lo, J. Vasiljevic, N. E. Jerger and G. Steffan, "DART: A programmable architecture for NoC simulation on FPGAs," *IEEE Transactions on Computers*, vol. 63, no. 3, pp. 664 - 678, 2014.

[46] T. Carlson, W. Heirman and L. Eeckhout, "Sniper: Exploring the Level of Abstraction for Scalable and Accurate Parallel Multi-Core Simulation," Intel Labs Europe, 2015.

[47] K. Swaminathan, D. Thakyal, S. G. Nambiar, G. Lakshminarayanan and S.-B. Ko, "Enhanced Noxim Simulator for Performance Evaluation of Network on Chip Topologies," in *Engineering and Computational Sciences (RAECS), 2014 Recent Advances in*, Chandigarh, 2014.

[48] H.-Y. Wang, C.-H. Chao, T.-C. Yin and A.-Y. Wu, "Buffer Depth Allocation for Thermal-Aware 3D Network-on-Chip Design," in *Routing Algorithms in Networks-on-Chip*, Springer, 2013, pp. 307-338.

[49] K. Manna, S. Chattopadhyay and I. Sengupta3, "Through silicon via placement and mapping strategy for 3D mesh based Network-on-Chip," in *Very Large Scale Integration (VLSI-SoC), 2014 22nd International Conference on*, Playa del Carmen, 2014.

[50]