# MMC with Parallel-connected MOSFETs as an Alternative to Wide Bandgap Converters for LVDC Distribution Networks

Yanni Zhong*, Nina M. Roscoe, Derrick Holliday, Stephen J. Finney

Department of Electronics and Electrical Engineering, University of Strathclyde, UK
*yanni.zhong@ieee.org

**Abstract:** LVDC networks offer improved conductor utilisation on existing infrastructure and reduced conversion stages, which can lead to a simpler and more efficient distribution network. However, LVDC networks must continue to support AC loads, requiring efficient, low distortion DC-AC converters. In addition, there are increasing numbers of DC loads on the LVAC network requiring controlled, low distortion, unity power factor AC-DC converters with increasing capacity, and bi-directional capability. An efficient AC-DC/DC-AC converter design is therefore proposed in this paper to minimise conversion loss and maximise power quality. A comparative analysis is carried out for a conventional IGBT 2-level converter, a SiC MOSFET 2-level converter, a Si MOSFET MMC and a GaN HEMT MMC, in terms of power loss, reliability, fault tolerance, converter cost, and heatsink size. The analysis indicates that the 5-level MMC with parallel-connected Si MOSFETs is an efficient, cost effective converter for LV converter applications. MMC converters suffer negligible switching loss, which enables reduced device switching without loss penalty from increased harmonics and filtering. Optimal extent of parallel connection for MOSFETs in an MMC is investigated. Experimental results are presented for current sharing in parallel-connected MOSFETs, showing reduction in device stress and EMI generating transients through the use of reduced switching.

## 1. Introduction

There have been reported cases of distribution networks operating close to their capacity limits [1]. DC networks are being suggested as a means of addressing the issue of converter rich AC networks and improving conductor utilisation, thus increasing network capacity using existing infrastructure. Reports state that LVDC technology could provide large power capacities without replacing the existing cables [2-4]. Furthermore, LVDC networks present the additional benefit of no reactive power flow and allow reduction in the number of conversion stages [5-7]. However, these systems will retain the need to supply local AC loads which must be provided by DC-AC converters meeting the same stringent performance criteria outlined above for AC-DC converters supplying DC loads such as EVs. Issues of power quality also affect LVDC networks and are complicated by the need to supress DC harmonics associated with single-phase loads and to have resilience to DC network faults.

Meanwhile, increasing load demands, distributed generation (DG), and the growing use of electricity for heating and vehicle transport contribute significant strains on existing LVAC distribution networks [1]. These increasing numbers of DC loads require controlled low distortion, unity power factor AC-DC converters with increasing capacities as well as bi-directional capacity. In the UK, statistics show that full penetration of electric vehicles (EVs) is predicted to increase total electricity consumption by

approximately 50% [8]. EV chargers present much high power loads operating at higher frequency and higher voltage than the existing numerous lighter power electronic loads (such as PC's, phone chargers etc), driving a need to facilitate the adoption of high performance converters capable of handling high power, frequency and voltage. These loads must be supplied whilst meeting strict harmonic limits and avoiding issues of circulating currents and control band oscillations associated with power electronic rich networks. This growth drives a critical need for improved converter performance in terms of efficiency, power quality and control.

The consequent numbers of converters required, when LVDC networks are combined with high numbers of EVs, further increases the pressure to improve converter efficiency as losses from thousands of converters accumulate, and underlines the imperative to meet strict harmonic standards to ensure continued grid stability [9-11]. To date, higher power applications have been met using two-level IGBT inverters, however IGBT devices are now at the limit of performance. Two solutions can be proposed for this. Wide Bandgap (WBG) devices are now available with appropriate voltage and power ratings. The exploitation of WBG fast switching behaviour can be used to increase modulating frequency while simultaneously increasing efficiency compared with IGBT. Higher modulating frequency in turn allows smaller, lower loss filters. Basic circuit topology remains unchanged but the devices are expensive and their high speed can introduce EMI issues [12]. Gate drivers for very fast switching devices can also be challenging to implement [13]. Alternatively, improved control and power quality can be facilitated at lower switching frequency by improvements in the converter output waveform, by using a stepped waveform such as that generated the Modular Multi-Level (MMC) topology. A stepped waveform reduces the harmonic content of the output current and voltage, which allows a reduction in filter size and complexity and leads to reduced VAR consumption, simplified control, reduced circulating harmonic/reactive current, greater stability and less filter damping loss.

Multi-level converters allow the decoupling of power quality and device switching frequency. They offer the potential to drive down conversion loss but have received little attention at low voltage due to the apparent increase in complexity. This paper will investigate the potential benefits and limitations of multi-level techniques in comparison to the extension of two level converters through the use of WBG devices.

In this study, a DC voltage of 600V is selected with 10 kW, single-phase power transfer. There are many suitable converter topologies at this voltage, each with different advantages, and hence this research aims to provide a comparison of converter topologies, comparing efficiency, volume and reliability, for converters capable of meeting strict harmonic standards. Generally, the complexity of the circuit topology and the large number of capacitors required are the main limits of using flying capacitor converters [14].

For neutral point clamped (NPC) converters, additional inverter control may be required to balance the neutral point. The losses are not equally distributed in NPC converters, thus limiting current rating by the most stressed semiconductor devices [15, 16].

Three principal converters stand out as being the most suitable, innovative solutions for this application: Si MOSFET MMC, GaN HEMT MMC and SiC 2-level [17]. Selecting which of these converters brings the best performance is non-trivial as efficiency is affected not only by semiconductor losses but also by the filtering required to meet harmonic standards. This research optimises the design of the three converters including filtering, and validates the outcome of the comparisons using experimental results for SiC and Si MOSFET. Discussion on reliability and fault tolerance differences between the three converters is also included, as well as a comparison of required heatsink volume.

Expected benefits of the LV MMC as an alternative to 2-level converters are summarised as: (1) continuous arm currents, (2) negligible switching loss, allowing slowed switching, leading to reduced dv/dt, (3) modular construction, (4) no need of a dc-side filter, (5) better output waveform quality leading to smaller AC filters, (6) negligible switching losses, and (7) the ability to prevent capacitor discharging current. The modular structure of the MMC allows the use of lower voltage rated Si MOSFETs in place of IGBTs, allowing further loss reduction through parallel-connection and synchronous rectification.

The 2-level Si MOSFET converter is excluded because a Si MOSFET (≥600 V) has a larger power dissipation than an IGBT [18, 19].

## 2. Design optimisation for low voltage converters: Si MOSFET MMC, GaN HEMT MMC and SiC 2-level

### *2.1. Operating Principle and component sizing of LV-MMC Type Converter*

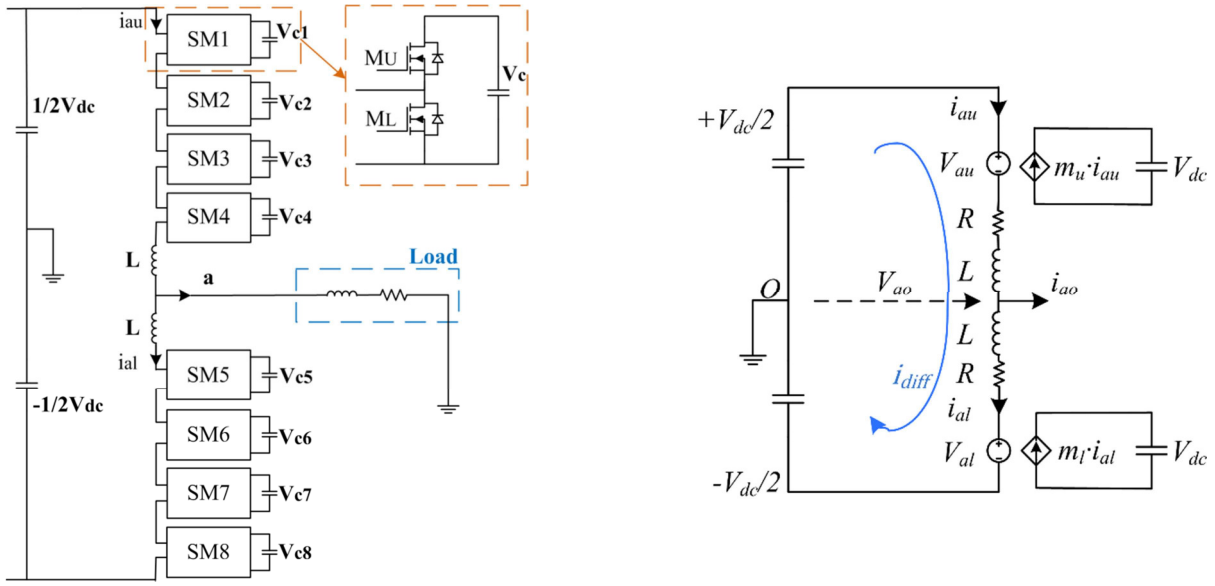
#### *A. Operating Principle*

The topology of a 5-level MMC, where four submodules and one arm inductor form one arm, is shown in Fig. 1(a). Fig. 1(b) illustrates the average model of a single phase MMC. In each arm, $R$ represents the semiconductors ohmic loss [20, 21].

This paper assumes that current suppression control eliminates all harmonics and the remaining circulating current ($i_{diff}$) has only a DC component $I_{dc}$. According to [22], arm currents can be expressed as (1) and (2), where $I_{dc}$ is the DC component of $i_{diff}$ and $i_{ao}$ is the sinusoidal output current.

$$i_{au} = i_{diff} + \frac{i_{ao}}{2} = I_{dc} + \frac{i_{ao}}{2} \quad (1)$$

$$i_{al} = i_{diff} - \frac{i_{ao}}{2} = I_{dc} - \frac{i_{ao}}{2} \quad (2)$$




(a) (b)

***Fig. 1****(a) Topology of a Si MOSFET 5-level MMC (b) Average model of an MMC*

### *B. Design of passive components (Sizing capacitors and inductors)*

To reduce MMC bulk, capacitance is set to the minimum required to stay within ±10% voltage fluctuation [23]. The submodule capacitance, $C_{sub}$, is sized based on maximum energy deviation [24] (adapted for a 2-phase-leg topology), so that submodule capacitance is given by (3) [25], where $n$ is the number of submodules in one arm, $\Delta V_{max}$ is maximum voltage difference in p.u., M is the modulation index and $|\bar{S}|$is apparent power.

$$C_{sub} = \frac{n \cdot |\bar{S}|}{2\omega \cdot M \cdot {V_{dc}}^2 \cdot \Delta V_{max}} \tag{3}$$

While current suppression control effectively reduces 2nd harmonic distortion, circulating currents at switching frequency can only be suppressed by arm inductance, since switching frequency exceeds controller bandwidth [24].

The difference between phase leg voltage and $V_{dc}$ results in circulating current. If arm currents are dominated by DC and fundamental components (1)-(2), the voltage difference $u_{diff}$ is given by (4) [20].

$$u_{diff} = \frac{V_{dc}-(v_{au}+v_{al})}{2} = \frac{n}{8C_{sub}}\left\{-\frac{3}{4\omega}M \cdot I_{ao} \cdot \sin(2\omega t - \varphi) + \frac{1}{\omega}M^2 I_{dc} \cdot \sin(2\omega t)\right\} \tag{4}$$

Peak-to-peak circulating current at the switching frequency is given by (5).

$$I_{pp} = \frac{u_{diff}}{L_{arm}} \cdot \Delta T \tag{5}$$

$\Delta T$ is the time between switching, with its largest value equal to the inverse of switching frequency $1/f_S$, and the maximum value of $I_{pp}$ is limited to 5% of the DC side current $I_d=2I_{dc}$.

$$I_{pp\_max} = 0.05 \cdot I_d = 0.05 \cdot 2I_{dc} = 0.1I_{dc} \quad (6)$$

Minimum arm inductance is given by (7) [25].

$$L_{arm} = \frac{5n}{4\omega C_{sub} f_s} \cdot \sqrt{(M^2 - 3)^2 + 9\tan^2 \varphi} \quad (7)$$

### *2.2. Si MOSFET 5-level MMC*

According to [25], 18 mF capacitors are chosen for the 2-level converter, which is calculated from the peak to peak energy deviation. By using (3), the required $C_{sub}$ for different levels of MMC at M=0.57 (240 $V_{rms}$ output) can be obtained and the calculated losses are compared in Fig. 2.

Interestingly with increasing number of MMC levels, capacitor losses are almost constant, while semiconductor losses decrease gradually. Parallel-connection of ≥2 MOSFETs reduces conduction loss dramatically. Converter power loss calculation will be presented in Section 3.

Fig. 2 shows how converter cost increases significantly with higher converter levels, dominated by capacitor costs. Significant capacitor loss means that simply increasing the number of levels is counterproductive for efficiency, while also adding complexity, volume and cost. The 5-level MMC with parallel-connected Si MOSFETs provides the optimum balance between control complexity, losses and costs.

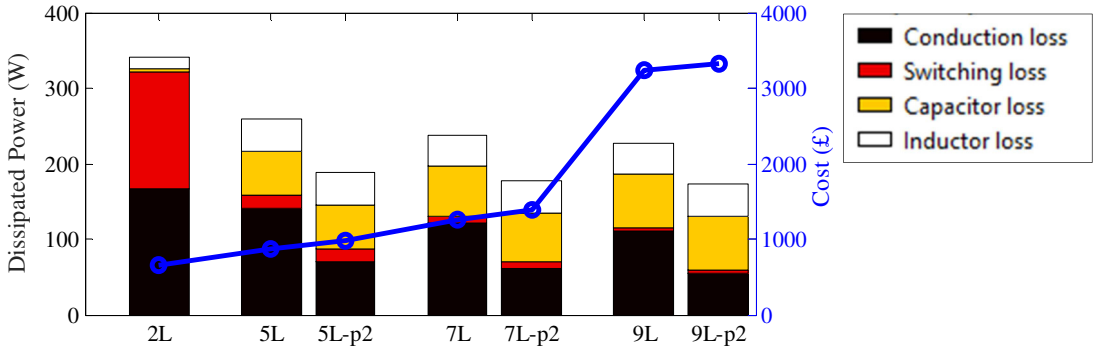



***Fig. 2*** *Power loss and cost comparison for H-bridge 2-level IGBT converter and different levels of Si MOSFET MMC at M=0.57, 10 kHz, 10 kW and unity power factor. 2L=2 level IGBT; 5L/7L/9L= 5/7/9 level MMC without parallel connection; 5L-p2/7L-p2/9L-p2= 5/7/9 level MMC with 2 parallel-connected devices*

### *2.3. GaN HEMT 3-level MMC*

Comparing available GaN HEMT devices showed that a GaN 3-level MMC using 650V GS66516T devices promises highest efficiency, as illustrated in Table 1.

### *2.4. SiC 2-level Converter*

With higher breakdown voltage [14], lower $R_{on}$ and very low diode recovery loss, SiC MOSFETs are increasingly adopted for high-efficiency. For LVDC at 600 $V_{dc}$ a 2-level converter is the most efficient SiC MOSFET topology. The 1.7 kV Cree CAS300M17BM2 device provides low $R_{on}$, as shown in Table 1.

**Table 1** Parameter comparison between different types of devices

| | SiC MOSFET | | GaN HEMT | | Si MOSFET | | |
|---|---|---|---|---|---|---|---|
| Available voltage ratings | **1.7 kV*** | 1.2 kV | **650 V*** | 100 V | 400 V | **200 V*** | 100 V |
| No. of Levels | **2-level** | 2-level | **3-level** | 9-level | 3-level | **5-level** | 9-level |
| Device | **CAS300M17BM2** | C2M0025120D | **GS66516T** | GS61008T | IRFP360 | **IRFP4668** | IRFP4110 |
| $R_{on}$ | **8 mΩ** | 25 mΩ | **27 mΩ** | 7.4 mΩ | 200 mΩ | **8 mΩ** | 3.7 mΩ |

*Devices selected in this study

## 3. Converter Power Loss Estimation

### *3.1. Semiconductor Losses*

MOSFET and GaN transistor conduction loss is given by (8), assuming synchronous rectification [26, 27].

$$P_{con} = \frac{1}{T}\int_0^T \left(i_{DS}(t)\right)^2 \cdot R_{on} dt \tag{8}$$

where $i_{DS}$ is the drain-source current. $R_{on}$ is the on-state resistance, given by (9) [28]

$$R_{on} = R_{on\_25} + k_{Ron} \cdot (T_j - 25) \tag{9}$$

where $R_{on-25}$ gives $R_{on}$ at 25°C and $k_{Ron}$ is a coefficient obtained from the datasheet.

Interpolation of SiC datasheet switching loss predicted far lower loss than experimental SiC switching loss measured by the authors. Measured SiC switching loss at 600 Vdc is presented in Section 5.1 below, and is used for all loss comparisons.

Si MOSFET and GaN transistor switching loss is given by (10) [29,30]

$$P_{SW} = \frac{1}{2} I_{DS} V_{DS} \left(t_{off} + t_{on}\right) f_s \tag{10}$$

where $t_{on}$ and $t_{off}$ are the turn-on and turn-off times respectively and are obtained from switching gate charge $Q_{SW}$ and average gate current $I_{GS}$ [31] (11) .

$$t_{on} = t_{off} = \frac{Q_{SW}}{I_{GS}} \tag{11}$$

$I_{GS}$ can be approximated by the Miller plateau gate current:

$$I_{GS} = \frac{V_{GS} - V_P}{R_g} \tag{12}$$

where $V_P$ is the Miller plateau voltage, and $R_g$ denotes total gate resistance.

Diode switching loss is :

$$P_{rr\_D} = Q_{rr} \cdot V_D \cdot f_s \tag{13}$$

### *3.2. Capacitor Loss Calculation*

At ≤400 V, electrolytic capacitors achieve small volume, but bulkier film capacitors provide low ESR. A comparison between electrolytic and film capacitors in Table 2 reveals that with film capacitors, capacitor loss is almost eliminated at a cost of increased weight and volume. Currently, lower voltage film capacitors are unavailable so parameters in the second row of Table 2 are estimates provided by API Capacitors.

**Table 2** Comparison between electrolytic and film capacitors

| | **Capacitance (μF)** | **Voltage (V)** | **Weight (g)** | **Volume (cc)** | **ESR (mΩ)** | **Part number** |
|---|---|---|---|---|---|---|
| Electrolytic | 2200 | 350 | 280 | 221 | 28 | B43456A4228M000 |
| Film | 2300 | 250 | 370 | 420 | 0.8 | Estimated by *API Capacitors** |
| | 2400 | 450 | 1985 | 1613 | 0.2 | DCHCH07240JH00KS00 |
| | 2030 | 600 | 1760 | 1480 | 1.6 | DCP6I07203ER00 |

*This product is not available for sale. Parameters are estimated by *API Capacitors* [32].

For the MMC, submodule capacitor losses in upper and lower arms are given by (14) and (15) respectively.

$$\bar{P}_{cap\_U} = \frac{1}{2\pi}\int_0^{2\pi} m_u \cdot (i_{au}^2 \cdot ESR) d(\omega t) \tag{14}$$

$$\bar{P}_{cap\_L} = \frac{1}{2\pi}\int_0^{2\pi} m_l \cdot (i_{al}^2 \cdot ESR) d(\omega t) \tag{15}$$

For the SiC 2-level converter, loss occurs in the DC-side capacitor. Using peak energy deviation [24, 25] it can be shown that the required capacitance is given by (16)

$$C_{dc} = \frac{\Delta E_{dc}}{4{V_{dc}}^2 \triangle V_{max}} \tag{16}$$

DC-side capacitor current, $i_{cap}$(t), is assumed to contain all of the ac components of the upper switch current (17).

$$i_{cap}(t) = \frac{1}{2} I_{ao} sin(\omega t - \varphi) - \frac{1}{4} M I_{ao} cos(2\omega t - \varphi) \tag{17}$$

Dc-side capacitor loss is then found from (18).

$$P_{C_{dc}} = \frac{1}{2\pi}\int_0^{2\pi} \left({i_{cap}}^2(t).ESR\right) d(\omega t) \tag{18}$$

### *3.3. Inductor Loss*

#### *A. MMC Arm Inductor Loss*

Using (10) and (14), the minimum arm inductance for a *10 kW, M=0.57, $f_s$=10 kHz, $V_{dc}$=600 V, $\Delta V_{max}$=0.1* MMC operating at unity power factor is 1.5 mH. Air-gapped Blinzinger ferrite E160/56/36 cores [33] were used to minimise inductor loss. Inductor loss is calculated using (21, 22).

$$\sqrt{{I_{dc}}^2 + \left(\frac{I_{ao}}{2}\right)^2} = 22.4\ A \tag{19}$$

$$P_{copper\_arm} = {I_{dc}}^2 R_{wire} + \frac{(I_{ao}/2)^2}{2} R_{wire} = 47.8W \tag{20}$$

Harmonic analysis calculations show that ferrite core loss may be neglected. With 4 arm inductors in total, MMC inductor loss is 192 W regardless of the number of levels.

### *B. 2-Level Converter Inductor Loss*

Analysis of single-phase 2-level converter harmonic performance showed that 1.7 mH of ac-side inductance is required to maintain harmonics below 5% of fundamental current. Blinzinger E160/56/36 cores [33] were used again. Harmonic analysis of the 2-level converter with 1.7 mH of converter-side inductance showed significant harmonics at the switching frequency of 10 kHz, and hence with skin effect, total loss in the ac-side inductor is 268 W.

In addition, to keep dc-side currents below 5% of dc input current, a dc-side inductance of 6.5 mH is required. Using the Blinzinger E160/56/36 cores again total dc-side inductor loss is estimated to be 88.5 W.

Total inductor loss for the 2-level converter is therefore 356.5 W.

## 4. Comparative Study of Converters

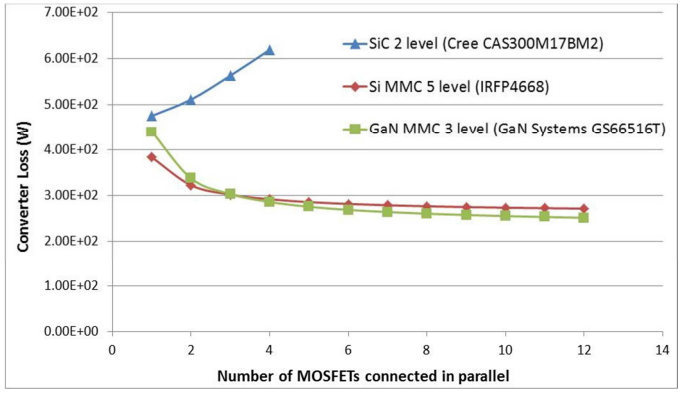
Three converter topologies based on Si MOSFET, SiC and GaN devices are proposed. Parallel-connection of switching devices is explored to reduce conduction losses and heatsink sizes are compared.

### *4.1. Power loss - Optimal Number of Parallel-Connected Devices*

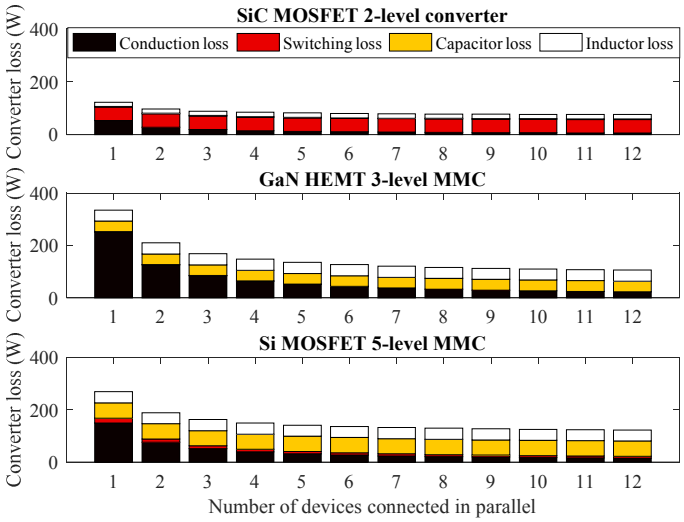
As shown in Fig. 2, parallel-connection can significantly reduce converter losses. With many parallel-connected devices, the effect of track resistance becomes more significant [30], imposing a limit on parallel-connection. In addition, this section discusses the current unbalance limits for parallel-connection.

Power losses for different numbers of parallel-connected devices are plotted in Fig. 3. Track resistance is seen to roughly limit the benefit of parallel-connection, with respect to efficiency, to four devices. With four IRFP4668 devices in parallel, total current rating is now 800 A, bringing strong potential reliability benefits to the Si MOSFET MMC in terms of device stress compared with the SiC module current limit of 300 A, and a current limit of 240 A for GaN 3-level MMC with four parallel devices.

For the MMC, low switching loss permits slower turn-on/off without undue impact on loss, enabling a lower EMI solution [27], in contrast to the SiC 2-level converter where high switching loss prohibits slow turn-on/off.




(a) Converter loss as a function of the number of parallel-connected devices




(b) Converter loss distribution as a function of the number of parallel-connected devices

***Fig. 3*** *Losses in converters with parallel-connected devices for an SiC MOSFET 2-level converter, a GaN HEMT 3-level and a Si MOSFET 5-level MMC at 10 kW, 10 kHz, 600 $V_{dc}$, M=0.57 and unity power factor*

In Fig. 3(a) the Si and GaN MMC offer lowest loss. Device packaging and footprint area impact parasitic resistance and inductance incurred by parallel-connection. For an LVDC MMC converter using Si MOSFETs all devices are available in TO-247 packaging. Laying out four TO-247 devices in the most efficient manner leads to a volume of around 16 $cm^3$ which is around 21% of the predicted heatsink volume. Hence, for around four devices in parallel, device packaging and size are a lesser concern compared with gate-drive complexity and efficiency when establishing optimal parallel-connection. For four TO-247 devices laid out efficiently and using slowed switching, gate threshold tolerances have far more impact on switching synchronisation than different gate track lengths imposed by layout, hence

efficiency dictates optimal parallel-connection for Si MOSFETs. Switch timing is experimentally investigated below.

Parallel-connection of many surface mount GaN devices may be more practical. However, currently GaN devices are expensive, and the diminishing improvement in efficiency with increased parallel-connection beyond 4-6 must be considered alongside the expense of more devices.

### *4.2. Reliability*

The luxury of being able to reduce switching speed in both Si and GaN MMC also improves reliability by allowing switching transients to be reduced and hence minimising voltage stress due to overshoot, as will be demonstrated in section 5 below. In addition, the availability of low cost, high current rating Si MOSFETs minimises current related device stress. Since device stress is a significant cause of converter failure, converter reliability seems likely to noticeably improve with the use of Si or GaN MMC, thus mitigating any reduction in reliability that can be attributed to increased complexity.

In [33], for PV applications, it is concluded that SiC offers a superior solution to Si IGBT due to a combination of lower life-cycle costs, lower part count, higher efficiency and power density. In [34], gate reliability of SiC power devices is found to be problematic, however, [35] suggests that up to date SiC devices suffer reduced gate relability issues.

GaN brings the advantage of very fast switching, but this comes at the cost of increased gate drive complexity, and increased risk of oscillation [13], both of which are likely to impact reliability. Mean time to failure for the Si MOSFET is around $1.5 \times 10^8$ hours [36], while with GaN it is around $1.9 \times 10^6$ hours [37], suggesting that the GaN power devices are less reliable.

The SiC converter contains 8 times fewer power switches than the Si MOSFET 5-level MMC, and if the reliability of both semiconductor switch types were equal, and if we ignore the reduced stresses on the devices in the MMC topology, this would equate to an improvement in reliability of 8 times. Hence, there is a complex balance required to compare the reliability of the converters. At this time, quantifying the potential reliability improvements offered by reduced voltage stress in MMC topologies and the relative impact of SiC gate reliability in 2-level converters is an area of interest which longer term industrial studies will demonstrate in time.

### *4.3. Fault tolerance*

The choice of converter topology will have implications for the fault response of LVDC networks, in particular severe pole-pole short circuits. The use of conventional 2-level converters results in rapid rise in fault current associated with the discharge of converter DC side capacitance accompanied by AC fault

contribution which builds through the converter body diodes as the DC voltage collapses below the envelope of the AC network [38]. Once the DC rail fully collapses both current components are transferred to the diode path placing significant stress on the converter power modules. Fast acting DC protection is therefore required to prevent both de-energisation of the network and damage to converters.

The impact of converter topology has seen significant research in HVDC applications. The adoption of the MMC topology can prevent the capacitive discharge component of the DC fault current, however the basic topology is still subject to fault current through the module diodes. The use of reverse blocking converters such as the full bridge and half bridge MMC have the ability to block both capacitor discharge and ac contribution to the DC fault [39]. Improved fault behaviour is achieved at the expense of additional devices and conduction loss.

MMC based converters can bring the same functionality to LVDC systems. In these cases the lower operating voltage provides greater degrees of freedom in the design. For instance, mixed device ratings may allow the use of fewer reverse blocking cells giving fault tolerance while minimising impact on overall converter loss.

An additional interesting point is that parallel-connection in MMC leads to high transient overload capacity allowing faults to trip conventional protection whilst at the same time reducing operational losses.

### *4.4. Cost*

Fig. 2 demonstrates the impact of increasing number of levels on Si MOSFET MMC cost, giving a cost of around £1000 for the parallel-connected 5-level case. For comparison, GaN 3-level MMC costs around £1150, and SiC 2-level converter around £1500. Si MOSFET MMC currently offers the lowest cost solution out of the three compared converters.

### *4.5. Thermal Design and Heatsink Sizing*

#### *A. Deriving Thermal Resistance*

Thermal design is carried out for 10 kW SiC MOSFET 2-level, GaN HEMT 3-level MMC and Si MOSFET 5-level MMC converters with four parallel-connected devices (‘3 converters’), and compared with a 10 kW IGBT 2-level converter. In order to follow the approach in [26] most thermal resistances can be obtained from the datasheet. Only the Si MOSFET datasheet provides the case-to-heatsink thermal resistance, $R_{\theta(C\text{-}S)}$, which is affected by the contact quality [40]. SiC MOSFET / GaN HEMT $R_{\theta(C\text{-}S)}$ is estimated by (21).

$$R_{\theta(C-S)SiC} = \frac{A_{Si}}{A_{SiC}} R_{\theta(C-S)Si} \tag{21}$$

where $A_{Si}$ and $A_{SiC}$ are the contact areas for the Si and SiC devices, and $R_{\theta(C\text{-}S)Si}$ is the datasheet Si MOSFET $R_{\theta(C\text{-}S)}$ [41].

To mount the optimal top-side cooled GaN HEMT device, a pedestal copper block is required [42], but the copper block has negligible thermal resistance.

### *B. Heatsink Sizing*

IGBT 2-level converter losses in one arm with $M$=0.57, $T_J$=125°C are listed in Table 3, along with required heatsink volume.

**Table 3** Heatsink sizing for the IGBT 2-level converter

| | $\mathbf{P_{arm}}$ (W) | $\mathbf{R_{\theta(J\text{-}S)}}$ (°C/W) | **Required** $\mathbf{R_{\theta(S\text{-}A)}}$ (°C/W) |
|---|---|---|---|
| **IGBT** | 59.2 | 0.51 | 0.71 |
| **Diode** | 21 | 0.61 | |
| **Heatsink** | h×w×l (mm) | Volume ($cm^3$) | Heatsink $R_{\theta(S\text{-}A)}$ (°C/W) |
| FISCHER ELEKTRONIK SK 47/100 SA | 80×200×100 | 1600 | 0.7 |

Power loss and required heatsink volume are listed in Table 4 for the '3 converters'. Despite similar loss in the GaN 3-level MMC compared to the Si 5-level converter, the small GaN transistor package leads to larger $R_{\theta(C\text{-}S)}$, and hence double the heatsink volume. Even when compared with GaN 3-level MMC, the heatsink volume required for a conventional IGBT 2-level converter is over 10 times larger.

**Table 4** Heatsink comparison between 3 converters with four parallel-connected devices (calculated for one-phase-leg). Heatsink manufacturer: FISCHER ELEKTRONIK

| **Converter Type** | $\mathbf{P_{arm}}$ | $\mathbf{R_{\theta(J\text{-}S)}}$ | **Required** $\boldsymbol{R_{\theta(S\text{-}A)}}$ | **Heatsink Part No.** | $\boldsymbol{R_{\theta(S\text{-}A)}}$ | **Volume** |
|---|---|---|---|---|---|---|
| SiC MOSFET 2-level | 33.1 W | 0.072 °C/W | 2.95 °C/W | SK 81/ 75 SA | 2.5 °C/W | 112.5 $cm^3$ |
| GaN 3-level MMC | 32.1 W | 0.68 °C/W | 2.44 °C/W | SK 81/ 100 SA | 2.1 °C/W | 150 $cm^3$ |
| Si MOSFET 5-level MMC | 24.4 W | 0.53 °C/W | 3.57 °C/W | SK 81/ 50 SA | 3.0 °C/W | 75 $cm^3$ |

## 5. Experimental Results and Analysis

### *5.1. Thermal Measurement for the Validation of Power Loss Calculation*

### *A. Experimental validation of Si MOSFET loss calculation*

Measurement of loss in the complete MMC is not practical, so loss in a single MMC module operating at fixed 50% duty cycle was measured instead. Loss was measured by firstly calibrating heat rise on the heatsink as a function of dissipated power by passing DC power through the Si MOSFET switches to calibrate temperature rise as a function of power loss in the switches. The experimental test rig is shown in Fig. 4, containing a single Si MOSFET MMC module with an R-L load, at 100 $V_{dc}$ and 1-20A AC-side load current range, using IRFB4127PbF MOSFETs.

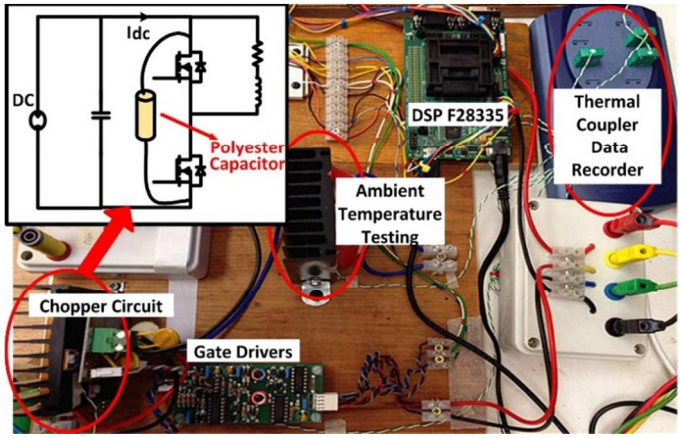



***Fig. 4*** *Experimental test rig for power loss measurement*

Fig. 5 shows the estimated and measured power dissipation for synchronous and non-synchronous rectification cases, highlighting the benefit that synchronous rectification brings for MOSFETs. Track resistance power losses are included since device on-resistance is now so low that track resistance becomes relevant in a prototype such as was available during this study [27]. Fig. 5 shows that measured and calculated losses agree closely, validating the power loss calculation in Section 3.

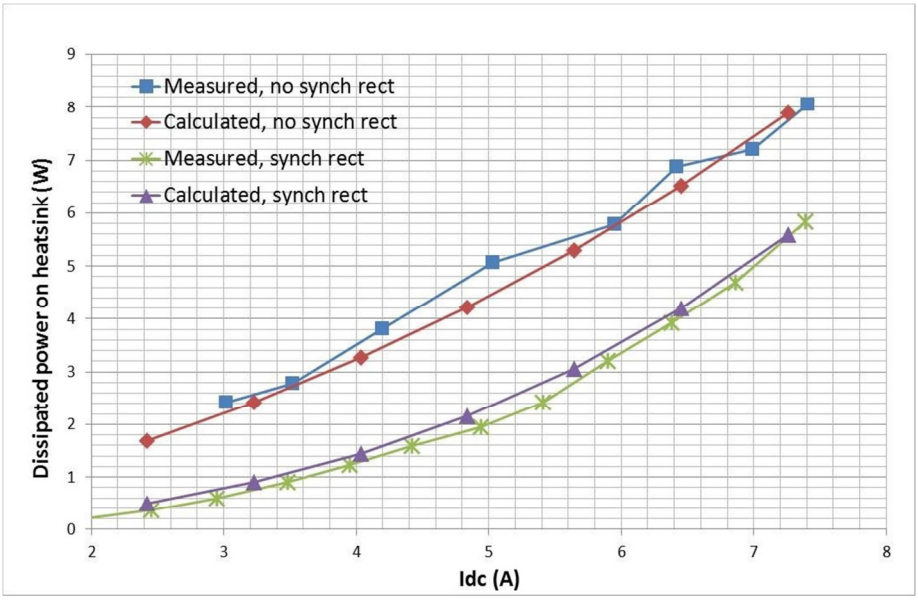



***Fig. 5*** *Heat dissipation for one MMC submodule with and without synchronous rectification, allowing for track resistance*

### *B. Experimental measurement of SiC MOSFET loss*

SiC losses were compared with losses calculated using interpolation from datasheet switching loss. Heat rise for this large SiC module was found to be too small to measure accurately, however, smooth and relatively slow switching (compared with Si MOSFETs) allowed accurate determination of losses using conventional voltage and current measurements. Switching loss as a function of current is presented in Fig. 6, showing little variation in switching loss with load current at these low load currents. This is due to the

dominance of capacitance effects in SiC switching loss [43]. For accurate loss comparison with Si MOSFET devices measured switching loss was used to calculate SiC 2-level converter efficiency. Conduction loss was found to agree with calculation.

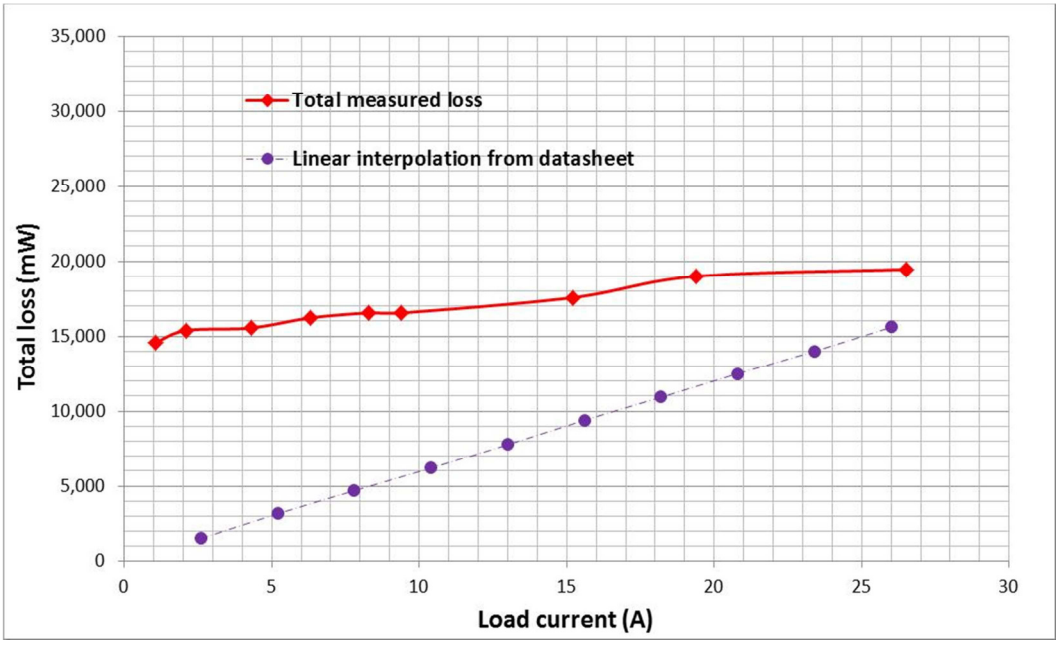


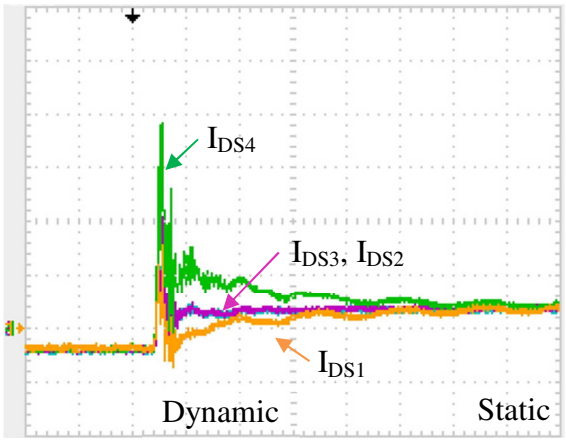

**Fig. 6** ***Measured switching loss for the CAS300M17BM2 module, at 600 V, 10 kHz switching frequency.***

### *5.2. Current Sharing in Parallel-Connected MOSFETs*

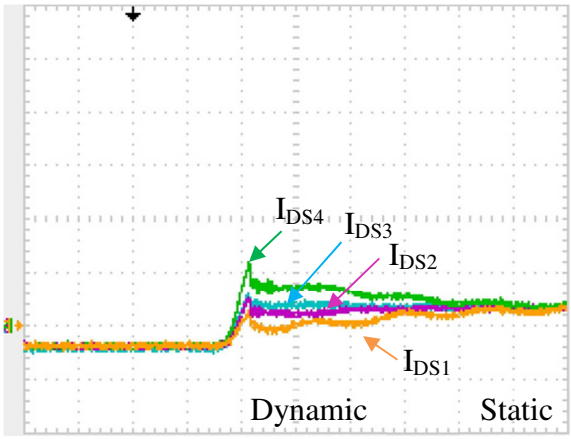
Parallel-connected devices are very desirable in MMC to reduce on-resistance since low device switching frequency of MMC means conduction loss dominates over switching loss. However, parallel-connection of MOSFETs risks increased damage to devices during switching transitions if oscillations exist between parallel-connected devices. It is therefore important to investigate the behaviour of parallel-connected MOSFETs, and explore options to mitigate the risks caused by transient behaviour.

As increasing gate resistance slows down switching speed EMI is reduced [27], and gate oscillations will be damped. However, increased gate resistance also exaggerates the spread in component tolerances leading to greater discrepancies in turn-on/off times. To explore the effects of increased gate resistance, current in individual devices in one submodule with four parallel-connected MOSFETs at 3 kHz switching frequency and 16 A load current, was measured. Non-symmetrical layouts lead to dynamic current imbalance, resulting in unbalanced switching losses [44], however with such low switching losses this effect is of no concern.

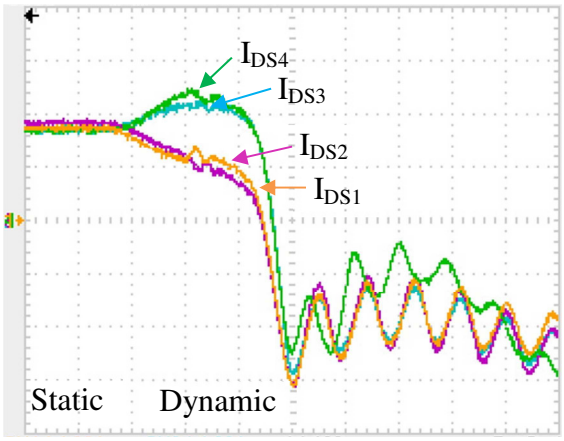
The dominant cause of static current unbalance is $R_{on}$ mismatch. Experimental results in Fig. 7 show good static current balance.



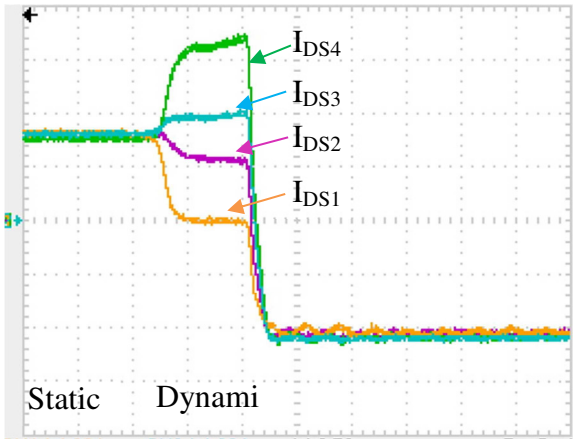

(a) Turn on with $R_G$=1 Ω (1 µs/div, 5 A/div)




(b) Turn on with $R_G$=100 Ω (1 µs/div, 5 A/div)




(c) Turn off with $R_G$=1 Ω (100 ns/div, 1 A/div)




(d) Turn off with $R_G$=100 Ω (2.5 µs/div, 1 A/div)

***Fig. 7*** *Current sharing between 4 parallel-connected MOSFETs ( IRFP4668s) with 16 A load current*

Different individual device threshold voltages and transconductances lead to varying switching rates as seen in Fig. 7 where MOSFET4 turns on first. The Miller effect then slows down the rise in $V_{GS}$ in the other 3 devices. The large current overshoot of MOSFET4 is caused by larger reverse recovery of its body diode resulting from its rapid turn-on transition. This dynamic current unbalance and the parasitic oscillations are exacerbated by the combined effects of the inductances, the gate and drain resistances, the gate-source capacitance, and the drain-source capacitance [44, 45]. Considering so many factors affecting the switching performance, it is practically impossible to match the MOSFET switching transients [44].

However, Fig. 7 shows that the current overshoot is safe for all devices even at a gate resistance of 1Ω, while with 100Ω the current overshoot with four devices parallel-connected is smaller than that for a single device switching with small gate resistance. As increased gate resistance slows down switching, oscillation and di/dt are attenuated significantly, reducing EMI. Fig. 7 clearly demonstrates that the MMC topology with increased gate resistance has significantly reduced device stress, while reduced ringing and slower transients will dramatically improve EMI, compared with a 2-level converter.

## 6. Conclusion

The complex factors which must be considered when determining an optimal converter design for LVDC distribution networks have been thoroughly investigated. Power loss including semiconductor conduction, switching, capacitor and inductor losses was calculated for 3 different competing converter topologies. MMC topologies offer 200W lower loss than the SiC 2-level converter, while offering the possibility of fault tolerance with minimal impact on loss. Slowed switching with no loss penalty in MMC converters also offers improved reliability as switching waveforms presented here show reduced device stress, while EMI will also be significantly reduced. With by far the smallest heatsink volume Si MOSFET MMC offers a surprisingly competitively compact solution despite the requirement for a larger number of cell capacitors. GaN appears to offer highest efficiency by a small margin, but it remains to be seen how the high-speed, sensitive GaN gate drivers perform in terms of reliability, while reliability of the GaN power devices appears to be lower than that of the Si MOSFET. However, since GaN is a new technology this reliability gap may close in time. In addition, counter-intuitively, the very small packaged GaN HEMT requires double the heatsink volume compared with Si MOSFET. The main advantage offered by the SiC 2-level converter is simplicity, but the relability history of SiC devices offsets this advantage, and with lower SiC 2-level efficiency, the MMC topologies are more attractive. At this time, Si MOSFET MMC offers the lowest cost converter for this application, although the authors note that relative costs are likely to be subject to much change.

Therefore, for low voltage, single-phase converters at 10 kW, Si MOSFET MMC offers the highest performance converter, with lowest cost, and small size.

Parallel-connection of devices offers lower MMC loss and further reduction in devices stress, bringing reliability improvement, hence has been analysed during this research. Power loss calculations indicate that four devices in parallel is optimal for the MMC topologies, while parallel-connection was unhelpful for the SiC 2-level converter due to the dominance of output capacitance related switching loss. Power loss was found to be the dominating factor dictating optimum extent of parallel-connection. Experimental results for four devices in parallel showed good static current sharing, and with slowed switching demonstrated lower device stress and order of magnitude slower and smaller transients to generate EMI. Further work is required to fully quantify EMI reduction.

Calculated loss was successfully validated through experimental measurement for a single MMC module, and for a SiC half-bridge converter.

## 7. Acknowledgments

The authors gratefully acknowledge the financial support of the EPSRC (EP/I031707/1) and the NSFC (EP/L00089X/1), and Mr Charles Croser who constructed the test circuits used in this study.

## 8. References

[1] V. Stanojevic, M. Bilton, J. Dragovic, J. Schofield, and G. Strbac, "Application of demand side response and energy storage to enhance the utilization of the existing distribution network capacity", in *22nd International Conference and Exhibition on Electricity Distribution*, Stockholm, Sweden, 2013, pp. 1-4.

[2] E. Borioli, M. Brenna, R. Faranda, and G. Simioli, "Comparison between the electrical capabilities of the cables used in LV AC and DC power lines", in *11th International Conference on Harmonics and Quality of Power*, 2004, pp. 408-413.

[3] T. Kaipia, P. Salonen, J. lassila, and J. Partanen, "Possibilities of the Low Voltage DC Distribution Systems", in *Proc. of NORDAC*, Stockholm, August 2006.

[4] A. Mattsson, V. Vaisanen, P. Nuutinen, T. Kaipia, A. Lana, P. Peltoniemi*, et al.*, "Implementation design of the converter-based galvanic isolation for low voltage DC distribution", in *Int. Power Electronics Conf. (ECCE-ASIA)*, Hiroshima, Japan, 2014, pp. 587-594.

[5] M. Amin, Y. Arafat, S. Lundberg, and S. Mangold, "Low voltage DC distribution system compared with 230 V AC", in *IEEE Electrical Power and Energy Conf. (EPEC)*, Winnipeg, Canada, 2011, pp. 340-345.

[6] D. Nilsson and A. Sannino, "Efficiency analysis of low- and medium- voltage DC distribution systems", in *IEEE Power Engineering Society General Meeting*, Denver, CO, 2004, pp. 2315-2321

[7] Y. Zhong, S. Finney, and D. Holliday, "An investigation of high efficiency DC-AC converters for LVDC distribution networks", in *7th IET Int. Conf. on Power Electronics, Machines and Drives (PEMD)*, Manchester, 2014, pp. 1-6.

[8] "Benefits of Advanced Smart Metering for Demand Response based Control of Distribution Networks", Summary Report, Imperial College London, April 2010.

[9] L. Chen and Y. Zhang, “Model and harmonic control strategy of electric vehicle chargers connected with the power system”, *2011 IEEE Power Engineering and Automation Conference (PEAM),* 2011, pp. 524-528.

[10] A. Lucas, F. Bonavitacola, E. Kotsakis and G. Fulli, “Grid harmonic impact of multiple electric vehicle fast charging”, *Electric Power Systems Research,* Vol.127, Oct 2015, pp. 13-21

[11] C. Delepaut, S. Siconolfi, O. Mourra and F. Tonicello, “MOSFET gate open failure analysis in power electronics”, *Applied Power Electronics Conference and Exposition (APEC),* May 2013.

[12] P. Bogonez-Franco, J.B. Sendra, "EMI comparison between Si and SiC technology in a boost converter", *EMC Europe*, Sept 2012.

[13] http://www.gansystems.com/_uploads/whitepapers/982304_GN001%20App%20Note%20-%20How%20to%20Drive%20GaN%20E-Mode%20Transistors%202014-10-21.pdf, accessed Jan 2017

[14] N. Mittal, B. Singh, S. P. Singh, R. Dixit, and D. Kumar, "Multilevel inverters: A literature survey on topologies and control strategies", in *2nd Int. Conf. on Power, Control and Embedded Systems (ICPCES)* Allahabad, India, 2012, pp. 1-11.

[15] S. R. Pulikanti, M. S. A. Dahidah, and V. G. Agelidis, "Voltage Balancing Control of Three-Level Active NPC Converter Using SHE-PWM", *IEEE Trans. Power Del.,* vol. 26, pp. 258-267, 2011.

[16] T. Bruckner, S. Bernet, and P. K. Steimer, "Feedforward Loss Control of Three-Level Active NPC Converters", *IEEE Trans. Ind. Appl.,* vol. 43, pp. 1588-1596, 2007.

[17] K. Li, "Wide Bandgap (SiC/GaN) Power Devices Characterization and Modeling: Application to HF Power Converters", PhD Thesis, Lille University of Science and Technology, 2014.
[18] B. Callanan, "Application Considerations for Silicon Carbide MOSFETs", CREE Inc, January 2011.
[19] "SiC Power Devices and Modules", Application Note, ROHM Semiconductor.June 2013.
[20] K. Ilves, A. Antonopoulos, S. Norrga, and H. P. Nee, "Steady-State Analysis of Interaction Between Harmonic Components of Arm and Line Quantities of Modular Multilevel Converters", *IEEE Trans. Power Electron.,* vol. 27, pp. 57-68, 2012.
[21] X. She, A. Huang, X. Ni, and R. Burgos, "AC circulating currents suppression in modular multilevel converter", in *IECON 2012 - 38th Annual Conf. on IEEE Industrial Electronics Society*, Montreal, Canada, 2012, pp. 191-196.
[22] Q. Tu, Z. Xu, and L. Xu, "Reduced Switching-Frequency Modulation and Circulating Current Suppression for Modular Multilevel Converters", *IEEE Trans. Power Del.,* vol. 26, pp. 2009-2017, 2011.
[23] NationalGrid, "The Grid Code - Connection Conditions", 22 Jan 2015.
[24] M. M. C. Merlin and T. C. Green, "Cell capacitor sizing in multilevel converters: cases of the modular multilevel converter and alternate arm converter", *IET Power Electronics,* vol. 8, pp. 350-360, 2015.
[25] Y. Zhong, "MOSFET-based MMC for Low voltage DC Distribution Networks", PhD thesis, University of Strathclyde, Glasgow, UK, 2016.
[26] Y. Zhong, D. Holliday, and S. J. Finney, "High-efficiency MOSFET-based MMC for LVDC distribution systems", in *IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, Canada, 2015, pp. 6691-6697.
[27] N. M. Roscoe, Y. Zhong, and S. J. Finney, "Comparing SiC MOSFET, IGBT and Si MOSFET in LV distribution inverters", in *41st Annual Conf. of the IEEE Industrial Electronics Society*, Yokohama, Japan, 2015.
[28] Y. Ren, M. Xu, J. Zhou, and F. C. Lee, "Analytical loss model of power MOSFET", *IEEE Trans. Power Electron.,* vol. 21, pp. 310-319, 2006.
[29] Y. Xiong, S. Sun, H. Jia, P. Shea, and Z. J. Shen, "New Physical Insights on Power MOSFET Switching Losses", *IEEE Trans. Power Electron.,* vol. 24, pp. 525-531, 2009.
[30] R. Ramachandran and M. Nymand, "Switching losses in a 1.7 kW GaN based full-bridge DC-DC converter with synchronous rectification", in *17th European Conf. on Power Electronics and Applications (EPE'15 ECCE-Europe)*, Geneva, Switzerland, 2015, pp. 1-10.
[31] "MOSFET Gate-Charge Origin and its Applications", AND9083/D Application Note, ON Semiconductor.
[32] http://www.api-capacitors.com/, accessed 20 Spet. 2016.
[33] R. Burkart and J. Kolar, “Comparative Life Cycle Costs Analysis of Si and SiC PV Converter Systems Based on Advanced Multi-Objective Optimization Techniques”, *IEEE Trans. on Power Electronics,* August 2016.
[34] T.T. Nguyen, A Ahmed, T.V. Thang and J.H. Park, “Gate oxide Reliabiltiy Issues of SiC MSOFETs under Short-Circuit Operation”, *IEEE Transactions on Power Electronics,* Vol. 30, Issue 5, May 2015.
[35] L.C. Yu, G.T. Dunne, K.S. Matocha, K.P. Cheung, J.S. Suehle and K. Sheng, “Reliability Issues of SiC MOSFETs: A Technology for High-Temperature Environments”, *IEEE Transactions on Device and Materials Reliabilty,* Vol. 10, Issue 4, Dec 2010.
[36] http://www.nxp.com/documents/technical_note/TN00008.pdf, accessed Jan 2017.
[37] http://epc-co.com/epc/Portals/0/epc/documents/product-training/EPC_Phase_Five_Rel_Report.pdf, accessed Jan 2017.

[38] F. Page, G. Adam, S. Finney, D. Holliday, L. Xu “DC Fault parameter sensitivity analysis”, *DPSP 2014*, March 2014
[39] G.P. Adam, S.J.Finney, B.W. Williams, D.R. Trainer, C.D.M.Oates and D.R. Critchley, “Network Fault Tolerant Voltage-Source-Converters for High-Voltage Applications”, *9th IET International Conference on AC and DC Power Transmission*, March 2010.
[40] A. Sawle and A. Woodworth, "Mounting Guidelines for the SUPER-220", International Rectifier Application Note AN-1000, 2016.
[41] *IRFP4668PbF HEXFET Power MOSFET*, Datasheet, International Rectifier.
[42] "GS66508T-EVBHB 650V GaN E-HEMT Half Bridge Evaluation Board User’s Guide", GaN Systems, 2015.
[43] X. Li, L. Zhang, S. Guo, Y. Lei, A.Q. Huang and B. Zhang, “Understanding switching losses in SiC MOSFET: toward lossless switching”, *IEEE 3rd workshop on Wide Bandgap Power Devices And Applications (WiPDA)*, 2015, pp. 257–262.
[44] "Application Note AN-941: Paralleling Power MOSFETs", International Rectifier.
[45] J. B. Forsythe, "Paralleling of Power MOSFETs for Higher Power Output", International Rectifier, E1 Segundo, California.