Modular Input-Series-Input-Parallel Output-Series DC/DC Converter Control with Fault Detection and Redundancy

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***Abstract*—A novel high-power modular input-series-input-parallel output-series connected DC/DC converter for medium-voltage application is proposed. Emphasis has been placed on power sharing control to compensate parameter mismatches and achieve equal power distribution between modules. Converter control is extended to achieve fault-tolerant operation by exploiting modularity to provide redundancy in the event of any failure. The proposed control scheme is validated through application-level simulations and scaled-down experiments to testify the reliability of the proposed control for ensuring power sharing between modules under a range of operating conditions. The results validate the proposed converter and associated control scheme indicating this to be a promising topology for high-power medium-voltage applications.**

Keywords—High-power DC/DC converter, Redundancy, Small-signal modelling, Input-series-input-parallel Output-series

I. INTRODUCTION

Studies have shown that medium-voltage DC (MVDC) connection may be advantageous for long cable networks, such as the collection grid of offshore wind farms. In such cases, DC connection has the potential to deliver lower system level losses through the elimination of AC charging current and better utilization of cable capacity. Reduction in system volume and weight may also be achieved by the replacement of line-frequency transformers with medium- or high-frequency DC/DC converters [1-4]. Realizing the benefits of MVDC will require the use of high-capacity DC/DC converters capable of operating at the required network voltages, e.g. wind generator DC link voltage step up (e.g. from 5kV DC) to a level compatible with an efficient wide area network connection (e.g. 33kV DC). Although some high-efficiency DC/DC converters have been developed [5, 6], transfer of these technologies to the required network voltages is still a challenge since both the input and output of the DC/DC converter must operate above the voltage capability of existing power semiconductors. A solution to this problem is the modular connection of multiple transformer-coupled converters in which each module operates within the voltage rating of individual semiconductor devices, which can achieve high-power without compromising the efficiency and switching frequency. This paper proposes a multi-module converter consists of *n* transformer-coupled full-bridge DC/DC modules, whose inputs are input-series-input-parallel connected, while the outputs are series connected, with uni-directional power flow capability.

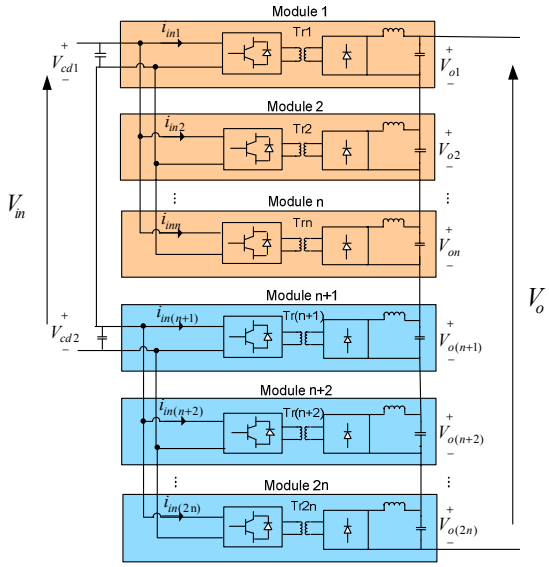


Fig.1 ISIPOS converter with full-bridge DC/DC modules

This configuration is well suited for offshore DC collection grid, where bi-directional power flow is not needed. In addition, it offers the potential for a more compact and lighter design [4, 7, 8]. Input-series-input-parallel connection of the power converters allows reduction of the current and voltage stresses in the power devices, thereby enabling device ratings and switching frequency to be optimized. With output-series connection, the turns-ratios of the isolation transformers can be reduced, leading to a reduction in leakage inductance. This proposed modular transformer-coupled DC/DC converter with input-series-input-parallel output-series (ISIPOS) connection presents a number of attractive properties: each module only contributes a small fraction of the total power and operates at voltages and currents that can be supported by available power semiconductors; the modular structure allows the

converter to be re-configured and higher switching frequency can be achieved without significant design challenges; and redundant cells in this modular configuration provide fault ride through operation with a level of redundancy [8-10].

Fig.1 shows the structure of a 2*n*-module ISIPOS DC/DC converter with two parallel arms (each has *n* modules) being series connected, where the number of parallel and series connected modules can be extended to any number according to the application requirements. Reliable operation of the converter requires a dedicated controller that compensates for any mismatch in the passive components and active switching devices, and that ensures equal power sharing between the modules. The proposed multi-module converter has internal fault management capability similar to that of a modular multilevel converter (MMC), in that the controller can be designed to allow faulty modules to be bypassed in order to allow continued system operation without any performance degradation. Having introduced the proposed converter in Section I, small-signal modeling is introduced in Section II. The control topology for power sharing operation is described in Section III, and both simulation and experimental results are presented to confirm the viability of the control schemes. Simulation of fault-tolerant operation is presented in Section IV. Conclusions are presented in Section V.

II. Small Signal Modeling

Although the DC/DC converter is a nonlinear system, the functions given here are used to facilitate controller design based on well-known linear feedback control techniques. The small-signal model of the four-module (n=2 in Fig.1) ISIPOS connected DC/DC converter, shown in Fig.2, builds upon a single module converter model [10] where k_1, k_2, k_3 and k_4 represent transformer turns ratios, L_r represents the transformer leakage inductance, L_{f1}, L_{f2}, L_{f3}, L_{f4}, C_{f1}, C_{f2}, C_{f3} and C_{f4} are filter inductances and capacitances, and Δv_{in} is input voltage perturbation. Input voltage perturbation components for Modules 1 and 2, and for Modules 3 and 4 are Δv_{cd1} and Δv_{cd2} respectively, input current perturbations are Δi_{in1}, Δi_{in2}, Δi_{in3} and Δi_{in4} respectively, and filter inductor current and capacitor voltage perturbations are represented by Δi_{lf1}, Δi_{lf2}, Δi_{lf3}, Δi_{lf4}, Δv_{o1}, Δv_{o2}, Δv_{o3}, Δv_{o4} respectively. D_e is the effective duty ratio per module, duty ratio perturbations are represented by Δd_1, Δd_2, Δd_3, and Δd_4, and Δd_{v1}, Δd_{v2}, Δd_{v3}, Δd_{v4}, Δd_{i1}, Δd_{i2}, Δd_{i3} and Δd_{i4} represent perturbations of the duty ratio due to the input voltage and output current, as defined in (1)

$$\begin{cases} \Delta d_{v1} = \Delta d_{v2} = \dfrac{32L_r D_e f_s}{k^2 V_{in} R_o}\Delta v_{cd1} \\ \Delta d_{v3} = \Delta d_{v4} = \dfrac{32L_r D_e f_s}{k^2 V_{in} R_o}\Delta v_{cd2} \\ \Delta d_{ij} = -\dfrac{8L_r f_s}{kV_{in}}\Delta i_{lfj} \end{cases} \tag{1}$$

where j=1, 2, 3 and 4.

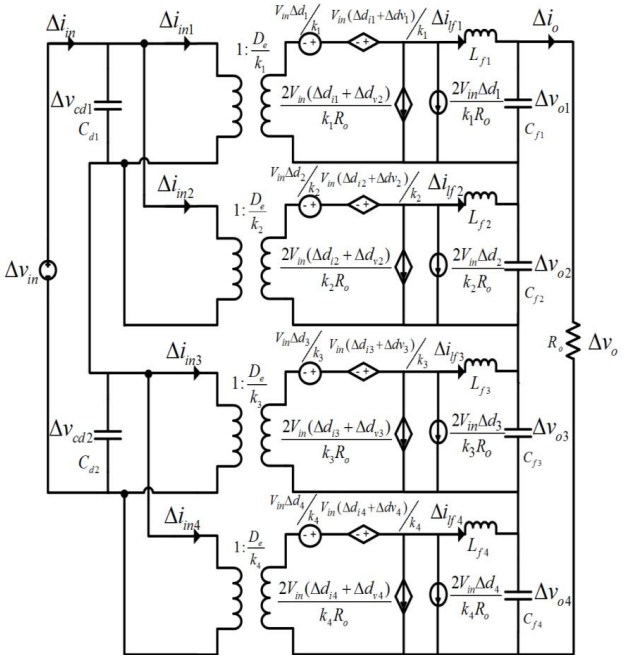


Fig.2 ISIPOS converter small-signal model

To simplify the analysis [11], four modules are assumed to have the same effective duty cycle, transformer turn ratio, and capacitor and inductor values. The corresponding equations, produced by application of KVL in Fig.2, are shown in (2).

$$\begin{cases} \dfrac{D_e\Delta v_{cd1}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_1 + \Delta d_{v1} + \Delta d_{i1}\right) = s\mathrm{L}_f\Delta i_{lf1} + \Delta v_{o1} \\ \dfrac{D_e\Delta v_{cd1}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_2 + \Delta d_{v2} + \Delta d_{i2}\right) = s\mathrm{L}_f\Delta i_{lf2} + \Delta v_{o2} \\ \dfrac{D_e\Delta v_{cd2}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_3 + \Delta d_{v3} + \Delta d_{i3}\right) = s\mathrm{L}_f\Delta i_{lf3} + \Delta v_{o3} \\ \dfrac{D_e\Delta v_{cd2}}{k} + \dfrac{V_{in}}{2k}\left(\Delta d_4 + \Delta d_{v4} + \Delta d_{i4}\right) = s\mathrm{L}_f\Delta i_{lf4} + \Delta v_{o4} \end{cases} \tag{2}$$

The relationship between output voltage and load current is derived [4] as (3).

$$G_{\mathrm{ovi}} = \frac{\Delta v_o}{\Delta i_o} = \frac{4L_f\mathrm{s} + \dfrac{16L_r f_s}{k^2}}{s^2 L_f C_f + s\left(\dfrac{4L_f}{R_o} + \dfrac{4L_r f_s C_f}{k^2}\right) + 1 + \dfrac{16L_r f_s}{k^2 R_o}} \tag{3}$$

The relationship between output voltage and duty ratio can be represented as (4), and the transfer function between load current and duty ratio can be represented as (5), where j=1, 2, 3, 4.

$$G_{\mathrm{ovd}} = \frac{\Delta v_o}{\Delta d_j} = \frac{V_{in}}{2k\left[s^2 L_f C_f + s\left(\dfrac{4L_f}{R_o} + \dfrac{4L_r f_s C_f}{k^2}\right) + 1 + \dfrac{16L_r f_s}{k^2 R_o}\right]} \tag{4}$$

$$G_{oid} = \frac{\Delta i_o}{\Delta d_j} = \frac{V_{in}}{2k\left[s^2 L_f C_f R_o + 4L_f s + \dfrac{4L_r f_s C_f R_o}{k^2}s + R_o + \dfrac{16L_r f_s}{k^2}\right]} \tag{5}$$

The relationship between modular voltage outputs and inductor currents can be represented as (6)

$$\begin{cases} \Delta v_{o1} = g_1 \Delta i_{lf1} - g_2 \left(\Delta i_{lf2} + \Delta i_{lf3} + \Delta i_{lf4} \right) \\ \Delta v_{o2} = g_1 \Delta i_{lf2} - g_2 \left(\Delta i_{lf1} + \Delta i_{lf3} + \Delta i_{lf4} \right) \\ \Delta v_{o3} = g_1 \Delta i_{lf3} - g_2 \left(\Delta i_{lf1} + \Delta i_{lf2} + \Delta i_{lf4} \right) \\ \Delta v_{o4} = g_1 \Delta i_{lf4} - g_2 \left(\Delta i_{lf1} + \Delta i_{lf2} + \Delta i_{lf3} \right) \end{cases} \tag{6}$$

where

$$\begin{cases} g_1 = \dfrac{sC_f R_o + 3}{s^2 C_f{}^2 R_o + 4sC_f} \\ g_2 = \dfrac{1}{s^2 C_f{}^2 R_o + 4sC_f} \end{cases} \tag{7}$$

The relationship between the two input capacitor voltages and duty ratios is shown in (8)

$$\begin{bmatrix} \Delta v_{cd1} \\ \Delta v_{cd2} \end{bmatrix} = \begin{bmatrix} \dfrac{A(s)}{2} & -\dfrac{A(s)}{2} \\ -\dfrac{A(s)}{2} & \dfrac{A(s)}{2} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_3 \end{bmatrix} \tag{8}$$

where

$$A(s) = -\frac{\dfrac{2V_{in}}{kR_o}(g_2 + g_1 + sL_f) + \dfrac{V_{in}}{2k}}{\dfrac{D_e}{k} + sCd\dfrac{k}{D_e}(g_1 + sL_f + g_2)} \tag{9}$$

The relationship between input currents and duty ratios is shown in (10)

$$\begin{bmatrix} \Delta i_{in1} \\ \Delta i_{in2} \end{bmatrix} = \begin{bmatrix} \dfrac{B(s)}{2} & -\dfrac{B(s)}{2} \\ -\dfrac{B(s)}{2} & \dfrac{B(s)}{2} \end{bmatrix} \begin{bmatrix} \Delta d_1 \\ \Delta d_2 \end{bmatrix}$$

$$\begin{bmatrix} \Delta i_{in3} \\ \Delta i_{in4} \end{bmatrix} = \begin{bmatrix} \dfrac{B(s)}{2} & -\dfrac{B(s)}{2} \\ -\dfrac{B(s)}{2} & \dfrac{B(s)}{2} \end{bmatrix} \begin{bmatrix} \Delta d_3 \\ \Delta d_4 \end{bmatrix} \tag{10}$$

where

$$B(s) = D_e\left(\frac{2V_{in}}{R_o} + g_3 - g_4\right)$$

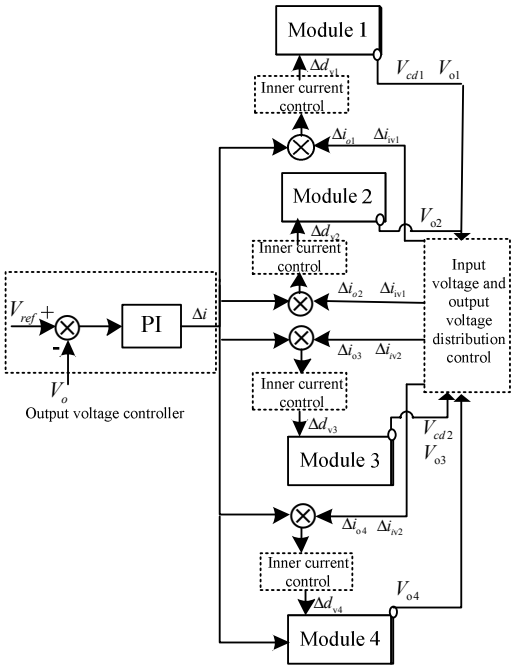
$$\begin{cases} g_3 = \dfrac{ac - 2bc}{(a+b)(a-3b)} \\ g_4 = \dfrac{bc}{(a+b)(a-3b)} \end{cases} \tag{11}$$

$$\begin{cases} a = sL_f + \dfrac{sC_f R_o + 3}{s^2 C_f{}^2 R_o + 4sC_f} + \dfrac{4L_r f_s}{k^2} \\ b = -\dfrac{1}{s^2 C_f{}^2 R_o + 4sC_f} \\ c = \dfrac{V_{in}}{2k} \end{cases}$$

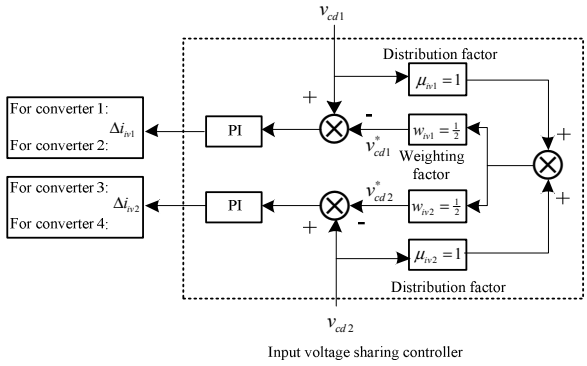
III. ISIPOS Converter Power Balancing Control

A. Power balancing control

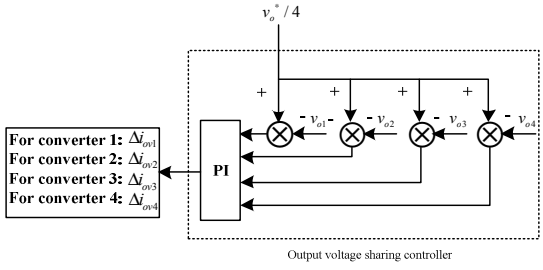
In order to ensure safe and reliable operation in the presence of internal mismatches and external transients, dedicated power balancing control is indispensable for ISIPOS DC/DC converters [11, 12].



(a)



(b)



(c)

Fig.3 Control scheme for the ISIPOS DC/DC converter (a) overall structure (b) input voltage sharing controller (c) output voltage sharing controller

The proposed control system shown in Fig.3 consists of four control loops: an output voltage control loop to control the load voltage, an output voltage sharing control loop to balance the modular output voltages, an input voltage sharing control loop to maintain the input capacitor voltages equal, and inner current loop that regulates the output inductance current of individual module and acts as safeguard against over-load.

As shown in Fig.3 (a), the output voltage controller contributes the main current signal Δi to all modules based on (3), which is then modified by the power balancing loops. The control scheme provides power balancing control between all the modules using two control loops:

- Input voltage sharing loop

This maintains equal input voltages across the input capacitors in order to correct the differences between input-series-output-series connected modules, e.g. Modules 1 and 3. For input-series connected modules, the average sharing method applied to v_{cd1} and v_{cd2} is used to generate the input voltage reference signals. Therefore distribution factor $\mu_{iv1}=\mu_{iv2}=1$, and weighting functions $W_{iv1}=W_{iv2}=1/2$, as shown in Fig.3 (b). The input voltage sharing controller generates the current contributions Δi_{iv1} for Modules 1 and 2, Δi_{iv2} for Modules 3 and 4.

- Output voltage sharing loop

This balances modular output voltages in order to maintain power balanced between the input-parallel-output-series modules, e.g. Modules 1 and 2, or Modules 3 and 4. For input-parallel connected modules, Δi_{ov1}, Δi_{ov2}, Δi_{ov3}, Δi_{ov4} are generated by the PI controller which eliminates the error between v_o^*/n, where n=2 in this case, and the output voltage from an individual module, as shown in Fig.3 (c).

Referring to Fig.3 (a), the current contributions produced by the three controllers are summed to provide the module current reference. Individual inner current control loops for filter inductor currents, which are capable of guaranteeing current performance, are added to obtain the duty cycle contributions from the PI current controller. Simulation and experimental results are presented in the next section to demonstrate its performance in the context of parameter mismatch and transience.

B. Power balancing control simulation results

The system parameters are listed in Table I. Note that some parameters are chosen to be different among the modules. Fig.4 presents selected simulation results for a step change in load output voltage, with parameter mismatches between the modules. Fig.4 (a) shows DC output voltage performance as the output voltage reference changes to 33kV at time t=0.1s and then reduces to 30kV at t=0.2s. Fig.4 (b) and (c) show the corresponding modular output voltages and output current performances. These results show that the multi-module ISIPOS DC/DC converter can achieve equal power sharing between the modules with the proposed control scheme in the presence of mismatches, and that it outperforms a large single DC/DC converter based on a two-level topology in terms of device stress, and based on an MMC topology in terms of dynamic performance and overall footprint resulting from its large capacitor requirement.

TABLE I: LIST OF PARAMETERS

Parameter	***Simulation Values***
DC/DC Converter Rated Power	5MW
Input DC Voltage	5kV
Output DC Voltage	33kV
Number of Modules	10
PWM Carrier Frequency	2.5kHz
Input Capacitance	C_{cd1}=1000μF C_{cd2}=1100μF
Transformer Turns Ratio	$T_1=T_3=T_5=T_7=T_9$= 1:1.2 $T_2=T_4=T_6=T_8=T_{10}$= 1:1.3
Output Inductance	$L_1=L_3=L_5=L_7=L_9$ = 0.5H $L_2=L_4=L_6=L_8=L_{10}$ = 0.55H
Output Capacitance	$C_1=C_3=C_5=C_7=C_9$ = 80μF $C_2=C_4=C_6=C_8=C_{10}$ = 100μF

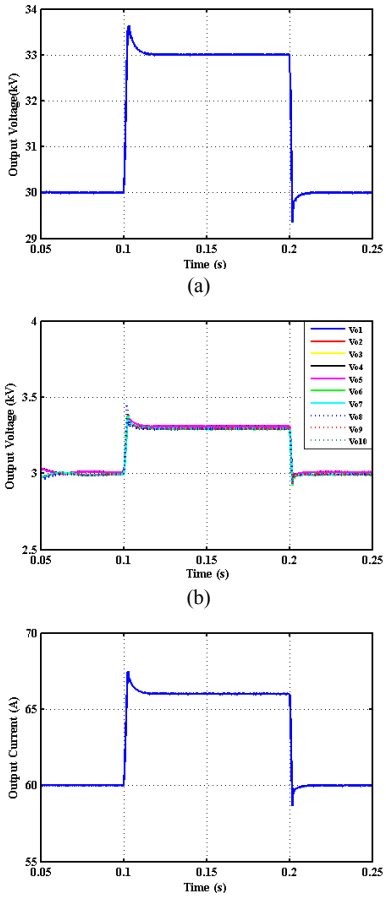


Fig.4 Simulation waveforms illustrating dynamic performance of the converter when a step change is applied to its DC output voltage reference (a) output voltage (b) modular output voltages (c) output current

C. Power balancing control experimental results

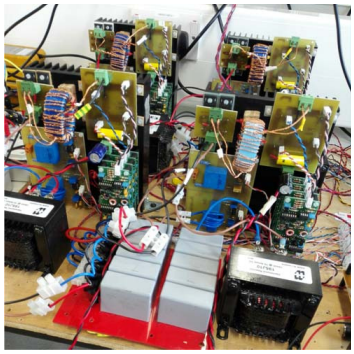


Fig.5 Test rig for the ISIPOS connected DC/DC converter

Performance was validated by using the test rig shown in Fig.5. The test rig consists of four ISIPOS connected modules (i.e where n=2 in Fig.1) and where the main system parameters are as listed in Table II.

TABLE II: LIST OF PARAMETERS

Parameter	***Simulation Values***
DC/DC Converter Rated Power	200W
Input DC Voltage	40V
Output DC Voltage	60V
Number of Modules	4
PWM Carrier Frequency	2.5kHz
Input Capacitance	C_{cd1}=45μF C_{cd2}=40μF
Transformer Turns Ratio	T_1= 1:1.4, T_2=1:1.2 T_3= 1:1.3, T_4=1:1.2
Output Inductance	$L_1 = L_3 = L_5 = L_7 = L_9$ = 0.5H $L_2 = L_4 = L_6 = L_8 = L_{10}$ = 0.55H
Output Capacitance	$C_1 = C_2$ = 160μF $C_3 = C_4$ = 200μF

Fig.6 shows selected experimental results for normal operation of the ISIPOS converter, with mismatches between module parameters as shown in Table II. Fig.6 (a) shows input capacitor voltages V_{cd1} and V_{cd2} during start-up, when the same duty cycle is applied to the modules. It can be seen that there is a difference between the two voltages. Fig.6 (b) shows the results obtained when employing the proposed controller to balance the input capacitor voltages and that, despite the parameter mismatches, input voltage sharing (IVS) is achieved. Fig.6 (c) shows that, initially, control action is not active and same duty cycle is applied to the modules, and that when control action is activated at t=150ms, IVS is achieved. This shows the effectiveness of the proposed control in achieving power sharing between the modules. Fig.6 (d) shows output voltage and current during start-up, where output voltage is regulated to the desired steady-state value of 60V after 5ms. Modular output voltage during start-up is shown in Fig.6 (e), whilst Fig.6 (f) shows modular output voltage during steady-state. Both figures highlight the output voltage sharing (OVS) ability of the proposed controller. It can be observed that the proposed control scheme successfully addresses the issue of mismatched modules by balancing the input capacitor voltages and modular output voltages.

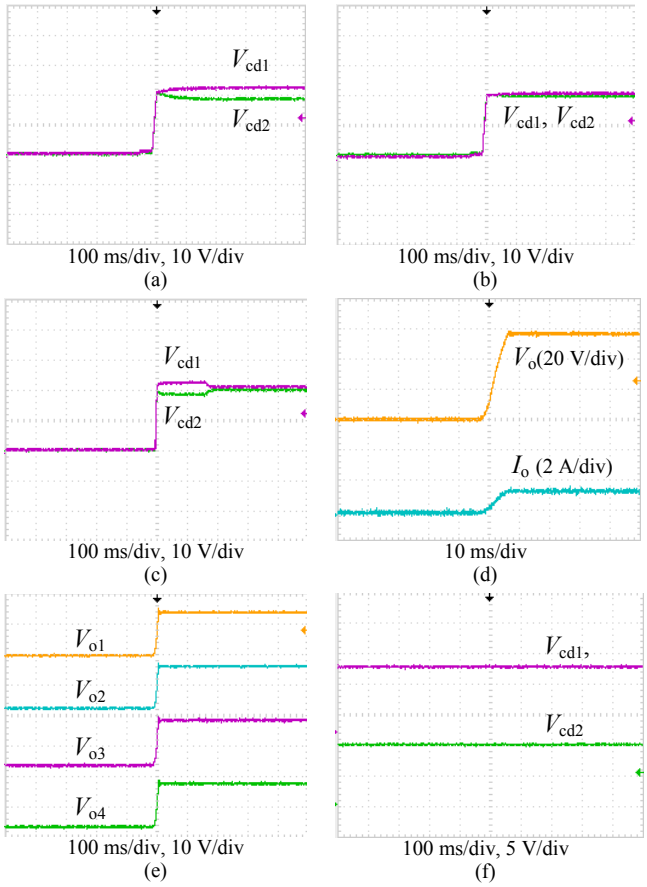


Fig.6 Experimental waveforms illustrating normal converter operation (a) input capacitor voltages without control (b) input capacitor voltages with control (c) input capacitor votlages without and with control (d) output votlage and current during start-up (e) modular output votlages during start-up (f) modular output votlages during steady-state

IV. ISIPOS CONVERTER FAULT DETECTION AND REDUNDANCY

A. Fault detection and redundancy control

One of the merits of using this modular architecture is the increased reliability it provides for given level of redundancy. More modules than required by the load may be introduced to cater for module failure, so that each module operates at power level lower than the rated value under normal operation. When a fault occurs, the modularity feature allows a pre-designed control strategy to isolate the faulty module, and to reconfigure the converter to use the remaining healthy modules to supply the load. However, there is often a trade-off between the extra cost incurred by the redundant modules and the impact of the failure [13].

Provision of redundancy can be illustrated by the converter in Fig.1, where n=5 and the faulty module is Module 5. Fault detection can be realized by monitoring the module output voltages, e.g. for the 10-module system shown in Fig.7, if the output voltage falls outside a pre-

defined range, e.g. $V_o/10.5<V_o<V_o/9.5$, then a protection strategy is activated. The faulty module is isolated by blocking its front-end pulse width modulated H-bridge converter and bypassing its output diode bridge using a combination of a bypass switch and a bleed resistor to dissipate the energy stored in the filter capacitor. Following that, there are two ways of obtaining the fault-tolerant operation for this 10-module system:

The first method is to isolate Module 5, maintain voltage balance across the input capacitors, and to increase the output voltages of the remaining healthy modules (Module 1, 2, 3, and 4) in upper parallel-connected arm by changing the modular output voltage references from $V_o/10$ to $V_o/8$, to compensate the loss of Module 5. The output voltage references for the 5 modules in lower parallel-connected arm remain the same at $V_o/10$. In doing this, the input currents to the modules in the upper parallel-connected arm are boosted to increase the input power.

For the second method, Module 5 and one module in the lower arm, e.g. Module 6, are isolated to maintain the symmetrical structure of the system. The output voltages of the remaining eight modules are boosted to track the new reference of $V_o/8$.

In terms of stability, the symmetry offered by the second method simplifies the control action. However, more redundant modules are required in comparison to the first option, leading to additional cost. Therefore, the first option is adopted. Simulation results are presented in the next section to verify performance and fault-tolerant operation.

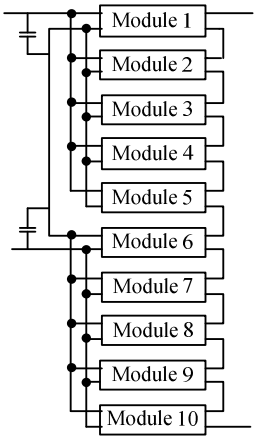


Fig.7 10-module ISIPOS DC/DC system

B. *Fault detection and redundancy control simulation results*

Fig.8 presents selected simulation results for fault-tolerant operation, with mismatches between module parameters as shown in Table I. A short-circuit fault is applied at the output of Module 5 at t=75ms. It can be seen from Fig.8 (a) that converter output voltage V_o recovers to its pre-fault value after a short time period. Following the fault, the faulty Module 5 is bypassed and its output becomes 0. The output voltages of the remaining modules in the upper arm are boosted to compensate for the loss, and the modules in lower arm maintain their outputs. Fig.8 (c) shows the output current disturbance caused by the fault and that the recovery time is only a few milliseconds. Fig.8 (d) proves the control loop can ensure input capacitor voltage balancing even under the fault condition. The results show that, with the mismatches in the system, the proposed control scheme provides fault-tolerant operation by isolating the faulty module and using the selected modules to compensate. This fault-tolerant operation proves the proposed converter has high reliability, which is an important factor in medium-voltage applications.

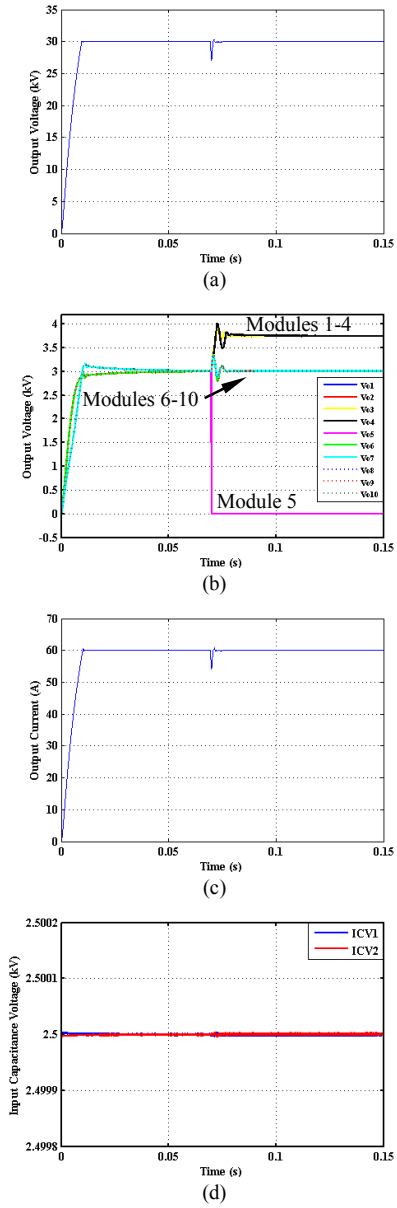


Fig.8 Simulation waveforms illustrating dynamic performance of the converter when a short-circuit fault is applied to the output of Module 5 (a) output voltage (b) modular output voltages (c) output current (d) input capacitor voltages

V. Conclusions

A new high-power DC/DC converter for medium-voltage applications is proposed, where full-bridge DC/DC converters are input-series-input-parallel output-series (ISIPOS) connected. Input voltage sharing (IVS) and output voltage sharing (OVS) control are proposed to achieve power sharing between the modules under conditions of module parameter mismatch. The power sharing control ability of the proposed control scheme is shown to effectively balance power distribution during dynamic operation. Simulation and experimental results to confirm this are presented based on a 10-module converter rated at 5MW and a 4-module scaled-down experimental test rig respectively. Reliability is an established metric for converter design, especially for high-power medium-voltage converters. Fault detection and redundancy can be easily employed in the proposed converter due to its modularity. This is verified through simulation of a 10-module converter with one module failure and the results show that the system exploits (n+1) redundancy. The proposed converter and control strategy can be extended to any number of modules and any allowable level of redundancy, making it a promising topology for high-power medium-voltage applications. Future work will incorporate additional modules into the converter, and will investigate application of (n+1) redundancy to ISIPOS connected converters to show equal power sharing performance following a fault.

Acknowledgment

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