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PWM STRATEGIES FOR MULTILEVEL MULTIPHASE AC DRIVES

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TABLE 4.4 PAGE 61 AND APPENDIX B CONTAINING PUBLISHED WORKS HAVE NOT BEEN SCANNED ON INSTRUCTION FROM THE UNIVERSITY

ABSTRACT

Pulse width modulation (PWM) strategies for multilevel multiphase ac drives have been analysed in this thesis. The large amount of published work in the area of multiphase drives recognises their advantages compared to the standard three-phase solutions. Some of them are improved power sharing capabilities, increased reliability and fault tolerance. However, in the most of these works two-level inverters were used for supply of multiphase machine. Also, huge amount of research has been done in the area of multilevel inverters. Nowadays, three-phase multilevel inverters are in use in high-power applications. However, the ideal scenario for high-power applications is supply of a multiphase machine from the multilevel inverters. So far no negative consequences of combination of these two topologies, apart from increased complexity of the system, have been identified, and this topology is the subject of this thesis.

The analysed topology is a multiphase machine with star-connected stator winding, supplied by a multilevel voltage source inverter. As the main envisaged application of such drives is in high-power systems, the efficiency is the most important issue. Because of the increased number of phases and increased number of levels of the inverter, proper control of such a system becomes more complicated. In this thesis both commonly used modulation strategies, carrier-based and space vector PWM, are analysed. Carrier-based strategies are easily extendable and applicable for a system with any number of phases and any number of levels. However, the number of possible switching states of the inverter that should be analysed in space vector modulation is l^n, where n represents the number of phases and l is the number of levels of the inverter. The applied method of analysis of the space vectors is through the vector space decomposition approach. This means that, in a multiphase case, more than one plane must be analysed simultaneously. Dealing with such a high number of combinations while satisfying reference requirements in more planes represents the main problem for development of the space vector algorithms. Hence, the space vector algorithms have to be analysed independently for each case and hence, in the thesis, five-phase and seven-phase three-level cases are elaborated. However, there are some general steps that can be applied, and those steps are described in the thesis. Because of the simplicity for implementation of carrier-based algorithms, detailed comparison of analysed space vector and carrier-based modulation strategies is conducted.

Five modulation strategies have been analysed for each case, five-phase three-level and seven-phase three-level topology. The strategies are compared theoretically, through the analysis of applied switching sequences, their regions of application and times of application of each switching state. The other method of comparison was through the time waveforms and through their spectra. Commonly used quality indicator of a signal, total harmonic distortion (THD), has been also calculated. The equivalence of one carrier-based and one space vector modulation strategy, for both cases, is confirmed. These strategies produce at the same time the minimum current THD. Regarding complexity, it is shown that carrier-based realisation is much simpler and thus is favourable for practical implementations. All results are confirmed by simulations and experiments and the results were always in good agreement.

Because of importance of the THD as a parameter in the analysis of the modulation strategies, the last part of the thesis considers and derives analytical formulae for leg and phase voltage RMS and THD. It gives analytical solution for produced leg voltage THD for an inverter with an arbitrary number of levels. For the phase voltage THD, two- and three-level cases with any number of phases are covered.

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CONTENTS

LIST OF PRINCIPAL SYMBOLS

n	Number of phases of the machine (of the inverter)
l	Number of levels of the inverter voltage output
v	Voltage
i	Current / Integer part of the reference leg voltages in Chapter 7
$A, B, C, \ldots, N$	Inverter legs in general or used in sub-script to associate the principal symbol with a certain leg e.g. v_A, i_A
$a, b, c, \ldots, n$	Phases of the machine/load or used in sub-script to associate the principal symbol with a certain phase e.g. v_a, i_a
NDC	Negative dc bus rail of the inverter (reference point for leg voltages)
PDC	Positive dc bus rail of the inverter
V_{dc}	Dc bus voltage of the inverter ($V_{dc} = V_{PDC} - V_{NDC}$)
α	Characteristic angle, $\alpha = 2\pi/n$
S	Neutral point (star) of the machine/load
$[\underline{E}_n]$	Complex transformation matrix for an n-phase system
$[C_n]$, $[\underline{C}_n]$	Decoupling transformation matrix for an n-phase system in real/complex form
α-β, x_1-y_1, x_2-y_2, …, 0^+-0^-	2-D planes after decoupling transformation
pl	Complex plane number (for 0^+ axis $pl=0$, for α-β plane $pl=1$, for x_1-y_1 plane $pl=2,\ldots$ for 0^- axis (exists for even n) $pl=n/2$)
p	Axis in the decoupled system ($p=\alpha, \beta, x_1, y_1, \ldots, 0^+, 0^-$)
$p(t)$	Instantaneous power of the signal
m	Modulation index
θ	Instantaneous reference space vector position
T_s	Switching period
f_s	Switching frequency
$T_{1,2,3\ldots}$	Times of application of space vectors, where sub-script defines a particular space vector
$T_{A,B,C\ldots}$	Time of application of high leg state, where sub-script defines a particular leg
$\delta_{1,2,3\ldots}$	Duty cycles of the space vectors, where sub-script defines a particular space vector
$\delta_{A,B,C\ldots}$	Duty cycles of the high leg states, where sub-script defines a particular leg
d	Differential operator
t	Time in general, or with sub-script that defines a particular instant
f	Frequency in general / Fundamental frequency of the periodical signal / Fractional part of the reference leg voltages in Chapter 7
T	Fundamental period of the periodical signal

L	Inductance, where sub-script can be used for more precise definition
R	Resistance, where sub-script can be used for more precise definition
C	Capacitance, where sub-script can be used for more precise definition
ω	Angular velocity
u	Voltage in relative units, V_{dc} corresponds to l–1 value ($u=v/V_{dc}\cdot(l-1)$), apart from Chapter 7 where $u=v/V_{dc}$ i.e. V_{dc} corresponds to 1
X_{rms}	Root mean squared value of signal $x(t)$
$P_{T_x}(x)$	Average power of signal x during the period T_x
THD(x)	Total harmonic distortion of signal x
HD(x)	Harmonic distortion, where sub-script defines a particular axis or plane
h	Harmonic index in spectrum
r	Number of harmonics for THD and HD calculation / number of planes
Λ	Distance between considered phases, e.g. Λ=1 for, *a-b*, *b-c*, ..., *n-a*, Λ=2 for, *a-c*, *b-d* etc.
int	Integer number in general
k	General counter
Δ	A/D converter (oscilloscope) sampling time
K	Number of samples per signal period

GENERAL

$\underline{x}$	Line below the symbol identifies complex value
$\overline{x}$	Line above binary value identifies complement (inverted) value
x^*	Asterisk in superscript, denotes the reference value
X	Capital letter stands for constant value, time independent
$x(t)$	Continuous signal in time
$x(kT_s)$	Discretised value of signal $x(t)$. $x(kT_s)$ does not change during the sampling period, T_s (for symmetrical sampling, i.e. during $T_s/2$ for asymmetrical sampling)
$x[t]$	Digitalised, discretised and quantised signal (signal takes a few digital values during the sampling period T_s)
$\breve{x}$	Symbol ˘ above variable denotes signal moved to the lowest dc bus level zone
$[x]$	Vector values are given in square brackets

LIST OF USED ABBREVIATIONS

ac	Alternating Current
A/D	Analogue to Digital
dc	Direct Current
CMV	Common Mode Voltage
2-D	Two-Dimensional
3-D	Three-Dimensional
DSP	Digital Signal Processor
IGBT	Insulated Gate Bipolar Transistor
FFT	Fast Fourier Transformation
DFT	Discrete Fourier Transformation
PWM	Pulse Width Modulation
RMS	Root Mean Square (value)
THD	Total Harmonic Distortion
HD	Harmonic Distortion
CBPWM	Carrier-Based Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
VSD	Vector Space Decomposition
VSI	Voltage Source Inverter
NPC	Neutral-Point Clamped
CHB	Cascaded H-Bridge
FC	Flying Capacitor
LS	Level-Shifted
PD	Phase Disposition
PS	Phase Shifted
POD	Phase Opposition Disposition
APOD	Alternative Phase Opposition Disposition
CPU	Central Processing Unit
FPGA	Field Programmable Gate Array
M-V	Medium-voltage

Chapter 1

INTRODUCTION

1.1 PRELIMINARY CONSIDERATIONS

Requirement for variable speed operation is of the primary importance in industrial applications. In the beginning, due to simplicity of speed control, only dc machines were in use. For this purpose ac machines were limited to operation at the fixed speed, determined by the construction and the grid. However, ac machines have a lot of advantages, compared to dc machines. Some of them are simplicity of the construction, absence of commutators and brushes that make dc machines unreliable and unsuitable to operate in dusty and explosive environment, and almost maintenance-free operation. These characteristics of the ac machines make them very desirable in industrial applications.

Utilisation of induction machines (IMs) is nowadays so widespread that they represent the biggest consumers of electrical energy worldwide. One interesting data from early 80s says that almost 70% of total electrical energy consumed in the USA was used to drive electrical machines, and more than 90% of that was used by ac drives that were operated at fixed speed [Bose (1982)]. Development of power semiconductor devices allowed operation of ac machines at variable speed. Progress in insulated-gate bipolar transistors (IGBTs) in the beginning of the 1990s made inverters highly efficient and applicable in wide range of applications and environments. This allowed replacement of the dc machines with ac machines, and also operation of currently used ac machines at variable speed, by supplying them from an inverter. In [Malik and Kluge (1998)] it is reported that 97% of the installed medium-voltage (M-V) motors operate at fixed speed, and only 3% are variable speed drives. Application of adjustable speed drives to many process control applications can result in a substantial saving of energy. An interesting fact related to the efficiency and power saving is that replacement of fixed speed M-V motors with variable speed drives results in a payback time of investment from 1 to 2.5 years [Schmitt and Sommer (2001)], and projected life-time of such systems is usually much longer.

Usage of inverters has a lot of consequences in industry. For example, ac machines are not necessarily constructed for 50Hz operation, and they can be adapted and optimised for a certain application. Also, ac machines are not any more limited to three phases, as they were limited by the grid supply. Voltage source inverters (VSIs) are predominantly in use in practice. Something that was a problem in the early days is more complicated control structure of ac machines, but with new digital signal processors (DSPs) this problem has been overcome.

Utilisation of multiphase machines is one of the solutions for improving performance in high power applications. Since power limitation ratings are per phase, utilisation of more phases allows obtaining of the higher power structures. Typical applications where multiphase machines are viable solutions are ship propulsion, railway traction, electric and hybrid electric vehicles, the 'more-electric' aircrafts, and the high-

power industrial applications (rolling mills, compressors, etc.) [Levi et al. (2007), Levi (2008)]. It should be noted that the predominantly utilised configuration of supply in variable-speed drives consists of two-level voltage source inverters at low voltage levels. However, current industrial standard in M-V variable speed drives is utilisation of multilevel (predominantly three-level) VSIs in conjunction with three-phase machines [Rodríguez et al. (2007)]. Utilisation of multilevel inverters in medium-voltage applications was the only solution to overcome shortcomings of used components, whose maximum voltage ratings are usually insufficient. This is the second way for increasing the system power ratings.

Utilisation of multiphase machines supplied from multilevel inverters is currently under development, and still has not been used in practice. At present it seems like the most logical way forward to combine benefits of both multilevel inverters and multiphase machines. This requires suitable supply control algorithms. Therefore, control algorithms, i.e. pulse width modulation (PWM) strategies, for single-sided supplied multiphase machines with star-connected winding with isolated neutral point, using multilevel inverters, have been investigated in this thesis (Fig. 1.1a). However, there is one more possible drive structure that can be used to achieve multilevel operation. In this case machine is supplied from two inverters. Namely, there is no star point, and the other terminals of the stator windings are also accessible and connected to the second inverter. The inverters can be two-level or multilevel. This topology is known as dual-sided supply or open-end winding configuration (Fig. 1.1b). This structure was focus of another research project that ran in parallel with this one at LJMU [Bodo (2013)]. The intention in this thesis was to cover only multiphase machines/inverters with an odd number of phases, namely five- and seven-phase structures. Even phase numbers and asymmetrical machine configurations are thus beyond the scope of this project.

The inverters are controlled digitally by pulse width modulation algorithms. Output voltage is governed by the fundamental of the output pulse sequence. In essence there are two main approaches to VSI PWM control. The first one is carrier-based (CBPWM) and the second one is space vector PWM (SVPWM). SVPWM is nowadays more popular for investigation, but not for implementation, where CBPWM is the dominant one, because of its simplicity. Since the electrical machines are one of the main energy consumers, it is very important to control them properly and improve their performance as much as possible.

Considered type of the machine in this research is an induction machine with sinusoidally distributed windings. The overall aim of the modulation strategy in this thesis is thus to produce sinusoidal output voltages, with the minimum harmonic distortion, and with minimum switching losses in the inverter. Sometimes some

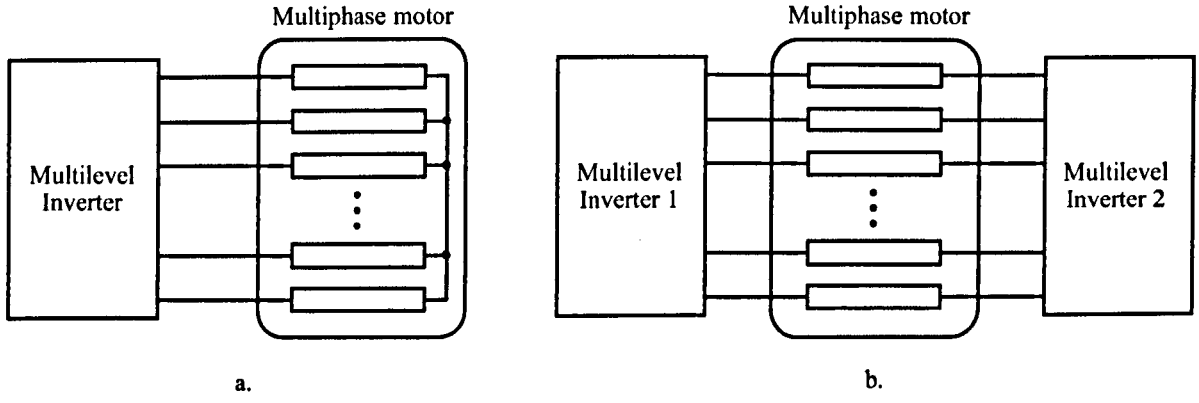


Fig. 1.1: General topology of a multilevel inverter supplying a multiphase load/machine: a. single-sided supply of a multiphase machine, b. open-end winding configuration.

additional requirements are imposed, such as balancing of the voltages of the dc bus capacitors in certain multilevel inverter structures, elimination of the common mode voltage, minimisation of current ripple, minimisation of the torque ripple, etc. Some of these additional requirements will also be analysed, when appropriate.

A short overview of the multiphase machines and multilevel inverters, with emphasis placed on the relevant modulation strategies, is given in the following section.

1.2 AN OVERVIEW OF THE MODULATION STRATEGIES

Utilisation of multilevel inverters for supply of multiphase drives is nowadays of great interest, since advantages of multiphase machines and multilevel inverters complement each other, leading to drive systems with better performance, compared to the existing solutions. Hence, construction of the modulation strategy that will make use of as many as possible good characteristics of both multiphase machines and multilevel inverters is a real challenge.

One of the first investigations of inverter-fed multiphase machine can be traced back to the late 1960s [Ward and Härer (1969)]. The obtained benefit was a reduced amplitude of the torque ripple in a five-phase machine, compared to a three-phase machine. This was given as a simple solution for torque ripple reduction using 180° conduction mode of operation. For applications with strict torque requirements PWM was advised. Nowadays, when inverters easily operate at high PWM frequency, this benefit of multiphase machines is not relevant. The other main advantages of multiphase machines that are still equally valid as in the early days are [Levi et al. (2007), Levi (2008)]:

- distribution of power over a phase number higher than three, so that for the given semiconductor ratings it becomes possible to realise a drive with the higher overall power rating; and,
- much better fault tolerance than with three-phase machines, since it is possible to continue operation of the machine with the rotating field, using modified control strategies, as long as there are at least three healthy phases regardless of the phase number.

Utilisation of multilevel inverters as the supply source results in some specific advantages such as [Rodríguez et al. (2002), Wu (2006)]:

- increase of the operating output voltage of the inverter for the given semiconductor voltage ratings;
- reduction of the dv/dt and total harmonic distortion (THD), due to the achieved output voltage waveforms with more steps of lower value;
- possibility to operate with lower switching frequency (reduced switching losses);
- input current can be with very low distortion;
- multilevel inverters enable post-fault operation;
- they are usually of modular structure, etc.

Some of disadvantages of multilevel inverters are [Seyed (2007), Panagis et al. (2008)]:

- voltage unbalance problems;
- unequal current stresses on semiconductors;
- higher implementation cost;
- reduced reliability due to an increased number of components; and

- more complex control algorithm.

Three multilevel inverter topologies that are commonly used in practice and that have found a place in commercial applications are: diode-clamped or neutral-point clamped (NPC); capacitor-clamped or flying capacitors (FC); and cascaded multi-cell with separate dc sources, cascaded H-bridge (CHB) topology [Rodríguez et al. (2002), Wu (2006)]. Multilevel inverters are nowadays widely used in conjunction with three-phase drives [Wu (2006)]. However, multiphase machines are commonly supplied from two-level inverters. One comprehensive review in this area is given in [Dujić (2008)].

Both approaches to PWM, carrier-based PWM and space vector PWM, are in use for multilevel inverters. CBPWM techniques simply extend two-level approach to multilevel, and two commonly used approaches are with level-shifted and with phase-shifted (PS) carriers [Wu (2006)]. Level-shifted carriers, further, can be with: all carriers in phase, phase disposition (PD) type; with a certain phase of carriers when they are above zero and with opposite phase when they are below zero, phase opposition disposition (POD); with carriers that alternatively change phase, alternating phase opposition disposition (APOD). These are the basic multicarrier dispositions, and some hybrids can be constructed also. Level-shifted disposition is natural modulation for diode-clamped VSIs, while phase-shifted disposition is natural for cascaded H-bridge and flying capacitor multilevel VSI topologies. On the other hand, extension of space vector modulation techniques from two to more levels is not straightforward. This is the reason why there is not any common classification of SVPWM strategies. Space vector algorithms directly apply chosen switching states to the inverter output. The number of possible switching states of a VSI is defined as l^n, where n is the number of phases and l is the number of output voltage levels per inverter leg. This gives exponential increase in the number of switching states as both the number of levels and the number of phases increase, and this represents the main problem in development and application of SVPWM algorithms. Nevertheless, some SVPWM methods are in use in industry for three-level VSIs supplying three-phase drives [Kouro et al. (2010)], although CBPWM dominates.

The first paper that gives analytical solution for multicarrier PWM strategies by comparing output leg voltage spectrum using 2-D Fourier approach is [Carrara et al. (1992)]. Basic carrier dispositions were compared and PD is favoured as one that will produce the minimal components in the phase voltage spectrum. Detailed analysis of CBPWM methods is given in [Holmes and Lipo (2003)]. Techniques are compared analytically using 2-D Fourier approach for signal spectrum calculation. Used approach is similar to the one presented in [Carrara et al. (1992)], but it is a little bit simplified. Two-level as well as multilevel CBPWM modulation strategies are analysed. Analysis is again based on spectrum calculation for single leg. Phase voltage spectrum can be obtained from leg voltage spectrum in a simple manner, and phase voltage characteristics are shown for single- and three-phase systems. Some additional works show that the same results can be obtained for different inverter topologies using different carrier-based techniques. One such comparison of multicarrier PWM strategies for multilevel inverters is given in [McGrath and Holmes (2002)], where it is shown that diode-clamped and cascaded H-bridge structures with the same or different dc voltages can perform equally if appropriate multicarrier disposition is applied.

Space-vector approach was originally used as a concept for three-phase machines. The first paper that introduced vector space decomposition (VSD) approach, and practically allowed utilisation of SVPWM concept for multiphase machines is [Zhao and Lipo (1995)]. SVPWM method performs selection of appropriate neighbouring space vectors around the reference space vector in the α-β plane and determines their dwell times

in such a way that the average value of the applied vectors equals the reference in each switching period. Since every chosen space vector has its projections into the other planes as well when the phase number is five or more, avoidance of the appearance of the undesired low-order harmonics requires that all planes are considered in the process of active space vector selection and dwell time calculation.

For the first space vector modulation strategies, for two-level three-phase systems, correlation with CBPWM was obvious, and it was confirmed by [Holmes (1992)] that SVPWM has identical performance as the CBPWM with min-max injection. Equivalence is shown also for the multiphase two-level case by [Dujić (2008)]. However, since direct control of switching states and some other advantages stem from different view of the problem, such as separation of harmonics into the mutually independent planes, space vector approach is still extensively in use and is still of the high interest.

The multilevel inverters were firstly applied to the three-phase machines. In a three-phase system only the α-β plane exists, so all space vector strategies use graphical approach. Some strategies do not apply transformation and analyse problem in 3-D space, where each axis is characterised by output leg voltage [Celanovic and Boroyevich (2001), Prats et al. (2003), Franquelo et al. (2006)]. However, in [Celanovic and Boroyevich (2001)] the problem is simplified to a 2-D plane since the sum of leg-to-leg voltages is zero, while other two references carry out analysis in the whole 3-D space. The problem with these approaches and usage of Euclidean coordinates is that the phase voltage space vector redundancy is not visible in a straightforward manner, as it is after space vector transformation. The other strategies, that use transformation, usually reduce to the determination of the triangle in which the reference is. All three-phase SVPWM strategies use the concept of the nearest three vectors. The aim of majority of these works was to give a general solution for any number of levels. One of the most cited and practically accepted as a universal three-phase SVPWM algorithm is [Celanovic and Boroyevich (2001)]. However, it does not give the complete solution, and some assumptions have to be used.

The comparison between CBPWM and SVPWM has been conducted for three-level three-phase case, and for multilevel three-phase case by [Wang (2002)] and [McGrath et al. (2003)], respectively. The common conclusion is that the space vector-like performance can be obtained using CBPWM with proper injection.

The first attempts of use of space vector concepts for multilevel multiphase drives followed three-phase algorithms. Hence, only the first plane was considered and only three space vectors were taken into account. One such algorithm is given by [Song et al. (2006)], for the five-phase three-level VSI. The consequence of using only three space vectors and not considering the other planes in a multiphase system is presence of the numerous low-order harmonics. Another group of algorithms that are aimed for a torque ripple minimisation [Huang and Corzine (2008), Hutson et al. (2008)], suffer from the same problem. The first paper that recognises problem and gives a complete solution using vector space decomposition method is [Gao and Fletcher (2010)]. This space vector algorithm is given for the three-level five-phase case. Both planes are taken into account and the algorithm provides cancelation of the space vector projections in the second plane, in order to provide sinusoidal output. The paper does not give a universal solution for an arbitrary number of level or phases, but it gives a lot of ideas that can be used for that purpose.

Another aim in developing space vector algorithms is generalisation for the multilevel multiphase case. First papers that give a universal PWM algorithm for multilevel multiphase case are [López et al. (2008b), López et al. (2009a)]. The algorithms use multidimensional space and matrix representation of the variables. An

entirely different possibility, that comes as a consequence of a series of investigations for single-phase modulators [Leon et al. (2008a), Leon et al. (2009a)], but now applied on per-phase basis in a multiphase system, has been elaborated in [Leon et al. (2010b)]. However, all of these algorithms do not use transformation of the variables and do not consider either α-β or x-y planes, and are, actually, closer to the carrier-based approach.

As it is already mentioned in section 1.1, another way of obtaining multilevel operation is open-end winding configuration. One of the first papers that introduced open-end winding configuration is [Stemmler and Guggenbach (1993)], and it was analysed for overcoming some of technological problems. The dc sources can be connected or isolated and advantages of isolated sources are also discussed here. Further, this structure was investigated by [Corzine et al. (1999)], where it was favoured when compared to the single-sided structures, since there is no capacitor voltage balancing problem and since the structure is simpler. Previously mentioned works considered three-phase machines and the first papers that apply open-end structures to multiphase machine were for a double star six-phase machine [Mohapatra et al. (2002), Mohapatra and Gopakumar (2006)]. However, these papers were not aimed at investigation of multilevel operation. The analysis of multilevel operation that can be obtained with open-end winding structure for symmetrical multiphase machines has started only recently, and some of the first results in this field are given by [Jones et al. (2010), Levi et al. (2010)].

For dual-sided supply structure, the number of switching states is given with $l_1^n \cdot l_2^n$, where l_1 and l_2 stand for the number of levels of the 1st and of the 2nd inverter, and n represents the number of phases. It can be seen that the number of switching states significantly increases with an increase in the number of phases and number of inverter voltage levels, so that development of space vector modulation strategies for open-end winding structure seems to be more involved. Detailed analysis of this topology and modulation techniques that can be applied is available in [Satiawan (2012), Bodo (2013)].

1.3 RESEARCH OBJECTIVES AND ORIGINALITY OF THE RESEARCH

The principal objectives of this research were:

1) To examine general principles of carrier-based PWM technique for inverters with more than two levels and an arbitrary odd number of phases, implement the algorithms in Matlab/Simulink environment, and verify theoretical concepts by performing extensive simulations for phase numbers equal to five and seven.
2) To investigate the rules required for the most appropriate selection of the space vectors for the space vector PWM, considering that there is a huge number of them, while the number of those applied in any switching period is always governed by the phase number (and equal to it). To develop space vector PWM techniques for five- and seven-phase drive systems supplied from three-level NPC VSI, and to verify operation by extensive simulations.
3) To derive general rules for space vector PWM algorithms based on vector space decomposition approach (VSD).
4) To investigate similarities and differences between carrier-based and space vector PWM algorithms for multilevel multiphase VSIs through the theoretical considerations and by the comparison of obtained results.
5) To perform a comparative analysis of pros and cons of space vector and carrier-based approach for multilevel multiphase inverters, and to select the best method among them for practical purposes.

6) To derive analytical formulae for leg voltage and phase voltage total harmonic distortion (THD) calculation for the most common numbers of levels and arbitrary number of phases.
7) To implement developed PWM techniques in the experimental rig and prove theoretical concepts by means of experimental investigation.

Original contributions to the field of electrical motor drives have been produced by achieving the above listed objectives. A particular contribution has been achieved by the development, for the first time, of the space vector modulation techniques for the seven-phase three-level topology, based on the vector space decomposition approach. This algorithm is described in Chapter 4. Also, significant is the mutual comparison of multiple carrier-based and space vector modulation strategies. Comparison is not only given through the simulation and experimental results analysis, but the theoretical considerations are given as well (Chapter 5 and Chapter 6). Original research results that had been generated by the thesis have been published in [Dordevic et al. (2011b), Dordevic et al. (2011a), Jones et al. (2011a), Jones et al. (2012), Dordevic et al. (2013a), Dordevic et al. (2013b)] (Chapter 4), [Dordevic et al. (2011a), Dordevic et al. (2013a)] (Chapter 5), and [Bodo et al. (2012), Dordevic et al. (2013a), Dordevic et al. (2013b)] (Chapter 6). A further contribution are still unpublished but for the first time obtained analytical formulae for the leg and phase voltage THD, given in Chapter 7. The papers, which are the outputs of the thesis, are given in Appendix B.

1.4 ORGANISATION OF THE THESIS

The thesis is divided into 8 chapters.

Chapter 1 contains a brief overview of utilisation of induction machines and explains shift of the focus of the research in this field from two-level inverters to multilevel structures and from three-phase to multiphase systems. It introduces ideas how modulation algorithms are adapted from standard three-phase two-level forms to multiphase multilevel topologies. Objectives and originality of the research are addressed towards the end of this chapter.

Chapter 2 presents literature survey. The emphasis is placed on modulation strategies for obtaining the sinusoidal output. Carrier-based techniques are surveyed at first, since they are very simple for realisation and can be used as a good reference for comparison with other methods. Space vector strategies are considered next, for three-phase multilevel, multiphase two-level, and multilevel multiphase drives, when neutral point of the machine is present. A brief review of open-end winding configurations is also given.

Chapter 3 introduces basic concepts, rules, definitions, and equations that will be used in this research. General structure and general equations of multilevel multiphase systems are analysed and the nature of signals is explained. Space vector transformation is defined and it is shown how it can be used for simple plotting of space vector projections into decoupled planes. General equations for calculation of space vector application times are further given. Mapping of the harmonics into 2-D planes is shown. Basic multilevel inverter topologies with their main advantages and drawbacks are surveyed.

Chapter 4 analyses space vector modulation strategies based on the VSD approach, for five- and seven-phase three-level VSIs. The first paper in this area that gives a complete solution and that analyses both planes for five-phase three-level case is [Gao and Fletcher (2010)]. This algorithm is explained in detail in this chapter with some specific solutions that are further used for development of the seven-phase three-level SVPWM algorithm. One modification of the algorithm is also presented. General structure of the VSD space vector

algorithms is given as well. Simulation and experimental results for a five-phase induction machine and a seven-phase *R–L* load are included in this chapter.

Chapter 5 examines carrier-based PWM algorithms, the aim being a comparison with SVPWM. Reduction of level-shifted multicarrier PWM to single-carrier PWM is shown. Change of the switching sequence, as a function of the number of phases and number of levels, as well as the dependence on the modulation index value, is analysed in time domain. Pure sinusoidal reference signals and signals with included min-max injection and with 'double' min-max injection are covered.

In Chapter 6 theoretical analysis of the switching sequences and regions of application of analysed space vector and carrier-based modulation strategies is given at first. Equivalence of one carrier-based and one space vector modulation strategy is revealed. Further, analysed modulation strategies are compared using waveforms obtained by simulations and experiments. Mentioned equivalence is thus confirmed.

Chapter 7 derives analytical formulae for leg and phase voltage RMS and THD. Derivations are based on the time domain analysis. Power of the signal, defined as a squared value of the signal, is used for derivation. Sinusoidal reference signal has been analysed. General formula for leg-voltage THD, produced by an *l*-level inverter, with equal output voltage steps is given. General formulae for phase-voltage THD produced by two-level inverter and for three-level inverter with PD and (A)POD carriers disposition, and for any number of phases, are derived. Theoretical curves are verified by simulation and experimental results. An extensive set of measurements for three-, five- and six-phase symmetrical induction machine and for seven-phase *R–L* load and for the whole modulation index range is included in this chapter.

Chapter 8 summarises work described in the thesis and gives the main conclusions. It also introduces some ideas that are not analysed in detail in this thesis and thus represent directions for the future work.

Chapter 9 gives the list of references used in this research.

Finally, in the appendices, description of the experimental setup, hardware and software, and the publications from the thesis are given.

Chapter 2

LITERATURE SURVEY

2.1 INTRODUCTION

The literature review in this chapter is focused on modulation techniques for star-connected multiphase machines with multilevel inverter supply. Three topologies are very closely connected with this topic: three-phase machines supplied from multilevel inverters; multiphase machines supplied from two-level inverters; and machines with dual-sided supply (open-end winding configuration). In addition to space vector approach, carrier-based approach, almost universal and similar for any number of phases and levels, is always available. Literature surveys for three-phase machines supplied from two-level inverters, for both carrier-based and space vector modulation strategy, and two-level carrier-based techniques applied to multiphase machines are omitted here as these are well-known methods. The review of literature in this chapter is divided into five logical parts, which are arranged historically as they were appearing.

Prior to the survey of the areas closely connected to this research, a short review of multiphase machines and multilevel inverters is due. Very good and comprehensive surveys of multiphase machines that include basic properties of multiphase machines, their variety, modelling, vector control, direct torque control, PWM strategies, fault tolerant strategies, multiphase multi-motor drive systems with single inverter supply, etc. are available in [Levi et al. (2007), Levi (2008)]. Surveys of three-phase multilevel inverters, including basic topologies, control and modulation strategies, industrial applications and technological aspects are given in [Rodríguez et al. (2002), Rodríguez et al. (2007)]. Also, [Seyed (2007)] represents a very good source that in detail compares three-phase multilevel converters for medium-voltage application. Some more recent reviews in this area are [Abu-Rub et al. (2010), Kouro et al. (2010)], which give recent data regarding technology, advantages, challenges and requirements for multilevel inverter applications. All of the mentioned multilevel inverter surveys are dedicated to three-phase systems.

2.2 CARRIER-BASED TECHNIQUES FOR MULTILEVEL INVERTERS

Carrier-based PWM techniques are well-established for three-phase multilevel VSIs. They simply extend two-level PWM approach to multilevel inverters. The extension is usually based on application of more than one carrier. Difference between these methods is in mutual disposition of carriers. The most common dispositions and thus multilevel carrier-based strategies are: phase-shifted (PS), in-phase disposition (PD) that is also known as level-shifted (LS) carriers, phase opposition disposition (POD), and alternative phase opposition disposition (APOD). Some hybrid carrier-based strategies are also available. As in the two-level case, the number of phases for all of these multilevel carrier-based techniques is not relevant, but there is not much evidence regarding

consequences of application of different CBPWM techniques to multilevel multiphase inverters supplying multiphase machines.

Since the process of producing PWM signal with carrier-based methods is independent of the number of phases, review of some basic works that analyse output leg voltage spectrum and compare CBPWM strategies for multilevel inverters using single-phase example is given first.

Mathematical analysis of spectrum characteristic, for different types of carrier-based techniques for multilevel inverters, is presented in [Carrara et al. (1992)]. All mentioned carrier disposition techniques (except for hybrid) are analysed. Analysis is based on a single output leg voltage spectrum. A method for application of two-dimensional Fourier transformation is presented. The analysis is given for the general case and it is not related to any of the specific inverter topologies. It is shown that level-shifted disposition has in general lower values of the harmonics except for the harmonic at the switching frequency. It is also concluded that in three-phase case this harmonic will not be present in the phase voltages, so that this method is favoured compared to others. Note that this conclusion also remains valid for any other number of phases greater than three. This type of analysis is further conducted in [Holmes and Lipo (2003)]. A similar analytical approach is used. Comparison of all carrier displacement methods for both linear and overmodulation range, including details regarding solving two-dimensional Fourier transformation, is given.

A similar comparison, but based on simulation results, is presented in [Calais et al. (2001)]. Single-phase five-level cascaded H-bridge (CHB) structure is analysed. Apart from the spectrum, for which the same conclusions as in [Carrara et al. (1992)] are given, resulting switching frequency and complexity of implementation regarding use of redundant switching states are discussed. One hybrid method is also analysed. PD method has unbalanced switch utilisation, for different values of the modulation index, in contrast to PS/APOD. Hybrid method has the same spectrum as PD and even better utilisation of switches, but it is the most complex to implement. Influence of the number of levels on spectrum and harmonic distortion through the extensive simulations for different carrier-based techniques was analysed in [Agelidis and Calais (1998)]. Results include both linear and overmodulation range. A further comprehensive analysis of carrier-based modulations for multilevel three-phase topologies is given in [Wu (2006)]. Different types of carrier disposition methods for most common topologies, their comparison, and calculation of device switching frequency are explained.

An analytical comparison, again for three-phase multilevel inverters is given in [McGrath and Holmes (2002)]. It is shown that alterative phase opposition disposition (APOD) based PWM for diode-clamped inverters, phase-shifted (PS) carriers for cascaded inverters, and hybrid PWM for hybrid inverters (cascaded with different dc voltages) have the same spectrum of the inverter leg voltages. Parameters of carriers are adjusted in such a way that compared methods have the same number of switch transitions during one period of the reference signal. The analysis is conducted using the double Fourier series (similarly to [Carrara et al. (1992)]), but a different analytical approach is used. Superiority of the level-shifted carrier-disposition, by placing significant harmonic at the switching frequency, so that it cancels in phase voltage, is once again proved. A new solution is further developed for CHB regular and hybrid structure. It uses discontinuous PWM with phase-shifted carries within each H-bridge. This modulation strategy gives very similar harmonic characteristics with cascaded structures, as PD gives with diode-clamped inverters.

As already mentioned, there are only a few studies regarding comparison and consequences that application of carrier-based modulation strategies for multilevel inverters can produce in multiphase machines. Some of the papers, mentioned further on, are more focused on capacitor voltage balancing strategies, than on behaviour of the machine.

One example of multilevel (three-level) multiphase (five-phase) carrier-based modulation study is presented in [Mwinyiwiwa et al. (2006)]. The inverter is of NPC topology and modulation is with two level-shifted triangular carriers. A simple hysteresis regulator for capacitor voltage balancing has been presented. It requires only the value of the neutral-point voltage. Developed modulation scheme has been verified through the simulations and experiments on a static *R-L* load. A DSP board and an FPGA device have been used for the experimental implementation. A very similar configuration, with the same aim, was analysed in [Karugaba et al. (2011)]. A further analysis of multilevel multiphase carrier-based strategy is given in [Nho and Lee (2007)]. Five-level, five-phase NPC structure is analysed. However, shown results are not explained in detail.

Some modified carrier-based strategies for dc-link capacitor voltage balancing for multilevel multiphase diode-clamped inverters are presented in [Busquets-Monge and Ruderman (2010)]. Proposed techniques are universal for any number of phases and any number of levels. All techniques guarantee balancing of capacitor voltages in each switching period without any additional hardware (provided that the sum of output leg currents is equal to zero). Improvement of the output voltage spectrum characteristics is obtained at the expense of an increased algorithm implementation complexity, which is in the proposed methods usually based on changing the angle between phase-shifted carriers.

2.3 SPACE VECTOR TECHNIQUES FOR THREE-PHASE MULTILEVEL INVERTERS

Multilevel inverters are nowadays widely used in conjunction with three-phase drives. Some of the space vector algorithms are in use in industry for multilevel converters, but only for the three-level case [Kouro et al. (2010)]. Extension of space vector modulation techniques from two to more levels is not a straightforward process even for the three-phase case. In [Celanovic and Boroyevich (2001)] one solution for extension of space vector modulation technique to any number of levels for the three-phase case is presented. This paper uses for the first time 3-D Euclidean coordinate system for leg-to-leg voltages for space vector representation. Since the sum of leg-to-leg voltages is zero, the problem is reduced to a 2-D plane. This also leads to the reduced computational load. The paper also introduces a transformation matrix and introduces a new *g-h* coordinate system. This transformation was usually regarded as the main disadvantage of the algorithm and it has been removed in a newer version of this method in [Castro et al. (2010)]. The original algorithm also assumes that the best approach to PWM is to use the three nearest vectors. It proposes one interesting logic that compares reference voltage with the first smaller and the first greater integer projections to g and h axes, for online determination of the switching state that will be used. The algorithm does not address the redundant switching state selection, so it does not give a unique solution. The problem is that the applied inverse transformation is not completely determined, so some assumptions have to be used.

In [Prats et al. (2003)] another 3-D method, based on geometrical considerations, is presented. It is also designed for three-phase converters with any number of levels. 3-D approaches actually attempt to visualize the problem and to link mathematical definition of orthogonality with geometrical imagination of it. Instead of α, β

and 0^+ axes, another set of also mutually orthogonal, 3-D Euclidean x, y, z, coordinates is used. Generally, if the system is unbalanced or if triplen harmonics are present, the reference vector cannot be placed in the single 2-D plane. Because of this, the paper identifies and uses the four vectors nearest to the reference vector. The vertices of the tetrahedron, to which the reference belongs, are the chosen space vectors. For the reason of minimisation of switching losses, each of the sequences contains two leg voltage space vectors that belong to the main diagonal of the cube. However, these leg voltage space vectors are actually redundant for the phase voltage space vectors, although the redundancy is not observable in the Euclidean coordinates, in contrast to the α-β plane. The 3-D methodology idea, based on using x, y, z, coordinates is extended in [Franquelo et al. (2006)] to four-leg multilevel converters. This paper also gives a complete solution for any number of levels. In contrast to [Prats et al. (2003)], switching state redundancy is here taken into account.

Another approach with the same aim, to create one universal multilevel three-phase space vector algorithm, is presented in [Gupta and Khambadkone (2006)]. Here multilevel sectors are reduced to two-level sectors. Reduction is done by considering each triangle separately, rather than the whole hexagon, as in [Holmes and Lipo (2003)]. Using projections on α and β axes, the method introduces rhombus and triangles determination. The proposed algorithm contains primary and secondary unit. The primary unit determines the sector, triangle number, and, from the fractional part of the reference, it determines application times within the two-level SVPWM block. The secondary unit generates gating signals using determined sector, triangle inside the sector, and times of application. Experimental results for three-level NPC and five-level CHB inverter are given.

In [Massoud et al. (2008)], a numerical analysis-based generalised algorithm for generating multilevel three-phase SVPWM, without any mapping to the two-level case, is presented. The algorithm uses the "three nearest vectors" strategy and it is compared with some of the previously described algorithms. Utilisation of redundancy is suggested. Experimental results for a three-level three-phase active power filter are given.

In [Kanchan et al. (2005)], a space vector modulation algorithm for the three-phase multilevel case is given. Presented modulation strategy is actually analogous to the carrier-based solution given by [McGrath et al. (2003)], in the base modulation index range. As an extension, a specific solution for the overmodulation range is also given.

As can be seen from the surveyed references, one of the aims in this area is the generalisation of three-phase space vector modulation techniques to any number of levels. The second aim is comparison of three-phase space vector modulation strategies with carrier-based approaches. For example, for two-level three-phase case it has been shown that both strategies can lead to the same results [Holmes (1992)].

Similarities between carrier-based and space vector approaches for three-level three-phase system are shown in [Wang (2002)]. It is shown in this paper that two techniques can be made equivalent through proper selection of the common-mode voltage (CMV) injection in the case of carrier-based modulation, or dwell time sub-division for the redundant switching states in the case of space vector modulation. The proof is provided in both directions. Firstly, times of application for each switching state of each sub-sector are mathematically expressed. Further, assuming that the application time of the redundant state is equally split, analytical expression for voltage reference value in each sub-sector is obtained from the averaging equation. For each value of the modulation index CMV is determined and it is concluded that, by applying that shape of CMV in CBPWM approach, space vector-like performance can be obtained. In the opposite direction, it is shown that for

any combination of reference voltage levels in the CBPWM method, the sub-sector with the same times of application per space vector can be found and therefore it can be obtained using space vector approach. Finally, one way of injection construction is proposed for simplified implementation of the space vector modulation using carrier-based approach.

In [McGrath et al. (2003)] the idea of proper injection that leads to space vector-like operation is extended to the multilevel case. As a general three-phase multilevel space vector algorithm, the one proposed in [Celanovic and Boroyevich (2001)] is adopted. It is also shown that equal sub-division of the application time of redundant switching states is the optimal choice for flux and current ripple minimisation in the three-phase case. Construction of the injection that provides equal sub-division for the redundant switching state application times is done in a simple manner. Injection can be constructed in three steps: centring signals using min-max injection, applying modulus function and then once again centring. This method is simpler and more universal than the specific solution given in [Wang (2002)] for the three-phase three-level VSI. The idea from [McGrath et al. (2003)] is also contained in [Holmes and Lipo (2003)], where it is additionally shown that two modulation approaches, carrier-based and space vector approach, effectively produce the same result.

[Yao et al. (2008)] compares some carrier-based and space vector modulation techniques for three-phase multilevel inverters with an arbitrary number of levels. As a basic algorithm [Celanovic and Boroyevich (2001)] is used again. It is mentioned that CBPWM and SVPWM techniques can lead to the same performance when four or less switching states during each switching period are used. However, it is proposed to use more redundant switching states during the switching period whenever possible. The length of the sequence is longer as the reference voltage vector magnitude gets smaller, due to the higher degree of redundancy of small space vectors and possibility to use them fewer times (by taking their redundant switching states). In fact, the paper proves well-known fact that the quality of a modulation technique is the trade-off between device switching frequency and output voltage characteristic. Thus the improvements in the output voltage spectrum are obtained at the expense of increased losses.

Comparison of carrier-based and space vector modulation techniques for three-phase multilevel inverters is conducted also in [Pereira and Martins (2009b), Pereira and Martins (2009a)]. The comparison is based on the capacitor voltage balancing strategies in both techniques, using three-level VSI as an example. In carrier-based techniques capacitor voltage balancing is obtained using common mode voltage injection. In space vector modulation strategies, it is usually solved using some form of manipulation of redundant switching states, where their relative duration compensates the error in the neutral-point voltage. It is shown that both approaches are essentially the same.

2.4 SPACE VECTOR TECHNIQUES FOR MULTIPHASE TWO-LEVEL INVERTERS

None of the afore mentioned three-phase two-level or multilevel space vector algorithms can be directly extended to a multiphase structure (extension of multilevel SVPWM techniques to multiphase case will be discussed in the next section). Space vectors represent the values of motor phase voltages with discrete states of inverter outputs. They contain data of all phase states in a single vector. This is in general a multidimensional structure, with the dimension equal to the number of phases. Due to the isolated neutral point the dimension of the problem can be reduced to $(n-1)$ and a graphical representation in a single plane is possible for three-phase

inverters (all algorithms of the previous sub-section use graphical representation of space vectors). In a symmetrical multiphase case more orthogonal planes are present, so solution of the problem regarding only the first α-β plane is not sufficient. For higher phase numbers ($n \geq 5$) direct graphical representation becomes impossible. The idea of vector space decomposition (VSD) into orthogonal planes, which enables a new way of graphical interpretation, was introduced by [Zhao and Lipo (1995)]. The analysed structure was a six-phase double-star asymmetrical induction machine supplied from two two-level three-phase inverters. Using VSD approach, vector space is decomposed into $(n-1)/2$ 2-D planes and one zero axis for odd n, and $(n-2)/2$ 2-D planes plus two zero axes for even n. The planes and axes are mutually orthogonal for the symmetrical case and they are usually denoted as α-β, x_1-y_1, x_2-y_2,... planes, and as 0^+ and 0^- axis. Development of the SVPWM schemes for multiphase machines most frequently follows this principle of the vector space decomposition.

Since space vector strategies are usually dependent on the number of phases and symmetry of the machine, classification of electrical machines should be done at first. Depending on the number of phases and their arrangement, multiphase machines can be classified into the following groups: 1) asymmetrical multiphase machines (commonly considered are those that consist of k three-phase windings ($n=3k$), spatially shifted by π/n, with k isolated neutral points), and symmetrical multiphase machines with 2) even or 3) odd number of phases (spatial shift between any two consecutive phases is $2\pi/n$). In all the cases when the phase number is not a prime number, the winding may have one or k isolated neutral points.

Control of the first category was studied by [Gopakumar et al. (1993)]. It was shown that if an asymmetrical six-phase machine is supplied from a VSI controlled using 180° conduction mode or the simplest SVPWM, large harmonic non-flux/torque producing currents appear in the machine. The solution of this problem was given later by [Zhao and Lipo (1995)] with already mentioned concept of the VSD and an appropriate PWM control.

Symmetrical multiphase machines with even number of phases are not commonly used in practice. A SVPWM scheme for a symmetrical six-phase machine with a single neutral point, using VSD approach, for various selections of active space vectors within the switching period, is given in [Dujic et al. (2006)]. Symmetrical multiphase machines with an even phase number are normally configured as machines with $n/2$ phases, by connecting pairs of phases in spatial opposition into a single phase.

Space vector PWM methods for symmetrical multiphase machines with an odd number of phases have been investigated most frequently in recent times. A SVPWM method for a symmetrical five-phase machine, which leads to the sinusoidal VSI output, was presented by [de Silva et al. (2004)]. Two large and two medium space vectors were used. Cancellation of space vector projections in the second plane is provided on average in each switching period. The same results were obtained by [Iqbal and Levi (2005), Iqbal and Levi (2006)], but with a different scheme for dwell time calculation. In principle, for obtaining pure sinusoidal output voltage, the number of applied space vectors must equal the number of phases [Kelly et al. (2003)], and this principle is also applied in the previous three papers. Selection of active space vectors must be performed considering all planes simultaneously, if the fundamental and low-order harmonics are to be correctly controlled.

A space vector method for a two-level seven-phase inverter was investigated in [Grandi et al. (2006b)]. Six active and the zero space vector were used. Dwell times were calculated in such a way that the cancellation of the 5^{th} and 3^{rd} harmonics in the 2^{nd} (x_1-y_1) and 3^{rd} (x_2-y_2) plane, respectively, was achieved. The proposed method requires one commutation per leg in each switching period, with the possibility to share the zero voltage

vector between the two zero states. Dc bus utilisation is increased by 2.57% compared to the pure sinusoidal modulation, but this value is smaller than in the five-phase case (which is considerably smaller than for a three-phase system).

A nine-phase machine with a single neutral point was analyzed by [Kelly et al. (2003)] and [Grandi et al. (2007)]. The first paper utilises carrier-based approach to simplify calculations. With injection of all harmonics that are odd multiples of the number of phases, obtained results are the same as those achievable with the SVPWM. The second paper gives a complete solution for the SVPWM, with the analysis conducted simultaneously for all four planes.

There are also some PWM methods that have been developed for higher numbers of phases. These however by and large follow the same methodology as reviewed here for lower phase numbers and in essence rely on the principles of PWM for multiphase systems, established in [Kelly et al. (2003)]. A generalised space vector PWM approach for sinusoidal output voltage generation with two-level multiphase voltage source inverters is presented in [Dujić (2008), Dujic et al. (2009)]. The analysed number of phases is an odd number. According to the proposed method, tedious analysis of 2^n space vectors can be completely avoided.

Usually, the only desired non-zero space vector components are in the flux/torque producing α-β plane. The situation is however different in series-connected multiphase drives supplied from a single inverter [Levi et al. (2004), Iqbal (2005), Jones (2005)] and in concentrated winding machines [Toliyat et al. (1991), Locment et al. (2006)], where non-zero reference components exist also in other planes. In the first case harmonics from the x-y plane of the first machine appear in the α-β plane of the second machine and vice versa, due to the method of phase connection, and machines are with the sinusoidally distributed windings. In the second case non-zero harmonic from the second plane is used for torque enhancement of the five-phase machine with concentrated windings.

The PWM strategies for two-level VSIs supplying multiphase machines are comprehensively covered in [Dujić (2008)], which also provides a detailed literature survey in this area until 2008. Moreover, comparison between carrier-based and space vector approach is given with the conclusion that the only difference is in the zero space vector application time management. The equivalence of the SVPWM (with assumption of equal sub-division of the application time between redundant switching states) and carrier-based modulation strategy with triangular signal injection (min-max injection) is shown.

2.5 SPACE VECTOR TECHNIQUES FOR MULTIPHASE MULTILEVEL INVERTERS

PWM techniques for multiphase multilevel inverters have started attracting attention only recently [Levi (2008)]. Due to the perceived advantages of combining multilevel inverters and multiphase machines, new modulation strategies that will provide desired output voltage in the best way are necessary. The development of new space vector strategies is very difficult because the number of space vectors that has to be handled becomes extremely large even for a small increase of the number of phases and number of levels.

The distinction between carrier-based and space vector techniques is not always clear. Some of the techniques are actually closer to something that can be classified as a separate group, that could be named as graphical or matrix methods, since they in essence describe carrier-based methods through flow charts or

equations. However, the majority of these ideas are presented in literature as space vector modulation techniques. Such PWM methods will be surveyed in this sub-section.

Probably the first paper that analyses application of multilevel topology for multiphase machines, as an option to additionally reduce torque ripple and in that way integrate these two technologies, is [Lu and Corzine (2005)]. A three-level five-phase NPC structure is discussed and compared through simulation results with two-level five-phase structure. It is shown that a proper selection of the vectors can be used to reduce the torque ripple. Modulation range is divided into three parts and for each an individual control strategy is presented. The current THD is increased for higher modulation index values. However, it is argued that the current distortion may not be a disadvantage in some specific applications such as analysed naval propulsion, where the torque ripple performance and high dc bus utilisation are the major concerns. One of conclusions of this work is that in the five-phase case the voltage/current THD is not any more relevant indicator of torque performance.

The first SVPWM techniques for multiphase VSIs were based on the simple extension of the three-phase multilevel SVPWM approaches, so that only the three vectors, nearest to the reference, were utilised. Such an extension from the three-phase to five-phase system, that divides each sector into four equal triangles, is given for a three-level inverter in [Song et al. (2006)]. As already mentioned, the number of applied vectors must equal the number of phases [Kelly et al. (2003)]. Utilisation of three instead of five space vectors during the switching period disregards this basic rule, only the first plane of the multiphase system is controlled, and therefore the other planes are not controlled. Hence numerous low-order harmonics are generated, which map into the second plane. The same applies to the work described in [Huang and Corzine (2008)], where 'walking' pattern around reference voltage is presented for a five-phase three-level VSI. The aim of this algorithm was minimisation of the torque ripple. This was achieved, however at the expense of large low-order harmonics in the second plane. A further example of the SVPWM for three-level five-phase VSI, again based on use of only three vectors, is the one in [Hutson et al. (2008)], where an optimal SVPWM switching strategy, based on modified discrete particle swarm optimisation (PSO), is presented. It is demonstrated for few modulation indices using the three-level five-phase machine model.

A space vector PWM technique for a five-phase three-level VSI, based on the decomposition of the five-dimensional space into 2-D planes, has been introduced in [Gao and Fletcher (2010)]. The considered topology is a five-phase three-level NPC VSI. The rule of using n vectors is respected in this paper. The reference voltage is in the first plane, while in the second plane one has to achieve zero voltage (on average) during each switching period. The technique at first eliminates some of the switching states that do not follow required phase order in time domain and significantly reduces the number of switching states from 243 to 113. The algorithm further searches for the possible switching sequences that produce level increase by one in each leg and groups redundant sequences together. Elimination of those that cannot be cancelled in the second plane is done next. With the simple rule, that the time of application must be in the range 0 to T_s, partition of the sectors into sub-sectors can be done. Final sequences are chosen to contain more 'ones' (output leg voltage is determined with dc bus midpoint) for better capacitor voltage balancing. [Gao and Fletcher (2010)] is probably the only paper that uses VSD approach and gives the complete solution for sinusoidal output generation for one concrete example of the single-sided supply of a multilevel multiphase drive system. It has been used as a basis for some of the developments in this thesis. The definition of the space vectors in this paper is the same as it is in this thesis

(section 3.4), and also the drive topology and the aim of sinusoidal output generation are the same as in this research.

A rather different approach to development of a SVPWM technique for a multilevel multiphase system is given for the general case of an l-level, n-phase VSI in [López et al. (2008b), López et al. (2009a)]. The algorithms are based on the considerations of the multidimensional (n-dimensional) space and they therefore do not include decomposition of the n-dimensional space into 2-D planes (i.e. VSD approach). Matrix approach is used in these papers.

A space vector PWM algorithm that can be applied to any number of phases and any number of levels is presented in [López et al. (2008b)]. The vector space is not transformed, so that decoupling transformation is not applied (as usually the case is in SVPWM algorithms). It is demonstrated that the multilevel multiphase modulator can be realised using a two-level modulator. One realisation of such a SVPWM two-level modulator is presented. Realisation is given in the matrix form and is based on re-ordering of the two-level (fractional) parts of references in a decreasing order and on re-ordering of the corresponding leg voltages in the same manner. Re-ordering takes place in each switching period and is stored in an appropriate matrix. The CHB inverter is used and the star of the load is connected to the mid-point of the inverter, so that the phase voltages are equal to the corresponding leg voltages. In this way the algorithm deals with leg voltages, and does not take redundancy into account. It is interesting to note that the starting point of the algorithm are not the switching states or space vectors. They are actually one of the final products of the algorithm. The algorithm is tested experimentally on a five-level five-phase CHB inverter.

Application of [López et al. (2008b)] algorithm to the three-phase VSI and its comparison with 3-D algorithm [Prats et al. (2003)] is given in [López et al. (2008a)]. It is shown that two algorithms are nearly the same. The only difference is in the applied switching state when two reference signals have the same value. However, the time of application of this state is zero, and it does not affect the final result. Which of the two legs that have the same references will switch the first is not important.

Use of redundancy actually means that the algorithm takes into account star-connected load structure. In that case some other parameters become important and should be considered as well. Such parameters are the linear modulation index range, fault tolerance, switching losses, capacitor voltage balancing etc. Enhancement of the previous algorithm [López et al. (2008b)], using redundancy of the converter switching states, is given in [López et al. (2009a)]. The algorithm now controls the load with an isolated neutral point. It is shown that the n-phase multilevel SVPWM modulator can be realised by means of a two-level (n–1)-phase SVPWM algorithm without redundancy. The dimension of the system is apparently reduced, but this is so since the whole application time of the redundant switching states is used for only one of them. Low computational cost of the algorithm is proved by simulations and experiments.

A somewhat similar method, in the sense that VSD decomposition into 2-D planes is not utilised, is the one in [Leon et al. (2010b)], where a multilevel multiphase PWM is developed using n single-phase modulators. The method is illustrated through the flow chart interpretation of a graphical method, which is actually a carrier-based method. For better understanding and easier analysis of this paper, which gives solution for any number of levels and any number of phases, a review of some single-phase multilevel space vector modulation strategies is also given in this chapter. These single-phase strategies are the basis for the mentioned multilevel multiphase algorithms.

In [Leon et al. (2007)] a single-phase (two-leg) inverter is analysed. The load is placed between two leg outputs of the three-level neutral-point clamped inverter. Vectors are represented in one-dimensional control region. The "two-nearest vectors" space vector modulation strategy (N2V-SVPWM) is presented. The modulation strategy is very simple and is based on the geometrical properties. The main algorithm does not use switching state redundancy. Two modifications of the basic algorithm that use this property, for improvement of the capacitor dc voltage balancing and for minimisation of losses, are presented. At the end one generalised form of N2V-SVM is given. All results are proven on a 150kVA diode-clamped inverter.

A similar analysis, but now for cascaded H-bridge topology, is given in [Leon et al. (2008b)]. The algorithm is presented for two-cell CHB with the same dc bus voltages and for a hybrid topology with dc voltage ratio of 3:1. In the hybrid structure output voltage quality is improved but redundancy that can be used for specific applications disappears. Capacitor voltage balancing features are examined when converter is used in rectifying mode of operation (in inverter mode, voltage on capacitors of CHB is constant if independent dc sources are used for each cell). Only simulation results are given, while experimental results and the missing dc voltage ratio 2:1 are covered in [Leon et al. (2009a)].

A follow-up paper is [Leon et al. (2008a)], where all the most popular topologies are analysed. The algorithm from [Leon et al. (2007)] for diode-clamped topology is rewritten in a simplified manner, and named as 1DM. It is shown that the same solution can be applied to the flying capacitor topology. Of course, for required output leg voltages different, specific switching states must be applied. A hybrid version of FC is also analysed. Experimental results are shown for the diode-clamped and cascaded inverter (with dc voltage ratios 1:1 and 3:1) configurations. Only the lower switching states are used in the experiments. Redundancy is analysed for capacitor voltage balancing problem and all three topologies are covered. The algorithm is always simple and it is usually not dependent on the number of levels.

In [Leon et al. (2009b)] the error of the dc bus voltage ratio in the CHB structure is analysed. Actually, the ratio of dc bus voltages can be arbitrary. The voltage and current waveform distortion that can appear are avoided with introduced feedforward SVPWM technique. Since plenty of cases are possible, only a two-cell converter is analysed (simplicity of the algorithm extension to multi-cell case is mentioned). Experimental results are given.

The transition from single-phase to multiphase topologies is shown in the already mentioned paper [Leon et al. (2010b)]. It is shown here that single-phase strategy, 1DM, introduced in [Leon et al. (2008a)], can be directly used for multiphase converters, by applying it to each leg separately. The method is also analytically (through the given examples) and experimentally compared with 2-D, 3-D and multiphase multilevel modulation strategies. As the characteristic examples for each of these categories, [Celanovic and Boroyevich (2001)], [Prats et al. (2003)] and [López et al. (2008b)] are chosen, respectively. All compared strategies give the same results and can be easily obtained with 1DM strategy. The difference between analysed 2-D SVPWM algorithm and 1DM in common mode voltage is addressed, but shown leg-to-leg voltages where CMV effect is not present, are identical.

The value of [Leon et al. (2010b)] paper is even greater, since it actually shows the equivalence of some space vector techniques with level-shifted CBPWM. Namely, the analysed 1DM technique directly replicates behaviour of level-shifted triangular-carrier (graphical approach) PWM principle into flow chart algorithm that is introduced as a new modulation technique, called 1DM. It is mentioned in the paper that the 1DM control

strategy eliminates CMV, which means that modulation signals in the CBPWM should be without any injections. Redundancy of switching states is not used in this way. This type of a modulator, which does not use redundancy, is actually analysed in [Leon et al. (2010b)], and is called raw modulator. The same 1DM technique is in essence used in all the previously mentioned single-phase related papers, but the name of the technique varies.

The algorithm presented in [López et al. (2008b)] does not take into account possible dc capacitor voltage imbalance. One solution for the voltage imbalance problem for multilevel multiphase converters is shown in [Leon et al. (2010a)]. As a basic algorithm, it uses solution from [López et al. (2008b)], and in this way extends the scope of its applicability. The solution is given in a general manner for any type of the converter and is described as feedforward SVPWM technique. It is given in matrix form, but actually each row of the matrix corresponds to the single phase. The control in each phase is done by finding and using the nearest obtainable leg voltages. Experimental results for different types of dc voltage disturbances are shown (sinusoidal oscillation, failure of one dc source). The output voltage in all cases follows the reference on average.

A different approach to analysing control region of a cascaded H-bridge inverter configuration is given in [Leon et al. (2011)]. The modulation technique is given for one leg, so that it can be easily applied to a multiphase case, although this is not mentioned in the paper. Positions of the switching states for phase-shifted, level-shifted and hybrid carrier-based techniques and single-dimensional technique from [Leon et al. (2008a)] are shown using the new representation of the control region. Feedforward version of the introduced technique is also given, and the results are verified by experiments.

2.6 MODULATION TECHNIQUES FOR OPEN-END WINDING CONFIGURATIONS

Use of an open-end winding configuration is an alternative way to obtain multilevel mode of operation. Analysis of modulation strategies for this configuration was conducted in two projects, which ran in parallel with this one, at LJMU [Satiawan (2012), Bodo (2013)]. Thus, only a brief review of some of the most important papers in this area is given here. Application of open-end winding structure for multiphase machines is very new, so that the majority of available references are for the three-phase case.

One of the first papers that dealt with dual-sided supply configuration is [Stemmler and Guggenbach (1993)], where utilisation of two-level and three-level inverters at both sides of a three-phase machine was discussed. Cases when dc sources are isolated (independent) and connected (common dc source) were analysed, and advantages of isolated dc source structure were explained. The open-end winding configuration was introduced here as a solution for improvement of torque harmonic characteristic and also for speed range increase, that were limited by slow GTO components available at the time.

Dual-sided supply configuration has some advantages compared to the single-sided counterpart, as discussed in [Corzine et al. (1999)]. Use of two two-level inverters for dual-sided supply configuration is analysed and it is suggested that this is a simpler topology than the classical multilevel single-sided topology. Depending on the choice of the applied dc voltages, application of two two-level inverters can yield three- or even four-level inverter equivalent voltages at the machine. This means that the equivalent single-sided topology is with either three- or four-level inverter supply. Identical performance and overall quality of operation in dual-sided supply mode and in single-side supply configuration with three- and four-level inverters are experimentally

confirmed. Reduction in the number of components and elimination of capacitor voltage balancing problem, when dual-sided configuration is applied, are also discussed in this paper [Corzine et al. (1999)].

Previously mentioned examples are some of the first references in this area and are for the three-phase case. The only previously published works that deal with open-end winding configuration for multiphase machines (the simplest case of asymmetrical dual three-phase machine was considered) are [Mohapatra et al. (2002)] and [Mohapatra and Gopakumar (2006)]. A double star six-phase machine is supplied from two three-phase two-level inverters at each side. However, the goal in these papers was not realisation of multilevel voltage waveform and such a waveform is therefore not created at all.

Some more recent works in this area are [Levi et al. (2010)] and [Jones et al. (2010)]. In [Levi et al. (2010)] the analysis of the switching states and space vectors for a five-phase machine in the open-end winding configuration, supplied from two two-level inverters with isolated dc sources, is given. The sinusoidal reference voltage is equally split between two inverters and delayed for 180°. Simulation results for carrier-based modulations are given. In [Jones et al. (2010)] unequal reference sharing is used, so that up to half of the maximum achievable output voltage only one inverter operates. The second one becomes active for higher modulation indices, leading to improved voltage THD with multilevel operation.

2.7 SUMMARY

In this chapter, a review of references relevant to this research was given. This project is focused on modulation techniques for multiphase multilevel inverters supplying load with an isolated neutral point. Table 2.1 and Table 2.2 give tabular representation of surveyed references, which as their main aim have investigation or analysis of some of the relevant modulation techniques. References are sorted according to their appearance in appropriate sections. It can be seen that some fields, which relate to the well-known techniques, are not

Table 2.1: Summary of references surveyed in this chapter, for single-sided supply topologies.

<table>
<tr><th colspan="4">Emphasis is on modulation technique</th></tr>
<tr><th colspan="2"></th><th>Single-phase*/Three-phase</th><th>Single-phase*/Multiphase</th></tr>
<tr><td rowspan="2">CBPWM</td><td>Two-level</td><td colspan="2">Not surveyed here (mature technology)</td></tr>
<tr><td>Multilevel</td><td>Carrara et al. (1992)*
Calais et al. (2001)*
Holmes and Lipo (2003)*
Wu (2006)
McGrath and Holmes (2002)</td><td>Mwinyiwiwa et al. (2006)
Nho and Lee (2007)
Busquets-Monge and Ruderman (2010)</td></tr>
<tr><td rowspan="2">SVPWM</td><td>Two-level</td><td>Not surveyed here
(mature technology)</td><td>Zhao and Lipo (1995)
Gopakumar et al. (1993)
Dujić et al. (2006)
de Silva et al. (2004)
Iqbal and Levi (2005)
Iqbal and Levi (2006)
Grandi et al. (2006a)
Kelly et al. (2003)
Grandi et al. (2007)
Dujić (2008)
Dujić et al. (2009)</td></tr>
<tr><td>Multilevel</td><td>Celanovic and Boroyevich (2001)
Castro et al. (2010)
Prats et al. (2003)
Franquelo et al. (2006)
Gupta and Khambadkone (2006)
Holmes and Lipo (2003)
Massoud et al. (2008)
Kanchan et al. (2005)</td><td>Lu and Corzine (2005)
Song et al. (2006)
Huang and Corzine (2008)
Hutson et al. (2008)
Gao and Fletcher (2010)
López et al. (2008b)
López et al. (2008a)
López et al. (2009a)
Leon et al. (2007)*
Leon et al. (2008b)*
Leon et al. (2009a)*
Leon et al. (2008a)*
Leon et al. (2009b)*
Leon et al. (2010b)
Leon et al. (2010a)
Leon et al. (2011)*</td></tr>
</table>

Table 2.2: Summary of references surveyed in this chapter, for single-sided supply topologies.

Emphasis is on comparison of carrier-based and space vector PWM			
		Three-phase	Multiphase
CB vs. SV	Two-level	Holmes (1992)	Dujić (2008)
	Multilevel	Wang (2002) McGrath et al. (2003) Holmes and Lipo (2003) Yao et al. (2008) Pereira and Martins (2009a) Pereira and Martins (2009b)	No references available

considered here. However, those relevant for the thesis topic, multilevel multiphase space vector modulation, are filled in. Carrier-based techniques for multilevel inverters are also analysed, due to the potential simplicity that they can provide for implementation of space vector modulation techniques. The empty field in Table 2.2 suggests one of the additional aims of this work, comparison of carrier-based and space vector modulation techniques for multilevel multiphase case.

Chapter 3

BASIC CONCEPTS

3.1 INTRODUCTION

This chapter introduces the basic sets of equations and transformations that are necessary for the analysis of SVPWM techniques for multilevel multiphase VSIs in subsequent chapters. In the beginning, a multilevel multiphase VSI is analysed for a general case, independently of the actual topology. General system of notation is thus established in this chapter. Starting from the general n-phase l-level VSI case, space vectors are defined and mathematical principle for the determination of times of vector application is given.

The chapter is organised as follows. In section 3.2, the analysed configuration is presented schematically for a general case. Further, appropriate rules according to the type of the signal and adopted notation are introduced. Signals of interest are analysed one by one. Their definition, mathematical representation, nature, and number of possible levels for digitalised signals are given. All equations are also given in matrix form. Further, transformation matrices are given in section 3.3 and, finally, in section 3.4, space vectors are defined. In relation to space vectors, a quick way for plotting, examples for a few typical space vector projection plots, and application time calculation in the general case, are included. After that main circuit structures are introduced to allow linking of the previously given general equations to a specific topology.

3.2 BASIC DEFINITIONS

The aim of this section is to define general configuration of the system that will be analysed in this research, to define all voltages and currents of interest, to explain their nature, and to set the rules for the notation used further on in this thesis.

A typical configuration of a star-connected symmetrical load that is supplied from an n-phase l-level

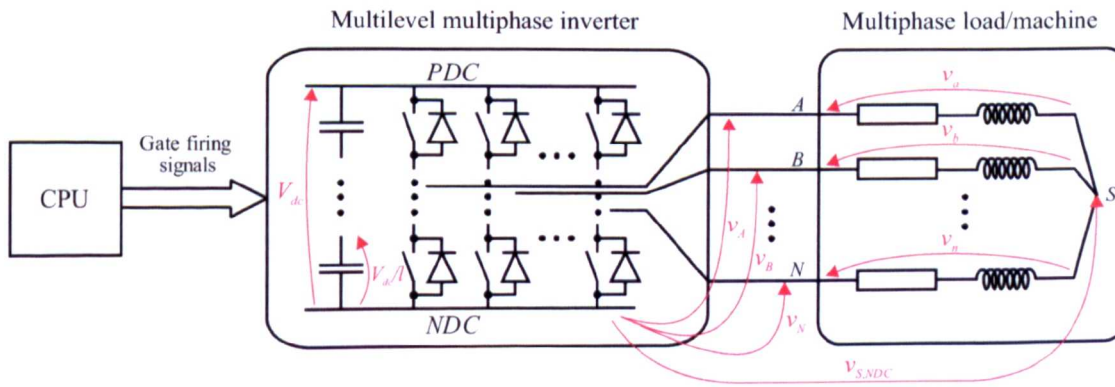


Fig. 3.1: General topology of a multilevel inverter supplying a multiphase load/machine.

inverter is shown in Fig. 3.1. Central processing unit (CPU) is a digital board with micro-processor or digital signal processor (DSP). Input parameters for the CPU are configurable by a user and they are defined by the control algorithm for the load/machine. Inside the CPU, process of modulation takes place. CPU-produced output signals are gate firing signals for the inverter. Inverter represents a power amplifier, and its outputs are high-power leg voltages. Connected load is symmetrical (the same in each phase) and in this research it will be a static n-phase R–L load or a multiphase induction machine. It is assumed that the load is star-connected and that it has only n accessible terminals (as it is shown in Fig. 3.1).

Legs of the inverter will be denoted with capital letters A, B, C, ..., N, so corresponding leg voltages are: v_A, v_B, v_C, ..., v_N. However, in a general case leg voltage of an arbitrary leg will be denoted as v_{LEG}. Phases of the load/machine will be denoted with lower-case letters a, b, c, ..., n, in the same order as the inverter legs, so that the corresponding phase voltages are: v_a, v_b, v_c, ..., v_n. Phase voltage of an arbitrary phase will be denoted as v_{ph}. It is assumed that there are no unconnected legs or phases, so that the numerical value of n is always equal to N.

Different voltages are of a different nature. The shapes of voltages of interest are shown in Fig. 3.2. This figure also contains adopted notation. Rules regarding notation are as follows:

- Continuous values in time are followed by (t), e.g. $v(t)$.
- Discretised – sampled values in time are followed by (kT_s) or $[k]$, e.g. $v(kT_s)=v[k]$, and the value is constant during the sampling period T_s.
- Digitalised, i.e. discretised and quantised values are followed by $[t]$, e.g. $v[t]$, and the value takes a couple of different quantisation levels inside a sampling period T_s. PWM signals are digitalised signals.
- Normalised voltages will be denoted with letter u, rather than v. Process of normalisation is done in such a way that per-unit value of l–1 corresponds to V_{dc} (except in the Chapter 7 where value of u=1 corresponds to $v=V_{dc}$).
- Voltage shifted to the lowest carrier zone (common carrier band) will be denoted with symbol ˜ above it, and will be introduced later in section 5.2.

As an example, a leg voltage undergoes a process of discretisation and digitalisation, and difference between the desired leg voltage, $v^*_{LEG}(t)$, sampled desired leg voltage, $v^*_{LEG}(kT_s)$ and output leg voltage, $v_{LEG}[t]$, can be observed in Fig. 3.2. In what follows, all signals and certain notions correlated with them will be explained in detail. For digitalised signals the number of possible levels will be calculated.

Leg voltages, $v_{LEG}[t]$, are digital signals (Fig. 3.2). In this research they are referenced to the negative dc-bus rail (*NDC*), as are all the other power circuit voltages inside an inverter. Depending on the number of levels, l, of the inverter output, leg voltages can take any discrete value from 0 to V_{dc} (voltage of the positive dc-bus rail *PDC*), with steps of $V_{dc}/(l-1)$. The case when leg voltage step is not constant is beyond the scope of this research. A typical shape of the multilevel inverter output leg voltage is shown in Fig. 3.2 for l=4. Since it is a digitalised PWM signal it is denoted as $v_{LEG}[t]$ in accordance with the given explanations.

Let us now define normalised representation of leg voltages, $u_{LEG}[t]$, obtained by dividing output leg voltage with the step of the inverter $V_{dc}/(l-1)$:

$$u_{LEG}[t] = v_{LEG}[t] \cdot \frac{l-1}{V_{dc}} \tag{3.1}$$

Defined normalised value of the leg voltage can take any integer value from 0 to l–1 (the normalised step is one).

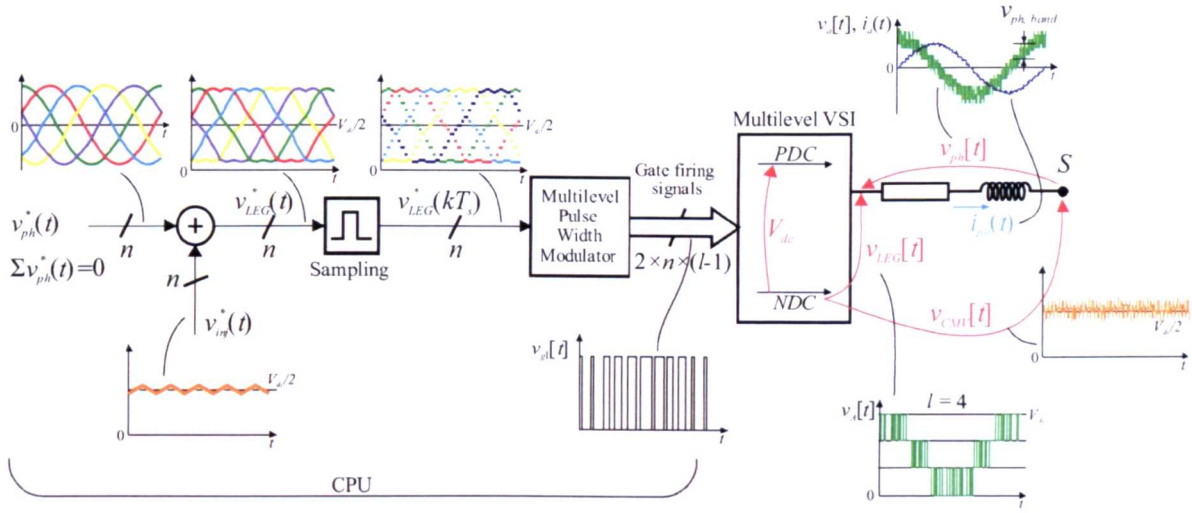


Fig. 3.2: Signals of interest with adopted notation and sketched waveforms in the system of Fig. 3.1. It is assumed that n=5 and l=4.

Set of instantaneous values of all normalised leg voltages represents the *switching state* of an inverter and is usually given in digital form, e.g. $[u_A\ u_B\ u_C\ u_D\ u_E]$=[2 0 1 3 1]. Number of switching states is the number of different combinations of leg voltage outputs. As there are n legs and any of them can take any of l different voltage values, the number of different switching states is defined with:

$$\text{Number of switching states} = l^n \tag{3.2}$$

It is not mandatory that modulation process takes all possible switching states into consideration.

Leg-to-leg (or line-to-line) voltage represents voltage between two inverter outputs and is given with:

$$v_{L\text{-}L}[t] = v_{LEG\,1}[t] - v_{LEG\,2}[t] \tag{3.3}$$

where $LEG1$ and $LEG2$ can take any value from A to N, and $LEG1 \neq LEG2$. Number of levels of the line-to-line voltages depends on the values of the leg voltages. Since it is assumed that step of leg voltages is constant and equal to $V_{dc}/(l\text{–}1)$, i.e. 1 in normalised form, that means that line-to-line voltage will have the same step, since it is obtained by subtraction. The theoretical minimum and maximum values of digitalised $u_{L\text{-}L}[t]$ that is defined in the same way as in (3.3), are $\pm(l\text{–}1)$. These values are obtained when one leg has the minimum and the other one has the maximum value. Finally, leg-to-leg voltage can take any integer value (step is 1) in between minimum, $-(l\text{–}1)$ and maximum, $+(l\text{–}1)$ value, so theoretical maximum number of levels that can appear in a leg-to-leg voltage is $2\cdot(l\text{–}1)+1$.

Phase voltages represent voltage across a phase of the load, which, in star-connected load case, is the difference between inverter output and the potential of the neutral (star) point of the load, S. According to Fig. 3.1, the following equations can be written:

$$\begin{aligned} v_A &= v_{S\,NDC} + v_a \\ v_B &= v_{S\,NDC} + v_b \\ &\vdots \\ v_N &= v_{S\,NDC} + v_n \end{aligned} \tag{3.4}$$

Since the nature of v_{ph} and $v_{S\,NDC}$ has not been explained yet, the dependence on time is omitted in (3.4). Summing equations in (3.4) and expressing voltage between the star point of the load/motor and the negative inverter dc-bus, $v_{S\,NDC}$, that actually represents *common mode voltage* (CMV), one gets:

$$v_{CMV} = v_{S\,NDC} = \frac{1}{n}\left(\sum_{LEG=A}^{N} v_{LEG} - \sum_{ph=a}^{n} v_{ph}\right) \tag{3.5}$$

where the sum of phase voltages is equal to zero, when the load is symmetrical, as it is assumed here. Thus, one gets from (3.5):

$$v_{CMV}[t] = v_{S\,NDC}[t] = \frac{1}{n}\sum_{LEG=A}^{N} v_{LEG}[t] \tag{3.6}$$

Since CMV depends only on leg voltages (for symmetrical load), it is also of the digitalised nature, as it is indicated in (3.6). Typical shape of the CMV is given in Fig. 3.2.

Substituting (3.6) into (3.4) one gets the phase voltages in the following form:

$$v_{ph}[t] = v_{LEG}[t] - \frac{\sum v_{LEG}[t]}{n} \tag{3.7}$$

or using normalised values for leg voltages:

$$v_{ph}[t] = \left(u_{LEG}[t] - \frac{\sum u_{LEG}[t]}{n}\right)\frac{V_{dc}}{l-1} \tag{3.8}$$

According to the introduced notation in the general form, it should be clear that *ph* and *LEG* in the index correspond to each other, i.e. that $ph = a$ to n corresponds to $LEG = A$ to N. Also, boundaries of the sum in (3.7) and (3.8) are from A to N. From (3.7) and (3.8) it is clear that phase voltages are also of the digitalised nature. Characteristic shape of a phase voltage is given in Fig. 3.2.

Let us also define normalised values for phase voltages $u_{ph}[t]$ as:

$$u_{ph}[t] = v_{ph}[t] \cdot \frac{l-1}{V_{dc}} \tag{3.9}$$

From (3.8) and (3.9) u_{ph} can be expressed in terms of u_{LEG}, as:

$$u_{ph}[t] = u_{LEG}[t] - \frac{\sum u_{LEG}[t]}{n} \tag{3.10}$$

where $ph = a$ to n corresponds to $LEG = A$ to N, and boundaries of the sum are from A to N.

Previous equations (3.8) and (3.10) can be rewritten in matrix form. Equation (3.8) becomes:

$$\begin{bmatrix} v_a \\ v_b \\ \vdots \\ v_n \end{bmatrix} = \left(\begin{bmatrix} u_A \\ u_B \\ \vdots \\ u_N \end{bmatrix} - \frac{\sum u_{LEG}}{n} \cdot \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}\right) \cdot \frac{V_{dc}}{l-1} = \left(\begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & & 0 \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix} - \frac{1}{n}\begin{bmatrix} 1 & 1 & \cdots & 1 \\ 1 & 1 & & 1 \\ \vdots & & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \end{bmatrix}\right) \cdot \begin{bmatrix} u_A \\ u_B \\ \vdots \\ u_N \end{bmatrix} \cdot \frac{V_{dc}}{l-1} \tag{3.11}$$

Brackets with time-related term, which defines the signal nature, are omitted in matrix form. Taking into account normalisation from (3.9), one gets:

$$\begin{bmatrix} u_a \\ u_b \\ \vdots \\ u_n \end{bmatrix} = \begin{bmatrix} u_A \\ u_B \\ \vdots \\ u_N \end{bmatrix} - \frac{\sum u_{LEG}}{n} \cdot \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} = \left(\begin{bmatrix} 1 & 0 & \cdots & 0 \\ 0 & 1 & & 0 \\ \vdots & & \ddots & \vdots \\ 0 & 0 & \cdots & 1 \end{bmatrix} - \frac{1}{n} \begin{bmatrix} 1 & 1 & \cdots & 1 \\ 1 & 1 & & 1 \\ \vdots & & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \end{bmatrix} \right) \cdot \begin{bmatrix} u_A \\ u_B \\ \vdots \\ u_N \end{bmatrix} \tag{3.12}$$

that represents equation (3.10) in matrix form.

Considerations regarding the number of levels and the notion of 'band' of phase voltage are given next. To get some general results, either standard form (3.8) or normalised form (3.10) of phase voltage can be considered. Again, as it has already been mentioned in conjunction with line-to-line voltages, the number of levels of the phase voltage can also only be determined in terms of the maximum possible number.

In (3.8) the theoretical maximum difference in brackets results when normalised value of one leg voltage is maximum, i.e. equal to (l–1), and its sum with normalised values of the other leg voltages is minimum, l-1+(n–1)·0 (all other legs are 0). Similarly, the part in brackets has theoretical minimum when one of leg voltages has the minimum value, 0, and the sum of it with the other leg voltages is maximum, 0+(n–1)·(l–1) (all other legs have maximum value, l–1). Using these values in (3.8) one gets that theoretical minimum and maximum value of a phase voltage are defined as:

$$v_{ph\,\max/\min}^{\text{theoretical}} = \pm \frac{n-1}{n} V_{dc} \tag{3.13}$$

The step for the values of the phase voltages is constant, since the step of leg voltages is constant as well, and is defined with the minimum non-zero value of the sum in the brackets in (3.8):

$$v_{ph\,\text{step}} = \frac{1}{n} \cdot \frac{V_{dc}}{l-1} \tag{3.14}$$

By dividing theoretical maximum/minimum value with the step, one gets the number of positive/negative levels of the phase voltages. Adding the always present additional zero level (e.g. when all leg voltages are equal) one gets that theoretical maximum number of levels of phase voltages is:

$$v_{ph\,\text{Number of Levels}}^{\text{theoretical maximum}} = 2 \cdot (n-1) \cdot (l-1) + 1 \tag{3.15}$$

The actual number of levels depends on the value of the reference phase voltage and also on the type of the modulation strategy used.

Note that the obtained CMV has the same voltage step as a phase voltage, as defined by (3.14). The maximum and minimum values are determined when all legs have maximum i.e. minimum value. Using the definition of CMV (3.6), one gets that these values are V_{dc} and 0, i.e. in normalised form l–1 and 0. This means that theoretical maximum number of levels in the CMV is n·(l–1)+1, and, again, depending on the modulation strategy all of them may or may not be present.

'Band' of the phase voltage is shown in Fig. 3.2 and it can be defined as variation around the average value during one switching period T_s. In equation (3.10) $u_{LEG}[t]$ represents digital PWM signals whose average value is equal to $u_{LEG}^{*}(kT_s)$ during T_s, as it is shown in Fig. 3.3a. $u_{LEG}[t]$ can be represented as a sum of a constant and an alternating part, during the switching period T_s (Fig. 3.3a):

$$u_{LEG}[t] = u_{LEG,const}(kT_s) + u_{LEG,alt}[t] \tag{3.16}$$

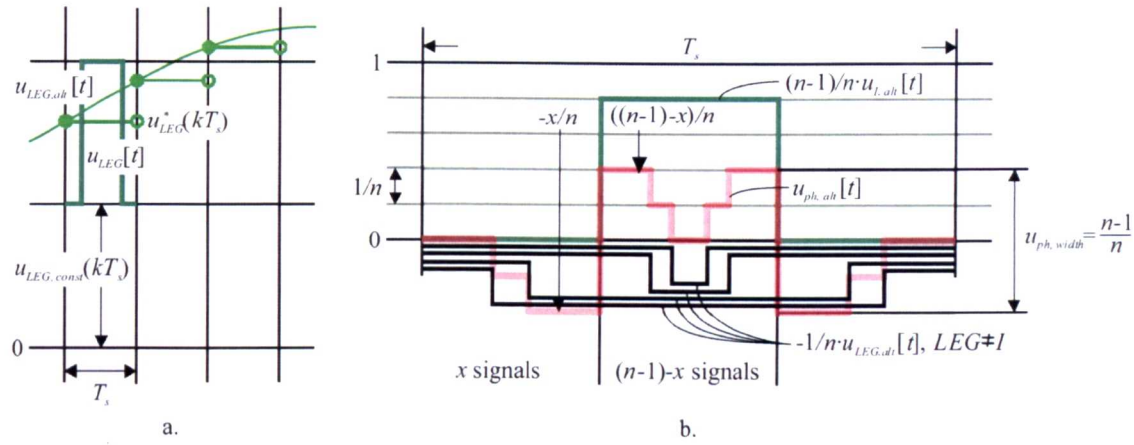


Fig. 3.3: Calculation of the 'band' of the phase voltage in the general case: a. Constant and alternating part of the PWM produced leg voltage. b. Graphical explanation of the sum in (3.18) for PD-PWM.

The constant part is in essence any integer value in the range 0 to l–2, while the alternating part is the PWM signal in the range 0 to 1. Note that it is not necessary that alternating part contains only two levels and also levels do not have to be the nearest ones, but in this way dv/dt and the number of switchings and hence losses of the inverter are minimised.

Substituting (3.16) into (3.10) one gets:

$$u_{ph}[t] = u_{LEG,const}(kTs) - \frac{\sum u_{LEG,const}(kTs)}{n} + u_{LEG,alt}[t] - \frac{\sum u_{LEG,alt}[t]}{n} \tag{3.17}$$

At this point it becomes important which type of modulation is used. It is assumed here that one 'up' and one 'down' transition, for one level, take place in all legs during the switching period, and that 'up' transition is in the first, while 'down' transition is in the second half of T_s. This represents the most common assumption for space vector algorithms; if CBPWM is used, this corresponds to in-phase carrier disposition (PD-PWM), as discussed in sub-section 5.2.1.

For the calculation of the 'band' of the phase voltage during T_s, only the alternating part of equation (3.17) is of interest, since the other part is constant during the whole period T_s. Let us consider the i^{th} phase. Taking leg voltage $u_{l,alt}[t]$ out from the sum, phase i alternating part can be expressed as:

$$u_{i,alt}[t] = \frac{n-1}{n} \cdot u_{l,alt}[t] - \sum_{LEG=1, LEG \neq l}^{N} \frac{u_{LEG,alt}[t]}{n} \tag{3.18}$$

Let us assume also that there are x leg voltages that have greater average value of the alternating part than the l^{th} leg voltage. This case is shown in Fig. 3.3b. Sum of (3.18) is graphically explained in Fig. 3.3b and from this figure it is clear that the minimum value of $u_{i,alt}[t]$ is $-x/n$, while the maximum is $((n-1)-x)/n$. This finally means that the 'band' of the phase voltage inside a switching period T_s is:

$$u_{ph\,\mathrm{band}} = \frac{n-1}{n} \tag{3.19}$$

or in non-normalised form:

$$v_{ph\,\mathrm{band}} = \frac{n-1}{n} \cdot \frac{V_{dc}}{l-1} = (n-1) \cdot v_{ph\,\mathrm{step}} \tag{3.20}$$

Previously explained signals are real measurable signals available in practice. All of these signals have their reference in the model inside the CPU. Reference values are continuous, but they are used only at instants governed by the sampling frequency. Also, note that desired reference voltages are always phase voltages, $v_{ph}^{*}(t)$. This does not entirely specify the modulation process since desired and output leg voltages ($v_{LEG}^{*}(t)$ and $v_{LEG}[t]$) contain CMV which represents a degree of freedom. It can be seen from (3.4) that leg and phase voltages are linked through the common mode voltage ($v_{SNDC}=v_{CMV}$). So, CMV is also a parameter that should be always of the high interest. CMV inside the processor unit is a continuous value and is denoted as injection, $v_{inj}^{*}(t)$. If regular symmetrical sampling is applied (samples are taken at the beginning of the sampling period), that means that sampled values of the continuous (desired) signals are equal to the average values of the corresponding digitalised signals in the same switching period. Also one should be aware that values in CPU in Fig. 3.2 are shown in their natural range that is desirable in the inverter and in the machine, but in practice all these values are scaled to CPU digital range and are in essence binary values.

One very important parameter that is defined according to the continuous reference values is a modulation index. It represents ratio of the magnitude of the fundamental desired phase voltage over the $V_{dc}/2$. Since desired phase voltage, for the machine with sinusoidally distributed windings, is pure sinusoidal signal, this definition can be simplified as:

$$m=\frac{V^{*}}{V_{dc}/2} \tag{3.21}$$

where V^{*} represents the amplitude of the sinusoidal reference signal.

3.3 TRANSFORMATIONS

In this sub-section commonly used transformations in multiphase system analysis are defined, described and rewritten in the form commonly used in the area of electrical machines. In the field of electrical machines the most wide-spread transformation is Clarke's transformation. It is a real transformation and is a specific case of the complex, Fortescue's transformation [White and Woodson (1959)]. Another transformation is the one that defines space vectors, and it is usually called space vector transformation. All of these transformations came from different science fields but in essence all of them are specific cases of the general discrete Fourier's transformation (DFT). An effort has been put in [Grandi et al. (2006a)] to explain differences and similarities between these transformations.

Let us consider space vector transformation in the case of an n-phase time-dependent system. Assume that x_k are real quantities related to that system (k = 1 to n). The general symmetrical space vector transformation can be defined as [Grandi et al. (2006a)]:

$$\underline{x}_{s,pl}=\frac{1}{n}\cdot\sum_{k=1}^{n}x_k\cdot e^{j\frac{2\pi}{n}(k-1)\cdot pl} \qquad pl=0,1,2,\ldots,n-1 \tag{3.22}$$

Value of pl is unlimited, but transformation is periodical, so in this way (taking pl = 0 to n–1) one period is selected. Quantities denoted as $\underline{x}_{s,pl}$ are complex values. The exceptions are the zero-sequence component $x_{s,0}$, and $x_{s,n/2}$ that is present if n is an even number, which are real quantities. Index s stands to highlight that the transformation in this form is symmetrical.

Variables $\underline{x}_{s,pl}$ are n different complex values for different value of pl. If matrix form is used, $[\underline{x}_s]=[x_{s,0}, \underline{x}_{s,1}, \underline{x}_{s,2}, \ldots, \underline{x}_{s,n-1}]^T$, it can be interpreted as an n-dimensional *space vector*, while $\underline{x}_{s,pl}$ can be interpreted as projections of that vector to a certain complex 2-D plane, pl.

The inverse transformation given by [Grandi et al. (2006a)] is:

$$x_k = \sum_{pl=0}^{n-1} \underline{x}_{s,pl} \cdot e^{-j\frac{2\pi}{n}(k-1)\cdot pl} \qquad k = 1, 2, 3, \ldots, n \tag{3.23}$$

Transformation pair, given by (3.22) and (3.23), is of the same form as Fortescue's transformation [Fortescue (1918)] and DFT transformation [Oppenheim and Schafer (2009)]. Interpretation of variable pl is different in electrical machine analysis, where it is interpreted as a complex plane (so it is denoted with pl) and in digital signal processing, for example, where it, when multiplied with $2\pi/n$, represents digital frequency [Oppenheim and Schafer (2009)].

It can be seen that the only difference between direct (3.22) and inverse (3.23) transformation is in the exponent sign, and in the scaling coefficient. The only requirements are that direct and inverse transformations have opposite-sign exponents and that the product of their normalisation factors is $1/n$ [Grandi et al. (2006a)]. Chosen normalisation will lead to power-variant form of the transformation (signal magnitudes before and after transformation are the same, but the total system power is not) that is more suitable for analysis of SVPWM techniques.

Transformation pair can be rewritten in the matrix form. If system variables x_k, and transformed values $\underline{x}_{s,pl}$ are represented as column matrices $[x]=[x_1, x_2, x_3,\ldots, x_n]^T$ and $[\underline{x}_s]=[x_{s,0}, \underline{x}_{s,1}, \underline{x}_{s,2},\ldots, \underline{x}_{s,n-1}]^T$, then (3.22) and (3.23) become:

$$\begin{aligned} [\underline{x}_s] &= [\underline{F}_{s,n}]\cdot[x] \\ [x] &= [\underline{F}_{s,n}]^{-1}\cdot[\underline{x}_s] \end{aligned} \tag{3.24}$$

where $[\underline{F}_{s,n}]$ represents full transformation that is given with:

$$[\underline{F}_{s,n}] = \frac{1}{n}\cdot\begin{bmatrix} \underline{a}^{0\cdot 0} & \underline{a}^{1\cdot 0} & \underline{a}^{2\cdot 0} & \cdots & \underline{a}^{(n-1)\cdot 0} \\ \underline{a}^{0\cdot 1} & \underline{a}^{1\cdot 1} & \underline{a}^{2\cdot 1} & \cdots & \underline{a}^{(n-1)\cdot 1} \\ \underline{a}^{0\cdot 2} & \underline{a}^{1\cdot 2} & \underline{a}^{2\cdot 3} & \cdots & \underline{a}^{(n-1)\cdot 2} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ \underline{a}^{0\cdot(n-1)} & \underline{a}^{1\cdot(n-1)} & \underline{a}^{2\cdot(n-1)} & \cdots & \underline{a}^{(n-1)\cdot(n-1)} \end{bmatrix} = \frac{1}{n}\cdot\begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \\ 1 & \underline{a}^{1} & \underline{a}^{2} & \cdots & \underline{a}^{n-1} \\ 1 & \underline{a}^{2} & \underline{a}^{4} & \cdots & \underline{a}^{2n-2} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & \underline{a}^{n-1} & \underline{a}^{2n-2} & \cdots & \underline{a}^{n^2+2n+1} \end{bmatrix} \tag{3.25}$$

where $\underline{a}=e^{j\cdot 2\pi/n}$. According to the definition of the transformation pair (3.22) and (3.23), inverse transformation in matrix form can be obtained as:

$$[\underline{F}_{s,n}]^{-1} = n\cdot[\underline{F}_{s,n}]^{T^*} \tag{3.26}$$

Since $\underline{a}^n$ is equal to 1, all factors with n can be removed from exponent in (3.25), which becomes:

$$[\underline{F}_{s,n}] = \frac{1}{n}\cdot\begin{bmatrix} 1 & 1 & 1 & \cdots & 1 \\ 1 & \underline{a}^{1} & \underline{a}^{2} & \cdots & \underline{a}^{-1} \\ 1 & \underline{a}^{2} & \underline{a}^{4} & \cdots & \underline{a}^{-2} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & \underline{a}^{-1} & \underline{a}^{-2} & \cdots & \underline{a}^{1} \end{bmatrix} \qquad \underline{a}=e^{j\cdot 2\pi/n} \tag{3.27}$$

From (3.27) it is clear that transformation matrix $[\underline{F}_{s,n}]$ is symmetrical, and index s is used again to highlight that. Also, it can be seen that the last row in (3.27) is the same as the 2nd row, but with the opposite signs in exponents. Thus, if x_k are real numbers (as it is in practice, since $[x]$ is a set of voltages, currents, ...), that finally means that for transformed quantities one has:

$$\underline{x}_{s,pl} = \underline{x}^{*}_{s,n-pl} = \underline{x}^{*}_{s,-pl} \qquad pl = 0, 1, 2, \ldots, n-1 \tag{3.28}$$

In other words, values $\underline{x}_{s,pl}$ and $\underline{x}_{s,n-pl}$ are the same values with the opposite phase sign. Equation (3.28) shows that space vector $[\underline{x}_s]$ can be fully described just with half of its elements, plus unique zero component (or components for even n). The equivalence in the digital signal processing field is the transformation of a two-sided to one-sided real signal spectrum. This principle of halving is also one of the basic principles for the fast Fourier algorithms [Oppenheim and Schafer (2009)].

Since only half of the transformation will be used (half of complex values plus one for odd n, or two for even n, real values), to retain the same magnitude of variables, normalisation factor in (3.22) and (3.25) must be changed, i.e. multiplied by 2. In this way unique real values will be also doubled, so they have to be divided once again by 2, to retain correct magnitude. Thus, for an n-phase system, space vector projections to a certain complex plane pl are defined with:

$$\begin{aligned} x_0 &= \frac{2}{n}\cdot\sum_{k=1}^{n}\frac{x_k}{2}, \qquad \left(x_{n/2} = \frac{2}{n}\cdot\sum_{k=1}^{n}\frac{x_k}{2}\cdot(-1)^{k-1} \ \text{present for even} \ n\right) \\ \underline{x}_{pl} &= \frac{2}{n}\cdot\sum_{k=1}^{n} x_k \cdot e^{j\frac{2\pi}{n}(k-1)\cdot pl} \qquad pl = 1 \text{ to } (n-1)/2, \text{ for odd } n, \text{ i.e. } (n-2)/2 \text{ for even } n \end{aligned} \tag{3.29}$$

or, in matrix form, plane by plane projections can be expressed as:

$$\underline{x}_{pl} = A\cdot\frac{2}{n}\cdot\begin{bmatrix}1 & e^{j\cdot pl\cdot\alpha} & \cdots & e^{j\cdot pl\cdot(n-1)\alpha}\end{bmatrix}\cdot\begin{bmatrix}x_1\\x_2\\\vdots\\x_n\end{bmatrix} = [\underline{F}_{n,pl}]\cdot[x] \tag{3.30}$$

where $pl = 0$ to $n/2-1$, for odd n, i.e. 0 to $n/2$, for even n. Constant $A=1/2$ for $pl = 0$ or $n/2$, otherwise $A=1$. Note that index s, that was standing for symmetrical transformed values $\underline{x}_{s,pl}$, and for symmetrical form of transformation $[\underline{F}_{s,n}]$, is now omitted. From this point onwards, this, asymmetrical, form of space vector transformation will be used. Notation of the planes will be also changed, to the traditional method of notation in the area of electrical machines. Axis 0 will be denoted as 0, or as 0^+ if n is even number when axis $n/2$ will be denoted as 0^-. Plane $pl=1$ will be traditionally denoted as α-β plane, while planes $pl=2, 3, \ldots$ will be denoted as x_1-y_1, x_2-y_2, ..., x_r-y_r. Equation (3.29) can be written in matrix form as:

$$\begin{bmatrix}\underline{x}_{\alpha-\beta}\\\underline{x}_{x_1-y_1}\\\vdots\\\underline{x}_{x_r-y_r}\\x_{0^+}\\x_{0^-}\end{bmatrix} = \frac{2}{n}\begin{bmatrix}1 & e^{j\alpha} & e^{j2\alpha} & \cdots & e^{j(n-1)\alpha}\\1 & e^{j2\alpha} & e^{j4\alpha} & \cdots & e^{j2(n-1)\alpha}\\\vdots & \vdots & \vdots & \ddots & \vdots\\1 & e^{jr\alpha} & e^{jr2\alpha} & \cdots & e^{jr(n-1)\alpha}\\1/2 & 1/2 & 1/2 & \cdots & 1/2\\1/2 & -1/2 & 1/2 & \cdots & -1/2\end{bmatrix}\cdot\begin{bmatrix}x_1\\x_2\\x_3\\\vdots\\x_n\end{bmatrix} = [\underline{F}_n]\cdot[x] \tag{3.31}$$

where $\alpha=2\cdot\pi/n$ and, for $n\geq 5$, $r=(n-1)/2-1$ for odd n and $(n-2)/2-1$ for even n. Unique transformation rows 0^+ and 0^- are now moved to their traditional positions at the bottom of the matrix. The last row 0^- exists only for even n.

Dot product of any two rows in the transformation matrix (3.31) is zero, so complex planes *pl* are mutually orthogonal, i.e. decoupled, in multidimensional space. By decomposing complex 2-D space vector projections into real and imaginary part as $\underline{x}_{pl}=x_{x,pl}+j\cdot x_{y,pl}$, (that are also orthogonal to each other) transformation matrix can be expressed in the form with all real terms, as:

$$[C_n]=\frac{2}{n}\cdot\begin{bmatrix} 1 & \cos(\alpha) & \cos(2\alpha) & \cdots & \cos((n-1)\alpha) \\ 0 & \sin(\alpha) & \sin(2\alpha) & \cdots & \sin((n-1)\alpha) \\ 1 & \cos(2\alpha) & \cos(4\alpha) & \cdots & \cos(2(n-1)\alpha) \\ 0 & \sin(2\alpha) & \sin(4\alpha) & \cdots & \sin(2(n-1)\alpha) \\ 1 & \cos(3\alpha) & \cos(6\alpha) & \cdots & \cos(3(n-1)\alpha) \\ 0 & \sin(3\alpha) & \sin(6\alpha) & \cdots & \sin(3(n-1)\alpha) \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & \cos(r\alpha) & \cos(r\cdot 2\alpha) & \cdots & \cos(r\cdot(n-1)\alpha) \\ 0 & \sin(r\alpha) & \sin(r\cdot 2\alpha) & \cdots & \sin(r\cdot(n-1)\alpha) \\ 1/2 & 1/2 & 1/2 & \cdots & 1/2 \\ 1/2 & -1/2 & 1/2 & \cdots & -1/2 \end{bmatrix}\begin{matrix} \alpha \\ \beta \\ x_1 \\ y_1 \\ x_2 \\ y_2 \\ \vdots \\ x_r \\ y_r \\ 0^+ \\ 0^- \end{matrix} \tag{3.32}$$

This is so-called real decoupling transformation form or an *n*-dimensional Clarke's transformation [White and Woodson (1959)]. Space vector column matrix produced using this transformation contains projections of the *n*-dimensional space vector onto mutually orthogonal axes (real values).

3.4 SPACE VECTORS

A space vector can be defined in general as any set of *n* system variables (original variables or variables after any transformation). In this research, space vectors are further defined by transformation matrices (3.30) to (3.32), that transform an *n*-dimensional system into a new set of variables, without the change of the system dimension. Column matrix of multiphase system variables, when multiplied by transformation matrix, produces a new column matrix that one calls space vector of the considered variables. This means that presented space vector definition is general and can be used for example for the set of leg voltages, $[v_A[t]\ v_B[t]\ \ldots\ v_M[t]]^T$, desired leg voltages, $[v_A^*(t)\ v_B^*(t)\ \ldots\ v_M^*(t)]^T$, phase voltages, $[v_a[t]\ v_b[t]\ \ldots\ v_n[t]]^T$, desired phase voltages, $[v_a^*(t)\ v_b^*(t)\ \ldots\ v_n^*(t)]^T$, and so on. Space vectors can be also defined for sets of currents or any other physical variables of the multiphase system. The difference between transformation matrices (3.31) and (3.32) is that (3.31) is in complex form, so that the space vector is represented as a complex number that describes projections on the real and imaginary axes of the mutually orthogonal planes. On the other hand, vector produced using real transformation (3.32), is a column matrix with real numbers that represent space vector projections to each of the *n* mutually orthogonal axes.

For example, space vector of the leg voltage set, using (3.31), is defined as:

$$[\underline{v}_{LEG}] = [\underline{F}_n] \cdot [v_{LEG}]$$

$$\begin{bmatrix} \underline{v}_{LEG,\alpha-\beta} \\ \underline{v}_{LEG,x_1-y_1} \\ \vdots \\ \underline{v}_{LEG,x_r-y_r} \\ v_{LEG,0^+} \\ v_{LEG,0^-} \end{bmatrix} = \frac{2}{n} \begin{bmatrix} 1 & e^{j\alpha} & e^{j2\alpha} & \cdots & e^{j(n-1)\alpha} \\ 1 & e^{j2\alpha} & e^{j4\alpha} & \cdots & e^{j2(n-1)\alpha} \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & e^{jr\alpha} & e^{jr2\alpha} & \cdots & e^{jr(n-1)\alpha} \\ 1/2 & 1/2 & 1/2 & \cdots & 1/2 \\ 1/2 & -1/2 & 1/2 & \cdots & -1/2 \end{bmatrix} \cdot \begin{bmatrix} v_A \\ v_B \\ v_C \\ \vdots \\ v_N \end{bmatrix} \tag{3.33}$$

where $\alpha=2\cdot\pi/n$. The last row that defines 0^- projection is present only for even n.

The nature of space vectors is determined by the nature of the considered signals. For example, obtained leg voltages or phase voltages take digital values (step is different, see (3.1) and (3.14)), so produced space vectors are also digital vectors, i.e. points, in the n-dimensional space. On the other hand, reference leg and reference phase voltages are of the continuous nature, so their space vectors (and all of space vector projections) are of the continuous nature. In accordance with this, time dependence $[t]$ for digital signal nature is omitted in matrix form in (3.33).

Let us now compare space vectors of leg and phase voltages. According to (3.30) space vector of the phase voltages is defined, through its projections into plane pl, as:

$$\underline{v}_{ph,pl}[t] = A \cdot \frac{2}{n} \cdot \begin{bmatrix} 1 & e^{j\cdot pl\cdot\alpha} & \cdots & e^{j\cdot pl\cdot(n-1)\alpha} \end{bmatrix} \cdot \begin{bmatrix} v_a \\ v_b \\ \vdots \\ v_n \end{bmatrix} \tag{3.34}$$

Using correlation between phase and leg voltages (3.7), (3.34) becomes:

$$\underline{v}_{ph,pl}[t] = A\frac{2}{n}\begin{bmatrix} 1 & e^{j\cdot pl\cdot\alpha} & \cdots & e^{j\cdot pl\cdot(n-1)\alpha} \end{bmatrix} \cdot \begin{bmatrix} v_A \\ v_B \\ \vdots \\ v_N \end{bmatrix} - A\frac{2}{n}\begin{bmatrix} 1 & e^{j\cdot pl\cdot\alpha} & \cdots & e^{j\cdot pl\cdot(n-1)\alpha} \end{bmatrix} \cdot \frac{\sum v_{LEG}}{n} \begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix} \tag{3.35}$$

The first term in (3.35) corresponds to the definition of the space vector for a set of leg voltages, while the second term can be rewritten as a sum of exponential terms:

$$\underline{v}_{ph,pl}[t] = \underline{v}_{LEG,pl}[t] - A \cdot \frac{2}{n} \cdot \frac{\sum v_{LEG}[t]}{n} \cdot \sum_{k=0}^{n-1} e^{j\cdot\alpha\cdot k\cdot pl} \tag{3.36}$$

The value of the second sum in (3.36) can be simply calculated as a geometrical progression. Using $\alpha=2\cdot\pi/n$ one gets that the value of the sum is equal to zero for all values of $pl\neq int\cdot n$, where *int* represents integer value. For $pl=int\cdot n$, the value of the sum is n. Since value of pl is limited from 0 to $(n-1)/2$ for odd n, i.e. 0 to $n/2$ for even n, that means that space vectors of the leg and phase voltages have only different projection for $pl=0$, i.e. onto 0^+ axis. In this case value of A is 1/2, value of the second sum is n, so the second term in (3.36) becomes of the same form as CMV (3.6). However, the space vector projection of the phase voltages to 0^+ plane is zero, since the value of the first term in (3.36) is also equal to CMV for $pl=0$. In other words, the projection to 0^+ plane represents average value of the signals ($1/n\cdot\Sigma v_{ph}$), which, for phase voltages, is zero. Also, projection of leg voltage space vectors to 0^+ plane is their average value, i.e. the CMV.

The final conclusion is that for a symmetrical star-connected load structure the phase and leg voltage space vector projections are the same for all axes, except for 0^+ axis, where the projection of phase voltage space vector is 0, while projection of the leg voltage space vector is equal to the v_{CMV} value. The same conclusion is valid also for the reference phase and reference leg voltages.

It is also of interest to analyse space vectors of the leg-to-leg voltages. In multiphase systems leg-to-leg voltages can be defined in different ways. For example, in a five-phase case set of leg-to-leg voltages can be defined as: v_A-v_B, v_B-v_C, ..., v_E-v_A, or as v_A-v_C, v_B-v_D, ..., v_E-v_B, etc. Let us introduce the distance between chosen legs and denote it with Λ. In the first set of leg-to-leg voltages in the shown example, the distance is Λ=1, while in the second set, Λ=2. The space vector definition for leg-to-leg voltages is the same as for any other set of voltages. Taking as an example Λ=1, and using (3.30), leg-to-leg space vectors for an n-phase system are:

$$\underline{v}_{L-L,pl} = [\underline{F}_{n,pl}] \cdot \begin{bmatrix} v_A - v_B \\ v_B - v_C \\ \vdots \\ v_N - v_A \end{bmatrix} = [\underline{F}_{n,pl}] \cdot \begin{bmatrix} 1 & -1 & 0 & \cdots & 0 \\ 0 & 1 & -1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ -1 & 0 & 0 & \cdots & 1 \end{bmatrix} \cdot \begin{bmatrix} v_A \\ v_B \\ \vdots \\ v_N \end{bmatrix} \tag{3.37}$$

Equation (3.37) can be further expressed as:

$$\underline{v}_{L-L,pl} = [\underline{F}_{n,pl}] \cdot \begin{bmatrix} v_A \\ v_B \\ \vdots \\ v_N \end{bmatrix} - [\underline{F}_{n,pl}] \cdot \begin{bmatrix} 0 & 1 & 0 & \cdots & 0 \\ 0 & 0 & 1 & \cdots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & 0 & 0 & \cdots & 0 \end{bmatrix} \cdot \begin{bmatrix} v_A \\ v_B \\ \vdots \\ v_N \end{bmatrix} \tag{3.38}$$

Square matrix in the second term in (3.38) can be obtained from the unity matrix after circularly shifting to the right, for Λ positions. Multiplication of the transformation matrix $[\underline{F}_{n,pl}]$ by that matrix will produce circular shifting to the right of the elements in $[\underline{F}_{n,pl}]$ row-matrix. Since the elements of the matrix $[\underline{F}_{n,pl}]$ are of the form $A \cdot 2/n \cdot e^{j \cdot pl \cdot k \cdot \alpha}$ and since $e^{j \cdot pl \cdot n \cdot \alpha}=1$, the circular rotation of elements for Λ positions can be obtained by multiplication of $[\underline{F}_{n,pl}]$ by $e^{-j \cdot pl \cdot \Lambda \cdot \alpha}$. That simplifies (3.38) to:

$$\underline{v}_{L-L,pl} = [\underline{F}_{n,pl}] \cdot \begin{bmatrix} v_A \\ v_B \\ \vdots \\ v_N \end{bmatrix} - e^{-j \cdot pl \cdot \Lambda \cdot \alpha} \cdot [\underline{F}_{n,pl}] \cdot \begin{bmatrix} v_A \\ v_B \\ \vdots \\ v_N \end{bmatrix} = (1 - e^{-j \cdot pl \cdot \Lambda \cdot \alpha}) \cdot \underline{v}_{LEG,pl} \tag{3.39}$$

From equation (3.39) it is clear that position of space vector projections of the leg-to-leg voltages can be easily obtained from positions of projections of the leg voltage space vectors. Term $1-e^{-j \cdot pl \cdot \Lambda \cdot \alpha}$, depending on the value of Λ, changes the magnitude and the phase of the leg voltage space vector projection. Also, one can see that in 0^+ axis, projection of leg-to-leg voltages is always zero (since pl=0). For even numbers of phases n, the 0^- axis is present and projection to this axis depends on Λ. For odd Λ it simply doubles projection of leg voltages, while for even Λ projection of leg-to-leg space vectors to 0^- axis is zero.

3.4.1 PLOTTING AND COUNTING OF SPACE VECTORS

In this sub-section space vector projections for two-level and three-level case for five- and seven-phase inverter leg voltages will be given. Graphical interpretation of space vectors is usually given through the projections of space vectors into certain planes. Thus, the defining equation (3.30) is very convenient for this purpose. By expressing space vectors for leg voltages using normalised form (3.1), one gets:

$$\underline{v}_{LEG,\,pl} = A \cdot \frac{2}{n} \cdot \begin{bmatrix} 1 & e^{j \cdot pl \cdot \alpha} & \dots & e^{j \cdot pl \cdot (n-1) \cdot \alpha} \end{bmatrix} \cdot \begin{bmatrix} u_A \\ u_B \\ \vdots \\ u_N \end{bmatrix} \cdot \frac{V_{dc}}{l-1} \tag{3.40}$$

Matrix product in (3.40) can be easily obtained graphically. For $pl \neq 0$, it represents the sum of integer-magnitude vectors u_A to u_N placed on axes that make angles $pl \cdot \alpha \cdot 0$ to $pl \cdot \alpha \cdot (n-1)$ with the primary x-axis, while for $pl=0$ it is a scalar value, Σu_{LEG}. Further on, axes should be only scaled by $2/n \cdot V_{dc}/(l-1)$ for $pl \neq 0$, i.e. by $1/n \cdot V_{dc}/(l-1)$ for $pl=0$. This consideration can be very convenient for manual plotting of space vector projections.

Space vector projections for leg voltages, for a two-level five-phase and seven-phase inverter, are shown in Fig. 3.4 and Fig. 3.5, respectively. Axes are shown in the normalised form (e.g. [Wang (2002)] is using normalised form for plotting of the SV diagram, and also redefines the modulation index to accommodate this, $m=V^*/(2/n \cdot V_{dc})$). It can be seen that symmetry in each of planes is present, and therefore planes are divided into sectors. Notation of sectors will be always as in Fig. 3.4.

Space vector projections of leg voltages for a three-level five-phase inverter are shown in Fig. 3.6. For higher number of phases or higher number of levels, the number of switching states becomes very high, so that such cases will be considered separately, later on, through the characteristic sectors.

It can be seen that in some planes more than one switching state give the same projections, so that the redundancy is present. Redundancy of projections in different planes varies. Only those switching states whose projections are the same in all planes give the same multi-dimensional space vector and are hence redundant.

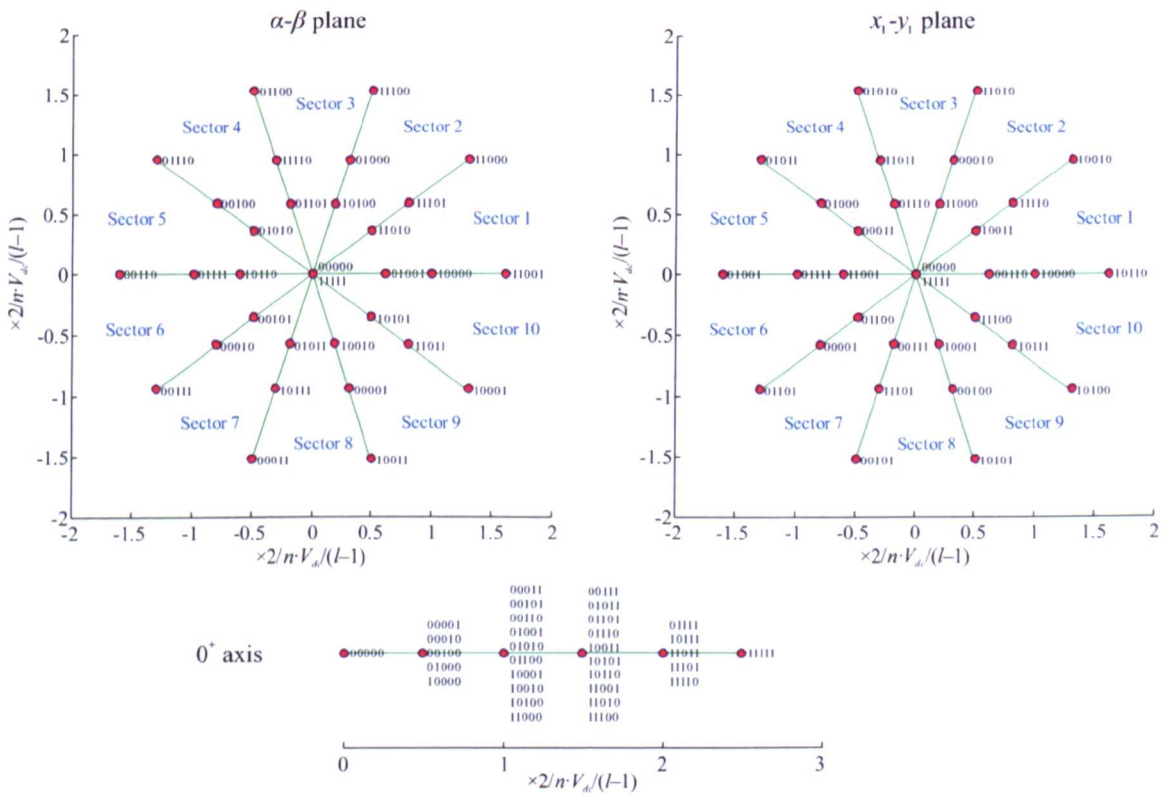


Fig. 3.4: Five-phase two-level inverter leg voltage space vector projections into the α-β, x_1-y_1 planes and 0^+ axis ($n=5$, $l=2$).

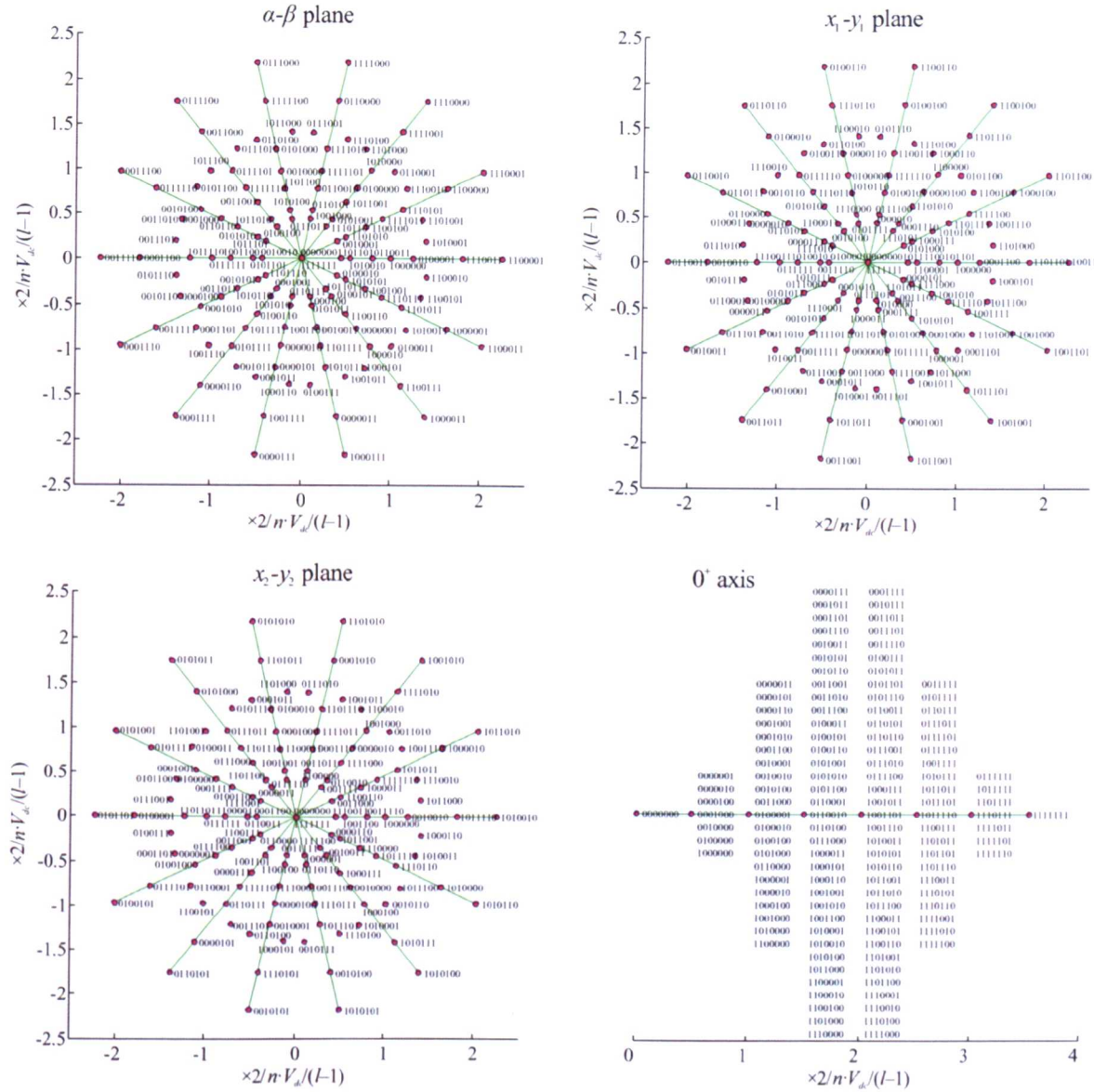


Fig. 3.5: Seven-phase two-level inverter leg voltage space vector projections into the α-β, x_1-y_1, x_2-y_2 planes and 0^+ axis (n=7, l=2).

Redundancy of phase voltage space vectors is important since it gives the information how many combinations of different leg voltages yield the same phase voltage. For example, the leg voltage space vectors represent all possible combinations of output leg voltages (the number of switching states is defined with (3.2)) and all of them are different, so the redundancy is not present. That means that the number of leg voltage space vectors is the same as the number of switching states, l^n. On the other hand, in the case of phase voltage space vectors, all have the same projection onto zero-axis, so that redundancy is present. The method of counting the number of phase voltage space vectors is given in [López et al. (2009b)], and final result is that all vectors whose corresponding switching states do not contain any leg with maximum value are not unique, i.e., are redundant. As a simple example, if all legs increase their level by one the phase voltage will remain the same so those two switching states produce redundant phase voltages.

Counting of space vectors is reduced to counting of those switching states that contain any leg voltage with maximum level. On the other hand, this is the same as to subtract all switching states that do not contain

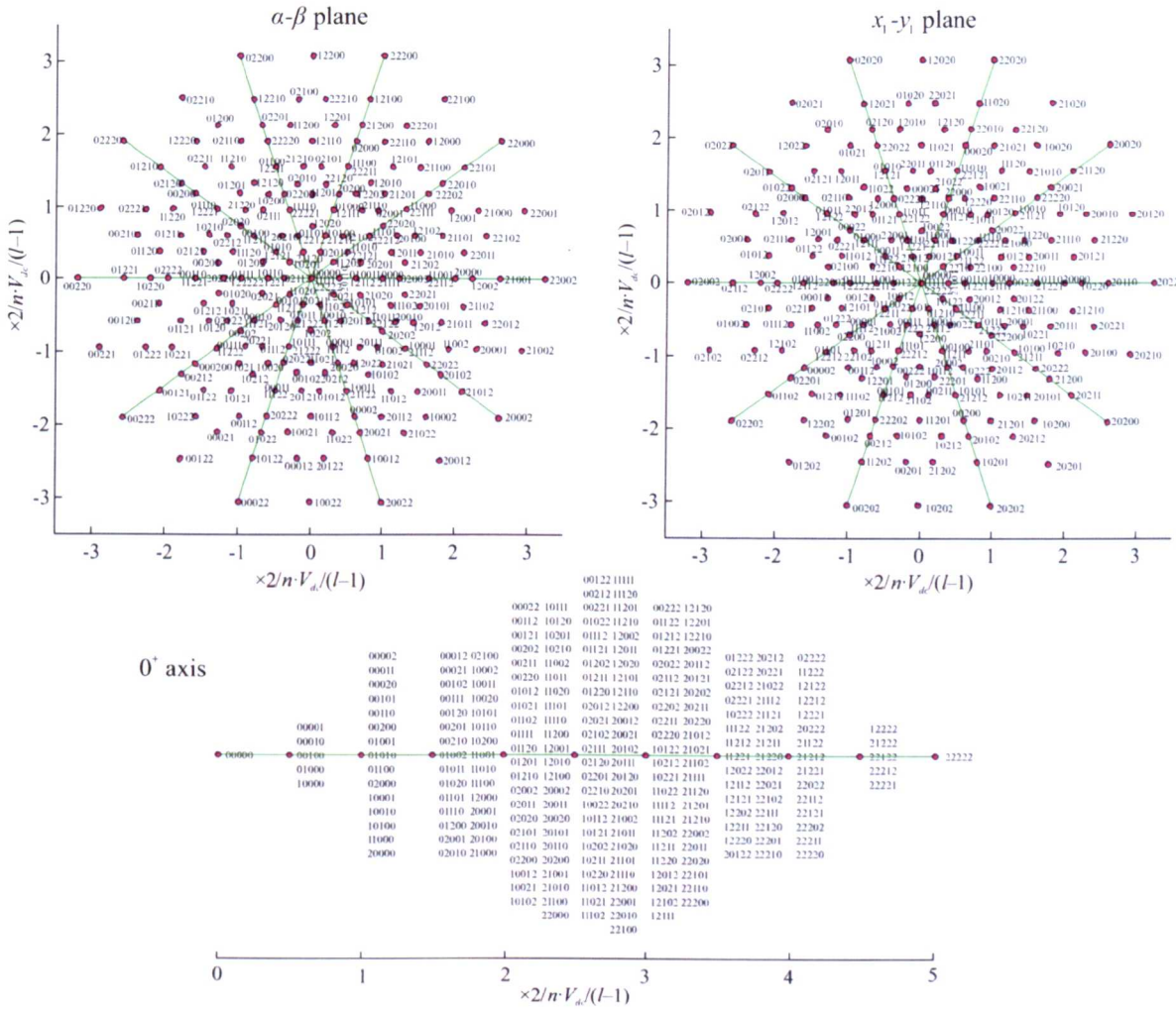


Fig. 3.6: Five-phase three-level inverter leg voltage space vector projections into the α-β, x_1-y_1 planes and 0^+ axis (n=5, l=3).

Table 3.1: Number of possible switching states and number of the phase voltage space vectors (given in brackets) for some of the configurations, most relevant to this research.

l / n	3	5	7
2	8 (7)	32 (31)	128 (127)
3	27 (19)	243 (211)	2187 (2059)
5	125 (61)	3125 (2101)	78125 (61741)

maximum level from the total number of switching states (3.2). Thus, the number of phase voltage space vectors is defined as [López et al. (2009b)]:

$$\text{Number of } v_{ph} \text{ SVs} = l^n - (l-1)^n \tag{3.41}$$

The numbers of switching states and unique phase voltage space vectors for cases that will be covered in this research are given in Table 3.1.

3.4.2 CALCULATION OF SPACE VECTOR APPLICATION TIMES

Space vector algorithms are based on selection of proper sequences of switching states and their times of application in such a way that desired shape of phase voltage is obtained on average. The controlled variables are output leg voltages and reference values are the desired phase voltages. With the explanation of equation (3.36)

it is shown that leg and phase voltage space vector projections into all planes, except 0^+ axis (pl=0), are the same. So for those planes ($pl \neq 0$) it can be said that process of averaging considers projections of the reference phase voltages and projections of obtainable phase voltages. Thus, it is obvious that space vector strategies do not control CMV that represents projection of the leg voltages to 0^+ axis (pl=0).

As already mentioned, *switching state* is the current state of the inverter output legs. Outputs are usually expressed in normalised form, so one example of the switching state of a five-phase three-level inverter is 22001 (see Fig. 3.6). *Switching sequence* is the set of consecutive switching states (space vectors), that is applied during one switching period, e.g.: 11001-11101-11111-21111-22111-22112-22111-21111-11111-11101-11001. The aim of the space vector methods is to at first determine switching sequence and then to determine times of applications of each switching state, so that the average value of the produced voltage in each phase is equal to the desired phase voltage during the switching period T_s.

Process of switching sequence creation is specific for each of the modulation strategies, but process of calculation of switching times can be regarded as general and will be explained shortly. Planes are mutually independent and process of averaging must be satisfied in all planes at the same time.

It is important to know the values of projections of reference voltages in all planes. In a general case, desired phase voltages are of arbitrary shape. It is assumed that they are all of the same shape, but mutually phase shifted for the characteristic angle $\alpha=2\pi/n$. According to the Fourier transformation they can be expressed as a sum of sinusoidal signals (harmonics), of the magnitudes V_h^* and angular frequencies $h\cdot\omega$, where ω is the fundamental angular frequency. Then, according to (3.30), space vector projection of the h^{th} harmonic into a certain plane is defined as:

$$\underline{v}_{h,pl}^{*} = A\cdot\frac{2}{n}\cdot\left[1 \quad e^{j\cdot pl\cdot\alpha} \quad \dots \quad e^{j\cdot pl\cdot(n-1)\cdot\alpha}\right]\cdot\begin{bmatrix} V_h^*\cdot\cos(h\cdot(\omega t-0\cdot\alpha)-\varphi_h) \\ V_h^*\cdot\cos(h\cdot(\omega t-1\cdot\alpha)-\varphi_h) \\ \vdots \\ V_h^*\cdot\cos(h\cdot(\omega t-(n-1)\cdot\alpha)-\varphi_h)\end{bmatrix} \tag{3.42}$$

where A=1/2 for pl=0, and A=1 otherwise, $\omega=2\pi f$ is the fundamental angular frequency and φ_h is for a particular harmonic the initial phase angle. Rewriting matrix multiplication as a sum and rewriting cosine function in exponential notation, (3.42) becomes:

$$\begin{aligned}\underline{v}_{h,pl}^{*} &= A\cdot\frac{2}{n}\cdot V_h^*\cdot\sum_{k=1}^{n} e^{j\cdot pl\cdot(k-1)\alpha}\cdot\cos(h(\omega t-(k-1)\cdot\alpha)-\varphi_h) \\ &= A\cdot\frac{2}{n}\cdot V_h^*\cdot\sum_{k=1}^{n} e^{j\cdot pl\cdot(k-1)\alpha}\cdot\frac{e^{j(h\omega t-h(k-1)\cdot\alpha-\varphi_h)}+e^{-j(h\omega t-h(k-1)\cdot\alpha-\varphi_h)}}{2}\end{aligned} \tag{3.43}$$

Leaving under the sum only the k-dependent terms, one gets:

$$\underline{v}_{h,pl}^{*} = A\cdot\frac{V_h^*}{n}\cdot\left(e^{j(h\omega t-\varphi_h)}\cdot\sum_{k=1}^{n} e^{j\cdot(pl-h)\cdot(k-1)\alpha}+e^{-j(h\omega t-\varphi_h)}\cdot\sum_{k=1}^{n} e^{j\cdot(pl+h)\cdot(k-1)\alpha}\right) \tag{3.44}$$

Sums in (3.44) represent geometrical progressions and one gets that the first one is equal to 0 for any value of (pl–h) except for (pl–h)=$int\cdot n$, when the value of the sum is n. Variable int is an integer number. Similarly, the second sum is 0 for any value of (pl+h) except for (pl+h)=$int\cdot n$, when the value of the sum is n. The only mathematical solution when both sums in (3.44) have non-zero values appears when (h–pl)=$int_1\cdot n$ and (h+pl)=$int_2\cdot n$. Since value of pl is limited from 0 to (n–1)/2 for odd n, i.e. 0 to n/2 for even n, this is only

possible for $pl=0$ (for the same int_1 and int_2) and for $pl=n/2$, when n is an even number (for consecutive int_1 and int_2). In that case:

$$v^*_{h,0/\frac{n}{2}} = \frac{1}{2}\cdot\frac{V^*_h}{n}\cdot\left(e^{j(h\omega t-\varphi_h)}\cdot n + e^{-j(h\omega t-\varphi_h)}\cdot n\right) = V^*_h\cdot\cos(h\omega t-\varphi_h) \tag{3.45}$$

where $h=int\cdot n$ for $pl=0$, i.e. $h=int\cdot n+n/2$ for $pl=n/2$ for even n.

For other values of pl ($pl\neq 0$ and $pl\neq n/2$) for certain value of h only one of the sums in (3.44) has non-zero value, n. If $h=int\cdot n+pl$ then the first sum has non-zero value, and if $h=int\cdot n-pl$ then it is the second sum. The value of the projection in those cases is:

$$\begin{aligned} \underline{v}^*_{h,pl} &= 1\cdot\frac{V^*_h}{n}\cdot\left(e^{j(h\omega t-\varphi_h)}\cdot n + e^{-j(h\omega t-\varphi_h)}\cdot 0\right) = V^*_h\cdot e^{j(h\omega t-\varphi_h)} && \text{for } h=int\cdot n+pl \\ \underline{v}^*_{h,pl} &= 1\cdot\frac{V^*_h}{n}\cdot\left(e^{j(h\omega t-\varphi_h)}\cdot 0 + e^{-j(h\omega t-\varphi_h)}\cdot n\right) = V^*_h\cdot e^{-j(h\omega t-\varphi_h)} && \text{for } h=int\cdot n-pl \end{aligned} \tag{3.46}$$

From (3.45) it is obvious that phase voltage space vector projections to 0^+ and 0^- axes are real numbers, with maximum value of $\pm V^*_h$. Projections are of the same form, but different harmonics are mapped into different planes. From (3.46) it can be seen that projections into other planes represent complex numbers which move along a circle of radius V^*_h with an angular frequency of $h\cdot\omega$. Direction of rotation for the harmonics of two equations in (3.46) is opposite. The starting angle is determined by φ_h.

In general, one can say that harmonics h that map into the plane pl are determined with:

$$h = int\cdot n \pm pl \tag{3.47}$$

One example of mapping of the phase voltage harmonics, with direction of rotation in a certain plane, for five-phase and symmetrical six-phase case, is shown in Fig. 3.7.

The process of digitalisation is always present in the digital signal processor based control of an inverter supplied drive. Hence, it is important to note that projections of discretised reference voltages into certain planes are discrete points on a circle, rather than continuous values. The angular distance between two consecutive

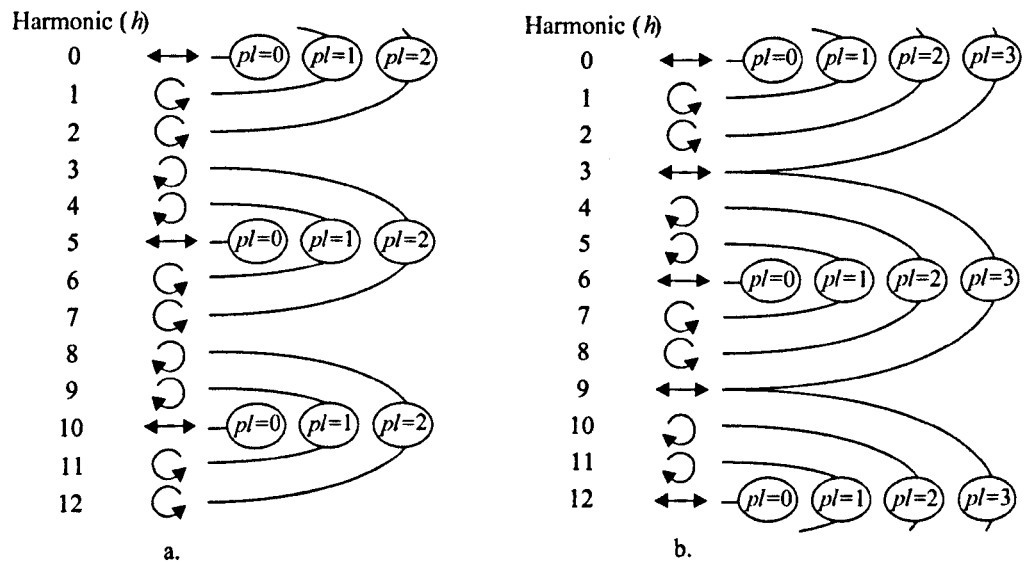


Fig. 3.7: Mapping of the reference phase voltage harmonics for: a. five-phase and b. six-phase case.

samples is determined as $h \cdot \omega \cdot T_s$, so that it is higher for higher harmonics. Also, direction of rotation is different for different h, as already explained.

The reference projection is actually determined by the sum of discrete values of the desired harmonics that map into a certain plane. If there is more than one harmonic (that maps into the certain plane), the trajectory is not circular. However, desired phase voltage references in this research are of the pure sinusoidal shape. That means that only the projections into the α-β plane (pl=1) belong to a circle, while projections into other planes are zero.

Determination of times of application requires knowledge of the chosen space vectors and the desired phase voltage reference projections into each plane. Since process represents a graphical averaging and some of the chosen switching states can be redundant, it is not important to know the exact switching sequence. It is enough to know chosen space vectors that will be used. Switching state redundancy in that case allows creation of more possible switching sequences. It is shown in [Kelly et al. (2003)] that, for obtaining the pure sinusoidal output in an n-phase case, n space vectors should be applied. Process of volt-second averaging can be done by projecting reference and chosen space vectors to any two arbitrary chosen axes x_{pl} and y_{pl} in each of the planes, pl, and applying voltage-second balance equation to each axis in each plane. Time of application of each space vector is determined by solution of the system of equations:

$$\begin{aligned} v^*_{x_{pl}} \cdot T_s &= \sum_{i=1}^{n} v_{x_{pl},i} \cdot T_i \\ v^*_{y_{pl}} \cdot T_s &= \sum_{i=1}^{n} v_{y_{pl},i} \cdot T_i \\ T_s &= \sum_{i=1}^{n} T_i \end{aligned} \tag{3.48}$$

where pl takes all values from 1 to $(n-1)/2$ for odd n, i.e. 1 to $n/2$ for even n, and index i stands for the i^{th} applied space vector. Axis pl=0, i.e. 0^+ axis, is not considered in (3.48) and, instead of it, the n^{th} equation for an n-variable system guarantees that the sum of application times is T_s. As already mentioned, space vector algorithms do not consider 0^+ axis. The projection to this axis, as already shown, represents CMV, hence replacement of the CMV equation with the time-balancing equation is logical. Axes x and y can be selected arbitrarily, but the best choice is to set x-axis as the real and y-axis as imaginary axis of the plane. Projections onto these axes are automatically determined by the space vector transformation. Rewritten in matrix form, (3.48) becomes:

$$\begin{bmatrix} v^*_{\alpha} \\ v^*_{\beta} \\ v^*_{x_1} \\ v^*_{y_1} \\ \vdots \\ 1 \\ v^*_{0^-} \end{bmatrix} \cdot T_s = \begin{bmatrix} v_{\alpha,1} & v_{\alpha,2} & \cdots & v_{\alpha,n} \\ v_{\beta,1} & v_{\beta,2} & \cdots & v_{\beta,n} \\ v_{x_1,1} & v_{x_1,2} & \cdots & v_{x_1,n} \\ v_{y_1,1} & v_{y_1,2} & \cdots & v_{y_1,n} \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \\ v_{0^-,1} & v_{0^-,2} & \cdots & v_{0^-,n} \end{bmatrix} \cdot \begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_n \end{bmatrix} \tag{3.49}$$

Finally, solving for matrix with times of application, one gets:

$$\begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_n \end{bmatrix} = \begin{bmatrix} v_{\alpha,1} & v_{\alpha,2} & \cdots & v_{\alpha,n} \\ v_{\beta,1} & v_{\beta,2} & \cdots & v_{\beta,n} \\ v_{x_1,1} & v_{x_1,2} & \cdots & v_{x_1,n} \\ v_{y_1,1} & v_{y_1,2} & \cdots & v_{y_1,n} \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \\ v_{0^-,1} & v_{0^-,2} & \cdots & v_{0^-,n} \end{bmatrix}^{-1} \cdot \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ v_{x_1}^* \\ v_{y_1}^* \\ \vdots \\ 1 \\ v_{0^-}^* \end{bmatrix} \cdot T_s \tag{3.50}$$

where $v_{p,i}$ is the projection of the i^{th} chosen space vector onto the axis p, $p=\alpha, \beta, x_1, y_1, \ldots$ and 0^-, and $i=1$ to n. Variable v_p^* is the projection of the reference phase voltage space vector onto p-axis.

If number of phases is an odd number and if pure sinusoidal output is desired, as it is the case in this research, 0^- axis is not present, and reference projections into x-y planes are zero, so that (3.50) becomes:

$$\begin{bmatrix} T_1 \\ T_2 \\ \vdots \\ T_n \end{bmatrix} = \begin{bmatrix} v_{\alpha,1} & v_{\alpha,2} & \cdots & v_{\alpha,n} \\ v_{\beta,1} & v_{\beta,2} & \cdots & v_{\beta,n} \\ v_{x_1,1} & v_{x_1,2} & \cdots & v_{x_1,n} \\ v_{y_1,1} & v_{y_1,2} & \cdots & v_{y_1,n} \\ \vdots & \vdots & \ddots & \vdots \\ 1 & 1 & \cdots & 1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ v_{x_1}^* \\ v_{y_1}^* \\ \vdots \\ 1 \end{bmatrix} \cdot T_s \tag{3.51}$$

This equation is in the form that will be usually used in this research.

3.5 MULTILEVEL INVERTER TOPOLOGIES

Multilevel inverters are becoming more attractive in high-voltage and high-efficiency applications because of the following characteristics [Rodríguez et al. (2002)]:

1) Multilevel inverters produce staircase waveform output leg voltage with lower total harmonic distortion (THD) and lower dv/dt compared to the classical two-level VSIs.

2) They draw input current with very low distortion.

3) They generate smaller CMV steps (that is the same as for phase voltages, (3.14)), thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CMV can be eliminated.

4) They can operate with a lower switching frequency, i.e. effective switching frequency to achieve the same voltage characteristics is lower than with the two-level inverter.

An ideal inverter can be regarded as a 'black-box' amplifier. However, the inverter topology is what specifies certain type of realisation of the inverter, and sometimes requires special features from the modulation strategy. A general classification of multilevel inverters is given in [Rodríguez et al. (2007)]. Classification branch of interest for this project, and in general for motor drives, is the entry 'indirect converters, voltage source, multilevel inverters'. There are a lot of different multilevel structures, but the main circuit topologies of these inverters that have been successfully implemented as standard products for medium-voltage industrial drives are [Rodríguez et al. (2002), Wu (2006), Rodríguez et al. (2007), Seyed (2007)]:

1) diode-clamped or neutral-point clamped voltage source inverters, NPC VSI;

2) serially connected multi-cells with separate dc sources or cascaded H-bridges, CHB VSI; and

3) capacitor-clamped or flying capacitor, FC VSI.

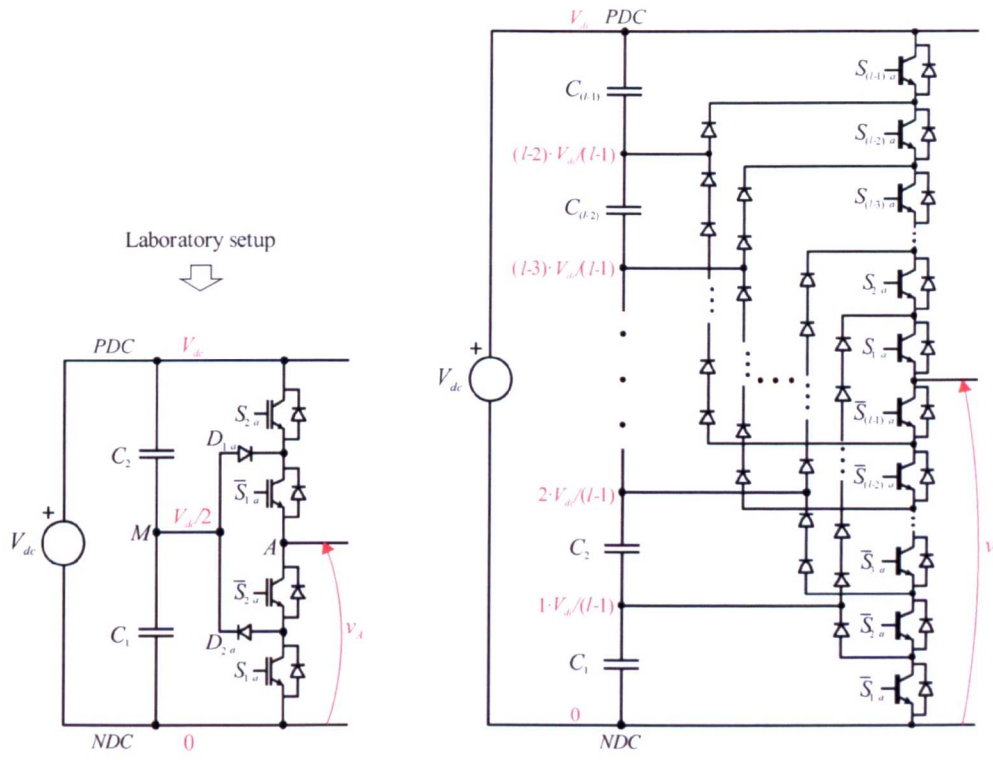


Fig. 3.8: Neutral-point clamped inverter (*NPC*): a. three-level case (switch notation corresponds to the laboratory setup), b. general case.

Currently these topologies cover voltage ranges from 2.3 to 13.8 kV [Rodríguez et al. (2007)].

A three-level diode-clamped inverter is shown in Fig. 3.8a. In this circuit, the dc-bus voltage is split into three levels by two series-connected bulk capacitors. The key components that distinguish this circuit from a conventional two-level inverter are diodes $D_{1\,a}$ and $D_{2\,a}$, that 'clamp' output voltage to the midpoint of the dc-bus. Sometimes, the middle point in three-level case is called neutral point, hence the name neutral-point clamped (NPC).

In Fig. 3.8b, an extension of the NPC topology to multilevel case is shown. In this case, diodes clamp output voltage to the dc-link capacitor voltages rather than to the neutral point (which, for even number of levels, is even not present). That means that the name NPC is not formally correct for multilevel diode-clamped inverters, but it is widely in use and will be also used here.

In general, one phase leg consists of $2(l–1)$ active switches and $(l–1)\cdot(l–2)$ clamping diodes with the same reverse blocking voltage. The total dc bus voltage V_{dc} is distributed across the dc capacitors C_1, C_2, …, $C_{(l-1)}$. Hence, an output voltage of 0, $1/(l–1)\cdot V_{dc}$, $2/(l–1)\cdot V_{dc}$, …, V_{dc} can be obtained at the leg output, v_A [Seyed (2007)]. The main problems of this topology are capacitor voltage balancing, different switching load of IGBTs and high voltage stress on the clamping diodes. For more than three levels, voltage balancing problem cannot be overcome by modulation techniques. Balancing circuits should be applied instead. This makes the NPC configuration unattractive for more than three levels [Seyed (2007)].

Switches are triggered in complementary pairs, i.e. when one of the complementary switches is on, the other one must be off. Complementary switches, such as pair $S_{1\,a}$ and $\overline{S}_{1\,a}$, for example, are connected with clamping diode branches (Fig. 3.8).

Table 3.2: Correlation of the IGBT switching states with output leg voltage for the used three-level NPC inverter.

S1	S2	Leg voltage (v_A)	Description
0	0	$V_{dc}/2$	Output connected to the middle point
0	1	0	Output connected to the PDC rail
1	0	V_{dc}	Output connected to the NDC rail
1	1	3-state	Floating output

A three-level NPC inverter is used in the experimental investigation in this research (see Appendix A). The switch notation in Fig. 3.8a is not the common one (in contrast to Fig. 3.8b), but it corresponds to the real, used, setup. In Table 3.2, correlation of the semiconductor switching states with an output leg voltage is shown.

Another fundamental topology of multilevel inverters is the flying capacitor, FC VSI. Flying capacitor inverter topologies for the three-level and for a general case are shown in Fig. 3.9. As the NPC, this topology also needs only one dc source for the supply. It uses capacitors rather than diodes. Voltage level of capacitor branches defines output leg voltage. Compared to NPC, flying capacitor inverter has one attractive feature, switching redundancy within the leg, which can be used for flying capacitor voltage balancing [Seyed (2007)].

One leg of FC topology inverter consists of $2(l-1)$ active switches and $(l-1)\cdot(l-2)/2$ flying capacitors of the same capacitance. Also $(l-2)$ dc link capacitors are present. The voltage on each capacitor is $V_{dc}/(l-1)$ (Fig. 3.9). The main problem of this topology is the capacitor voltage balancing [Rodríguez et al. (2002)].

The third very popular topology is the cascaded H-bridge, CHB. It is different from the above mentioned two and it is based on series connection of single-phase inverters with separate dc sources. Fig. 3.10a shows the power circuit for one leg of a three-level H-bridge (full-bridge), that is the basic unit for CHB topology, and one leg circuit for CHB structure with an arbitrary number of levels (Fig. 3.10b). The resulting leg voltage is

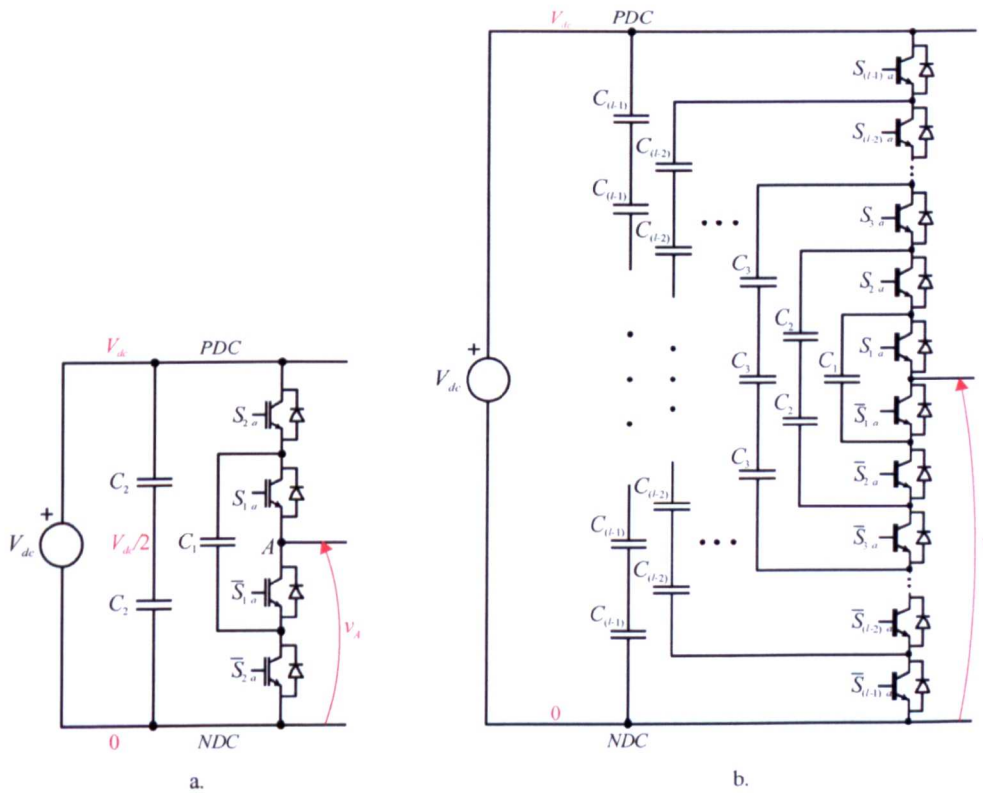
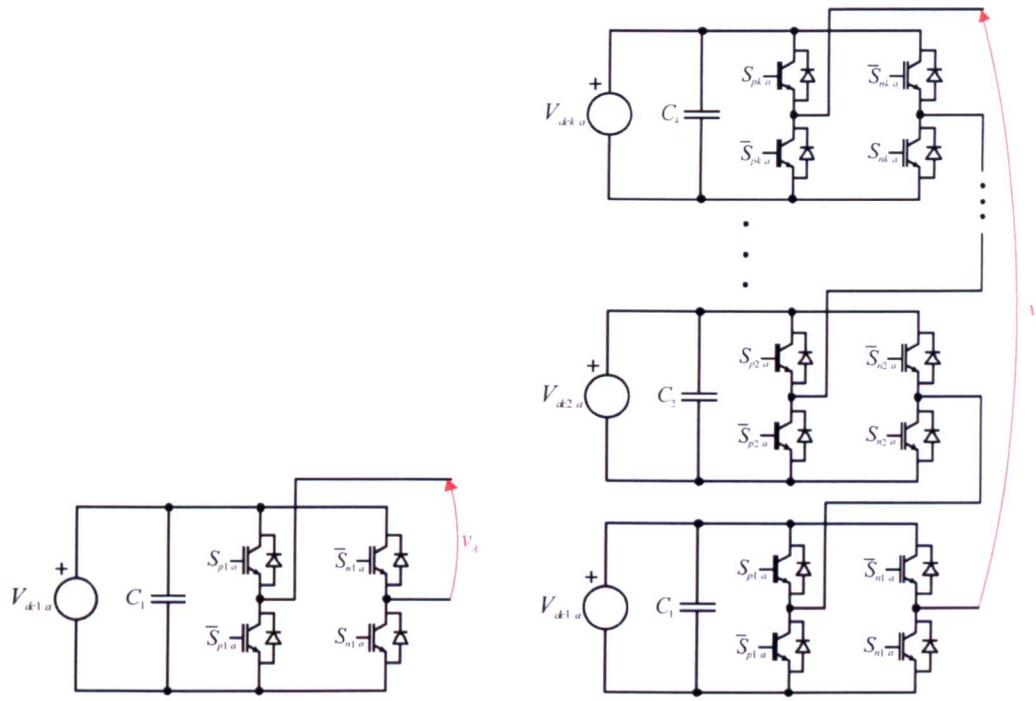


Fig. 3.9: Flying capacitor (FC) inverter topology: a. three-level case, b. general case.



a. b.

Fig. 3.10: Cascaded H-bridge (CHB) inverter topology: a. full-bridge (three-level) basic cell, b. general case.

obtained by the addition of voltages generated by different cells. Each single-phase H-bridge inverter can generate three voltages at the output, $-V_{dc\,i}$, 0 and $V_{dc\,i}$, where i stands for the i^{th} cell. Depending on the number of cells in a leg and dc voltage ratio between cells, the number of output levels changes [Manjrekar et al. (2000)]. The basic topology uses the same voltage supply for each cell [Rodríguez et al. (2002)], since otherwise the cell power rating would be unequal and the design of the cells may have to be different from each other. This leads to asymmetry and non-modular structure, that are not desirable.

The main advantage of the CHB structure is the ability to synthesize higher number of output voltage levels with an excellent harmonic spectrum utilising low-cost low-voltage power semiconductors and capacitors. Also, modulation, control, and protection requirements of each bridge are modular, which makes CHB very attractive for usage [McGrath and Holmes (2002)]. However, the main drawback of this topology is the need to supply each cell with a complex and expensive isolated transformer [Seyed (2007)]. Also, potential advantages of a hybrid structure, with non-equal dc-bus voltages per cell, and improvement of output voltage characteristics are always obtained at the expense of the loss of modularity and loss of redundancy that can be used for different purposes [Leon et al. (2008a)].

3.6 SUMMARY

This chapter contains the basic equations, definitions and explanations that will be used in the thesis. The main configuration of the system that will be analysed and all voltages and currents of interest are defined. Some rules related to symbols and notation, are introduced. In particular, definitions of leg voltages, switching states, leg-to-leg voltages, phase voltage, common mode voltages, etc. are given. Definitions cover the nature of the signals and, for digitalised signals, the number of levels and basic step calculations. Wherever possible,

equations are given in scalar and in matrix form. Decoupling transformation that defines space vectors is introduced. Transformation is given in a variety of different forms. Space vectors are defined and the number of phase voltage space vectors and redundancy are introduced. It is shown how different harmonics of the reference voltage map into different planes. Calculation of space vector application times is explained in a general case. At the end, basic multilevel inverter topologies with their main advantages and drawbacks are presented.

Chapter 4

MULTILEVEL MULTIPHASE SPACE VECTOR MODULATION TECHNIQUES

4.1 INTRODUCTION

This chapter analyses space vector algorithms for multilevel multiphase inverters. The goal is always to create sinusoidal output phase voltages since the analysed load is an induction machine with sinusoidally distributed windings. Space vectors are defined as in section 3.4, where an explanation of space vector projections is also given. Process of representation of space vectors through the projections is usually called vector space decomposition (VSD) and it was introduced by [Zhao and Lipo (1995)]. VSD approach is widely in use in conjunction with multiphase two-level inverters.

Extension of space vector modulation from two to more levels is not straightforward. The number of possible switching states of a VSI is defined as l^n, where n is the number of phases and l is the number of output voltage levels per inverter leg. This gives exponential increase in the number of switching states as both the number of levels and the number of phases increase, and this represents the main problem in development and application of SVPWM algorithms.

PWM techniques for multiphase multilevel inverters have started attracting attention only recently [Levi (2008)]. However, majority of existing works are either based on extension of the three-phase algorithms and utilisation of the three nearest vectors, or on some other principles that do not account for the existence of x-y planes. This produces large low-order harmonics. Some other methods use different approaches, that are closer to the carrier-based one, and do not use VSD approach. Survey of the relevant papers was given in section 2.5.

The first paper that applies VSD approach to multilevel multiphase inverters is [Gao and Fletcher (2010)]. The considered case is a three-level five-phase neutral-point clamped VSI. Another paper that applies VSD approach to a three-level seven-phase inverter for the first time [Dordevic et al. (2011b)] is the result of this thesis. The core algorithm follows the methodology of [Gao and Fletcher (2010)], but the paper reveals problems and gives solutions when the number of phases increases. Both cases are explained in detail in the following sections 4.2 and 4.3. One modification of the algorithms is also presented. Simulation and experimental results are further included in sub-sections 4.2.8 and 4.3.8. Only basic results that confirm correctness of the algorithms are shown, while comparison between modulation strategies is left for Chapter 6. Finally, section 4.4 briefly discusses algorithm generalisation.

Original contributions of this chapter has been presented in three conference papers [Dordevic et al. (2011b), Dordevic et al. (2011a), Jones et al. (2011a)] and three journal papers [Jones et al. (2012), Dordevic et al. (2013a), Dordevic et al. (2013b)]. Content of section 4.2 has been used in [Dordevic et al. (2011a), Dordevic et al. (2013a)]. In [Jones et al. (2011a), Jones et al. (2012)] a comparison with open-end winding algorithms is reported. Content of section 4.3 is available in [Dordevic et al. (2011b), Dordevic et al. (2013b)].

4.2 FIVE-PHASE THREE-LEVEL SPACE VECTOR ALGORITHM BASED ON VSD APPROACH

As noted, the first VSD-based SVPWM control strategy for multiphase machines supplied from multilevel VSIs is given in [Gao and Fletcher (2010)]. Configuration of the analysed topology, the three-level five-phase NPC VSI supplied drive system, is shown in Fig. 4.1. One logical but novel way of elimination of switching states that are not useful, as well as determination of switching sequences and their sub-sectors of application, are proposed in this paper. Suppression of the low-order harmonics is provided by cancelation of space vectors in the x_1-y_1 plane, and choice of redundant switching sequences is done in such a way as to provide as good as possible capacitor voltage balancing, and minimisation of the switching losses. Although the proposed method contains clear and universal steps for any number of phases and any number of levels, the problem is that it requires a lot of manual manipulation, and some geometry in the process of region partitioning. Hence, the algorithm will be explained here step by step, in the following sub-sections. For a number of steps, new specific solutions are given, with a tendency for simplification and generalisation. It will be shown finally that method is simple for implementation and simulation and experimental results will be given.

4.2.1 VECTOR SPACE DECOMPOSITION

Process of VSD has already been explained in section 3.4, and it will be here only briefly reviewed. In the considered case of a five-phase three-level inverter (n=5, l=3), according to (3.2) there are 3^5=243 switching states, and 211 unique phase voltage space vectors (from equation (3.41), 3^5-2^5=211). Leg voltage space vector projections and corresponding switching states are shown in Fig. 3.6. Desired phase voltages are sinusoidal, and for symmetrical case can be defined, in general, as:

$$v_{ph}^{*}(t) = V^{*} \cdot \cos(2\pi ft - 2\pi / n \cdot (ph-1)) \tag{4.1}$$

where V^* and f are the amplitude and frequency of the desired phase voltages, n is the number of phases, and ph=a to n determines the phase. VSD can be applied to any set of desired and obtained phase and leg voltages. From Fig. 3.2 it can be seen that the route from the desired to obtained phase voltages is through the desired leg and output leg voltages, so the analysis has to be done in terms of projections of all of them. From the discussion after equation (3.36), it is clear that projections of desired and obtained leg and phase voltages are different only in 0^+ axis, i.e. in CMV. Therefore, VSD based algorithms do not consider CMV voltage, and directly apply

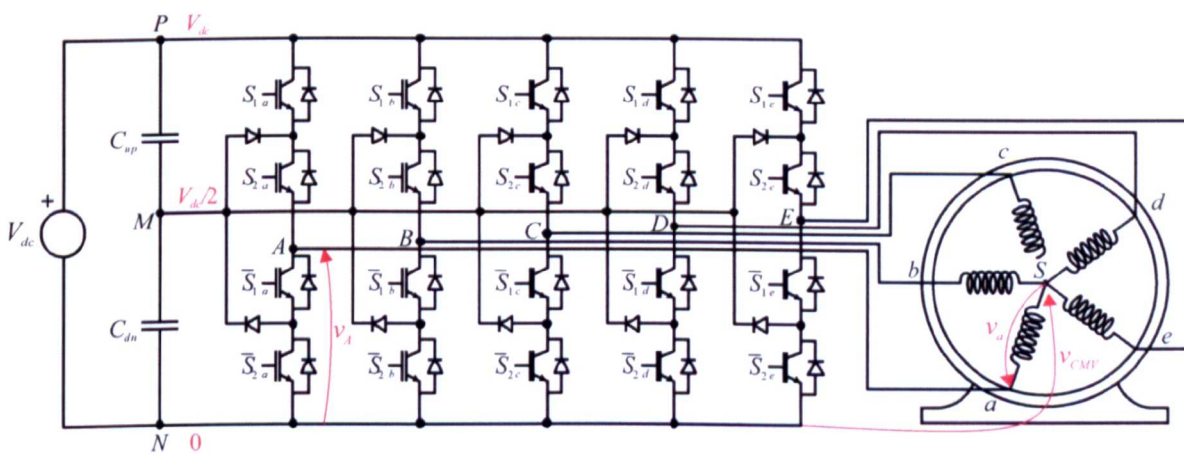


Fig. 4.1: Analysed topology of a three-level five-phase NPC VSI-supplied induction motor drive.

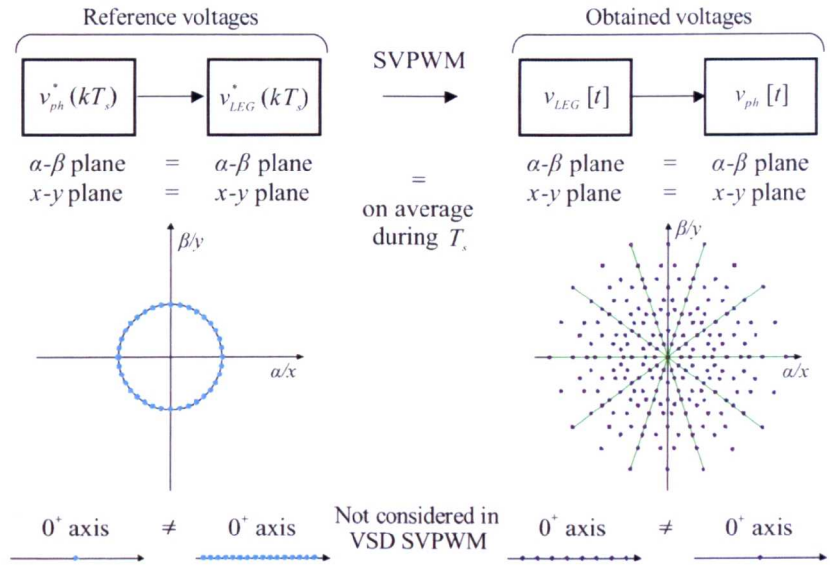


Fig. 4.2: Graphical description of the VSD SVPWM.

process of averaging (PWM) in all other planes for desired and obtained values. This process is graphically described in Fig. 4.2.

4.2.2 ORDER-PER-SECTOR LAW AND REDUCTION OF THE NUMBER OF SWITCHING STATES

From the comparison of the time domain relationships and switching states in the α-β plane, a very simple method for elimination of the switching states that are not useful has been developed in [Gao and Fletcher (2010)]. Correlation between reference phase and reference leg voltages is given as:

$$v^*_{ph}(t) = v^*_{LEG}(t) - (1/n)\sum_{LEG=A}^{N} v^*_{LEG}(t) = v^*_{LEG}(t) - C(t) \tag{4.2}$$

where index *LEG* identifies the leg and takes the same values as the motor phase index *ph*. It is clear from (4.2) that the order of the reference phase voltages is the same as the order of the reference leg voltages at all times since the value $C(t)$ is the same for any of *LEG-ph* index pair. The same equation with the same conclusion can be given for obtained output leg and phase voltages.

It is thus clear that the same order will be followed between the reference and between the obtained phase and leg voltages independently, as it is shown in (4.2). For example, if $v^*_a \geq v^*_b$, that means that reference leg voltages will follow the same relationship, $v^*_A \geq v^*_B$; and also, if $v_A \geq v_B$ that automatically means that for the obtained phase voltages $v_a \geq v_b$ will be true. However, it does not necessarily mean that if $v^*_a \geq v^*_b$, then $v_a \geq v_b$, or if $v^*_A \geq v^*_B$ then $v_A \geq v_B$, in each instant of time. Whether or not this is satisfied, depends on the type of the modulation technique.

Let us consider five-phase three-level case, but note that following explanations are also valid in a general case. If a symmetrical PWM is considered, and if transitions are only for one step (for minimum losses), then if $v^*_A \geq v^*_B$ relationship $v_A \geq v_B$ always holds true (Fig. 4.3a and Fig. 4.3b). Note that instead of > sign, ≥ must be used. Some counter examples when obtained leg voltage signals are not centred, or when non-equal leg voltage steps are in use, are shown in Fig. 4.3c and Fig. 4.3d. Here it is shown that in those cases produced leg voltages do not follow ordering of the reference leg voltages. Finally, one can say that, according to the explanations of (4.2) and Fig. 4.3, if symmetrical PWM is utilised in conjunction with the principle of minimum losses (application of two

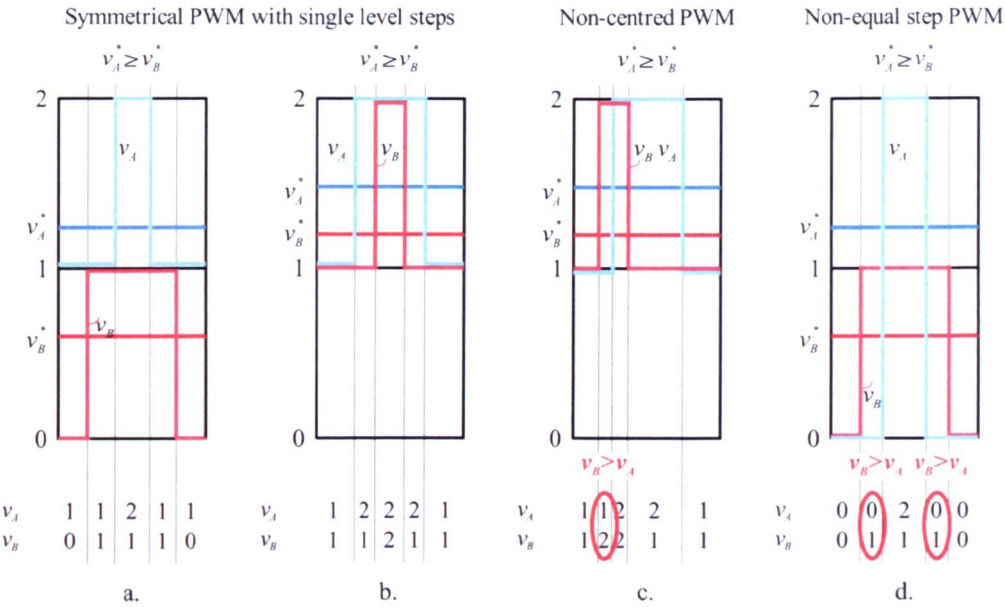


Fig. 4.3: Leg voltages will follow ordering of the reference leg voltages if sequence is symmetrical with single level steps (a. and b.). Counter examples for: c. asymmetrical PWM, d. non-equal step PWM case.

nearest leg voltage levels), then produced values of phase and output leg voltages will follow order of reference leg and phase voltages, in each instant of time.

The phase voltage references in the five-phase case change their order each 36°, and in this way the full period can be divided into 10 sectors, Fig. 4.4. Order of reference phase voltages in each sector is summarised in Table 4.1. According to (3.46), space vector trajectory of the sinusoidal reference phase voltages (4.1) in the α-β plane is a circle with magnitude V^* and angle ωt. This means that angle of 36° directly corresponds to the sector angle, so sectors from the time domain correspond to the sectors in the α-β plane.

Taken together, this gives definition of the order-per-sector law, that ordering of phase voltages in each sector in time domain will be followed by the ordering of digital values of output leg voltages in an appropriate sector in the α-β plane, if symmetrical PWM principle with single level step is in use.

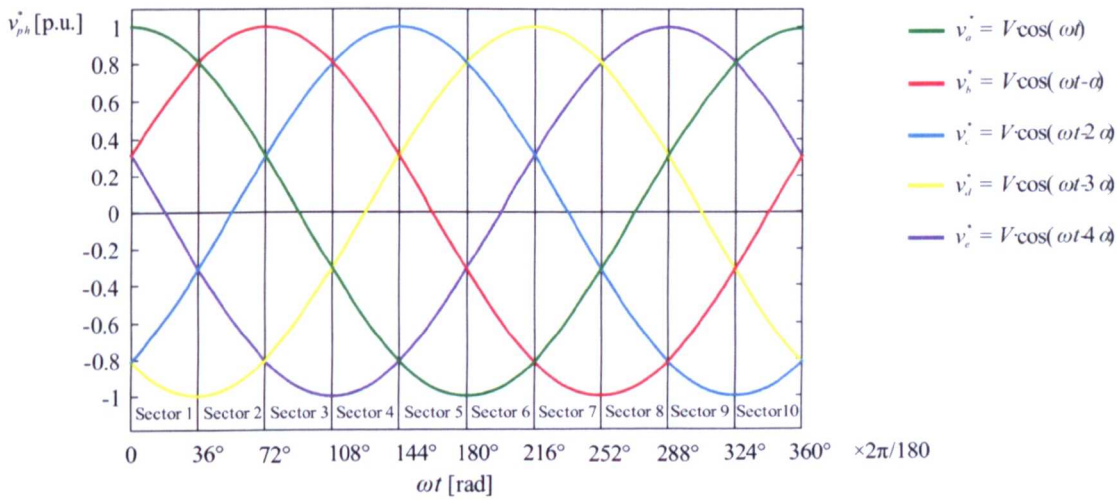


Fig. 4.4: Desired phase voltages for five-phase induction machine in time domain, with identified sectors that correspond to the sectors in the α-β plane of Fig. 3.6.

Table 4.1: Order-per-sector law for phase voltages for the five-phase case (see Fig. 4.4).

Sector	Phase voltages order
1	$v_a^* \geq v_b^* \geq v_e^* \geq v_c^* \geq v_d^*$
2	$v_b^* \geq v_a^* \geq v_c^* \geq v_e^* \geq v_d^*$
3	$v_b^* \geq v_c^* \geq v_a^* \geq v_d^* \geq v_e^*$
4	$v_c^* \geq v_b^* \geq v_d^* \geq v_a^* \geq v_e^*$
5	$v_c^* \geq v_d^* \geq v_b^* \geq v_e^* \geq v_a^*$
6	$v_d^* \geq v_c^* \geq v_e^* \geq v_b^* \geq v_a^*$
7	$v_d^* \geq v_e^* \geq v_c^* \geq v_a^* \geq v_b^*$
8	$v_e^* \geq v_d^* \geq v_a^* \geq v_c^* \geq v_b^*$
9	$v_e^* \geq v_a^* \geq v_d^* \geq v_b^* \geq v_c^*$
10	$v_a^* \geq v_e^* \geq v_b^* \geq v_d^* \geq v_c^*$

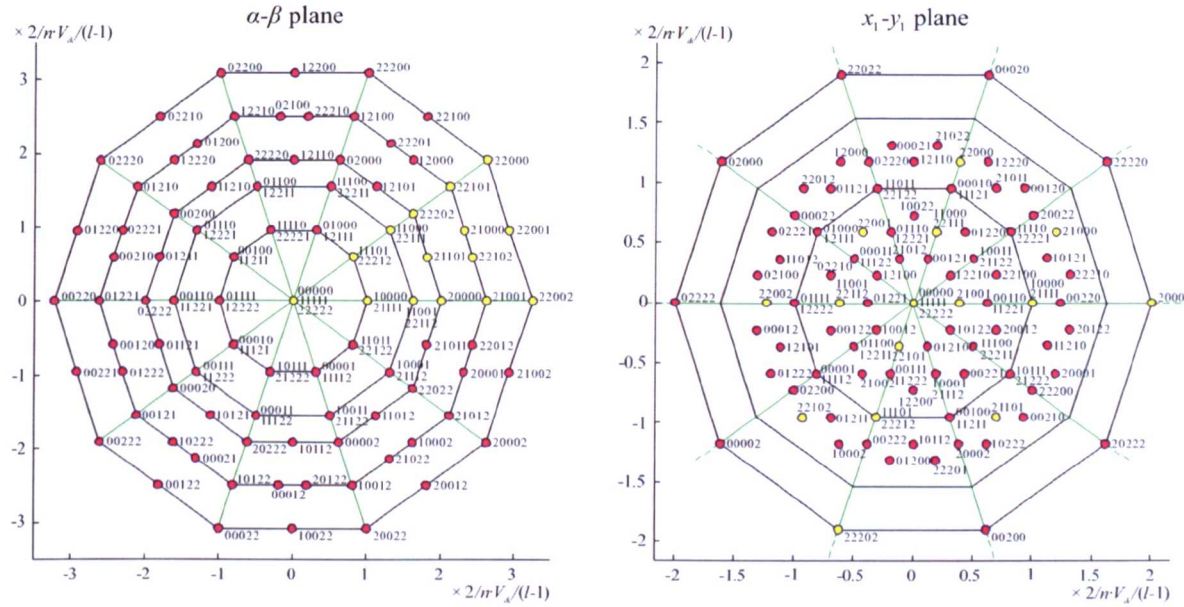


Fig. 4.5: Remaining space vectors in the α-β and x_1-y_1 plane after application of the order-per-sector law.

According to the previous explanations, if sinusoidal output is desired, all switching states that do not satisfy required order-per-sector law should be eliminated. For example, switching state 22011 belongs to the first sector (Fig. 3.6), but does not satisfy required ordering for the first sector, since $v_D > v_C$. The number of switching states of interest can be significantly reduced in this way, from 243 to 113. Projections of space vectors of 113 remaining switching states, into α-β and x_1-y_1 plane, are given in Fig. 4.5. Space vectors from the first sector and those from the second that are at the sector border line are shown in different colour, since later on only the first sector will be analysed. Note that scales for two planes in Fig. 4.5 are different. Number of switching states that correspond to the same space vector remain unchanged after this space vector number reduction. It can be seen that this method of reducing the number of switching states, according to the order-per-sector law, is general for any number of phases and any number of levels [Gao and Fletcher (2010)].

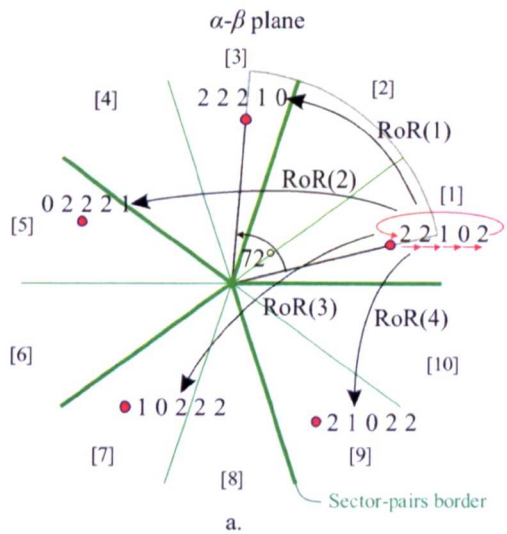
4.2.3 DETERMINATION OF POSSIBLE SWITCHING SEQUENCES

Next, switching sequences should be determined. Switching sequence represents the set of switching states that should be applied during one switching period, T_s. The rules that should be satisfied during determination of the switching sequences are as follows:

1) In order to produce sinusoidal output in an n-phase machine, switching sequence must contain n space vectors [Kelly et al. (2003)].
2) During one switching period every leg has to once increase and once decrease its level. In this way, each leg can produce desired value on average and the first and the last switching state are the same, so that moving to the next switching period minimises losses.
3) Symmetrical sequences are desirable, so it is assumed that in the first half of the switching period all legs increase their level, while in the second half all legs decrease the level.
4) For the sake of loss minimisation and reduction of dv/dt, increase and decrease is always for one level. Higher step (e.g. from 0 to 2) will produce higher dv/dt, and also more switches would change state (higher losses), which are both undesirable.

It can be seen that previous rules are predominantly based on loss minimisation, and on the requirement that average value can be obtained in each switching period in each leg. Note also that requirements for symmetrical and equal-step PWM sequence, that are necessary for application of the order-per-sector law (Fig. 4.3), are included in the rules.

It will be shown here that it is enough to consider space vectors and their sequences just in the first two sectors and, eventually, in the first sector only. It is interesting to note that all space vectors that are in the first (i.e. α-β) plane shifted by an angle $\alpha=2\pi/5$, have the same switching state but are just circularly shifted, i.e. rotated to the right for one position (rotate to right or RoR operation). That means that switching states in the second sector-pair can be obtained by rotating to the right for one position appropriate switching state records from the first sector-pair. Switching states in the third sector-pair are the same as those in the first after RoR operation for 2 positions, etc. (Fig. 4.6a). Comparing sector-pairs in the α-β plane with sector-pairs in time domain it can be seen that the first sector in time domain is of the same shape as the third and all the odd sectors; also the second sector is of the same shape as the fourth and all the even sectors. Reading from max to min value in the first sector, the order of applied voltages is: v_a, v_b, v_e, v_c, v_d, while in the third sector the order is: v_b, v_c, v_a, v_d, v_e. This means that in the third sector v_a takes position of v_b ($a \rightarrow b$), v_b becomes v_c ($b \rightarrow c$), v_e becomes v_a ($e \rightarrow a$), v_c becomes v_d ($c \rightarrow d$) and v_d is at the position of v_e ($d \rightarrow e$), so that all voltages have rotated to the right



Firing signals for used three-level NPC VSI

	S1	S2
0	0	1
1	0	0
2	1	0

	2	2	1	0	2
S1	1	1	0	0	1
S2	0	0	0	1	0

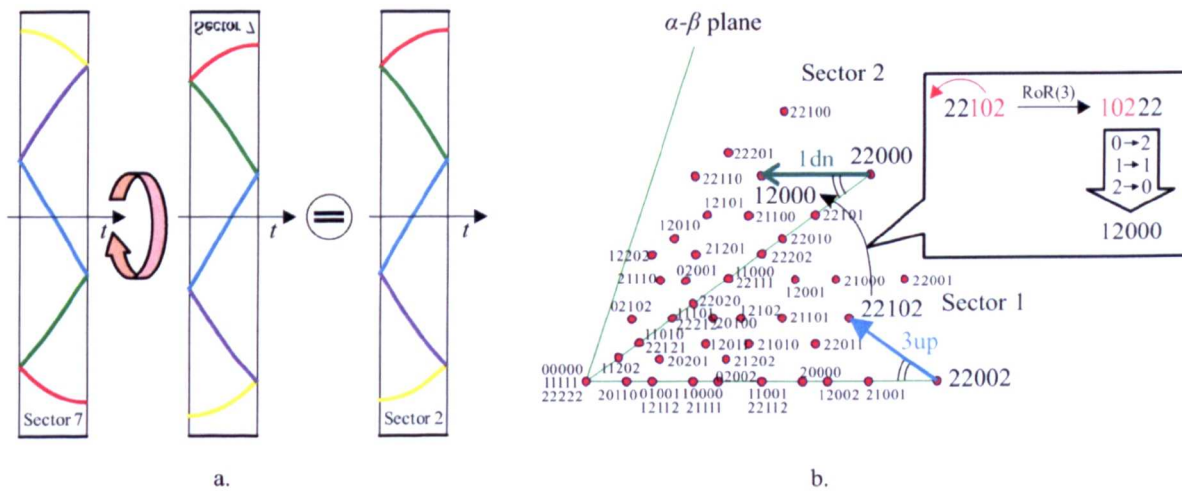
b.

Fig. 4.6: Switching state symmetry in the α-β plane: a. all switching states are determined by RoR operation of one sector-pair. b. Transition from decimal to binary representation for RoR operation in the microprocessors.

their position for one place. The same conclusion applies for the second and the fourth sector. This is a very important conclusion since RoR operation is easy to realise with any microprocessor. At the first sight it appears that there is a problem since non-binary values should be subjected to rotating operation, but every level is defined with appropriate binary gate firing signals (Table 3.2 gives an example for the used three-level NPC VSI). Thus, switching states have to be at first separated into appropriate switching state groups for each gate firing level (Fig. 4.6b), and then subjected to the same RoR operation and set at output simultaneously. It is thus clear that it is enough to analyse only the first sector-pair, while switching states in the other sector-pairs (i^{th} sector-pair) can be easily produced by the explained RoR(i–1) operation.

To prove that it is enough to consider only sequences in the first sector, relation between sequences in the first and the second sector, or, say, between odd and even sectors is needed. This is easier to find starting from the time domain. In Fig. 4.4, the second sector can be obtained after rotation of the seventh sector for 180° around time axis. This is highlighted in Fig. 4.7a. Since the seventh is an odd sector, its switching states can be obtained from the switching states in the first sector, after application of RoR(3) operation. Thus only the influence of rotation for 180° around time axis should be established. Rotation around time axis can be obtained by changing the signs of the applied voltages, or in multilevel digital domain (where all states are denoted with positive numbers, 0, 1, 2...), by changing maximum with minimum value and so on (for a three-level case this means change of 2 with 0, 1 remains 1, and 0 changes to 2). So, it can be said that, in the five-phase case, switching states in even sectors can be found by applying RoR operation three times – RoR(3) to the first sector and swapping each digital output value u_{LEG} with (l–1)–u_{LEG} (Fig. 4.7b). Previous explanation shows how switching states are mapped from the first sector to the second sector, i.e. from the odd to the even sector, and it proves that it is enough to analyse only the first sector. Generalisation of previous analysis can be done, in a simple manner, for any other odd number of phases.

Consider next what happens with switching sequences that have the same position in the odd and in the even sector. Switching sequence that should be applied in even sectors is the same as in odd sectors, but in even sectors the same switching sequence will produce a decrease of the leg levels in the first half-period of the switching period, and an increase in the second (since the signs of appropriate signals in odd and even sectors are opposite: 0 has been changed to 2, 1 to 1, and 2 to 0). Note also that transition takes place in the different leg,



a. b.

Fig. 4.7: Correlation between odd and even sectors: a. in time domain, b. in the α-β plane.

due to RoR(3) operation, as it is shown in Fig. 4.7b (transition 3up becomes 1dn). So switching states in even sectors should be applied in the opposite direction than in the odd sectors to retain symmetry and to minimise the number of switching transitions when change of the sector takes place. Thus it is clear that it is enough to analyse only the first sector and then, from it, to construct switching states in the second sector, and in all the other sectors. It has been clarified how the switching sequences are constructed in the even sectors as well.

Let us assume that the present switching state is $[x_1\ x_2\ x_3\ x_4\ x_5]^T$, and that the first transition happens in the third leg. The next switching state is then $[x_1\ x_2\ x_3{+}1\ x_4\ x_5]^T$. With regard to the transition in the α-β plane, this represents the distance between projections of these two switching state projections (blue '3up' arrow in Fig. 4.7b). Projection into the α-β plane is determined as in (3.30), so the distance between these two vectors (i.e. transition for one level in the third leg) is defined as:

$$\Delta_3 \underline{x}_{\alpha-\beta} = \frac{2}{5}\cdot(x_1 + x_2\cdot e^{j\cdot 1\cdot\alpha} + (x_3+1)\cdot e^{j\cdot 2\cdot\alpha} + x_4\cdot e^{j\cdot 3\cdot\alpha} + x_5\cdot e^{j\cdot 4\cdot\alpha}) - \frac{2}{5}\cdot(x_1 + x_2\cdot e^{j\cdot 1\cdot\alpha} + x_3\cdot e^{j\cdot 2\cdot\alpha} + x_4\cdot e^{j\cdot 3\cdot\alpha} + x_5\cdot e^{j\cdot 4\cdot\alpha}) = \frac{2}{5}\cdot e^{j\cdot 2\cdot\alpha} = \frac{2}{5}\cdot e^{j\cdot(3-1)\cdot\alpha} \tag{4.3}$$

With simple generalisation of (4.3), this means that transition for one level in the k^{th} leg maps into $2/n$ scaled unit vector inclined for $2\pi/n\cdot(k-1)$ radians with respect to the α-axis. For generalisation purposes, note that this inclination angle to α (i.e. x-axis) will be multiplied in other planes by the plane number pl (for 0^+-axis, pl=0; for α-β plane pl=1, for x_1-y_1, pl=2, etc.). The start of the transition vector is in the first switching state projection. If increasing transitions occur in each leg, to form the first half of the switching sequence, this means that the last (the sixth, in the five-phase case) switching state will be $[x_1{+}1\ x_2{+}1\ x_3{+}1\ x_4{+}1\ x_5{+}1]^T$. Applying space vector transformation matrix (3.30) to the last switching state, one gets that it has the same projection as the first (the starting) switching state, in all planes except 0^+-axis. However, difference in the 0^+ axis is not considered in the VSD SVPWM approach.

The first sector of the α-β plane, with reduced number of switching states according to the order-per-sector law, and with all possible transitions, is shown in Fig. 4.8. Transition in each leg is shown in a different colour. Only transitions that increase leg level (up-transitions) are shown. Down-transitions that should be in use

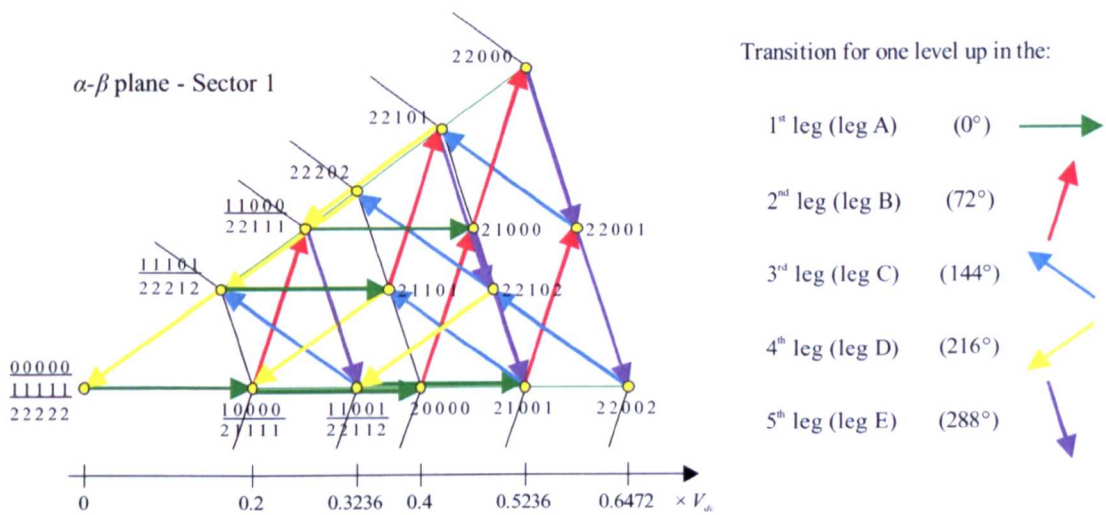


Fig. 4.8: Possible transitions from each switching state in the 1st sector of the α-β plane after order-per-sector law application. Only level-increasing transitions are shown.

in the second-half of the switching sequence have the opposite direction. Graphically, construction of a switching sequence means that one has to find all closed (the first and the last switching states correspond to the same projection) five-angle patterns that contain all five different colours (transition for one level appears in each leg). Since the first and the last switching state correspond to the same space vector, this means that potential starting space vector has to have redundancy. Next, the starting switching sequence must not contain the highest level (in a three-level VSI this is 2), since an increase by one level in that leg would lead to leg level 3, which is not possible. Finally, potential starting switching states of switching sequences are shown underlined in Fig. 4.8.

There are 16 closed patterns, as shown in Fig. 4.9. However, switching sequences are not yet completely determined at this stage, since some of the patterns contain more potential beginnings of the switching sequence and also some of the patterns cannot provide cancellation (i.e. zeroing of the average voltage) in the x_1-y_1 plane.

Consider first switching sequence redundancy per pattern. For the sake of clarity, only underlined starting switching states from Fig. 4.8 are shown in Fig. 4.9. Projections of space vectors of those states are denoted with 'o' – potential start of the sequence. Multiple 'o' represents more potential starting switching states. For example, the first (A) pattern contains six underlined ('o'-signed) switching states, so corresponding switching sequences that start with those states are: 00000-10000-11000-11001-11101-11111; 10000-11000-11001-11101-11111-21111; 11000-11001-11101-11111-21111-22111; 11001-11101-11111-21111-22111-22112; 11101-11111-21111-22111-22112-22212; 11111-21111-22111-22112-22212-22222 (only the first, i.e. increasing, halves of the sequences are shown). Next, B pattern can be obtained by starting the sequence from four 'o' denoted switching states (that do not contain 2), and so on. The number of switching sequences that correspond to each pattern is also shown in Fig. 4.9 (e.g. ×6 for A pattern). Summing all of them, one gets that there are 32

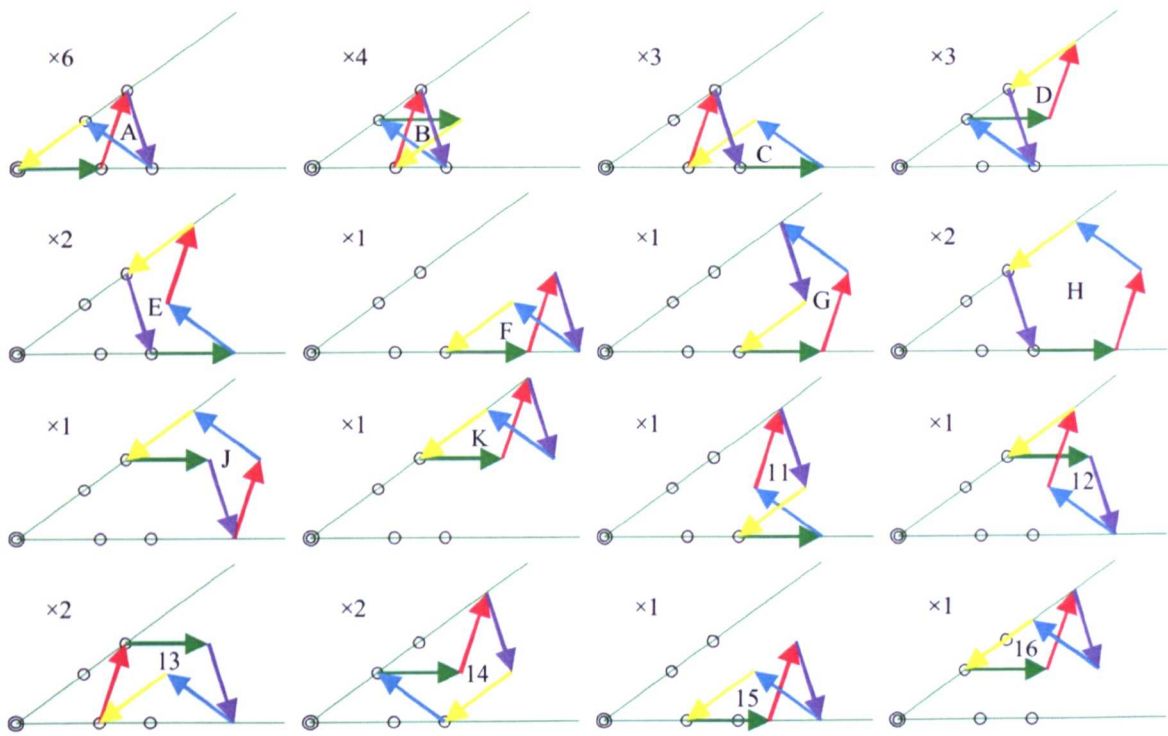


Fig. 4.9: All possible 16 patterns in the 1st sector of the α-β plane (five-phase three-level VSI). Symbol 'o' represents potential start of the switching sequences (the number of 'o'-s is shown after × sign).

possible switching sequences. It should be emphasised again that corresponding switching sequences in other sectors can be determined with RoR and sign changing operations, and taking vectors in the opposite direction for even sectors, as it has been explained previously.

Positions of 'o'-s potential sequence starts, in Fig. 4.9, are the same as positions of medium and large space vectors for two-level inverters with $0.5 \cdot V_{dc}$. For more levels, starts of switching sequences will be determined with switching states that do not contain maximum level and satisfy order-per-sector law, so the positions are determined with positions of the appropriate switching states of l–1 level case with $(l-2)/(l-1) \cdot V_{dc}$ scaled voltage.

When sequences are determined (there are 32 possible switching sequences), the next step in [Gao and Fletcher (2010)] algorithm is to eliminate those sequences whose space vector projections cannot be cancelled in the x_1-y_1 plane by adjusting their application times. Mapping of all switching states from the first sector of the α-β plane into the x_1-y_1 plane, with the possible one-level increasing transitions, is shown in Fig. 4.10. It can be seen that in this plane angles of vector transitions are doubled, since the angle in the transformation is doubled and parameter pl=2, as it was explained in conjunction with (4.3). The length of vector transitions is of course the same, 2/5 times the unit vector, since regarded leg transitions are for one level.

The mapping of the patterns from the α-β plane of Fig. 4.9 into the x_1-y_1 plane is shown in Fig. 4.11. It can be seen that patterns denoted with numbers 11 to 16 are located in such a way that these patterns cannot provide voltage cancelation in this plane. That means that the number of possible switching patterns is reduced to 10, denoted with letters A to K in Fig. 4.9 and Fig. 4.11 (letter 'I' is not used). Switching sequences that correspond to patterns A-K (24 of them) are shown in Table 4.2, while those eight that correspond to patterns 11 to 16 are omitted.

Up to this point, patterns of interest are determined and corresponding redundant switching sequences are identified. Projections of chosen space vectors, i.e. pattern, determine dwell times of the switching states, and this will be analysed in the following sub-section. Determination of the final switching sequence will be elaborated in the sub-section 4.2.5.

4.2.4 DWELL TIME CALCULATION AND SECTOR PARTITIONING

As it was explained in 3.4.2, for the process of dwell time calculation only projections of space vectors into planes are important. For this purpose, general equation for dwell time calculation (3.51) is adapted to the five-phase system:

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \end{bmatrix} = \begin{bmatrix} v_{\alpha,1} & v_{\alpha,2} & v_{\alpha,3} & v_{\alpha,4} & v_{\alpha,5} \\ v_{\beta,1} & v_{\beta,2} & v_{\beta,3} & v_{\beta,4} & v_{\beta,5} \\ v_{x_1,1} & v_{x_1,2} & v_{x_1,3} & v_{x_1,4} & v_{x_1,5} \\ v_{y_1,1} & v_{y_1,2} & v_{y_1,3} & v_{y_1,4} & v_{y_1,5} \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ v_{x_1}^* \\ v_{y_1}^* \\ 1 \end{bmatrix} \cdot T_s \tag{4.4}$$

where T_i (i=1, 2, ..., 5) stands for time of application of the appropriate space vector in the pattern – dwell time, while $v_{p,i}$ represents the i^{th} space vector projection on the p-axis (α, β, x_1, y_1). As desired reference signals are pure sine waves without any higher harmonics, that means that reference projections on the α and β axes are $V^* \cdot \cos(\theta)$ and $V^* \cdot \sin(\theta)$, respectively (see (3.46)), while projections on x_1 and y_1 axes are zero. Substituting these values into (4.4), one gets:

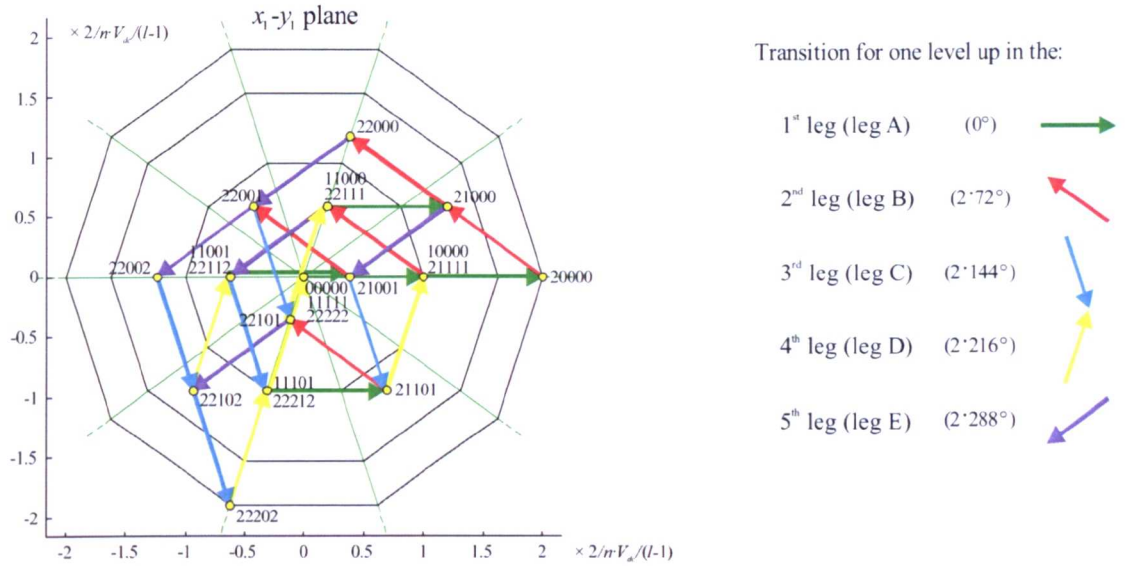


Fig. 4.10: Mapping of chosen switching states from the 1st sector of the α-β plane into x_1-y_1 plane with possible transitions (only level-increasing vector transitions are shown).

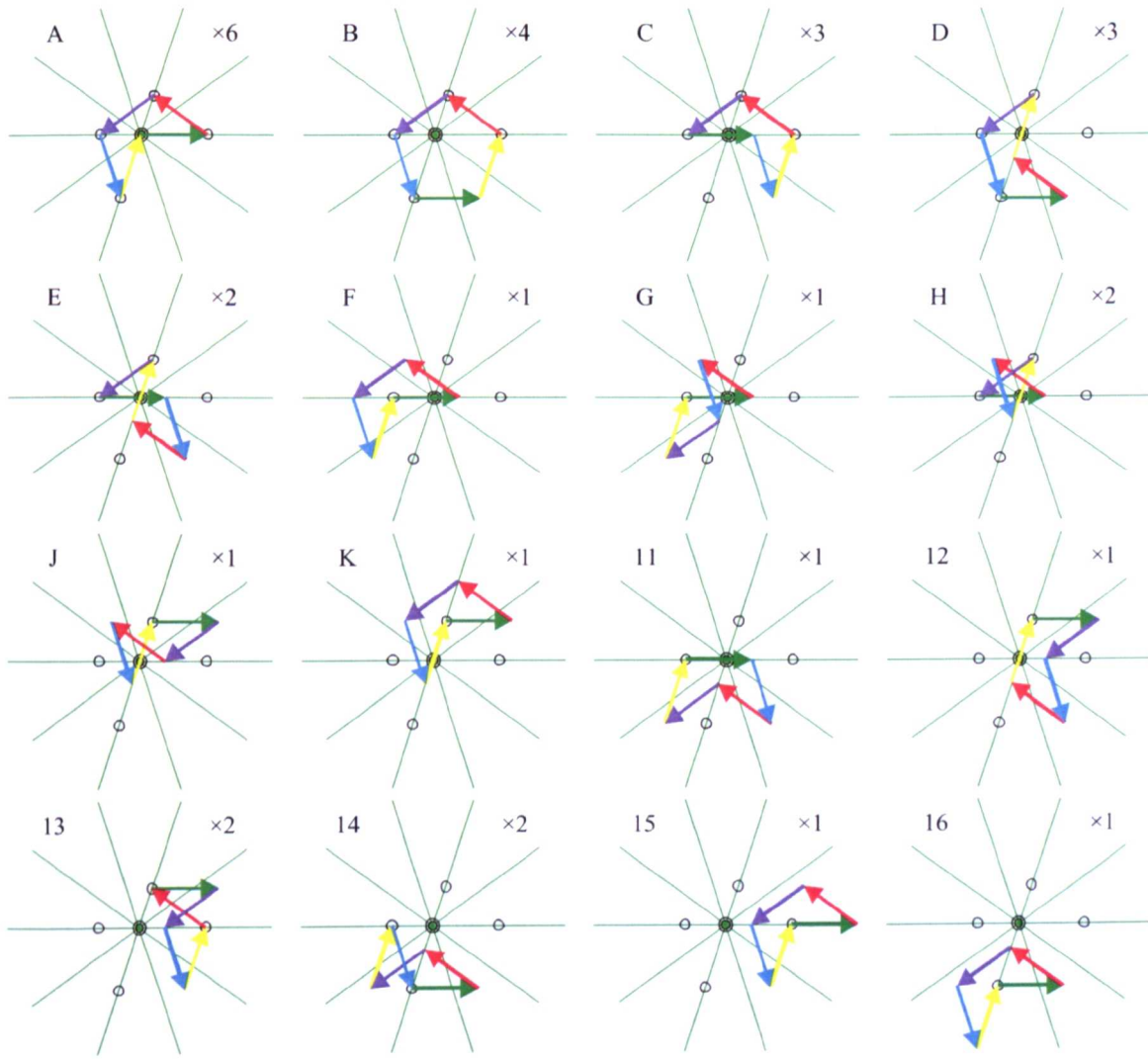


Fig. 4.11: Mapping of all possible patterns from Fig. 4.9 into the x_1-y_1 plane. Symbol 'o' represents potential start of the switching sequences (the number of 'o'-s is shown after × sign).

Table 4.2: Switching sequences in the 1st sector that can provide zero average voltage in the x_1-y_1 plane.

Sub-sector	Possible sequences in the 1st sector		No.of 1s
	One level increasing half	One level decreasing half	
A1	00000-10000-11000-11001-11101-**11111**-11101-11001-11000-10000-00000		25
	10000-11000-11001-11101-11111-**21111**-11111-11101-11001-11000-10000		34
	11000-11001-11101-11111-21111-**22111**-21111-11111-11101-11001-11000		39
	*11001-11101-11111-21111-22111-**22112**-22111-21111-11111-11101-11001		**40**
	11101-11111-21111-22111-22112-**22212**-22112-22111-21111-11111-11101		37
	11111-21111-22111-22112-22212-**22222**-22212-22112-22111-21111-11111		30
B1	10000-11000-11001-11101-21101-**21111**-21101-11101-11001-11000-10000		30
	11000-11001-11101-21101-21111-**22111**-21111-21101-11101-11001-11000		35
	*11001-11101-21101-21111-22111-**22112**-22111-21111-21101-11101-11001		**36**
	11101-21101-21111-22111-22112-**22212**-22112-22111-21111-21101-11101		33
C1	10000-11000-11001-21001-21101-**21111**-21101-21001-11001-11000-10000		26
	11000-11001-21001-21101-21111-**22111**-21111-21101-21001-11001-11000		31
	*11001-21001-21101-21111-22111-**22112**-22111-21111-21101-21001-11001		**32**
D1	11000-11001-11101-21101-22101-**22111**-22101-21101-11101-11001-11000		31
	*11001-11101-21101-22101-22111-**22112**-22111-22101-21101-11101-11001		**32**
	11101-21101-22101-22111-22112-**22212**-22112-22111-22101-21101-11101		29
E1	11000-11001-21001-21101-22101-**22111**-22101-21101-21001-11001-11000		27
	*11001-21001-21101-22101-22111-**22112**-22111-22101-21101-21001-11001		**28**
F1	*11001-21001-22001-22002-22102-**22112**-22102-22002-22001-21001-11001		**16**
G1	*11001-21001-22001-22101-22102-**22112**-22101-22101-22001-21001-11001		**20**
H1	11000-11001-21001-22001-22101-**22111**-22101-22001-21001-11001-11000		23
	*11001-21001-22001-22101-22111-**22112**-22111-22101-22001-21001-11001		**24**
J1	*11000-21000-21001-22001-22101-**22111**-22101-22001-21001-21000-11000		**19**
K1	*11000-21000-22000-22001-22101-**22111**-22101-22001-22000-21000-11000		**15**

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \end{bmatrix} = \begin{bmatrix} v_{\alpha,1} & v_{\alpha,2} & v_{\alpha,3} & v_{\alpha,4} & v_{\alpha,5} \\ v_{\beta,1} & v_{\beta,2} & v_{\beta,3} & v_{\beta,4} & v_{\beta,5} \\ v_{x_1,1} & v_{x_1,2} & v_{x_1,3} & v_{x_1,4} & v_{x_1,5} \\ v_{y_1,1} & v_{y_1,2} & v_{y_1,3} & v_{y_1,4} & v_{y_1,5} \\ 1 & 1 & 1 & 1 & 1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} V^* \cdot \cos(\theta) \\ V^* \cdot \sin(\theta) \\ 0 \\ 0 \\ 1 \end{bmatrix} \cdot T_s \tag{4.5}$$

where $\theta=\omega t$, stands for the reference angle, and V^* represents amplitude of the reference phase voltages.

Sub-sectors, that determine region of applicability of the chosen patterns, can now be determined. Partitioning of the sector into sub-sectors can be easily determined with the simple constraint that times of applications, which result as the solution of (4.5), must be in the range from 0 to T_s [Gao and Fletcher (2010)]. This constraint, combined with the reference plotting in the α-β plane ($\underline{v}^*_{\alpha\text{-}\beta}= V^* e^{j\theta}$, i.e. $v^*_\alpha= V^* \cdot \cos(\theta)$, $v^*_\beta= V^* \cdot \sin(\theta)$), yields the sub-sector for application of the chosen space vectors. This part is somewhat complicated for analytical calculation but is still straightforward if a computer is used. The problem is solved with Matlab programme, which solves equation (4.5) for each switching pattern, increasing in incremental steps the values of the reference angle θ and magnitude V^*, covering the whole α-β plane. If a solution exists for a temporary pair of V^* and θ, and if all dwell times are in the range 0 to T_s, the programme plots a dot on a certain position, $V^* e^{j\theta}$ in the α-β plane. This means that the current pair of V^* and θ (plotted dot) belongs to the region of applicability for the selected pattern. All pairs of V^* and θ (all plotted dots) represent the region of application of the selected pattern. As an example of the output of this code, Fig. 4.12 shows the area that is covered by the pattern C of Fig. 4.9. Regions of applicability for other patterns in sector 1 are determined in the same way, and

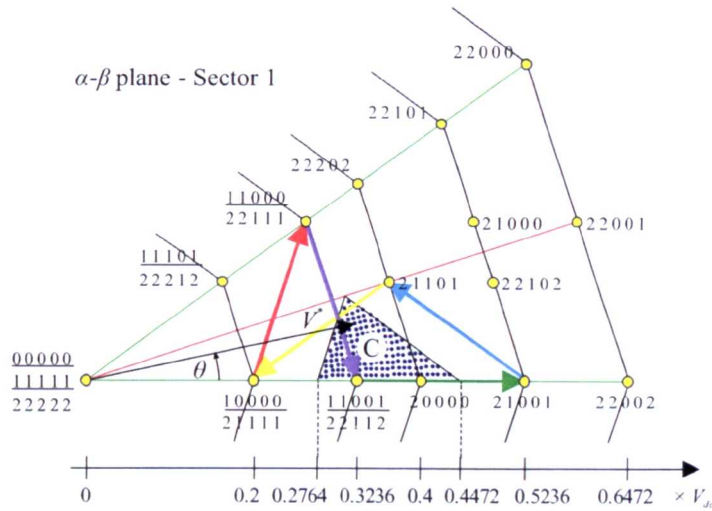


Fig. 4.12: Plot from the Matlab code: region of applicability for pattern C from Fig. 4.9.

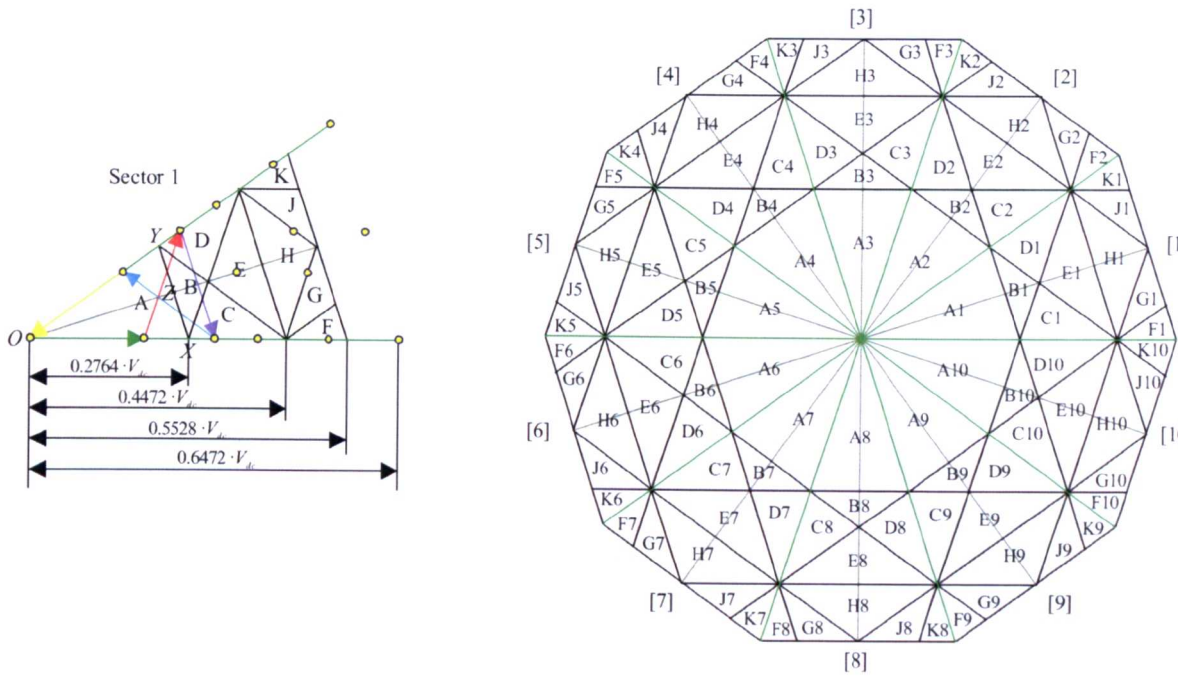
are shown in Fig. 4.13a. Position of sub-sectors in other sectors is shown in Fig. 4.13b. It should be noted that borders of sub-sectors are not the same as the borders of corresponding patterns. This is clear from Fig. 4.12, and is also shown for pattern A in Fig. 4.13a.

Values of specific limits are given numerically, since they are determined using Matlab code; however, analytical values for the sub-sector borders are desirable. One can see that the borders between sub-sectors are straight lines and they form angles of $1\cdot\pi/5$, $2\cdot\pi/5$, ..., $5\cdot\pi/5$ with the α-axis. The border of the sub-sector A in Fig. 4.13a could be obtained analytically by solving (4.5). (which looks too complicated), or by using the fact that this sub-sector is determined by the pattern to which the switching sequence corresponds: 00000-10000-11000-11001-11101-11111, which is one of six redundant switching sequences for this pattern (Fig. 4.9). This sequence is specific since it contains only zeros and ones. This means that it is obtainable by an equivalent two-level inverter (with halved dc-bus value). Thus, one can say that the line *XY* represents the border between two-level and three-level operation of the inverter. The length of line *OZ* is one-half of the value of the maximum modulation index for the two-level five-phase inverter ($m_{\max 5,2}$), since the value of the dc-bus voltage of the equivalent inverter is halved. If the modulation index m is defined as the ratio of the fundamental peak of the phase voltage over the $V_{dc}/2$, as in (3.21), then, using analytical value for $m_{\max 5,2}$ [Levi et al. (2008)], one gets that the length of *OZ* is given with:

$$OZ = \frac{1}{2}\cdot m_{\max 5,2}\cdot\frac{V_{dc}}{2} = \frac{V_{dc}}{4}\cdot\frac{1}{\cos(\pi/10)} \tag{4.6}$$

Since all angles are known, analytical values for all the other lengths in Fig. 4.13a can be determined using (4.6) and some geometry. For example, three characteristic values, given in Fig. 4.13a, can be calculated as:

$$\begin{aligned} 0.2764\cdot V_{dc} &= \frac{OZ}{\cos(\pi/10)} \\ 0.4472\cdot V_{dc} &= 2\cdot\frac{OZ}{\cos(\pi/10)}\cdot\cos(\pi/5) \\ 0.5528\cdot V_{dc} &= \frac{m_{\max 5,2}\cdot V_{dc}/2}{\cos(\pi/10)} = \frac{2\cdot OZ}{\cos(\pi/10)} \end{aligned} \tag{4.7}$$



a. b.

Fig. 4.13: Regions of applicability for appropriate patterns: a. for the first sector and b. for all 10 sectors in α-β plane, defining sub-sectors A-K.

Times of vector applications in each sub-sector are determined by (4.5). However, this does not give information about sub-division of those times, for the first and the second half. In accordance with Fig. 4.3a, assumed sub-division of time for all eleven switching states that constitute switching sequence is: $T_1/4$, $T_2/2$, $T_3/2$, $T_4/2$, $T_5/2$, $T_1/2$, $T_5/2$, $T_4/2$, $T_3/2$, $T_2/2$, $T_1/4$.

4.2.5 SWITCHING SEQUENCE OPTIMISATION

The next step in the algorithm [Gao and Fletcher (2010)] is choosing of the switching sequences for each of the remaining 10 (A-K) switching patterns, since each pattern can be realised with more than one sequence. The principles that should be used for this process are:

1) A minimum number of transitions between sub-sectors is desirable for minimum switching losses.
2) For capacitor voltage balancing purposes (three-level NPC VSI topology), sequences that contain more 'ones' are preferable since in that case output is defined by the capacitor dc voltage mid-point [Gao and Fletcher (2010)].

The first rule is a basic optimisation criterion. According to it, it is desirable that all sub-sector sequences have the same starting switching state, if possible, to avoid additional switching when reference changes sub-sector, i.e. sector. Unfortunately, it can be seen that unique sequences F, G and J, K start with different switching states, 11001 and 11000, respectively (Table 4.2). However, all other sub-sector sequences can start with both switching states (either 11001 or 11000). In conjunction with the second rule, the number of ones is counted, and is shown in the last column of Table 4.2, for each sequence. Preferable sequences according to this rule (sequences with maximum number of ones), are denoted with bold number of ones in this column. It can be seen that two requirements coincide for all sequences A-H if the chosen start is 11001, and additional switching appears when reference enters sub-sectors J and K. In this way, the optimised switching sequences are determined for the first sector and they are denoted with '*' in Table 4.2.

Table 4.3: The first half of the chosen switching sequence in the 2nd sector.

Sub-sector	Chosen sequences for the 2nd sector
A2	11000-11100-11101-11111-12111-22111
B2	11000-11100-11101-12101-12111-22111
C2	11000-11100-11101-12101-22101-22111
D2	11000-11100-12100-12101-12111-22111
E2	11000-11100-12100-12101-22101-22111
F2	11000-12000-22000-22100-22101-22111
G2	11000-12000-12100-22100-22101-22111
H2	11000-11100-12100-22100-22101-22111
J2	11100-12100-22100-22101-22201-22211
K2	11100-12100-22100-22200-22201-22211

Switching sequences that should be applied in the second sector are given in Table 4.3. Shown sequences correspond to those chosen in the first sector (denoted with '*' in Table 4.2). Only increasing-level half of sequences is shown. These sequences are obtained from their counterparts from the first sector after applying RoR operation for three positions to each switching state, replacing 0, 1 and 2 with 2, 1 and 0, respectively, and finally changing direction of the switching state application. Table 4.2 and Table 4.3 give switching sequences for the first sector-pair and switching sequences for all the other sector-pairs can be directly determined by RoR operation, as already explained in 4.2.3.

In the chosen switching sequence solution, five extra switching transitions, one for one level up and one for one level down in each phase, appear during one period of the sinusoidal reference signal (during passing through all 10 sectors). These extra transitions appear regardless of the modulation index value. The positions of the extra switchings are shown in Fig. 4.14. Switching state in each partition of the new partitioning scheme presents the start, i.e. the first and the last switching state (because of symmetry), in each region inside new partition lines.

4.2.6 DETERMINATION OF THE SUB-SECTORS

As there are 10 sub-sectors in the first sector, leading to the total of 100 sub-sectors in the α–β plane, the

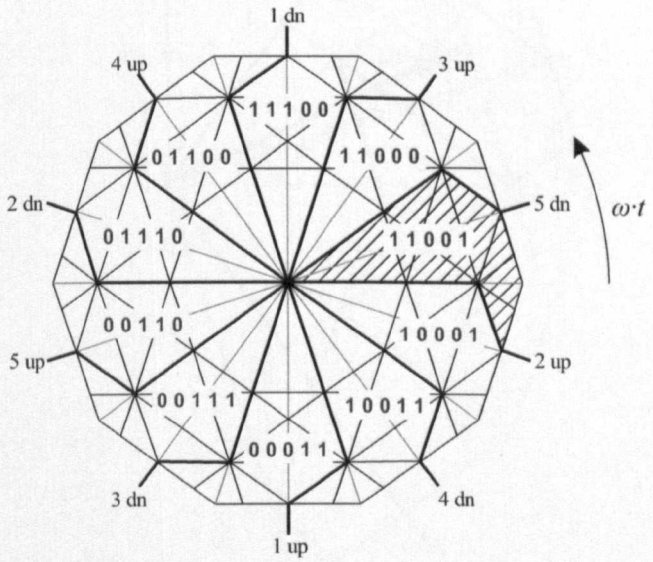


Fig. 4.14: Transitions when extra switchings appear for the original space vector algorithm. Denoted up and down changes represent increase or decrease of appropriate leg output level for one step.

change of the sub-sector is frequent and an efficient way of sub-sector determination has to be used. One graphical method for determination of the sub-sectors was presented in [Gao and Fletcher (2010)]. Process of determination in which sub-sector of the first sector the reference voltage is, is shown in Fig. 4.15. As already mentioned, all borders between sub-sectors can be divided into five groups, forming angles of $1\cdot\pi/5$, $2\cdot\pi/5$, ..., $5\cdot\pi/5$ with the α-axis. Each group contains only border-lines that are in parallel. In Fig. 4.15, borders belonging to the same group are shown in the same colour. Axes orthogonal to these borders are denoted with x_5, x_4, ..., x_1, respectively (see Fig. 4.15; use of symbol x here is not related to the x-y planes). For sub-sector determination, it is enough to find the projections of the reference vector $\underline{v}^*_{\alpha\text{-}\beta}$ to the defined axes x_1 to x_5 (V_{ref1} to V_{ref5}) and to compare the position of these projections with the position of projections of the borders L_{11}, L_{21}, L_{22},..., L_{51}. For example, if the reference is in the sub-sector E1, as it is shown in Fig. 4.15, this means that the reference is located down-left from the border with sub-sector H1, i.e., the reference projection to the x_3-axis $V_{ref3}\leq L_{32}$; the reference must be located down-right from the border with sub-sector D1, i.e., $V_{ref4}>L_{41}$; and considering the border with sub-sector C1, the reference must be located up-right, $V_{ref2}>L_{21}$. Rules for the determination of all 10 sub-sectors inside the first sector ($0\leq\omega t<2\pi/10$) are summarised in Table 4.4. Values of projections of the reference vector onto axes x_1 to x_5 (V_{ref1} to V_{ref5}) are also included in the table. Choice of the sign $<$, $>$, $\leq$ or $\geq$ in Table 4.4 has been done precisely, so that any point belongs only to one sub-sector.

Note that, considering the length from the origin to the intersecting point, one has $L_{11}=L_{21}=L_{31}=L_{41}=L_{51}$, $L_{22}=L_{32}=L_{42}$, and these will be denoted further with L_1 and L_2, respectively, while L_{33} will be denoted as L_3. Analytical value of L_1 is already given by (4.6), L_2 can be directly obtained from L_1 using simple geometry,

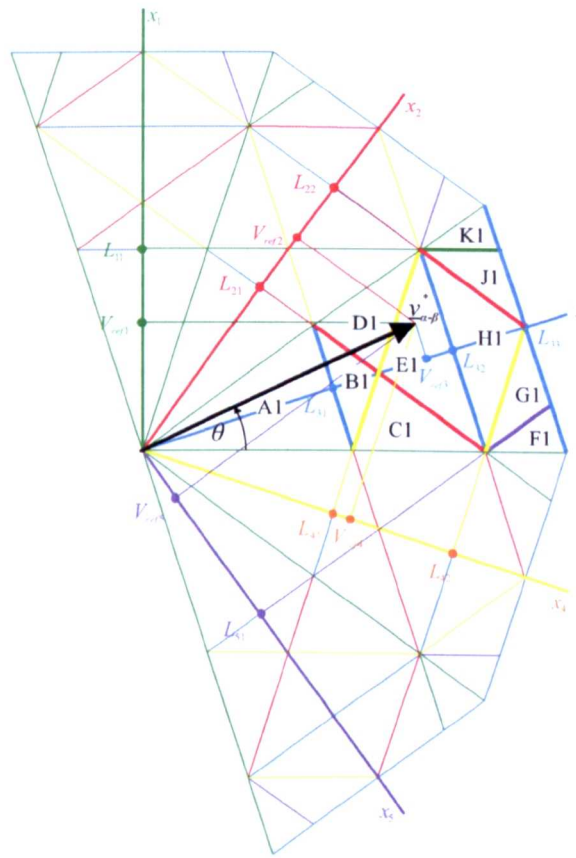


Fig. 4.15: Geometrical explanation of sub-sector determination in the five-phase three-level case.

while L_3 corresponds to the maximum modulation index for a five-phase VSI [Levi et al. (2008)] ($L_3=2\cdot L_1$):

$$L_1 = \frac{V_{dc}}{4\cdot\cos(\pi/10)} = 0.2629\cdot V_{dc}$$
$$L_2 = \frac{V_{dc}}{4\cdot\cos(3\pi/10)} = 0.4253\cdot V_{dc} \tag{4.8}$$
$$L_3 = \frac{V_{dc}}{2\cdot\cos(\pi/10)} = 0.5257\cdot V_{dc}$$

So far the rules for sub-sector determination are defined just for the first sector ($0\leq\theta<2\pi/10$); with shifting down reference signal position (shifting back reference angle $\theta=\text{mod}(\theta, 2\pi/10)$) to the first sector, the procedure will be applicable to all other sectors. It can be seen that the whole process requires some geometry, but once when the rules are established, it reduces to the comparison with constant values.

Implementation of the algorithm is rather simple. To avoid online operations for construction of the even sequences from the odd sequences, it is easier to consider sector-pairs instead of sectors. Data for the first two sectors must be stored in memory, so reduction of the complexity is at the expense of the used memory. Note that the inverted matrix in (4.5) can be calculated in advance for each of the switching sequences (from the first two sectors) and also stored in memory. This is very important since complex operation of matrix inversion will be avoided in this way. So, data for the sequences (Table 4.2 and Table 4.3), and for the application times calculation (pre-calculated inverted matrix from (4.5)), should be stored in memory. Simple logic from Table 4.4 determines the sub-sector, and data for the switching sequence and for the dwell time calculation for that sub-sector are loaded from the memory. Switching sequences in other sector-pairs are determined by RoR operation that is simple.

4.2.7 MODIFICATION OF THE PROPOSED ALGORITHM

The basic idea of the modification is to reduce variations of the common mode voltage. The symmetry around the eighteen degree line in the first sector is utilised to introduce an additional sub-division of each sector into two halves and reorganise the switching sequences accordingly. Namely, in the first sector, which occupies the first 36° of the reference signal period in the five-phase case, the fifth phase reference voltage v_e^* is crossing

zero, and is positive in the first 18° and negative between 18° and 36° (Fig. 4.4). The proposed switching sequence, taking as the example small values of the modulation index (m<0.5257, i.e. V^*<0.2628·V_{dc}) when the reference is in the sub-sector A (Fig. 4.13), contains at the fifth positions only ones and twos (sequence A1*, Table 4.2, underlined values). That means that the fifth leg voltage is boosted, i.e. that CMV is always greater than one (i.e., V_{dc}/2) in the first sector (CMV is referred to the negative dc bus rail). Further, in the second sector the third phase v_c^* changes sign from the negative to the positive (Fig. 4.4). The algorithm gives only zeros and ones in the appropriate sequence for the third leg (sequence A2, Table 4.3, underlined values), so CMV is less than one (i.e., V_{dc}/2). The same happens for higher values of the modulation index, but more sub-sectors are involved. With the proposed sub-division of the sectors into two equal parts, and developing independent switching sequence for each part, it is possible to obtain average value of the CMV equal to one (i.e., V_{dc}/2) during the time interval which corresponds to the whole sector (36°). The maximum value of the CMV voltage alternating part is reduced in this way.

After modification, original sub-sectors A, B, E and H (Fig. 4.13) are additionally divided into lower and upper parts (Fig. 4.16). This produces four additional sub-sectors, so the total number of sub-sectors per sector in the modified algorithm is 14. Switching sequences for the upper sub-sectors are different than in the original algorithm, while they remain the same for the lower parts of the four sub-sectors that have undergone further sub-division. The first to the fifth switching states of the lower sub-sector sequence become the second to the sixth switching states of the upper sequence, while the first is the redundant switching state that corresponds to the same space vector as the sixth. Also, the same rule must be applied to the original sequence of sub-sector D. Switching sequences for corresponding 14 sub-sectors are given in Table 4.5. Note that upper and lower sequences (e.g. A_{up} and A_{dn}) are redundant switching sequences and correspond to the same pattern. In this way all switching sequences in the lower and in the upper half of the sector will have the same starting switching state (11001 and 11000, respectively). The starting switching state in the lower half of the second sector is 11000, so that the number of extra switchings (and also total switchings) remains the same as before modification, but the line when they appear is now a straight line at 18°, i.e. at mid-point of the sector. Traces when extra switchings in the modified algorithm appear, for any value of the modulation index, are shown in Fig. 4.17 (to be compared with Fig. 4.14). Also, the capacitor voltage balancing is not affected since the total number of 'ones' remains the same for each value of the modulation index.

The increase of the number of sub-sectors from 10 to 14 within the original 36° sectors slightly increases the complexity of the algorithm. For example, an additional condition for angle position is necessary for sub-sector determination. If $0 \leq \theta < \pi/10$, then lower sequences are in use, and if $\pi/10 \leq \theta < 2\pi/10$, then upper sequences

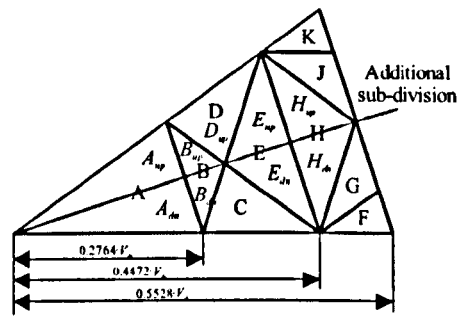


Fig. 4.16: The first sector sub-sectors after additional sub-division.

Table 4.5: Switching sequences for sub-sectors of Fig. 4.16.

Sub-sector	Sequence
A = A_{dn}	11001-11101-11111-21111-22111-22112
B = B_{dn}	11001-11101-21101-21111-22111-22112
C	11001-21001-21101-21111-22111-22112
D ($\neq D_{up}$)	11001-11101-21101-22101-22111-22112
E = E_{dn}	11001-21001-21101-22101-22111-22112
F	11001-21001-22001-22002-22102-22112
G	11001-21001-22001-22101-22102-22112
H = H_{dn}	11001-21001-22001-22101-22111-22112
J	11000-21000-21001-22001-22101-22111
K	11000-21000-22000-22001-22101-22111
A_{up}	11000-11001-11101-11111-21111-22111
B_{up}	11000-11001-11101-21101-21111-22111
D_{up}	11000-11001-11101-21101-22101-22111
E_{up}	11000-11001-21001-21101-22101-22111
H_{up}	11000-11001-21001-22001-22101-22111

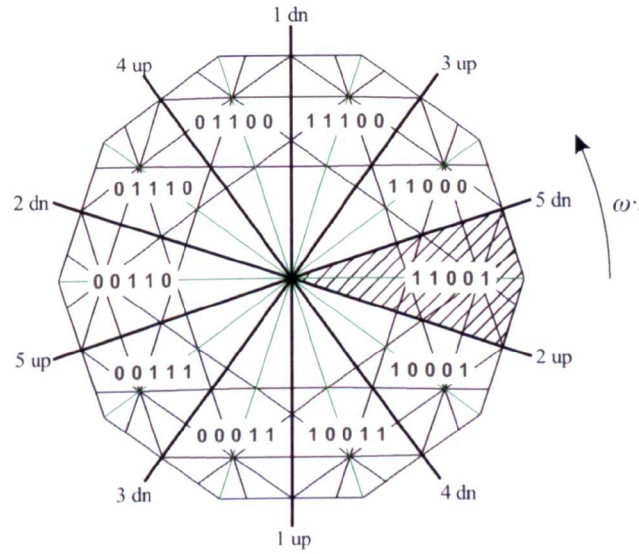


Fig. 4.17: Transitions when extra switchings appear for modified space vector algorithm. Denoted up and down changes represent increase or decrease of appropriate leg output level for one step.

should be applied. Also, required memory storage for the data for 14 sub-sectors, instead of 10, becomes 40% higher.

4.2.8 SIMULATION AND EXPERIMENTAL RESULTS

In this sub-section, selected simulation and experimental results for the original and modified SVPWM algorithm, for the five-phase three-level case described in this section, are given. The accompanying analysis is related to the comparison of simulations and experiments, and to confirmation of the proper functioning of the modulation methods. Detailed mutual comparison of these results, as well as the comparison with the other modulation strategies, is postponed for Chapter 6.

Using previously described steps, models for the described original and modified algorithms have been developed in Matlab/Simulink while the circuit part was obtained using PLECS block-set package. Although the algorithm steps of sub-sector and switching sequence determination are quite tedious, the final model is very simple, and developed modulator in Simulink directly follows the general structure, given in section 4.4, where

generalisation of the VSD space vector algorithm is presented. In used realisations memory usage is deliberately sacrificed to reduce calculation burden, so data not only for the first sector, but for the second sector as well, are stored in the memory. Thus, for the original algorithm the model contains set of 2×10 sequences per sector from Table 4.2 and Table 4.3 and 2×10 corresponding, pre-calculated, inverted matrices for switching state application times from (4.5). For the modified algorithm there are 14 sub-sectors per sector, and values from Table 4.5 are used for the first sector. Data for the second sector are calculated from the sequences for the first sector in the same way as for the original algorithm in sub-section 4.2.5 (application of RoR(3) to each switching state, replacing 0, 1 and 2 with 2, 1 and 0 respectively, and changing direction of the switching state application). Pre-calculated inverted matrices for switching state application times from (4.5) for each sequence are also stored as constants. Determination of the sub-sector, i.e. selection which pair of stored sequences and inverted matrices will be used, is defined by the current reference magnitude and angle, according to Table 4.4 for the original algorithm, while for the modified algorithm additional condition whether $\theta<\pi/10$ was also checked.

Parameters of the inverter in the simulation were set to the following values: dc-bus voltage V_{dc}=600V, switching frequency f_s=2kHz, and inverter dead time 6μs. Modulation signal frequency was varied according to the V/f=constant law (m/f=1/50). Only linear PWM region is analysed, and the maximum modulation index is 1.0515. NPC inverter was modelled using IGBT switches with zero forward voltage, and with on-resistance of 10mΩ. Flywheel diodes and clamping diodes are modelled using only on-state resistance of 10mΩ. Five-phase induction machine has two pole pairs and is modelled using the following estimated parameters: R_s=3Ω, L_{ls}=45mH, R_r'=3Ω, L_{lr}'=15mH, L_m=515mH, J=0.1kg·m^2. The same parameters were used also for the other modulation techniques for the five-phase case that will be discussed later. The values in simulations were adjusted to match the corresponding values used in experiments. The algorithm in the experiments was executed on the dSpace ds1006 real-time processor. Used three-level NPC inverter is custom-built and can be used for up to six output phases. Dead time is implemented by the hardware and is around 6μs. For dc-bus supply, an external dc source Sorensen SGI 600/25 has been employed, and the dc-bus voltage value has been set to V_{dc}=600V. Simulation and experimental parameters, with detailed explanations, including figures of the setup, are given in the Appendix A.

Original algorithm

Simulation and experimental results, for modulation indices 0.4 and 1, for the original algorithm are shown side by side in Fig. 4.18 and Fig. 4.19, respectively. This algorithm will be denoted as SVPWM1. Waveforms and spectra are shown for the inverter leg voltage, output phase voltage, CMV (note that CMV is referenced to the negative rail of the dc bus, hence the dc component) and phase current. For processing the data from the oscilloscope, Matlab script that searches for the sample when the phase of the leg voltage fundamental is zero (starts as cosine) and shows one period starting from that point, was used. In this way an easy comparison of the simulation and experimental results is provided. This program was used for processing of all the data in this thesis. Some screenshots from the oscilloscope for modulation indices of 0.4, 0.6, 0.8 and 1 are shown in Fig. 4.20.

From Fig. 4.18 and Fig. 4.19 one can see that simulation and experimental results are in a very good agreement. Required fundamental output voltage is achieved without any low-order voltage harmonics in the phase voltage. Slightly lower voltage values in the experimental results can be explained by the non-modelled voltage drops on the switching components. For the chosen low modulation index of 0.4 in Fig. 4.18, reference

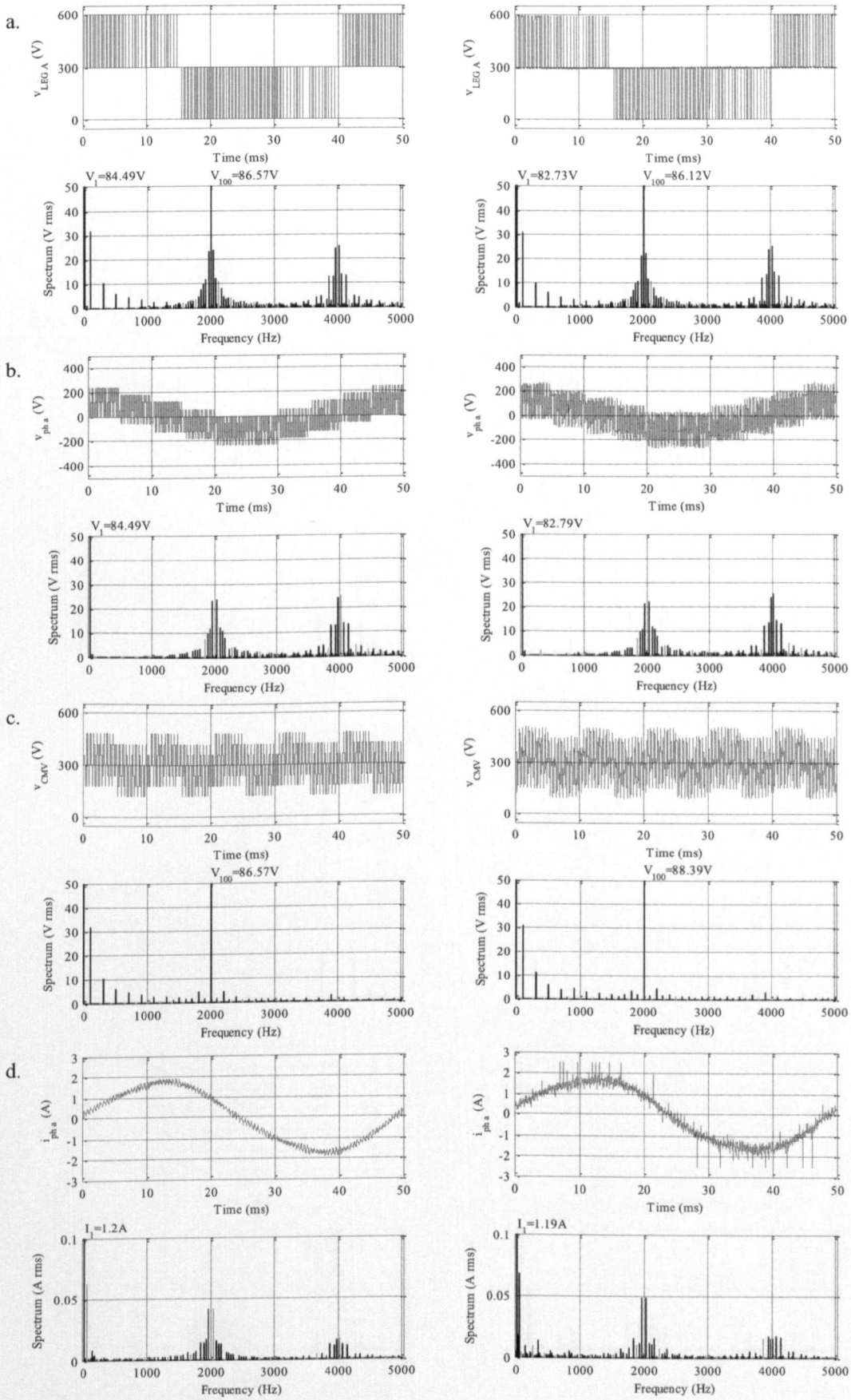


Fig. 4.18: Simulation (left column) and experimental (right column) results for the original five-phase three-level SVPWM method. a. Leg *A* voltage, b. phase *a* voltage, c. CMV, d. phase *a* current, with associated spectra. Results are for the modulation index m=0.4 (SVPWM1, n=5, l=3).

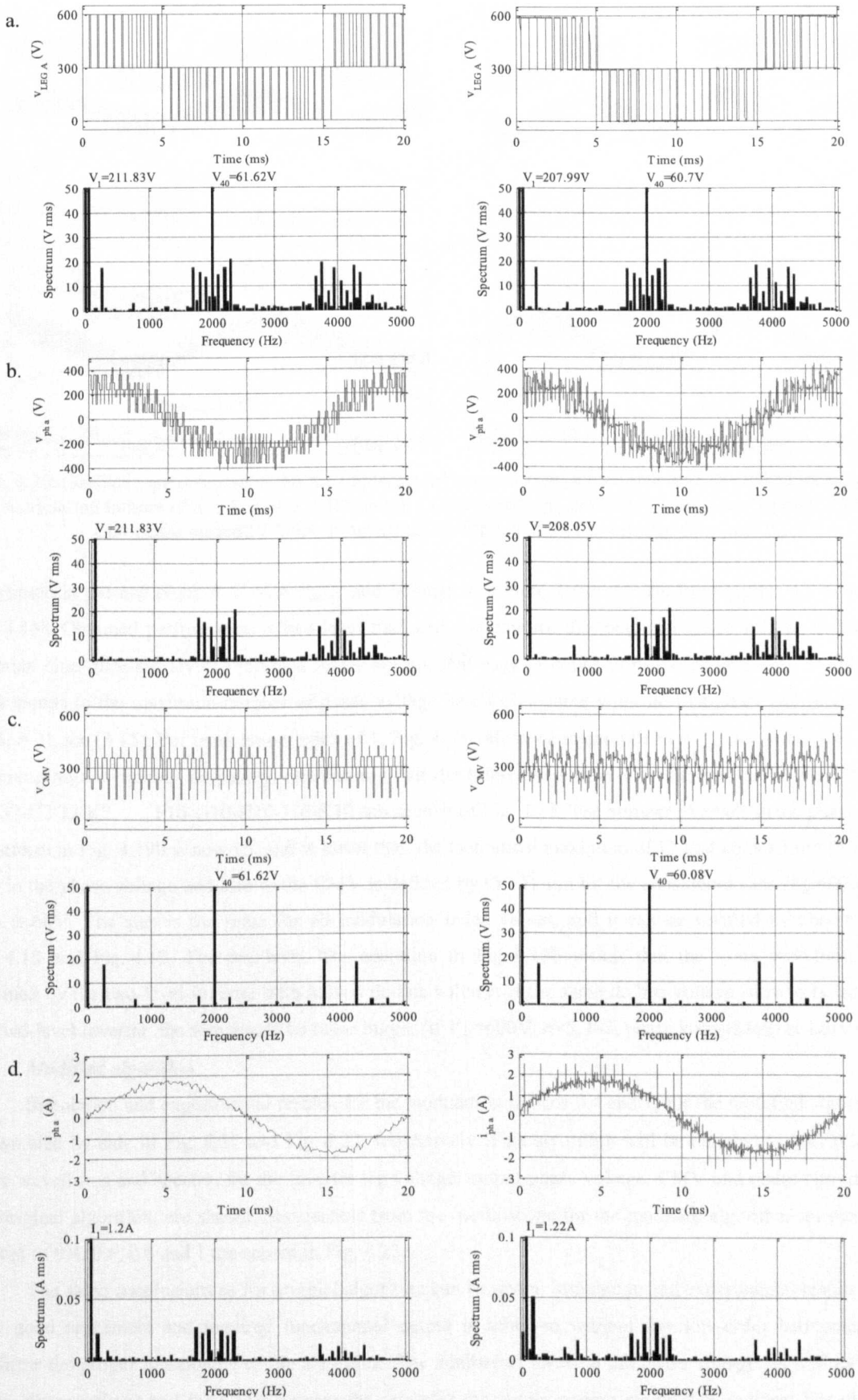


Fig. 4.19: Simulation (left column) and experimental (right column) results for the original five-phase three-level SVPWM method. a. Leg *A* voltage, b. phase *a* voltage, c. CMV, d. phase *a* current, with associated spectra. Results are for the modulation index m=1 (SVPWM1, n=5, l=3).

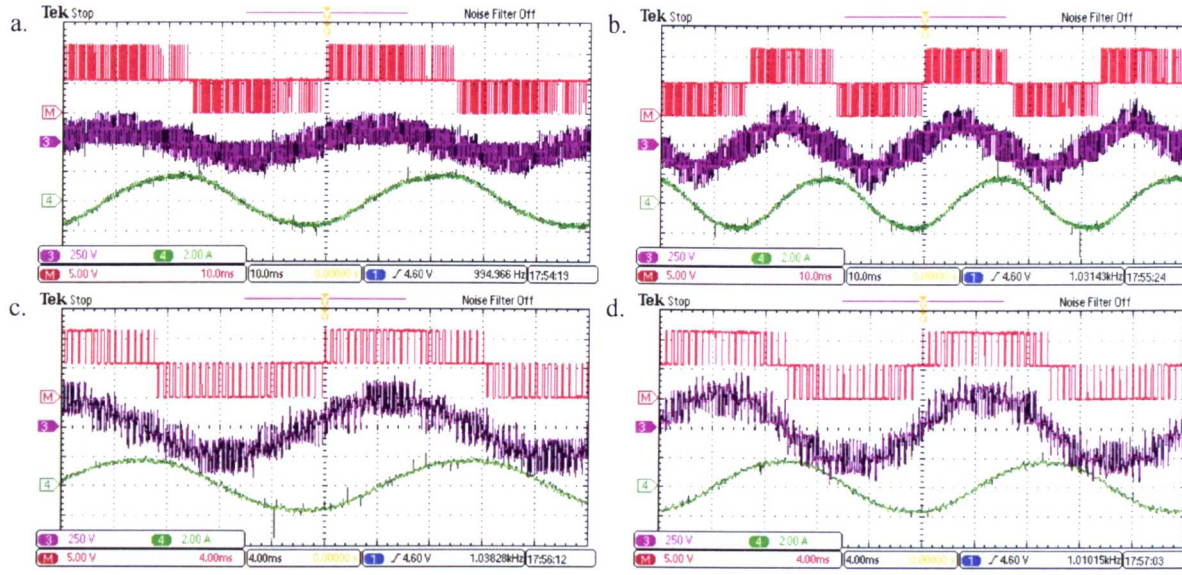


Fig. 4.20: Oscilloscope screenshots for the implemented original five-phase three-level SVPWM technique for the modulation indices of a. 0.4, b. 0.6, c. 0.8 and d. 1 (M-leg voltage, 260V/div; Ch3-phase voltage, 250V/div; Ch4-phase current, 2A/div; time=10ms/div for a. and b., i.e. 4ms/div for c. and d.).

magnitude in the α-β plane is V^*=0.4·V_{dc}/2, and belongs to region A (i.e. travels from region A1 to A10, see Fig. 4.13). Obtained performance is two-level like, and one can see that obtained phase voltage in Fig. 4.18b contains nine different levels (obtained levels are not that easy to count from the experimental results). This corresponds to the maximum number of phase voltage levels obtainable with the five-phase two-level inverter (n=5, l=2), see (3.15). For modulation index of 1, Fig. 4.19, reference magnitude in α-β plane is V^*=1·V_{dc}/2, and, assuming high switching frequency, one can say that the reference is travelling through the F1-G1-H1-J1-K1, F2-G2-H2-J2-K2, …, F10-G10-H10-J10-K10 sub-sectors of Fig. 4.13. The number of levels in the phase voltage waveform in Fig. 4.19b is now 15, and is lower than the theoretical maximum of 17 that comes from (3.15). The step in the phase voltage and also in the CMV is defined by (3.14) and for the considered case (V_{dc}=600V, n=5, l=3) is 60V. The step is the same for all modulation index values, and it can be verified by observation of Fig. 4.18 and Fig. 4.19. The two-level like operation in Fig. 4.18b means that the same waveform can be obtained by the two-level inverter with halved dc-bus voltage; if the same dc bus voltage were to be applied to the two-level inverter, the step would be twice bigger (if V_{dc}=600V, n=5, l=2, phase voltage step is 120V).

Modified algorithm

Simulation and experimental results, for the modulation indices 0.4 and 1, for the modified algorithm are shown side by side in Fig. 4.21 and Fig. 4.22, respectively. This algorithm will be denoted as SVPWM2. The same waveforms and spectra, for the inverter leg voltage, output phase voltage, CMV and phase current, as for the original algorithm, are shown. Screenshots from the oscilloscope for the modified algorithm for modulation indices of 0.4, 0.6, 0.8 and 1 are shown in Fig. 4.23.

The same conclusions as for original algorithm can be given. Simulation and experimental results are in a very good agreement and required fundamental output is achieved without any low-order harmonics – this confirms the proper functioning of the algorithm. The number of levels in the phase voltage, as well as the step of the phase voltage and the CMV, remain the same for the corresponding modulation indices. The difference between these two modulation strategies is hardly noticeable in time domain traces (Fig. 4.18 vs. Fig. 4.21, Fig. 4.19 vs. Fig. 4.22, and Fig. 4.20 vs. Fig. 4.23). The only noticeable difference is in the leg voltages where

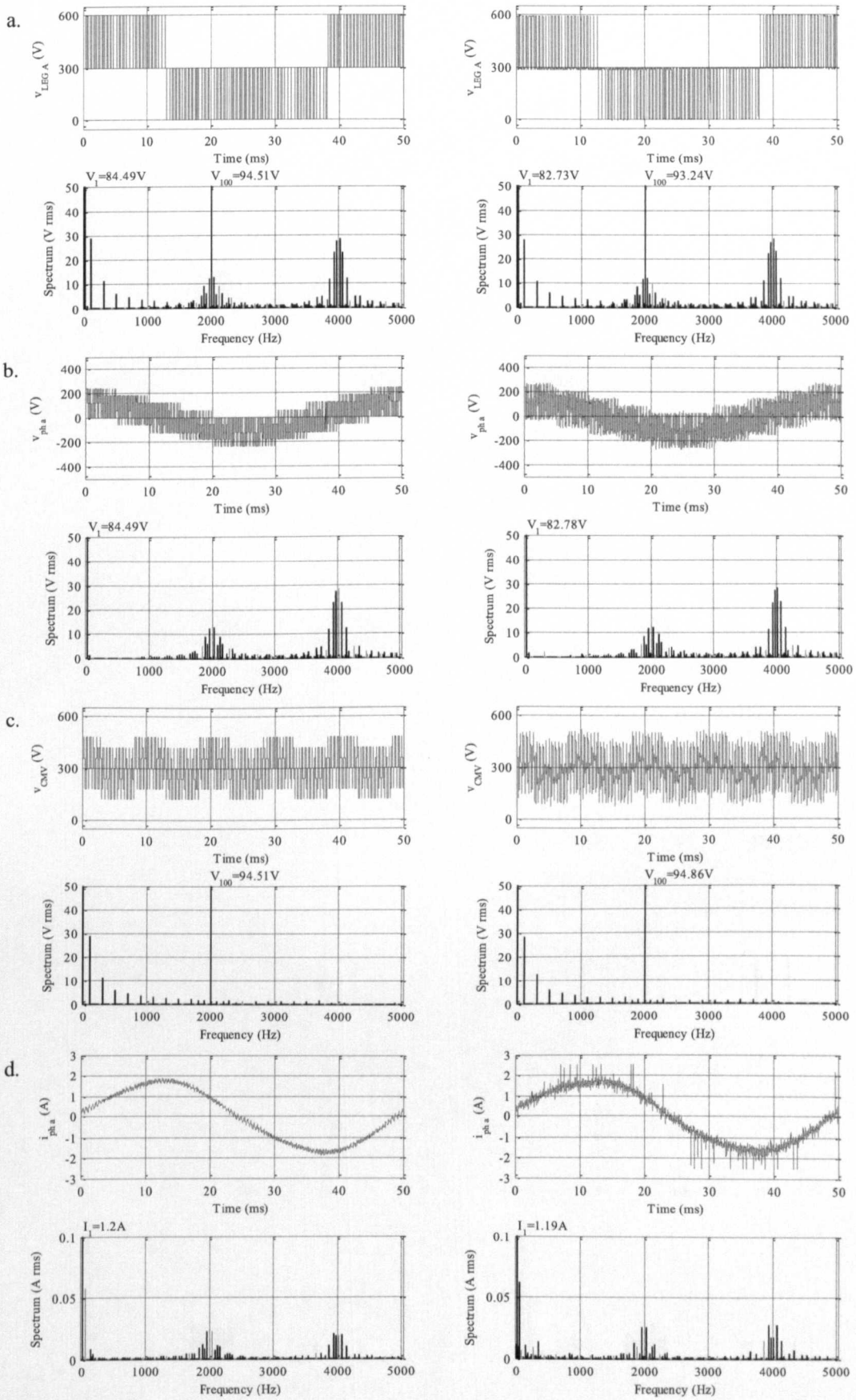


Fig. 4.21: Simulation (left column) and experimental (right column) results for modified five-phase three-level SVPWM algorithm. a. Leg *A* voltage, b. phase *a* voltage, c. CMV, d. phase *a* current, with associated spectra. Results are for the modulation index m=0.4 (SVPWM2, n=5, l=3).

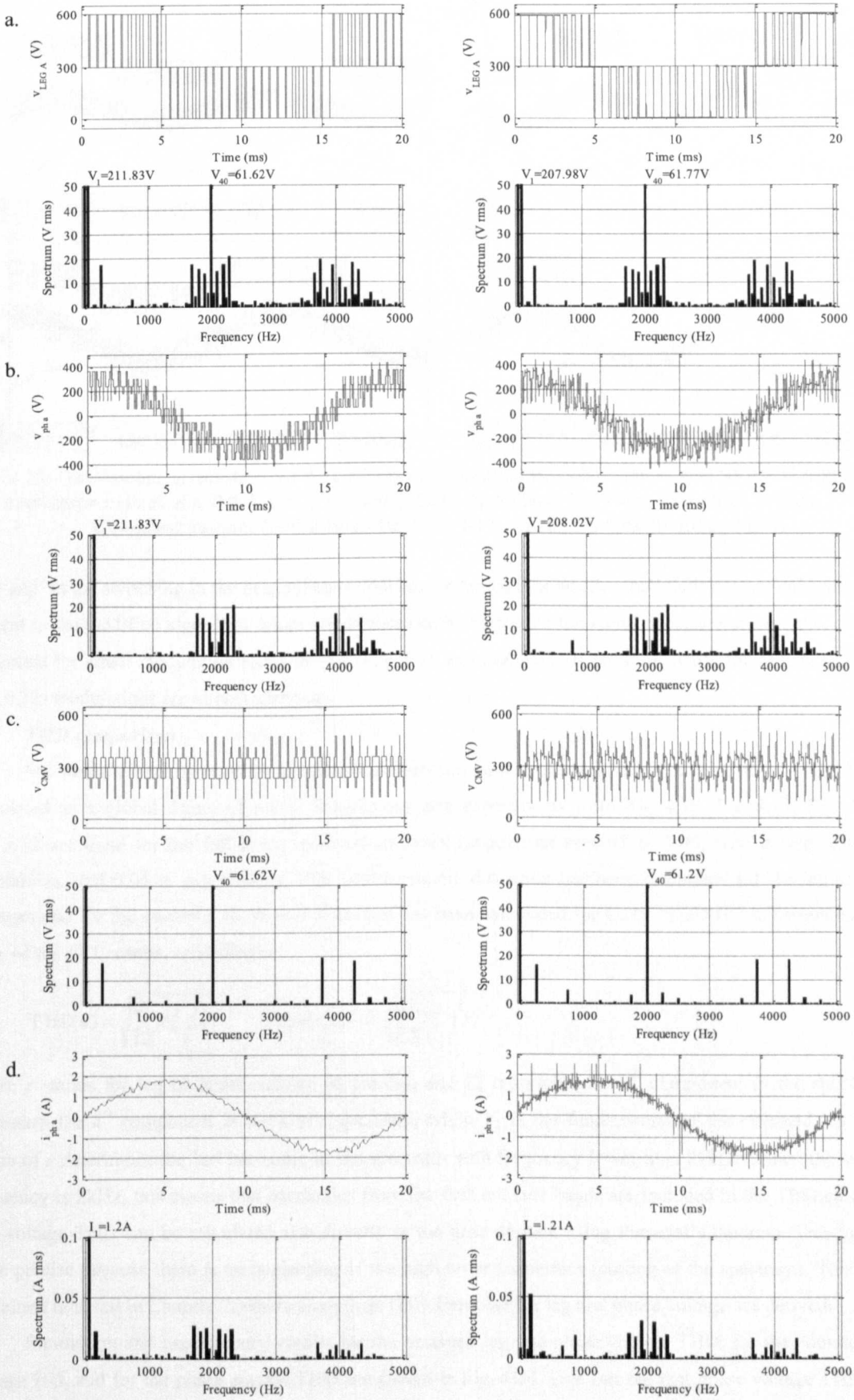


Fig. 4.22: Simulation (left column) and experimental (right column) results for modified five-phase three-level SVPWM algorithm. a. Leg *A* voltage, b. phase *a* voltage, c. CMV, d. phase *a* current, with associated spectra. Results are for the modulation index m=1 (SVPWM2, n=5, l=3).

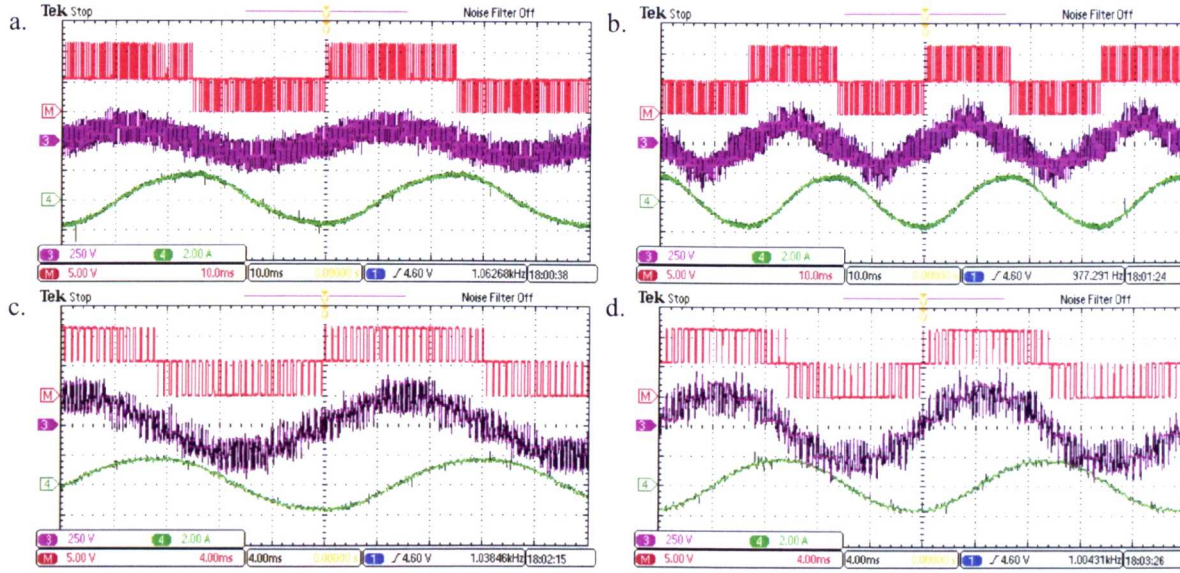


Fig. 4.23: Oscilloscope screenshots for the implemented modified five-phase three-level SVPWM technique for the modulation indices of a. 0.4, b. 0.6, c. 0.8 and d. 1 (M-leg voltage, 260V/div; Ch3-phase voltage, 250V/div; Ch4-phase current, 2A/div; time=10ms/div for a. and b., i.e. 4ms/div for c. and d.).

one 'gap' in the switching in the original algorithm can be noticed for smaller modulation index values that is not present in the modified algorithm. More differences can be noticed in the signal spectra. For example, difference in spectra for small modulation index m=0.4 (Fig. 4.18 and Fig. 4.21) is obvious, while for m=1 (Fig. 4.19 and Fig. 4.22) modulations are almost identical.

THD comparison

For initial comparison of the presented modulation strategies total harmonic distortion, THD, has been calculated as a global figure of merit. Simulations and experiments from Fig. 4.18, Fig. 4.19, Fig. 4.21 and Fig. 4.22 are done for the full linear modulation index range from m=0.05 to 1.05, with a step of 0.025 in simulations, and 0.05 in experiments. The total harmonic distortion has been calculated for the leg and phase voltages and for the currents. Harmonic distortion has been calculated for CMV. THD/HD is computed, on the basis of the FFT results, according to:

$$\mathrm{THD}(z) = \sqrt{\sum_{k=2}^{r} Z_k^2 \Big/ Z_1^2} \qquad \mathrm{HD}(v_{\mathrm{CMV}}) = \sqrt{\sum_{k=2}^{r} V_k^2 \Big/ V_1^2} \tag{4.9}$$

where z stands for leg or phase voltage or current, and Z_k represents the k^{th} component in the spectrum, V_k represents the k^{th} component in the CMV spectrum, while V_1 is the fundamental of the obtained leg voltage. Value of r determines the last harmonic in the spectrum with frequency lower than 21kHz. Since the switching frequency is 2kHz, this means that harmonics from the first ten side bands are included in the THD calculation. The voltage THD can be calculated also directly in the time domain using Parseval's theorem. This method is more precise because there is no neglecting of the high order harmonics (cutting of the spectrum). This topic is explained in detail in Chapter 7, where analytical THD formulae for leg and phase voltage are derived.

Simulation and experimental results for the obtained leg and phase voltage THD, for the common mode voltage HD, and for the phase current THD are shown in Fig. 4.24. One can see that phase voltage THD values for both strategies are identical, and the same values are obtained by simulations and by experiments, Fig. 4.24b. Because of that, a small difference that is observable in the leg voltage THD for the two modulation strategies,

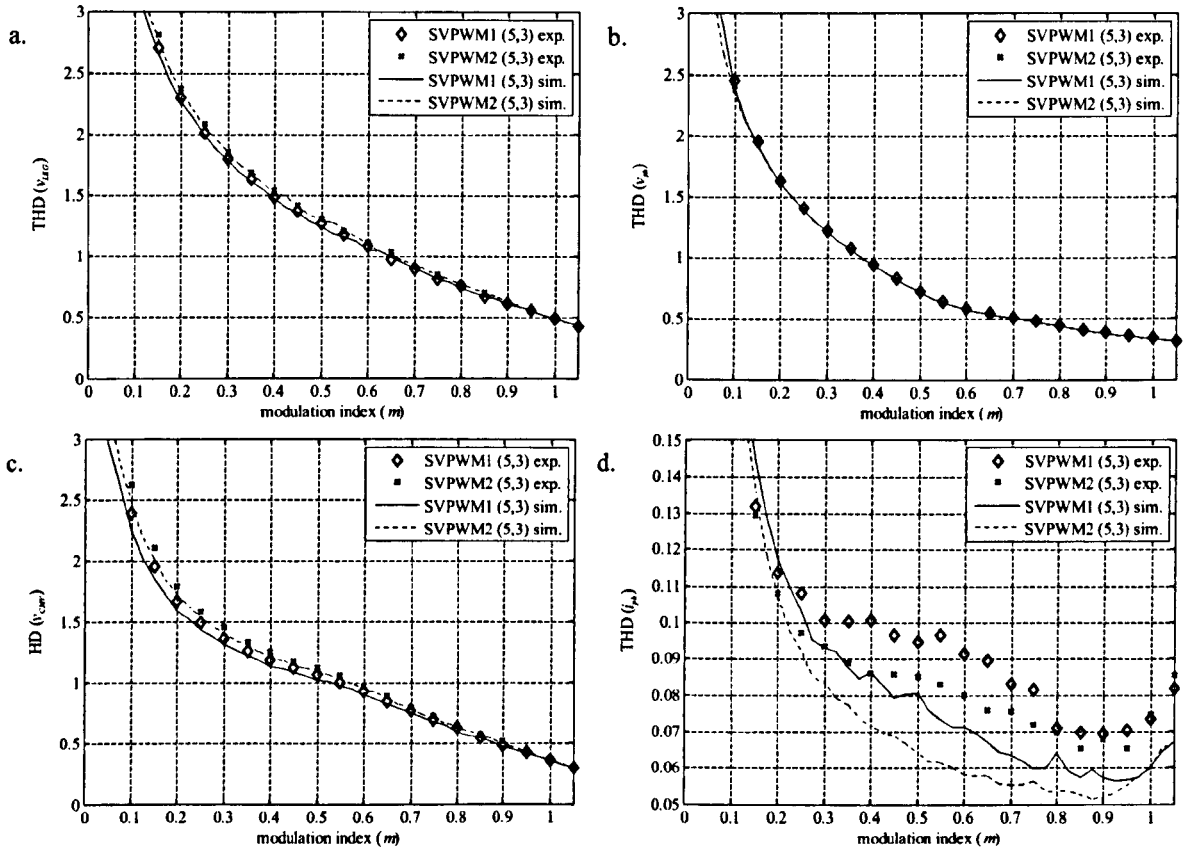


Fig. 4.24: Simulation and experimental results for the original (SVPWM1) and modified (SVPWM2) algorithm for the a. leg voltage THD, b. phase voltage THD, c. CMV HD and d. phase current THD (n=5, l=3).

Fig. 4.24a, is also present in the common mode voltage HD, Fig. 4.24c. For all analysed voltage THD/HD, simulation and experimental results are in a very good agreement. As can be seen, increase of the modulation index reduces THD/HD. Namely, with an increase of the modulation index value, reference passes through more sub-sectors, so more switching states that are closer to the reference are in use. This represents a benefit of multilevel operation. The mentioned increased similarity between original and modified algorithms is also obvious from the THD plots, Fig. 4.24.

Current THD is shown in Fig. 4.24d. One can see that some difference between simulation and experimental curves for corresponding modulation strategies is present. This comes from the simplified model used in simulations, where it is assumed that all parameters are constant. However it should be noted that the shown current THD has a very narrow range with very small values (0.05-0.15) and that simulation curves follow the order and the shape of the experimental results.

A further analysis regarding comparison between different strategies is given in Chapter 6. In that chapter presented space vector modulation strategies are compared with some carrier-based modulation techniques, which will be introduced in the next chapter.

4.3 SEVEN-PHASE THREE-LEVEL SPACE VECTOR ALGORITHM BASED ON VSD APPROACH

The results of this section are reported in [Dordevic et al. (2011b)], which represents the first space vector modulation technique, based on the voltage space decomposition, for three-level seven-phase VSIs. A considerably expanded version has been further published in [Dordevic et al. (2013b)]. In the seven-phase case, cancelation of the components in both the second and the third plane is necessary in order to achieve the sinusoidal output voltages. All the steps from the previous section 4.2 will be now briefly reviewed, with the appropriate modifications, caused by the change of the number of phases, highlighted. Modification of the original algorithm that has been presented for the five-phase case (sub-section 4.2.7) will be also applied to the seven-phase algorithm. Topology of the system is shown in Fig. 4.25. A seven-phase induction machine (in experiments an *R–L* load was used) is supplied from a seven-phase three-level neutral-point clamped VSI.

4.3.1 VECTOR SPACE DECOMPOSITION

Process of the VSD is based on the same principles as in the five-phase case, since it uses the universal space vector definition from section 3.4. In the seven-phase three-level case (n=7, l=3), according to (3.2), there are 3^7=2187 switching states, and 2059 unique phase voltage space vectors (Table 3.1). This is significantly more than in the five-phase case (243/211), so all the steps are much more involved. For the sake of illustration, only projections of the obtained leg (phase) voltage space vectors in the first, α-β, plane are shown in Fig. 4.26. Sinusoidal symmetrical phase reference voltages are defined as in (4.1). As it has already been explained in sub-section 4.2.1, VSD based algorithms do not consider zero axis and CMV voltage, and directly apply process of the averaging (PWM) in all the other planes for the desired and obtained values. So only projections to α-β, x_1-y_1, x_2-y_2 planes are of interest, and they are defined as in (3.30), where A=1 and pl = 1, 2, 3 for the mentioned planes, respectively.

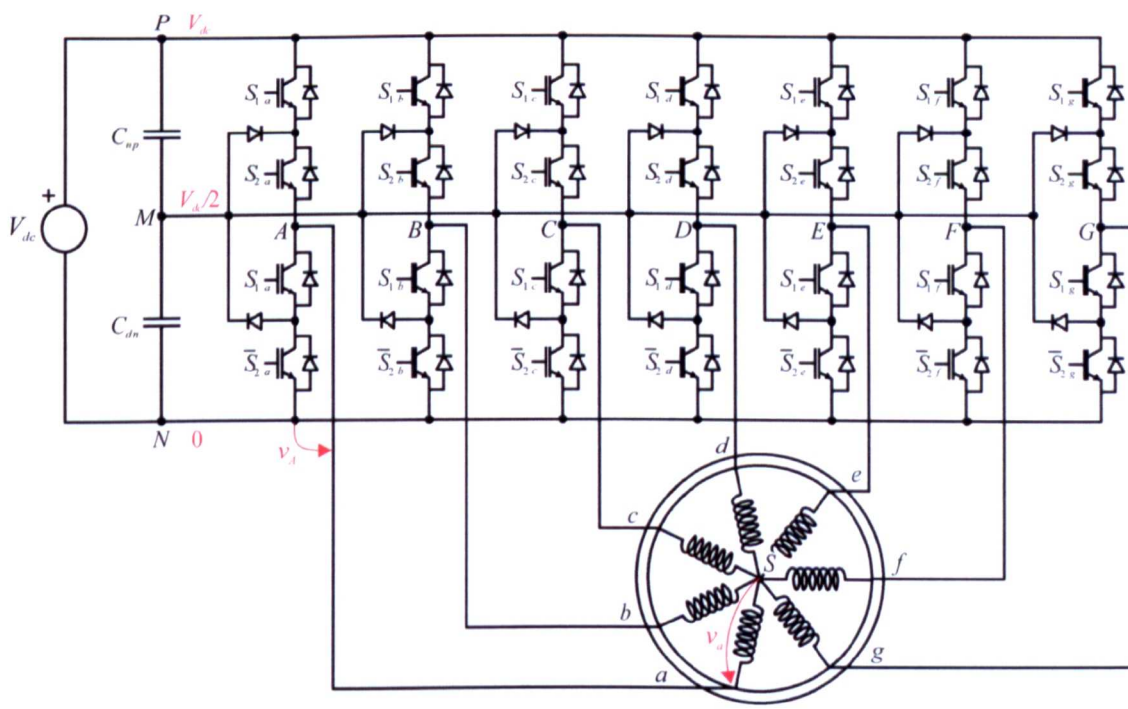


Fig. 4.25: Analysed topology of a three-level seven-phase NPC VSI-supplied induction motor drive.

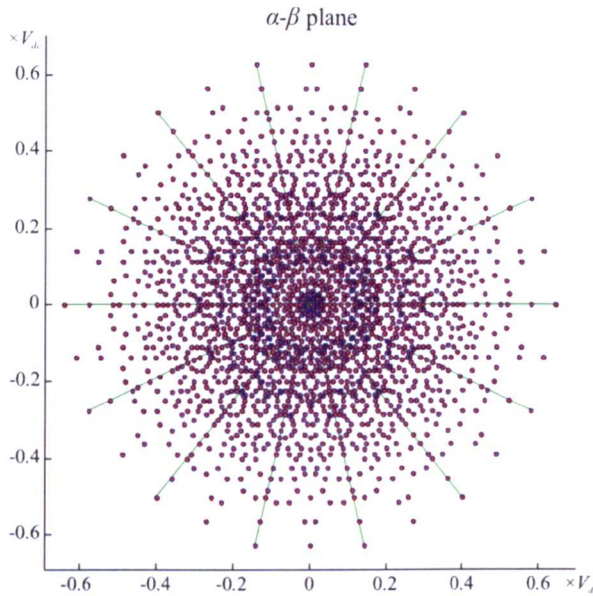


Fig. 4.26: All 2187 states giving 2059 space vector projections in the first (α-β) plane for the three-level seven-phase system.

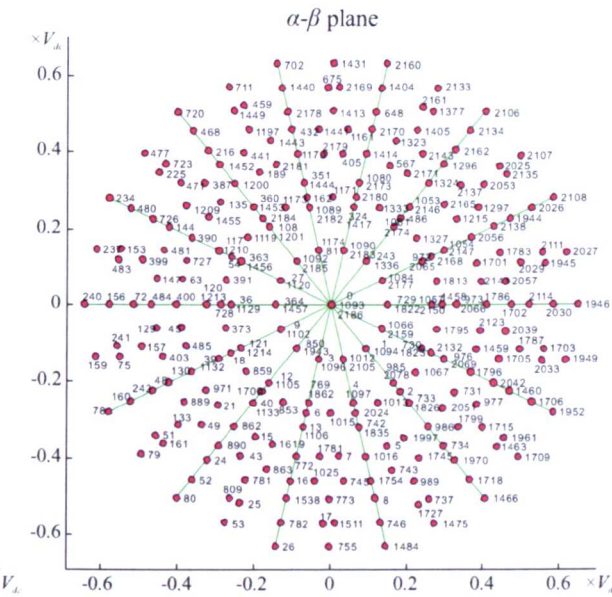


Fig. 4.27: Remaining switching states after application of the order-per-sector law, in the α-β plane.

4.3.2 ORDER-PER-SECTOR LAW AND REDUCTION OF THE NUMBER OF SWITCHING STATES

As it was explained in sub-section 4.2.2, order-per-sector law from time domain is universal, so it can be applied in a straightforward manner to the seven-phase case, where there are 14 different sectors. Ordering of the reference phase voltages in each sector is given in Table 4.6. For example, in the first sector $v_a^* \geq v_b^* \geq v_g^* \geq v_c^* \geq v_f^* \geq v_d^* \geq v_e^*$, and, according to the order-per-sector law, reference leg voltages and also obtained leg and phase voltages will follow the same ordering. Thus, if sinusoidal output is desired, some switching states, that do not satisfy introduced order-per-sector law, can be eliminated. For instance, switching state 2120012 belongs to the first sector, but does not satisfy required ordering for the first sector, since $v_B < v_C$. The number of switching states of interest can be significantly reduced in this way, from 2187 to 297. The remaining 297 switching states are

Table 4.6: Per-sector ordering of reference phase voltages for the seven-phase case.

Sector	Phase voltages order
1	$v_a^* \geq v_b^* \geq v_g^* \geq v_c^* \geq v_f^* \geq v_d^* \geq v_e^*$
2	$v_b^* \geq v_a^* \geq v_c^* \geq v_g^* \geq v_d^* \geq v_f^* \geq v_e^*$
3	$v_b^* \geq v_c^* \geq v_a^* \geq v_d^* \geq v_g^* \geq v_e^* \geq v_f^*$
4	$v_c^* \geq v_b^* \geq v_d^* \geq v_a^* \geq v_e^* \geq v_g^* \geq v_f^*$
5	$v_c^* \geq v_d^* \geq v_b^* \geq v_e^* \geq v_a^* \geq v_f^* \geq v_g^*$
6	$v_d^* \geq v_c^* \geq v_e^* \geq v_b^* \geq v_f^* \geq v_a^* \geq v_g^*$
7	$v_d^* \geq v_e^* \geq v_c^* \geq v_f^* \geq v_b^* \geq v_g^* \geq v_a^*$
8	$v_e^* \geq v_d^* \geq v_f^* \geq v_c^* \geq v_g^* \geq v_b^* \geq v_a^*$
9	$v_e^* \geq v_f^* \geq v_d^* \geq v_g^* \geq v_c^* \geq v_a^* \geq v_b^*$
10	$v_f^* \geq v_e^* \geq v_g^* \geq v_d^* \geq v_a^* \geq v_c^* \geq v_b^*$
11	$v_f^* \geq v_g^* \geq v_e^* \geq v_a^* \geq v_d^* \geq v_b^* \geq v_c^*$
12	$v_g^* \geq v_f^* \geq v_a^* \geq v_e^* \geq v_b^* \geq v_d^* \geq v_c^*$
13	$v_g^* \geq v_a^* \geq v_f^* \geq v_b^* \geq v_e^* \geq v_c^* \geq v_d^*$
14	$v_a^* \geq v_g^* \geq v_b^* \geq v_f^* \geq v_c^* \geq v_e^* \geq v_d^*$

shown in Fig. 4.27 in the α-β plane. Switching states are shown using decimal representation. For example, switching state 2210002 in decimal notation is 2027 (since $2027 = 2\cdot3^6 + 2\cdot3^5 + 1\cdot3^4 + 0\cdot3^3 + 0\cdot3^2 + 0\cdot3^1 + 2\cdot3^0$).

4.3.3 DETERMINATION OF POSSIBLE SWITCHING SEQUENCES

Switching sequences are determined in the same way as explained for the five-phase case in sub-section 4.2.3. The first sector of the α-β plane, with reduced number of switching states according to the order-per-sector law, and with all possible transitions, is shown in Fig. 4.28. According to the graphical interpretation of one level transition in the k^{th} leg as a $2/n$ scaled unit vector inclined for $2\pi/n\cdot(k-1)$ radians with respect to the α-axis, it is easy to obtain Fig. 4.28. Transition in each leg is shown in a different colour. Note also that there are n arrows of each colour. As explained, construction of switching sequences means that one has to find all closed (the first and the last switching states correspond to the same space vector) seven-angle patterns that contain all seven different colours (transition for one level appears in each leg). The starting switching state has to be redundant, and also must not contain the highest level (in three-level VSI this is 2), since an increase by one level in that leg would lead to leg level 3, which is not possible. Potential starting switching states of switching sequences (eight of them) are shown underlined in Fig. 4.28. Determination of all closed seven-angle patterns is solved using Matlab code. Programme is of a simple structure. It contains all switching states from Fig. 4.28 and it creates all possible permutations of transitions and adds that to the starting switching states. If all produced states belong to the set of the switching states from Fig. 4.28, then it is one of the possible switching sequences. Further, the code determines position of the possible switching sequence projections in the α-β plane and those with the same projections (pattern) are regarded as redundant sequences. One gets that there are a total of 128 possible switching sequences corresponding to all 64 patterns. The number of 64 closed patterns is significantly more than in the five-phase case, where there were only 16. Also, in the five-phase case there were only 32 switching sequences.

Switching sequences are not yet completely determined at this stage, since some of the patterns cannot provide cancellation (i.e. zeroing of the average voltage) in the x-y planes. Recall that in the five-phase case this problem was solved graphically by examining position of the patterns in the x_1-y_1 plane. In the seven-phase case this is not the sufficient condition, as it will be explained in the following sub-section. Also, some of the patterns contain more potential beginnings of the switching sequence. For example, the pattern in Fig. 4.28, shown with oversized arrows, contains five potential starting (underlined) switching states, i.e. there are five possible, redundant, switching sequences. These two problems will be addressed in the following two sub-sections.

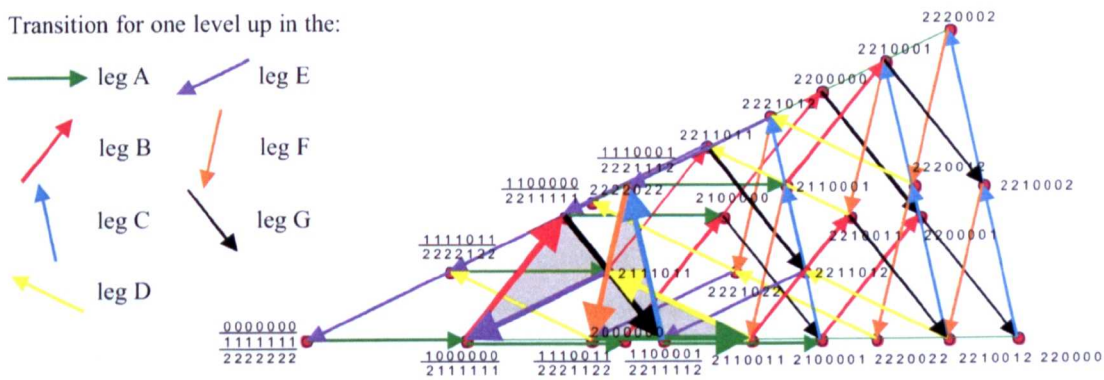


Fig. 4.28: The first sector in the α-β plane with reduced number of switching states and with all possible single-level increasing transitions.

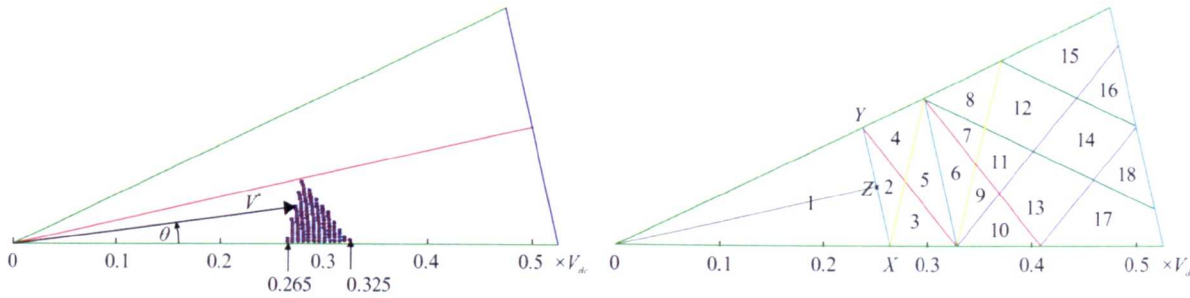
4.3.4 DWELL TIME CALCULATION AND SECTOR PARTITIONING

For dwell time calculation, only projections of space vectors into planes are important. Rewriting (3.51) for the seven-phase system, one has:

$$\begin{bmatrix} T_1 \\ T_2 \\ T_3 \\ T_4 \\ T_5 \\ T_6 \\ T_7 \end{bmatrix} = \begin{bmatrix} v_{\alpha,1} & v_{\alpha,2} & v_{\alpha,3} & v_{\alpha,4} & v_{\alpha,5} & v_{\alpha,6} & v_{\alpha,7} \\ v_{\beta,1} & v_{\beta,2} & v_{\beta,3} & v_{\beta,4} & v_{\beta,5} & v_{\beta,6} & v_{\beta,7} \\ v_{x_1,1} & v_{x_1,2} & v_{x_1,3} & v_{x_1,4} & v_{x_1,5} & v_{x_1,6} & v_{x_1,7} \\ v_{y_1,1} & v_{y_1,2} & v_{y_1,3} & v_{y_1,4} & v_{y_1,5} & v_{y_1,6} & v_{y_1,7} \\ v_{x_2,1} & v_{x_2,2} & v_{x_2,3} & v_{x_2,4} & v_{x_2,5} & v_{x_2,6} & v_{x_2,7} \\ v_{y_2,1} & v_{y_2,2} & v_{y_2,3} & v_{y_2,4} & v_{y_2,5} & v_{y_2,6} & v_{y_2,7} \\ 1 & 1 & 1 & 1 & 1 & 1 & 1 \end{bmatrix}^{-1} \cdot \begin{bmatrix} v_\alpha^* \\ v_\beta^* \\ v_{x_1}^* \\ v_{y_1}^* \\ v_{x_2}^* \\ v_{y_2}^* \\ 1 \end{bmatrix} \cdot T_s \tag{4.10}$$

where T_i (i=1, 2, ..., 7) stands for the time of application of an appropriate space vector in the pattern – dwell time, and $v_{p,i}$ represents the i^{th} space vector projection onto p-axis (α, β, x_1, y_1, x_2, y_2). Since generation of the sinusoidal reference voltage is desired, one has in (4.10) $v_\alpha^* = V^* \cdot \cos(\omega t)$, $v_\beta^* = V^* \cdot \sin(\omega t)$, $v_{x1}^* = 0$, $v_{y1}^* = 0$, $v_{x2}^* = 0$, $v_{y2}^* = 0$.

The regions of application of each pattern can be again determined using the simple constraint from [Gao and Fletcher (2010)] that time of application of each vector must be in the range 0 to T_s. Even for the five-phase case it was concluded that analytical solution of the dwell time equation, and further application of the constraint $0 \leq \{T_1, T_2, \ldots\} \leq T_s$, to get analytical values for sub-sector borders, is very difficult. Also, in the five-phase case, equation (4.5) (five-phase equivalent of (4.10)) was solved for only 10 patterns, since 6 patterns were automatically eliminated. Projections of those six patterns into the x_1-y_1 plane were placed at the same side of the line that passes through the origin, so that those patterns could not lead to the desired zero average value in this plane. In the seven-phase case, the problem is more complicated, and this part represents the main difference between the five- and seven-phase cases. In the seven-phase case there are 64 patterns, and graphical method of considering position of the patterns in the x-y planes is not the sufficient condition for reduction of the possible switching pattern number. To be more precise, only 16 out of 64 patterns can be eliminated using this graphical method. The problem is that there are patterns with which cancellation in both of x-y planes can be achieved independently, but the solutions do no not overlap, meaning that x-y components cannot be cancelled in both planes at the same time. This is indeed one of the major additional difficulties, brought in by the higher number of phases, compared to the five-phase case. Hence the problem is solved with a Matlab programme, very similar to the one used in the five-phase case, which solves equation (4.10) for each of 64 (i.e. 64–18=46) switching patterns, increasing in incremental steps the values of the reference angle θ and magnitude V^*. If a solution exists and if all dwell times are in the range 0 to T_s, the programme plots a dot on a certain position, $V^* e^{j\theta}$, in the α-β plane. This means that the current pair of V^* and θ belongs to the region of applicability for the selected pattern, and all plotted dots for the selected pattern represent region of application for the selected pattern. As an example of the output of this code Fig. 4.29a shows the area that is covered by the pattern shown with oversized arrows in Fig. 4.28. Note that the graphical method for the elimination of those patterns that cannot provide cancellation in the second or in the third plane is not necessary because these patterns will be recognized and eliminated anyway by this numerical procedure (executed by the Matlab program). For these patterns the solution of (4.10) does not exist.



a. b.

Fig. 4.29: Sub-sector region of applicability: a. area that is encompassed by oversized arrows in Fig. 4.28 (plot from the Matlab code), b. division of the first sector into sub-sectors.

One finds in this way that only 18 out of 64 patterns enable simultaneous cancellation of the voltage, on average, in both x-y planes, while simultaneously satisfying the set conditions for the permissible range of dwell times. These 18 patterns should not be confused with 18 patterns that can be eliminated graphically. This means that the first sector can be sub-divided into 18 sub-sectors, as shown in Fig. 4.29b. The problem was solved numerically, so that the borders between sub-sectors can be approximately read from the nearest points. From Fig. 4.29b, it is clear that all partitioning lines are straight lines and they form angles of $2 \cdot 2\pi/14$, $3 \cdot 2\pi/14$, ..., $6 \cdot 2\pi/14$ with the α-axis. Analytical values of the borders between sub-sectors in Fig. 4.29b are desirable. However, analytical solution looks too complicated. Similarly as for five-phase case (sub-section 4.2.4) one can see that one of the redundant sequences for the sub-sector 1 in Fig. 4.29b is: 0000000-1000000-1100000-1100001-1110001-1110011-1111011-1111111, which is one of the eight (see underlined switching states for this pattern in Fig. 4.28) redundant switching sequences for this pattern. This sequence contains only zeros and ones; thus it can be obtained by an equivalent two-level inverter with halved dc-bus voltage value. The border between two-level and three-level operation of the inverter is now defined by XY line, and the length of OZ represents one half of the value of the maximum modulation index for the two-level seven-phase inverter $m_{\max 7,2}$ [Levi et al. (2008)]. Hence:

$$OZ = \frac{1}{2} \cdot m_{\max 7,2} \cdot \frac{V_{dc}}{2} = \frac{V_{dc}}{4} \cdot \frac{1}{\cos(\pi/14)} \tag{4.11}$$

All angles in Fig. 4.29b are known, so analytical values for all the other lengths can be obtained using value of OZ and some simple geometry.

4.3.5 SWITCHING SEQUENCE OPTIMISATION

Final decision, which of the redundant switching sequences that correspond to the same pattern will be used, is done in the same way as for the five-phase case. As the result of the previous step, it follows that only 18 patterns (with corresponding 56 sequences) have to be analysed. The basic optimisation criteria are minimisation of the switching losses and capacitor voltage balancing. For minimisation of the switching losses, it is desirable that all sub-sector sequences have the same starting switching state, if possible, to avoid additional switching when reference changes sub-sector. Also, according to [Gao and Fletcher (2010)], more desirable sequences, for better voltage balancing of the capacitor voltages, are those that contain more 'ones'. Switching state denoted with '1' represents output voltage of an inverter leg of $V_{dc}/2$. In that case, for the analysed NPC VSI configuration, output of the leg is determined by the dc-bus mid-point, so that the more 'ones' there are in the

Table 4.7: Selected switching sequences for SVPWM in the first sector (n=7, l=3).

Sub-sector	Chosen switching sequence
1	1110001-1110011-1111011-1111111-2111111-2211111-2211112-2221112
2	1110001-1110011-1111011-2111011-2111111-2211111-2211112-2221112
3	1110001-1110011-2110011-2111011-2111111-2211111-2211112-2221112
4	1110001-1110011-1111011-2111011-2211011-2211111-2211112-2221112
5	1110001-1110011-2110011-2111011-2211011-2211111-2211112-2221112
6	1110001-1110011-2110011-2210011-2211011-2211111-2211112-2221112
7	1110001-2110001-2110011-2210011-2211011-2211111-2211112-2221112
8	1110001-2110001-2210001-2210011-2211011-2211111-2211112-2221112
9	1110001-1110011-2110011-2210011-2211011-2211012-2211112-2221112
10	1110001-1110011-2110011-2210011-2210012-2211012-2211112-2221112
11	1110001-2110001-2110011-2210011-2211011-2211012-2211112-2221112
12	1110001-2110001-2210001-2210011-2211011-2211012-2211112-2221112
13	1110001-2110001-2110011-2210011-2210012-2211012-2211112-2221112
14	1110001-2110001-2210001-2210011-2210012-2211012-2211112-2221112
15	1110001-2110001-2210001-2210011-2211011-2211012-2221012-2221112
16	1110001-2110001-2210001-2210011-2210012-2211012-2221012-2221112
17	1100001-2100001-2110001-2110011-2210011-2210012-2211012-2211112
18	1100001-2100001-2110001-2210001-2210011-2210012-2211012-2211112

sequence (which encompasses all the relevant switching states applied in one switching period), better the balancing of the capacitor voltages can be achieved. Using these rules, final selection of the sequences for sub-sectors of Fig. 4.29b is as shown in Table 4.7. Only sub-sectors 17 and 18 have different starting switching state.

4.3.6 DETERMINATION OF THE SUB-SECTORS

Sub-sectors are determined in a similar way as for the five-phase case (sub-section 4.2.6). As there are 18 sub-sectors in the first sector, leading to the total of 252 sub-sectors in the α-β plane, the change of the sub-sector is even more frequent than in the five-phase case; thus the efficiency of sub-sector determination is even more important. Fig. 4.30 is used for determination of the sub-sectors. One can see that all borders between sectors can be divided into five groups. Each group contains only border-lines that are in parallel and form angles of $2\cdot 2\pi/14$, $3\cdot 2\pi/14$, ..., $6\cdot\pi/14$ with the α-axis. In Fig. 4.30, borders belonging to the same group are shown in the same colour. Intersections of sector border-lines with axes x_1 to x_5 define points L_{11}, L_{22}, ..., L_{52}, which are sufficient to explain each of the borders, since corresponding region is only the first sector (again, use of symbol x here is not related to the x–y planes). For example, if the reference is in the sub-sector 13 (as it is shown in Fig. 4.30), this means that the reference is located down-left from the border with sub-sector 14, i.e., the reference projection to the x_1-axis $V_{ref\,1}\leq L_{11}$; the reference must be located down-right from the border with sub-sector 11, i.e., $V_{ref\,5}>L_{51}$; considering the border with sub-sector 10, the reference must be located up-right, $V_{ref\,2}>L_{22}$; and from border with sub-sector 17, one gets $V_{ref\,5}\leq L_{52}$. Conditions for the sub-sector determination for all 18 sub-sectors inside the first sector ($0\leq\omega t<2\pi/14$) are given in Table 4.8. Note that, considering the length from the origin to the intersecting point, one has $L_{11} = L_{21} = L_{31} = L_{41} = L_{51}$, $L_{12} = L_{22} = L_{32} = L_{42} = L_{52}$, and these will be denoted further with L_1 and L_2, respectively, while L_{33} will be denoted as L_3.

Analytical value of L_1 is already given by (4.11), L_2 can be directly obtained from L_1 using simple geometry, while L_3 corresponds to the maximum modulation index for a seven-phase VSI [Levi et al. (2008)] (L_3=2L_1):

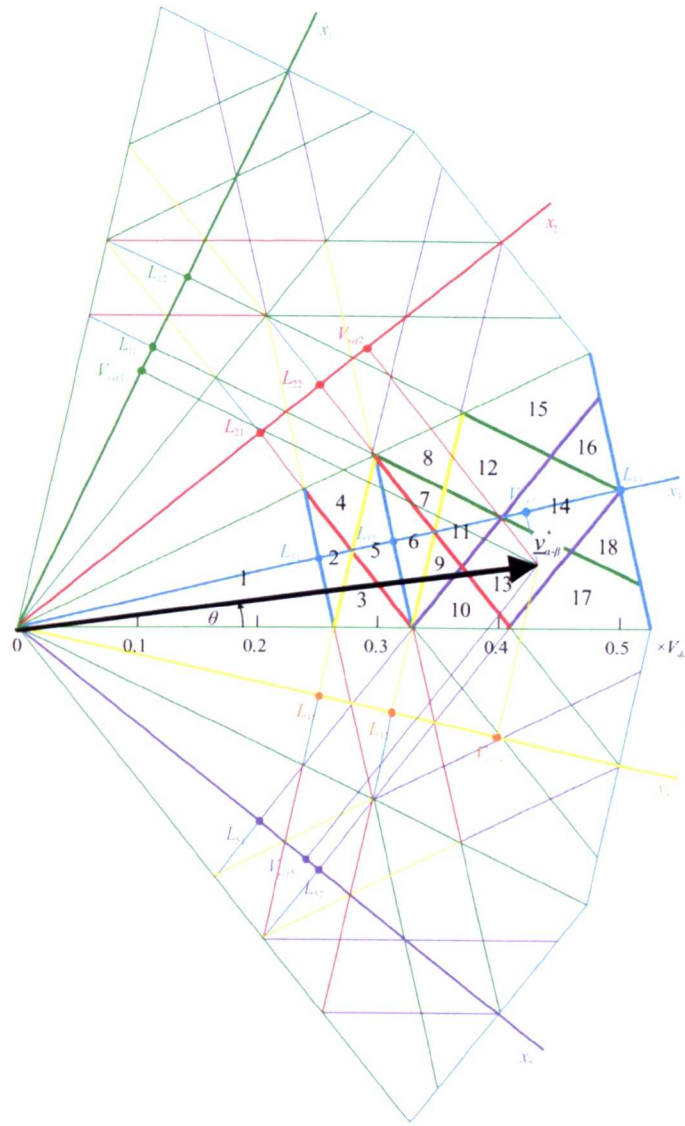


Fig. 4.30: Geometrical explanation of sub-sector determination in the seven-phase three-level case.

$$L_1 = \frac{V_{dc}}{4} \cdot \frac{1}{\cos(\pi/14)} = 0.2564 \cdot V_{dc}$$
$$L_2 = \frac{V_{dc}}{2} \cdot \frac{\cos(2\pi/7)}{\cos(\pi/14)} = 0.3198 \cdot V_{dc} \qquad (4.12)$$
$$L_3 = \frac{V_{dc}}{2} \cdot \frac{1}{\cos(\pi/14)} = 0.5129 \cdot V_{dc}$$

Projections of the reference vector onto axes x_1 to x_5 are denoted as V_{ref1} to V_{ref5}, and are given in Table 4.8 as well.

4.3.7 MODIFICATION OF THE PROPOSED ALGORITHM

The same modification with the same reasoning, as presented in sub-section 4.2.7 with halving of the sectors, can be applied in the seven-phase case. After halving of $2\pi/14$ sectors, 6 new sub-sectors appear, so the total number of sub-sectors per sector is increased from 18 to 24. Additional sub-division line leading to the new division of the first sector into sub-sectors is shown in Fig. 4.31. As it was explained in the five-phase case, from

Table 4.8: Sub-sector determination for the first sector ($0 \leq \theta < 2\pi/14$).

Reference projection	Value
V_{ref1}	$V^* \cdot \cos(5\pi/14-\theta)$
V_{ref2}	$V^* \cdot \cos(3\pi/14-\theta)$
V_{ref3}	$V^* \cdot \cos(\pi/14-\theta)$
V_{ref4}	$V^* \cdot \cos(\pi/14+\theta)$
V_{ref5}	$V^* \cdot \cos(3\pi/14+\theta)$
Sub-sector	Chosen switching sequence
1	$V_{ref3} \leq L_1$
2	$V_{ref2} \leq L_1$ and $V_{ref3} > L_1$ and $V_{ref4} \leq L_1$
3	$V_{ref2} \leq L_1$ and $V_{ref4} > L_1$
4	$V_{ref2} > L_1$ and $V_{ref4} \leq L_1$
5	$V_{ref2} > L_1$ and $V_{ref3} \leq L_2$ and $V_{ref4} > L_1$
6	$V_{ref2} \leq L_2$ and $V_{ref3} > L_2$ and $V_{ref4} \leq L_2$
7	$V_{ref1} \leq L_1$ and $V_{ref2} > L_2$ and $V_{ref4} \leq L_2$
8	$V_{ref1} > L_1$ and $V_{ref4} \leq L_2$
9	$V_{ref2} \leq L_2$ and $V_{ref4} > L_2$ and $V_{ref5} \leq L_1$
10	$V_{ref2} \leq L_2$ and $V_{ref5} > L_1$
11	$V_{ref1} \leq L_1$ and $V_{ref2} > L_2$ and $V_{ref4} > L_2$ and $V_{ref5} \leq L_1$
12	$V_{ref1} > L_1$ and $V_{ref1} \leq L_2$ and $V_{ref4} > L_2$ and $V_{ref5} \leq L_1$
13	$V_{ref1} \leq L_1$ and $V_{ref2} > L_2$ and $V_{ref5} > L_1$ and $V_{ref5} \leq L_2$
14	$V_{ref1} > L_1$ and $V_{ref1} \leq L_2$ and $V_{ref5} > L_1$ and $V_{ref5} \leq L_2$
15	$V_{ref1} > L_2$ and $V_{ref3} \leq L_3$ and $V_{ref5} \leq L_1$
16	$V_{ref1} > L_2$ and $V_{ref3} \leq L_3$ and $V_{ref5} > L_1$
17	$V_{ref1} \leq L_1$ and $V_{ref3} \leq L_3$ and $V_{ref5} > L_2$
18	$V_{ref1} > L_1$ and $V_{ref3} \leq L_3$ and $V_{ref5} > L_2$

the redundant switching sequences per pattern one should choose those which in the upper and in the lower half have the same starting switching state. The starting switching state for the lower half in the first sector is now 1100001, and for the upper half 1110001. The starting switching state in the lower half of the second sector is the same as for the upper half from the first sector; thus, once again, position of the extra transition is moved from the border between sectors and sub-sectors 17 and 18 (as denoted with thick lines in Fig. 4.31), to the straight line that halves the sector (i.e. to the newly added sub-division line). That means that with this modification losses are not increased. Also, as in the five-phase case, the capacitor voltage balancing is not affected.

Implementation of the proposed modification is simple. Only the additional condition for reference angular position should be included, and new sequences for the upper and the lower half of the sector should be

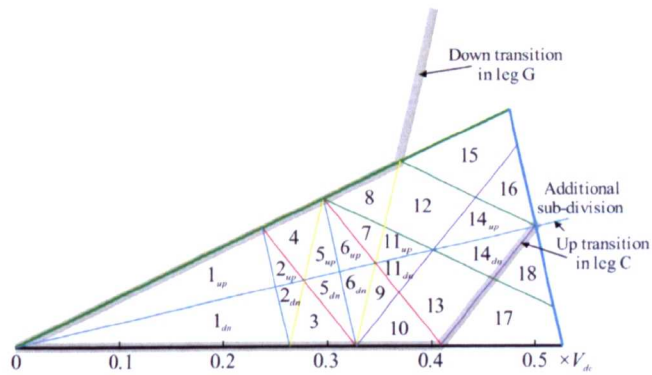


Fig. 4.31: Division of the first sector into sub-sectors after introduced modification.

Table 4.9: Selected switching sequences for modified SVPWM in the first sector (n=7, l=3).

Sub-sector	Chosen switching sequence
1_{dn}	1100001-1110001-1110011-1111011-1111111-2111111-2211111-2211112
2_{dn}	1100001-1110001-1110011-1111011-2111011-2111111-2211111-2211112
3_{dn}	1100001-1110001-1110011-2110011-2111011-2111111-2211111-2211112
5_{dn}	1100001-1110001-1110011-2110011-2111011-2211011-2211111-2211112
6_{dn}	1100001-1110001-1110011-2110011-2210011-2211011-2211111-2211112
9_{dn}	1100001-1110001-1110011-2110011-2210011-2211011-2211012-2211112
10_{dn}	1100001-1110001-1110011-2110011-2210011-2210012-2211012-2211112
11_{dn}	1100001-1110001-2110001-2110011-2210011-2211011-2211012-2211112
13_{dn}	1100001-1110001-2110001-2110011-2210011-2210012-2211012-2211112
14_{dn}	1100001-1110001-2110001-2210001-2210011-2210012-2211012-2211112
17	1100001-2100001-2110001-2110011-2210011-2210012-2211012-2211112
18	1100001-2100001-2110001-2210001-2210011-2210012-2211012-2211112
1_{up}	1110001-1110011-1111011-1111111-2111111-2211111-2211112-2221112
2_{up}	1110001-1110011-1111011-2111011-2111111-2211111-2211112-2221112
4	1110001-1110011-1111011-2111011-2211011-2211111-2211112-2221112
5_{up}	1110001-1110011-2110011-2111011-2211011-2211111-2211112-2221112
6_{up}	1110001-1110011-2110011-2210011-2211011-2211111-2211112-2221112
7	1110001-2110001-2110011-2210011-2211011-2211111-2211112-2221112
8	1110001-2110001-2210001-2210011-2211011-2211111-2211112-2221112
11_{up}	1110001-2110001-2110011-2210011-2211011-2211012-2211112-2221112
12	1110001-2110001-2210001-2210011-2211011-2211012-2211112-2221112
14_{up}	1110001-2110001-2210001-2210011-2210012-2211012-2211112-2221112
15	1110001-2110001-2210001-2210011-2211011-2211012-2221012-2221112
16	1110001-2110001-2210001-2210011-2210012-2211012-2221012-2221112

applied. Selected switching sequences for the new sub-sectors from Fig. 4.31 are given in Table 4.9

4.3.8 SIMULATION AND EXPERIMENTAL RESULTS

Simulation and experimental results for the original and the modified seven-phase three-level SVPWM algorithm are given in this sub-section. As in sub-section 4.2.8 for five-phase case, only a basic analysis related to the comparison of simulations and experiments and to confirmation of proper functioning of the modulation methods is given. Detailed mutual comparison of these results, as well as the comparison with the other modulation strategies, is postponed for Chapter 6.

Models for original and modified algorithms have been developed in Matlab/Simulink and the circuit part is realised again using PLECS block-set package. For the experimental purposes, the same Matlab/Simulink developed modulator block has been run on the real-time hardware dSpace ds1006. The algorithm steps for the seven-phase are more involved than for the five-phase case but the final models of the modulators are very similar. Developed model is again of the general structure which is given in the following section 4.4, where generalisation of the VSD space vector algorithms is discussed. The main difference in the realised models is in the memory requirements. So, for the original seven-phase three-level algorithm, 18 sequences per sector from Table 4.7, and corresponding 18, pre-calculated, inverted matrices for the switching state application times from (4.10) are stored in the memory. For the modified algorithm the same set of data are stored in memory, but now the number of sub-sectors is 24 and the switching sequences for the first sector are given by Table 4.9. As in the five-phase realisation, memory has been sacrificed for the algorithm speed purposes, so the same data for the second sector are also saved in the memory. The switching sequences for the second sector for both algorithms are obtained in the standard way: by application of RoR operation, but now for four places, to each switching

state; by replacing 0, 1 and 2 with 2, 1 and 0 respectively (see Fig. 4.7 but now n=7); and by changing direction of application of the switching states. Corresponding inverted matrices from (4.10) for the second sector for 18, i.e. 24, sub-sectors for two developed algorithms, are also stored. Sub-sector determination for the original algorithm is realised as explained in sub-section 4.3.6, by using data from Table 4.8. For the modified algorithm additional condition $\theta<\pi/14$ has also to be examined.

The same custom made inverter units with up to six phases have been used for the experimental verification of the realised algorithms. For obtaining seven phases, two inverter units have been connected in parallel, i.e. positive, negative and middle-point dc-bus rails of both inverters were connected each one to the other, providing in this way up to 12-phase three-level NPC inverter. For the control of the inverters real-time hardware dSpace ds1006 was used. Because of the lack a of seven-phase machine static R–L load has been used for the experimental verification. Value of the dc-bus voltage was set to V_{dc}=600V and was provided by an external dc supply Sorensen SGI 600/25. Used switching frequency was f_s=2kHz and the inverter dead time 6μs. As in the five-phase case and in the rest of this thesis, V/f=const. Linear modulation region up to the maximum modulation index of 1.0257 [Levi et al. (2008)] was analysed. One can see that, when possible, used values are the same as for the five-phase case for the sake of comparison. Parameters in the simulations were set to correspond to those used for the experimental verification. NPC inverter was modelled again using IGBT components with zero forward voltage and 10mΩ on-state resistance. Flywheel and clamping diodes are the same as before, and on-state resistance is set to 10mΩ. Parameters for the R–L load are estimated from the phase voltage and current fundamental magnitude and angle values from the test experiment, and are assumed to be constant for a certain modulation index. These values are given in Table A.2 in Appendix A.

Original algorithm

Simulation and experimental results, for modulation indices 0.4 and 1, for the original seven-phase SVPWM algorithm are shown side by side in Fig. 4.32 and Fig. 4.33, respectively. The original algorithm will be denoted as SVPWM1. Results are shown for the leg voltages, phase voltages, CMV and the phase currents. Time waveforms and frequency spectra are given. Again, as in the previous section, common mode voltage is referred to the negative dc-bus rail, thus dc component of $V_{dc}/2$ is present. The same Matalb programme for processing the data (so that leg voltage fundamental angle is zero) was used. Oscilloscope screenshots with the leg, phase voltages and current for the phase a, for modulation indices of 0.4, 0.6, 0.8 and 1, are shown in Fig. 4.34.

Simulation and experimental results are in very good agreement, as is evident from Fig. 4.32 and Fig. 4.33. The required phase voltage fundamental value was achieved, and the first significant harmonics appear around the switching frequency. This confirms proper functioning of the algorithm. Slightly lower fundamental voltages than expected (for m=0.4, $0.4\cdot300/\sqrt{2}$=84.85Vrms, and for m=1, $300/\sqrt{2}$=212.13Vrms), are the consequence of the relatively high value of the dead time of 6μs, which in the seven-phase case becomes more pronounced. Also, because the voltage drop on the IGBTs was neglected in the simulations, the fundamental components obtained by experiments are slightly lower.

The different shape of the phase voltage for low modulation index m=0.4 (Fig. 4.32b) and for high modulation index m=1 (Fig. 4.33b) is obvious. Namely, looking at the phase voltages one can say that for m=0.4 the inverter has two-level like performance, and the obtained phase voltage has 13 levels. This corresponds to the maximum number of the phase voltage levels obtainable with the seven-phase two-level inverter (n=7, l=2), see

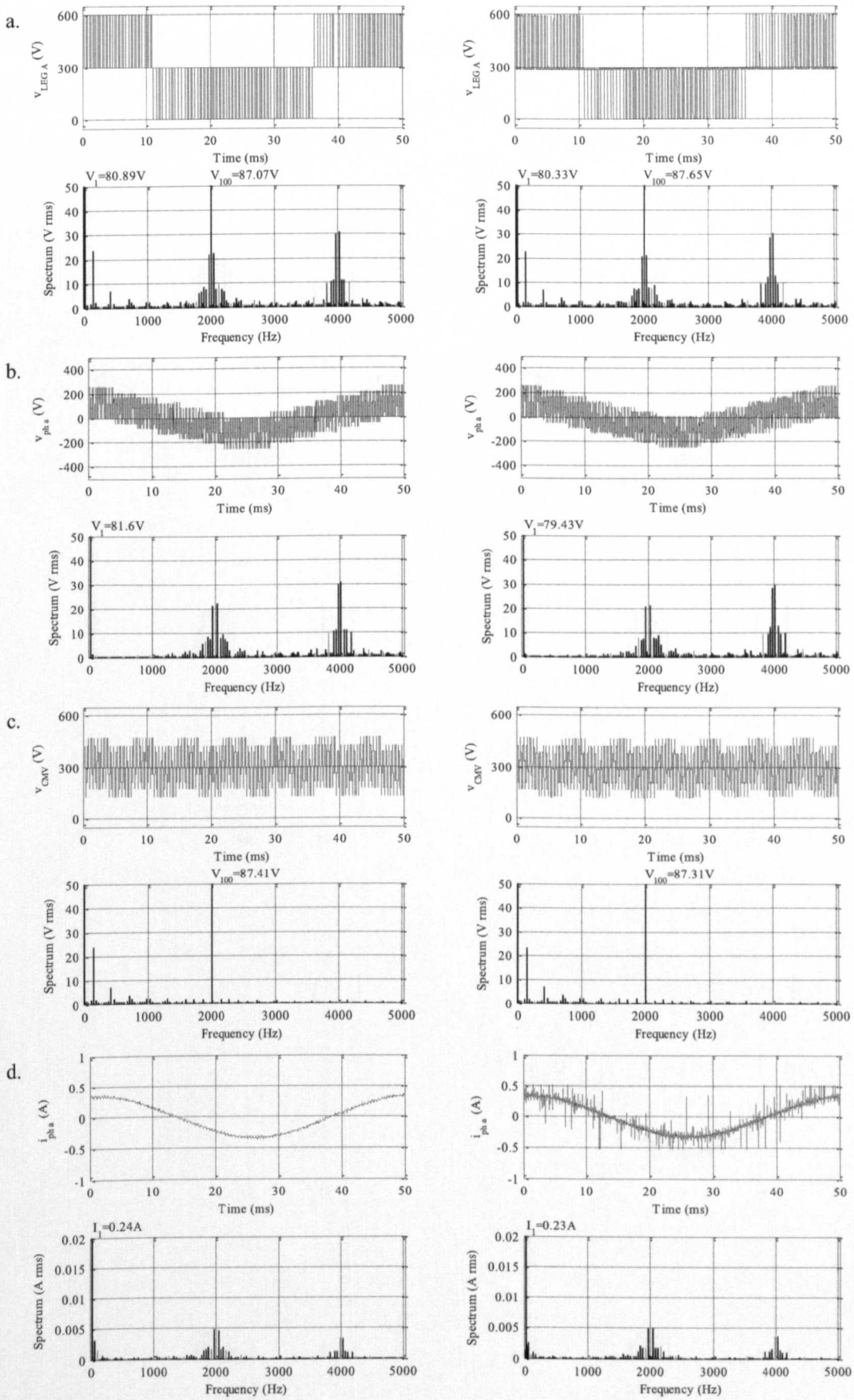


Fig. 4.32: Simulation (left column) and experimental (right column) results for the original seven-phase three-level SVPWM method. a. Leg *A* voltage, b. phase *a* voltage, c. CMV, d. phase *a* current, with associated spectra. Results are for the modulation index m=0.4 (SVPWM1, n=7, l=3).

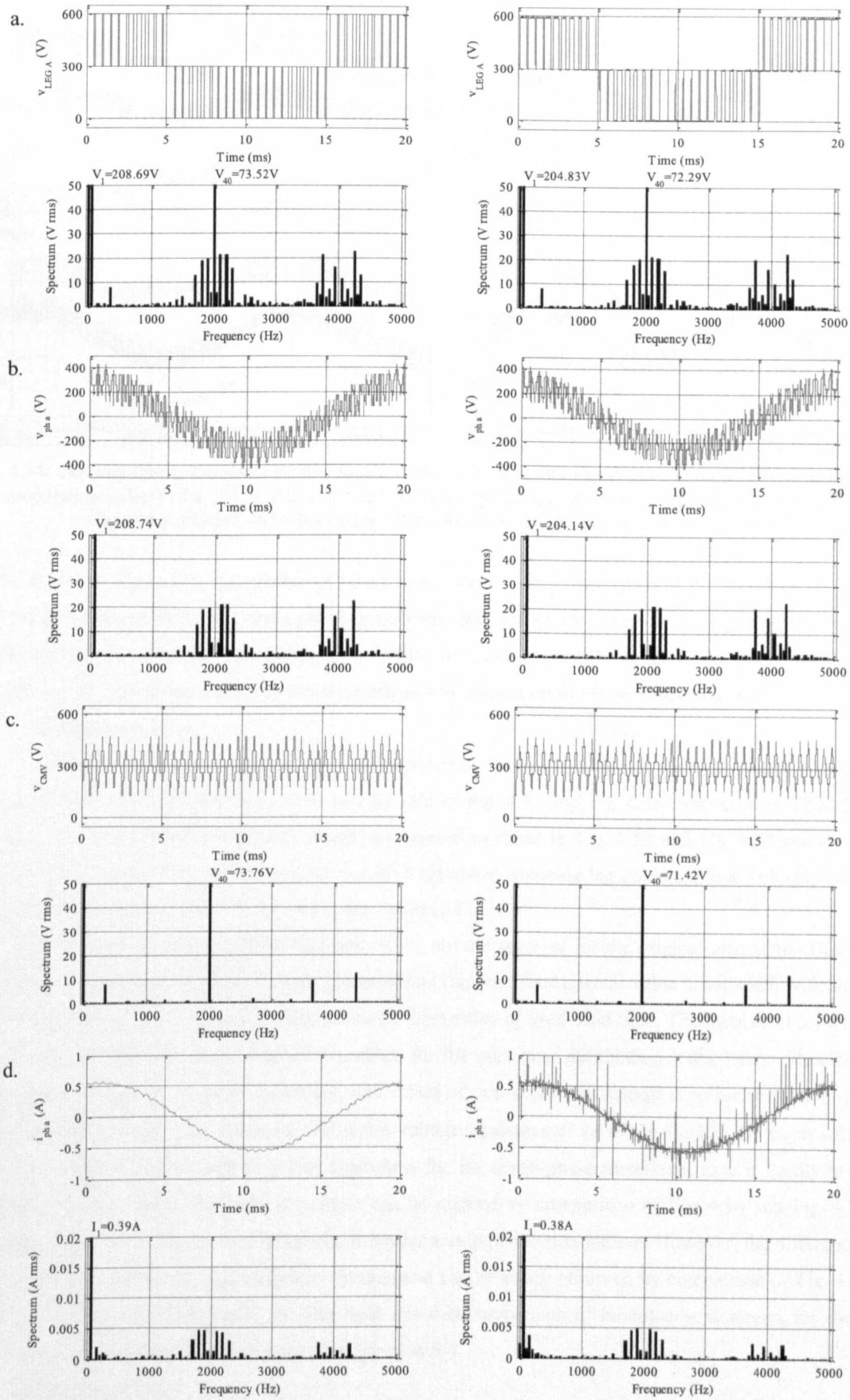


Fig. 4.33: Simulation (left column) and experimental (right column) results for the original seven-phase three-level SVPWM method. a. Leg *A* voltage, b. phase *a* voltage, c. CMV, d. phase *a* current, with associated spectra. Results are for the modulation index m=1 (SVPWM1, n=7, l=3).

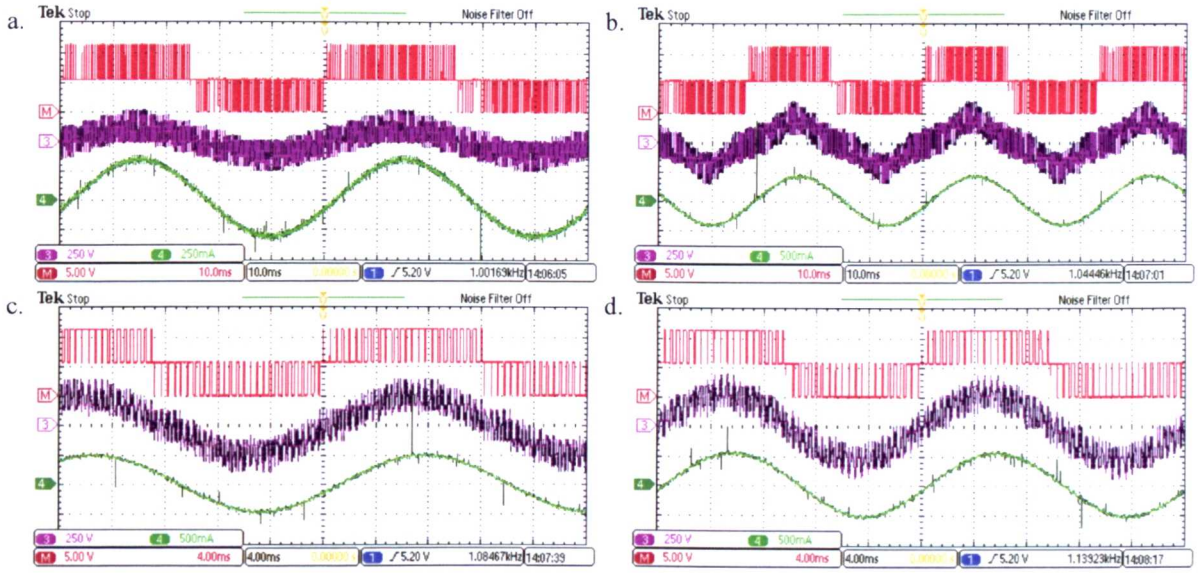


Fig. 4.34: Oscilloscope screenshots for the implemented original seven-phase three-level SVPWM technique for the modulation indices of a. 0.4, b. 0.6, c. 0.8 and d. 1 (M-leg voltage, 260V/div; Ch3-phase voltage, 250V/div; Ch4-phase current, 0.5A/div; time=10ms/div for a. and b., i.e. 4ms/div for c. and d.).

(3.15). For m=1, Fig. 4.33b, the number of levels in the phase voltage waveform is 21, and does not reach the theoretical maximum of 25 for seven-phase three-level case, see (3.15). The step in a phase voltage/CMV is defined by (3.14) and for the used values of V_{dc}=600V, n=7, l=3 amounts to 42.857V. As mentioned, the step is the same for all modulation indices as can be confirmed by inspection of Fig. 4.32 and Fig. 4.33.

Modified algorithm

Simulation and experimental results, for modulation indices 0.4 and 1, for the modified seven-phase three-level SVPWM algorithm are shown side by side in Fig. 4.35 and Fig. 4.36, respectively. This algorithm will be denoted as SVPWM2. Shown results correspond to those in Fig. 4.32 and Fig. 4.33 for the original algorithm. Oscilloscope screenshots for the modified algorithm, showing leg voltage, phase voltage and current, for modulation indices of 0.4, 0.6, 0.8 and 1, are shown in Fig. 4.37.

General conclusions regarding obtained results are the same as for the original algorithm. There are no low-order harmonics in the phase voltage spectrum and required fundamental value is satisfied, with somewhat lower value that is the consequence of the relatively high value of used dead time. The number of levels and the step remains the same as in the original algorithm for the particular modulation index value. Simulation and experimental results are in good agreement, and effect of non-modelled voltage drop on inverter switches is noticeable through somewhat lower leg and phase voltage fundamental value obtained in the experiments. The difference between original and modified algorithms for the seven-phase three-level case is hardly noticeable from time domain traces. The only difference can be noticed by comparison of Fig. 4.34 and Fig. 4.37, in a switching 'gap' that exists in the original algorithm for small modulation indices. However, the differences are a little bit more pronounced in the frequency domain and can be easily observed by comparison of Fig. 4.32 with Fig. 4.35 and Fig. 4.33 with Fig. 4.36. The more detailed comparison of modulation strategies for the seven-phase three-level modulation strategies will be given in 6.4.

THD comparison

For the time being, the initial comparison based on THD/HD calculations using (4.9), will be shown. Simulations and experiments have been done for full linear modulation index range from m=0.05 to 1 with the

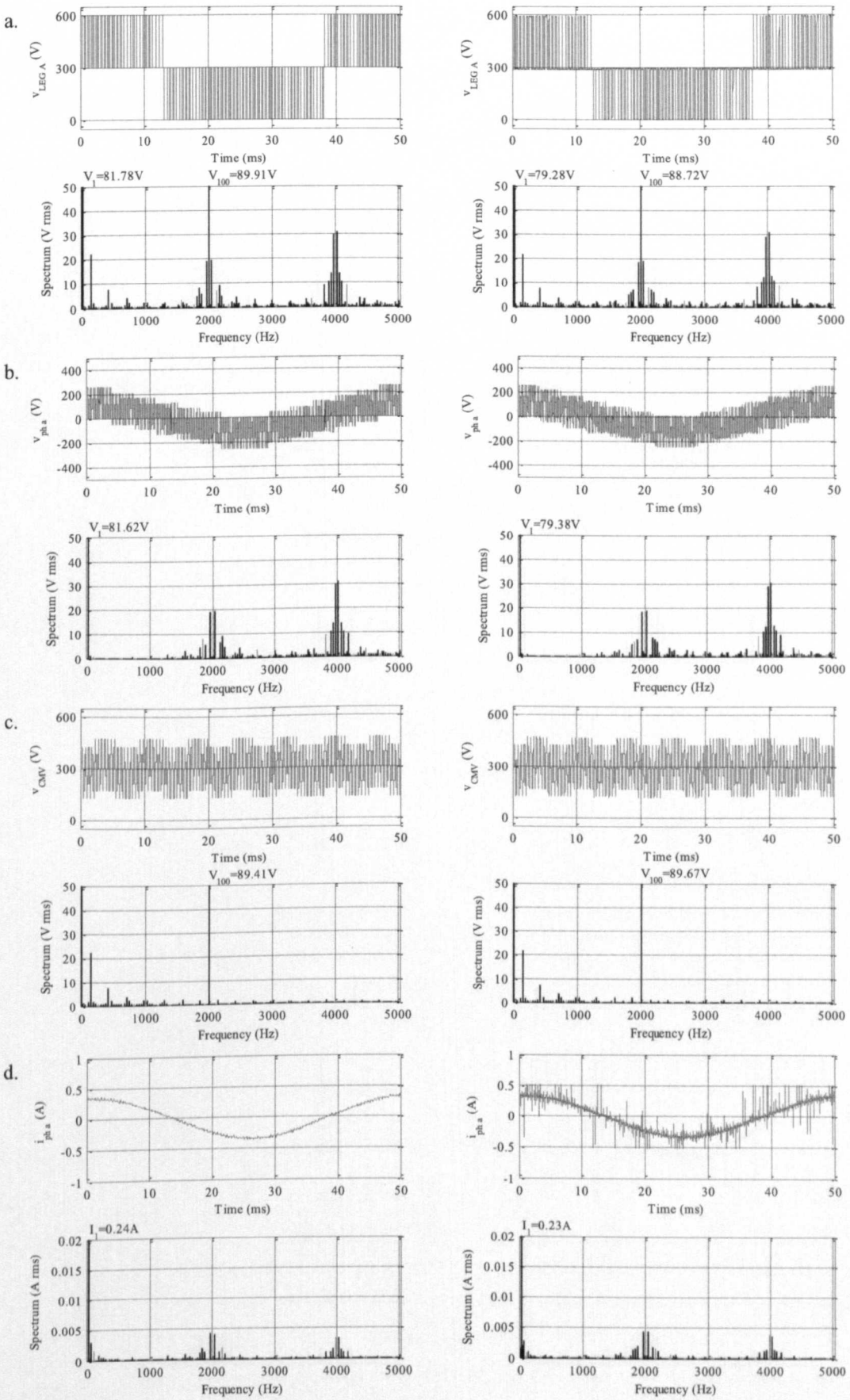


Fig. 4.35: Simulation (left column) and experimental (right column) results for modified seven-phase three-level SVPWM algorithm. a. Leg *A* voltage, b. phase *a* voltage, c. CMV, d. phase *a* current, with associated spectra. Results are for the modulation index m=0.4 (SVPWM2, n=7, l=3).

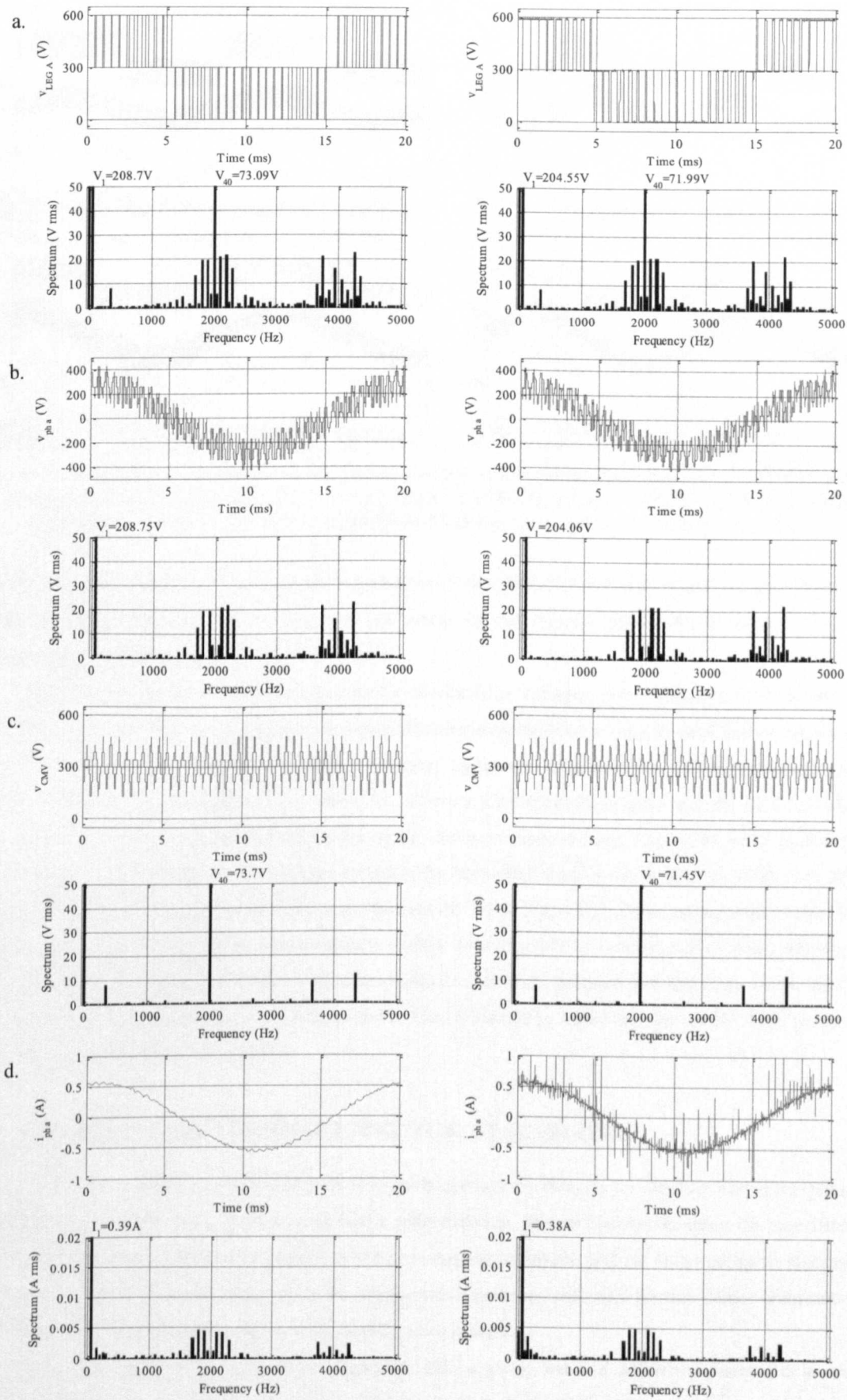


Fig. 4.36: Simulation (left column) and experimental (right column) results for modified seven-phase three-level SVPWM algorithm. a. Leg *A* voltage, b. phase *a* voltage, c. CMV, d. phase *a* current, with associated spectra. Results are for the modulation index m=1 (SVPWM2, n=7, l=3).

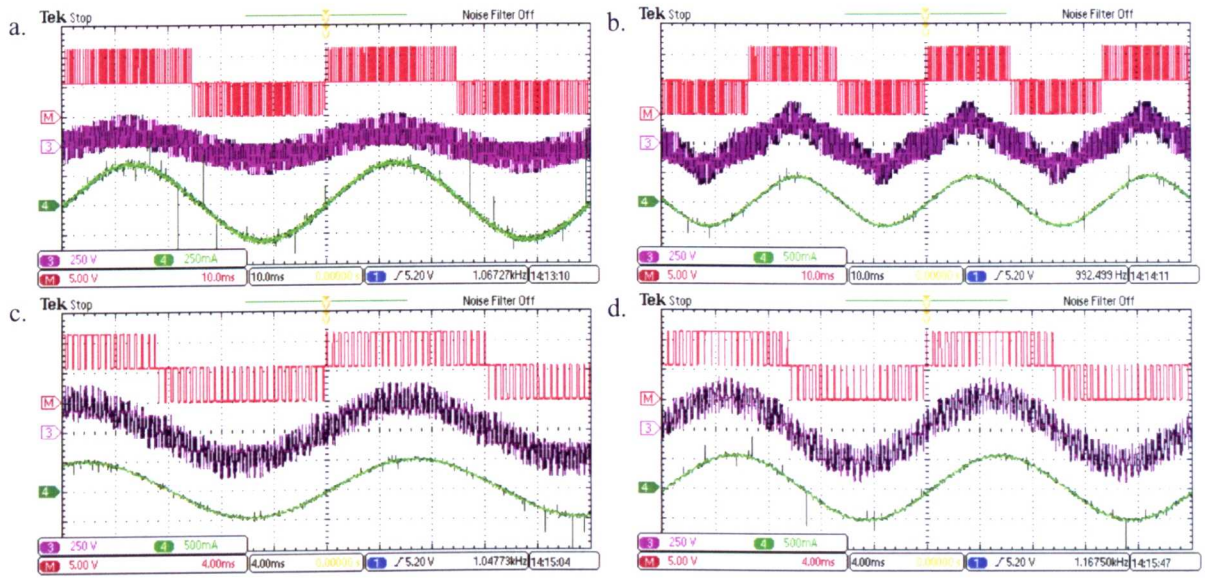


Fig. 4.37: Oscilloscope screenshots for the implemented modified seven-phase three-level SVPWM technique for the modulation indices of a. 0.4, b. 0.6, c. 0.8 and d. 1 (M-leg voltage, 260V/div; Ch3-phase voltage, 250V/div; Ch4-phase current, 0.5A/div; time=10ms/div for a. and b. i.e., 4ms/div for c. and d.).

step of 0.05, and additionally for maximum modulation index of 1.025, for both examined algorithms. So, the results shown in Fig. 4.32 to Fig. 4.37 are just some of the representative data from the whole set of measurements and simulations that have been done.

THD curves versus modulation index m, for obtained leg voltages, phase voltages, and currents, as well as the HD of the common mode voltage, for simulation and experimental results for both presented seven-phase SVPWM strategies, are shown in Fig. 4.38. Very good agreement of simulation and experimental results for voltage THD/HD characteristics is clear. Also, the difference between the original and the modified algorithm, which in the five-phase case was noticeable for leg i.e. common mode voltage, Fig. 4.24a and c, is now reduced, Fig. 4.38a and c. THD of the phase voltages produced by both algorithms is identical, Fig. 4.38b. The difference between modulation strategies is obvious from the current THD, Fig. 4.38d. Some unexpected behaviour at the low modulation indices during the experiments is visible. This could be a consequence of using non-linear load, see Appendix A. However, for modulation indices greater than 0.25, position and the shape of the curves from simulations and experiments are in good agreement. Also, it should be noted that the current THD is restricted to a very narrow range, from 0.02 to 0.07.

4.4 GENERALISED VSD SPACE VECTOR ALGORITHM

One can see that the algorithm presented in the previous two sections for the five- and seven-phase three-level case can be generalised. It is obvious that a generalisation, and an attempt to apply the algorithm to any other case with a higher number of phases, or a higher number of levels, will be followed by an increase of the pre-processing cost. However, once when the appropriate sequences and rules for sub-sector determination are established, the implementation will be only slightly more complex.

Here, once again all the steps of the algorithm will be given, but in a different manner. Let us recall that the aim of the algorithm is to produce sinusoidal phase voltages in the symmetrical star-connected machine with sinusoidally distributed windings. The machine is supplied from a voltage source inverter of the diode-clamped

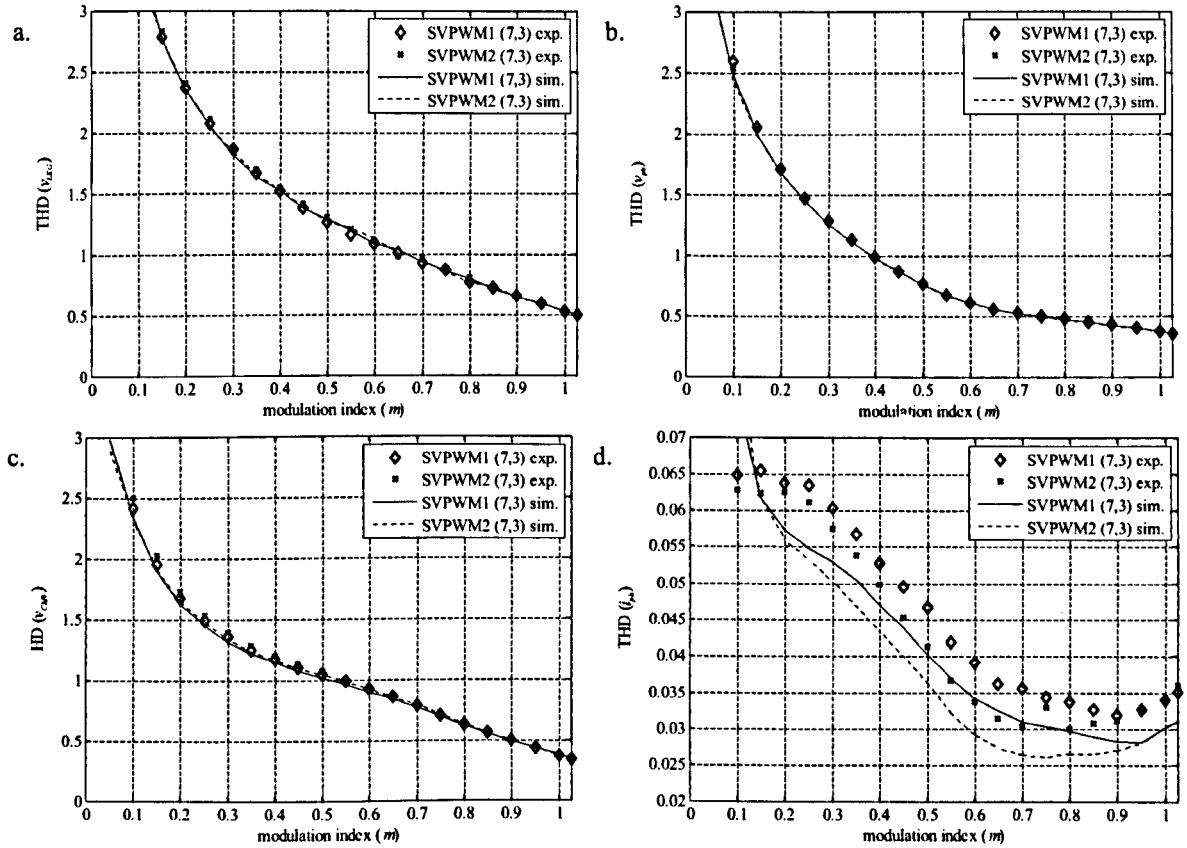


Fig. 4.38: Simulation and experimental results for original (SVPWM1) and modified (SVPWM2) algorithm for the a. leg voltage THD, b. phase voltage THD, c. CMV HD and d. phase current THD (n=7, l=3).

structure. Let us assume that the number of phases of the inverter is n, and that the number of levels is l. The steps of the algorithm are as follows:

1) First, order-per-sector law should be established, regarding desired phase voltages in the time domain.
2) Further, switching states whose projections into the α-β plane have an angle in the range $0 \leq \theta \leq \pi/n$, should be extracted.
3) From switching states of step 2), those switching states that follow the ordering for the first sector from 1) are the useful switching states – switching states after order-per-sector law application.
4) From the useful switching states of step 3), choose those that do not contain maximum level, l–1. These switching states are the possible starts of the switching sequences.
5) Create all possible (n!) permutations of one-level transitions, and apply all of them to each of the possible starting switching states. If each switching state belongs to the set of the useful switching states, regard that sequence as a possible sequence.
6) If all the switching state projections of the possible switching sequences are the same, then those switching sequences are redundant. Group redundant switching sequences together. They correspond to the same pattern.
7) For desired reference voltages and for each pattern of step 6), examine equation (3.51) (with increasing values for the reference amplitude and angle) in the whole region ($0 \leq \theta \leq 2\pi$, $0 \leq m \leq m_{max}$), and check if the constraint that all dwell times are in the range from 0 to T_s is satisfied. If the solution

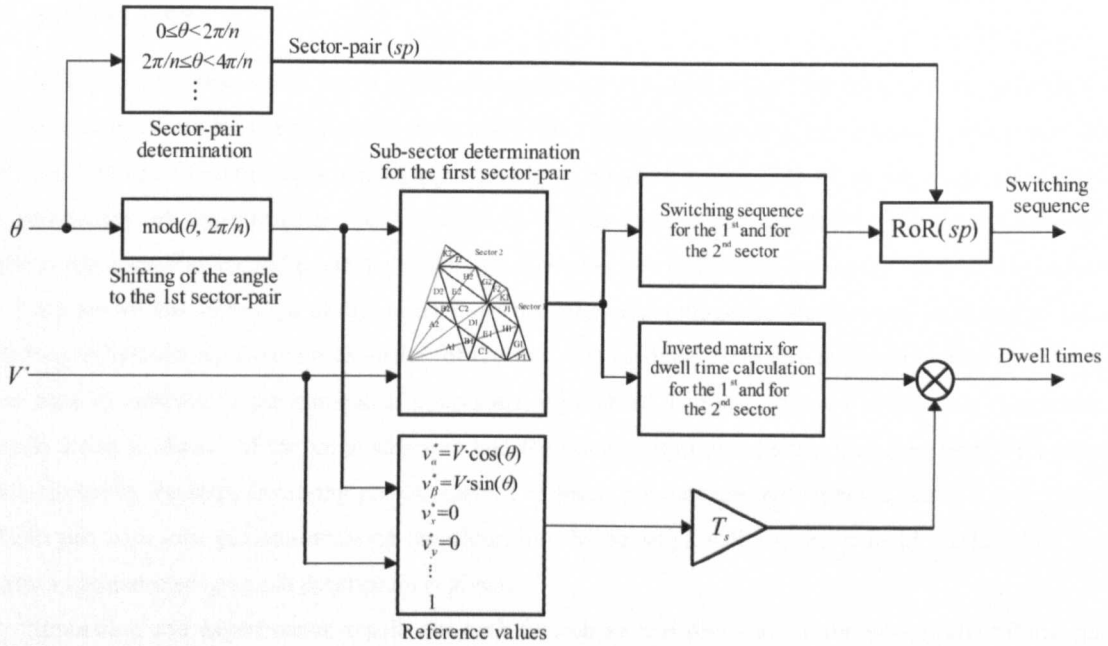


Fig. 4.39: Implementation structure block diagram for the SVPWM method based on the VSD approach in a general case.

does not exist, that means that the pattern cannot produce desired phase voltage, i.e. if desired phase voltages are pure sinusoidal, it cannot provide zero value in the *x-y* planes. Values $m=m(\theta)$, determine regions of applicability for each pattern – i.e. sub-sectors.

8) For each pattern that has a solution in the step 7), calculate the inverse matrix from (3.51) and store it.

9) In NPC inverters with more than three levels capacitor balancing is not possible just by the modulation technique [Akagi (2011)]. But, if the aim of optimisation is e.g. to produce the CMV around $V_{dc}/2$, from redundant sequences, for patterns determined in step 7), choose those that contain more $(l-1)/2$ states, for odd l, i.e. more $l/2$ and $l/2-1$ states for even l.

10) Using data for sub-sector borders from the step 7), applying some geometry, a table similar to Table 4.4 and Table 4.8, with rules for sub-sector determination, should be constructed.

11) When sequences from the step 9) and inverted matrices from the step 8) are determined, and when logic for sub-sector determination from the step 10) is established, implementation of the algorithm is simple and always of the same structure, as shown in Fig. 4.39. Shown structure stores data for the first two sectors and it increases memory usage, but reduces computational costs, as already explained for the five-phase case in sub-section 4.2.6, and also applied for the seven-phase algorithm realisation.

Given steps are aimed at an actual implementation, but in a few steps manual manipulations are required. Note that the presented algorithm can be also easily applied to other topologies. The only step that depends on the inverter structure is the choice of the switching sequence from the redundant sequences for a pattern. The redundant switching sequences have different mean value, so they produce different CMV. Also, with an arbitrary choice of the redundant switching sequences, losses can be increased and capacitor voltage balancing can be disturbed.

4.5 SUMMARY

In this chapter, four space vector modulation techniques, based on the VSD approach, are presented. The first two techniques are for the five-phase three-level NPC voltage source inverter with sinusoidal phase voltage references. The first of them was originally presented by [Gao and Fletcher (2010)]; in this chapter it is reviewed with introduction of some original specific solutions for the steps of the algorithm. One modification of that algorithm represents the second presented technique. The next two techniques are for the seven-phase three-level case. They are for the same type of the inverter and the reference voltages as the first two presented techniques. These two techniques represent an extension of the first two methods from five to seven phases. Problems that appear with an increase of the number of phases are highlighted, and solutions are given. It is shown that the implementation is always of the same structure and the complexity only slightly increases with the number of phases. However, the steps involving pre-calculation of necessary data are quite tedious, and a significant effort has been put here into generalisation of the algorithm. Some steps still require manual work, while for the majority a computer programme description is given.

Simulation and experimental results for both five-phase and seven-phase three-level algorithms, for the original and for the modified version, are given. Given results are aimed to show proper functioning of the algorithms and to compare simulation and experimental results, while mutual comparison and comparison with some of the carrier-based techniques that will be introduced in Chapter 5 will be given in Chapter 6.

Chapter 5

MULTILEVEL MULTIPHASE CARRIER-BASED PWM

5.1 INTRODUCTION

Analysis of carrier-based PWM techniques is very important and very useful, since it is the simplest for implementation. Hence, it can be used as the reference algorithm for comparison and for quality evaluation of any other modulation technique. CBPWM techniques for multilevel inverters for single-leg case are covered in detail in [Holmes and Lipo (2003)]. The analytical comparison of spectra for different carrier dispositions is given there. The aim of this chapter is rather different. It will start with the basics, such as the concept of forming the PWM signals using carrier-based approach as the simplest solution, and it will highlight some facts that will be the base for comparison of this method with the SVPWM approach.

The goal throughout this project is to generate sinusoidal (single-frequency) output voltage signals. However, it is important to note that, if multi-frequency output voltage is required, as in certain applications the case may be [Levi (2008)], this is a straightforward task with carrier-based methods. It is only necessary to modify the modulating signals in accordance with the required output voltage.

In this chapter, due to the similarities between different triangular carrier-based techniques, and already established advantage to produce minimum THD in the phase voltage [Carrara et al. (1992)], the emphasis is on the level-shifted carrier-based technique, and on the symmetrical sampling. Particularly, only the PD-PWM will be analysed. The reason why this disposition is chosen is explained. For the sake of explanation, a three-level five-phase inverter is subjected to analysis and sampled reference leg voltages for symmetrical sinusoidal output are shown in Fig. 5.1. However, generalisation to any number of levels and any number of phases is also given.

At first, pure sinusoidal references are considered in section 5.2. Using this as an example, the choice of the carrier-based disposition is explained. One method for reduction of the multicarrier PD-PWM to the single-carrier PWM, as well as an explanation of the switching sequences and their change in time domain, are given next. Further, in section 5.3, min-max injection is explained as a natural solution for linear modulation index range extension. Change of the switching sequences is explained and double min-max injection is introduced. Simulation and experimental results, that use introduced carrier-based techniques, are given in Chapter 6 where they are compared with previously explained SVPWM techniques. Original material from this chapter has been published in [Dordevic et al. (2011a), Dordevic et al. (2013a)].

5.2 PURE SINUSOIDAL REFERENCES

Desired phase voltages are symmetrical sinusoidal signals. Due to the pure sinusoidal references, it is assumed that the only injection that produces reference leg voltages from the reference phase voltages is the dc value of $V_{dc}/2$. So, in a general case, pure sinusoidal desired leg voltages are defined as:

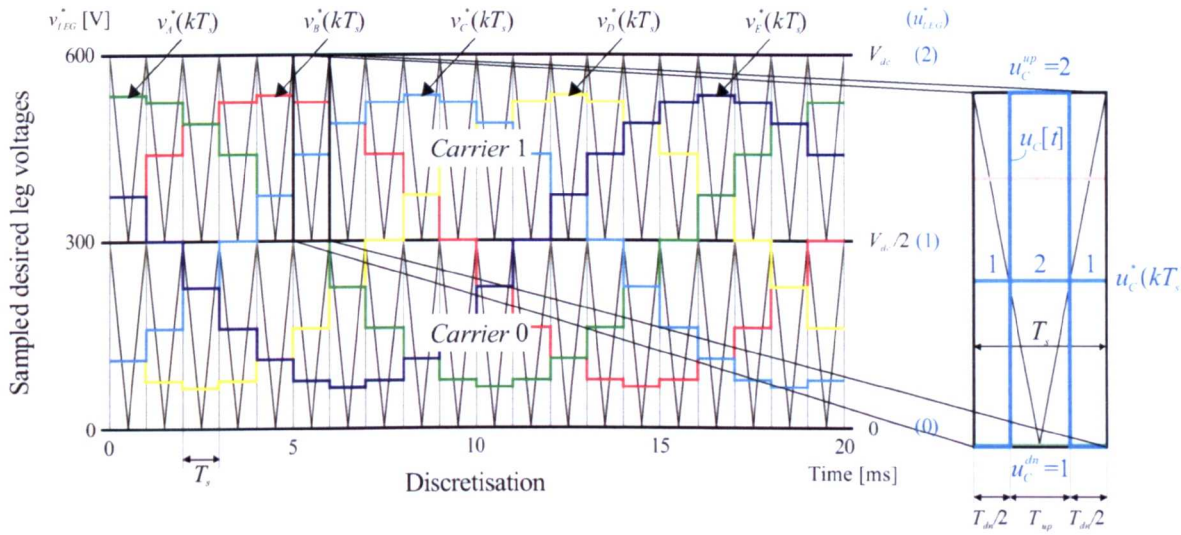


Fig. 5.1: Sampled desired leg voltages for a five-phase machine supplied from a three-level inverter. Highlighted segment on the right-hand side explains the process of averaging.

$$v^*_{LEG}(t) = V^* \cdot \cos(2\pi ft - 2\pi/n \cdot (k-1)) + V_{dc}/2 \tag{5.1}$$

where V^* and f are the amplitude and the frequency of the desired phase voltages, n is number of phases, and k=1 to n corresponds to the appropriate leg A to N. Dc injection $V_{dc}/2$ is chosen to centre signals between minimum and maximum dc-bus voltage. In the five-phase three-level example in Fig. 5.1 desired leg voltages are sinusoidal. Dc bus voltage in this example is 600V, so that dc injection is equal to $V_{dc}/2$=300V. Signal amplitude and frequency are 240V/50Hz. Switching frequency is 1kHz and peak-to-peak values of level-shifted carriers are 300V.

In an inverter, process of digitalisation takes place, as already mentioned in 3.2. This will be now explained in more detail in the case of CBPWM. Digitalisation occurs in two parts, discretisation and quantisation. Discretisation is defined by the sampling time (switching period) T_s, while quantisation refers to mapping of the discrete (sampled) signal values to the quantisation level set (digital values). Vertical lines at T_s distance (Fig. 5.1) represent process of discretisation when samples of the continuous reference leg voltage signal $v^*_{LEG}(t)$ are taken. Samples $v^*_{LEG}(kT_s)$ are taken at the beginning and held at the same value during T_s. This type of sampling is called symmetrical sampling [Holmes and Lipo (2003)]. Under the process of quantisation one usually means that signal magnitude range is divided into certain sectors and that signal values map into the value adopted for the sector to which it belongs. New set of values contains quantisation levels, i.e. digitalised values. Set of digitalised values is defined with the number of levels of the inverter. In an inverter, process of quantisation has to be executed with an extra requirement. Namely, the average value during the switching period, of digitalised values of the signal $v_{LEG}[t]$, must be equal to the value of the sampled signal, $v^*_{LEG}(kT_s)$, in that switching period. This means that if the value of a sample is not exactly equal to any of the digital values from the set, which is almost always the case, then more than one digital value must be used during the sampling period, T_s, to form output leg voltage, $v_{LEG}[t]$. Process of quantisation, with signal averaging in each switching period, can be easily explained graphically by considering one segment. Let us assume that the desired leg voltage signal in blue is selected in the highlighted segment in Fig. 5.1 ($v^*_C(kT_s)$, i.e. $u^*_C(kT_s)$, in normalised form (3.1)). The aim of the process of averaging is to reach on average, during the switching period, desired value of

the sampled reference leg voltage ($u^*_{LEG}(kT_s)$), applying for certain time intervals the nearest digitalised levels of the voltage (u^{dn}_{LEG} and u^{up}_{LEG}). In the highlighted case in Fig. 5.1 u^{dn}_C=1 and u^{up}_C=2, i.e. in non-normalised form $V_{dc}/2$ and V_{dc}, respectively. Only the nearest levels are applied since this will produce minimum dv/dt and minimum losses, as will be discussed in detail in 7.4.

Averaging equation in terms of the normalised voltage values is given with:

$$u^{dn}_{LEG} \cdot T_{dn} + u^{up}_{LEG} \cdot T_{up} = u^*_{LEG}(kT_s) \cdot T_s \tag{5.2}$$

The easiest way to satisfy equation (5.2) is to compare reference value ($u^*_{LEG}(kT_s)$) with the saw-tooth signal that is increasing during the whole switching period from u^{dn}_{LEG} to u^{up}_{LEG}, and to apply each higher and lower voltage level proportionally to the reference signal level inside saw-tooth band. In other words, using simple geometry (similarity of triangles), that means that output leg voltage should be set to the value u^{up}_{LEG} when the signal is greater than the saw-tooth and to the u^{dn}_{LEG} when it is below. This principle of quantisation with averaging requirement produces square wave signals that contain two digital values in each switching period.

This saw-tooth carrier signal suffers from simultaneous multiple switching transitions at the beginning (end) of the switching period if there is more than one reference signal in the same segment, which, in general, a very common case is (and this is the case in the highlighted segment in Fig. 5.1). Therefore, symmetrical triangular carrier (already shown in Fig. 5.1) is applied instead, to avoid this problem. Value of the triangular carrier is the same at the beginning and at the end of T_s period, so that there is no undesired effect. Process of averaging with triangular carrier is again as in the equation (5.2). The shape of the obtained pulsed leg voltage, for the chosen leg C ($u_C[t]$), is shown in the highlighted segment, Fig. 5.1.

It is chosen here that the triangular carrier starts from its maximum value at the beginning of the switching period (Fig. 5.1). Another situation is possible, when carrier starts from its minimum at the beginning of the switching period; it gives the same results in terms of averaging. The difference is the following: in the former case, at the beginning of the switching period, output level is always u^{dn}_{LEG}, in the middle its value is u^{up}_{LEG}, and at the end it is the same as in the beginning, while in the latter case it is the other way round. That means that in the first case levels are increasing in the first half of the switching period, and are decreasing in the second half. It is the other way round in the latter case. Also, it is possible that different types of carriers are applied in different carrier bands. According to that, level-shifted carrier dispositions can be classified into in-phase disposition, PD, phase opposition disposition POD, and alternative phase opposition disposition APOD-PWM [Carrara et al. (1992)]. PD case is shown in Fig. 5.1, and it will be used in this thesis for easier comparison with the space vector strategies. It should be noted that phase shifted carrier disposition is also commonly in use.

5.2.1 CHOICE OF THE CARRIER DISPOSITION

One of the aims of this research is a comparison of carrier-based and space vector modulation strategies. Theoretical part of that comparison will be started in sub-sections 5.2.3 and 5.3.1 and finalised in section 6.2. This analysis is based on the comparison of the position of change of the switching sequence. The second part represents the comparison of the obtained waveforms by different carrier-based and space vector modulation strategies and is given in Chapter 6 in sections 6.3 and 6.4. The comparison of space vector and carrier-based PWM methods is important, since it reveals similarities and differences, thus enabling the selection of the best technique for a given application. Choice of the PD-PWM is good for comparison with the space vector strategies for NPC topology and has already been used in three-phase case related comparisons in [Wang (2002),

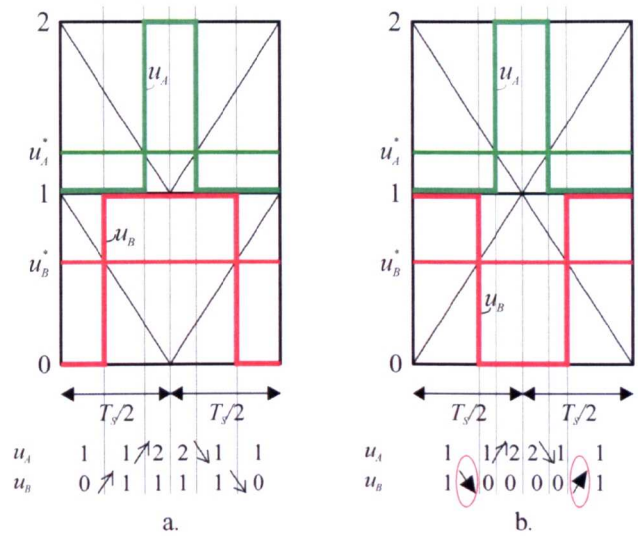


Fig. 5.2: Choice of CBPWM that is suitable for comparison with SVPWM techniques: a. PD-PWM. b. POD and APOD for three-level case.

McGrath et al. (2003)]. Superiority of the PD-PWM, compared to the other modulation strategies, in terms of produced phase voltage spectrum, has been shown in [Carrara et al. (1992)]. However, the actual reason why PD-PWM is the most suitable for comparison with SVPWM is the following. During the construction of the space vector sequence it is normally assumed that each leg increases (decreases) its level during the first half-period of the switching period T_s, and then each leg decreases (increases) its level in the second half-period. For the same reasons as for the carrier-based strategies, increase and decrease are usually for one level. Let us now consider the mentioned multilevel carrier dispositions PD, POD, and APOD. It is enough to look at the three-level case, and for the sake of clarity, only two phases (legs) are shown in Fig. 5.2. For the three-level case APOD and POD are identical (that does not affect the generality of the example). One can see that the only method in which all legs always change its level in the same direction (all increase or all decrease their level) in each half-period of the switching period is PD, Fig. 5.2a. Thus, this is the actual reason why PD-PWM is the most suitable carrier-based PWM strategy for comparison with SVPWM methods for the NPC VSI topology. This is also why only PD-PWM is analysed in this chapter.

5.2.2 REDUCTION OF PD-PWM TO A SINGLE-CARRIER PWM

Let us introduce notation for the carriers. If the carrier is in the range 0 to 1, it will be denoted as *Carrier* 0, if it is in between 1 and 2, it is the *Carrier* 1, etc. In a general case there are l–1 level-shifted carriers. Note that, in this notation, digital value of the leg output u_{LEG}^{dn} is equal to the carrier number, while u_{LEG}^{up} is greater by one:

$$\begin{aligned} u_{LEG}^{dn} &= Carrier^{No} \\ u_{LEG}^{up} &= Carrier^{No} + 1 \end{aligned} \tag{5.3}$$

Substituting (5.3) into averaging equation (5.2), taking into account that $T_s=T_{up}+T_{dn}$ (Fig. 5.1), and after dividing both sides of the equation with T_s, one gets:

$$Carrier^{No} + \frac{T_{up}}{T_s} = u_{LEG}^*(kT_s) \tag{5.4}$$

From this equation T_{up}, which in the chosen solution should be symmetrically applied in the middle of the switching period, can be easily expressed. It should be noted that moving $Carrier^{No}$ value to the right-hand side of (5.4) corresponds to shifting of all the voltage levels to the lowest level, i.e. multilevel (multicarrier) system is reduced to a two-level system. Also, if all carriers are in phase, as in PD-PWM, then all of them will overlap in the reduced two-level system, and hence can be replaced by a single carrier. The difference $u^*_{LEG}(kT_s)$–$Carrier^{No}$ is denoted with $\breve{u}^*_{LEG}(kT_s)$, and it represents the normalised value of the discretised reference leg voltage moved to the lowest carrier band (this value is in the range 0 to 1). Normalised value of T_{up} time can then be given with:

$$\delta_{up} = \frac{T_{up}}{T_s} = u^*_{LEG}(kT_s) - Carrier^{No} = \breve{u}^*_{LEG}(kT_s) \tag{5.5}$$

Explained reduction of the three-level PD-PWM system of Fig. 5.1 to the two-level system with a single-carrier is shown in Fig. 5.3. It can be seen that this reduction is general and can be applied to any number of levels and any number of phases. After comparison with the single-carrier in *Carrier* 0 band, produced square-wave output $\breve{u}^*_{LEG}[t]$, when increased for the corresponding $Carrier^{No}$ value, represents normalised output leg voltage $u_{LEG}[t]$.

Previous explanation of the reduction of the PD carrier-based modulation to the single-carrier band was graphical. This principle has been explained in a simple manner, mathematically, in [McGrath et al. (2003)]. Hence, introduced notation will be adapted from graphical to numerical interpretation. For example, $Carrier^{No}$ in numerical interpretation represents integer value of the normalised discrete value of $u^*_{LEG}(kT_s)$, and can be denoted as $u^*_{LEG,\,\mathrm{int}}(kT_s)$. Also, the value of $\breve{u}^*_{LEG}(kT_s)$ represents fractional part of the numerical value of $u^*_{LEG}(kT_s)$, and can be denoted as $u^*_{LEG,f}(kT_s)$. Integer part can be found using *integer* or *floor* function that rounds to the first integer value toward minus infinity, while fractional part can be obtained using modulus function (mod(x,1)), or by subtraction of the integer part from the sampled value:

$$\begin{aligned} u^*_{LEG,f}(kT_s) &= u^*_{LEG}(kT_s) - \lfloor u^*_{LEG}(kT_s) \rfloor \\ &= u^*_{LEG}(kT_s) - u^*_{LEG,\,\mathrm{int}}(kT_s) \\ &= \mathrm{mod}(u^*_{LEG}(kT_s), 1) \end{aligned} \tag{5.6}$$

Using new notation, equation (5.5) can be rewritten as:

$$\delta_{up} = \frac{T_{up}}{T_s} = u^*_{LEG}(kT_s) - u^*_{LEG,\,\mathrm{int}}(kT_s) = u^*_{LEG,f}(kT_s) \tag{5.7}$$

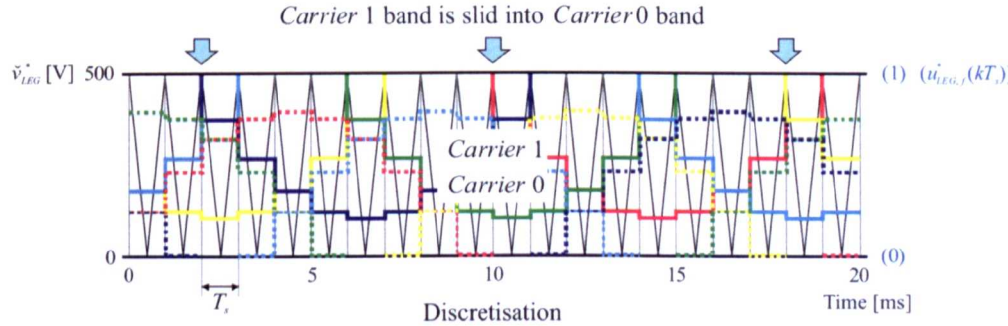


Fig. 5.3: Reduction of the three-level PD-PWM to the two-level system in time domain. Dashed line is for signals from *Carrier* 1 band.

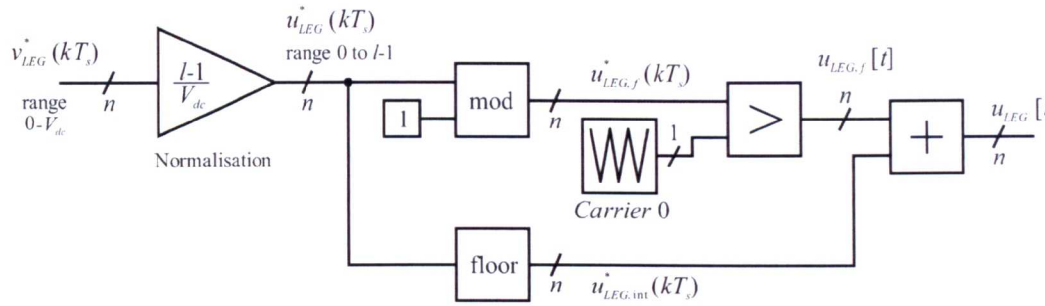


Fig. 5.4: Example of realisation of the multilevel carrier-based PD-PWM using only one carrier.

Equation (5.6) represents mathematical definition of reduction of a multicarrier system to the common carrier band. For production of final outputs, fractional part of the desired leg voltages should be compared with the single carrier. Produced $u_{LEG,f}[t]$ must be further increased for the corresponding integer value $u^*_{LEG,\text{int}}(kT_s)$ to get the final leg output in normalised form, $u_{LEG}[t]$. Block diagram of this process (that can be directly implemented in Simulink) is shown in Fig. 5.4 (note that, according to (5.6), different realisations are possible). Note also that this principle of reduction of the multicarrier to single-carrier system, with all carriers in phase, is universal, and is applicable for any shape of the reference leg voltages.

5.2.3 CHANGING OF SWITCHING SEQUENCE IN TIME DOMAIN

Consider now one segment that contains more than one reference signal (Fig. 5.5). Assume that the segment is in the *Carrier* 0 zone. If PD carrier disposition is considered, generalisation is not lost in this way, since every level can be translated into any other. Assume that there are only two reference voltages, $u^*_{A,f}(kT_s)$ and $u^*_{B,f}(kT_s)$. If $u^*_{A,f}(kT_s)>u^*_{B,f}(kT_s)$, then applied switching states (switching sequence) are: 00, 10, 11, 10, 00 (Fig. 5.5a). Explained symmetry and increase of the level in the first switching half-period should be noted. If voltage $u^*_{A,f}(kT_s)$ has decreasing tendency, and $u^*_{B,f}(kT_s)$ is increasing in time, after the crossover of the two signals the switching sequence will be changed. One switching period when $u^*_{B,f}(kT_s)>u^*_{A,f}(kT_s)$ is shown in Fig. 5.5b. New switching sequence is: 00, 01, 11, 01, 00. From this example it is clear that change of the applied sequence appears when reference voltages change the order in the *Carrier* 0 band. In other words, in a multilevel system with carriers in phase, change of the switching sequence appears when two fractional parts change their

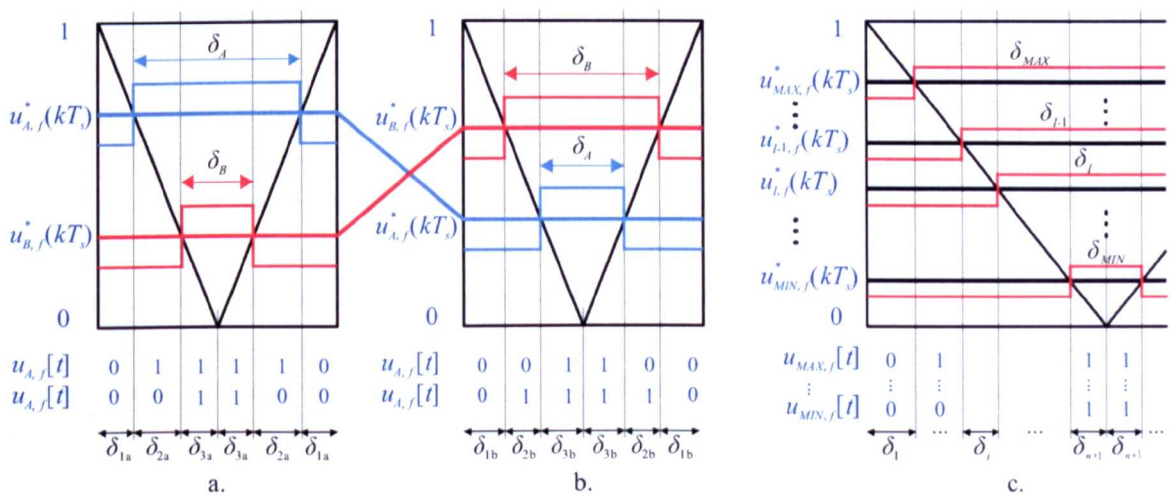


Fig. 5.5: Graphical explanation of: a. and b. change of applied switching sequence, c. switching sequence application time calculation in a general case.

positions. This conclusion will be very important for comparison of carrier-based and space vector modulation techniques.

It is also clear that only the half of the switching period can be considered. Times of application are always defined by (5.7) for each leg. For each switching state dwell times can be easily determined as follows. If T_{up}/T_s of $u^*_{A,f}(kT_s)$ and $u^*_{B,f}(kT_s)$ are denoted with δ_A and δ_B (normalised values), then $\delta_{1a}=(1-\delta_A)/2$, $\delta_{2a}=(\delta_A-\delta_B)/2$, $\delta_{3a}=\delta_B/2$ and $\delta_{1b}=(1-\delta_B)/2$, $\delta_{2b}=(\delta_B-\delta_A)/2$, $\delta_{3b}=\delta_A/2$ (Fig. 5.5a and Fig. 5.5b). Since $u^*_{A,f}(kT_s)$ and $u^*_{B,f}(kT_s)$ have changed places, δ_A and δ_B have changed their positions too in the equations for time calculations. For the general case of an n-phase system, *Carrier* 0 zone and calculation of the switching state application times are shown in Fig. 5.5c (only the first switching half-period is shown). If leg voltages are re-ordered from the one with maximum fractional part value in that switching period to the one with the minimum value, normalised times of switching state applications are given with:

$$\begin{aligned}
&\delta_1 = (1-\delta_{MAX})/2 \\
&\vdots \\
&\delta_i = (\delta_{I-1}-\delta_I)/2, \qquad \text{where } i,I \in (2..n) \\
&\vdots \\
&\delta_{n+1} = \delta_{MIN}/2
\end{aligned} \tag{5.8}$$

Substitution of (5.7) into (5.8) enables rewriting of (5.8) as a function of the voltages:

$$\begin{aligned}
&\delta_1 = (1-u^*_{MAX,f}(kT_s))/2 \\
&\vdots \\
&\delta_i = (u^*_{I-1,f}(kT_s)-u^*_{I,f}(kT_s))/2, \qquad \text{where } i,I \in (2..n) \\
&\vdots \\
&\delta_{n+1} = u^*_{MIN,f}(kT_s)/2
\end{aligned} \tag{5.9}$$

Let us now consider in more detail the fact that the change of order of the fractional parts of reference leg voltages produces change of the switching sequence in a five-phase three-level case. At first, the signals will be observed in a full range without reduction to the single-carrier band. Intersection of the references implies intersection of their fractional parts, so it causes the change of the switching sequence (as in Fig. 5.5a and Fig. 5.5b). In the five-phase case, this produces 10 basic sectors, as shown in Fig. 5.6. Also, as a consequence of the presence of more levels, change of the switching sequence happens each time when transition to another carrier region takes place. In the time instant when reference changes its carrier region, considering it in the lowest *Carrier* 0 zone, value of that reference changes from min 0 (max 1) to max 1 (min 0) value, depending on whether it is moving to the lower or the higher carrier zone. This instantaneous jump of fractional part of a certain leg reference, in *Carrier* 0 region, from 0 to 1 (i.e. 1 to 0) will automatically change position (intersection) with regard to all the other reference fractional parts. The second rule for change of the switching sequence will produce additional division of each sector into two half-sectors, as it is shown in Fig. 5.6.

From Fig. 5.5a and Fig. 5.5b it can be seen that start of both sequences is the same. Start of the sequence remains the same at all times when reference leg voltages do not change their carrier zones (do not change their integer parts, $u^*_{LEG,\,int}(kT_s)$). This means that in that case there is no extra transition (no extra losses) between two switching periods. However, if any leg reference voltage transits to the upper (lower) zone the digital value of that leg will increase (decrease) for 1, and the first switching state of the next switching period sequence will be different. That means that transition from one to the other carrier band produces extra switching in the leg in

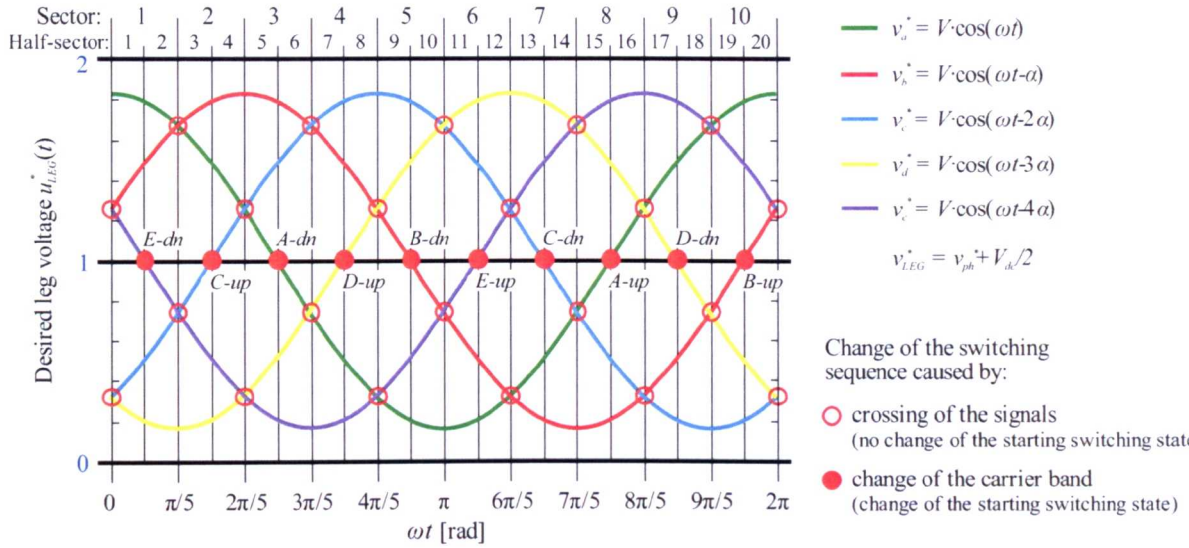


Fig. 5.6: Basic partitioning into sub-sectors, present for any value of the modulation index, for the three-level five-phase case.

which transition has occurred. Positions of these transitions and additional extra switchings are highlighted in Fig. 5.6. For example, label *E-dn* (*E-up*) means that additional switching has occurred in leg *E*, and that it has decreased (increased) its level for one. After change of the carrier band all switching states in the switching sequence will be changed.

One additional conclusion can be derived from Fig. 5.5. Say that example in Fig. 5.5 is a part of a multiphase system, and that legs *A* and *B* are the only legs that changed mutual order of their fractional parts in transition from one to the other switching period, shown in Fig. 5.5a and Fig. 5.5b. The switching sequences before and after will differ only in one switching state, and inside that switching state only the first (corresponding to leg *A*) and the second (corresponding to leg *B*) state will be different. This rule can be generalised for any other two phases which changed mutual order of fractional parts. Looking at Fig. 5.6 one can see that two of these fractional part crossings appear for all modulation index values at the borders between sectors. The starting switching sequence before and after remains the same, but applied sequences before and after will differ in two switching states. Corresponding switching states will differ in positions that correspond to the legs that intersected.

Let us now analyse references reduced to the single-carrier band and the influence of the modulation index value on the change of the applied switching sequence. Firstly, let us try to create a graphical interpretation. The aim is to show when additional intersections of the fractional parts appear in *Carrier* 0 region, with increasing modulation index. One such process is shown through the twelve pictures in Fig. 5.7 for step-by-step increase of the modulation index, *m*, for the three-level five-phase example. For better visibility it is assumed that the signals are continuous, i.e. switching frequency is infinite. Also, because of symmetry, only the first two sectors from Fig. 5.6 are shown.

Modulation index is defined in Chapter 3, equation (3.21). Here it is also given using the normalised values (3.1):

$$m = \frac{V^*}{V_{dc}/2} = \frac{U^*}{(l-1)/2} \tag{5.10}$$

Desired phase voltage is sinusoidal with amplitude V^*. From (5.10) it is clear that the maximum value of the modulation index for symmetrical sinusoidal system, without any harmonic injection, is 1.

Characteristic modulation indices when new switching sequence sets appear are shown in Fig. 5.7b, d, f, h and j (captions of these figures are underlined). The other figures are for indices in between these values. It is very important to find the exact position of the fractional part intersections as a function of the modulation index. These intersection points are labelled in Fig. 5.7 with vertical lines and these vertical lines represent points where new switching sequence takes place. With increase of the modulation index, new vertical lines appear and some disappear, i.e. some new switching sequences appear and some old ones are not in use any more. For example, as modulation index increases from 0 value, the first change of the applied switching sequence appears when yellow, $v^*_{D,f}(kT_s)$, trace touches green, $v^*_{A,f}(kT_s)$, and red, $v^*_{B,f}(kT_s)$, line (Fig. 5.7b). Note that these two intersections happen in different instants of time, but for the same value of the modulation index. The intersection conditions are:

$$\begin{aligned} D-A: &\quad v^*_{D,f}(t_1) = v^*_{A,f}(t_1) \\ D-B: &\quad v^*_{D,f}(t_2) = v^*_{B,f}(t_2) \end{aligned} \tag{5.11}$$

Equations for all these curves are given at the bottom of the Fig. 5.7. Additional numbers in the sub-script represent half-sectors where that equation is valid. Substituting these values into (5.11) one gets:

$$\begin{aligned} D-A: &\quad V\cdot\cos(\omega t_1 - 3\alpha) + V_{dc}/2 = V\cdot\cos(\omega t_1) \\ D-B: &\quad V\cdot\cos(\omega t_2 - 3\alpha) + V_{dc}/2 = V\cdot\cos(\omega t_2 - \alpha) \end{aligned} \tag{5.12}$$

After dividing (5.12) by $V_{dc}/2$, using (5.10), and expressing modulation index m, one gets that correlation between time and modulation index for *D-A* and *D-B* curve crossing is determined by:

$$\begin{aligned} D-A: &\quad m = 1/(\cos(\omega t_1) - \cos(\omega t_1 - 3\alpha)) \\ D-B: &\quad m = 1/(\cos(\omega t_2 - \alpha) - \cos(\omega t_2 - 3\alpha)) \end{aligned} \tag{5.13}$$

Equation (5.13) contains two equations that must be solved separately. It can be seen form Fig. 5.7c that, for example, curves *D* and *A* have two crossing points (denoted with vertical gray lines), i.e. equation (5.13) for *D-A* has a double solution. Modulation index value shown in Fig. 5.7b represents the specific case when solution is singular (both solutions are the same). In that point the derivative of both crossing curves will be the same. Equating derivatives of *D* and *A* one gets: $\omega t_1 = \pi/10 + int\cdot\pi$, and for *D* and *B* $\omega t_2 = 3\pi/10 + int\cdot\pi$, where *int* is an integer number. Since equations shown in Fig. 5.7 are valid only for the shown range $0 \le \omega t < 2\pi/5$, ωt_1 and ωt_2 are uniquely determined. Putting these values back into (5.13), the same value of the modulation index $m=0.5257$ is obtained from both equations, *D-A* and *D-B*. This case is shown in Fig. 5.7b.

Because of the symmetry between half-sectors 1 and 4, and 2 and 3, it is enough to analyse only half-sectors 1 and 2, i.e. sector 1 ($0 \le \omega t < 2\pi/10$, or, in general case $0 \le \omega t < \alpha/2$). Further on, intersection of other fractional parts of desired leg voltages can be written in a similar way as in (5.13), and other relevant modulation indices in Fig. 5.7 can be calculated.

In a general case, if an n-phase system is considered, the desired I^{th} and J^{th} sinusoidal leg voltages can be described according to (5.1), as:

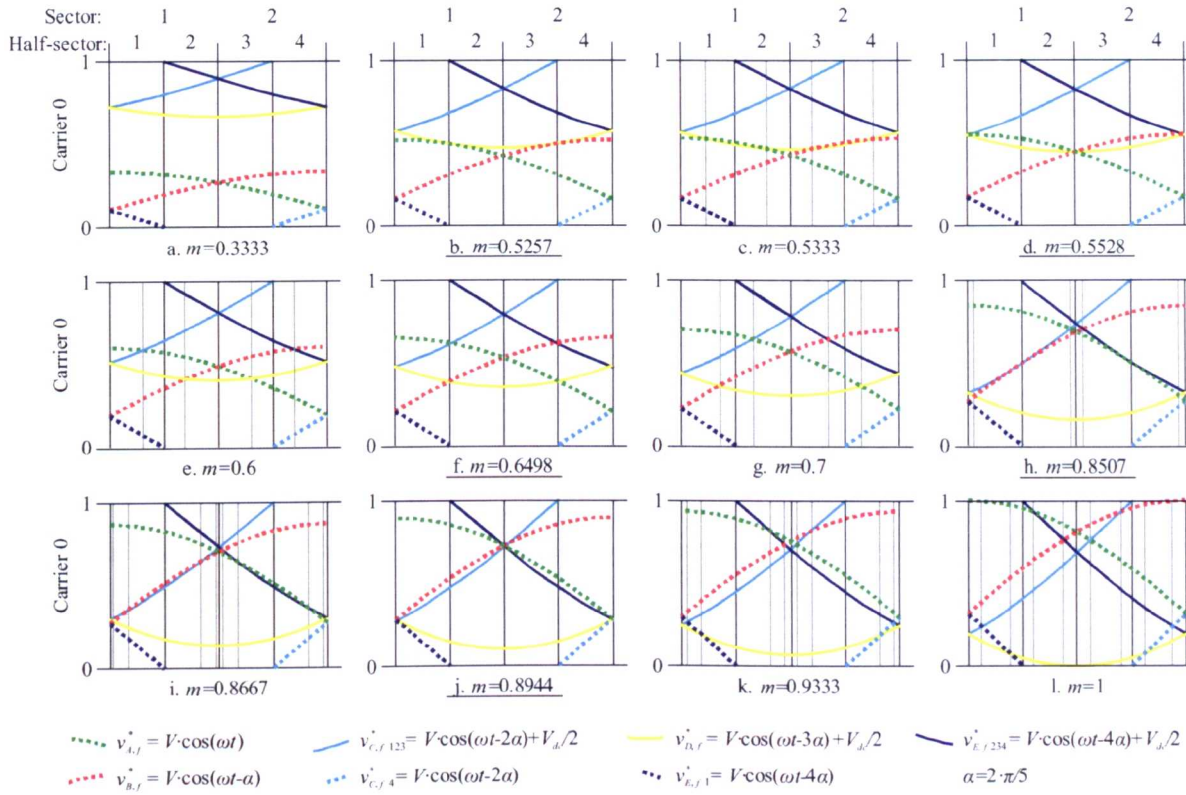


Fig. 5.7: Changes of the applied switching sequence according to the modulation index for the first 1/5 of the output period of the five-phase three-level inverter leg reference signals. Each vertical line denotes application of a new switching sequence. Dashed lines are for signals transferred downwards from *Carrier* 1 band.

$$\begin{aligned} v_I^* &= V \cdot \cos(\omega t - (I-1)\cdot\alpha) + V_{dc}/2 \\ v_J^* &= V \cdot \cos(\omega t - (J-1)\cdot\alpha) + V_{dc}/2 \end{aligned} \qquad I,J \in [1,\ldots,n] \tag{5.14}$$

After normalisation (3.1) and application of the definition of the modulation index value (5.10), (5.14) becomes:

$$\begin{aligned} u_I^* &= \frac{l-1}{2}(m \cdot \cos(\omega t - (I-1)\cdot\alpha) + 1) \\ u_J^* &= \frac{l-1}{2}(m \cdot \cos(\omega t - (J-1)\cdot\alpha) + 1) \end{aligned} \qquad I,J \in [1,\ldots,n] \tag{5.15}$$

For the determination of the change of the switching sequence, the fractional part should be considered. So, expressing each of the desired leg voltages as $u_{LEG}^* = u_{LEG,\,\mathrm{int}}^* + u_{LEG,\,f}^*$ yields:

$$\begin{aligned} u_{I,f}^* &= \frac{l-1}{2} \cdot (m \cdot \cos(\omega t - (I-1)\cdot\alpha) + 1) - u_{I,\mathrm{int}}^* \\ u_{J,f}^* &= \frac{l-1}{2} \cdot (m \cdot \cos(\omega t - (J-1)\cdot\alpha) + 1) - u_{J,\mathrm{int}}^* \end{aligned} \qquad I,J \in [1,\ldots,n] \tag{5.16}$$

Equating equations in (5.16) and expressing m, it is found that the intersection of traces I and J, i.e. the instant of change of the applied sequence, is determined in the general case with:

$$m_{IJ}(t) = \frac{2}{l-1} \cdot \frac{u_{I,\mathrm{int}}^*(t) - u_{J,\mathrm{int}}^*(t)}{\cos(\omega t - (I-1)\cdot\alpha) - \cos(\omega t - (J-1)\cdot\alpha)} \qquad I,J \in [1,\ldots,n] \tag{5.17}$$

It is emphasised in (5.17) that variables are time dependent, but one should be also aware that variables are sampled, so they take discrete values at kT_s instants of time. Equation (5.17) is universal, but has to be solved

from case to case, since the integer part changes. For the three-level case situation is somewhat simpler because integer part is constant during the half-periods of the signal. For the five-level case, for example, instants when reference crosses from *Carrier* 0 to *Carrier* 1 i.e. from *Carrier* 2 to *Carrier* 3 band and thus changes integer value, is dependent on the modulation index; hence application of (5.17) is not straightforward for manual calculation. Because of the symmetry, it is enough to analyse only the range $0 \leq \omega t < \alpha/2$. As an example of using (5.17), which is easy for manual calculation in the three-level case, let us calculate the position of v_D and v_E intersection in Fig. 5.7 (yellow and violet trace, respectively). Equation (5.17) becomes:

$$m_{ED}(t) = \frac{2}{3-1} \cdot \frac{u^*_{E,\text{int}}(t) - u^*_{D,\text{int}}(t)}{\cos(\omega t - 4\alpha) - \cos(\omega t - 3\alpha)} \tag{5.18}$$

Desired leg voltage u^*_D changes integer part, i.e. $Carrier^{No}$ value, between the 1st and the 2nd half-sectors. So its integer value changes from 1 to 0 (here also a change of the applied sequence appears, and start of the sequence is changed). Equation (5.18) should be considered separately in these two half-sectors 1 and 2. Intersection for each half-sector is determined with:

$$\begin{aligned} &a) \quad m_{ED\,1}(t) = \frac{1-0}{\cos(\omega t - 4\alpha) - \cos(\omega t - 3\alpha)} \\ &b) \quad m_{ED\,2}(t) = \frac{0-0}{\cos(\omega t - 4\alpha) - \cos(\omega t - 3\alpha)} \end{aligned} \tag{5.19}$$

As can be seen from (5.19), in the second half-sector intersection is obtained for 0 modulation index at all times. This is also clear from Fig. 5.7; for zero voltage amplitude (m=0) yellow (u^*_D) and violet (u^*_E) line will overlap each other in the second half-sector. However, zero voltage reference amplitude is not of interest. In the first half-sector movement of the intersection of u^*_D with u^*_E (Fig. 5.7j, k, l) is defined with (5.19), and has the same form as (5.13) that describes intersections of u^*_D with u^*_A and u^*_B in the first sector.

Fig. 5.7 and equation (5.17) reveal some similarities between carrier-based and space vector modulation techniques. Namely, in (5.17) time dependence can be directly replaced with dependence on the angle $\theta = \omega t$, so that (5.17) can be expressed as:

$$m_{IJ}(\theta) = \frac{2}{I-1} \cdot \frac{u^*_{I,\text{int}}(\theta) - u^*_{J,\text{int}}(\theta)}{\cos(\theta - (I-1)\cdot\alpha) - \cos(\theta - (J-1)\cdot\alpha)} \qquad I,J \in [1,\ldots,n] \tag{5.20}$$

Thus (5.20) represents an equation in time domain ($\theta = \omega t$) that shows when the change of the switching sequence takes place (fractional parts change mutual order). This equation is expressed as $m(\theta)$, so in accordance with space vector approach, if $m \cdot e^{j\theta}$ is plotted it will represent position in the α-β plane where change of the switching sequence takes place. In space vector terminology of Chapter 4, this represents the sub-sector borders.

If (5.20) is applied to all pairs of reference leg voltages u^*_I, u^*_J for one period of the normalised sinusoidal reference voltages (5.1), and if position of $m \cdot e^{j\theta}$ is plotted in the α-β plane, division of the sectors into sub-sectors can be obtained. One such division for the five-phase three-level case with in-phase carriers is shown in Fig. 5.8. This figure is obtained by Matlab script that in incremental steps changes angle θ and modulation index m. Every time when condition that fractional parts of any two reference leg voltages are the same is satisfied, the programme plots a dot at $m \cdot e^{j\theta} \cdot V_{dc}/2$ position. Modulation index was set to change in incremental steps from zero to 1.2, thus a part of the overmodulation region is also covered. For better clarity, the figure from Matlab has been re-plotted using a specialist's drawing software. The figure looks complicated, but it contains a lot of data.

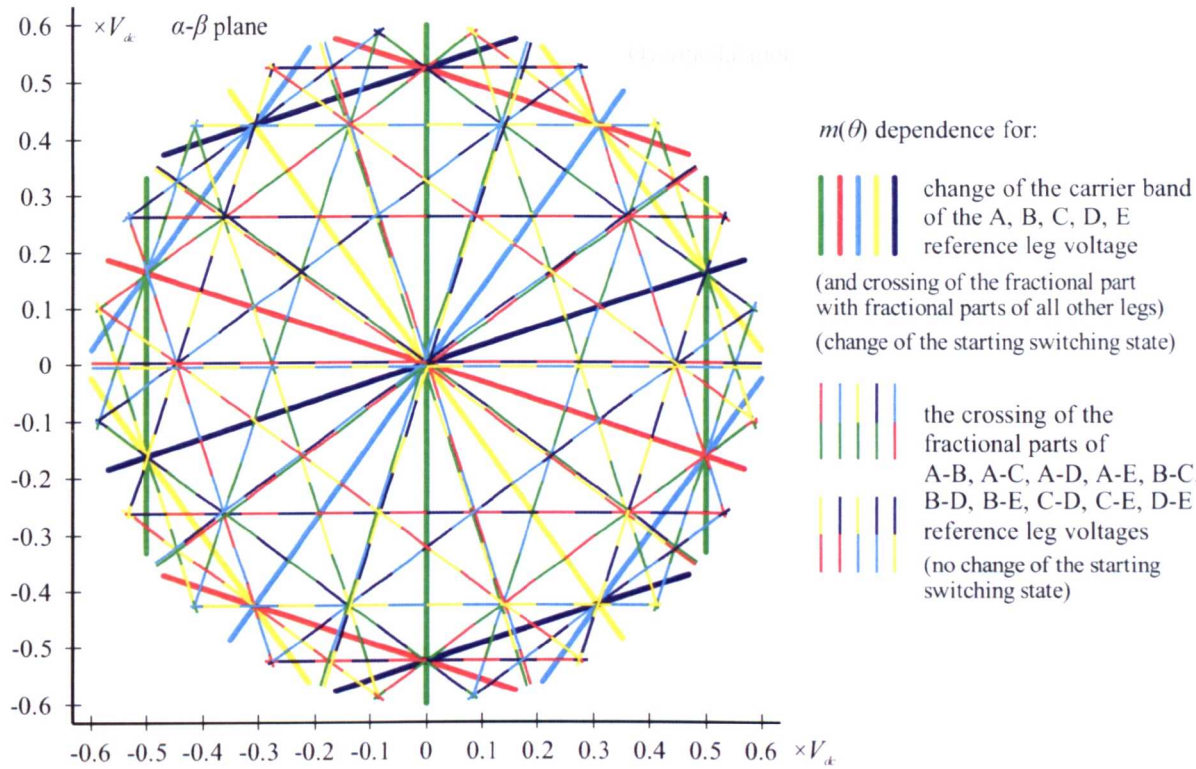


Fig. 5.8: Change of the switching sequence, determined by intersection of the two fractional parts in time domain, mapped into the α-β plane for pure sinusoidal references.

With thick lines intersections of the fractional part of the particular leg (determined by colour of the line) with all the other reference fractional parts are determined. In other words, these points represent the change of the carrier zone. There are three thick lines of the same colour that are in parallel. The line that is crossing the origin is when the reference changes from *Carrier* 0 to *Carrier* 1 band, while the other two are when the reference moves out of the linear PWM region, going into overmodulation. As already explained, at these positions change of the starting switching state appears and that governs where additional switchings appear. If only linear modulation region is analysed, this appears at $(2k-1)\cdot\pi/10$, where k is an integer number. Thus position θ when this appears directly corresponds to the values in Fig. 5.6.

Position $m(\theta)=m\cdot e^{j\theta}\cdot V_{dc}/2$ when two reference leg voltage fractional pars intersect is denoted with two-colour lines. Hence, position of $m_{AB}(\theta)$ for example is shown with green-red line according to the assumed colour code. One can see that at $k\cdot\pi/5$, where k is an integer number, two switching states are changing in a sequence, i.e. two intersections take place. For example, at $\theta=\pi/5$ both fractional parts of the reference leg voltages A and B (green-red) and C and E (blue-violet line in Fig. 5.8) intersect. This corresponds to the intersection of the mentioned reference leg voltages in Fig. 5.6 for the same angle.

This analysis reveals similarity between space vectors and carrier-based approach. Namely, one can see that division of the sector into sub-sectors for modified five-phase three-level algorithm of 4.2.7 (Fig. 4.17), is almost identical as the one shown in Fig. 5.8. The only difference is in the maximum modulation index range that in Fig. 5.8 is limited to 1, while in Fig. 4.17, it is extended to 1.0515. This will be overcome by min-max injection, as explained in the following section.

5.3 SINUSOIDAL REFERENCES WITH MIN-MAX INJECTION

All previous explanations are general, and, for the sake of simplicity and requirements of real-world applications, they were given for symmetrical sinusoidal reference signals. Another very useful and commonly used signal shape for leg voltages is sinusoidal signal with min-max injection. It has a universal validity, in a sense that it does not depend on either the number of phases or on the shape of the modulating signals [Levi et al. (2008)]. It actually comes as a logical solution to the problem of centring signals within dc-bus rails in each instant of time. Illustration of the centring for one switching period T_s of the reference leg voltages for the five-phase three-level inverter is shown in Fig. 5.9. In terms of the desired leg voltages, since they should be centred around $V_{dc}/2$, this injection can be expressed as:

$$v_{inj} = -\frac{v^*_{MIN} + v^*_{MAX}}{2} + \frac{V_{dc}}{2} \tag{5.21}$$

where v^*_{MIN} and v^*_{MAX} stand for the minimum and maximum value, respectively, of the reference leg voltages (Fig. 5.9a). With this injection the linear modulation index range is extended to the maximum value for any number of phases, since desired leg voltages are always centred in between 0 and V_{dc} (Fig. 5.9b).

Equation (5.21) is usually expressed in terms of the phase voltages, and in that case it has the form:

$$v_{inj} = -\frac{v^*_{\min} + v^*_{\max}}{2} \tag{5.22}$$

where $v^*_{\min}$ and $v^*_{\max}$ stand for the instantaneous minimum and maximum reference phase voltages, respectively. In this case, the signals are centred around 0, but the value of the injection v_{inj} is the same as in (5.21).

In the case of symmetrical sinusoidal references this injection is of the triangular shape at n times output frequency. This triangular signal represents injection of harmonics with frequencies equal to the odd multiples of n times fundamental frequency. Hence, min-max injection is in literature sometimes called triangular signal injection. Also, a commonly considered injection in the literature is the one that takes only the fundamental component of the triangular signal, so it represents sinusoidal n^{th} harmonic injection. One example, for the five-phase case with min-max injection, is shown in Fig. 5.10. With min-max injection the maximum modulation index in the five-phase system in the linear PWM region is increased to its maximum value of 1.0515.

5.3.1 CHANGE OF THE SWITCHING SEQUENCE

Rule which governs the change of the switching sequence when two fractional parts of the reference leg

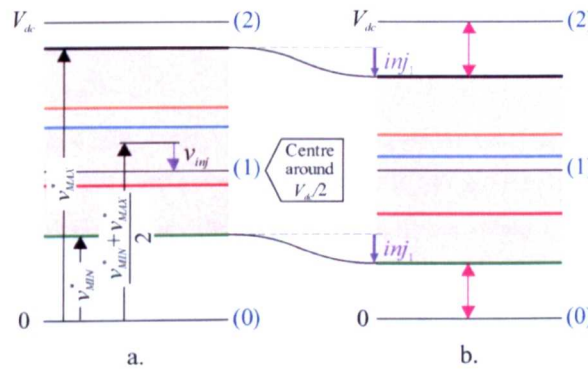


Fig. 5.9: Centring of the desired leg voltage signals: a. sampled signals (not centred), b. with min-max injection, centred signals between dc-bus rails. One switching period (T_s) is shown.

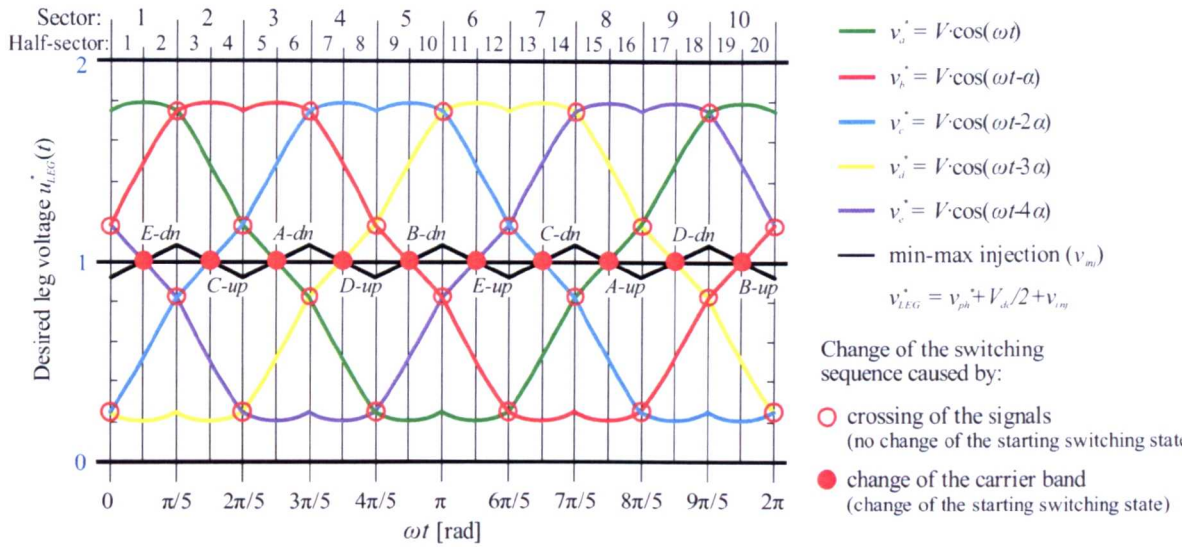
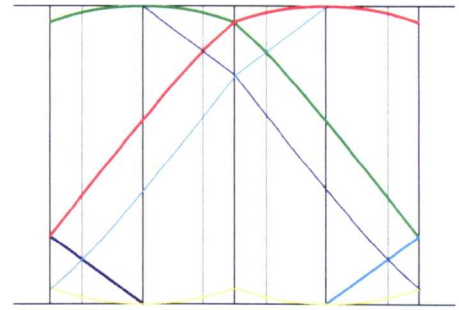


Fig. 5.10: Symmetrical sinusoidal leg voltage references with min-max injection.

voltages are intersecting (Fig. 5.5a and Fig. 5.5b) is general, and it will now be analysed using sinusoidal references with min-max injection. Another principle, for determination of the switching state dwell times from sorted fractional parts of the reference leg voltages (i.e. from the common carrier band), is also general. This rule is expressed in Fig. 5.5c and equation (5.9). For the sake of explanation, the effect of change of the switching sequence will be here shown for the three-level five-phase case with symmetrical sinusoidal references and min-max injection, Fig. 5.10.

It can be seen from Fig. 5.10 that min-max injection in the five-phase three-level case does not change integer part of the desired leg voltages until m=1, which represents linear modulation index range for pure sinusoidal references. That means that in this region only the fractional parts are changed, i.e., considering Fig. 5.5c, a constant value injection is added to all signals. As there is no change of the integer part, this injection does not move any of the signals out of the range 0 to 1. In that way only the values of δ_1 and δ_{n+1} will be changed and the difference will be for the normalised value of the injection. Also, if δ_1 is increased, δ_{n+1} will be decreased for the same value and vice versa. Times of application for all the other voltages remain the same since injected signals cancel each other in expressions for δ_i (5.9). The sum of times of application remains equal to the switching period T_s. So, in the three-level five-phase case, min-max injection only changes the times of application of the first and of the $(n+1)^{th}$ switching state. There is no change of the integer-part values, and no change of the order of the fractional parts, so the switching sequences remain the same. For the modulation index values from 1 to 1.5015, the integer parts remains the same as for m=1, so the order of the fractional parts and the sequence in use will be the same.

It can be seen that the basic sector and half-sector sub-division remains the same as in Fig. 5.6, as it is shown in Fig. 5.10. Let us analyse now influence of the change of the modulation index value on the change of the switching sequences if PD is used. Considering again desired leg voltages v_I^* and v_J^*, they will differ from values in equations (5.14) only for a constant value. As final equation (5.17) results after equating of equations for v_I^* and for v_J^*, this injection will be cancelled. Since integer part is unchanged, equation (5.17), i.e. (5.20), remains valid. That means that the change of the switching sequence appears in the same instants of time, and for the same modulation index values as for the pure sinusoidal references. The only difference is in the value of the



m=1.0515

Fig. 5.11: Change of the applied switching sequence for the maximum modulation index for the first 1/5 of the output period of the five-phase three-level inverter with references consisting of sums of sinusoidal signals and min-max injection.

maximum modulation index that is now increased by 5.15% for the five-phase case. The graphical representation, similar to those in Fig. 5.7, is given in Fig. 5.11, for the maximum modulation index value. All the other modulation index values for which change in the switching sequence takes place remain as in Fig. 5.7.

As in a previous section where no injection was present, $m_{IJ}(\theta)$ dependence can be obtained. As explained, equation (5.20) remains valid, but the time dependence of integer parts of the reference leg voltages will be changed for modulation indices greater than one. This has as a consequence that representation of the change of the switching sequences from time domain in the α-β plane, for sinusoidal references with min-max injection, for the five-phase three-level case, will be different from those shown in Fig. 5.8, but only regarding the lines that were governing maximum modulation index value. Plot of the $m \cdot e^{j\theta} \cdot V_{dc}/2$ values, for all pairs of the reference leg voltages u_I^*, u_J^*, for one period of the normalised sinusoidal references with min-max injection, is

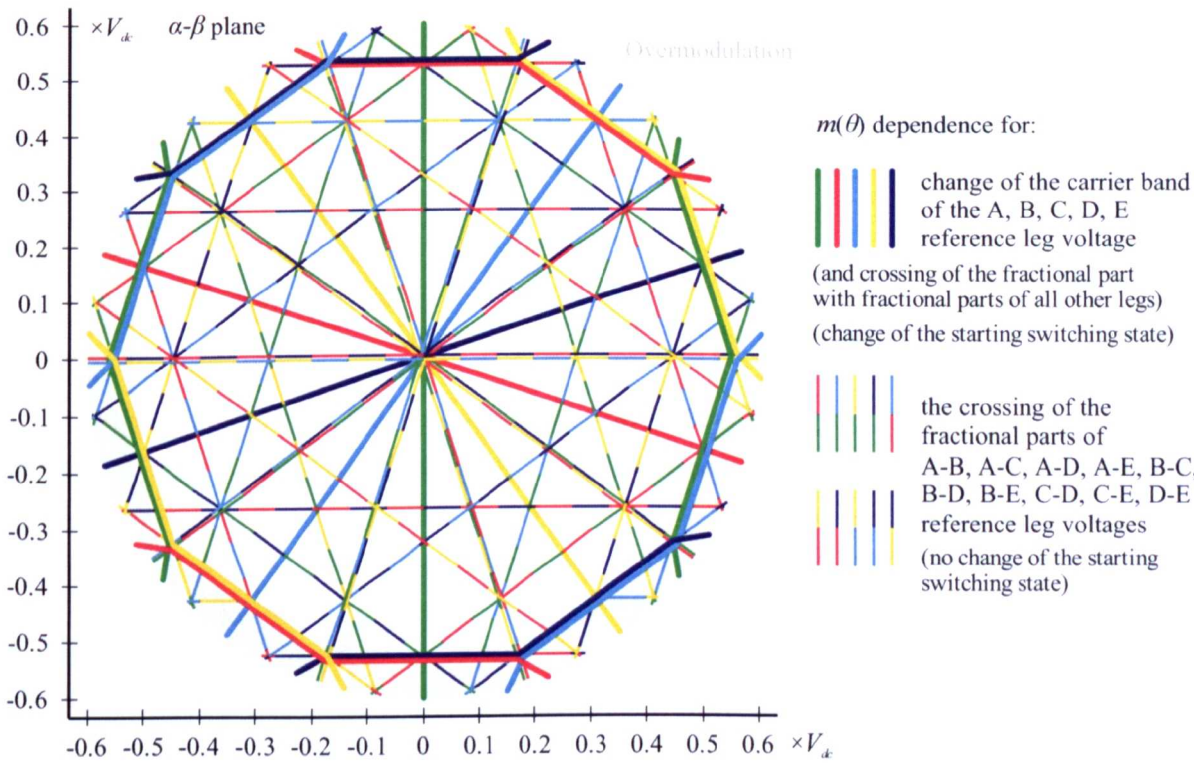


Fig. 5.12: Change of the switching sequence, governed by the intersection of the two fractional parts in time domain, mapped into the α-β plane for sinusoidal references with min-max injection.

shown in Fig. 5.12. Now, similarity with space vector division of the α-β plane into sub-sectors for the modified algorithm, Fig. 4.17, is much more pronounced, than it was without any injection, Fig. 5.8. Obviously, min-min max injection has increased the maximum modulation index value. From Fig. 5.11 one can see that for the maximum modulation index of 1.0515 two references simultaneously touch upper and lower dc-bus, i.e. when reduced to the single carrier band these two references simultaneously touch 0 and 1. For example, at instant $\pi/10$ reference A fractional part (u^*_{Af}, green line) reaches 1, while reference D (u^*_{Df}, yellow line) touches 0. For $\theta=3\pi/10$ this is the case for references B and D (red and yellow line). This simultaneous change of the carrier zone for two references is also obvious in Fig. 5.12, where for angle of $\theta=\pi/10$ and m=1.0515 one can see that there exist two thick lines, green and yellow, while for $3\pi/10$ changes of the carrier zone happen simultaneously in legs B and D, red and yellow lines.

5.3.2 DOUBLE MIN-MAX INJECTION

This type of injection was for the first time introduced by [Lee et al. (2000)]. Later on, it was used by [McGrath et al. (2003)] where the aim was to generate the injection that produces the same output as the optimized space vector algorithm of [Celanovic and Boroyevich (2001)], which is widely accepted as the reference three-phase multilevel space vector algorithm. Optimisation of the choice of the switching sequences to minimise the number of transitions, and optimisation for space vector positions within a switching period, that is based on the flux trajectory concept, are included in the algorithm. It is shown that for the three-phase case the optimal space vector algorithm that leads to the minimum flux distortion is the one in which the total time of application of the redundant switching states is equally shared between two states.

In order to increase the modulation index range the reference signals must already contain min-max injection (5.21), which will be called here inj_1. Equal sharing of redundant switching states (for optimisation of the flux trajectory), in time domain, means that dwell times δ_1 and δ_{n+1} are equal in (5.9). Graphically, considering Fig. 5.5c, that means that the distance from $u^*_{MAX,f}(kT_s)$ to 1 is the same as the distance from 0 to $u^*_{MIN,f}(kT_s)$, or, in other words, that fractional parts of the signals are centred in 0 to 1 zone (the lowest carrier band). Centring of signals can be done again with min-max injection, but now signals should be centred around 0.5 value (i.e. around $0.5 \cdot V_{dc}/(l-1)$ in non-normalised form). So, min-max equation from (5.21), in normalised form, for the second centring becomes:

$$u_{inj} = -\frac{u^*_{MIN.f} + u^*_{MAX.f}}{2} + 0.5 \tag{5.23}$$

This injection will be denoted as inj_2.

Finally, construction of the injection proposed in [McGrath et al. (2003)] represents sum of two min-max injections (inj_1 and inj_2) applied to the reference leg voltages, where the second injection is constructed after all reference signals (that already include the first min-max injection) are shifted to the common carrier band.

Graphical interpretation of the double injection is shown in Fig. 5.13. It is very similar to the one in Fig. 5.9, for the single min-max injection (the first centring, Fig. 5.13a and Fig. 5.13b), but it also explains the additional two steps. Moving of all the reference signals (with one min-max injection) to the common carrier band is shown in Fig. 5.13c, and leg reference signals after double centring are shown in Fig. 5.13d. Note that the second centring does not change modulation index range, so that with double injection the same maximum modulation index can be obtained.

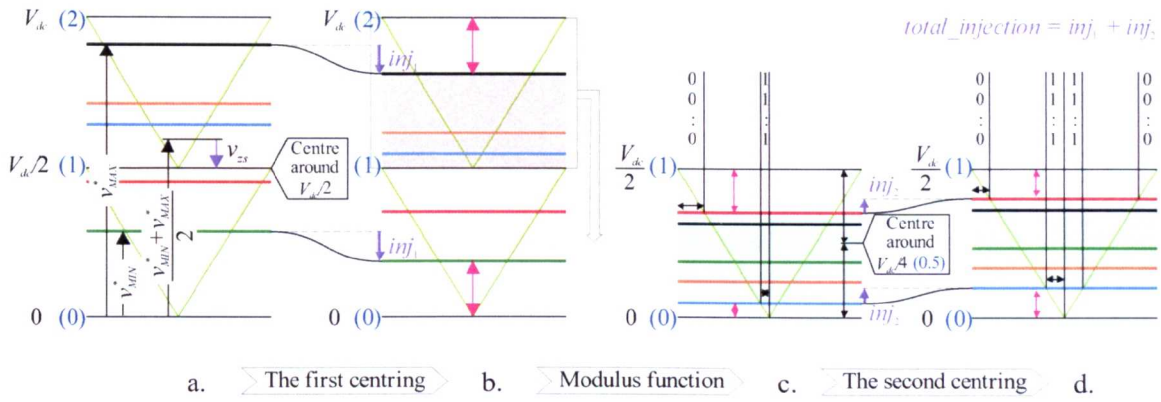


Fig. 5.13: Construction of the double min-max injection (n=5, l=3): a. sampled signals (not centred), b. signals centred between dc-bus rails, c. signals referred to the common carrier band, d. centred signals within the common carrier band. One switching period (T_s) is shown.

It can be seen that the double min-max injection is universal. It can be constructed and applied to any shape of the reference signals, and it is also independent of the number of phases and the number of levels. There is no evidence that this technique has ever before been applied to multiphase systems. At the moment, it is beyond the scope to investigate whether optimal values in the three-phase case remain optimal when the same type of injection is constructed and applied in a multiphase case, and this represents one of the directions for future work.

One can see that the second injection does not change mutual order of the fractional parts of the reference leg voltages that was set by the first min-max injection, Fig. 5.13c and Fig. 5.13d. Also, it is applied inside the common carrier band, so it does not change the carrier zone, i.e. integer values of the references. This has as a consequence that switching sequences and points when new sequences appear for the sinusoidal references with the single and with double min-max injection are the same. The only thing that is changed is application time of the first and of the last switching state that is equalised by the second injection, as already explained. Thus Fig. 5.12 is also valid for the sinusoidal references with the double min-max injection. This injection is the most suitable for comparison of carrier-based modulation strategies with the space vectors algorithms. The division of the α-β plane is identical as for the modified five-phase three-level space vector algorithm in 4.2.7, Fig. 4.17. Furthermore, equal application time of the first and the last switching state, i.e. redundant switching states, is a typical assumption for the space vector algorithms. Eventually, in Chapter 6, it will be shown that these two modulation strategies lead to identical performance.

5.4 SUMMARY

In this chapter some characteristics of the level-shifted disposition with in-phase triangular carrier signals, for multilevel multiphase VSIs, were analysed. In-phase disposition of carriers was selected for easier comparison with the space vector techniques. It is explained that multicarrier PD-PWM can be reduced in the simple manner to the single-carrier case, using simple modulus function. The primary purpose of the min-max injection, centring of signals between dc-bus rails, is explained. One more type, double min-max injection, that equalises times of applications of the redundant switching states in the sequence, is also given. Very important part of this chapter represents investigation of the switching sequences in the time domain and analysis when a new sequence appears. This analysis is given for pure sinusoidal references and for sinusoidal references with

single and with double min-max injection. The position of appearance of the new switching sequence is a function of $m(\theta)$ and its representation in the α-β plane is given for all three cases. Similarity with the space vector algorithms is highlighted.

Chapter 6

COMPARISON OF ANALYSED MODULATION STRATEGIES

6.1 INTRODUCTION

In this chapter a comparison of the space vector and carrier-based modulation strategies from previous two chapters will be done. Two configurations are considered: five-phase three-level and seven-phase three-level topology. In both configurations neutral-point clamped, NPC, inverter was used for the experimental verification, and in both cases the load was symmetrical and star-connected. For the five-phase case experiments induction machine was used, while for seven-phase case *R–L* was utilised. Five algorithms from the previous two chapters were analysed for both topologies. From Chapter 5 three carrier-based modulation strategies using disposition with in-phase carriers are used: with pure sinusoidal references, with min-max injection and with double min-max injection. These strategies will be denoted here as CBPWM0, CBPWM1 and CBPWM2, respectively. Analysed space vector strategies are the original and modified algorithm from Chapter 4, and will be denoted as SVPWM1 and SVPWM2.

As already mentioned before, comparison of the space vector and carrier-based techniques is very important. Due to the simplicity for implementation, carrier-based techniques are used much more in practice. The equivalence of performance of these two techniques has been shown for the three-phase two-level case [Holmes (1992)], and later on, it was confirmed for some three-phase three-level and multilevel cases [Wang (2002), McGrath et al. (2003)]. Such a proof is also available for the multiphase two-level case [Dujic et al. (2009)]. The missing part is the analysis of a general multilevel multiphase case; hence, some comparisons and first steps in this direction are given in this chapter.

The chapter contains the following sections. In section 6.2 a theoretical comparison of the space vector and carrier-based modulation strategies is given. Further, in 6.3 and 6.4 the comparison is underpinned by experimental results for the five- and seven-phase three-level cases. The content of this chapter, based on experimental results, has been published in [Bodo et al. (2012), Dordevic et al. (2013a), Dordevic et al. (2013b)].

6.2 THEORETICAL COMPARISON OF ANALYSED STRATEGIES

Comparison between carrier-based and space vector modulation strategies can be done in two directions. The first direction is how to produce space vector modulation strategy using a carrier-based algorithm, and the second is how to obtain a carrier-based method using space vectors. The first direction is more important since the carrier-based strategy is easier for practical implementation. The analysis will be given here based on the considered CBPWM and SVPWM strategies that are aimed for sinusoidal output phase voltage. The most of the attention will be paid to the comparison of the applied switching sequences with carrier-based and with space

vector strategies and on division of the sectors into sub-sectors, i.e. regions of applications where these sequences should be applied.

There is not any general multilevel multiphase space vector modulation strategy that is based on VSD, but there are some general rules that are commonly in use with SVPWM techniques, and that were used in the analysed modulation strategies in Chapter 4. As explained, there are common assumptions that every leg changes its level for one level-up in the first half of the switching period, and symmetrically for one level-down in the second half of T_s. Also, time of application of the redundant switching states is usually equally shared.

If the desired output is sinusoidal, then the reference projection into the α-β plane is a circle, and in the x-y planes it must be zero. As explained, projection onto 0-axis can be arbitrary because it is not considered by the space vector algorithms. According to the mapping of the harmonics, 3.4.2, one can see that only multiples of the n-th harmonics are mapped onto the 0-axis. These harmonics in time domain are the only ones that can be injected into the sinusoidal set of the references without affecting the sinusoidal shape of the output phase voltages. Multiples of the n-th harmonics injection will keep the symmetry of the reference leg voltages and actually will appear as the CMV. That means that for obtaining the space vector modulation by a carrier-based modulation strategy only the injection has to be varied.

Space vector implementation of the carrier-based algorithms with in-phase carriers can be easily done in the following way. According to the explanations in 5.2.2 and 5.2.3, one can see that the applied switching sequences can be obtained in a straightforward manner from the time domain using a single-carrier band in a way as it was done in Fig. 5.5a and Fig. 5.5b and with adding the integer part on it. Then, from the applied switching states, space vector projections can be obtained using some of the equations from (3.30) to (3.32), and times of application can be calculated using (3.51). Because the time division for the redundant space vector is not necessarily equal for every carrier-based algorithm, (5.9) and Fig. 5.5c have to be used as well in the calculation of the application times. Equal time of application of the redundant switching states will exist if the centring inside the common carrier band exists. It is obvious that there are a few different switching sequences that have to be applied during the period of the fundamental. Also, if modulation index increases, different sequences have to be applied. The process for division of the α-β plane into sub-sectors when different switching sequences have to be applied is explained for the three mentioned carrier-based modulation strategies in Chapter 5, and it is general. Final division for the analysed strategies was given in Fig. 5.8 for CBPWM0 and in Fig. 5.12 for CBPWM1 and CBPWM2. Now, for each sub-sector, switching states, and thus space vectors, can be read from the time domain and saved. Again, as explained for the other space vector algorithms, only the first sector (or the first sector-pair) can be analysed, and all the other general methods for implementation, used in Chapter 4, can be applied.

Let us now compare applied switching sequences for the analysed carrier-based modulation techniques with single and with double min-max injection for the five-phase three-level case with switching sequences used for the modified space vector algorithm of 4.2.7. For obtaining switching sequences for the carrier-based modulation Fig. 5.7 can be used. It is valid up to the modulation index of 1, because it is given for pure sinusoidal references. If Fig. 5.7 were to be drawn for sinusoidal references with min-max injection, it would increase the maximum modulation index value to the maximal one, and the order of the fractional parts would remain the same. This is because min-max injection in the three-level case does not change the integer part (change of the carrier zone) and it only moves all the reference fractional parts for the same value. The second

injection does not change the order of the references inside the single carrier zone, i.e. it does not change applied sequences. Hence Fig. 5.7 can be used for analysis of the applied switching states for all three analysed carrier-based strategies up to m=1. This is also clear from Fig. 5.8 and Fig. 5.12, because the change of the switching states appears for the same values of m and θ and figures are identical for m<1. From Fig. 5.7a and Fig. 5.7b one can see that the order of the fractional parts of the references in the first half sector, the first 18°, is: $u^*_{C,f}$, $u^*_{D,f}$, $u^*_{A,f}$, $u^*_{B,f}$, $u^*_{E,f}$ (blue, yellow, green, red, violet) from top to bottom. According to Fig. 5.5c one can say that leg *C* will be the first to increase its level by one, then leg *D* etc. in the first half of T_s. For obtaining the starting switching state integer values of the references are important. They can be read directly from Fig. 5.6 or Fig. 5.10 and the result is: 11001 (u^*_A, u^*_B and u^*_E are in *Carrier* 1 zone, while u^*_C, u^*_D are in *Carrier* 0 band). Then, as the $u^*_{C,f}$ is the largest fractional part it will change the state first, and the next switching state in the sequence will be **1**1101 (changed leg is shown in bold), then the leg with the second largest fractional part $u^*_{D,f}$ will increase its level for one, so the switching state will be 11**1**11, then leg *A* will change leading to **2**1111, then leg *B*, 22**1**11 and finally leg *E*, 221**1**2. That means that the switching sequence that will be in use for all three analysed carrier-based algorithms for the first half-sector (first 18°) and for the modulation index up to 0.5257 (shown in Fig. 5.7b), will be: 11001-11101-11111-21111-22111-22112. If the legs are denoted with order numbers 1 to 5 for legs *A* to *E*, then one simply can say that the order of the fractional parts in the first 18°, $u^*_{C,f}$, $u^*_{D,f}$, $u^*_{A,f}$, $u^*_{B,f}$, $u^*_{E,f}$ can be denoted as 34125, and this will correspond to the position of the leg that changes inside the sequence. This means that the switching sequence from the starting switching state (11001) can be constructed as: 11001-$_{(3)}$-11101-$_{(4)}$-11111-$_{(1)}$-21111-$_{(2)}$-22111-$_{(5)}$-22112, where numbers in brackets denote transition in a particular leg.

Similarly in the second half-sector in Fig. 5.7a and Fig. 5.7b (from 18° to 36°), the order of the fractional parts is: $u^*_{E,f}$, $u^*_{C,f}$, $u^*_{D,f}$, $u^*_{A,f}$, $u^*_{B,f}$, (violet, blue, yellow, green, red) or, using numerical notation of legs, the order is 53412, and the starting switching state is: 11000 (see Fig. 5.6 or Fig. 5.10). Thus the applied switching sequence in this zone for small m<0.5257 will be 11000-$_{(5)}$-11001-$_{(3)}$-11101-$_{(4)}$-11111-$_{(1)}$-21111-$_{(2)}$-22111. By simple comparison of these switching sequences with A_{dn} and A_{up} in Table 4.5 for the modified space vector algorithm, one can see that they are identical. This investigation can be continued further in the same manner. However, some simplifications can be used as well. For example, when the modulation index is between 0.5257 and 0.5528, as it is for example in Fig. 5.7c, one can see that one additional change of the switching sequence in each 18° half-sector appears. It comes from crossing of the references *A* and *D* (green and yellow line). Green-yellow border in the first 36° for 0.5257<m<0.5528 should be also noted in Fig. 5.8 and Fig. 5.12. In the first 18° this will produce change of the order of fractional parts from $u^*_{C,f}$, $u^*_{D,f}$, $u^*_{A,f}$, $u^*_{B,f}$, $u^*_{E,f}$ to $u^*_{C,f}$, $u^*_{A,f}$, $u^*_{D,f}$, $u^*_{B,f}$, $u^*_{E,f}$, i.e. in numerical notation from 34125 to 31425; *D* and *A* change the place. This will produce change of the switching sequence from 11001-$_{(3)}$-11101-$_{(4)}$-11111-$_{(1)}$-21111-$_{(2)}$-22111-$_{(5)}$-22112 to the switching sequence 11001-$_{(3)}$-11101-$_{(1)}$-21101-$_{(4)}$-21111-$_{(2)}$-22111-$_{(5)}$-22112. Hence the same starting switching state remains and the only transition appears first in leg *A* and then in leg *D*. For the angle from 18° to 36°, the second half-sector in Fig. 5.7c, one can see that sequence that was valid for the small modulation indices stays valid in the second part, while in the first part of the half-sector fractional part of the reference *A* is greater than for reference *D*. Considering numerical notation of the legs one can say that the fractional parts now changed order from 53142 to 53412. Hence, in the beginning of the second half-sector, the switching sequence will be 11000-$_{(5)}$-11001-$_{(3)}$-

11101-$_{(1)}$-21101-$_{(4)}$-21111-$_{(2)}$-22111 and after crossing of fractional parts, of reference leg voltages A and D, the switching sequence will be 11000-$_{(5)}$-11001-$_{(3)}$-11101-$_{(4)}$-11111-$_{(1)}$-21111-$_{(2)}$-22111.

If compared with the modified space vector algorithm, one can see that division of the sectors into sub-sectors in Fig. 4.17 is identical as in Fig. 5.12, as already revealed in 5.3.1. Now, it is also shown that the applied switching sequences for sub-sectors A_{dn} and A_{up} are identical for the modified SVPWM and for the analysed carrier-based techniques. Analysed case when $0.5257<m<0.5528$ corresponds to the reference that starts in A_{dn} sub-sector, then passes through B_{dn} (during $0°\leq\theta<18°$) and then goes from B_{up} to A_{up} sub-sector (for $18°\leq\theta<36°$), Fig. 4.16.

In Fig. 5.12 thick line of a particular colour will change the starting switching state by changing the state that corresponds to the colour. For example, for A_{dn} starting switching state is 11001, and it is separated from A_{up} by the thick violet line (leg E, position 5), thus in A_{up} starting switching state will be 11000 (the starting switching state cannot contain the maximum level, so the fifth leg decreased from 1 to 0). Also, as shown, thin borders which contain two colours in Fig. 5.12 do not change starting switching state. Transition of the reference through the two-colour line border, will only change in the switching sequence the place of the increase of the legs that correspond to the line colours. For example, consider the yellow-green border that separates sub-sectors A_{dn} and B_{dn}. The switching sequence for A_{dn} is determined with the starting switching state 11001 and by the switching order (order of fractional parts) 34125. The switching sequence for B_{dn} will be determined by the same starting switching state and by the order in which legs A and D (green and yellow) change positions, 31425. Note that in this way, starting switching sequence plus the switching order, can be alternatively used for the switching sequences labelling. Also note that for determination of the switching sequences for all 10×14 sub-sectors, it is enough to know the starting switching sequence for one sub-sector, e.g. A_{dn}, in the first sector. Using the explained changes that apply in a sequence when transition to the other sub-sector in Fig. 5.8, i.e. Fig. 5.12, appears can be used for determination of the sequences for all the other sub-sectors. These changes are determined by the thickness and the colour(s) of the border lines, as explained.

This section gave theoretical background for comparison of the carrier-based and space vector modulation strategies. In what follows, the equivalence of the two mentioned strategies will be confirmed by experiments.

6.3 EXPERIMENTAL COMPARISON: FIVE-PHASE THREE-LEVEL CASE

In this section experimental results for the five modulation strategies, three carrier-based (CBPWM0, CBPWM1, CBPWM2) and two space vector modulation strategies (SVPWM1 and SVPWM2) for the five-phase three-level VSI are compared. Experimental results for the space vector modulation strategies have been already given in 4.2.8. Used carrier-based strategies have been analysed in Chapter 5 where only the theoretical considerations were given, while experimental results are given here. CBPWM0 strategy, with pure sinusoidal references has been used as the reference modulation strategy.

Experimental setup for all five analysed strategies was the same, and settings have been already stated in 4.2.8. Also, some additional data regarding hardware and a photograph of the experimental setup are given in Appendix A. However, let us recall that the five-phase induction machine with sinusoidal distribution of the stator windings has been used, and it was supplied from the custom-built three-level NPC inverter. Some relevant inverter parameters are: V_{dc}=600V, f_s=2kHz, dead time 6μs. Ratio V/f was kept constant. For the algorithm implementation in real-time, dSpace system has been used.

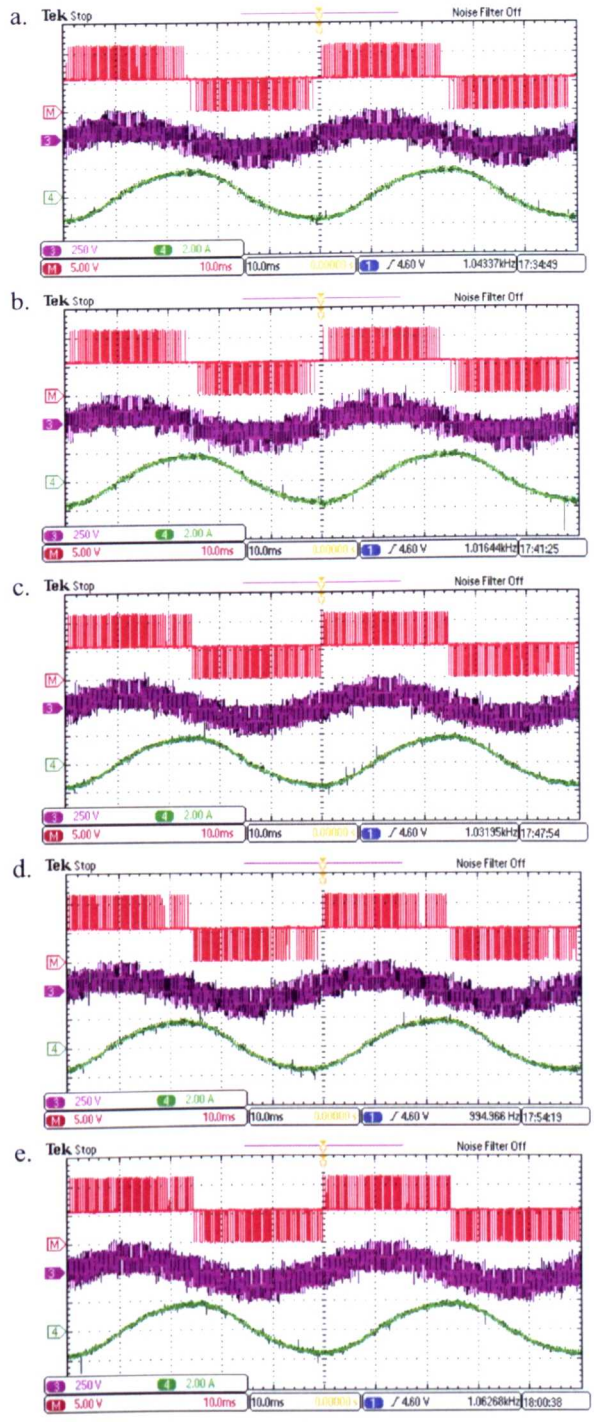


Fig. 6.1: Oscilloscope recording of the v_{LEG}, v_{ph} and i_{ph}, at m=0.4 for a. CBPWM0, b. CBPWM1, c. CBPWM2, d. SVPWM1, and e. SVPWM2 (M-leg voltage, 260V/div; Ch3-phase voltage, 250V/div; Ch4-phase current, 2A/div; time = 10ms/div).

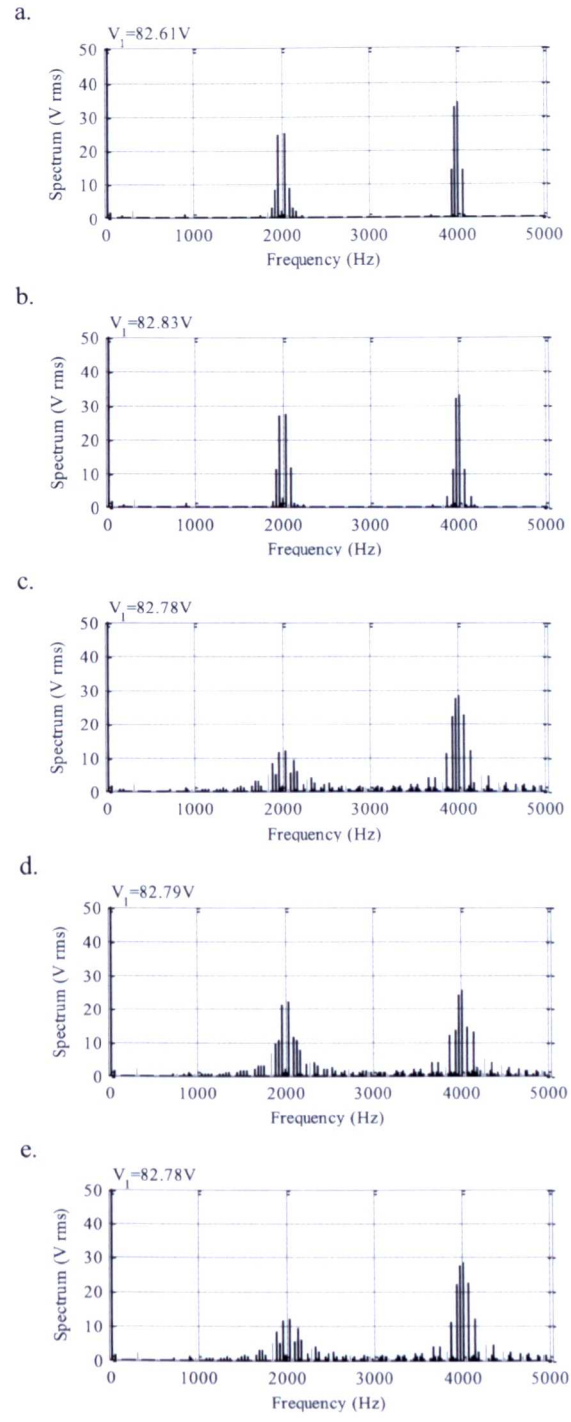


Fig. 6.2: Experimental results for the modulation index m=0.4 showing phase voltage spectrum for the analysed strategies: a. CBPWM0, b. CBPWM1, c. CBPWM2, d. SVPWM1, and e. SVPWM2 (n=5, l=3).

Waveforms produced by the investigated modulation strategies are very similar and become even more similar with the increase of the modulation index value. In order to highlight the differences, a small modulation index m=0.4 has been chosen. Simulation and experimental results for this modulation index for the SVPWM1 and SVPWM2 were already shown in Fig. 4.18 and Fig. 4.21, i.e. in Fig. 4.20a and Fig. 4.23a. Oscilloscope waveforms of these two modulation strategies together with three analysed carrier-based strategies are given in

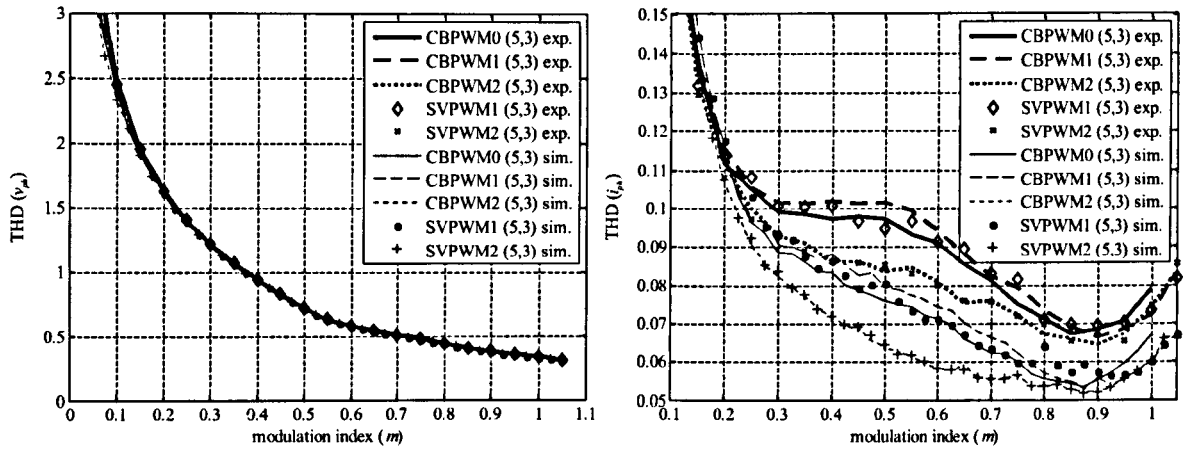


Fig. 6.3: a. Phase voltage and b. motor current THD comparison for all five modulation strategies (simulations and experiments), for the full linear range of the modulation index, m=0.05 to 1.05 (i.e. 1 for CBPWM0).

Fig. 6.1. Leg voltage, phase voltage, and motor current are shown. The differences in waveforms between modulations are marginal.

Some characteristics of the strategies are more evident in the harmonic spectra, which are shown in Fig. 6.2 for all considered strategies for the phase voltage (Fig. 6.2a to Fig. 6.2e). One can see that there are a lot of similarities between compared modulation strategies. All strategies achieve required fundamental output voltage with hardly any low-order harmonics in the phase voltage. The observable differences that appear in the spectra are predominantly related to the side-bands around multiples of the switching frequency. Due to the explained theoretical identities, one expected conclusion is that two of the methods, CBPWM2 and SVPWM2, should show identical performance; this is obvious from Fig. 6.2c and Fig. 6.2e. This conclusion is valid for the whole investigated linear modulation index range from 0 to 1.0515. This will be proven further by the THD comparison. The cleanest spectra result with the CBPWM0 and CBPWM1 methods.

Under ideal conditions no lower order harmonics should be present in the phase voltage spectrum. However, in the shown experimental results in Fig. 6.2 it is evident that there are some small values of the third harmonic (at 60Hz), caused by the inverter dead time [Jones et al. (2009)] as well as a non-negligible 15th harmonic at 300Hz (m=0.4, f=20Hz). This is a zero-sequence harmonic in a perfectly symmetrical machine and its origin are discussed in [Bodo (2013)].

Study of the type shown in Fig. 6.2 has been conducted, using both experiments and simulations, for the whole linear PWM region. Simulation model for the carrier-based techniques is developed in Simulink block-set and diagram from Fig. 5.4 has been used in the realisation. The same inverter and machine PLECS block-set models, with the same parameters, already used in simulations with SVPWM1 and SVPWM2 in 4.2.8, were used. For the CBPWM0 method the linear region is up to m=1, while it is up to 1.0515 for all the other modulation strategies. Simulations were done for the modulation index values from 0.05 up to 1.05 (i.e. 1 for CBPWM0), with the step of 0.025, while experiments were done with the doubled step, 0.05. On the basis of the FFT results, THD has been calculated up to 21kHz, according to (4.9).

Comparison of the simulation and experimental THD results, for all five analysed strategies, for the phase voltage and current THDs, is given in Fig. 6.3. Note that the same curves for SVPWM1 and SVPWM2 were already given in Fig. 4.24b and Fig. 4.24d. From Fig. 6.3a it can be seen that for the given modulation index

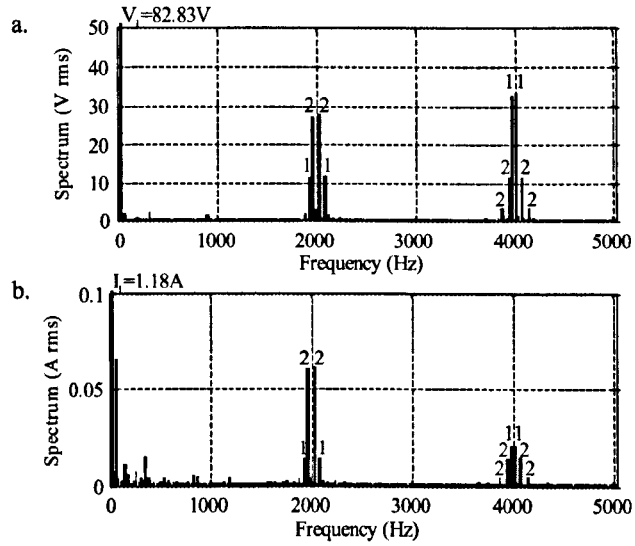


Fig. 6.4: Zoomed extracts from phase voltage and current spectra: experimental results for CBPWM1, m=0.4. a. Phase voltage spectrum. b. Motor current spectrum.

range all modulation strategies produce essentially the same phase voltage THD value. Also, very good agreement between simulation and experimental results is visible. The small difference between simulation and experimental results for low modulation indices is believed to originate from inaccurate knowledge of the dead time, which impacts on the results more in the low modulation index region.

Current THD analysis, illustrated in Fig. 6.3b, confirms again that the CBPWM2 and SVPWM2 yield identical performance. Experimental results show, in general, somewhat higher current THD than simulations. This is caused by the assumption that leakage inductances are constant and equal at all frequencies in the simulations, which is in reality not satisfied [Jones et al. (2011b)]. However, regardless of the differences in the numerical values (which are, it should be stressed, rather small), the trend of all curves and their mutual position is the same in both simulations and experiments. The noticeable difference between strategies exists for the medium to high modulation index values; clearly, CBPWM2 and SVPWM2 can be characterised as being the best. These two strategies equally share redundant vector application time, and in the three-phase case they were proven as optimal according to the flux harmonic distortion [Lee et al. (2000), McGrath et al. (2003)]. The findings reported here prove that these PWM strategies offer the lowest current THD in the five-phase case as well.

Consider now the operation with the modulation index of m=0.4 from Fig. 6.2. A five-phase system is characterised with two planes and the voltage/current harmonics map into one of the two planes, according to the rules given in Fig. 3.7a. The mapping of the harmonics is very important since the equivalent impedance is not the same in the two planes. Equivalent inductances in the first (torque/flux producing) and the second (non-flux/torque producing) plane are governed by $(L_{ls}+L'_{lr})$ and L_{ls}, respectively, where the symbols stand for the stator and rotor leakage inductances, [Jones et al. (2011b)]. CBPWM1 strategy is taken as an example for further analysis. Phase voltage spectrum of Fig. 6.2b and current spectrum, obtained experimentally, are shown in Fig. 6.4 (note the y-axis scaling). Mapping of the significant harmonics is defined with numbers '1' and '2'. Number '1' stands for harmonics that map into the α-β plane, while '2' denotes harmonics that map into the x_1-y_1 plane, Fig. 6.4a and Fig. 6.4b. For all five compared modulation strategies, the most significant harmonics of the phase voltage in the second side-band are greater than the most significant harmonics in the first side-band

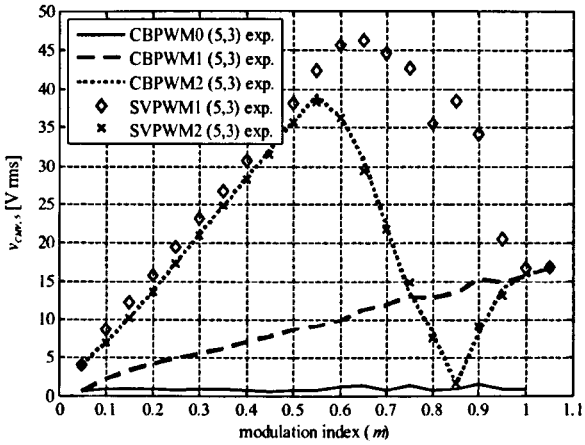


Fig. 6.5: Experimental results: variation of the fifth harmonic in the CMV against modulation index for the considered five PWM strategies.

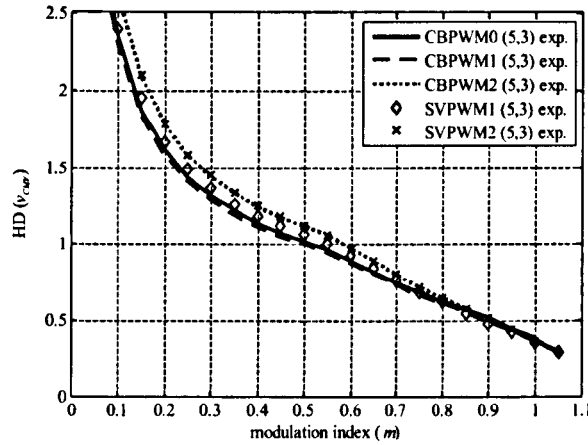


Fig. 6.6: Experimental results: variation of HD for CMV against the modulation index for the considered five PWM strategies.

(Fig. 6.2). However, according to the mapping of the harmonics and Fig. 6.4, one can see that the most significant harmonics in the first side-band map into the second plane (that has lower impedance), while those highest in the second side-band map into the first plane (that has higher impedance). This means that, in the current spectrum, the highest harmonics from the second side-band will have much smaller influence than those from the first side-band (Fig. 6.4a and Fig. 6.4b). In Fig. 6.2a to Fig. 6.2e the smallest harmonics in the first side-band are present for the CBPWM2 and SVPWM2 modulation strategies (Fig. 6.2c and Fig. 6.2e), while those in the second side-band are all similar. It is therefore obvious that these two modulation strategies have a smaller current THD value than the other strategies, as confirmed by the THD in Fig. 6.3b for the considered modulation index of m=0.4.

One can see in Fig. 6.4b that small amounts of harmonics are present at low frequencies (3rd, 7th, etc.) in the phase current spectrum. This is a consequence of the dead-time effect [Jones et al. (2009)], which in the current hardware is around 6μs, and which is not compensated. The drive is controlled in an open-loop manner, without closed current control loops, leading to the appearance of these small current harmonics.

Variation of the CMV has been at first analysed by examining the amount of the fifth harmonic in it as a function of the modulation index, for all PWM techniques. This is illustrated in Fig. 6.5. As expected, CBPWM0 has practically zero value of the fifth harmonic throughout the linear modulation region. For CBPWM1 the 5th harmonic magnitude increases with the modulation index m practically linearly. Other modulation strategies have different dependences, as is evident in Fig. 6.5. One can see that the SVPWM2 modulation strategy is characterised with a smaller 5th harmonic, when compared to SVPWM1, in the whole modulation index range, and this was the basic idea in 4.2.7 for developing the SVPWM2.

Harmonic distortion of the CMV is analysed as well. Expression (4.9) has been used for the calculation. All modulation strategies have very similar CMV HD values, as can be seen in Fig. 6.6. It is interesting to note that the SVPWM2 modulation strategy, which was originally developed to reduce CMV variations and which has the lower fifth harmonic value than the SVPWM1 (Fig. 6.5), has actually higher HD in the whole modulation index range.

Complexity of the algorithms has been analysed by comparing the estimated number of different operations per switching cycle and through the measurement of the execution time on the dSpace, using dSpace

Table 6.1: An approximate algorithm complexity comparison by the number of operations.

Method	+	×	> <	sin or cos	Memory (integer / real variables)
CBPWM0	8	8	0	5	-
CBPWM1	14	9	8	5	-
CBPWM2	21	10	16	5	-
SVPWM1	54	52	11	7	600/500
SVPWM2	55	51	11	6	840/700

Profiler tool. Comparison of the arithmetic operation number is shown in Table 6.1 (logical operations are not included) up to the stage at which the reference leg voltages are created. The data in Table 6.1 correspond to how the algorithms have been implemented and should not be taken as benchmark values, since different ways of realisation may result in a different number of operations. Nevertheless, it is obvious from the given data that the algorithm complexity increases in the order in which the PWM techniques are listed.

The same conclusion is arrived at by measuring the algorithm execution time on the real-time hardware dSpace ds1006 with Profiler tool. The execution time of all carrier-based strategies is very similar and is around 0.7μs in each switching period. Execution time for the two SVPWM strategies is also similar, around 1.65μs. Thus the analysed SVPWM strategies ask for around 2.3 times higher execution time than CBPWM, on average. Another important issue is the memory consumption. Carrier-based strategies do not require any memory storage. On the other hand, SVPWM1 and SVPWM2 strategies require 600 integer (2 sectors × 10 sub-sectors × 6 five-phase switching states, data from Table 4.2 and Table 4.3) and 500 real variables (pre-calculated 5×5 inverted matrix from (4.5) for space vectors that correspond to the saved switching sequences), and 840 integer (2 sectors × 14 sub-sectors × 6 five-phase switching states, data from Table 4.5 and corresponding data for the second sector) and 700 real variables (pre-calculated inverse matrices), respectively, to be stored in the memory. Because time of application of redundant switching states is equally shared, the number of saved real variables is 5/6 times lower than for integer values. As mentioned in Chapter 4, in the actual realisation of the SVPWM algorithms, the memory consumption was deliberately sacrificed, by saving data for the first two sectors instead only for the first one, to achieve a reduction in the computation time of the algorithms.

Finally, Table 6.2 provides a comparison of the major characteristics of all the considered modulation strategies. As expected, carrier-based techniques are more favourable for the real-world implementation. Also, an extension to higher numbers of levels and phases is straightforward, which is in huge contrast to the SVPWM strategies where each pair of the number of levels and number of phases has to be considered separately.

As already mentioned, the other possibility for obtaining multilevel operation is use of dual-sided supply

Table 6.2: Main characteristics of the compared five-phase three-level modulation strategies.

	CBPWM0	CBPWM1	CBPWM2	SVPWM1	SVPWM2
Concept	PD-CBPWM	PD-CBPWM	PD-CBPWM	VSD-SVPWM	VSD-SVPWM
Offline complexity	none	none	none	very high	very high
Complexity for implementation	simple	simple	simple	medium	medium
Memory requirement	none	none	none	high	high
Execution time on dSpace ds1006	≈0.7μs	≈0.7μs	≈0.7μs	≈1.65μs	≈1.65μs
State redundancy	yes	yes	yes	yes	yes
Extension to higher numbers of phases and levels	easy	easy	easy	difficult	difficult

topology. A comparative analysis of some of the results from this section and dual-inverter supply in the open-end winding topology using two two-level VSIs for a five-phase induction motor drive is reported in [Bodo et al. (2012)]. For practical purposes carrier-based modulation strategy with min-max injection has been chosen. It is shown, using extensive experimental and simulation investigation, that the overall performance of the two drive topologies is in essence identical.

6.4 EXPERIMENTAL COMPARISON: SEVEN-PHASE THREE-LEVEL CASE

A similar comparison as in the previous section has been done for the seven-phase three-level modulation strategies. The same three carrier-based modulation strategies CBPWM0, CBPWM1 and CBPWM2, but now applied to the seven-phase case, have been analysed. Two space vector methods are the original (SVWPM1) and modified (SVPWM2) algorithms from 4.3. Some of the results for space vector algorithms have already been given in 4.3.8 and will be used here again and compared with the listed carrier-based techniques.

The main difference in the hardware configuration, compared to the five-phase case, is that seven-phase star-connected passive *R–L* load had to be used, due to unavailability of the machine. This has no impact on any voltage-related considerations and affects only the current ripple analysis. Parameters of hardware that have also been used in simulations are as in 4.3.8. For forming the seven-phase inverter, two six-phase NPC inverters with the common dc-link have been used. More explanations regarding the used hardware and software, including the setup photograph, are given in Appendix A. Once more, V_{dc}=600V, dead time is 6μs, f_s=2kHz, and V/f=const law were used, where the 300V (peak value) and 50Hz have been chosen as the nominal values.

Very similar conclusions as for the five-phase case can be given. Again, with an increase of the modulation index value, modulation strategies become more and more similar. Also, because of the higher number of phases and more frequent change of the sub-sectors, similarity between modulation strategies is generally higher than in the five-phase case. Let us take the same modulation index of 0.4, as for the five-phase case, as an example. Time domain waveforms for all five modulation strategies for the leg voltage, phase voltage, and current are shown in Fig. 6.7. Any difference is hardly noticeable. For highlighting some differences phase voltage spectrum has been calculated for all five analysed modulation strategies. Phase voltage spectrum is given in Fig. 6.8, in parallel to the corresponding time waveforms in Fig. 6.7. Again, as in the five-phase case, the cleanest spectrum is for CBPWM0 and CBPWM1. All strategies easily achieve required fundamental value that is a bit lower than in the five-phase case because of the dead-time effect that is more expressed in the seven-phase case, as mentioned in 4.3.8. In the seven-phase case 14 inverter leg transitions occur during one switching period and thus 14 dead times take the part in the reduction of the fundamental value. No dead-time compensation has been applied. Of course, voltage is additionally reduced, compared to the theoretical values, because of the voltage drop on the switching components. From Fig. 6.8c and Fig. 6.8e, one can see again that for the seven-phase three-level case CBPWM2 and SVPWM2 modulation strategies yield identical performance. Because of the increased number of sub-sectors, the difference between these two strategies and SVPWM1, Fig. 6.8d, is hardly noticeable.

To validate the algorithms and prove the equivalence of the CBPWM2 and SVPWM2, and to highlight their difference compared to the other three strategies, total harmonic distortion THD has been calculated again for the full linear modulation index range. Maximum modulation index for the seven-phase case is 1.0257, as already stated in 4.3.8, and it is achievable by all the modulation strategies apart from CBPWM0, where it is

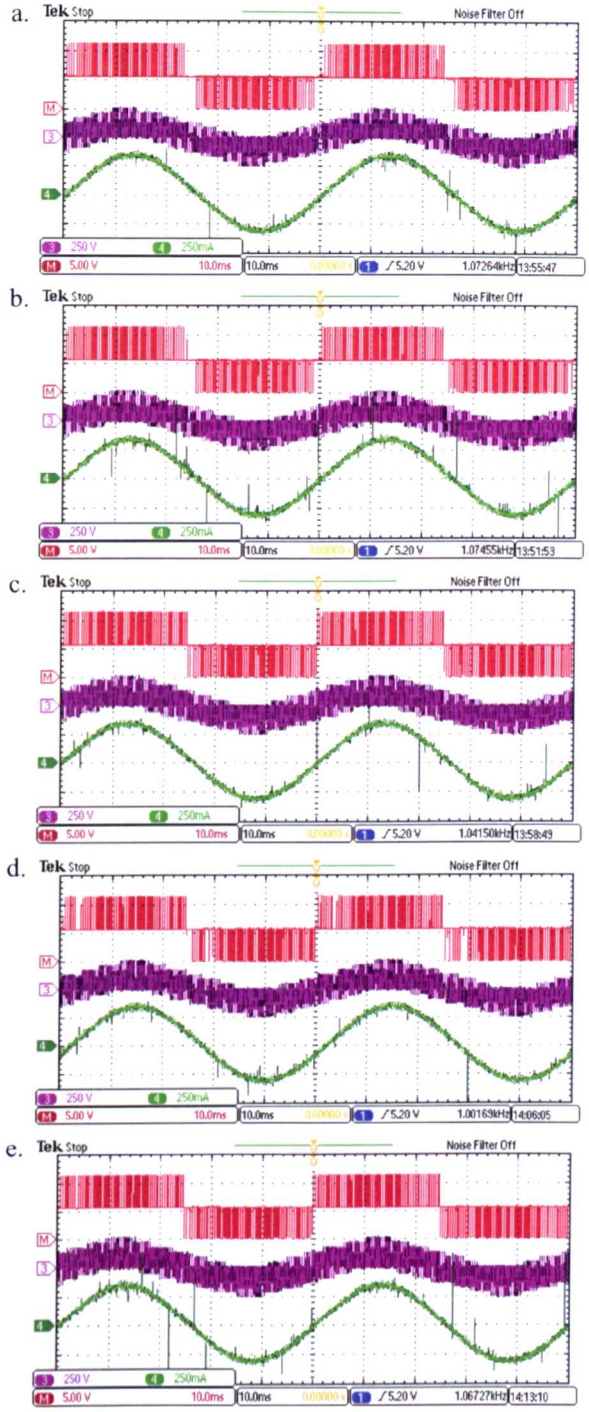


Fig. 6.7: Oscilloscope recording of the v_{LEG}, v_{ph} and i_{ph}, at m=0.4 for a. CBPWM0, b. CBPWM1, c. CBPWM2, d. SVPWM1, and e. SVPWM2 (M-leg voltage, 260V/div; Ch3-phase voltage, 250V/div; Ch4-phase current, 250mA/div; time = 10ms/div).

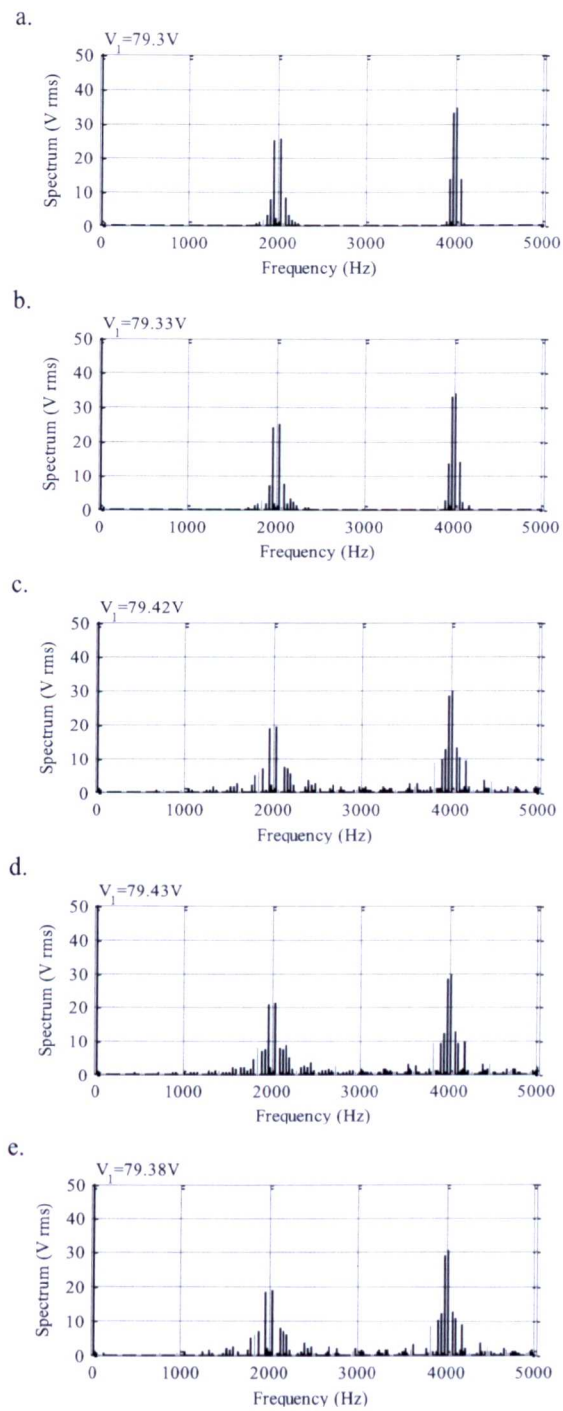


Fig. 6.8: Experimental results for the modulation index m=0.4 showing phase voltage spectrum for the analysed strategies: a. CBPWM0, b. CBPWM1, c. CBPWM2, d. SVPWM1, and e. SVPWM2 (n=7, l=3).

limited to 1. Simulations and experiments are done for the modulation indices from 0.05 up to 1, with the step of 0.05 and additionally for m=1.025 (for all the modulation strategies apart from CBPWM0). THD is computed, on the basis of the FFT results, according to (4.9), taking all the harmonics up to 21kHz. Simulation and experimental results for obtained phase voltage and current THD are shown in Fig. 6.9. One can see that phase voltage THD values for all five strategies are identical, and the same values are obtained by simulations and by

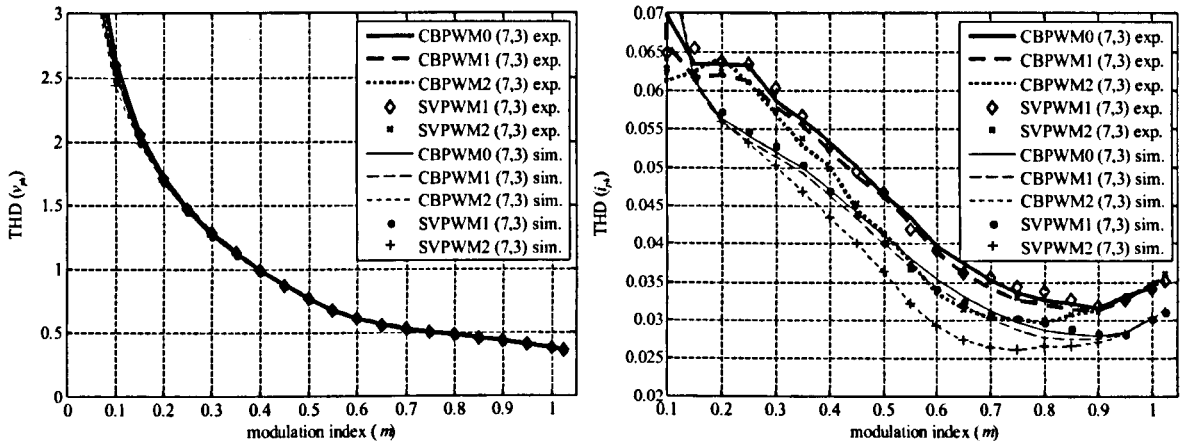


Fig. 6.9: a. Phase voltage and b. current THD comparison for all five modulation strategies (simulations and experiments), for the full linear range of the modulation index, m=0.05 to 1.025 (i.e. 1 for CBPWM0).

experiments, Fig. 6.9a. From the current THD, Fig. 6.9b, the difference between strategies is more obvious, although it should be noted that the range for THD is quite narrow and the values are quite small. It can be seen that the two PWM methods CBPWM2 and SVPWM2 yield in essence identical current ripple (i.e. THD) behaviour, which means that the same switching harmonic related side-bands are produced and are mapped in the three planes in the same manner. Due to the hugely variable impedance of the load, some disagreement between simulation and experimental results at the low modulation indices appears. However, one can say that for the modulation indices higher than 0.2, simulation and experimental results are in a good agreement. The mutual position of the curves and the shape are the same in experiments and simulations. Slightly lower values in simulation results are believed to be the consequence of the wrong parameter estimation, and the assumption that they are constant. However, this difference is quite small. Also, note again that the two modulation strategies CBPWM2 and SVPWM2, that equally share the time of application of the redundant switching states, have the minimum current THD in almost whole modulation index range.

Finally, the complexity of the algorithms has been compared by measuring the algorithm execution time on the dSpace using dSpace Profiler tool. The execution time of the applied carrier-based method is around 1.06μs, while the execution time of the space vector algorithm is around 2.25μs. Recall that in the five-phase case, in section 6.3, these values were 0.7μs and 1.65μs. A relatively small difference in the processor time consumption of the compared algorithms is due to the particular realisation of the space vector algorithm, which requires a lot of memory. The consumed memory by the original SVPWM1 space vector algorithm is 2016 integer values for storage of the switching sequences (18 sub-sectors × 8 seven-phase switching states data from Table 4.7, and the same for the second sector) and 1764 real variables (for pre-calculated inverted 7×7 matrices from (4.10) for all 18 sub-sectors for each of the first two sectors). For the modified algorithm, because the number of sub-sectors is increased from 18 to 24 per sector, these values are 2688 integer (data for the first sector are given in Table 4.9) and 2352 real variables. Note that the carrier-based methods do not require any memory, which with an increased number of phases obviously becomes an important factor. Thus, use of the specific realisation from Fig. 4.39 only slightly, roughly linearly, increases execution time of the space vector algorithms, however the memory requirement is much higher (more than 7/5 times) than in the five-phase case. Comparing space vector to carrier-based strategies, note also that the carrier-based strategies do not need any

off-line calculations, while the space vector algorithms, as demonstrated in 4.3, require a very involved off-line procedure. Thus, for the practical implementation carrier-based realisation will always be the first choice. The same conclusion was given for the five-phase case, and with increased number of phases the complexity of space vector algorithms becomes more pronounced. However, the importance of the SVPWM should not be underestimated, since it gives a much better insight into the switching behaviour of the inverter and the mapping of the harmonics into different planes. It should be noted that there are situations where only the space vector approach can be used to explain physically the working of the system: this applies to, for example, independent control of series-connected multiphase multi-motor drive systems [Levi et al. (2004)], where no insight can be gained from time (or, equivalently, carrier-based) domain, while complex space vector domain makes analysis not only clear but also easy to understand.

6.5 SUMMARY

In this chapter the comparison of the carrier-based and space vector modulation strategies for multilevel multiphase case has been given. The first part of analysis was given through the theoretical comparison of the applied switching sequences for the carrier-based and space vector algorithms. More specifically, CBPWM2 and SVPWM2 modulation strategies were compared and it was shown that they use the same switching states, and also that those switching states are applied in the same regions, i.e. sub-sectors. Thus, the identity of these two strategies has been shown. Further, these two strategies together with all the other modulation strategies were analysed according to the obtained simulation and experimental results for the five-phase and seven-phase three-level VSI supplying star-connected load. For each case two space vector and three carrier-based modulation strategies were elaborated. Simulation and experimental results are shown to be in good agreement. An identical output characteristic was shown for the carrier-based, CBPWM2, and space vector modulation strategy, SVPWM2, experimentally confirming theoretical considerations. The identity is shown for both the five- and seven-phase case. However, the execution time of the space vector strategy, even after minimisation of the number of calculations by storing as many as possible data in the memory, is still more than two times higher than for the carrier-based method for both cases. In both cases, five- and seven-phase case, all analysed strategies are characterised with the same phase voltage THD in the whole linear modulation index range. Comparison of the current THD shows that the two already mentioned modulation strategies, CBPWM2 and SVPWM2 (that equally share the time of application of the redundant space vector), have the smallest current THD for both examined cases. Hence, taking all relevant aspects into consideration, CBPWM2 is the best for real-world applications.

Chapter 7

ANALYTICAL FORMULAE FOR LEG AND PHASE VOLTAGE RMS AND THD

7.1 INTRODUCTION

So far, the analysis of the PWM techniques that can be used for the control of multilevel multiphase inverters has been given. It can be seen that a lot of the analysis has been based on the comparison of the total harmonic distortion results. THD was calculated by application of the Fourier transformation and by taking a limited number of harmonics into the consideration. In this chapter derivation of analytical formulae for the leg and phase voltage total harmonic distortion THD will be presented. The considered system is again a symmetrical multiphase star-connected load, supplied from a multilevel pulse width modulated voltage source inverter. The solution is based on the Parseval's theorem, which links frequency spectrum and time domain through the average power (i.e. RMS squared value) of the signal. The assumption throughout the derivations is that the ratio of the switching to fundamental frequency is high ($f_s/f \to \infty$). Derivations are based on the integration of the power of the PWM signal in a single switching period over the fundamental period of the signal. Only ideal sinusoidal reference leg voltages are analysed, and no injection of any type is considered; this therefore corresponds to the CBPWM0. Analytical expressions for the leg voltage THD are given for any number of levels. Formulae for phase voltage THD for any number of phases are derived for two- and three-level cases, for the most commonly used carrier-based methods. Comparison of the analytically obtained curves with simulation and experimental results shows a high level of agreement and validates the analysis and derivations.

The chapter is organised as follows. First, a survey of the existing knowledge is given in 7.2. In section 7.3 a review of the basic definitions of the signal power and THD is given. The next section 7.4 considers average power (and THD) of the PWM signal obtained by an l-level inverter for the constant reference signal. In 7.5 results of the previous section 7.4 are used and applied to the sample-by-sample constant parts of the sinusoidal reference signal. Hence, analytical formulae for the average power and THD of the produced PWM leg voltage by an l-level inverter, for ideal sinusoidal reference signal, are derived. In 7.6 correlation of the average power of the leg voltages and phase voltages is shown and the analytical formulae for phase voltage signal power and THD are given. Considered cases are a two-level inverter with carrier-based PWM and three-level case with in-phase disposition of carriers (PD-PWM) and with carriers in phase opposition disposition (POD), which is for the three-level case identical to the alternative phase opposition disposition (APOD) [Carrara et al. (1992)]. In 7.7 analytical results are compared with simulation and experimental result, where THD calculation is based on the numerical calculations and on frequency domain with limited number of harmonics, respectively. Conclusions are given in the last section 7.8.

7.2 REVIEW OF THE RELEVANT ISSUES

The most common way of evaluating the total harmonic distortion (THD) in practice is by using the numerical approach, based on calculation of the Fourier transformation (FFT) of the signal. However, THD can be also calculated analytically, and the aim in this chapter is to develop analytical formulae for the leg and phase voltage THD. Considered system is an n-phase symmetrical star-connected load (e.g. induction machine) supplied from the multilevel (l-level) voltage source inverter (VSI). The inverter output voltage is obtained by means of the pulse width modulation (PWM).

The importance of the THD as a measure of the waveform quality is highlighted in [Holmes and Lipo (2003)]. In [Holmes and Lipo (2003)], the risk of taking a THD indiscriminately as a figure of merit is also emphasised. It is shown, using a simple example, that two completely different square-waveforms can result in the same THD although the distribution of the energy in the spectrum is totally different. The emphasis in [Holmes and Lipo (2003)] is on the weighted THD (WTHD), which is more appropriate for the current THD and is thus useful as an indicator of the additional motor losses. However, the illustrations in [Holmes and Lipo (2003)] are not given for PWM signals; quasi-square-wave signals were considered instead.

Similar non-PWM based modulation strategies with the same methods of integration, as the one shown in [Holmes and Lipo (2003)], were used in [Farokhnia et al. (2011a), Farokhnia et al. (2011b), Yousefpoor et al. (2012)]. In [Farokhnia et al. (2011b)] leg-to-leg staircase waveform, produced by a multilevel three-phase inverter with unequal dc-bus voltages, was analysed. Depending on the mutual position of the switching angles that appear in the two considered phases, whose leg-to-leg voltage is examined, nine different zones for the five-level case were analysed. Analytical formula for each region is given. The difference between the use of analytical formula and commonly used formula that takes into account e.g. the first 49, 63 etc. harmonics is highlighted. In [Yousefpoor et al. (2012)] THD of the line-to-line (leg-to-leg) voltage is minimised by direct determination of the switching angles of cascaded H-bridge (CHB) units for a staircase waveform operation. Considered case is a seven-level three-phase CHB inverter and genetic algorithm (GA) was used for the minimisation purposes. It is proven that minimisation of the leg voltage THD does not lead to the minimal leg-to-leg voltage THD, and that optimisation algorithm has to be applied directly to the leg-to-leg voltages. In [Farokhnia et al. (2011a)] variation of the dc-bus voltages is also included as an additional parameter in relation to the work described in [Yousefpoor et al. (2012)]. A genetic algorithm was used again. As expected, it is shown that reduction of the dc-bus voltages for small modulation indices will improve the THD. Of course, this can only be applied in systems where variable dc sources are available and where high dynamics are not a primary concern.

The case considered in this chapter is PWM operation rather than the quasi-square-wave modulation. The first aim here, analytical calculation of the PWM modulated multilevel inverter leg voltage THD, has already been considered in [Van Der Broeck (2003), Leon et al. (2004)]. The solution given in [Van Der Broeck (2003)] is analytical and is given for the leg voltage THD and for the WTHD. The solution has been developed for the most typical numbers of levels, two, three and five, individually for each. The research of [Van Der Broeck (2003)] was extended in [Leon et al. (2004)] with an attempt at generalisation for an arbitrary number of levels. However, the generalisation is given in a piece-wise integral form and the integrals are not solved analytically, since this is a difficult problem due to the dependence of the borders of integration on the modulation index value. Numerical solution of the problem is rather simple, so it appears that the curves given for the multilevel

cases in [Leon et al. (2004)] were obtained by a computer program that does the integration. In this chapter, the research of [Leon et al. (2004)] is advanced and the integrals are solved analytically. General analytical formulae for the leg voltage and also, for the first time, for the phase voltage THD are given. Circumstances when results are valid are explained. The same idea of integration and for obtaining general formulae has been used in [Ruderman and Reznikov (2010a), Ruderman and Reznikov (2010b), Ruderman et al. (2013)]. However, the results in these two papers are actually not valid for the shape of voltage that they are aimed for.

7.3 SIGNAL POWER AND DEFINITION OF THD

All signals in practice are continuous signals and after measurement they become discrete. Physical signals are usually sampled with the devices (such as an oscilloscope) with the constant time step Δ, and samples are stored in a memory of the device. Only periodical signals are of interest, so it will be assumed that sampled signal represents one period of the periodical signal. Finite number of signal samples is convenient for computer signal processing. It is assumed that sampling time Δ is constant. The discrete representation of the continuous signal $x(t)$ is $x(k\Delta)$ (or $x[k]$), where k is an integer value that identifies sample number. If period of the signal is T, then the number of samples per period is $K = \lfloor T/\Delta \rfloor$.

One of the common approaches in signal processing is to obtain spectrum of the signal and then perform analysis in the frequency domain. For obtaining spectrum, Fourier analysis is commonly in use. Discrete Fourier transformation (DFT) is a transform for Fourier analysis of the finite-domain discrete-time functions, so it can be applied for the samples within one period of the signal. This transformation is sometimes called discrete time Fourier series (DTFS), because it transforms discrete and periodic time signal into discrete and periodic spectrum. DFT is usually calculated using fast Fourier transformation (FFT) algorithm that can be applied if the number of samples is a power of 2. The number of harmonic components in the spectrum of the signal $x(k\Delta)$, calculated using DFT algorithms, is equal to the number of samples in time domain, K [Oppenheim and Schafer (2009)].

Fourier transformation is closely related to the definition of the energy and the power of the signal. The instantaneous power $p(t)$ and the energy W of the continuous signal $x(t)$ can be defined as [Oppenheim et al. (1997)]:

$$W = \int_{t_1}^{t_2} p(t)\mathrm{d}t = \int_{t_1}^{t_2} |x(t)|^2 \mathrm{d}t \tag{7.1}$$

The equation equivalent to (7.1) for discrete time signals is:

$$W = \sum_{k_1}^{k_2} p(k) = \sum_{k_1}^{k_2} |x[k]|^2 \tag{7.2}$$

In (7.1) and (7.2) t_1 and t_2, i.e. k_1 and k_2, represent instants in time between which the energy is calculated. For obtaining total energy of the signal $t_1 \to -\infty$ and $t_2 \to +\infty$.

For periodical signals it is very useful to define average power per signal period. The average (active) power of the continuous and discrete periodical signal is defined as:

$$P = \frac{1}{T}\int_0^T |x(t)|^2 \mathrm{d}t \quad \Leftrightarrow \quad P = \frac{1}{K}\sum_{k=1}^{K} |x[k]|^2 \tag{7.3}$$

Since $x(t)$ and $x[k]$ are real values (measured signal), symbol for magnitude "$|\ |$" in equations (7.1) to (7.3) can be omitted and it will not be used further on.

Note that the average power in (7.3) represents the mean squared value of the signal. Thus the RMS value of signal can be defined as:

$$X_{rms} = \sqrt{\frac{1}{T}\int_0^T x(t)^2 \mathrm{d}t} = \sqrt{P} \tag{7.4}$$

or, in other words, average power P can be defined as RMS^2.

The equation that links energy in the time and in the frequency domain is known as the Parseval's theorem. The Parseval's theorem for the periodical signal states that the energy in one period of the signal $x(t)$ (i.e. the average power P), is equal to the energy (power) in the spectrum [Oppenheim et al. (1997)]:

$$P = \frac{1}{T}\int_0^T x(t)^2 \mathrm{d}t = \sum_{h=-\infty}^{+\infty} |\underline{X}_h|^2 \tag{7.5}$$

In discrete domain (7.5) becomes:

$$P = \frac{1}{K}\sum_{k=1}^{K} x[k]^2 = \sum_{h=0}^{K-1} |\underline{X}_h|^2 \tag{7.6}$$

where $\underline{X}_h$ are complex values of the Fourier transformation (complex series) of the signal $x(t)$ in (7.5), i.e. $x[k]$ in (7.6). Indices in the spectrum are chosen to start from 0, hence $X_{dc}=X_0$ is the zero component (that is, mean or dc value) of the signal $x(t)$, i.e. $x[k]$, during the fundamental period T.

If signal $x(t)$ (i.e. $x[k]$) is real, the spectrum will be conjugate-symmetrical [Oppenheim and Schafer (2009)]. Both real periodical signals, continuous and discontinuous, will produce a symmetrical discrete spectrum, but in the first case it will be aperiodic, while in the second it will be periodic, with K samples per period. Conjugate-symmetrical spectrum of a discrete periodical signal means that the magnitudes of the 1^{st} and $(K-1)^{st}$, 2^{nd} and $(K-2)^{nd}$ harmonic etc. are identical, while they are in counter phase. Since all the measured signals in practice are real values, it is common that equal halves of symmetrical (two-sided, bilateral) spectrum (1^{st} and $(K-1)^{th}$, 2^{nd} and $(K-2)^{th}$ harmonic etc.) are overlapped forming asymmetrical (single-sided, one-sided, unilateral) spectrum. Recall that the same has been done for the transformation in 3.3 that in essence is Fourier transformation. The only unpaired spectrum components are the zero component (0^{th} harmonic) and $K/2$ (i.e. $(K/2)^{th}$ harmonic) if K is even. These unpaired components are the only pure real values in the spectrum; the others are complex. The number of components in the asymmetrical spectrum is equal to $1+\lfloor K/2 \rfloor$.

When symmetrical sides of the spectrum are overlapped to form an asymmetrical spectrum, there are two main ways for new magnitude representation. Magnitudes of all the symmetrical components that are overlapped can be multiplied by 2, while unpaired components (0^{th} and $(K/2)^{th}$ harmonic) remain the same as in the symmetrical spectrum. In this case magnitudes represent peak values of the harmonics (sinusoidal waves with corresponding frequencies and phases that should be summed for reconstruction of the original signal). In this way power of the spectrum ($\sum_{h=0}^{\lfloor K/2 \rfloor} |\underline{X}_h|^2$) is changed, hence it represents power variant asymmetrical spectrum. This way is convenient for the space vectors and has been used in section 3.3. The other option is to represent magnitudes of the asymmetrical spectrum by RMS values of the harmonics (magnitudes of the overlapped components from the first solution divided by $\sqrt{2}$). In this case power of the spectrum ($\sum_{h=0}^{\lfloor K/2 \rfloor} X_{rms,h}^2$) remains

unchanged (note that the RMS of the real, dc values, 0^{th} and $(K/2)^{th}$ harmonic, that exist for even K, remain the same and should not be divided by $\sqrt{2}$). If this representation of asymmetrical spectrum is in use, then (7.6) can be used, but $|\underline{X}_h|$ should be replaced by the RMS values $X_{rms,h}$, and the upper limit of the corresponding sum becomes $\lfloor K/2 \rfloor$.

The usual way for THD calculation in practice is based on the signal spectrum and on the DFT calculation. Although there are two main formulae for THD, used definition in this thesis is in agreement with the one used in [Holmes and Lipo (2003)]. THD is defined as a distortion of the harmonics compared to the harmonic that is of interest (useful harmonic). In that case dc value of the signal is usually excluded from calculation (it is not considered as distortion), and this will also be assumed here. For example, THD of an arbitrary real but periodic signal $x[k]$ (with period T) can be calculated as:

$$\mathrm{THD}(x) = \sqrt{\frac{\sum_{h=2}^{K-2} |\underline{X}_h|^2}{2|\underline{X}_1|^2}} = \sqrt{\frac{\sum_{h=2}^{\lfloor K/2 \rfloor} X_{rms,h}^2}{X_{rms,1}^2}} \tag{7.7}$$

where $|\underline{X}_h|$ and $X_{rms,h}$ represent magnitude in the symmetrical, i.e. RMS value in the single-sided (asymmetrical), spectrum of the h^{th} component, respectively. One can see that the THD is a square root from the ratio of the distorting power over the useful power. Note that, if symmetrical form is used, the useful signal components (at the fundamental frequency) are the 1^{st} and the symmetrical one, the $(K-1)^{st}$, component (the same frequency, counter phase), hence factor 2 in denominator in (7.7).

The sampling frequency $1/\Delta$ of A/D converting devices is limited. This means that the number of samples of a periodic signal and the number of samples in one period of the spectrum are also limited to $K = \lfloor T/\Delta \rfloor$. Nevertheless, the number of harmonics that are taken into consideration for THD calculation is usually smaller in practice and is limited to a certain value. The reason for that is that the system naturally filters higher order harmonics, so they are not of interest. The other reason can be a simpler calculation. However, one should notice that in this case use of the term THD is not entirely correct, because not all harmonics are taken into consideration in the calculation. This also means that the calculated value is always smaller than the actual total harmonic distortion. As it has already been mentioned, THD is a common measure-of-quality parameter and in the area of electrical machines it is commonly calculated for leg and phase voltages as has been demonstrated in the previous parts of the thesis. If the machine is supplied from the pulse width modulated (PWM) inverter, then the non-negligible harmonics are present at the very high frequencies, and a limitation of the sum for THD calculation in (7.7) can significantly affect the result. This will be shown later in section 7.7, where theoretical curves are compared with experimental results, with the THD calculated for a limited number of harmonics. Formula (4.9) that has been used in previous chapters is of the same form as (7.7) but not all harmonics are taken into account. Only harmonics up to 21kHz were encompassed.

THD in (7.7) can be expressed in a different way. If Parseval's theorem (7.6) for RMS values of the asymmetrical spectrum and the fact that $X_{rms} = \sqrt{P}$ from (7.4) are applied, (7.7) becomes:

$$\mathrm{THD}(x) = \sqrt{\frac{X_{rms}^2 - X_{rms,1}^2 - X_{dc}^2}{X_{rms,1}^2}} \tag{7.8}$$

From (7.8) THD can be easily numerically calculated from the time domain without full spectrum calculation. X_{dc} is the average value of the signal samples $x[k]$, X_{rms}^2 is the average value of the squared samples (7.3), and the first harmonic can be calculated using a part of the DFT transformation:

$$X_{rms,1} = \sqrt{2} \cdot \left| \frac{1}{K} \sum_{k=1}^{K} (x[k]\cos(k\Delta) + jx[k]\sin(k\Delta)) \right| \tag{7.9}$$

Note that $x[k]$ in (7.9) is actually $x[k\Delta]$.

7.4 AVERAGE POWER AND THD OF THE PWM SIGNAL OBTAINED BY L-LEVEL PWM VSI FOR CONSTANT REFERENCE SIGNAL

In this section, using the Parseval's theorem and the idea from [Ruderman and Reznikov (2010b), Ruderman and Reznikov (2010a)], the average power of the obtained pulse width modulated (PWM) signal for a constant reference will be calculated. The simplest case of the two-level PWM is considered first. Normalisation will be used, but it will be changed in this chapter, so that the signal is in the range from 0 to 1 (0 to V_{dc}). In this way comparison of obtained results will be easier. The difference with respect to the previously used normalisation (3.1) is in the $(l-1)$ factor. The switching period used for PWM is denoted as T_s. A signal $x^*(t)$, that is constant during the switching period T_s, of the normalised value D ($0 \le D \le 1$), is shown in Fig. 7.1.

The PWM signal is continuous but takes discrete values in time and is denoted as $x[t]$. The aim of the PWM is that obtained signal $x[t]$ has the same average value, during each switching period T_s, as the sampled reference signal $x^*(kT_s)$. One can see that in Fig. 7.1 averaging (PWM) has been obtained using symmetrical triangular carrier signal. It is clear that the averaging can be obtained in any other way but it will only change the position of the DT_s pulse inside the switching period T_s. Of course, PWM can be obtained using more pulses during the switching period, but it will be assumed here that during one switching period only one pulse inside the switching period T_s exists, i.e. one up and one down transitions occur. Signal $x[t]$ represents scaled output leg voltage of the inverter and, in practice, minimisation of the number of the transitions is desirable to minimise

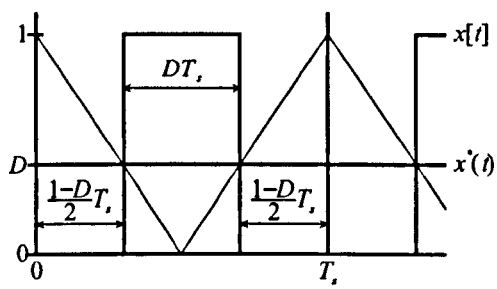


Fig. 7.1: Reference signal $x^*(t)=D$ and obtained two-level PWM signal $x[t]$.

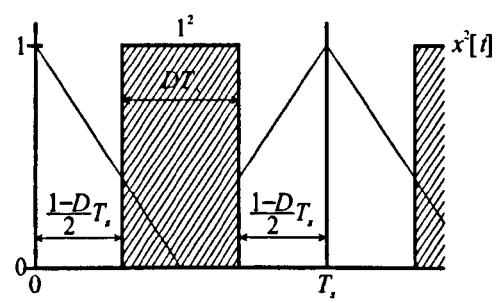


Fig. 7.2: Graphical determination of the active power of the PWM signal $x[t]$.

inverter switching losses.

The average power of the PWM signal $x[t]$ during the switching period T_s can be calculated using the integration in time as in (7.3). One gets that the average power of the PWM signal $x[t]$, which corresponds to the dc signal $x^*(t) = D$, is:

$$P_{T_s}(x[t]) = \frac{1}{T_s}\int_0^{T_s} x[t]^2 \, \mathrm{d}t = D \tag{7.10}$$

The process of integration is represented graphically in Fig. 7.2.

The average power of the reference dc signal $x^*(t) = D$ is equal to $P_{T_s}(x^*(t)) = D^2$. The difference between these two powers $D - D^2$ is the cost, i.e. the power of the additional harmonics that exist in the spectrum of the square waveform $x[t]$ to produce average value D. Terminology used in [Ruderman and Reznikov (2010b), Ruderman and Reznikov (2010a)] is somewhat different, so for average power the notion used is the normalised mean square (NMS). Hence the calculated difference of the power of the produced PWM signal and the reference signal represents ripple voltage NMS. Spectra of $x^*(t)$ and $x[t]$ for $D = 0.4$ and $T_s = 0.5\text{ms}$ are shown in Fig. 7.3, where presence of the additional harmonics in the spectrum of the PWM signal is obvious.

Note that the average power of the two-level PWM signal $P_{T_s}(x[t])$ is independent of the PWM strategy, i.e. position and number of pulses inside T_s.

Consider next the case when the PWM output is obtained using multilevel modulator with l levels. A signal $x^*(t)$ of the normalised value D ($0 \le D \le 1$) and pulse-width modulated signal $x[t]$ are shown in Fig. 7.4.

The average power of the multilevel PWM signal $x[t]$ during the switching period T_s can be calculated again using (7.3). One gets that the average power of the signal $x[t]$ is:

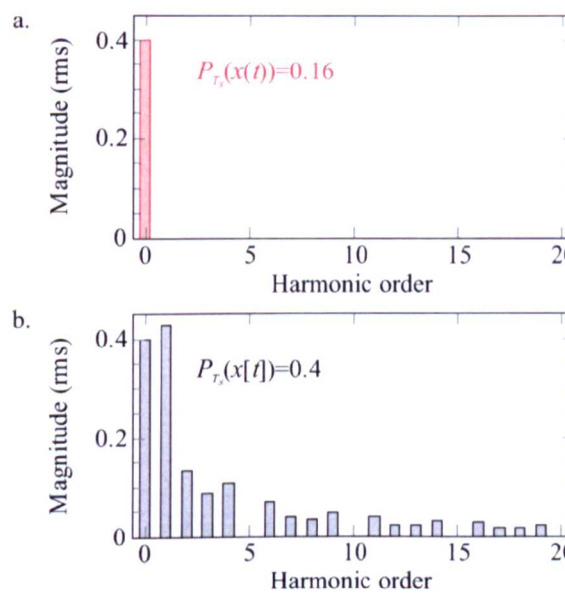


Fig. 7.3: a. Spectrum of the constant signal $x^*(t)=0.4$, b. spectrum of the corresponding two-level PWM signal $x[t]$.

$$P_{T_s}(x[t]) = \frac{1}{T_s}\int_0^{T_s} x[t]^2 \,\mathrm{d}t = \frac{2i+1}{l-1}D - \frac{i(i+1)}{(l-1)^2} \tag{7.11}$$

where integer value i is level counter and is in the range from 0 up to $l-2$. PWM is here obtained using two adjacent voltage levels, so the value of i can be determined as $i = \lfloor D/(1/(l-1)) \rfloor$. PWM signal $x[t]$ can be created also using non-adjacent levels. However, in such a case inverter switching losses would be higher and the higher power of the PWM signal would be needed (that means that more power would be wasted, as will be explained later); a higher $\mathrm{d}v/\mathrm{d}t$ in the output leg voltage would also be generated. Note that two-level case of (7.10) is also covered by (7.11). In this case $l = 2$, and the only value for i is $i = 0$, that leads to $P_{T_s}(x[t]) = D$. Again, the position and number of pulses can be different inside the switching period T_s. This will not affect the value of the average power $P_{T_s}(x[t])$. The process of integration is represented graphically in Fig. 7.5.

The difference between the average power $P_{T_s}(x[t])$ of the multilevel PWM produced signal $x[t]$ in (7.11) and the average power $P_{T_s}(x^*(t)) = D^2$ of the reference dc signal $x^*(t) = D$ gives an additional power, contained in the multilevel PWM signal $x[t]$, to obtain on average value of D. This additional power is variable and depends on the value of D, but is always lower than in the two-level case (in the two-level case this difference was $D - D^2$). To prove this, consider the same example as in the two-level case ($D = 0.4$ and $T_s = 0.5\,\mathrm{ms}$) but now the PWM signal $x[t]$ is obtained using e.g. a five-level inverter. Spectra and powers of the reference $x^*(t)$ and of the PWM signal $x[t]$ obtained using five-level modulator are shown in Fig. 7.6.

One can see that the power of the additional harmonics is 0.175–0.16= 0.015, which is much lower than in the two-level case, 0.4–0.16= 0.24. If with a five-level inverter non-adjacent levels are used, the shape of two-level PWM signal could be easily obtained by four-level transitions. From the previous example it is clear that in this case more additional harmonics will be produced. This is one of the reasons and an explanation of the previous statement why only adjacent levels are used in the multilevel inverters. More pulses per switching period can be used but that will increase inverter switching losses; hence, this is out of the scope of

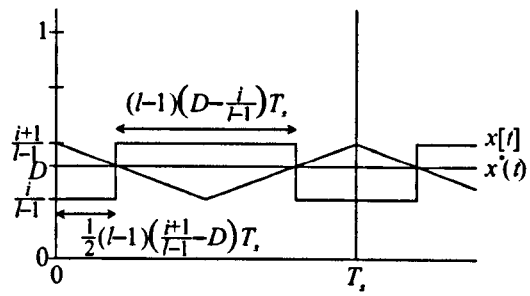


Fig. 7.4: Multilevel pulse width modulated constant signal $x^*(t)=D$.

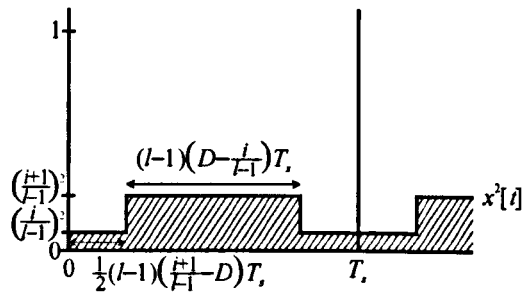


Fig. 7.5: Graphical determination of the active power of the multilevel PWM signal $x[t]$.

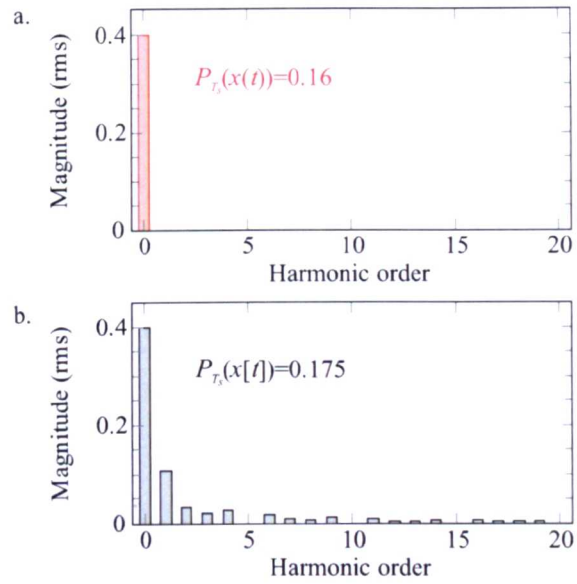


Fig. 7.6: a. Spectrum of the constant signal $x^*(t)$=0.4, b. spectrum of the corresponding PWM signal $x[t]$ obtained using a five-level modulator.

considerations here. Recall that only adjacent levels were used in all the analysed strategies in the thesis. The variation of the average power of the multilevel (2, 3, 4 and 5 level) PWM produced signal $x[t]$, using adjacent levels, for dc signal $x^*(t)$ in the range $0 \le D \le 1$, is shown in Fig. 7.7. The average power of the reference signal $x^*(t)$ is shown with thick gray dashed line.

Fig. 7.8 shows additional power, contained in the multilevel PWM signal to obtain average value of D, for 2, 3, 4 and 5 level cases. One can see that when the reference value is equal to some of the inverter levels, there is no need for PWM, hence the additional required power is 0. The values in Fig. 7.8 represent values from Fig. 7.7, reduced by D^2 (the average power of the reference dc signal D). Values from the previous example (from Fig. 7.3 and Fig. 7.6) for $D=$ 0.4 are highlighted in Fig. 7.7 and in Fig. 7.8. Local maximum values in Fig. 7.8 are $0.25/(\ell-1)^2$ [Ruderman and Reznikov (2010a)], and can be obtained by equating the first derivative of $P_{T_s}(x[t])-P_{T_s}(x^*(t))$ to zero.

Total harmonic distortion is defined with reference to the useful signal that is in this case dc value of the

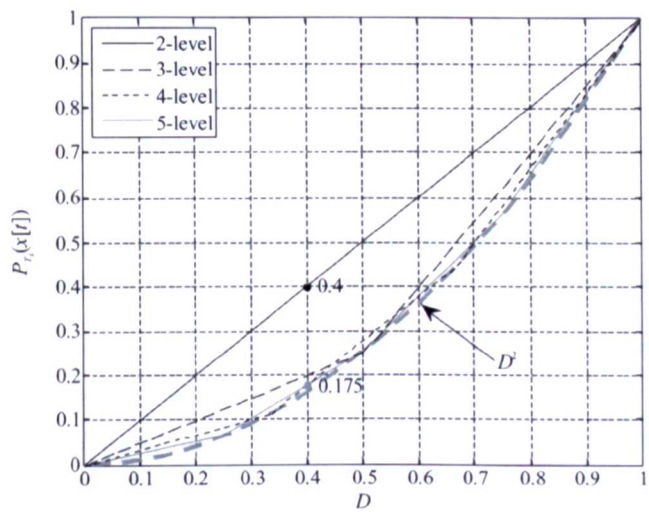


Fig. 7.7: The average power of the signal $x[t]$ obtained using multilevel PWM, whose average value is $x^*(t)=D$.

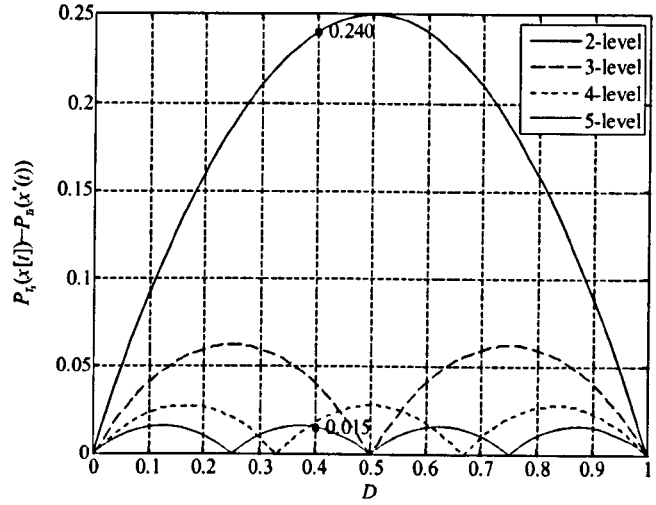


Fig. 7.8: The additional power, contained in the signal $x[t]$, produced by the multilevel PWM, to obtain dc value of D on average.

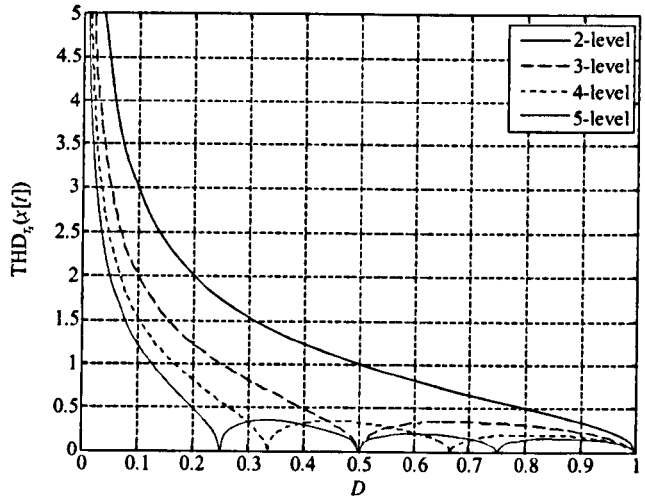


Fig. 7.9: The THD of the multilevel PWM signal $x[t]$ whose average value is $x^*(t)=D$.

obtained signal, rather than the first harmonic. Thus it can be calculated as:

$$\mathrm{THD}_{T_1}(x[t]) = \frac{\sqrt{P_{T_1}(x[t]) - P_{T_1}(x^*(t))}}{D} = \frac{\sqrt{\left(\frac{2i+1}{l-1}D - \frac{i(i+1)}{(l-1)^2}\right) - D^2}}{D} \tag{7.12}$$

Plot of $\mathrm{THD}_{T_1}(x[t])$ versus reference signal, i.e. average value D, is shown in Fig. 7.9.

7.5 AVERAGE POWER AND THD OF THE PWM SIGNAL OBTAINED BY L-LEVEL PWM VSI FOR SINUSOIDAL REFERENCE SIGNAL

The assumed reference in this section is sinusoidal signal and the results from the previous section will be used for determination of the average power of the PWM generated sinusoidal signal. As in the previous section, output leg voltage is examined, but now the whole fundamental period of the sinusoidal reference, rather than just one switching period in which reference is constant, is considered. Average power is obtained by integration of the PWM signal squared value from one switching period, throughout the whole fundamental period. The

same idea and the same result as in this section have already been shown in [Van Der Broeck (2003)] individually for 2, 3 and 5 level single-phase PWM inverter. As noted, the work of [Van Der Broeck (2003)] was extended and generalised in [Leon et al. (2004)]. However, the final integrals were actually not solved analytically, in contrast to the situation here. Hence the analytical results obtained in this section are much more convenient for use and they also encompass results of [Van Der Broeck (2003)] in a generalised manner.

The sinusoidal signal is taken as $x^*(t) = A\cos(\omega t - \varphi)$, $\omega = 2\pi/T$. Since it is assumed that the inverter levels are from 0 to 1 (in normalised form), that means that value of A must be in the range from 0 to 0.5. Also, it is assumed that the signal is centred between levels 0 and 1 during the signal period of T; that means that dc value of 0.5 should be added to $x^*(t)$. Since the phase delay of the signal is not important for these calculations, it will be assumed that $\varphi = 0$. Next, if modulation index m is defined as the ratio of the first harmonic of the reference over the half-distance of the maximum output level of the inverter (as in (3.21)), then $A = m/2$. The correlation between real reference leg voltage $v^*_{LEG}(t)$ and normalised reference leg voltage is $u^*_{LEG}(t) = v^*_{LEG}(t)/V_{dc}$ (normalisation from (3.1) is not used in this chapter). Finally, normalised leg voltage, used as the reference for production of the PWM signal, is defined as:

$$u^*_{LEG}(t) = \frac{1}{2} + \frac{m}{2}\cos(\omega t) \tag{7.13}$$

For PWM generation of the signal symmetrical regular sampling will be used. This means that produced PWM signal $u_{LEG}[t]$ will have the same average value during each switching period as the sample $u^*_{LEG}(kT_s)$ taken at the beginning of that switching period. Reference leg voltage $u^*_{LEG}(t)$, sampled reference voltage $u^*_{LEG}(kT_s)$, and produced leg voltage $u_{LEG}[t]$ are shown in Fig. 7.10a. Since the signal is constant during each switching period T_s, the average power of the PWM sinusoidal signal (obtained leg voltage $u_{LEG}[t]$), during fundamental period T, can be calculated as an average value of the average powers of the dc signals from each switching period T_s. In other words, results from the previous section can be used here, with the value of D in

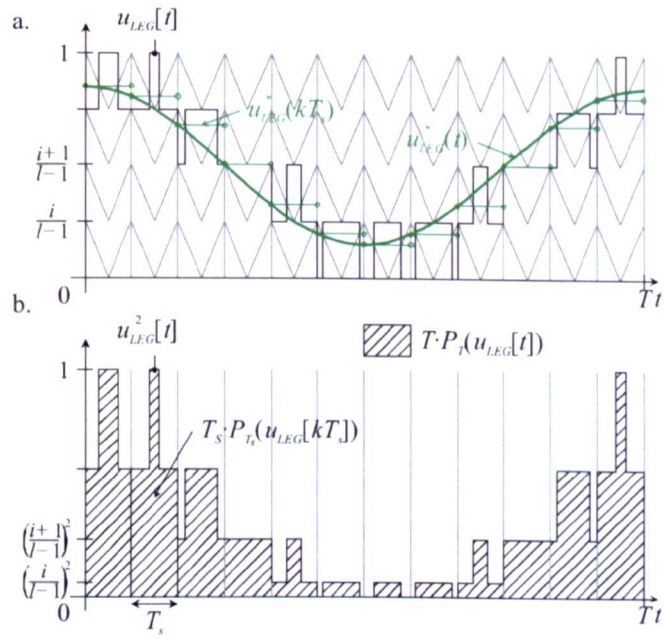


Fig. 7.10: a. Normalised reference leg voltage $u^*_{LEG}(t)$ and l-level VSI generated output leg voltage $u_{LEG}[t]$.
b. Graphical determination of the average power of the obtained leg voltage.

each switching period determined as $D(k)=u^*_{LEG}(kTs)$.

Hence the average power of the produced leg voltage during one period of the fundamental T is:

$$P_T(u_{LEG}[t])=\frac{1}{K}\sum_{k=1}^{K}P_{T_s}(u_{LEG}[kT_s]) \tag{7.14}$$

where K is the number of samples during one period of the signal, $K=\lfloor T/T_s \rfloor$. Calculation of $P_T(u_{LEG}[t])$ is graphically represented in Fig. 7.10b. Replacing the value of $P_{T_s}(u_{LEG}[kT_s])$ with (7.11), and taking into account that $D(k)=u^*_{LEG}(kT_s)=1/2+(m/2)\cos(\omega kT_s)$, one gets:

$$P_T(u_{LEG}[t])=\frac{1}{K}\sum_{k=1}^{K}\left(\frac{2i+1}{l-1}u^*_{LEG}(kT_s)-\frac{i(i+1)}{(l-1)^2}\right) \tag{7.15}$$

where i is governed with $i=\lfloor u^*_{LEG}(kT_s)/(1/(l-1))\rfloor$. This expression covers both two-level and multilevel cases. If the sampling period T_s is much smaller than the period of the signal T, then formulae (7.14) and (7.15) can be written in integral form:

$$P_T(u_{LEG}[t])=\frac{1}{T}\int_{t=0}^{T}P_{T_s}(u_{LEG}[t])\mathrm{d}t=\frac{1}{T}\int_{t=0}^{T}\left(\frac{2i+1}{l-1}u^*_{LEG}(t)-\frac{i(i+1)}{(l-1)^2}\right)\mathrm{d}t \tag{7.16}$$

where reference leg voltage $u^*_{LEG}(t)$ is as in (7.13) and integer value $i=\lfloor u^*_{LEG}(t)/(1/(l-1))\rfloor$.

Since integer value of i is dependent on $u^*_{LEG}(t)$, equation (7.16) has to be solved piece-wise. Note also that (7.16) is valid for any shape of the reference leg voltage $u^*_{LEG}(t)$ whose PWM signal $u_{LEG}[t]$ is obtained using adjacent levels, as explained in the section 7.4. Based on the results of the previous section one can see that the position of the pulse inside the switching period T_s is still unimportant. This practically means that if in an l-level inverter modulation strategy uses only adjacent voltage levels to switch, and if the step of the output voltage is constant, then power of the obtained leg voltage will be the same regardless of the particular applied modulation strategy. For example, if carrier-based methods are considered, this means that PD, POD, APOD will have the same $P_T(u_{LEG}[t])$. Of course, this only holds true if the ratio of f_s/f is high.

The analytical solution of (7.16) can be easily obtained for pure sinusoidal signal and for 2 and 3 levels. For the two-level case ($l=2$) the value of i is constant during the whole period $0\le\omega t\le 2\pi$, and is equal to 0. In the three-level case ($l=3$) the value of i is constant during the specific intervals: $i=1$ for $0\le\omega t\le\pi/2$, $i=0$ for $\pi/2\le\omega t\le 3\pi/2$ and $i=1$ for $3\pi/2\le\omega t\le 2\pi$. Analytical solutions of (7.16) for the two- and three-level cases are:

$$\begin{aligned}P_T(u_{LEG,2}[t])&=\frac{1}{2}\\ P_T(u_{LEG,3}[t])&=\frac{1}{4}+\frac{m}{2\pi}\end{aligned} \tag{7.17}$$

For more than three-levels value of i and intervals of integration in (7.16) become dependent on the value of m and finding analytical solution becomes more difficult. Thus (7.16) has to be evaluated part-by-part, with the borders of integration being dependent on m. If l is an odd number, the borders between these integration segments, for example in 7-level case, are when modulation index becomes greater than $m_1=1/3$ and when it becomes greater than $m_2=2/3$. Generally, this means that these borders for odd l appear at $m_k=2k/(l-1)$, and similarly for even l at $m_k=(2k-1)/(l-1)$. Value of index k is in the range from $k=1$ to $\lfloor l/2\rfloor-1$.

After individual evaluation of (7.16) for the average power of the PWM signal, obtained for sinusoidal reference signal with multilevel inverter with odd (l = 3, 5, 7, and 9) number of levels, and with even (l = 2, 4, 6, and 8) number of levels, a generalised expression was formulated. The following variables are introduced first:

$$A_0 = \begin{cases} 1/4 + m/(\pi(l-1)) & \text{for odd } l \\ 1/2 - l(l-2)/(4(l-1)^2) & \text{for even } l \end{cases}$$
$$A_k = \frac{2}{\pi(l-1)} \cdot (m \sin\tau_k - m_k \tau_k) \tag{7.18}$$

where $\tau_k = \arccos(m_k/m)$ and where $\sin\tau_k$ can be expressed using a basic trigonometry as $\sqrt{1-(m_k/m)^2}$. One finds that after using values defined in (7.18), $P_T(u_{LEG,l}[t])$ (or, shortly, just $P_{T,LEG}$) for any number of levels l can be expressed as:

$$P_{T,LEG} = \begin{cases} A_0 & 0 \le m \le m_1 \\ A_0 + A_1 & m_1 \le m \le m_2 \\ A_0 + A_1 + A_2 & m_2 \le m \le m_3 \\ \vdots & \vdots \\ A_0 + A_1 + \ldots + A_{\lfloor \frac{l}{2} \rfloor - 1} & m_{\lfloor \frac{l}{2} \rfloor - 1} \le m \le 1 \end{cases} \tag{7.19}$$

The analytical solutions for two- and three-level case (7.17) are also covered by (7.19). Plot of the $P_T(u_{LEG}[t])$ for sinusoidal reference voltage (7.13) versus m obtained by analytical formula (7.19) is given in Fig. 7.11.

As an example of using (7.19), a seven-level case, not shown in Fig. 7.11, is addressed. Variable k is in the range $k=1$ to $\lfloor 7/2 \rfloor - 1 = 2$, and values of $m_k = 2k/(7-1)$ are: $m_1 = 1/3$ and $m_2 = 2/3$. Thus (7.19) for the seven-level case becomes:

$$P_T(u_{LEG,7}[t]) = \begin{cases} A_0 & 0 \le m \le 1/3 \\ A_0 + A_1 & 1/3 \le m \le 2/3 \\ A_0 + A_1 + A_2 & 2/3 \le m \le 1 \end{cases} \tag{7.20}$$

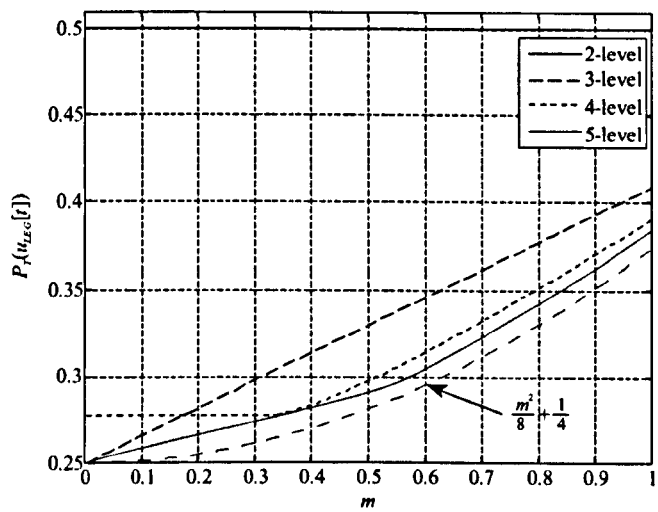


Fig. 7.11: Average power of the leg voltage $u_{LEG}[t]$, obtained by an ideal PWM l-level VSI, for sinusoidal reference $u_{LEG}(t)=1/2+m/2\cos(\omega t)$.

where variables A_0, A_1 and A_2 are determined by (7.18) as:

$$A_0 = \frac{1}{4} + \frac{m}{\pi(7-1)}$$

$$A_1 = \frac{2}{\pi(7-1)} \cdot \left(m\sqrt{1-\left(\frac{1}{3m}\right)^2} - \frac{1}{3}\arccos\left(\frac{1}{3m}\right) \right)$$

$$A_2 = \frac{2}{\pi(7-1)} \cdot \left(m\sqrt{1-\left(\frac{2}{3m}\right)^2} - \frac{2}{3}\arccos\left(\frac{2}{3m}\right) \right)$$

This confirms that the expression (7.19) is general and applicable to any number of levels. This is in contrast to [Van Der Broeck (2003)] where only particular solutions for two, three and five levels were given. In [Leon et al. (2004)] the analytical derivations finished with integral equation (7.16), with defined borders for piece-wise integration τ_k, so that no general analytical expression of the form of (7.19) was derived. Thus the equations (7.18)-(7.19) describe the generalised solution, that is exposed here for the first time.

Note that, for an even number of levels l, the term A_0 that represents $P_T(u_{LEG,l}[t])$ for small modulation index values (less than $m_1 = 1/(l-1)$) is independent of m. This is expected since the signal stays in the two-level zone, and, as shown for the two-level case, it has the constant value of 1/2. The value in multilevel case is 1/2 minus a certain value (see A_0 in (7.18) for even l), because this zone represents two-level operation part of the multilevel inverter and operating levels are closer than in the two-level case.

The average power of the sinusoidal reference leg voltage $u^*_{LEG}(t)$ can be obtained using the same principle as in (7.16), i.e. by integration of the average powers of the dc signal in one switching period (equal to D^2) throughout fundamental period T, $P_T(u^*_{LEG}(t)) = 1/T\int_{t=0}^{T} D^2(t)\mathrm{d}t$. Alternatively, it can be directly calculated by using (7.1). One gets that:

$$P_T(u^*_{LEG}(t)) = \frac{m^2}{8} + \frac{1}{4} \tag{7.21}$$

Average power of the reference sinusoidal signal (7.21) versus modulation index m is also shown in Fig. 7.11. The difference between the average power of the pulse width modulated signal (7.19) and the average power of the reference sinusoidal signal (7.21), $P_T(u_{LEG}[t]) - P_T(u^*_{LEG}(t))$ ("wasted power") for $l = 2$ to 5 is shown in Fig. 7.12.

Now, the first component of the spectrum U_1, i.e. the sinusoidal signal with phase ωt, should be considered as the useful signal, so the total harmonic distortion can be defined with reference to U_1. Also, dc component is related to the point of referencing and it will not therefore be considered in the THD as a "distorting" component. The fundamental and the dc component form the power of the reference signal $P_T(u^*_{LEG}(t))$ as in (7.21). Similarly as in (7.12), the THD can now be defined as:

$$\mathrm{THD}_T(u_{LEG}[t]) = \frac{\sqrt{P_T(u_{LEG}[t]) - P_T(u^*_{LEG}(t))}}{U_{LEG,rms,1}} \tag{7.22}$$

where $U_{LEG,rms,1}$ represents the RMS value of the fundamental component in the spectrum, $U_{LEG,rms,1} = 1/\sqrt{2} \cdot (m/2)$. Plot of $\mathrm{THD}_T(u_{LEG}[t])$ versus modulation index m is shown in Fig. 7.13.

Results for the additional power cost, that is a necessity in the PWM process, shown in Fig. 7.12, and for THD (Fig. 7.13), are in very good agreement with those presented in [Van Der Broeck (2003)] and [Leon et al.

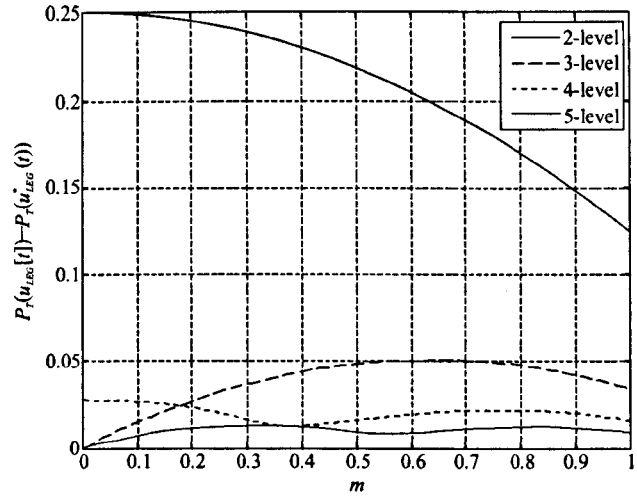


Fig. 7.12: Additional power, contained in the $u_{LEG}[t]$ produced by an ideal PWM l-level VSI, to obtain $u^*_{LEG}(t)=1/2+m/2\cos(\omega t)$ on average.

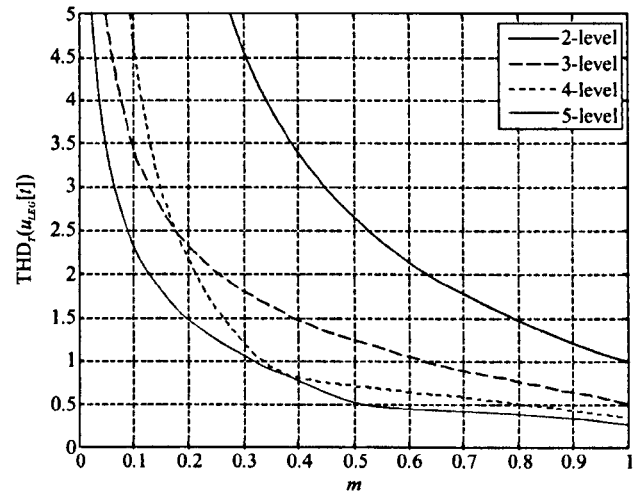


Fig. 7.13: THD of the leg voltage $u_{LEG,l}[t]$, generated by an ideal PWM l-level VSI, for sinusoidal reference leg voltage $u^*_{LEG}(t)=1/2+m/2\cos(\omega t)$.

(2004)]. Note that values in Fig. 7.12 are 1/4 of KU factor calculated in [Leon et al. (2004)] because of the assumed $\pm V_{dc}$ dc-bus voltage notation, instead of 0 to V_{dc} that is used here. Since this factor cancels in THD calculation, corresponding values for the THD are identical.

The five-level case for different carrier-based modulation strategies was covered in [Agelidis and Calais (1998)]. The THD values given in [Agelidis and Calais (1998)] are slightly lower than in Fig. 7.13, which could be a consequence of not taking all the harmonics into consideration. Also, a low f_s/f ratio was analysed, so for some values of f_s/f the difference between analysed leg voltage THDs appear. However, it is confirmed here that if the ratio of f_s/f is high enough, then the analysed carrier based methods (PD, POD, APOD, etc.) will produce the same $P_T(u_{LEG}[t])$ and thus the same THD. It should be noted here that with PD, POD, and APOD carrier dispositions some broader sets of carriers may be considered. More specifically, it is not necessary that falling and rising slope of the carrier have the same duration. For PD-PWM all carriers must be in phase and just be shifted by a level. That means that sawtooth carrier can be used as well (although it will not, because of the multiple leg switchings on the vertical edge). For POD and APOD, carriers that are in anti-phase must represent mirror images, and slope duration division is not important.

7.6 MULTIPHASE TWO- AND THREE-LEVEL PHASE VOLTAGE AVERAGE POWER AND THD

In this section multiphase (including three-phase) case will be considered. The results from the previous section and the general formula (7.19) will be used to obtain a general expression for the average power and THD of the phase voltages, produced by the PWM multilevel multiphase inverter. As mentioned, for the sake of generalisation, voltage values normalised with respect to the dc-bus voltage will be used, $u=v/V_{dc}$. Normalised reference voltages are assumed to be a symmetrical set of n (n being the phase number) sinusoidal signals:

$$\begin{aligned} u^*_{ph}(t) &= \frac{m}{2}\cos\left(\omega t - \frac{2\pi}{n}(k-1)\right) \\ u^*_{LEG}(t) &= \frac{1}{2} + \frac{m}{2}\cos\left(\omega t - \frac{2\pi}{n}(k-1)\right) \end{aligned} \tag{7.23}$$

where $ph = a, b, c, \ldots, n$, LEG stands for the corresponding leg $LEG = A, B, C, \ldots, N$, and k is the phase/leg index $k = 1$ to n. Position of the pulse inside the switching period was not important until now. However, since the phase voltages are obtained by combination of a number of leg voltages, the pulse position now becomes important, as it will be shown later on for the PD, POD and APOD cases. Due to the already mentioned reasons, further analysis will be given only for the PWM methods that use two adjacent levels for creating leg voltages.

Considered topology is a star-connected symmetrical load. Because the load is the same in all phases, phase voltages can be expressed as in (3.7), i.e. as:

$$u_{ph}[t] = u_{LEG}[t] - \frac{\sum u_{LEG}[t]}{n} = u_{LEG}[t] - u_{CMV}[t] \tag{7.24}$$

Leg voltages $u_{LEG}[t]$ are obtained from reference leg voltages $u^*_{LEG}(t)$, by application of a particular PWM technique.

Calculation of the average power of a signal requires the signal's squared value. To obtain the average power of the phase voltage (7.24), general expression (7.3) can be used:

$$P_T(u_{ph}[t]) = \frac{1}{T}\int_0^T u^2_{ph}[t]\,\mathrm{d}t = \frac{1}{T}\int_0^T (u^2_{LEG} - 2u_{LEG}u_{CMV} + u^2_{CMV})\,\mathrm{d}t \tag{7.25}$$

It can be shown that if the produced leg voltages form a symmetrical n-phase system (identical waveforms in all legs, with only the difference in the phase shift of $2\pi/n$ between consecutive legs), then $1/T\int_0^T u_{LEG}u_{CMV}\,\mathrm{d}t = 1/T\int_0^T u^2_{CMV}\,\mathrm{d}t$; this term is denoted further on as $P_T(u_{CMV}[t])$. The first part of the integral in (7.25) represents $P_T(u_{LEG}[t])$ and it can be calculated using (7.19). This leads to:

$$P_T(u_{ph}[t]) = P_T(u_{LEG}[t]) - P_T(u_{CMV}[t]) \tag{7.26}$$

which represents an expected result.

Since $P_T(u_{LEG}[t])$ is determined by (7.19), the problem of finding $P_T(u_{ph}[t])$ according to (7.26) can be reduced to calculation of the $P_T(u_{CMV}[t])$. For calculation of $P_T(u_{CMV}[t])$ the starting point is again (7.3):

$$P_T(u_{CMV}[t]) = \frac{1}{T}\int_0^T u^2_{CMV}\,\mathrm{d}t = \frac{1}{T}\int_0^T \frac{\left(\sum_{I=A}^{N} u_I\right)^2}{n^2}\mathrm{d}t = \frac{1}{T}\int_0^T \frac{\sum_{I=A}^{N} u_I^2 + \sum_{I,J=A,I\neq J}^{N} u_I u_J}{n^2}\mathrm{d}t \tag{7.27}$$

Since obtained leg voltages are symmetrical, then $P_T(u_I)=1/T\int_0^T u_I^2\mathrm{d}t$ is the same for every I and represents $P_T(u_{LEG}[t])$, so that it can be calculated with (7.19). Also, because of symmetry, values of $P_T(u_Iu_J)=1/T\int_0^T u_Iu_J\mathrm{d}t$ are identical for the same angular span between phases. If the phase angle between phases $2\pi/n$ is denoted with α, then the angle span between phases I,J ($I\neq J$) can take discrete values of $\Lambda\alpha$, where $\Lambda=1,2,\ldots,\lfloor n/2\rfloor$. Finally this means that the values of $P_T(u_Iu_J)$ are mutually equal for the same Λ. For example, in the five-phase case for $\Lambda=1$, $P_T(u_Au_B)=P_T(u_Bu_A)=P_T(u_Bu_C)=\ldots=P_T(u_Iu_J,1)$ and for $\Lambda=2$, $P_T(u_Au_C)=P_T(u_Cu_A)=P_T(u_Bu_D)=\ldots=P_T(u_Iu_J,2)$. For each Λ there are exactly $2n$ pairs of I,J that have the same $P_T(u_Iu_J,\Lambda)$ except for the last $\Lambda=n/2$ for even n, for which there are n pairs of I,J with the same value of $P_T(u_Iu_J,n/2)$. Graphical proof of this statement for the five- and six-phase cases (odd and even n) is shown in Fig. 7.14. Taking this into account, (7.27) can be rewritten as:

$$P_T(u_{CMV})=\frac{1}{n}P_T(u_{LEG})+\frac{1}{n}\sum_{\Lambda=1}^{\left\lfloor\frac{n}{2}\right\rfloor}K_\Lambda P_T(u_Iu_J,\Lambda) \tag{7.28}$$

Coefficient K_Λ in (7.28) is equal to 2 for every $1\leq\Lambda<n/2$, while for $\Lambda=n/2$ (that exists only for even n) it is equal to $K_{n/2}=1$. Generally, K_Λ can be expressed e.g. as $K_\Lambda=1+\lceil|\sin\Lambda\alpha|\rceil$. With the introduced parameter Λ one can say that $P_T(u_{LEG})$ can be written as $P_T(u_Iu_J,0)$. This can be used for further simplification of (7.28) to only the second term where the start of the sum should be changed to Λ=0, and where K_0=1. However, use of value Λ=0 will be avoided in what follows.

Substituting (7.28) into equation for the phase voltage average power (7.26), one gets:

$$P_T(u_{ph})=\frac{n-1}{n}P_T(u_{LEG})-\frac{1}{n}\sum_{\Lambda=1}^{\left\lfloor\frac{n}{2}\right\rfloor}K_\Lambda P_T(u_Iu_J,\Lambda) \tag{7.29}$$

This means that the problem of calculation of the phase voltage and CMV average powers is reduced now to calculation of the $P_T(u_Iu_J)$, i.e. calculation of $P_T(u_Iu_J,\Lambda)$.

Value of $P_T(u_Iu_J)$ can be calculated in a similar manner as used for the average power calculation of the sinusoidal signal in 7.5. Because u_I and u_J are PWM leg voltage square-waveform signals (Fig. 7.15a, Fig. 7.16a and Fig. 7.16c), this means that the process will start again with a switching period and progress with further integration throughout the whole fundamental period. The area under the product of two switching signals has to be calculated; thus position of the pulses inside switching period T_s now becomes important. The

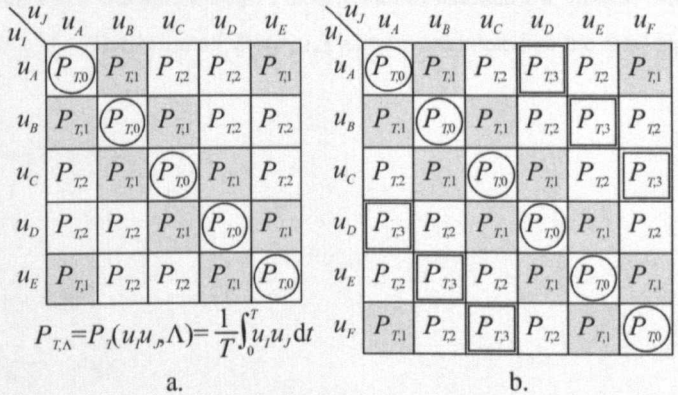


Fig. 7.14: Graphical representation of (7.27) for the a. five- and b. six-phase case. $P_T(u_{CMV}[t])$ is equal to the sum of all the elements in table.

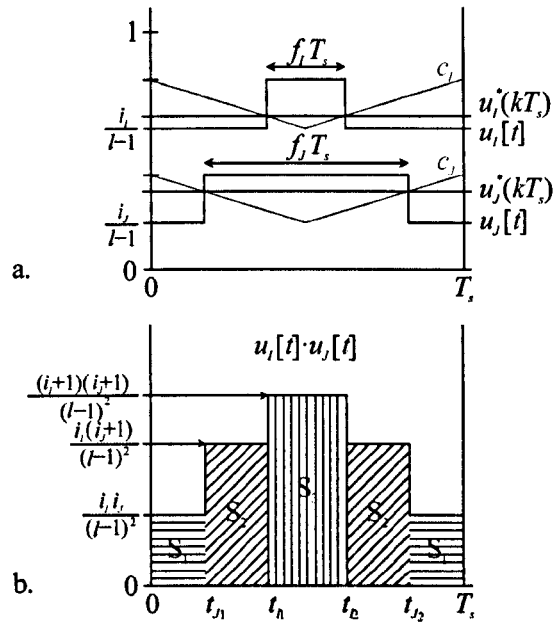


Fig. 7.15: Graphical interpretation of the calculation of $P_{T_s}(u_I u_J)$ if carriers are in phase. a. Reference signals and produced PWM signals. b. Product of the produced reference signals. One switching period T_s is shown.

most typical dispositions of the carriers are PD, POD and APOD. However, for calculation of $P_{T_s}(u_I u_J)$ the only important issue is the mutual disposition of the carriers c_I and c_J, in a particular switching period T_s, with which the reference signals u_I^* and u_J^*, respectively, are compared. The case when c_I and c_J are in phase is shown in Fig. 7.15, while Fig. 7.16 illustrates situation when they are in counter-phase. One switching period T_s is shown.

Graphical process of calculation of $P_{T_s}(u_I u_J)$ during one switching period T_s when c_I and c_J are in phase is shown in Fig. 7.15b. Values of i_I, f_I and i_J, f_J are defined as:

$$i_{I,J} = \left\lfloor \frac{u_{I,J}^*(kT_s)}{1/(l-1)} \right\rfloor$$
$$f_{I,J} = \frac{u_{I,J}^*(kT_s) - i_{I,J}/(l-1)}{l-1} \tag{7.30}$$

Integer parameter $i_{I,J}$ takes values $0,1,2,\ldots,(l-2)$, while fractional part is in the range $0 \le f_{I,J} < 1$.

The shaded area has to be calculated next. For the sake of calculation, shaded blocks can be rearranged in the order: S_1, S_1, S_2, S_2, S_3. The value of $P_{T_s}(u_I u_J)$ can be calculated as the total shaded area divided by the switching period T_s:

$$P_{T_s}(u_I u_J) = (2S_1 + 2S_2 + S_3)/T_s \tag{7.31}$$

where:

$$2S_1 = \frac{i_I i_J}{(l-1)^2}(1-f_J)T_s$$
$$2S_2 = \frac{i_I(i_J+1)}{(l-1)^2}(f_J - f_I)T_s$$
$$S_3 = \frac{(i_I+1)(i_J+1)}{(l-1)^2} f_I T_s$$

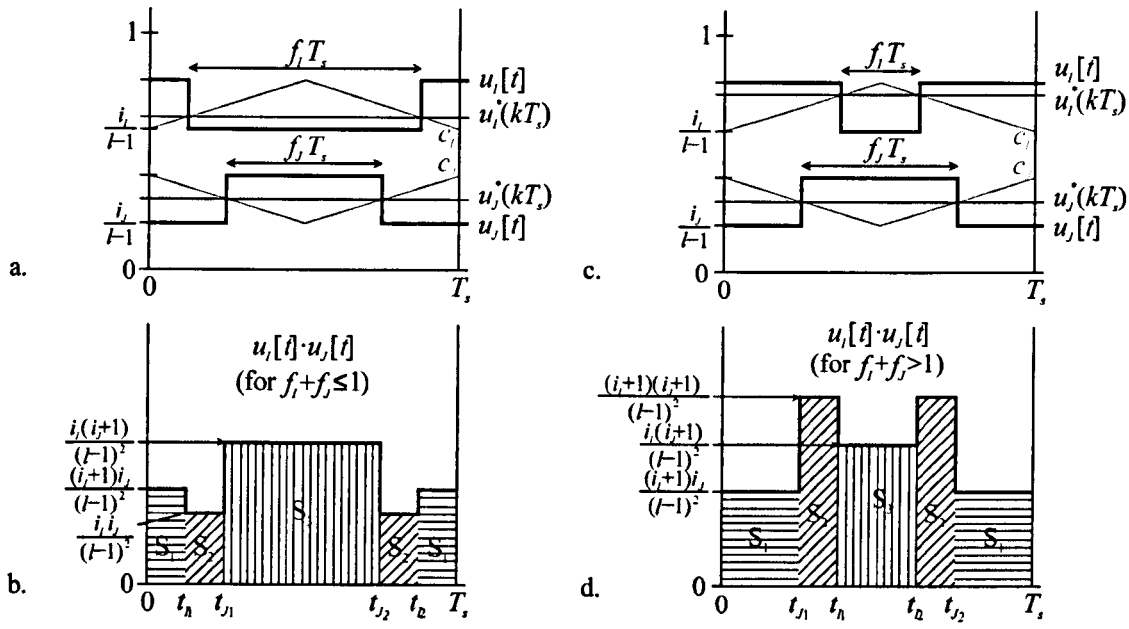


Fig. 7.16: Graphical interpretation of calculation of $P_{T_s}(u_I u_J)$ when carriers are in counter-phase. a. Reference signals and produced PWM signals and b. product of the produced reference signals, if $f_I+f_J\leq 1$; c. Reference signals and produced PWM signals and d. product of the produced reference signals, if $f_I+f_J>1$. One switching period T_s is shown.

After simplification of (7.31) one gets:

$$P_{T_s}(u_I u_J)=\frac{1}{(l-1)^2}(i_I i_J+i_I f_J+i_J f_I+f_I) \tag{7.32}$$

In the given example in Fig. 7.15 the signal $u_I^*(kT_s)$ has a smaller fractional part ($f_I < f_J$). Because of that, the last term in the sum in brackets in (7.32) is f_I. If one wants to generalise (7.32), then it can be rewritten as:

$$P_{T_s}(u_I u_J)=\frac{1}{(l-1)^2}(i_I i_J+i_I f_J+i_J f_I+f_{smaller}) \tag{7.33}$$

where $f_{smaller}=\min(f_I,f_J)$.

Similarly as in section 7.5, $P_T(u_I u_J)$ during one fundamental period can be obtained as integral of $P_{T_s}(u_I u_J)$. Integrals of $i_I f_J$ and $i_J f_I$ during the fundamental period are the same because of the symmetry, so that one gets:

$$P_T(u_I u_J)=\frac{1}{(l-1)^2}\left(\frac{1}{T}\int_0^T i_I i_J\,\mathrm{d}t+\frac{2}{T}\int_0^T i_I f_J\,\mathrm{d}t+\frac{1}{T}\int_0^T f_{smaller}\,\mathrm{d}t\right)=\frac{1}{(l-1)^2}(P_{ii}'+2P_{if}'+P_{f_s}') \tag{7.34}$$

Thus $P_T(u_I u_J)$ can be determined by calculation of three integrals P_{ii}', P_{if}' and P_{f_s}' in (7.34). Primed symbol is used as a reminder that these values have to be divided by the factor $(l-1)^2$.

The situation when carriers c_I and c_J are in counter-phase in a particular switching period is shown in Fig. 7.16. Values of $i_{I,J}$ and $f_{I,J}$ remain as in (3.30). Graphical calculation of $P_{T_s}(u_I u_J)$ is shown in Fig. 7.16b and Fig. 7.16d. One can see that two cases have to be considered, when $f_I+f_J\leq 1$ (Fig. 7.16a and Fig. 7.16b) and when $f_I+f_J>1$ (Fig. 7.16c and Fig. 7.16d). Similarly as in (7.31), the area of $2S_1+2S_2+S3$ can be calculated. One gets that:

$$P_{T_s}(u_I u_J) = \frac{1}{(l-1)^2}\left(i_I i_J + i_I f_J + i_J f_I + \begin{cases} 0 & f_I + f_J \le 1 \\ f_I + f_J - 1 & f_I + f_J > 1 \end{cases}\right) \tag{7.35}$$

Form of (7.35) is very similar to the one of (7.33), the only difference being in the last term of the summation in brackets. As when the carriers are in phase, the expression (7.35) has to be integrated during the fundamental period to obtain the average power of the product of the PWM signals u_I and u_J ($P_T(u_I u_J)$). Here some care has to be exercised. Most frequently signals u_I^* and u_J^* do not belong to the carriers that are in counter-phase during the whole fundamental period. This means that in some intervals, when references belong to the carriers that are in phase, or to the same carrier, $f_{smaller}$ has to be integrated as the last term in the summation in brackets. When references are compared with carriers that are in counter-phase and if $f_I + f_J \le 1$, the last term is 0, i.e. if $f_I + f_J > 1$, $(f_I + f_J - 1)$ has to be integrated as the last term in (7.34). This will be explained using the three-level case as an example, with carriers in POD, i.e. in APOD (these two are equivalent in the three-level case).

From the previous analysis one can see that the position of pulses inside the switching period T_s becomes important. For different position of pulses different area under $u_I u_J$ curve, i.e. $P_{T_s}(u_I u_J)$, will be obtained, see (7.33) and (7.35). If the carriers are in phase (Fig. 7.15), then the area, i.e. the value of $P_{T_s}(u_I u_J)$, is greater than if the carriers are in counter-phase, Fig. 7.16 (proof: $\min(f_I, f_J) > f_I + f_J - 1$ for $0 \le f_I, f_J < 1$). A consequence of this is that after integration over the fundamental period the obtained value of $P_T(u_I u_J)$ will be greater for PD-PWM than for POD- or APOD-PWM for any pair of I and J. Referring this back to (7.29), where these terms appear with minus sign, this means that PD-PWM will produce phase voltages that contain less power than those produced by POD and APOD carrier dispositions. This is in agreement with conclusions of [Carrara et al. (1992)]. In [Carrara et al. (1992)] double Fourier transformation analysis of the leg voltages has been done. It was shown that PD-PWM localises high amount of energy at the multiples of the switching frequency and, since those harmonics cancel in phase voltages, PD-PWM has been proposed as superior when compared to the POD and APOD. The same conclusion is obtained here through the time domain analysis, and through the spectral analysis in [Carrara et al. (1992)], thanks to the Parseval's theorem (7.6) that links a signal power in the time and in spectral domains.

Functions $i_{I,J}$ are of the square-wave shape and for more than three levels are dependent on the modulation index value. Variables $f_{I,J}$ are also time and modulation index dependent. This makes calculation of the integrals in $P_T(u_I u_J)$, in (7.34), more difficult for a general l-level case. However, the situation is simpler for two- and three-level cases, which will be analysed in more detail in the following sub-sections.

7.6.1 TWO-LEVEL CASE

For the two-level case values of $i_{I,J}$ are 0 at all times, so the first two integrals in (7.34) are zero ($P_{ii}' = 0$ and $P_{if}' = 0$). Since only one carrier exists, carriers c_I and c_J for any two considered phases I and J are always in phase. Thus the third integral can be calculated easily by integration of the $f_{smaller}$ during the whole fundamental period. One gets that:

$$P_{f_s}' = \frac{1}{2\pi}\left(\pi - 2m\sin\frac{\Lambda\pi}{n}\right) \tag{7.36}$$

An analytical solution for the phase and CMV voltage, for the two-level case and any number of phases, is obtained in this way. $P_T(u_{ph})$ is given with (7.29) where $P_T(u_{LEG})$ is defined by (7.19), which for the two-level case equals $A_0(l=2) = 1/2$, see (7.17), and $P_T(u_I u_J, \Lambda)$ is equal to the value in (7.36) since the multiplier

$1/(l-1)^2$ in (7.34) for $l=2$ is 1 and the other two integrals are equal to zero. Also note here that for $\Lambda=0$, $P_T(u_I u_J,0)=1/2$, which corresponds to $P_T(u_{LEG})$. Finally, (7.29) for the two-level case becomes:

$$P_T(u_{ph})=\frac{m}{n\pi}\sum_{\Lambda=1}^{\left\lfloor\frac{n}{2}\right\rfloor}K_\Lambda \sin\frac{\Lambda\pi}{n} \tag{7.37}$$

where $K_\Lambda=2$ for every Λ, i.e. $K_\Lambda=1$ if $\Lambda=n/2$ that exists only if n is an even number. The value of $P_T(u_{CMV})$ can be expressed in a very similar way using (7.28), or simply by substituting (7.17) for the two-level case and (7.37) into (7.26).

7.6.2 THREE-LEVEL PD-PWM CASE

For a three-level case the situation is somewhat more involved. Calculation of $P_{T_s}(u_I u_J)$ depends on the carrier disposition. Thus PD-PWM disposition will be analysed first; this will be followed by the consideration for POD, which is in the three-level case equivalent to APOD, in the following sub-section.

For PD-PWM, for any set of I and J carriers, c_I and c_J are in phase. Hence $P_{T_s}(u_I u_J)$ will be calculated as in Fig. 7.15, i.e. using (7.33) and $P_T(u_I u_J)$ will be calculated by integration of (7.33) over the whole fundamental period, as in (7.34). As an illustration, Fig. 7.17, which is given for the three-level five-phase case for $\Lambda=1$ and for $u_I=u_A$ and $u_J=u_B$, will be used.

The value of the first integral in (7.34) is independent of the modulation index value and carrier disposition and is equal to:

$$P'_{ii}=\frac{1}{2}-\frac{\Lambda}{n} \tag{7.38}$$

Graphically, this value represents area S'_{ii} in Fig. 7.17b divided by the period of the signal T, i.e. by 2π. This can be easily calculated since reference u^*_A has integer value of 1 from $\omega t=-\pi/2+2\pi k$ to $\pi/2+2\pi k$ (where k is an integer number), otherwise it is zero. References u^*_B and u^*_C have the integer value 1 from $\omega t=\Lambda\alpha-\pi/2+2\pi k$ to $\Lambda\alpha+\pi/2+2\pi k$, otherwise they are zero. For $\Lambda=1$, value of $i_A i_B$ is 1 from $\omega t=1\alpha-\pi/2+2\pi k$ to $\pi/2+2\pi k$, and for $\Lambda=2$, value of $\omega t=i_A i_C$ is 1 from $2\alpha-\pi/2+2\pi k$ to $\pi/2+2\pi k$. That means that $i_A i_B$ is 1 for interval $\pi-1\alpha$, and $i_A i_C$ is 1 for $\pi-2\alpha$, or in general case $\pi-\Lambda\alpha$. Thus the average value of $1/T\int_0^T i_I i_J \mathrm{d}t$ is $1/(2\pi)(\pi-\Lambda\alpha)$, that represents (7.38).

The second integral can also be easily determined since the limits of integration remain constant in the three-level case for any modulation index value and for any value of I and J. This term exists and is equal for both dispositions of carriers, i.e. c_I and c_J in phase or c_I and c_J in counter-phase. As a graphical illustration for calculation of P'_{if}, Fig. 7.17c can be used ($P'_{if}=S'_{if}/(2\pi)$). As an example, in the five-phase case, let us consider $f_A i_B$ and $f_A i_C$, i.e. $\Lambda=1$ and $\Lambda=2$, which includes the whole set of Λ values for the five-phase case. References u^*_B and u^*_C have integer value 1 from $\omega t=\Lambda\alpha-\pi/2+2\pi k$ to $\Lambda\alpha+\pi/2+2\pi k$, otherwise they are zero. Hence, only the integral of f_A between these borders (when i_B, i.e. i_C is 1) should be calculated. Note that f_A has a value of $(l-1)(m/2)\cos(\omega t)$, i.e. $m\cos(\omega t)$ (since $l=3$), for $-\pi/2+2\pi k\le\omega t\le\pi/2+2\pi k$, while in the other half-period it is $1+m\cos(\omega t)$. One can see that all the borders of integration are constant, so that ($\tau=\omega t$):

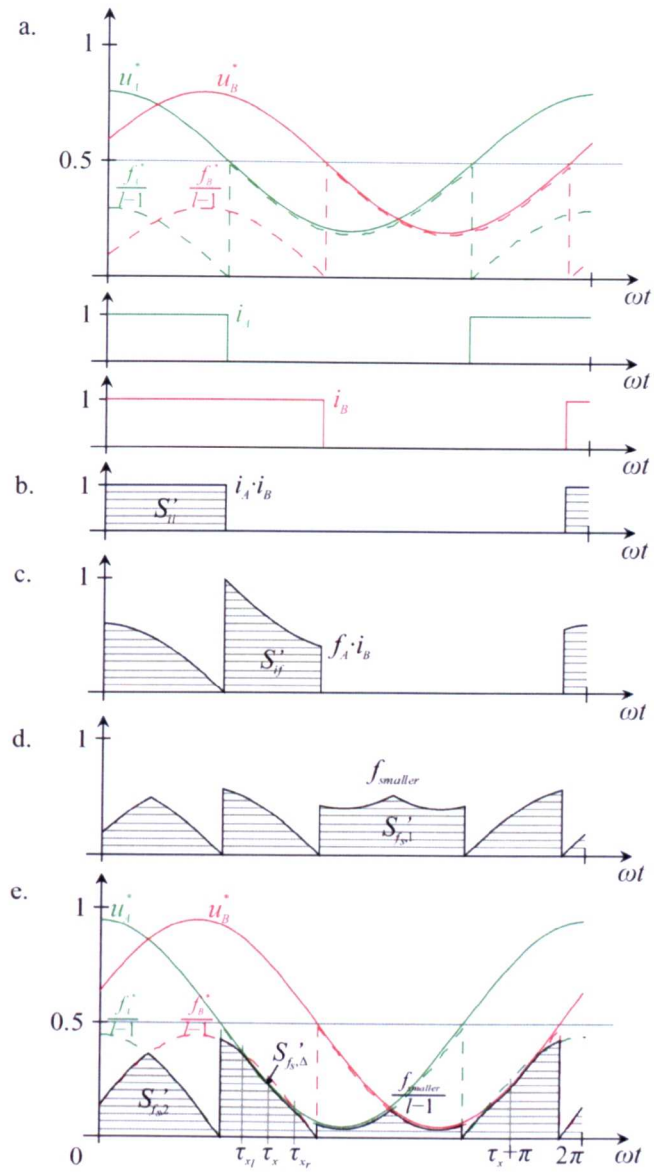


Fig. 7.17: a. Leg voltage reference signals u_A^* and u_B^* (Λ=1) with fractional (f_A, f_B, l=3) and integer (i_A, i_B) parts. b. $i_A i_B$ product. c. $f_A i_B$ product. Calculation of P'_{f_s} term of (7.34) for PD-PWM: d. $f_{smaller}$ for $0 \le m \le 1/m_x$ and e. $f_{smaller}$ for $1/m_x < m \le 1$.

$$P'_{if} = \frac{1}{2\pi}\left(\int_{\Lambda\alpha-\frac{\pi}{2}}^{\frac{\pi}{2}} m\cos\tau \,\mathrm{d}\tau + \int_{\frac{\pi}{2}}^{\Lambda\alpha+\frac{\pi}{2}} (1+m\cos\tau)\,\mathrm{d}\tau \right) \tag{7.39}$$

In a general case, for any value of Λ, one gets:

$$P'_{if} = \frac{1}{2\pi}\left(\Lambda\alpha + 2m\cos(\Lambda\alpha)\right) \tag{7.40}$$

Calculation of the third integral in (7.34) is the most complicated. Integration of $f_{smaller}$ that has to be used for PD-PWM for calculation of P'_{f_s} is graphically represented in Fig. 7.17d and Fig. 7.17e. One can see that borders of integration for the small modulation index values are constant, as it is illustrated in Fig. 7.17d. However, when the modulation index exceeds a certain value m_x some borders of integration ($\tau_{x_1} + k\pi$ and

$\tau_{x_r}+k\pi$) become dependent on the modulation index m, Fig. 7.17e. Substitution $\tau=\omega t$ will be used for the sake of simplicity in calculations. Values of τ_{x_l} and τ_{x_r} in Fig. 7.17e can be determined as the crossing points of the lines u_A^* and $u_B^*-0.5$, or, in a general case for any Λ, using the condition $0.5+(m/2)\cos(\tau)=(m/2)\cos(\tau-\Lambda\alpha)$. This leads to:

$$\sin\left(\tau_{x_{l,r}}-\frac{\Lambda\alpha}{2}\right)=\frac{1}{2m\sin\dfrac{\Lambda\alpha}{2}} \tag{7.41}$$

Value of m_x corresponds to $\omega t=\tau_x$ that is determined with $\tau_{x_l}=\tau_{x_r}$. The value of τ_x can be obtained in a straightforward manner from Fig. 7.17e since it is in the middle of the span from $\pi/2$ to $\pi/2+\Lambda\alpha$, where the reference leg voltages cross horizontal line of 0.5; thus $\tau_x=\pi/2+\Lambda\alpha/2$. Substituting $\tau_{x_{l,r}}$ with τ_x in (7.41) one gets $m_x=1/(2\sin(\Lambda\alpha/2))$. Taking this into account and by using (7.41), values of τ_{x_l} and τ_{x_r}, as a function of m, in Fig. 7.17e can be expressed as:

$$\tau_{x_{l,r}}=\frac{\Lambda\alpha}{2}+\arcsin\frac{m_x}{m}=\tau_x\mp\left|\arccos\frac{m_x}{m}\right| \tag{7.42}$$

The value of the integral $P'_{f_s,1}$ when $0\le m\le m_x$ can be calculated according to the graphical interpretation shown in Fig. 7.17d, i.e. by dividing area of $S'_{f_s,1}$ by 2π. Due to the symmetry the value of the integral can be calculated as:

$$P'_{f_s,1}=\frac{2}{2\pi}\left(\int_{\frac{\Lambda\alpha}{2}}^{\frac{\pi}{2}}m\cos\tau\,\mathrm{d}\tau+\int_{\frac{\pi}{2}}^{\frac{\pi}{2}+\Lambda\alpha}m\cos(\tau-\Lambda\alpha)\,\mathrm{d}\tau+\int_{\frac{\pi}{2}+\Lambda\alpha}^{\frac{\Lambda\alpha}{2}+\pi}(1+m\cos\tau)\,\mathrm{d}\tau\right) \tag{7.43}$$

One gets that:

$$P'_{f_s,1}=\frac{2m}{\pi}\left(1-\sin\frac{\Lambda\alpha}{2}-\cos\Lambda\alpha\right)+\frac{1}{2}-\frac{\Lambda\alpha}{2\pi} \tag{7.44}$$

where $0\le m\le m_x$.

For the higher modulation index values $m_x<m\le 1$ value of the integral $P'_{f_s,2}$ can be calculated directly by integration of the area $S'_{f_s,2}$ in Fig. 7.17e, and by dividing by 2π. However, it can be also calculated in a simpler way using previously obtained expression (7.44). One can see from Fig. 7.17e that $S'_{f_s,2}=S'_{f_s,1}-2S'_{f_s,\Delta}$ i.e. after dividing by 2π, that $P'_{f_s,2}=P'_{f_s,1}-2P'_{f_s,\Delta}$. Here, $P'_{f_s,\Delta}=1/(2\pi)\int_{\tau_q}^{\tau_{x_r}}(f_B-f_A)\mathrm{d}\tau$ and $P'_{f_s,1}$ is as in (7.44), but now calculated for $m_x<m\le 1$. Values of τ_{x_l} and τ_{x_r} are given by (7.42). Thus, only the value of $P'_{f_s,\Delta}$ has to be additionally calculated. For any value of Λ (e.g. in the five-phase case $\Lambda=1$ and $\Lambda=2$):

$$P'_{f_s,\Delta}=\frac{1}{2\pi}\int_{\tau_q}^{\tau_{x_r}}\left(m\cos(\tau-\Lambda\alpha)-(1+m\cos(\tau))\right)\mathrm{d}\tau \tag{7.45}$$

After calculation of the integral one gets:

$$P'_{f_s,\Delta}=\frac{1}{\pi}\left(\sqrt{\left(\frac{m}{m_x}\right)^2-1}-\left|\arccos\frac{m_x}{m}\right|\right) \tag{7.46}$$

Finally, to complete the set of equations, one recalls that:

$$P'_{f_s,2} = P'_{f_s,1} - 2P'_{f_s,\Delta} \tag{7.47}$$

where $P'_{f_s,1}$ is determined by (7.44), $P'_{f_s,\Delta}$ is given by (7.46), while $m_x < m \le 1$ ($m_x = 1/(2\sin(\Lambda\alpha/2))$).

For determination of $P_T(u_I u_J, \Lambda)$ in (7.34) values of P'_{ii}, P'_{if} and P'_{f_s} should be replaced by values from (7.38), (7.40) and (7.44) for $0 \le m \le m_x$, i.e. (7.47) for $m_x < m \le 1$, respectively. After all the substitutions one gets ($m_x = 1/(2\sin(\Lambda\pi/n))$):

$$P_T(u_I u_J) = \frac{1}{(l-1)^2}\left(1 + \frac{2m}{\pi}\left(1 - \sin\frac{\Lambda\pi}{n}\right) + \begin{cases} 0 & 0 \le m \le m_x \\ -\frac{2}{\pi}\left(\sqrt{\frac{m^2}{m_x^2} - 1} - \left|\arccos\frac{m_x}{m}\right|\right) & m_x < m \le 1 \end{cases}\right) \tag{7.48}$$

An analytical solution can be obtained now for phase and CMV voltage for the three-level case with PD-PWM for any number of phases. $P_T(u_{ph})$ is given by (7.29) where $P_T(u_{LEG})$ is defined by (7.19), which for the three-level case equals $A_0(l=3) = 1/4 + m/(\pi(3-1))$ (as given in (7.17)), and $P_T(u_I u_J, \Lambda)$ is given by (7.48). Finally, after all the substitutions into (7.29), $P_T(u_{ph})$ for the three-level n-phase PD-PWM case becomes:

$$P_T(u_{ph}) = \frac{1}{2n\pi}\sum_{\Lambda=1}^{\left\lfloor\frac{n}{2}\right\rfloor}\left(K_\Lambda m \sin\frac{\Lambda\pi}{n} + \begin{cases} 0 & 0 \le m \le m_x \\ K_\Lambda\left(\sqrt{\frac{m^2}{m_x^2} - 1} - \left|\arccos\frac{m_x}{m}\right|\right) & m_x < m \le 1 \end{cases}\right) \tag{7.49}$$

where $m_x = 1/(2\sin(\Lambda\pi/n))$, $K_\Lambda = 2$ for $1 \le \Lambda < n/2$, i.e. $K_\Lambda = 1$ for $\Lambda = n/2$ (this exists only for even n), and $\Lambda = 1, 2, \ldots, \lfloor n/2 \rfloor$. Note that m_x depends on the value of Λ; thus each value in the summation has to be calculated first. It should also be noted that the value of m_x for some values of n and Λ can be greater than 1, e.g. for $n = 7$ and $\Lambda = 1$, thus in that case the second term in the summation of (7.49) is zero for the whole range $0 \le m \le 1$.

Using (7.28) $P_T(u_{CMV})$ can be determined in a very similar way, if it is of interest. Also, $P_T(u_{CMV})$ can be obtained as $P_T(u_{CMV}) = P_T(u_{LEG}) - P_T(u_{ph})$, see (7.26), where used values are defined by (7.17) and (7.49), respectively.

7.6.3 THREE-LEVEL (A)POD-PWM CASE

The POD, i.e. APOD, PWM will be analysed in this sub-section. As already mentioned, by comparing the formulae for $P_{T_s}(u_I u_J)$ for the carriers in phase and in counter-phase (equations (7.33) and (7.35), respectively) one can see that the only difference is in the last term in the summation. Hence the integrals of $i_I i_J$ and of the $i_I f_J$, i.e. $i_J f_I$, P'_{ii} and P'_{if} during the fundamental period are determined again by (7.38) and (7.40). From Fig. 7.18 it is obvious that in some zones during the fundamental period carriers c_I and c_J (c_A and c_B in the example shown; phases A and B are chosen, $I = A$, $J = B$) are in phase while in some zones they are in counter-phase.

Let us recall that c_I is the carrier intersected by the reference signal u_I^*. This means that for calculation of $P_T(u_I u_J)$ for (A)POD, formulae (7.33) and (7.35) have to be combined during the fundamental period. It is very important to note that in those zones where carriers are in counter-phase and where (7.35) should be used, the condition $f_I + f_J > 1$ is satisfied only in the first half of that interval, Fig. 7.18. This means that in zones where carries are in counter-phase in the first half of the interval the second condition in (7.35) should be used,

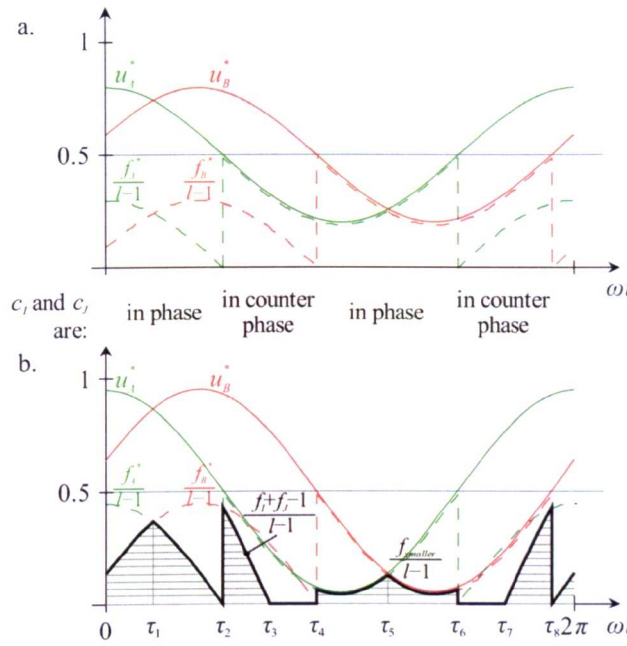


Fig. 7.18: a. Leg voltage reference signals u_A^* and u_B^* (Λ=1) with fractional (f_A, f_B, l=3) and integer (i_A, i_B) parts. b. Calculation of P_{f_s}' represents a combination of (7.33) and (7.35) when carriers are in phase and in counter phase.

while in the second half the first condition should be applied. In the example shown in Fig. 7.18 shaded area represents the last integral, and, because of symmetry, it can be calculated as:

$$P_{f_s}' = 2\frac{1}{2\pi}\left(\int_{\tau_1}^{\tau_2} f_{smaller}\,\mathrm{d}\tau + \int_{\tau_2}^{\tau_3}(f_I + f_J - 1)\mathrm{d}\tau + \int_{\tau_4}^{\tau_5} f_{smaller}\,\mathrm{d}\tau\right) \tag{7.50}$$

where $\tau_1 = 0.2\pi$, $\tau_2 = 0.5\pi$, $\tau_3 = 0.7\pi$, $\tau_4 = 0.9\pi$ and $\tau_5 = 1.2\pi$. One can see that the borders of integration $(\tau_1, \tau_2, \ldots, \tau_8)$ are not changing with the increase of the modulation index m. This simplifies integration. In general, since $P_T(u_I u_J)$ is the same for every pair I, J for the same Λ, it is enough to calculate $P_T(u_A u_J)$ $(I = A)$ and $J = B, C$ etc. until all possible values of Λ are covered for the considered number of phases n. Equation (7.50) in the general case becomes:

$$P_{f_s}' = \frac{2}{2\pi}\left(\int_{\frac{\Lambda\alpha}{2}}^{\frac{\pi}{2}} m\cos\tau\,\mathrm{d}\tau + \int_{\frac{\pi}{2}}^{\frac{\pi}{2}+\frac{\Lambda\alpha}{2}}((1+m\cos\tau)+m\cos(\tau-\Lambda\alpha)-1)\mathrm{d}\tau + \int_{\frac{\pi}{2}+\Lambda\alpha}^{\pi+\frac{\Lambda\alpha}{2}}(1+m\cos\tau)\mathrm{d}\tau\right) \tag{7.51}$$

After calculation of the integral for the general case one gets:

$$P_{f_s}' = \frac{2m}{\pi}\left(\cos\frac{\Lambda\alpha}{2} - \sin\frac{\Lambda\alpha}{2} - \cos\Lambda\alpha\right) + \frac{1}{2} - \frac{\Lambda\alpha}{2\pi} \tag{7.52}$$

As already mentioned, there is no change of the borders of integration, so (7.52) is valid for the whole modulation index range of m from 0 to 1. Similarity of (7.52) with the corresponding expression (7.44) for the PD-PWM is obvious.

The value of $P_T(u_I u_J, \Lambda)$, for any Λ, for (A)POD-PWM case can be calculated next. It is determined by a sum of terms, as in (7.34), where P_{ii}' and P_{if}' are given with (7.38) and (7.40), respectively, and P_{f_s}' is now defined by (7.52). After substitutions one gets:

$$P_T(u_l u_J) = \frac{1}{(l-1)^2}\left(1+\frac{2m}{\pi}\left(\cos\frac{\Lambda\pi}{n}-\sin\frac{\Lambda\pi}{n}\right)\right) \tag{7.53}$$

An analytical solution can be now obtained for phase and CMV voltage for the three-level case with (A)POD carrier disposition, for an n-phase system. Again, $P_T(u_{ph})$ is given with (7.29) where $P_T(u_{LEG})$ is defined by (7.19) (which is for the three-level case equal to $A_0(l=3)=1/4+m/(\pi(3-1))$, in accordance with (7.17)), and $P_T(u_l u_J,\Lambda)$ is given by (7.53). After these substitutions into (7.29), $P_T(u_{ph})$ for the three-level n-phase case with carriers in (A)POD becomes:

$$P_T(u_{ph}) = \frac{m}{2n\pi}\left(n-1-\sum_{\Lambda=1}^{\lfloor n/2\rfloor}K_\Lambda\left(\cos\frac{\Lambda\pi}{n}-\sin\frac{\Lambda\pi}{n}\right)\right) \tag{7.54}$$

where $K_\Lambda = 2$ for $1 \le \Lambda < n/2$, i.e. $K_\Lambda = 1$ for $\Lambda = n/2$ (which exists only for even n), and $\Lambda = 1,2,\ \ldots,\ \lfloor n/2 \rfloor$. Note that the power of the produced phase voltage is linearly proportional to the value of the modulation index m, with the coefficient of proportionality being different for the different numbers of phases n. Linear dependence was also present in the two-level case (7.37), while in the three-level case with PD-PWM the dependence was more complex.

If of interest, substitution of (7.17) and (7.54) into (7.26) yields $P_T(u_{CMV})$.

7.6.4 GRAPHICAL REPRESENTATION OF PHASE VOLTAGE POWER AND THD

Phase voltage power, according to the analytical expressions (7.37), (7.49) and (7.54) for the two- and three-level case with PD and (A)POD carrier dispositions, respectively, and for phase numbers $n = 3,5,6$ and 7 is shown graphically in Fig. 7.19. Power of the reference phase voltages, given with (7.23), can be easily calculated using (7.3) and is also shown in Fig. 7.19 (gray dashed line, $P_T(u^*_{ph}) = m^2/8$).

Fig. 7.19 clarifies the previously given statement, that the phase voltage produced by the PD-PWM has a smaller average power (smaller higher order harmonics) than the voltage produced by the (A)POD-PWM for the same number of phases. Of course, phase voltage produced by the (A)POD-PWM has a smaller average power than the one produced by the two-level PWM inverter. An interesting fact to be noted is that the phase voltage

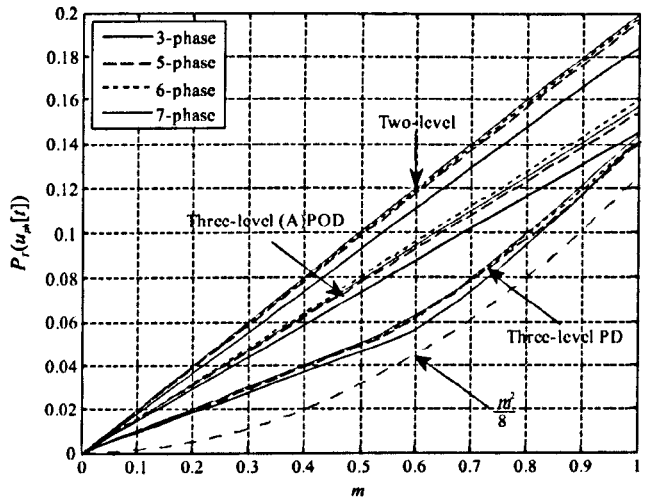


Fig. 7.19: Analytical curves plotted using (7.37), (7.49) and (7.54): the average power during the fundamental period of the phase voltage generated by two- and three-level PWM multiphase inverters with PD and (A)POD carriers, $P_T(u_{ph})$.

produced by a three-phase inverter has smaller power than those produced by inverters with higher numbers of phases. For the two-level case and for three-level case with PD-PWM this can be generalised into a statement that power of the phase voltage increases with the phase number n; however, for (A)POD this is not the case.

Note that the values for the three-level PD-PWM in Fig. 7.19 are twice smaller than for the two-level case for the given number of phases, for small modulation index values. This is also obvious from equations (7.37) and (7.49). The maximum value of the modulation index m up to which this applies is determined by the smallest value of m_x for a particular n, i.e. by $\min(1/(2\sin(\Lambda\pi/n)))$. Thus for the three-phase case this is true up to the modulation index of 0.5774, for the five-phase case up to 0.5257, for the six-phase case up to 0.5, and for the seven-phase case up to 0.5129.

Operation of the three-level inverter with PD carrier disposition for small modulation index values is similar to the operation of the two-level VSI with halved dc-bus voltage, since the same space vectors are used. The power curves in Fig. 7.19 are for the normalised voltages, so that they have to be multiplied with V_{dc}^2 to calculate the power in physical units. This justifies used normalisation, because power curves for the normalised voltages are directly comparable without any additional scaling. Thus, at the first sight, it appears that the power at small modulation indices for the three-level case should be four times smaller than for the equivalent two-level inverter with halved dc-bus voltage, because normalised value for the two-level case from Fig. 7.19 has to be multiplied with $(V_{dc}/2)^2$. However, if the dc-bus voltage is halved that means that corresponding modulation index for the two-level inverter is doubled. Hence, if a small modulation index, say $m=0.4$, is taken as an example, the power of the three-level PD-PWM produced phase voltage is equal to the value from Fig. 7.19 multiplied by V_{dc}^2. This value is actually equal to the value obtained with the two-level inverter with halved dc-bus voltage, which is the value in Fig. 7.19 for $m=0.8$ multiplied by $(V_{dc}/2)^2$. For the same reference signal the dc-bus voltage is halved so the corresponding modulation index is doubled and amounts to $m=0.8$. Because of the linear dependence on the modulation index value for the two-level case, this finally confirms that normalised values for the phase voltage power produced by the three-level inverter with PD carriers, in zone of small modulation index values, are actually two (rather than four) times smaller than the normalised values for the two-level case.

From the point of view of the space vectors and sub-sectors, used space vectors for sub-sectors of the three-level case are identical for the small modulation index values as for the two-level case with halved dc-bus value. Maximum modulation index in the linear modulation region for an n-phase system, for odd numbers of phases, is given with $m_{max}=1/\cos(\pi/(2n))$ [Levi et al. (2008)], and it is obtained with min-max zero-sequence injection. For even numbers of phases m_{max}=1 and linear region cannot be extended. Particular values of the modulation index m_x, up to which the power of the phase voltage obtained with the two-level inverter is twice more than the power obtained with the three-level inverter (0.5774, 0.5257, etc.), are equal to $m_{max}/2$ for any particular number of phases. This result can look unexpected because the reference signals analysed here are pure sinusoidal signals without any injection. However, the min-max injection is not reflected in the phase voltages and sub-sector division for phase voltage space vectors is the same for pure sinusoidal reference signals and for sinusoidal signals with added min-max injection; the only difference is in the maximum achievable modulation index in the linear PWM region, as explained in 5.3.1.

By using analytical expressions (7.37), (7.49) and (7.54) for the phase voltage average power obtained with two- and three-level multiphase PWM inverter with PD and (A)POD carriers, and by using (7.8), THD

values of the phase voltages can be obtained. Note that, according to (7.4), RMS values of the phase voltages can be calculated as $U_{ph,rms} = \sqrt{P_T(u_{ph})}$. As in section 7.5, where leg voltage THD is defined with (7.22), total harmonic distortion is defined with reference to the fundamental (first harmonic) of the output. The fundamental value of the generated phase voltages, since dead time is not taken into consideration and due to the assumption of high switching frequency, is equal to the reference magnitude, i.e. its RMS value is equal in per unit to $U_{ph,rms,1} = m/(2\sqrt{2})$. The dc component of the output voltage is $U_{ph,dc}=0$. The power of the reference phase voltage is $P_T(u^*_{ph}) = m^2/8$, as already explained. Actually, the first harmonic and the dc components (if any) form the power of the reference signal, i.e. $P_T(u^*_{ph}) = U^2_{ph,rms,1} + U^2_{ph,dc}$. Substituting these expressions into (7.8), an equation similar to the one for THD of the leg voltage (7.22), can be written as:

$$\mathrm{THD}_T(u_{ph}) = \frac{\sqrt{P_T(u_{ph}) - P_T(u^*_{ph})}}{U_{ph,rms,1}} = \sqrt{\frac{8P_T(u_{ph})}{m^2} - 1} \tag{7.55}$$

where $P_T(u_{ph})$ is given by (7.37), (7.49) and (7.54) for the considered cases of the two-level and three-level PWM with PD and (A)POD carriers, respectively, and m is the modulation index value $0 \le m \le 1$.

Additional power that is contained in the created phase voltages, in excess of the power of the ideal sinusoidal signal, is $P_T(u_{ph}) - P_T(u^*_{ph})$. It is shown in Fig. 7.20. This is in essence difference between the values in Fig. 7.19 and $m^2/8$.

Curves that represent THD of the phase voltages, for the two-level and three-level PWM with PD and with (A)POD carriers, are generated according to the analytical expression (7.55) for various phase numbers and are shown in Fig. 7.21.

A comparison of Fig. 7.20 with Fig. 7.12 for leg voltages (curves for the two and three-level case) shows that the difference between the "wasted" power in the leg and in the phase voltage for the three-level case for (A)POD is very small. The comparison can be also done directly by comparing Fig. 7.19 and Fig. 7.11. In this case one should be aware that the power of the reference leg voltages in Fig. 7.11 contains an additional offset of 0.25, since leg reference voltages contain dc-value of 0.5 (see (7.13)), that keeps them centred between dc-bus rails. According to (7.26) this means that for (A)POD in the three-level case very little energy goes into non-dc harmonics in the CMV. If this parameter is of interest, than the (A)POD represents the best choice. Further, one

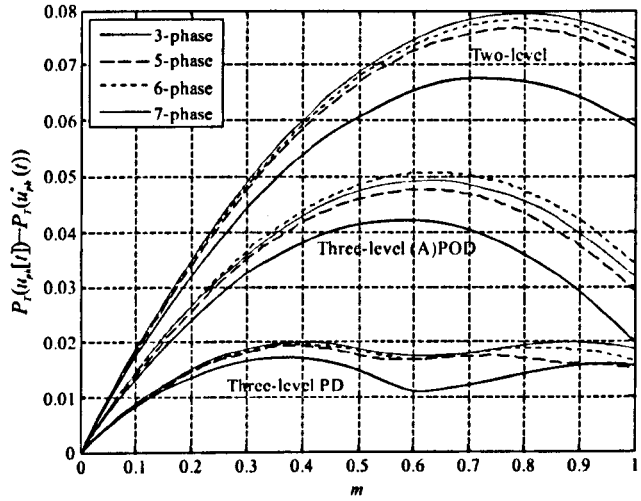


Fig. 7.20: Power in excess of the power of the ideal sinusoidal signal, contained in the generated phase voltages with two- and three-level multiphase inverters.

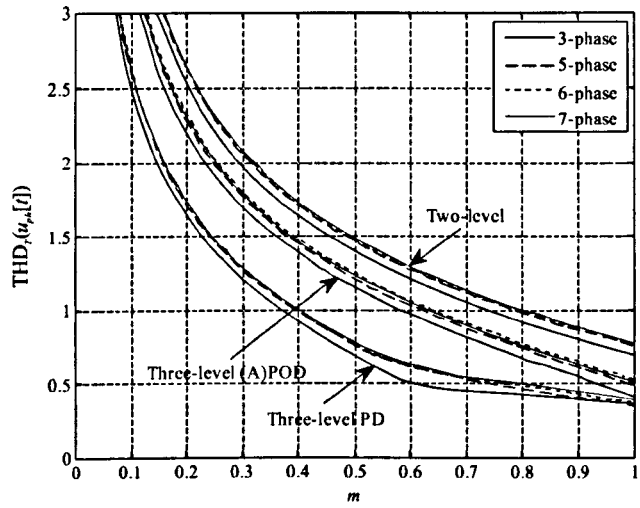


Fig. 7.21: THD, as given by the analytical expressions (7.55), for the generated output phase voltage of the two- and three-level PWM multiphase inverters, $THD_T(u_{ph})$.

can see that (7.54) for even numbers of phases n becomes equal to $P_T(u_{ph}) = m/(2\pi)$. Comparing this result with the power of the leg voltage (7.17), for the three-level case, one can see that the only difference is in the constant term 1/4. This means that for an even n and for the three-level inverters with carriers in (A)POD the CMV does not contain any ripple and is a pure dc-value or zero, depending on the point to which it is referenced. Because of the mirror-symmetry around the time axis, this conclusion can be generalised to any even number of phases with an odd number of levels, and to both POD and APOD carriers.

Calculation of the phase voltage and CMV power and of the phase voltage THD for any other number of levels can be executed in the same manner. However, due to complex analytical calculations and due to the simplicity of finding the problem solution numerically, full solution for only the most common cases in practice, two-level and three-level PD and (A)POD PWM, was given here. Numerical calculation of the THD does not necessarily mean calculation by finding the spectrum first; THD can be also calculated numerically in time domain, as explained at the end of section 7.3. Some results for the phase voltage THD, for the three-phase load supplied from the five, seven and nine-level inverter with different carrier-based strategies, are given in [Calais et al. (2001)], where the region of overmodulation is also covered. The method of THD calculation in [Calais et al. (2001)] was obviously numerical, by means of the spectrum determination; however the number of harmonics taken into consideration is not given.

7.6.5 A DIFFERENT VIEW ON CALCULATION OF THE LEG VOLTAGE POWER

Derivation of the power of the PWM produced leg voltage by an l-level inverter was given in section 7.5. The final equation for the $P_T(u_{LEG})$ is given by (7.19). This equation was derived by integration of the power of the signal from one switching period, $P_{T_s}(u_{LEG})$, governed by (7.11). The same principle was used for calculation of the power of the product of two PWM signals. Average power of the product of two signals during one switching period, $P_{T_s}(u_l u_J)$, for carriers in PD, is given by (7.33). As already mentioned, for Λ=0, $P_{T_s}(u_l u_J) = P_{T_s}(u_l u_l)$ represents $P_{T_s}(u_{LEG})$. It is worth recalling here the definitions used, namely: $P_{T_s}(u_l u_l) = 1/T_s \int_0^{T_s} u_l u_l \mathrm{d}t$, while $P_{T_s}(u_{LEG}) = 1/T_s \int_0^{T_s} u_{LEG}^2 \mathrm{d}t$ (rather than $1/T_s \int_0^{T_s} u_{LEG} \mathrm{d}t$). This means that equations (7.11) and (7.33) for Λ=0 are the same.

For Λ=0, (7.33) becomes:

$$P_{T_s}(u_{LEG}) = \frac{1}{(l-1)^2}(i^2 + 2if + f) \tag{7.56}$$

where index I is omitted; note that $f_{smaller} = \min(f_1, f_1)$ equals f_1, i.e. f. Also note that integer index i in (7.11) corresponds to definition of i in (7.30). If in (7.11) D is replaced with $(i+f)/(l-1)$, the identity with (7.33), i.e. (7.56), becomes obvious. This expression can be alternatively written as:

$$P_{T_s}(u_{LEG}) = \frac{1}{(l-1)^2}((i+f)^2 + f - f^2) = D^2 + \frac{f(1-f)}{(l-1)^2} = P_{T_s}(u^*_{LEG}) + \frac{f(1-f)}{(l-1)^2} \tag{7.57}$$

Equation (7.57) is identical to (7.11) but it is clearer in the meaning, because it directly shows that the power of the produced leg voltage during one switching period is equal to the sum of the power of the reference leg voltage plus part that comes from switching between two adjacent levels. Using this formula for THD, equation (7.12) becomes simpler:

$$\mathrm{THD}_{T_s}(u_{LEG}[t]) = \frac{\sqrt{f(1-f)}}{(l-1)D} \tag{7.58}$$

where $D = u^*_{LEG}(kT_s)$. By integration of (7.57) across the whole fundamental period, as in section 7.5, the general equation (7.19) can be derived in the same form.

7.7 COMPARISON OF THE THEORETICAL CURVES WITH SIMULATION AND EXPERIMENTAL RESULTS

To validate the theoretically obtained analytical results, simulations and experiments have been done. Simulation software PLECS block-set has been used. Scope in this software has a built-in function for RMS and THD calculation. The built-in functions use exact numerical approach as the one described in section 7.3, but are also adapted to work with a variable simulation step time [Allmeling and Hammer (2012)]. According to (7.4) average power of the signals is calculated as a squared value of the RMS value from the PLECS scope. This way of calculation is very precise and that is the reason why this software has been used for proper simulation verification of analytical results.

Theoretical curves for the leg voltage THD, shown in Fig. 7.13 for the two- to five-level cases for pure sinusoidal references, are compared in Fig. 7.22 with the values obtained by simulation using PLECS scope.

Simulations are done for the constant V/f ratio ($m/f = 1/50$), for V_{dc}=1 V (for easier comparison of power curves, when needed), and for the switching frequency of $f_s = 2$ kHz. Excellent agreement between simulation and analytical results is obvious. This means that the used switching frequency, i.e. ratio f_s/f, is high enough for all the modulation indices. Also, one can see that the different carrier-based dispositions (PD, POD and APOD) do produce the same THD in a leg voltage, as long as the single-level transitions are used, output voltage steps are equal, carriers are centred, and f_s is high enough. This conclusion has been given after theoretical considerations in 7.5 after (7.16).

Theoretical (analytical) curves for the leg voltage THD of Fig. 7.13 are compared next with the experimentally obtained THD values in Fig. 7.23 for the two-level and three-level cases.

Experimental THD values for leg voltages in Fig. 7.23 apply to the experimental rig with the five-phase induction machine, but voltage THD is of course independent of the load. As in simulations, V/f ratio was kept constant and equal to $m/f = 1/50$. Custom-made two-level and three-level inverter of the neutral-point clamped

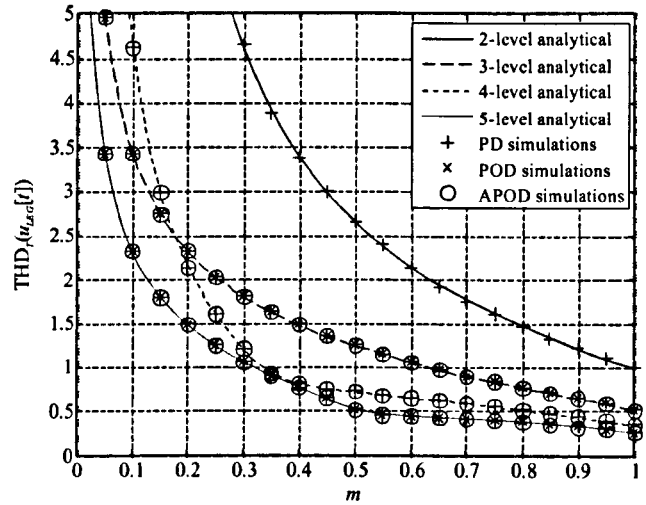


Fig. 7.22: Comparison of the analytical curves for leg voltage THD of Fig. 7.13 (solid and dashed lines) with simulation results from PLECS scope (values shown with markers).

(NPC) type were supplied from Sorensen SGI 600/25 dc source (as also used for the other experimental results in this thesis). Dc bus voltage was set to 600V. To obtain the THD from the experimental results, spectrum has been calculated first. The length of the spectrum varies because the number of samples from the oscilloscope inside one switching period varies (V/f has been used, and time scale was adjusted for each measurement). The THDs when full spectrum has been used and when only components from the first ten side-bands (up to 21kHz) are taken into consideration (according to (4.9)), were calculated and are shown in Fig. 7.23. Recall that this way of calculation was used in all the previous chapters of this thesis. Because of the lack of availability of the hardware for more than three-level operation, only results for the two-level and three-level cases are shown. One can see that, because of the dead time, which is 6μs in the implementation for both inverters, the THD from the experiments is very slightly higher (worse) than the one predicted by the theoretical curves. This is visible in Fig. 7.23 only for low modulation indices, where the dead-time effect is more pronounced. The influence of the finite switching frequency is obviously not very important, as can be seen in Fig. 7.22 where the same switching

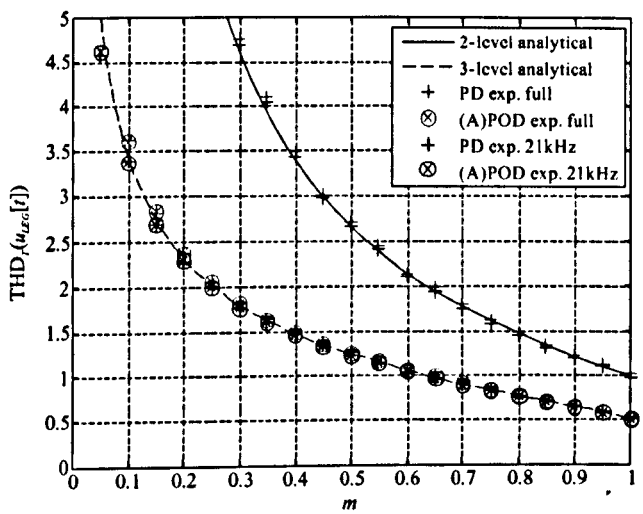


Fig. 7.23: Comparison of the analytical curves for the leg voltage THD of Fig. 7.13 (continuous lines) with experimental results using full and up to 21kHz spectrum for the THD calculation (discrete values labelled with corresponding markers) for the two-level and three-level operation.

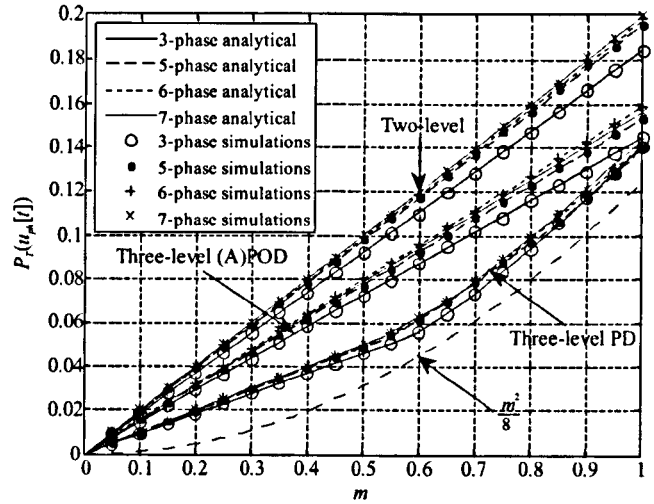


Fig. 7.24: Comparison of the analytical curves for the average power of the phase voltage generated by two- and three-level PWM multiphase inverter (Fig. 7.19; continuous lines) with simulation results from PLECS scope RMS^2 (discrete values, identified with markers).

frequency of 2kHz was used, but where dead time was neglected. Also, if the finite number of samples is taken into consideration (the value used here is 21kHz and is much higher than many that are usually in use in practice), the calculated THD can be easily lower than the correct analytical value, see Fig. 7.23. This problem is well known and also has been analysed in [Farokhnia et al. (2011a), Farokhnia et al. (2011b)].

Theoretical analytical curves for power of the generated output phase voltage of Fig. 7.19 are compared with simulation values from PLECS scope (RMS^2) in Fig. 7.24. A corresponding comparison of the analytical THD traces with simulation results, which are the values read from the PLECS scope, is shown in Fig. 7.25.

By inspecting Fig. 7.24 and Fig. 7.25 one can see an excellent agreement between the results obtained using analytical expressions and simulation results for both power and THD of the obtained phase voltages, similar to the agreement achieved for the leg voltages.

The experiments have been done using three-, five-, and six-phase symmetrical induction machines and for symmetrical seven-phase $R-L$ load. Dc voltage, provided from Sorensen SGI 600/25 dc source, was 600V

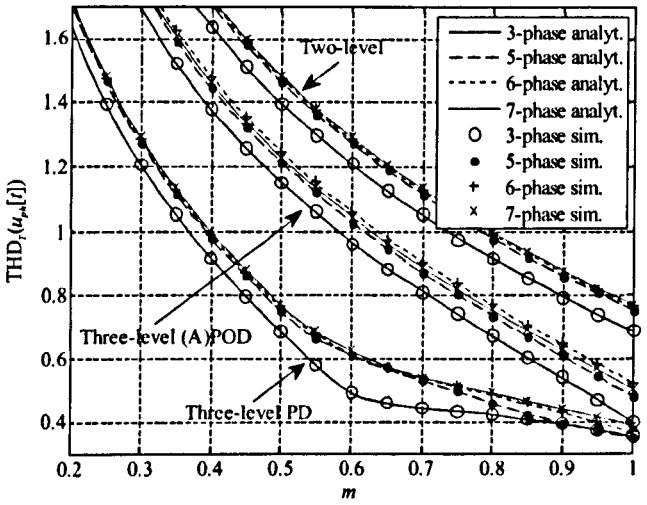


Fig. 7.25: Comparison of the analytical curves for phase voltage THD (Fig. 7.21; continuous lines) with simulation results from PLECS scope (discrete values, identified with markers).

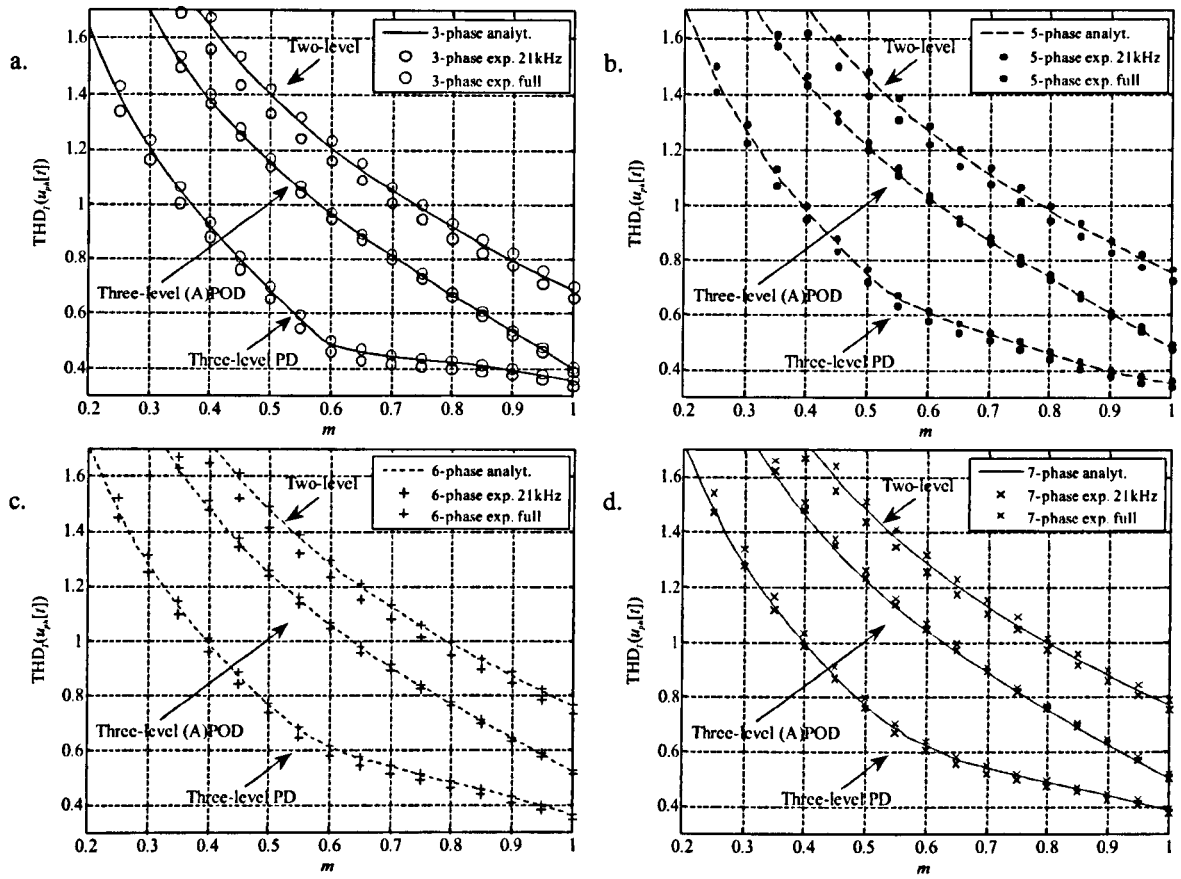


Fig. 7.26: Comparison of the analytical curves (continuous lines) for the phase voltage THD (Fig. 7.21) with experimental results using the full and up to 21kHz spectrum for THD calculation (discrete values labelled with corresponding markers), for a. three-, b. five-, c. six- and d. seven-phase configuration.

in all the cases, except for the six-phase machine where it had to be lowered to 250V due to the limitation imposed by the voltage rating of the machine. The same procedure and the same settings as before apply here as well. As for leg voltages, THD was calculated using Fourier transformation and the harmonic spectrum was limited at 21kHz, see (4.9). Comparison of theoretical analytical curves and experimental results for the THD is given in Fig. 7.26.

The effect of truncating the spectrum at 21kHz is evident in Fig. 7.26, since all the experimental THD values are slightly lower than the theoretically predicted values. It should be noted in this context that the THD in experiments is actually slightly increased because of the dead-time induced harmonics; hence the values calculated using full spectrum appear above analytical curves. The same was the case for the obtained leg voltages, Fig. 7.23.

7.8 CONCLUSION

Analytical expressions for the average power and THD for the PWM produced leg and phase voltage are derived in this chapter. Considered reference voltage is purely sinusoidal. Derived analytical formulae for the leg voltage average power and THD are for any number of levels. Phase voltage is further analysed for star-connected symmetrical load. Due to the difficulties encountered in the analytical derivation, and simultaneous simplicity in obtaining the results numerically, only two- and three-level n-phase cases were analysed. However,

the principle used is general and it can be applied to any number of levels and phases. For the three-level case PD-PWM and POD (i.e. APOD) PWM are covered. The superiority of the PD-PWM is confirmed once again by the time domain power analysis here. Analytical curves are compared with simulation and experimental results, and an excellent agreement is demonstrated.

Chapter 8

CONCLUSION

8.1 SUMMARY AND CONCLUSIONS

In this thesis, an analysis of PWM techniques that can be used for control of multilevel VSI supplied multiphase machines is given. Analysed machines are with the sinusoidal distribution of windings, so the aim of the PWM algorithms is always to produce sinusoidal output. Five-phase and seven-phase three-level structures are covered in detail. Also, an effort has been made to present all the algorithms in a general form, so that the introduced algorithms can be applied to an arbitrary number of phases and an arbitrary number of levels. Research is concentrated more on the space vector algorithms since carrier-based ones are universal and easy to extend. Carrier-based algorithms are used in this research as a reference point, and all the space vector techniques are compared with them. The comparison in the research is based on the time domain waveforms, produced by particular strategies, and on their spectra. Commonly used in practice global figure of merit, THD, has been also used for comparison purposes. Analytical formulae for leg and phase voltage THD for different types of modulation strategies are developed, so that the additional consequences of the PWM schemes on the inverter and machine operation under the different conditions can be investigated. In this research proper functioning of developed modulation strategies has been confirmed by experimental results using a five-phase induction machine in open-loop operation and using a passive R–L load for the seven-phase case, in conjunction with a custom-built NPC three-level VSIs.

The thesis starts with the literature survey of modulation strategies relevant for the research topic. It gives a review of carrier-based and space vector PWM techniques. As the starting point, a survey of the carrier-based techniques for multilevel inverters is given. Modulation strategies for other drive topologies that are related to the analysed multilevel single-sided supply of multiphase machines using voltage source inverters are covered. At first, the main works on space vector techniques for three-phase multilevel inverters are addressed. Next, a reference review of space vector techniques for multiphase two-level inverters is given. Some of the first modulation techniques for open-end winding configurations, as an alternative for multilevel operation, are surveyed. The survey of the multilevel multiphase voltage source inverters shows that only a few papers can be considered as 'real' space vector algorithms, according to the space vectors definition used in this thesis. Among them only one method is considered as a proper space vector one, since it considers all the planes in the vector space decomposition approach. A survey of some non-VSD based multilevel multiphase algorithms was included as well. The existence of only one proper space vector algorithm, based on the VSD approach, has confirmed that there is enough space for investigation in this field. Some of the aims are therefore set as the extension to higher number of phases and possible generalisation. Also, a comparison of the space vector algorithms with the carrier-based algorithms was set as one of the main objectives, because of much easier implementation of the carrier-based techniques.

Before explanation of the specific algorithms, in Chapter 3, a general structure of a single-sided inverter fed induction machine is discussed and some general equations are given. The process of digitalisation with extra requirement for averaging in each switching period is explained. A lot of attention is devoted to the transformations, to the explanation of the space vectors, and to the vector space decomposition approach analysis. The definition of space vectors does not appear to be uniform and, through the literature survey, one can note that different authors assume different definitions of it. In this thesis the VSD has been assumed as the only space vectors approach because it strictly defines the space, it defines vectors in that space, and it decomposes and analyses 2-D projections of the vectors. Also, the VSD approach has been used in the majority of existing papers, and, most importantly, it has been used for the two-level multiphase algorithms where more than one 2-D plane is present and has to be considered. A simple method for plotting of the space vector projections is shown as well, as a supporting tool for an easier analysis of the space vectors.

Space vector algorithms have been analysed in Chapter 4. Space vector techniques consider signals in decomposed space after transformation. The number of switching states and space vectors rapidly increases with higher numbers of phases and levels of the inverter. All spaces have to be analysed simultaneously. This makes the task very difficult for realisation for any particular case and especially for generalisation. The first analysed technique in Chapter 4, for the five-phase three-level case, includes an in-depth analysis of the existing algorithm that gives the complete VSD algorithm solution for this particular case. A lot of steps of this algorithm are explained in a different manner, to facilitate the development of the algorithm for the seven-phase three-level case and to make it easier for the generalisation. One modification of the original algorithm, which aims at reduction of the magnitude of the main (the fifth) harmonic in the CMV and that increases symmetry of the sector sub-division, is developed. The algorithm for the seven-phase three-level case is developed next for the first time and this is undoubtedly one of the main contributions of this thesis. The same modification of the original algorithm, as in five-phase case, is also applied to the seven-phase algorithm. Proper functioning of the all four space vector algorithms has been confirmed through the simulations and experiments. A general form of the algorithm is also given. The reduction of the number of switching states from the total of 243 to 113 in the five-phase, i.e. from 2187 to an acceptable 297 in the seven-phase case, is obtained by the application of the order-per-sector law from the time domain. Correlation between leg state (level) transitions in the time domain and in the α-β plane is explained, and a method for determination of the switching sequences, by finding the closed n-angle patterns, is presented. Partitioning of the sectors into sub-sectors, by limiting the time of application of each vector to the 0 to T_s interval and requiring cancellation (on average) of voltages in the x-y planes, is done. Final sequences are chosen to minimise losses and also to contain the maximum number of 'ones', for the better dc-bus capacitor voltage balancing in the three-level case. Sub-sector determination is realised by a simple comparison of the reference voltage projections with constant values.

In Chapter 5 carrier-based techniques are introduced in a manner convenient for comparison with the space vector techniques. Chosen carrier disposition is the level-shifted one, of PD type (all carriers are in phase), since it is the only type that produces increasing transitions in the first half of the switching period and decreasing transitions in the second half, as it is assumed in the SVPWM algorithms. Pure sinusoidal references are analysed at first. Reduction of the PD-PWM to the single carrier band has been used for simpler implementation and for explanation of the change of the switching sequences that appear in time domain. The change of the switching sequence is explained in detail and is reduced to the simple rule that it appears when two

reference leg voltage fractional parts change mutual order. Conditions when the starting switching state of the new sequence changes are explained. Influence of the modulation index on change of the mutual order of fractional parts, i.e. on the change of the applied sequences, is analysed. Plots that show this dependence in the α-β plane are given. The same analysis is repeated for the sinusoidal references with min-max injection as an option for extension of the linear modulation index range. Double min-max injection, that additionally centres fractional parts of the reference leg voltages inside the common carrier band is also analysed. The second centring of the signals provides equal times of application for the redundant switching states, which is a common assumption in the space vector algorithms.

In Chapter 6 comparative analysis of the presented space vector and carrier-based modulation strategies is given. The first part of the analysis is theoretical, and is based on a comparison of the switching sequences and on sub-sector division that defines regions of applicability of these sequences. Five-phase three-level case is used as the example. It is highlighted that sub-division of the α-β plane into sub-sectors of the modified space vector algorithm and of the carrier-based algorithm with min-max, i.e. double min-max, injection are identical. Also, for a few sub-sectors it is proven that the same switching sequences are used. Finally, double min-max injection will equally distribute times of application of the redundant switching states, so the equivalence of this algorithm with the modified space vector algorithm is theoretically demonstrated. The second part of the analysis of the presented modulation strategies for the five- and seven-phase three-level case is given through the comparison of experimental results. Three carrier-based (with pure sinusoidal references, with min-max injection and with double min-max injection) and two space-vector (original and modified) PWM methods are encompassed by the experimental comparison, for both topologies. It is shown that, while all methods have the same maximum modulation index (apart from CBPWM0) in the linear region and yield essentially the same phase voltage and current output, differences exist in the spectra of the phase voltage, common mode voltage and current. Two of the methods, carrier-based with double min-max injection (CBPWM2), and modified space vector algorithm (SVPWM2) are characterised with identical voltage spectra for all modulation index values, confirming the theoretical analysis. Phase voltage THD is found to be the same for all methods, although the individual harmonics differ in magnitudes. With regard to the harmonic distortion of the CMV, the best performance in the low to medium modulation index range is obtained with carrier-based technique with the single min-max injection (CBPWM1). The best current THD is obtained with strategies that equally share the time of application of the redundant switching states, CBPWM2 i.e. SVPWM2. These conclusions are valid for both five- and seven-phase topologies. With respect to the complexity and memory consumption it is shown that the carrier-based algorithms are much more efficient and are thus favourable for practical implementation.

Analytical considerations regarding leg and phase voltage power and THD are given in Chapter 7. Pure sinusoidal references are analysed. Parasitic effects, such as dead-time, were not considered. The analysis is based on the integration of the values from a single switching period throughout the fundamental period. Thus the analysis is given in the time domain. The analysis is valid as long as the ratio of f_s/f is high enough. Analytical equations for leg voltage power and THD, obtained by an l-level inverter, are derived. It is shown theoretically and later confirmed experimentally that all the analysed carrier-based modulation strategies (PD, POD, APOD) will produce the same leg voltage power, i.e. THD. This conclusion can be generalised to all modulation strategies that have one up and one down leg transition during the switching period, and that apply only adjacent levels. It is also important that output leg voltage step is equal and constant. Analytical equations

for the power and THD of the phase voltage, generated by two- and three-level inverters with an arbitrary number of phases are also derived. These equations are derived for the first time in this thesis and will be a subject of further publications. In the three-level case, PD- and POD-, i.e. APOD-, PWM are analysed. It is shown that the phase voltage obtained with the three-level PD-PWM contains less power than the phase voltage yielded by (A)POD. This conclusion is in agreement with the existing conclusion, obtained by the spectral analysis of the three-phase case. Of course, this power is lower than the power of the phase voltage generated by the two-level inverter. If the aim is reduction of the power that goes into the CMV, with the possibility of elimination of the CMV, then (A)POD is to be favoured. Minimum power means minimum additional power in addition to the power of the ideal sinusoidal output, leading to the minimum THD. Thus PD-PWM is proven to have the lowest phase voltage THD among the analysed cases. Used principle for analytical calculation is straightforward for numerical implementation. Analytical curves are checked by simulations and by numerical methods for the power and THD calculation. An excellent agreement is demonstrated. THDs for experimental results of the leg voltage and the phase voltage, generated by the two- and three-level inverters with three-, five-, six- and seven-phase symmetrical load (induction machines were used, except for the seven-phase case where an *R-L* load has been utilised), have been calculated and compared with the theoretical curves. It is shown that, by limiting the number of harmonics to the first ten side-bands (the method that has been used in this thesis), the obtained THD is slightly below theoretical curves. When the THD is calculated for the full spectrum the values are slightly above the theoretical curves, which proves an increase of the THD when dead time is present.

8.2 FUTURE WORK

The work presented in this thesis brings some considerable new knowledge in the area of space vector control of multilevel multiphase VSIs. A number of very important facts for the comparison of the space vector and carrier-based modulation strategies are presented. However, the investigation here was narrowed to some specific cases, e.g. only machines with sinusoidally distributed windings were analysed, and only linear modulation index range was investigated. The analysed space vector modulation strategies are based on the VSD approach and have been compared with the carrier-based approaches. However, there are more modulation strategies that can be applied to a multilevel multiphase VSI. Some of them are mentioned in the initial review, such as matrix approach or single-phase modulators, and they are characterised here as a different description of the carrier-based approaches. However, it would be wise to confirm this identity by experimental results. All of this gives a lot of scope for the new research that can be done. Some of the topics for the future work could be:

- Extension of the presented space-vector modulation techniques to overmodulation range.
- Realisation of the original space vector algorithm by using the carrier-based approach, i.e. construction of the specific injection.
- Application of the presented space vector algorithms for multi-frequency output.
- Investigation if optimality according to the flux ripple, which characterises the CBPWM2 in the three-phase case remains valid in the multiphase case.
- Experimental comparison of the presented modulation strategies with the matrix approach based ones and the single-phase modulators.
- Detailed investigation of the influence of the used modulation strategies on the capacitor voltage balancing.

- Development of the space vector modulation technique for the nine-phase three-level case.
- Additional comparison with open-end winding structures.
- Derivation of the analytical expressions for leg and phase voltage power and THD when the references are with min-max injection.

Chapter 9

REFERENCES

Abu-Rub, H., Holtz, J., Rodriguez, J., Baoming, G., (2010), Medium-voltage multilevel converters - State of the art, challenges, and requirements in industrial applications, *IEEE Trans. on Industrial Electronics*, vol. 57, no. 8, pp. 2581-2596.

Agelidis, V. G., Calais, M., (1998), Application specific harmonic performance evaluation of multicarrier PWM techniques, *Proc. IEEE Power Electronics Specialists Conf. PESC*, Fukuoka, Japan, pp. 172-178.

Akagi, H., (2011), New trends in medium-voltage power converters and motor drives, *Proc. IEEE Int. Symposium on Industrial Electronics ISIE*, Gdansk, Poland, pp. 5-14.

Allmeling, J., Hammer, W., (2012, 27. Aug.), *PLECS - User Manual*, Version 3.3, Retrieved 20. Feb., 2013, from http://www.plexim.com/files/plecsmanual.pdf.

Bodo, N., Dordevic, O., Jones, M., Levi, E., (2012), A comparison of three-level single-sided and dual-inverter supply for a five-phase drive, *Proc. Int. Power Electronics and Motion Control Conf. EPE-PEMC*, Novi Sad, Serbia, pp. LS1c.2-1-LS1c.2-6.

Bodo, N., (2013), PWM strategies for open-end winding multiphase drives, *PhD Thesis*, Liverpool John Moores University, Liverpool, U.K.

Bose, B. K., (1982), Adjustable speed AC drives - A technology status review, *Proceedings of the IEEE*, vol. 70, no. 2, pp. 116-135.

Busquets-Monge, S., Ruderman, A., (2010), Carrier-based PWM strategies for the comprehensive capacitor voltage balance of multilevel multileg diode-clamped converters, *Proc. IEEE Int. Symposium on Industrial Electronics ISIE*, Bari, Italy, pp. 688-693.

Calais, M., Borle, L. J., Agelidis, V. G., (2001), Analysis of multicarrier PWM methods for a single-phase five level inverter, *Proc. IEEE Power Electronics Specialists Conf. PESC*, Vancouver, BC, Canada, pp. 1351-1356.

Carrara, G., Gardella, S., Marchesoni, M., Salutari, R., Sciutto, G., (1992), A new multilevel PWM method: a theoretical analysis, *IEEE Trans. on Power Electronics*, vol. 7, no. 3, pp. 497-505.

Castro, L. G., Corrêa, M. B., Jacobina, C. B., Boroyevich, D., (2010), A fast space-vector algorithm for multilevel converters without coordinates transformation, *Proc. IEEE Energy Conversion Congress & Expo ECCE*, Atlanta, GA, pp. 2543-2547.

Celanovic, N., Boroyevich, D., (2001), A fast space-vector modulation algorithm for multilevel three-phase converters, *IEEE Trans. on Industry Applications*, vol. 37, no. 2, pp. 637-641.

Corzine, K. A., Sudhoff, S. D., Whitcomb, C. A., (1999), Performance characteristics of a cascaded two-level converter, *IEEE Trans. on Energy Conversion*, vol. 14, no. 3, pp. 433-439.

de Silva, P. S. N., Fletcher, J. E., Williams, B. W., (2004), Development of space vector modulation strategies for five phase voltage source inverters, *Proc. IEE Power Electronics, Machines and Drives Conf. PEMD*, Edinburgh, U.K., pp. 650-655.

Dordevic, O., Jones, M., Levi, E., (2011a), A comparison of PWM techniques for three-level five-phase voltage source inverters, *Proc. European Power Electronics and Applications Conf. EPE*, Birmingham, U.K., CD-ROM paper 0620.

Dordevic, O., Jones, M., Levi, E., (2011b), A space vector PWM algorithm for a three-level seven-phase voltage source inverter, *Proc. European Power Electronics and Applications Conf. EPE*, Birmingham, U.K., CD-ROM paper 0123.

Dordevic, O., Jones, M., Levi, E., (2013a), A comparison of carrier-based and space vector PWM techniques for three-level five-phase voltage source inverters, *IEEE Trans. on Industrial Informatics*, vol. 9, no. 2, pp. 609-619.

Dordevic, O., Levi, E., Jones, M., (2013b), A vector space decomposition based space vector PWM algorithm for a three-level seven-phase voltage source inverter, *IEEE Trans. on Power Electronics*, vol. 28, no. 2, pp. 637-649.

Đorđević, O., Bodo, N., Jones, M., (2010), Model of an induction machine with an arbitrary phase number in Matlab/Simulink for educational use, *Proc. Universities Power Engineering Conference UPEC*, Cardiff, U.K., CD-ROM paper 222.

Dujic, D., Iqbal, A., Levi, E., Vasic, V., (2006), Analysis of space vector pulse width modulation for a symmetrical six-phase voltage source inverter, *Proc. Int. Power Conversion and Intelligent Motion Conf. PCIM*, Nürnberg, Germany, CD-ROM paper 154_S6b-04_Dujic.

Dujic, D., Jones, M., Levi, E., (2009), Generalised space vector PWM for sinusoidal output voltage generation with multiphase voltage source inverters, *Int. Journal of Industrial Electronics and Drives*, vol. 1, no. 1, pp. 1-13.

Dujić, D., (2008), Development of pulse-width-modulation techniques for multi-phase and multi-leg voltage source inverters, *PhD Thesis*, Liverpool John Moores University, Liverpool, U.K.

Farokhnia, N., Fathi, S. H., Yousefpoor, N., Bakhshizadeh, M. K., (2011a), Minimisation of total harmonic distortion in a cascaded multilevel inverter by regulating voltages of dc sources, *IET Power Electronics*, vol. 5, no. 1, pp. 106-114.

Farokhnia, N., Vadizadeh, H., Fathi, S. H., Anvariasl, F., (2011b), Calculating the formula of line-voltage THD in multilevel inverter with unequal DC sources, *IEEE Trans. on Industrial Electronics*, vol. 58, no. 8, pp. 3359-3372.

Fortescue, C. L., (1918), Method of symmetrical co-ordinates applied to the solution of polyphase networks, *Trans. of the American Institute of Electrical Engineers AIEE*, vol. 37, no. 2, pp. 1027-1140.

Franquelo, L. G., Prats, M. A. M., Portillo, R. C., Galvan, J. I. L., Perales, M. A., Carrasco, J. M., Diez, E. G., Jimenez, J. L. M., (2006), Three-dimensional space-vector modulation algorithm for four-leg multilevel converters using abc coordinates, *IEEE Trans. on Industrial Electronics*, vol. 53, no. 2, pp. 458-466.

Gao, L., Fletcher, J. E., (2010), A space vector switching strategy for three-level five-phase inverter drives, *IEEE Trans. on Industrial Electronics*, vol. 57, no. 7, pp. 2332-2343.

Gopakumar, K., Ranganthan, V. T., Bhat, S. R., (1993), Split-phase induction motor operation from PWM voltage source inverter, *IEEE Trans. on Industry Applications*, vol. 29, no. 5, pp. 927-932.

Grandi, G., Serra, G., Tani, A., (2006a), General analysis of multi-phase systems based on space vector approach, *Proc. EPE Power Electronics and Motion Control Conf. PEMC*, Portorož, Slovenia, pp. 834-840.

Grandi, G., Serra, G., Tani, A., (2006b), Space vector modulation of a seven-phase voltage source inverter, *Proc. Int. Symposium on Power Electronics, Electrical Drives, Automation and Motion SPEEDAM*, Taormina, Italy, CD-ROM paper S8-6.

Grandi, G., Serra, G., Tani, A., (2007), Space vector modulation of a nine-phase voltage source inverter, *Proc. IEEE Int. Symposium on Industrial Electronics ISIE*, Vigo, Spain, pp. 431-436.

Gupta, A. K., Khambadkone, A. M., (2006), A space vector PWM scheme for multilevel inverters based on two-level space vector PWM, *IEEE Trans. on Industrial Electronics*, vol. 53, no. 5, pp. 1631-1639.

Holmes, D. G., (1992), The general relationship between regular-sampled pulse-width-modulation and space vector modulation for hard switched converters, *Proc. IEEE Industry Applications Society Annual Meeting IAS*, Houston, TX, pp. 1002-1009.

Holmes, D. G., Lipo, T. A., (2003), *Pulse width modulation for power converters: principles and practice*, IEEE Press, Piscataway, NJ.

Huang, J., Corzine, K. A., (2008), A new walking pattern SVM technique for five-phase motor drives, *Proc. IEEE Industry Applications Society Annual Meeting IAS*, Edmonton, Alberta, Canada, CD-ROM.

Hutson, C. M., Venayagamoorthy, G. K., Corzine, K. A., (2008), Optimal SVM switching for a multilevel multi-phase machine using modified discrete PSO, *Proc. IEEE Swarm Intelligence Symposium SIS*, St. Louis, MO, CD-ROM.

Iqbal, A., (2005), Modelling and control of series-connected five-phase and six-phase two-motor drives, *PhD Thesis*, Liverpool John Moores University, Liverpool, U.K.

Iqbal, A., Levi, E., (2005), Space vector modulation schemes for a five-phase voltage source inverter, *Proc. European Power Electronics and Applications Conf. EPE*, Dresden, Germany, CD-ROM paper 0006.

Iqbal, A., Levi, E., (2006), Space vector PWM techniques for sinusoidal output voltage generation with a five-phase voltage source inverter, *Electric Power Components and Systems*, vol. 34, no. 2, pp. 119-140.

Jones, M., (2005), A novel concept of a multi-phase, multi-motor vector controlled drive system, *PhD Thesis*, Liverpool John Moores University, Liverpool, U.K.

Jones, M., Vukosavic, S. N., Dujic, D., Levi, E., (2009), A synchronous current control scheme for multiphase induction motor drives, *IEEE Trans. on Energy Conversion*, vol. 24, no. 4, pp. 860-868.

Jones, M., Satiawan, W., Levi, E., (2010), A five-phase multilevel space-vector PWM algorithm for a dual-inverter supplied drive, *Proc. IEEE Industrial Electronics Society Annual Conf. IECON*, Glendale, AZ, pp. 2461-2466.

Jones, M., Dordevic, O., Bodo, N., Levi, E., (2011a), PWM algorithms for multilevel inverter supplied multiphase variable-speed drives, *Proc. Int. Symposium on Power Electronics Ee 2011*, Novi Sad, Serbia.

Jones, M., Dujic, D., Levi, E., Prieto, J., Barrero, F., (2011b), Switching ripple characteristics of space vector PWM schemes for five-phase two-level voltage source inverters - Part 2: Current ripple, *IEEE Trans. on Industrial Electronics*, vol. 58, no. 7, pp. 2799 - 2808.

Jones, M., Dordevic, O., Bodo, N., Levi, E., (2012), PWM algorithms for multilevel inverter supplied multiphase variable-speed drives, *Electronics*, vol. 16, no. 1, pp. 22-31.

Kanchan, R. S., Baiju, M. R., Mohapatra, K. K., Ouseph, P. P., Gopakumar, K., (2005), Space vector PWM signal generation for multilevel inverters using only the sampled amplitudes of reference phase voltages, *IEE Proc.-Electric Power Applications*, vol. 152, no. 2, pp. 297-309.

Karugaba, S., Ojo, O., Abreham, M., (2011), Carrier based PWM scheme for a three-level diode-clamped five-phase voltage source inverter ensuring capacitor voltage balancing, *Proc. IEEE Applied Power Electronics Conf. and Exposition APEC*, Fort Worth, TX, pp. 1194-1201.

Kelly, J. W., Strangas, E. G., Miller, J. M., (2003), Multiphase space vector pulse width modulation, *IEEE Trans. on Energy Conversion*, vol. 18, no. 2, pp. 259-264.

Kouro, S., Malinowski, M., Gopakumar, K., Pou, J., Franquelo, L. G., Wu, B., Rodriguez, J., Perez, M. A., Leon, J. I., (2010), Recent advances and industrial applications of multilevel converters, *IEEE Trans. on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580.

Lee, Y., Kim, D., Hyun, D., (2000), Carrier based SVPWM method for multi-level system with reduced HDF [harmonic distortion factor], *Proc. IEEE Industry Applications Society Annual Meeting IAS*, Rome, Italy, pp. 1996-2003.

Leon, J. I., Franquelo, L. G., Galvan, E., Prats, M. M., Carrasco, J. M., (2004), Generalized analytical approach of the calculation of the harmonic effects of single phase multilevel PWM inverters, *Proc. IEEE Industrial Electronics Society Annual Conf. IECON*, Busan, South Korea, pp. 1658-1663.

Leon, J. I., Portillo, R., Franquelo, L. G., Vazquez, S., Carrasco, J. M., Dominguez, E., (2007), New space vector modulation technique for single-phase multilevel converters, *Proc. IEEE Int. Symposium on Industrial Electronics ISIE*, Vigo, Spain, pp. 617-622.

Leon, J. I., Portillo, R., Vazquez, S., Padilla, J. J., Franquelo, L. G., Carrasco, J. M., (2008a), Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters, *IEEE Trans. on Industrial Electronics*, vol. 55, no. 9, pp. 3239-3248.

Leon, J. I., Vazquez, S., Watson, A., Franquelo, L. G., Wheeler, P., Carrasco, J. M., (2008b), A simple and low cost modulation technique for single-phase multilevel cascade converters based on geometrical considerations, *Proc. IEEE Int. Conf. Industrial Technology ICIT*, Chengdu, China, CD-ROM.

Leon, J. I., Vazquez, S., Kouro, S., Franquelo, L. G., Carrasco, J. M., Rodriguez, J., (2009a), Unidimensional modulation technique for cascaded multilevel converters, *IEEE Trans. on Industrial Electronics*, vol. 56, no. 8, pp. 2981-2986.

Leon, J. I., Vazquez, S., Watson, A. J., Franquelo, L. G., Wheeler, P. W., Carrasco, J. M., (2009b), Feed-forward space vector modulation for single-phase multilevel cascaded converters with any DC voltage ratio, *IEEE Trans. on Industrial Electronics*, vol. 56, no. 2, pp. 315-325.

Leon, J. I., Lopez, O., Franquelo, L. G., Doval-Gandoy, J., Vazquez, S., Alvarez, J., Freijedo, F. D., (2010a), Multilevel multiphase feedforward space-vector modulation technique, *IEEE Trans. on Industrial Electronics*, vol. 57, no. 6, pp. 2066-2075.

Leon, J. I., Vazquez, S., Sanchez, J. A., Portillo, R., Franquelo, L. G., Carrasco, J. M., Dominguez, E., (2010b), Conventional space-vector modulation techniques versus the single-phase modulator for multilevel converters, *IEEE Trans. on Industrial Electronics*, vol. 57, no. 7, pp. 2473-2482.

Leon, J. I., Kouro, S., Vazquez, S., Portillo, R., Franquelo, L. G., Carrasco, J. M., Rodriguez, J., (2011), Multidimensional modulation technique for cascaded multilevel converters, *IEEE Trans. on Industrial Electronics*, vol. 58, no. 2, pp. 412-420.

Levi, E., Jones, M., Vukosavić, S. N., Toliyat, H. A., (2004), A novel concept of a multiphase, multimotor vector controlled drive system supplied from a single voltage source inverter, *IEEE Trans. on Power Electronics*, vol. 19, no. 2, pp. 320-335.

Levi, E., Bojoi, R., Profumo, F., Toliyat, H. A., Williamson, S., (2007), Multiphase induction motor drives - a technology status review, *IET Electric Power Applications*, vol. 1, no. 4, pp. 489-516.

Levi, E., (2008), Multiphase electric machines for variable-speed applications, *IEEE Trans. on Industrial Electronics*, vol. 55, no. 5, pp. 1893-1909.

Levi, E., Dujic, D., Jones, M., Grandi, G., (2008), Analytical determination of DC-bus utilization limits in multiphase VSI supplied AC drives, *IEEE Trans. on Energy Conversion*, vol. 23, no. 2, pp. 433-443.

Levi, E., Jones, M., Satiawan, W., (2010), A multiphase dual-inverter supplied drive structure for electric and hybrid electric vehicles, *Proc. IEEE Vehicle Power and Propulsion Conf. VPPC*, Lille, France, CD-ROM paper 95-45630.

Locment, F., Semail, E., Kestelyn, X., Bouscayrol, A., (2006), Control of a seven-phase axial flux machine designed for fault operation, *Proc. IEEE Industrial Electronics Society Annual Conf. IECON*, Paris, France, pp. 1101-1107.

López, O., Alvarez, J., Doval-Gandoy, J., Freijedo, F., Nogueiras, A., Penalver, C. M., (2008a), Multilevel multiphase space vector PWM algorithm applied to three-phase converters, *Proc. IEEE Industrial Electronics Society Annual Conf. IECON*, Orlando, FL, pp. 3290-3295.

López, O., Alvarez, J., Doval-Gandoy, J., Freijedo, F. D., (2008b), Multilevel multiphase space vector PWM algorithm, *IEEE Trans. on Industrial Electronics*, vol. 55, no. 5, pp. 1933-1942.

López, O., Alvarez, J., Doval-Gandoy, J., Freijedo, F. D., (2009a), Multilevel multiphase space vector PWM algorithm with switching state redundancy, *IEEE Trans. on Industrial Electronics*, vol. 56, no. 3, pp. 792-804.

López, O., Levi, E., Freijedo, F. D., Doval-Gandoy, J., (2009b), Number of switching state vectors and space vectors in multilevel multiphase converters, *Electronics Letters*, vol. 45, no. 10, pp. 524-525.

Lu, S., Corzine, K., (2005), Multilevel multi-phase propulsion drives, *Proc. IEEE Electric Ship Technologies Symposium ESTS*, Philadelphia, PA, pp. 363-370.

Malik, S., Kluge, D., (1998), ACS 1000—World's first standard AC drive for medium-voltage applications, *ABB Review*, vol. 2, pp. 4–11.

Manjrekar, M. D., Steimer, P. K., Lipo, T. A., (2000), Hybrid multilevel power conversion system: a competitive solution for high-power applications, *IEEE Trans. on Industry Applications*, vol. 36, no. 3, pp. 834-841.

Massoud, A. M., Finney, S. J., Williams, B. W., (2008), Systematic analytical-based generalised algorithm for multilevel space vector modulation with a fixed execution time, *IET Power Electronics*, vol. 1, no. 2, pp. 175-193.

McGrath, B. P., Holmes, D. G., (2002), Multicarrier PWM strategies for multilevel inverters, *IEEE Trans. on Industrial Electronics*, vol. 49, no. 4, pp. 858-867.

McGrath, B. P., Holmes, D. G., Lipo, T., (2003), Optimized space vector switching sequences for multilevel inverters, *IEEE Trans. on Power Electronics*, vol. 18, no. 6, pp. 1293-1301.

Mohapatra, K. K., Gopakumar, K., Somasekhar, V. T., Umanand, L., (2002), A novel modulation scheme for a six phase induction motor with open-end windings, *Proc. IEEE Industrial Electronics Society Annual Conf. IECON*, Seville, Spain, pp. 810-815.

Mohapatra, K. K., Gopakumar, K., (2006), A novel split phase induction motor drive without harmonic filters and with linear voltage control for the full modulation range, *European Power Electronics Journal*, vol. 16, no. 4, pp. 20-28.

Mwinyiwiwa, B., Ojo, O., Wu, Z., (2006), A five phase three-level neutral point clamped converter using DSP and FPGA based control scheme, *Proc. IEEE Power Electronics Specialists Conf. PESC*, Jeju, South Korea, pp. 3266-3272.

Nho, N. V., Lee, H.-H., (2007), Carrier PWM algorithm for multileg multilevel inverter, *Proc. European Power Electronics and Applications Conf. EPE*, Aalborg, Denmark, CD-ROM.

Oppenheim, A. V., Willsky, A. S., Nawab, H. S., (1997), *Signals and systems*, Prentice Hall Press, Upper Saddle River, NJ.

Oppenheim, A. V., Schafer, R. W., (2009), *Discrete-time signal processing*, Prentice Hall Press, Upper Saddle River, NJ.

Panagis, P., Stergiopoulos, F., Marabeas, P., Manias, S., (2008), Comparison of state of the art multilevel inverters, *Proc. IEEE Power Electronics Specialists Conf. PESC*, Rhodes, Greece, pp. 4296-4301.

Pereira, I., Martins, A., (2009a), Multicarrier and space vector modulation for three-phase NPC converters: A comparative analysis, *Proc. European Power Electronics and Applications Conf. EPE*, Barcelona, Spain, CD-ROM.

Pereira, I., Martins, A., (2009b), Experimental comparison of carrier and space vector PWM control methods for tree-phase NPC converters, *Proc. Int. Conf. on Renewable Energies and Power Quality ICREPQ*, Valencia, Spain, CD-ROM.

Prats, M. M., Franquelo, L. G., Portillo, R., Leon, J. I., Galvan, E., Carrasco, J. M., (2003), A 3-D space vector modulation generalized algorithm for multilevel converters, *IEEE Power Electronics Letters*, vol. 1, no. 4, pp. 110-114.

Riveros, J. A., Yepes, A. G., Barrero, F., Doval-Gandoy, J., Bogado, B., Lopez, O., Jones, M., Levi, E., (2012), Parameter identification of multiphase induction machines with distributed windings; Part 2: Time-domain techniques, *IEEE Trans. on Energy Conversion*, vol. 27, no. 4, pp. 1067-1077.

Rodríguez, J., Lai, J. S., Peng, F. Z., (2002), Multilevel inverters: A survey of topologies, controls and applications, *IEEE Trans. on Industrial Electronics*, vol. 49, no. 4, pp. 724-738.

Rodríguez, J., Bernet, S., Wu, B., Pontt, J. O., Kouro, S., (2007), Multilevel voltage-source-converter topologies for industrial medium-voltage drives, *IEEE Trans. on Industrial Electronics*, vol. 54, no. 6, pp. 2930-2945.

Ruderman, A., Reznikov, B., (2010a), Time domain evaluation of filterless grid-connected multilevel PWM converter voltage quality, *Proc. IEEE Int. Symposium on Industrial Electronics ISIE*, Bari, Italy, pp. 2940-2945.

Ruderman, A., Reznikov, B., (2010b), PWM power converter voltage quality bounds and their applicability to non-PWM control schemes, *Proc. Int. Conf. Optimization of Electrical and Electronic Equipment OPTIM*, Brasov, Romania, pp. 618-624.

Ruderman, A., Reznikov, B., Busquets-Monge, S., (2013), Asymptotic time domain evaluation of a multilevel multiphase PWM converter voltage quality, *IEEE Trans. on Industrial Electronics*, vol. 60, no. 5, pp. 1999-2009.

Satiawan, W., (2012), Pulse width modulation control of dual-inverter supply for five-phase variable-speed drives, *PhD Thesis*, Liverpool John Moores University, Liverpool, U.K.

Schmitt, B. P., Sommer, R., (2001), Retrofit of fixed speed induction motors with medium voltage drive converters using NPC three-level inverter high-voltage IGBT based topology, *Proc. IEEE Int. Symposium on Industrial Electronics ISIE*, Busan, Korea, pp. 746-751.

Seyed, S. F., (2007), Investigation and comparison of multi-level converters for medium voltage applications, *PhD Thesis*, Technische Universität Berlin, Berlin, Germany.

Song, Q., Zhang, X., Yu, F., Zhang, C., (2006), Research on PWM techniques of five-phase three-level inverter, *Proc. Int. Symposium on Power Electronics, Electrical Drives, Automation and Motion SPEEDAM*, Taormina, Italy, pp. 561-565.

Stemmler, H., Guggenbach, P., (1993), Configurations of high-power voltage source inverter drives, *Proc. European Power Electronics and Applications Conf. EPE*, Brighton, U.K., vol. 5, pp. 7-14.

Toliyat, H. A., Lipo, T. A., White, J. C., (1991), Analysis of a concentrated winding induction machine for adjustable speed drive applications. II. Motor design and performance, *IEEE Trans. on Energy Conversion*, vol. 6, no. 4, pp. 684-692.

Van Der Broeck, H. W., (2003), Analytical calculation of the harmonic effects of single phase multilevel PWM inverters, *Proc. IEEE Industrial Electronics Society Annual Conf. IECON*, Roanoke, VA, pp. 243-248.

Wang, F., (2002), Sine-triangle versus space-vector modulation for three-level PWM voltage-source inverters, *IEEE Trans. on Industry Applications*, vol. 38, no. 2, pp. 500-506.

Ward, E. E., Härer, H., (1969), Preliminary investigation of an invertor-fed 5-phase induction motor, *Proc. of the Institution of Electrical Engineers*, vol. 116, no. 6, pp. 980-984.

White, D. C., Woodson, H. H., (1959), *Electromechanical energy conversion*, New York, NY, John Wiley & Sons.

Wu, B., (2006), *High-power converters and AC drives*, Hoboken, NJ, IEEE Press - John Wiley & Sons.

Yao, W., Hu, H., Lu, Z., (2008), Comparisons of space-vector modulation and carrier-based modulation of multilevel inverter, *IEEE Trans. on Power Electronics*, vol. 23, no. 1, pp. 45-51.

Yepes, A. G., Riveros, J. A., Doval-Gandoy, J., Barrero, F., Lopez, O., Bogado, B., Jones, M., Levi, E., (2012), Parameter identification of multiphase induction machines with distributed windings; Part 1: Sinusoidal excitation methods, *IEEE Trans. on Energy Conversion*, vol. 27, no. 4, pp. 1056-1066.

Yousefpoor, N., Fathi, S. H., Farokhnia, N., Abyaneh, H. A., (2012), THD minimization applied directly on the line-to-line voltage of multilevel inverters, *IEEE Trans. on Industrial Electronics*, vol. 59, no. 1, pp. 373-380.

Zhao, Y., Lipo, T. A., (1995), Space vector PWM control of dual three-phase induction machine using vector space decomposition, *IEEE Trans. on Industry Applications*, vol. 31, no. 5, pp. 1100-1109.

Appendix A

DESCRIPTION OF THE EXPERIMENTAL SETUP

A description of the used hardware for the experimental work in this thesis is given here. The main hardware units used are the two-level eight-phase and three-level six-phase custom made inverters and they were controlled by dSpace ds1006 real-time system. The software code that was running on ds1006 processor board was automatically generated and loaded from the Matlab/Simulink. Utilised machines in the experiments were symmetrical three-, five- and six-phase induction machines. Due to the unavailability of a seven-phase machine, a static *R–L* load was used for obtaining the experimental results. In what follows, each of the hardware components and used software are briefly discussed.

A.1 CUSTOM-BUILT INVERTERS

The main inverter in this research was the three-level neutral-point clamped (NPC) inverter. The basic topology of this inverter is as in Fig. 3.8, Fig. 4.1 and Fig. 4.25. For the purposes of experimental testing, two six-phase three-level inverters of NPC type have been built. They can be seen in Fig. A.1 and Fig. A.2. For some experimental results in Chapter 7, a two-level inverter has been used as well. All the inverters share the same control board for connection to the dSpace system, so they have the same protection features and a very similar interface.

The three-level NPC inverters have six output legs. As can be seen from Fig. 3.8a, each leg contains four IGBTs. The IGBTs are Semikron SKM50GB12T4 modules with two transistors with back-to-back diodes in the package. The maximum V_{CE} voltage is 1200V, and the nominal current is 50A. Each leg is controlled by two TTL signals, while gating signals for the second complementary switch are provided internally by the circuit that produces complementary signal and that implements dead time. The dead time is configurable in the hardware and is set to 6μs. If TTL signals that control each leg are denoted by S1 and S2, then the control logic for obtaining three-level output in the actual inverters is as in Table 3.2. Twelve TTL signals from dSpace PWM unit ds5101 are used for control of all six legs. Additional TTL input is required for enabling output of the inverter that is AND-ed with hardware ENABLE switch on the inverter. The inverters can be supplied from the three-phase mains or by the external dc source, which can be selected by MAIN POWER switch at front panel of the inverters. If mains supply is used, internal three-phase diode bridge rectifies the voltage. Equivalent values of the dc-bus bulk capacitors, using notation from Fig. 4.1 and Fig. 4.25, are C_{up}=C_{dn}=3mF. For the soft start dc-bus capacitors are charged through the 22Ω high-power resistor that should be shorted by SOFTSTART switch by putting it into RUN position after capacitors are fully charged. During all experiments an external dc-supply, Sorensen SGI 600/25, has been used rather than the mains. The rated power of the inverters is governed by the heat sink parameters, and if no additional cooling is provided it is about 17.8kVA. Inverters have built-in overvoltage, overcurrent and overtemperature protections. Dynamic braking resistor for the overvoltage

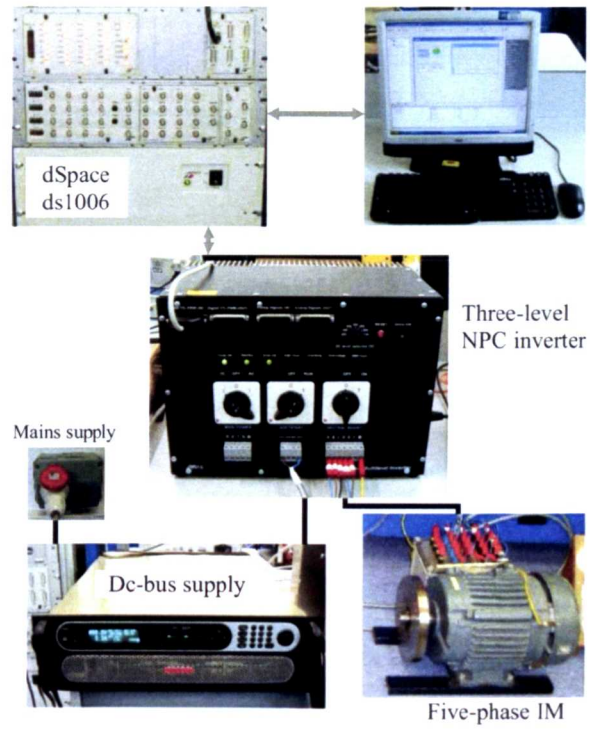


Fig. A.1: Experimental setup used for the analysed five-phase three-level algorithms.

protection enables selection of a few ranges for the limits. Inverters have feedback for measured currents and for measured dc-bus voltage. However, these values have not been utilised in the experiments in this thesis. All experiments have been done with no closed-loop control, so no feedback has been used.

The seven-phase inverter is obtained by connection of two six-phase inverter units in parallel, as demonstrated in Fig. A.2. The negative rail, mid-point and positive rail of the dc-circuits of the inverters are connected each one to the other. Had the mains and the internal rectifier been used, the connection of two inverters would have been more complicated. This is the main reason why the external dc supply was used. Two TTL signals that have not been used for control of the legs of the first inverter are taken out and connected to appropriate pins of the second inverter to control leg A, that is used as the seventh leg of the system (i.e. leg G in Fig. 4.25).

The two-level inverters have up to 8 output legs. One such inverter has been used for the experiments with three-, five-, six-phase induction machine and with the seven-phase symmetrical *R-L* load. These results are used in Chapter 7 for obtaining the leg and phase voltage THD plots (Fig. 7.23 and Fig. 7.26). Used switches inside the two-level inverters are three six-pack Infineon modules FS50R12KE3. This provides 9 legs with two transistors per-leg. Eight legs are used for providing output voltage, while one transistor from the ninth leg is used for the dynamic breaking. Equivalent dc-bus bulk capacitance is 1.5mF. Modes of supply and protections are the same as for the three-level inverters. This inverter was, again, supplied from the external dc-source Sorensen SGI 600/25.

A.2 DATA OF THE FIVE-PHASE MACHINE AND STATIC LOAD

Several machines were used in the experiments in this thesis. However, more detailed analysis, including current analysis, is only shown for the five-phase case. Other used machines, three- and six-phase, were used for

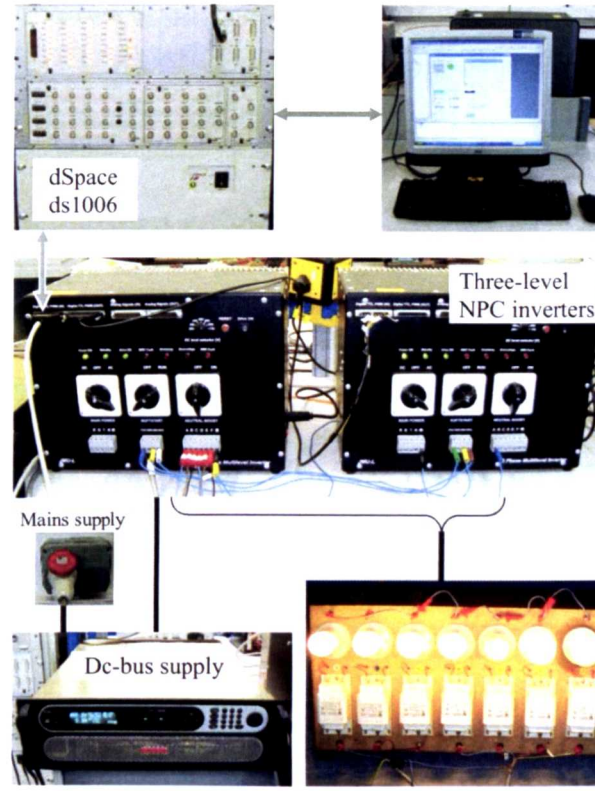


Fig. A.2: Experimental setup used for the analysed seven-phase three-level algorithms.

obtaining leg and phase voltage power and THD results for comparison with analytical curves in Chapter 7. For this analysis, exact parameters of the machine are not important, and the only relevant factor is that machine/load is symmetrical. It should be mentioned that the six-phase machine has a lower nominal phase voltage, hence to avoid saturation dc-bus voltage during the experiments was lowered to 250V. In all other cases dc-bus voltage was kept at 600V. For the seven-phase case a symmetrical *R-L* load, consisting of chokes and light bulbs, were used. The seven-phase *R-L* load can be seen in Fig. A.2. For these reasons, only parameters of the five-phase induction machine and the seven-phase *R-L* load will be given here.

The five-phase machine was obtained by cutting new stator laminations with 40 slots for a machine that was originally a three-phase one. The five-phase machine's winding is single-layer, with 4 poles (two pole pairs). The winding has 2 slots per phase per pole, and the winding pitch is 10 slots. Each phase winding consists of two half-windings that can be connected either in series or in parallel. During all tests half-windings were connected in series.

Parameters of the five-phase induction machine are given in Table A.1 and are assumed as a being constant at all times. A more detailed discussion, related to the estimation of the parameters of this machine, is

Table A.1: Five-phase induction machine parameters.

Parameter	Symbol	Value
Stator resistance	R_s	3Ω
Rotor resistance	R_r	3Ω
Stator leakage inductance	L_{ls}	45mH
Rotor leakage inductance	L_{lr}	15mH
Magnetising inductance	L_m	515mH

Table A.2: Static seven-phase *R-L* load parameters.

m	0.1	0.2	0.3	0.4	0.5	0.6	0.7	0.8	0.9	1
R [Ω]	150	238	295	342	380	413	444	472	499	522

The inductance was practically constant for all modulation indices. Estimated value is: 360mH.

available in [Riveros et al. (2012), Yepes et al. (2012)].

Parameters of the static *R-L* load are given in Table A.2. These parameters have been estimated by voltage, current and power measurement for the first harmonic.

A.3 DESCRIPTION OF THE SOFTWARE AND MEASUREMENTS

All simulation results have been obtained using Matlab/Simulink and PLECS Block-Set software. The initial model of the multiphase machine has been developed in [Đorđević et al. (2010)]. This was further extended to a new model, developed in PLECS Block-Set using electrical components, and this model has been used for obtaining all the simulation results shown in this thesis.

A few programmes have been developed for the fast measurement data collection and for fast data processing. All signals were recorded by the mixed signal oscilloscope Tektronix MSO2014. For measurement of the high voltages, voltage dividers with the ratio of 1/52 (10kΩ/(10kΩ+510kΩ)) were used. Three such dividers were connected between the output of the inverter and the ground, star of the load and the ground and negative dc rail and the ground. The resulting low voltages were measured on channels 1 to 3, respectively. Finally, leg voltage was determined as (Ch1–Ch3)·52, phase voltage was determined as (Ch1–Ch2)·52 and common mode voltage was determined as (Ch2–Ch3)·52, where Ch1 to Ch3 represent voltages measured on the oscilloscope. Channel 4 was always used for the current measurement, using the current probe Tektronix TCP0030. The oscilloscope is a deep memory scope and all the measurements were done by saving 125000 samples per channel. For the fast collection of the data, Python script for control of the oscilloscope from the PC and for fast data collection has been developed. With this script all settings of the oscilloscope for each modulation index are adjusted automatically, and also time for saving the data to the PC is reduced roughly 8 times.

As already mentioned in 4.2.8, Matlab script has been developed for the fast processing of the data. This script produces final reports with leg, phase, and common mode voltage, and current waveforms for each modulation index, and also another file that contains the THD via modulation index data in tabular form, for all the measured waveforms. Script searches for the sample when the angle of the leg voltage fundamental is zero, and takes one period of the signals starting from that point. In this way all leg voltages start as a cosine function, thus all shown results in the thesis are represented in the same manner. The same script has been used for processing data from simulations. This provides an easy comparison of all shown results.

The software used together with the dSpace system are Matlab/Simulink, Control Desk and dSpace Profiler tool. Matlab and Simulink were used for creating the model and programming of the dSpace by incremental building of the developed model. Control Desk has been used for creating graphical user interface for control of the particular Simulink variables and for their visualisation. Profiler tool is the dSpace tool for time measurements, and it has been used for control algorithm execution time measurements in the complexity comparison of developed modulation strategies.