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Performance Analysis of Video PHY Controller Using Unidirection and Bi-directional IO Standard via 7 Series FPGA

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Abstract— **The Video PHY controller offers an interface between transmitters/receivers and video ports. These video ports are categorized in HDMI or Displayport. HDMI Video PHY controller are mostly used for their high speed operation for high resolution graphics. However, the execution of high resolution graphics consumes more power, this creates a need of designing the low power design for Video PHY controller. In this paper, the performance of Video PHY controller is analyzed by comparing the power consumption of unidirectional and bi-directional IO Standard over 7 series FPGA. It is determined that total on-chip power is reduced for unidirectional IO Standard based Video PHY controller compared to bidirectional IO Standard based Video PHY controller. The most significant achievement of this work is that it is concluded that unidirectional IO Standard based Video PHY controller consume least standby power compared to bidirectional IO Standard based Video PHY controller. It is defined that for 6 GHz operated frequency Video PHY controller, the 32% total on-chip power is reduced using unidirectional IO Standard based Video PHY controller is less compared to bidirectional IO Standard based Video PHY controller. It is also demonstrated that 97% device static power i.e. standby mode power consumption is reduced using unidirectional IO Standard based Video PHY controller is less compared to bidirectional IO Standard based Video PHY controller. The proposed design will be to provide high resolution video processing at low standby power consumption using unidirectional IO Standard based Video PHY controller is less compared to bidirectional IO Standard based Video PHY controller.**

Keywords- Power Consumption, Static Power Consumption, Standby Power Consumption, Unidirectional and Bidirectional IO Standard, Video PHY Controller, 7 Series Field Prograaming Gate Array.

I. INTRODUCTION

The Video PHY controller is used to organize, the PHY layer with video controllers. The Video PHY controller offers the processing of high resolution video data. It is reported that the processing of high resolution video consumes high power for operating frequencies of 2.0 GHz to 6.25 GHz [1-2]. There are several techniques are utilized in order to control or reduce the power consumption of different devices such as; optical transmitter [3], energy efficient laser driver [4], Ethernet [5], filters [6]. These techniques include; these techniques include; clock gating, voltage scaling [7], variable frequency and etc. However, each techniques has its own advantages and disadvantages. It has been demonstrated in [8-9] that for different variation in suitable IO Standard the power consumption of device can be reduced depend upon the core voltage of Field Programming Gate Array (FPGA), operating voltage of the device and IO Standard voltage selected for particular device. There are different types of IO Standard. The unidirectional and bi-directional IO Standard are categorized for their signal termination. The unidirectional signaling defines IO pins are assigned for signal transferring via input to output or vice versa. In the IO Standard description, the DCI versions of class-I

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SSTL and HSTL I/O standards only have internal split-termination resistors present on inputs (not outputs). The DCI versions of class-II SSTL and HSTL I/O standards always have internal split-termination resistors present on input, outputs, or bidirectional pins. There are different IO Standard are available in 7 series FPGA, such as; unidirectional IO Standard, bi-directional IO Standard and also some of the both unidirectional and bi-directional IO Standard [11]. In this paper, the power analysis for low power consumption is demonstrated for Video PHY controller for high frequency using unidirectional and bi-directional IO Standard via 7 series Field Programming Gate Array. It is important to note that unidirectional and bi-directional IO Standard are of many types, the selection of particular IO Standard depends upon the specific circuit and the core voltage of FPGA.

II. METHODOLOGY

The power analysis for Video PHY controller at high frequency using unidirectional and bi-directional IO Standard is designed using different design steps as demonstrated in Figure 1. It is illustrated in Figure 1 that in first design step, Video PHY controller is designed using Vivado design suite via vhdl coding by defining the different parameters and configuration of transmitter and receiver. In the second design step, the vhdl based Video PHY controller is designed using unidirectional and bi-directional IO Standard. The IO Standard are selected based upon the core voltage of FPGA, and operating voltage of Video PHY controller. In the third design step, the vhdl Video PHY controller using unidirectional and bi-directional IO Standard is tested for different high frequencies in order to analyze the performance of the designed low power Video PHY controller.

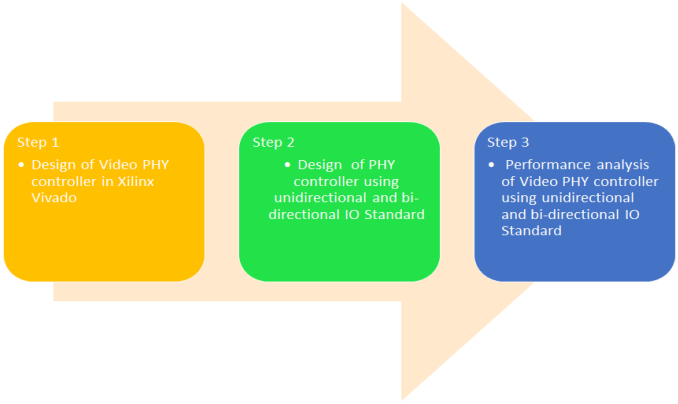

Figure 1. Design steps for performance analysis of Video PHY controller using unidirectional and bi-directional IO Standard

A. Design Step 1: vhdl based HDMI based Video PHY controller

The HDMI based Video PHY controller is designed in Xilinx Vivado Suite using vhdl. The elaborated/schematic design of Video PHY controller is shown in Figure 2.

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Figure 2. Schematic design of Video PHY controller

The Video PHY controller in Figure 2 is designed using different protocols parameters as illustrated in Table 1.

Table 1. Protocol parameters for HDMI based Video PHY controller

NAME OF PARAMETER	PARAMETER CONFIGURATION
Tx Protocol	DP
Tx Max GT line rate	5.4 Gb/s
Tx channels	2
Tx PLL type	QPLL 0/2
Tx Ref Clock	GTREFCLK1
Rx Protocol	HDMI
Rx Max GT line rate	5.4 Gb/s
Rx channels	3
Rx PLL type	CPLL
Rx Ref Clock	GTREFCLK0
No of pixels per clock	8
Clock Frequency	60 MHz

Table 1 describes the different protocols parameters for HDMI based Video PHY controller. The interface for the Video controller is HDMI. There different clock signals are utilized to synchronize the transmitter and receiver data rate. In 7 series FPGA, an I/O tile is defined with I/O buffers, I/O logics and I/O delays. Each IOB contains both input and output logic and IO drivers. These drivers can be configured to various I/O standards [9]. The IO Standard based schematic diagram of Video PHY controller is demonstrated using Figure 3. It is defined in Figure 2 device configuration has been changed by adding the IO Standard and its related operating voltage in VHLD based HDMI based Video PHY controller. Virtex 7 series FPGA support many IO Standard a long list is available in [11]. In this research, authors have selected the unidirectional and bi-directional IO Standards that meet the requirements for Video PHY controller. These IO Standards are specified in the Electronic Industry Alliance JEDEC [10]. The reason for selecting the unidirectional and bi-directional IO Standards for Video PHY controller is that to compare the performance of Video PHY controller at unidirectional and bi-directional IO Standards. Both unidirectional and bi-directional IO Standards has there own characteristics. It is advisable to verify the power

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consumption of Video PHY controller at unidirectional and bi-directional IO Standards. In the IO Standard description, the DCI versions of class-I SSTL and HSTL I/O standards only have internal split-termination resistors present on inputs (not outputs). The DCI versions of class-II SSTL and HSTL I/O standards always have internal split-termination resistors present on input, outputs, or bidirectional pins. In the next section, the unidirectional and bi-directional Io Standard specification are discussed.

1) Unidirectional and Bi-directional IO Standard Specification

It is defined in [11] that class-I SSTL and HSTL I/O standards are only supported for unidirectional. In this work, the class-I HSTL is considered because the video controller need a high speed buffering for video processing. HSTL (High-Speed Transceiver Logic) is the IO Standard for high-speed bus standard is defined by JEDEC (JESD8-6). The HSTL standards have four variations (classes), to support clocking high-speed memory interfaces. 7 series FPGA I/O supports class-I for the 1.2V version of HSTL (in HP banks), and class-I and II for the 1.5V and 1.8V versions, including the differential versions. HSTL_ I use VCCO/2 as a parallel-termination voltage (VTT) and are intended for use in unidirectional links. HSTL_ II use VCCO/2 as a parallel-termination voltage (VTT) and are intended for use in bidirectional links. This HSTL IO Standard is also configured for different other Io Standards such as; DCI (Digital Controlled Impedance), DIFF (Differential Impedance) [11]. In this paper, only the HSTL IO Standard with Class I and II are utilized for developing the unidirectional and bidirectional IO Standard base design for Video PHY controller. The syntax for changing the IO Standards from default to user defined unidirectional and bidirectional IO Standard is mentioned as following manner:

a) For HSTL_ I IO Standard

```
attribute IOSTANDARD : string;
attribute IOSTANDARD of IDIOA0 :
label is- "HSTL_ I";
```

b) For HSTL_ II IO Standard

```
attribute IOSTANDARD : string;
attribute IOSTANDARD of IDIOA0 :
label is- "HSTL_ II";
```

In the above discussion, unidirectional and bidirectional IO Standard section and syntax to choose the unidirectional and bidirectional IO Standard for Video PHY controller is demonstrated in the next, the performance of the Video PHY controller is analyzed for aforementioned Io Standards.

B. Design Step 3: Performance Analysis of IO Standard based HDMI based Video PHY controller using power analysis

The performance of the unidirectional and bidirectional IO Standard based Video PHY controller IO Standard based HDMI Video PHY controller is analyzed for high frequency operation of 6 GHz. The power analysis is performed for these high frequencies using HSTL_ I IO Standard, and HSTL_ II IO Standard, and HSTL_ II_18 IO Standard. The power analysis for Video PHY controller in 7 series FPGA power is comprises of sum of device static power, design static power and design dynamic power presented in equation (1) [9].

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Total FPGA power = Design Dynamic Power + Device Static Power + Design Static Power (1)

Device static power characterizes the transistor leakage power when devices is powered and not configured. Design Dynamic power epitomizes the power associated with design activity and switching events in the core or I/O of the device. Dynamic power is determined by node capacitance, supply voltage, and switching frequency. Design static power denotes the power consumption when the device is configured with no switching activates. The power consume by clock manager. In the next section, the power analysis is performed for Video PHY controller IO Standard for different IO Standards.

1) Performance Analysis of Video PHY controller for 6 GHz frequency via Unidirectional IO Standard

The performance of the Video PHY controller is analyzed for 6 GHz for Unidirectional IO Standard by measuring the on-chip power. The unidirectional IO Standards is selected for performance analysis is HSTL_ I IO Standard. The on-chip power consumption for HSTL_ I IO Standard at 6 GHz for Video PHY controller is illustrated in Table 1.

Table 1. Power Consumption in W for Video PHY controller using HSTL_ I IO Standard at 6 GHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
3.4	0.001	0.6	4.001

It is illustrated in Table 1 that when vhdl based design of Video PHY controller is operated at 6 GHz using HSTL_ I IO Standard. The total on-chip power consumption is 4.001 W. In this, the maximum power consumption is 3.4 W. The device static power consumption is recorded as 0.001 W. The design static power consumption is 0.6 W. In the next, the power consumption of vhdl based design of Video PHY controller is operated at 6 GHz is analyzed for bidirectional IO Standard.

2) Performance Analysis of Video PHY controller for 6 GHz frequency via Bidirectional IO Standard

The performance of the Video PHY controller is analyzed for 6 GHz for bidirectional IO Standard by measuring the on-chip power. The bidirectional IO Standards is selected for performance analysis is HSTL_ II IO Standard. The on-chip power consumption for HSTL_ I IO Standard at 6 GHz for Video PHY controller is illustrated in Table 2.

Table 2. Power Consumption in W for Video PHY controller using HSTL_ II IO Standard at 6 GHz

Design Dynamic Power	Device Static Power	Design Static Power	Total Power
4.67	0.045	1.25	5.965

Table 2 shows the on-chip power consumption for vhdl based design of Video PHY controller operated at 6 GHz using HSTL_II IO Standard. The total on-chip power consumption is 5.965 W. It can be analyzed that design dynamic power is increased compared to unidirectional IO Standard design for vhdl based design of Video PHY controller is operated at 6 GHz. The most important thing to note that standby mode power

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i.e. device static power is increased to 0.045 W for vhdl based design of Video PHY controller operated at 6 GHz using HSTL_II IO Standard compared to vhdl based design of Video PHY controller operated at 6 GHz using HSTL_I IO Standard. In this section, the power analysis is discussed for Video PHY controller operated at 6 GHz for unidirectional and bidirectional IO Standards. In the next section, the results attained are discussed for Video PHY controller operated at 6 GHz for unidirectional and bidirectional IO Standards.

III. RESULTS AND DISCUSSION

In this paper, power analysis for Video PHY controller is proposed using unidirectional and bidirectional IO Standard. The IO Standard are selected according to specification of for Video PHY controller and 7 series FPGA. It is determined that for Video PHY controller is tested 6 GHz using unidirectional and bidirectional IO Standards. The power consumption analysis for Video PHY controller is proposed using unidirectional and bidirectional IO Standard is demonstrated in Figure 3.

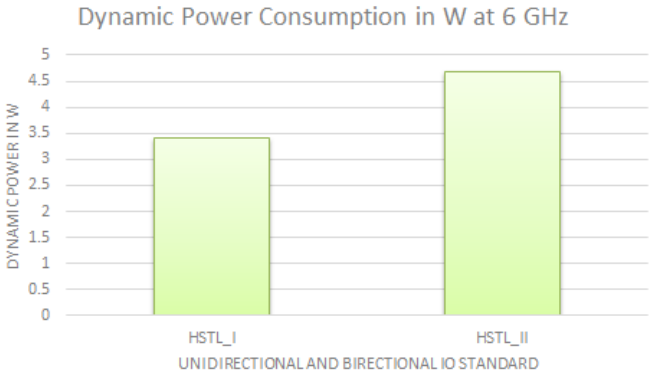

Figure 3. Design dynamic power analysis for Video PHY controller using unidirectional and bidirectional IO Standard

It can be analyzed from Figure 3 that when Video PHY controller is designed using unidirectional the design dynamic power consumption is 3.4 W. However, when Video PHY controller is designed using bidirectional IO Standard, the design dynamic power recorded is 4.67 W. It is determined that unidirectional IO Standard based design consumes less power than bidirectional IO Standard for Video PHY controller. The reason for this less power consumption is that HSTL_I which is unidirectional IO Standard has operating voltage of 1.5 V and HSTL_II which is bidirectional IO Standard has operating voltage of 1.8 V. The operating voltage of Video PHY controller is 1.5 V. The difference between core voltage of series 7 FPGA and bidirectional IO Standard based design of Video PHY controller is consume more power compared to unidirectional IO Standard based design of Video PHY controller. It can defined as 27% power reduction is achieved using unidirectional IO Standard based design of Video PHY controller compared to bidirectional IO Standard based design of Video PHY controller. The device static power consumption analysis for Video PHY controller using unidirectional and bidirectional IO Standard is demonstrated in Figure 4.

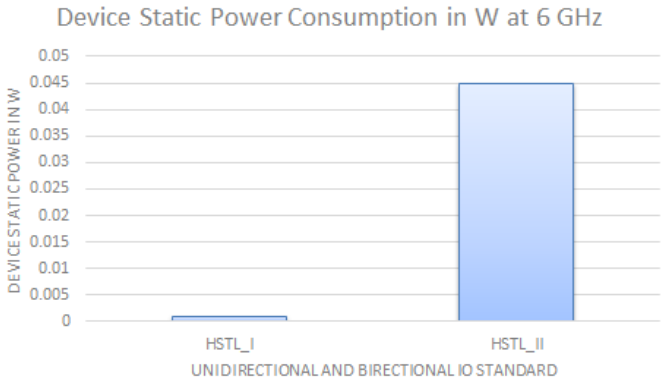

Figure 4. Device Static power analysis for Video PHY controller using unidirectional and bidirectional IO Standard

Figure 4 demonstrates the device static power consumption for Video PHY controller is designed using unidirectional and bidirectional IO Standard. It is illustrated that for unidirectional IO Standard based design of Video PHY controller device static power is 0.001 W. For bidirectional IO Standard based design of Video PHY controller device static power is 0.045 W. The device static power is more for bidirectional IO Standard based design of Video PHY controller. It is calculated that power reduction in device static power is attained for unidirectional IO Standard based design of Video PHY controller compared to bidirectional IO Standard based design of Video PHY controller. The power reduction is of 97%. It means the unidirectional IO Standard based design of Video PHY controller consumes very less power in standby mode. The reason for this less power consumption is the difference between the core voltage of 7 series FPGA and IO Standard based design of Video PHY controller. The difference between core voltage of 7 series FPGA and bidirectional IO Standard based design of Video PHY controller is high, due to this leakage current is increased and this cause to increase the device static power. Similarly, the power reduction of design static power of Video PHY controller is achieved for unidirectional Io Standard compared to bidirectional IO Standard based design of Video PHY controller. This power consumption is demonstrated in Figure 5.

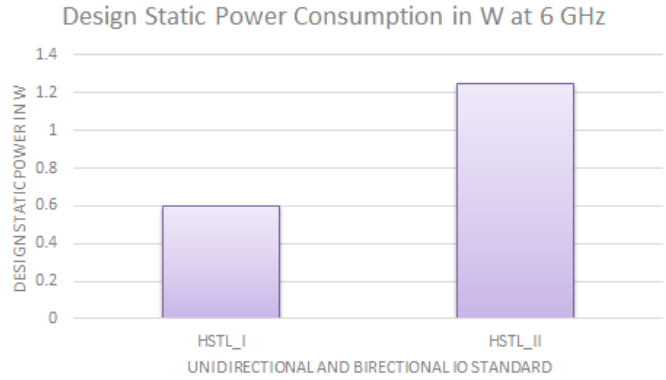

Figure 5. Design Static power analysis for Video PHY controller using unidirectional and bidirectional IO Standard

It can be analyzed from Figure 5 that when Video PHY controller is designed using unidirectional the design static power consumption is 0.6 W. However, when Video PHY controller is designed using bidirectional IO Standard, the design dynamic power recorded is 1.2 W. It is determined that unidirectional IO Standard based design consumes less power than bidirectional IO Standard for Video PHY controller. It is illustrated that 50% design

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static power reduction is achieved using unidirectional IO Standard based design of Video PHY controller compared to bidirectional IO Standard based design of Video PHY controller. The power consumption analysis for Video PHY controller is proposed using unidirectional and bidirectional IO Standard is demonstrated in Figure 3. The total on-chip power analysis is also performed for Video PHY controller using unidirectional and bidirectional IO Standard. It is shown in Figure 6 that total on-chip power of Video PHY controller is less for unidirectional IO Standard design for Video PHY controller compared to directional IO Standard based of Video PHY controller.

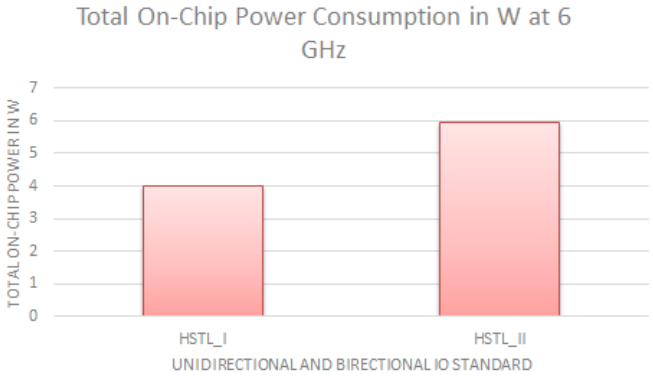

Figure 6. Total on-chip power analysis for Video PHY controller using unidirectional and bidirectional IO Standard

Figure 6 demonstrates the total on-chip power consumption for Video PHY controller for both unidirectional and bidirectional IO Standards. It can be analyzed that total power consumption of unidirectional IO Standard based Video PHY controller is less compared to bidirectional IO Standard based Video PHY controller. It can observed that total on-chip power for unidirectional IO Standard based Video PHY controller is 4.001 W and total on-chip power for bidirectional IO Standard based Video PHY controller is 5.965 W. It is determined that overall, 33% power reduction is achieved for unidirectional IO Standard based Video PHY controller compared to bidirectional IO Standard based Video PHY controller for 6 GHz operating frequency. The reason for this less power consumption for unidirectional IO Standard based Video PHY controller is that it has same operating voltage for Video PHY controller and for core voltage of 7 series FPGA. The unidirectional IO Standard based Video PHY controller also has less termination impedance compared to bidirectional IO Standard based Video PHY controller. It is therefore defined that Video PHY controller operated at 6 GHz, the unidirectional IO Standard based Video PHY controller consume less power compared to bidirectional IO Standard based Video PHY controller.

IV. CONCLUSION AND FUTURE WORK

The power performance analysis for Video PHY controller is proposed in this work using unidirectional and bidirectional IO Standard for high performance. The Video PHY controller is tested for high frequency operation of 6 GHz and 6 GHz unidirectional IO Standard based Video PHY controller and bidirectional IO Standard based Video PHY controller. The total on-chip power is calculated for Video PHY controller using unidirectional IO Standard and bidirectional IO Standard. It is defined that total 33% power consumption is reduced for based Video PHY controller using unidirectional IO Standard based Video PHY controller is less compared to bidirectional IO. It also defined using unidirectional IO Standard based Video PHY controller 95% standby power is saved compared to bidirectional IO Standard

based Video PHY controller. It is therefore, concluded that unidirectional IO Standard based Video PHY controller offers the least power consumption for standby mode. The unidirectional IO Standard based Video PHY controller will be supportive to produce high resolution video and will provide minimum standby power consumption. In the future, the resolution for the Video PHY controller can be improved using proposed technique at lowes standby power consumption.

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