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Performance evaluation of Type-3 PLLs under wide variation in input voltage and frequency

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***Abstract*— This paper presents a detailed analysis of Type-3 PLL under wide variation in input voltage and frequency. Using small signal modeling, the performance of both single loop and dual loop type-3 PLL for variation in input voltage and frequency is studied. The analysis shows that for the same bandwidth, both the single loop and dual loop Type-3 PLL exhibit similar dynamics provided the supply voltage is balanced. However, under voltage sag conditions, dual loop PLL shows improved dynamic response without affecting its stability. Further, the tracking time is reduced as the feed forward frequency is a function of supply frequency. To improve the filtering characteristics under frequency deviations, a dual loop Type 3 adaptive PLL which accurately tracks the phase and frequency of the input signal under wide frequency deviations is developed. Simulations are carried out in MATLAB and experimentally verified by implementing in ALTERA cyclone II FPGA board.**

***Index Terms*— Phase Locked Loop, Feed forward PLL, Type-3 PLL**

I. Introduction

The rapid increase in the utilization of renewable energy sources is changing the power generation scenario [1]. The improvement in the power electronics technology has made the integration of renewable energy system with the grid much easier [2]-[3]. On the other hand, increased penetration of the grid integrated systems can create instability in the power system [4]-[5]. Interfacing power electronic converters to the grid requires proper synchronization for the operation and control of power converter. The signals used for synchronization are often distorted due to the presence of harmonics, unbalance, and phase jump and frequency deviations that exist in the grid [6].

The synchronous reference frame (SRF) based Phase Locked Loop (PLL) is the widely used technique for grid synchronization in which the phase angle estimation is adaptively updated by a closed loop mechanism [7]-[9]. Though the technique is simple, it exhibits double frequency ripple under unbalance conditions [10]. Incorporating a low pass filter in the loop removes the high frequency ripple at the cost of increasing the response time [11]. Thus there is a need for improvement in the existing SRF PLL structure.

Various techniques [12]-[14] based on SRF PLL have been proposed to improve the performance of the system under distorted conditions. The addition of a notch filter [12] removes the double frequency ripple caused due to voltage unbalance and harmonics. However, when the frequency deviates from the nominal value, the performance of the system deteriorates, as the centre frequency of the notch filter is fixed. A chain of prefilters [13] are used to attenuate the different distortion components present in the grid and the phase lags introduced by the various filters are compensated by a lead compensator. The Adaptive Linear Optimal Filter (ALOF) [14] based PLL consists of separate sub filters for eliminating individual harmonics and the computational load of ALOF depends on the number of harmonics considered for elimination. Further, choosing the learning rate parameter is a cumbersome task as it has a significant effect on the frequency characteristics of the system, accuracy and the convergence speed. Based on signal reforming [15], the unbalance signals are reformed to balance signal without deteriorating the phase angle. This reforming process enhances it's response speed with a higher bandwidth. A variety of moving average filter based PLL are presented in the literature [16]-[18]. MAF [16] is one of the most popular and widely used techniques owing to its simple digital realization, low computational burden, and effectiveness. The incorporation of MAF [17] into the PLL structure drastically reduces the open loop bandwidth which in turn decreases the dynamic performance of the PLL. A differential MAF- PLL [17] is developed to improve the dynamic performance of the PLL. Further, to improve the response time, a dqCDSC PLL is developed [18] and detailed analysis shows that the performance of MAF and dqCDSC PLL are same under certain conditions. A comparative performance evaluation among the state-of-the-art orthogonal signal generator based phase-locked loops under grid abnormal condition is presented [19]. Moreover, an MAF filter is incorporated to improve the performance of PLL.

Introduction of lead compensators [20] in the PLL structure claims to obtain fast tracking of the grid voltage phase. The lead compensators are designed to selectively eliminate specific frequencies and introduce a phase boost. The low-pass filter, which is used to avoid oscillations and instability in steady state, reduces the bandwidth of the PLL. Further, the

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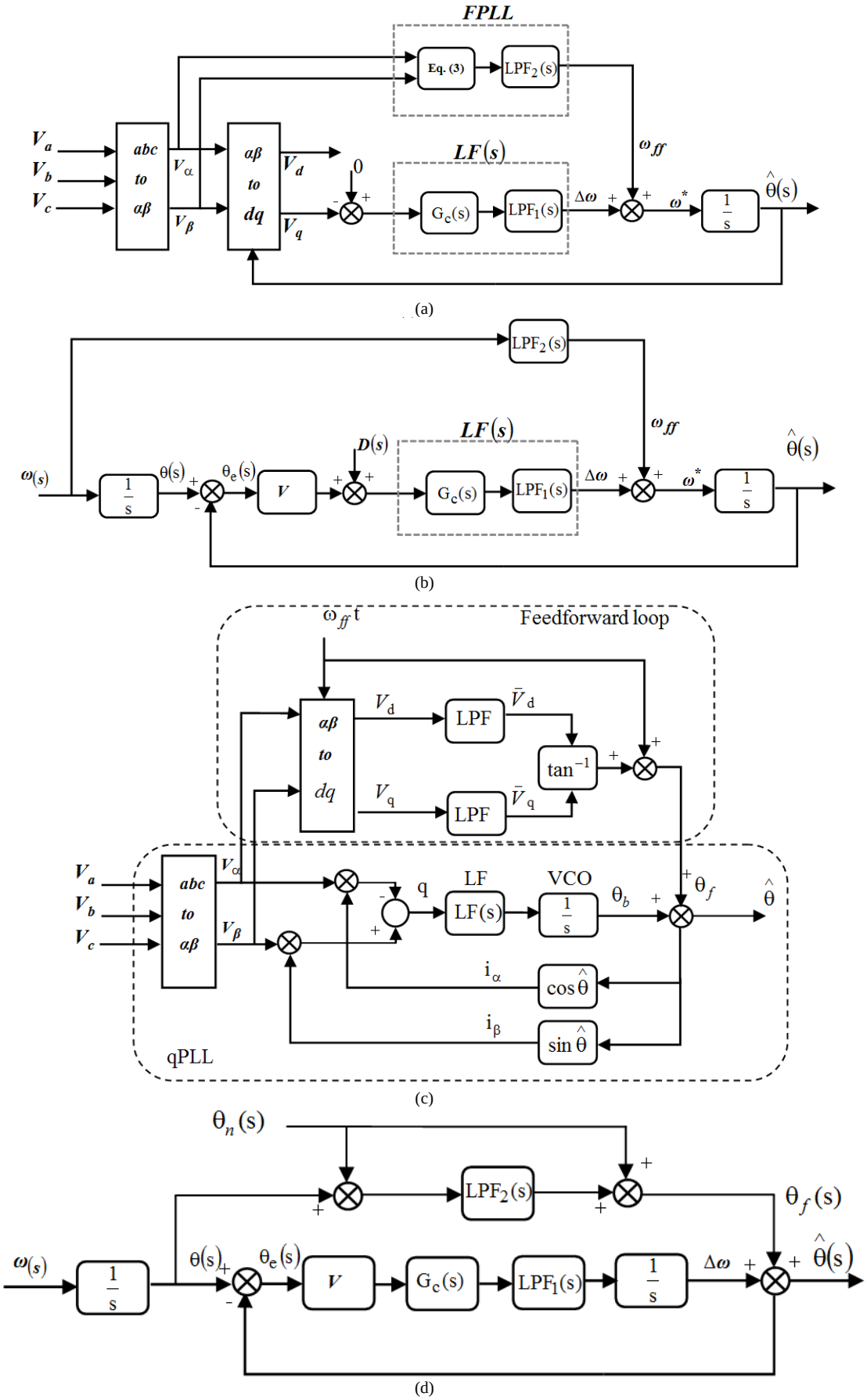


Fig. 1. Dual loop Type-3 PLL (a) FPLL (b) Small-signal model of FPLL (c) FF*q*PLL (d) Small-signal model of FFqPLL

frequency tracking is not as fast as phase tracking with lead compensators. The decoupled double synchronous reference frame (DDSRF) PLL [21] is developed to eliminate the double frequency error due to unbalance voltage conditions. This technique is capable of tracking the frequency variations however; it requires some improvement under harmonic conditions.

An Adaptive Notch Filter (ANF) has been proposed for the frequency estimation of single phase power systems [22]. The ANF concept extended to the three-phase power system [23] consists of three parallel adaptive sub filters and a frequency update loop. A sub filter is provided in each phase and the output information of all sub filters are used to estimate the frequency. The simple low-pass filters used to smoothen the estimated frequency increases the transient time of the system. The addition of band pass filter removes the high frequency noise and harmonics but introduces a delay into the system. A modified PLL structure [24] incorporating a feed forward action with a feedback controller is proposed to improve the dynamic performance and reduce the phase-angle estimation error to zero.

Some attempts have been made to improve PLL performance by introducing a feed forward action in PLL. The All Digital Phase Locked Loop (ADPLL) [25] proposed for improving the tracking speed, reduced output jittering and extended lock in range by changing the center frequency. A modified classical qPLL closed loop structure incorporating a feed forward loop action was presented in [26]-[27]. The qPLL is extended with a feed forward loop (FFqPLL) to increase the fast and accurate phase and frequency deduction under unbalanced utility conditions.

Recently, a feed forward PLL (FPLL) [28] is proposed to accurately track the phase and frequency of the input signal under wide frequency variations. In this dual loop PLL, feed forward action reduces the frequency error while the feedback loop takes care of the phase error. However, the moving average filter used to improve the filtering characteristics is designed for a centre frequency. Under large frequency deviations, this deteriorates the performance of the PLL. Hence, it is necessary to have an adaptive filter which filters out the ripples even under wide frequency deviations. Golestan.S et al [29]-[30] proposed a single loop type-3 PLL to track frequency ramp input with zero steady state phase error by changing the loop filter of a conventional Type-2 PLL.

This paper analyses the performance of single loop and dual loop Type-3 PLL under wide variation in input voltage. From the analysis presented in section III, it is observed that the effect of variation in input voltage (even for 80% voltage sag) on the performance of dual loop Type-3 PLL is less and its stability is independent of voltage. This paper also presents an adaptive dual loop PLL which is an extension of [28] and employs a frequency adaptive FIR filter to reduce the ripple in the estimated frequency.

II. SMALL SIGNAL MODELING

In this section, the small signal modelling of the Type-3 PLL with dual loop PLL and single loop [29]-[30] are briefly presented. Based on the models, the effect of input voltage variation on the performance of system and its stability is studied.

A. Dual loop PLL

To study the effect of feed forward loop, two dual loop Type - 3 PLL are considered.

a. *FPLL*

Fig. 1(a) illustrates the block diagram of FPLL, which includes a conventional SRF PLL and a feed forward loop. *LF(s)* represents the loop filter transfer function, ω_{ff} is the feed forward frequency, $\Delta\omega$ is the change in frequency in rad/s and ω^* is the estimated frequency. The small signal model of dual loop PLL is obtained as shown in Fig. 1(b), where *V* is the input voltage amplitude, LPF(s) is a first order low pass filter ($\mathrm{LPF(s)} = \omega_p/(s+\omega_p)$), $D(s)$ is the disturbance in the input signal, $\theta(s)$, $\theta^*(s)$ and $\theta_e(s)$ are the input angle, estimated angle and phase angle error respectively. The loop filter of the dual loop PLL is

$$\mathrm{LF(s)} = \frac{K_P\omega_p s + K_I\omega_p}{s(s+\omega_p)} \tag{1}$$

The open loop transfer function of the FPLL is expressed as

$$G_{ol}(s) = \frac{\theta^*(s)}{\theta(s)} = \left(\frac{\omega_p s^2 + K_p V\omega_p s + K_i V\omega_p}{s^3}\right) \tag{2}$$

The feed forward frequency of the FPLL is

$\omega_{ff}(s) = \mathrm{LPF}_2(s)\ \omega(s)$

where

$$\omega(s) = L\left(\frac{d\left\{\tan^{-1}(V_\beta(t)/V_\alpha(t))\right\}}{dt}\right) \tag{3}$$

The FPLL structure shown in Fig.1 is proposed to improve the dynamic response of the system under wide frequency deviations. The ω_{ff} is updated in addition to the change in $\Delta\omega$ and the frequency error is eliminated quickly. The PI controller reduces the phase error and hence there is a significant reduction in the tracking time.

b. *FFqPLL*

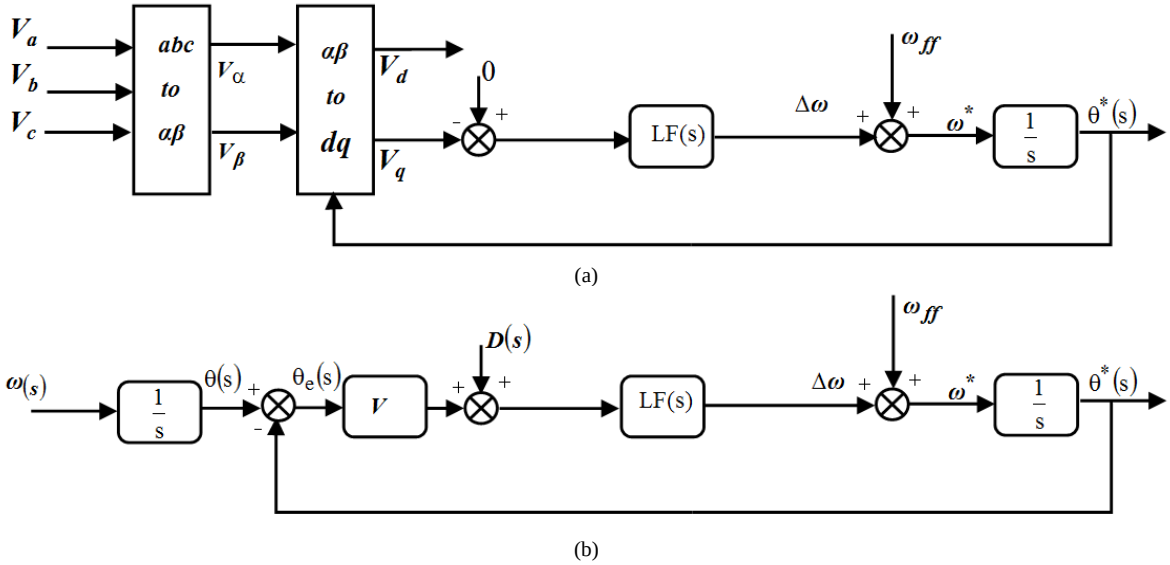
Fig. 1(c) illustrates the basic scheme of the feed forward *q*PLL (FF*q*PLL) which consist of a quadrature PLL (qPLL) and a feed forward loop. The small signal model of FFqPLL is shown in Fig. 1(d). The open loop transfer function of FF*q*PLL is

$$G_{ol}(s) = \frac{\hat{\theta}(s) - \theta_n(s)}{\theta_e(s)} = \frac{\omega_p s^2 + K_p V\omega_p s + K_i V\omega_p}{s^3} \tag{4}$$

From (2) and (4), it is clear that in both the dual loop Type-3 PLL, the open loop transfer function is same and the voltage amplitude (V) does not appear as a pure gain in the open loop transfer function.

B. Single loop PLL

Fig. 2(a) illustrates the block diagram of single loop PLL, in which LF(s) is the loop filter transfer function, ω_{ff} is a feed forward frequency, $\Delta\omega$ is the change in frequency in rad/s and ω^* is the estimated frequency. The small signal model of single loop PLL is obtained as shown in Fig. 2(b), where *V* is



(a)

(b)

Fig. 2. Single loop Type-3 PLL (a) Block diagram of single loop PLL (b) Small-signal model of single loop PLL

the input volage amplitude, D(s) is the disturbance in the input signal, $\theta(s)$,$\theta^*(s)$ and $\theta_e(s)$ are the input angle , estimated angle and phase angle error respectively.

The loop filter of single loop Type-3 PLL [30] is considered as

$$LF(s) = \frac{c_{n2}s^2 + c_{n1}s + c_{n0}}{s^2} \quad (5)$$

Where c_{n0} , c_{n1} and c_{n2} are non-zero positive constants.

The open loop transfer function of the system is given by

$$G_{ol}(s) = V\left(\frac{c_{n2}s^2 + c_{n1}s + c_{n0}}{s^3}\right) \quad (6)$$

It is clear from (6) that voltage amplitude (V) appears as a gain in the open loop transfer function of single loop PLL. Further, as the centre frequency is fixed, whenever there is a variation in supply frequency, the loop filter provides a correction around the nominal frequency and the response time increases. However, in dual loop PLL, the feed forward frequency is a function of supply frequency and therefore under frequency deviations, the frequency error is eliminated and tracking of input signal is faster.

III. Performance Analysis Of Single Loop And Dual Loop Type-3 PLL

The performance of the single loop and dual loop Type-3 PLL are analyzed under balanced and distorted conditions and the results are presented in this section.

A. *Under balanced and undistorted utility*

Under balanced and undistorted utility conditions, the input voltage *V*=1.p.u. and the distortion in the input signal is D(s) =0. From the open loop transfer function given by (2) and (6), the characteristic polynomial of the single loop and dual loop Type-3 PLL are obtained as

$$s^3 + Vc_{n2}s^2 + Vc_{n1}s + Vc_{n0} = 0 \quad (7)$$

and

$$s^3 + \omega_p s^2 + VK_P\omega_p s + VK_I\omega_p = 0 \quad (8)$$

For $c_{n2} = \omega_p/V$, $c_{n1} = K_P\omega_p$ and $c_{n0} = K_I\omega_p$ the single loop PLL and dual loop Type-3 PLL have the same closed loop transfer function (Table-I) and this results in the same dynamics.

The coefficients of loop filter (c_{n0}= $K_I\omega_p$=187277.5, c_{n1}=$K_P\omega_p$=8511.5, c_{n2}=ω_p=96.7) are selected by assuming the input voltage as 1.p.u. and both PLL have same bandwidth. Only under these conditions the single loop and dual loop Type-3 PLL have the same closed loop response. However, the coefficients of loop filter depend on the input voltage amplitude which affects the system performance and the same is presented in the next section.

B. *Effect of voltage magnitude on stability*

The stability of the system is verified by varying the input voltage from 0 to 1 p.u. When the input voltage is less than 0.23 p.u., the single loop PLL becomes unstable according to the Routh-Hurwitz stability criteria. In case of dual loop Type-3 PLL, for input voltage 0 to 1 p.u. the system is always stable. This is verified by applying Routh-Hurwitz stability criteria to the characteristic polynomial equation of dual loop Type-3 PLL (8) which yields the stability conditions as

$$\left.\begin{array}{l}\omega_p > 0\\ K_I > 0\\ V > 0\\ \tau_i > \tau_f\end{array}\right\} \quad (9)$$

The stability of the single loop and dual loop Type-3 PLL can also be verified by plotting the root locus as shown in Fig 3. Any change in the input voltage amplitude affects the loop gain and zeros of both the PLLs transfer function. When the input voltage is less than 0.23 p.u., then the closed loop poles of single loop Type-3 PLL shift to right side of the S-plane which makes the system unstable and the same is shown in root locus plot in Fig. 3. However, in case of dual loop Type-3 PLL, the voltage variation does not affect the system stability as shown in Fig.3.

TABLE-I
CLOSED LOOP TRANSFER FUNCTION FOR SINGLE LOOP AND DUAL LOOP TYPE-3 PLL

Input voltage V p.u.	single loop Type-3 PLL	dual loop Type-3 PLL
In terms of 'V'	$G_{SRF}(s)=\frac{Vc_{n2}s^2+Vc_{n1}s+Vc_{n0}}{s^3+Vc_{n2}s^2+Vc_{n1}s+Vc_{n0}}$	$G_{FPLL}(s)=\frac{\omega_p s^2+VK_P\omega_p s+VK_I\omega_p}{s^3+\omega_p s^2+VK_P\omega_p s+VK_I\omega_p}$
For V=1.p.u.	$G_{SRF}(s)=\frac{\omega_p s^2+K_P\omega_p s+K_I\omega_p}{s^3+\omega_p s^2+K_P\omega_p s+K_I\omega_p}$	$G_{FPLL}(s)=\frac{\omega_p s^2+K_P\omega_p s+K_I\omega_p}{s^3+\omega_p s^2+K_P\omega_p s+K_I\omega_p}$

TABLE-II
STABILITY ANALYSIS OF SINGLE LOOP AND DUAL LOOP TYPE-3 PLL

Voltage (p.u.)	*a*		$\xi\ \omega_n$		ω_c	
	Type-3 SRF PLL	FPLL	Type-3 SRF PLL	FPLL	Type-3 SRF PLL	FPLL
1	28.51	28.51	34.03	34.03	166	166
0.8	27.55	31.50	24.33	32.40	145	154
0.6	26.29	39.44	14.37	28.28	121	140
0.4	24.50	61.02	4.97	17.51	95	126
0.2	21.43	81.44	-4.18	7.50	65	111

TABLE- III
PERFORMANCE COMPARISON OF PLLS

Type of PLL	Balance performance	Unbalance performance	Harmonics THD (%)	Harmonics performance	Harmonics THD (%)	Voltage sag performance	Stability
Single loop Type-3 PLL	Good	Poor	16.67	Poor	16.31	Poor	Unstable
Single loop Type-3 PLL with AMA	Good	Poor	16.67	Poor	16.31	Poor	Stable
Dual loop Type-3 PLL	Good	Good	4.59	Good	4.50	Good	Stable

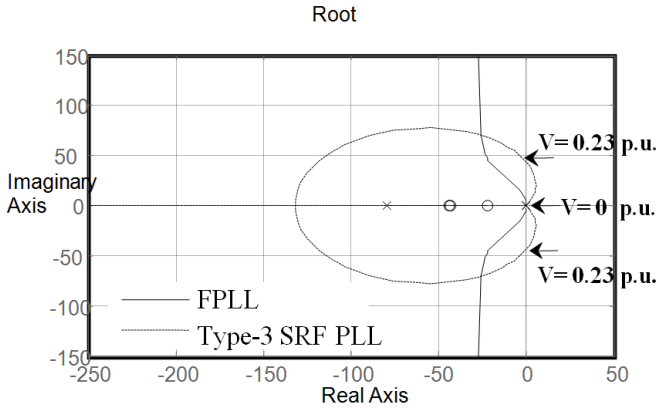


Fig. 3 Root locus of single loop and dual loop Type-3 PLL with the amplitude V as a variable parameter

C. *Effect of voltage sag on system performance*

From the small signal model of single loop and dual loop Type-3 PLL, the error transfer function (i.e. $\theta_e(s)/\theta s)/$) are written as

$$G_e(s)_{Type-3SRF}=\frac{\theta_e(s)}{\theta(s)}=\frac{s^3}{s^3+Vc_{n2}s^2+Vc_{n1}s+Vc_{n0}}\theta(s) \quad (10)$$

$$G_e(s)_{FPLL}=\frac{\theta_e(s)}{\theta(s)}=\frac{s^3}{s^3+c_{n2}s^2+Vc_{n1}s+Vc_{n0}}\theta(s) \quad (11)$$

The denominator polynomial of single loop and dual loop Type-3 PLL are compared with third order under damped system in (12)

$$(s+a)\left(s^2+2\xi\xi_n s+\omega_n^2\right)=0 \quad (12)$$

where

ξ -damping ratio and ω_n - natural frequency of oscillation.

The roots of the third order under-damped system are determined by PLL parameters and are expressed in (13) and (14)

$$a^3-a^2Vcn_2+aVcn_1-Vcn_0=0 \text{ (Single loop Type-3 PLL)} \quad (13)$$

$$a^3-a^2cn_2+aVcn_1-Vcn_0=0 \text{ (dual loop Type-3 PLL)} \quad (14)$$

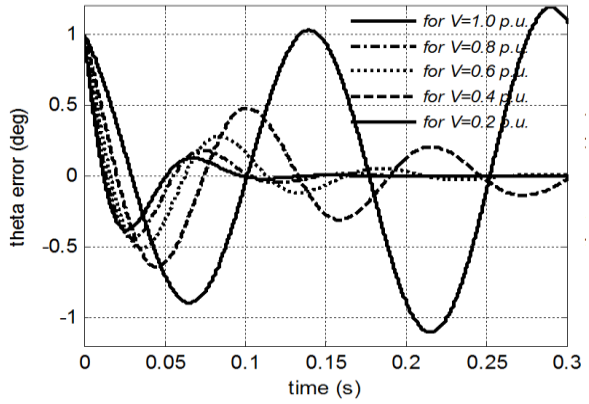
By solving (13) and (14), taking real positive real root to determine the value of natural frequency of oscillation (ω_n).

$$\omega_{n\ SingleloopType-3PLL}=\sqrt{\frac{Vcn_0}{a}} \quad (15)$$

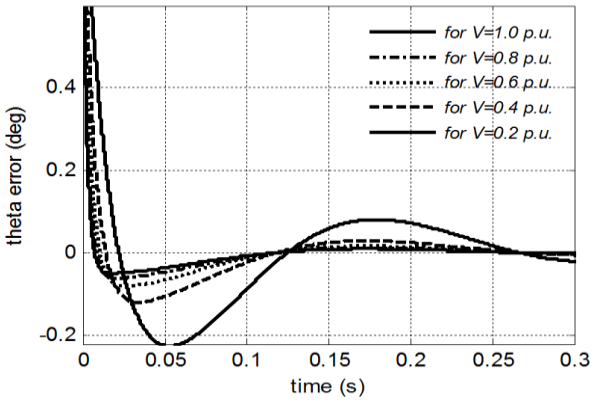
$$\omega'_{n\ DualloopType-3PLL}=\sqrt{\frac{Vcn_0}{a}} \quad (16)$$

The damping ratio (ξ) of single loop and dual loop Type-3 PLL are determined by

$$\xi_{SingleloopType-3PLL}=\frac{Vcn_2-a}{2\omega_n} \quad (17)$$



(a)



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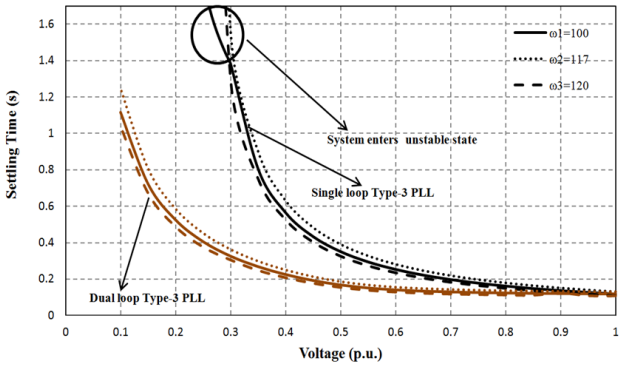


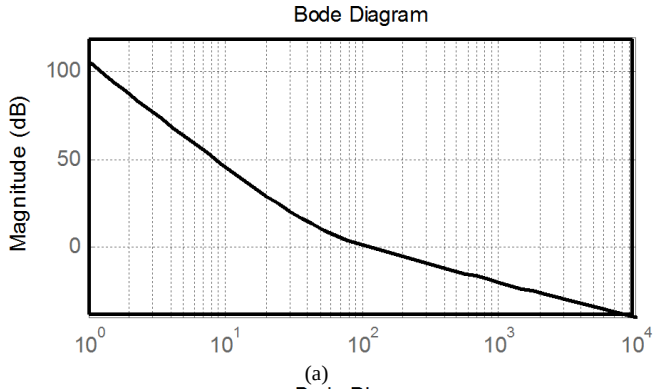
(c)

Fig . 4 Phase error of system with the amplitude V as a variable parameter (a) single loop Type-3 PLL, (b) dual loop Type-3 PLL.(c) Settling time

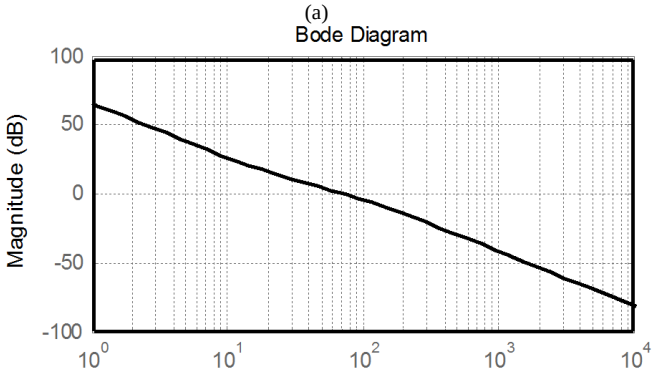
$$\xi'_{\text{DualloopType-3PLL}} = \frac{cn_2 - a}{2\omega_n} \tag{18}$$

$$\theta_e(t) = K_1 e^{-at} + K_2 e^{-\zeta\omega_n t}\cos(\omega_d + \theta) \tag{19}$$

The equation (19) shows that, the error in theta depends on the magnitude of real pole (a) and real term of complex pole ($\xi\omega_n$). In single loop Type-3 PLL, the decrease in input voltage reduces the magnitude of 'a' and $\xi\omega_n$ (Table-II) which in turn affects the transient performance of the system and it is shown in Fig. 4(a). In dual loop Type-3 PLL, the decrease in input voltage increases the magnitude of '*a*' and decreases the magnitude of $\xi\omega_n$. This increase in real pole magnitude ('*a*') reduces the effect of transient response of the system under variation in input voltage as shown in Fig. 4(b). Fig. 4(c) shows the settling time of PLLs with different bandwidth (ω),



(a)



(b)

Fig. 5.Magnitude bode plot of disturbance transfer function (a) single loop Type-3 PLL (b) dual loop Type-3 PLL

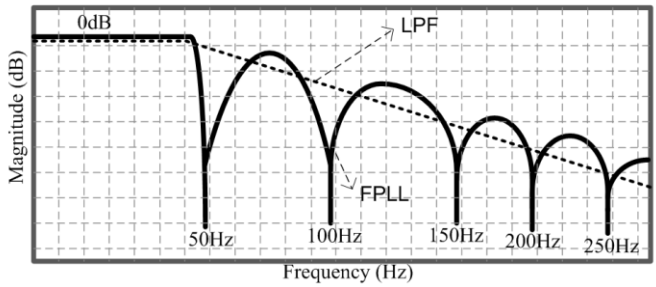


Fig. 6. Frequency characteristic of FIR Filter

in which the settling time of single loop Type-3 PLL increases gradually upto 0.5p.u. for reductions in voltage and above 0.5p.u. the settling time increases rapidly and becomes unstable at 0.23p.u. In dual loop Type-3 PLL, the settling time increases gradually and remains stable. The performance analysis of PLLs under various conditions such as voltage sag, unbalance and harmonics shows that dual loop Type 3 PLL works satisfactorily under distorted conditions as shown in Table III.

D. Filtering characteristics

In the earlier analysis (section II), the FIR filter is considered as a first order low pass filter to verify the stability of the single loop and dual loop Type-3 PLL. In this section, the filtering characteristics of FIR Filter are analyzed under distorted supply conditions. Usually in any power system, the system voltage consists of harmonics in the order of multiples of fundamental frequency. If phase voltages are unbalanced, then a double frequency oscillation appears in *d-q* axes variables. A low pass filter meets the specification but it has

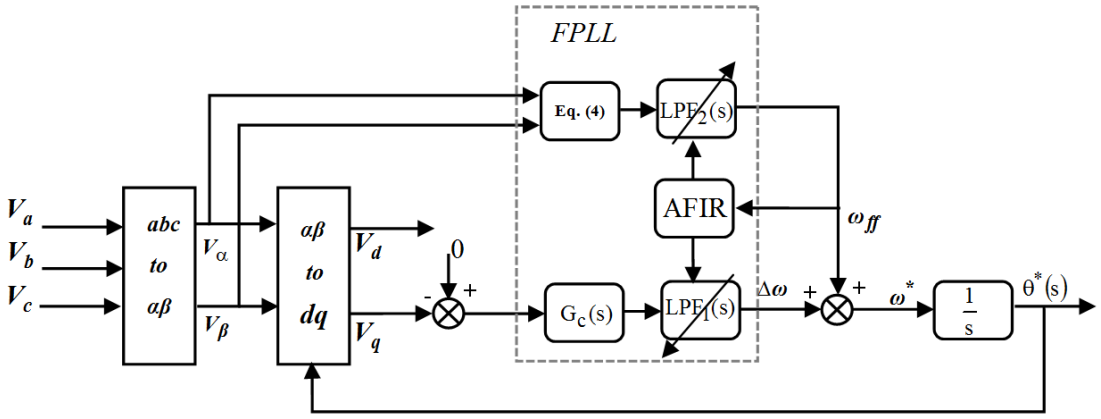


Fig. 7. Dual loop Type-3 PLL with Adaptive FIR Filter

low attenuation under 2nd, 3rd, 5th and 7th harmonics components and this ripples result in erroneous estimation of 'θ'. Hence a filter which provides high attenuation to 2nd, 3rd, 5th and 7th harmonics components is required. A linear phase low pass FIR filter is designed to have a high attenuation under desired frequency and the phase response is a linear function of the desired frequency and thus the FIR is free from phase or delay distortion [31]. Fig.5(a) shows the bode plot of $\theta(s)/d(s)$ of single loop Type-3 PLL for phase of 133° at zero frequency with a slope of -20 dB / dec whereas the open loop bode plot of dual loop Type-3 PLL with FIR shows that (Fig. 5(b)) it has a phase of 144° at zero frequency with slope of -40dB/dec. Therefore, the diminution of dB/dec in single loop Type-3 PLL reduces the attenuation factor. This indicates that dual loop Type-3 PLL has high attenuation factor which improves the accuracy in 'θ'estimation even though the supply is distorted.

E. A frequency adaptive dual loop Type-3 PLL

In the FPLL[28], a Moving Average Filter (MAF) is used to remove the multiple frequency ripples caused by supply disturbances. A MAF is a linear-phase finite-impulse-response filter and has the advantages of easy implementation and low computational burden. The MAF completely eliminates any ripple which is a multiple of the frequency for which it is designed and thus the double frequency ripple and the harmonics which are multiple of supply frequency are easily cancelled out. The major problem with MAF is that they exhibit frequency dependent attenuation characteristics. When the supply frequency changes the ripple due to disturbances also changes. In such cases, the MAF cannot completely block the disturbance components and PLL shows poor performance. Hence it is necessary to design a frequency adaptive MAF to improve the filtering characteristics. Fig. 6 shows the frequency characteristic of FIR filter in which the filter provides high attenuation at fundamental frequency (50Hz) and also at multiples of fundamental frequency [31]. The notch frequency 50Hz is considered to avoid the possibility of DC components. However, when the frequency deviates from the nominal value, ripples appear in the estimated frequency, as the centre frequency of the FIR filter is fixed. In order to overcome this problem, an adaptive FIR filter which updates its parameters for change in supply frequency is required.

Fig. 7 shows the block diagram of dual loop Type-3 PLL with frequency adaptive FIR filter. The MAF can be made adaptive by adjusting PLL sampling frequency with respect to supply frequency, by changing the order of filter according to the grid frequency variations or by using a look up table. In the present work, a lookup table is used to change the coefficient of the FIR filter. The coefficients for input supply frequency range of 20Hz to 60Hz are loaded in a look up table. The range of frequency is divided into 14 bands with a bandwidth of 3Hz. Lowering the bandwidth may increase the accuracy of adaptive filter but increases the computational burden. Hence a bandwidth of 3 Hz with reasonable accuracy is chosen. For every change of 3Hz, the coefficients of Adaptive filter will update from the lookup table. For instance, if the supply frequency is in the band of 48-50 Hz, the coefficient of FIR Filter is changed to K1. Similarly, for the frequency band of 51-53 Hz, the coefficient is updated to K2. Hence, the adaptive MAF filter updates the coefficient of filter automatically based on supply frequency which enables to filter out the ripples under distorted conditions.

IV. Result and Discussions

The performance of the frequency adaptive dual loop Type-3 PLL is evaluated by means of simulations using Matlab/Simulink and is also implemented in ALTERA cyclone II FPGA controller for a 3 phase, 415V, 50Hz utility. In the experiment, the unbalance in voltage, harmonics and voltage sag are incorporated using a programmable AC voltage source. LEM sensors are used to measure the grid voltage and current. The performances of the PLLs are evaluated under balanced grid condition and for variations in the input voltage and frequency. To show the dynamic performance of dual loop PLL under voltage sag conditions, the results of the dual loop PLL are compared with single loop PLL. Further, to validate the performance of the frequency adaptive filter under frequency deviations, the performance of dual loop PLL with and without filter is studied and the simulation and experimental results are presented.

A. Under balanced and undistorted utility

As seen from Table-I, the closed loop transfer function of both single loop and dual loop Type-3 PLL are identical for V=1p.u.. Under balanced and undistroted utility conditions, the performance of the both single loop and dual loop Type-3

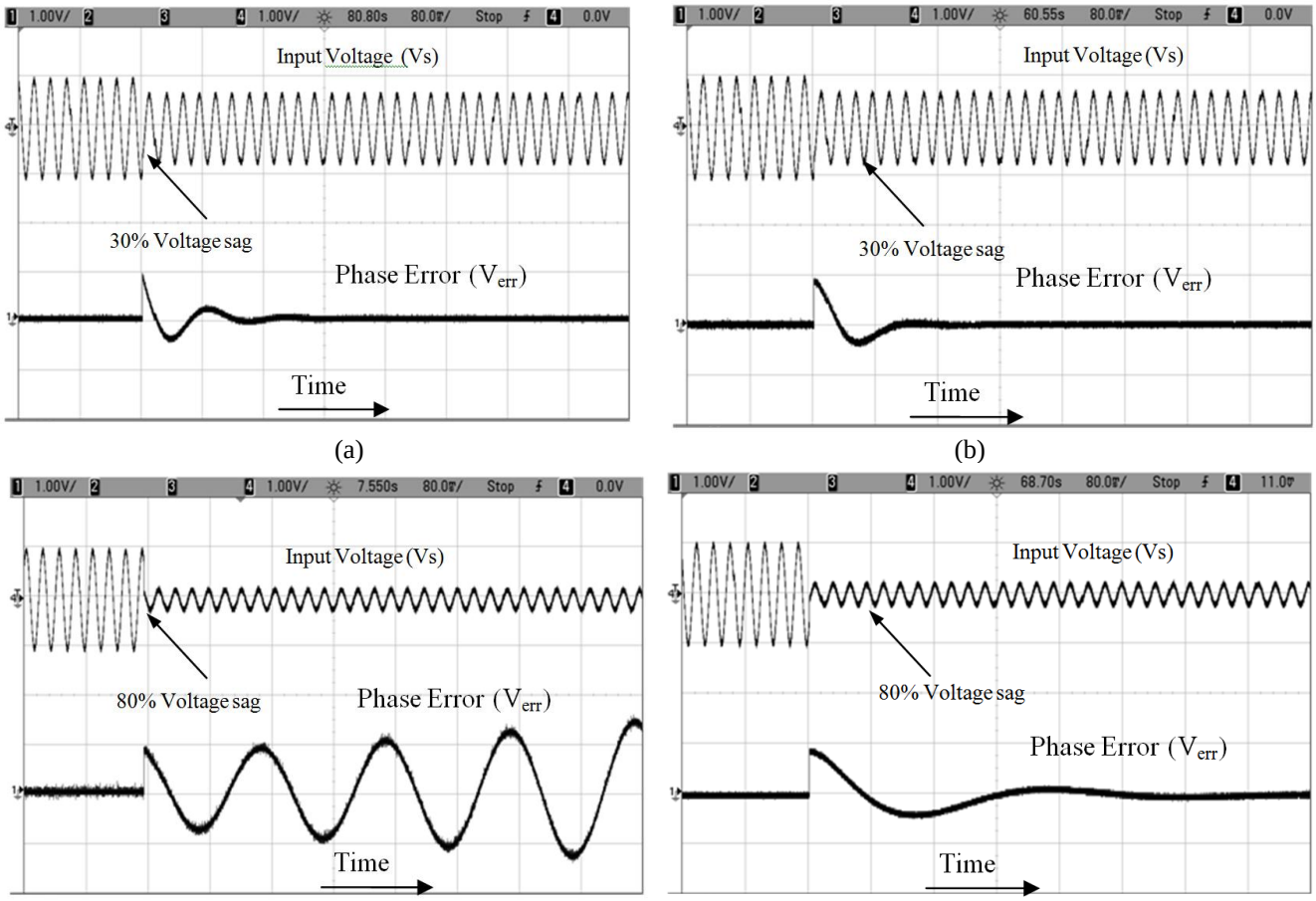


Fig. 8. Settling time of single loop and dual loop Type-3 PLL, (a)Settling time of single loop Type-3 PLL at 30% of voltage sag(Vs-1V/div, V_{err}-1V/div), (b)Settling time of dual loop Type-3 PLL at 30% of voltage sag(Vs-1V/div, V_{err}-1V/div), (c)Settling time of single loop Type-3 PLL at 80% of voltage sag(Vs-1V/div, V_{err}-1V/div), (d)Settling time of dual loop Type-3 PLL at 80% of voltage sag (Vs-1V/div, V_{err}-1V/div). time: 0.06 s/div

PLL is same and both have good quality output signals.

B. Effect of voltage variation

The behavior of the single loop and dual loop Type-3 PLL under wide input voltage variation is examined. Intially the system is in balanced condition and the phase error is zero in both thecases. When a voltage sag of 30% is created at t=1.11 seconds as shown in Fig.8(a), the phase error in the single loop Type-3 PLL takes eleven seconds to settle, where as in dual loop Type-3 PLL the loop filter provides high attenuation factor which reduces the phase error and settles within six seconds as shown in 8(b). When a voltage sag of 80% is applied with the single loop Type-3 PLL, the system enters into unstable region (Fig. 8(c)). In dual loop Type-3 PLL, the phase error is reduces to zero within 20 seconds (Fig. 8(d)) and system remains stable.

C. Dual loop Type-3 PLL with Frequency Adaptive Filter.

With an unbalanced utility voltage, the variation in input frequency varies the frequency of ripple content in the synchronous rotating reference frame. To eliminate this frequency ripple, a frequency adaptive filter is used in dual loop Type-3 PLL which updates the filter cutoff frequency with respect to the change in utility frequency. Fig. 9 shows the steady state response of the dual loop Type-3 PLL with and without adaptive FIR Filter under frequency deviations. The frequency variation and unbalance in voltage is achieved with a help of a programmable ac source. To study the performance of the Adaptive FPLL for ramp change in frequency under distorted conditions, a voltage sag of 20% is created in 'a' phase at t = 0.16 s and a ramp change in frequency from 50 Hz to 40 Hz is applied at t = 0.18 s (shown in Fig. 9 a). Fig.9(b) shows the response of the adaptive FPLL for a signal polluted with harmonics (5^{th} and 7^{th} harmonics are added to the source) and subjected to ramp change in frequency. Under this condition, the PLL is able to track the phase and frequency of the input signal in 2 cycles. Fig. 9.c shows that, initially the utility voltage is unbalanced with 50Hz. At t=0.2s the frequency is changed from 50Hz to 40Hz. This change in frequency creates double frequency oscillations(80 Hz) in the Vq components of dual loop Type-3 PLL. As seen from Fig.9(c), the steady state error Vq reduces drastically when an adaptive FIR filter is used. Similarly, the system is verified for ramp change in frequency from 50Hz to 60Hz. As observed from Fig. 9(d), the change in supply frequency changes the ripple frequency to 120 Hz and filter designed to filter out 100 Hz cannot satisfactorily remove the distortions in Vq component. As the filtering characteristics of adaptive FIR filter changes with supply frequency, the 120 Hz

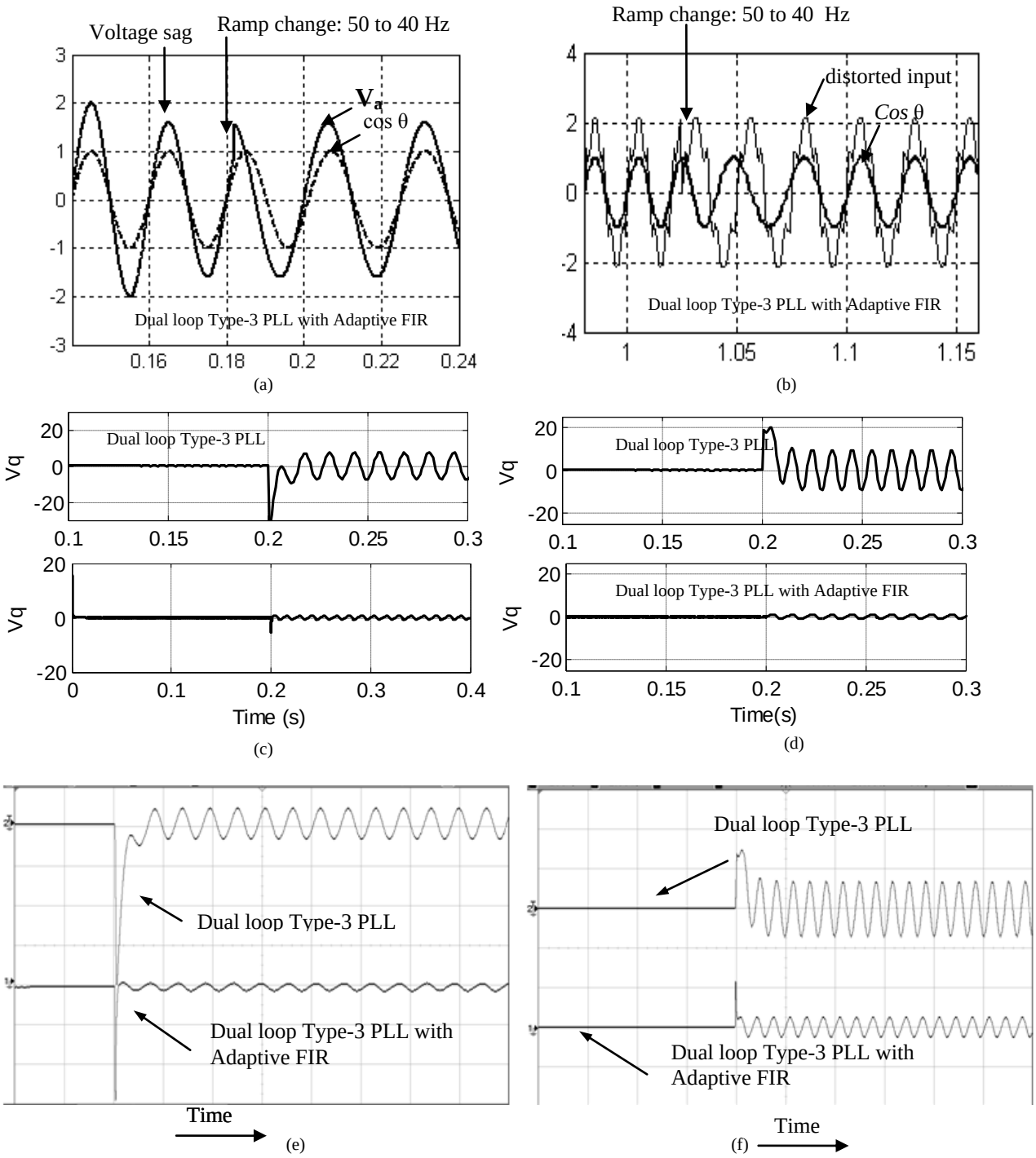


Fig. 9. Double frequency content with a ramp change in frequency (a) response during voltage sag in 'a' phase (b) response during distorted input signal(c) response during decrease in frequency from 50Hz to 40Hz (Simulation) (d) response during increase in frequency from 50Hz to 60Hz (simulation) (e) response during decrease in frequency from 50Hz to 40Hz (Experimental-without Adaptive FIR- Vq-2V/div, with Adaptive FIR- Vq-0.2V/div,)time-0.02s) (f) response during increase in frequency from 50Hz to 60Hz (Experimental- without Adaptive FIR- Vq-2V/div, with Adaptive FIR- Vq-0.2V/div,)time-0.02s)

ripple is eliminated in the Vq component. The same is verified through experimentation and similar response is observed as shown in Fig 9(e) and 9(f).

V. Conclusion

This paper analyses the performance of the single loop and dual loop Type-3 PLL for variations in input voltage and frequency. It is observed from the analysis that Type-3 PLL with secondary loop improves the dynamic response and also increases the stability region under large voltage sag. Further, the loop filter provides a high attenuation to harmonics and yields good filtering characteristics under distorted conditions. To improve the performance of dual loop Type-3 PLL under wide frequency deviations, a frequency adaptive filter is used. It is also validated through simulation and experimental results that, the introduction of frequency adaptive filter in the dual

loop Type-3 PLL, reduces the ripples in the estimated frequency. Thus the developed frequency adaptive feed forward PLL can be preferred in applications where the voltage and frequency variation are significant.

REFERENCES

[1] Blaabjerg, F. ; Ma, K.; , "Future on Power Electronics for Wind Turbine Systems", Emerging and Selected Topics in Power Electronics, IEEE Journal of, vol.1, no.3, pp. 139-152, Sep. 2013

[2] Qing-Chang Zhong; Phi-Long Nguyen; Zhenyu Ma; Wanxing Sheng, "Self-Synchronized Synchronverters: Inverters Without a Dedicated Synchronization Unit," *IEEE Transactions on Power Electronics*, , vol.29, no.2, pp.617-630, Feb. 2014

[3] Hudgins, J.L.; , "Power Electronic Devices in the Future", *Emerging and Selected Topics in Power Electronics, IEEE Journal of*, vol.1, no.1, pp. 11-17, Mar. 2013

[4] Serban, I.; Marinescu, C., "Control Strategy of Three-Phase Battery Energy Storage Systems for Frequency Support in Microgrids and with Uninterrupted Supply of Local Loads," *IEEE Transactions on Power Electronics*, , vol.29, no.9, pp.5010-5020, Sept. 2014

[5] Zheng Zeng; Huan Yang; Shengqing Tang; Rongxiang Zhao,"Objective-Oriented Power Quality Compensation of Multifunctional Grid-Tied Inverters and Its Application in Microgrids," *IEEE Transactions on Power Electronics*, vol.30, no.3, pp.1255-1265, March 2015

[6] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and E. Acha. "A generic open loop algorithm for three phase grid voltage/current synchronization with particular reference to phase, frequency and amplitude estimation" *IEEE Transactions on Power Electronics*. vol.24, no.1, pp. 94-107, Feb. 2009

[7] Eider Robles, Salvador Ceballos, Josep Pou, Jose Luis Martin, Jordi Zaragoza, and Pedro Iba˜nez. "Variable-Frequency Grid-Sequence Detector Based on a Quasi-Ideal Low-Pass Filter Stage and a Phase-Locked Loop" *IEEE Transactions on Power Electronics*.,vol.25, no10, pp2552-63, May. 2010.

[8] Masoud Karimi-Ghartemani, S. Ali Khajehoddin, Praveen K. Jain, and Alireza Bakhshai, "Problems of Startup and Phase Jumps in PLL Systems", *IEEE Transactions on Power Electronics*, vol.27, no4, pp1830-38,Feb. 2012.

[9] Kulkarni, A.; John, V., "Analysis of Bandwidth–Unit-Vector-Distortion Tradeoff in PLL During Abnormal Grid Conditions,"IEEE *Transactions on Industrial Electronics.*,vol.60, no.12, pp.5820,5829, Dec. 2013.

[10] Masoud Karimi-Ghartemani, S. Ali Khajehoddin, Praveen K. Jain, Alireza Bakhshai, and Mohsen Mojiri. "Addressing DC Component in PLL and Notch Filter Algorithms", *IEEE Transactions on Power Electronics*.,vol.27, no1, pp78-86., Jan 2012.

[11] Ghoshal, Anirban and John, Vinod " A Method to Improve PLL Performance Under Abnormal Grid Conditions" In: *National Power Electronics Conference 2007*, 17-19 Dec. 2007, Indian Institute of Science , Bangalore.

[12] F. D. Freijedo, J. Doval-Gandoy, O. Lopez, and C. Jacobo "Robust phase locked loops optimized for DSP implementation in power quality applications", *34th Annual Conference of IEEE Ind. Electron*., pp.3052-3057, IECON 2008.

[13] Rakesh Kumar Sinha, Parthasarathi Sensarma "A pre-filter based PLL for three-phase grid connected applications*", Electric Power Systems Research*, vol.81. pp129-37, Jan. 2011.

[14] Yang Han, Lin Xu, M. M. Khan "A novel synchronization scheme for grid-connected converters by using adaptive linear optimal filter based PLL (ALOF-PLL)", *Simulation Modelling Practice and Theory*, vol.17, no. 7, pp. 1299-1345, Aug. 2009.

[15] Baoquan Liu; Fang Zhuo; Yixin Zhu; Hao Yi; Feng Wang, "A Three-Phase PLL Algorithm Based on Signal Reforming Under Distorted Grid Conditions," *IEEE Transactions on Power Electronics*, vol.30, no.9, pp.5272-5283, Sept. 2015.

[16] Golestan, S.; Ramezani, M.; Guerrero, J.M.; Freijedo, F.D.; Monfared, M., "Moving Average Filter Based Phase-Locked Loops: Performance Analysis and Design Guidelines," *IEEE Transactions on Power Electronics*, vol.29, no.6, pp.2750-2763, June 2014

[17] Jinyu Wang; Jun Liang; Feng Gao; Li Zhang; Zhuodi Wang, "A Method to Improve the Dynamic Performance of Moving Average Filter-Based PLL," *IEEE Transactions on Power Electronics* , vol.30, no.10, pp.5978-5990, Oct. 2015

[18] Golestan, S.; Ramezani, M.; Guerrero, J.M.; Monfared, M., "dq-Frame Cascaded Delayed Signal Cancellation- Based PLL: Analysis, Design, and Comparison With Moving Average Filter-Based PLL," *IEEE Transactions on Power Electronics*, vol.30, no.3, pp.1618-1632, March 2015

[19] Han, Y.; Luo, M.; Zhao, X.; Guerrero, J.; Xu, L., "Comparative Performance Evaluation of Orthogonal-Signal-Generators based Single-Phase PLL Algorithms," , IEEE Transactions on Power Electronics, vol.PP, no.99, pp.1-1 (Early Access Article)

[20] Francisco D. Freijedo, Alejandro G. Yepes, Oscar Lopez, Ana Vidal, and Jesus Doval-Gandoy "Three-Phase PLLs with fast postfault retracking and steady-state rejection of voltage unbalance and harmonics by means of lead compensation", *IEEE Transactions on Power Electronics*.,vol.26, no.1, pp.85-97, Jan. 2011.

[21] P. Rodriguez, J. Bergas, J.I. Candela, R.P.Burgos and D.Boroyeich "Decoupled Double Synchronous Reference Frame PLL for Power Converters Control *IEEE Transactions on Power Electronics*.,vol.22, no.2, pp.584-92, Mar. 2007.

[22] M. Mojiri, M. Karimi-Ghartemani, and A. R. Bakhshai, "Estimation of power system frequency using an adaptive notch filter," *IEEE Trans. Instrum. Meas.*, vol. 50, no. 6, pp. 2470–2477, Dec. 2007.

[23] Mohsen Mojiri, Davood Yazdani, and Alireza Bakhshai "Robust Adaptive Frequency Estimation of Three-Phase Power Systems", *IEEE Trans. Instrum. Meas.*, vol.59,no.7,pp.1793-1802, Jun. 2010.

[24] Yazdani, M. Mojiri, A. Bakhshai, and G. Joos "A fast and accurate synchronization technique for extraction of symmetrical components", *IEEE Transactions on Power Electronics*,vol.24, no.3, pp. 674–684, Apr. 2009.

[25] H. Geng, D. Xu, and B. Wu, "A Novel hardware based All Digital PhaseLocked-Loop applied to Grid-connected Power Converters," *IEEE Transactions on Industrial Electronics*, vol. 58, no. 5, pp. 1737-1745, May 2011.

[26] Liccardo, P. Marino, C. Schiano, and N. Visciano, "A new robust phase tracking system for asymmetrical and distorted three phase networks," *Proc. in 11th Int. Conf. Harmon. Quality Power*, Sep. 12–15,2004, pp. 525–530.

[27] Liccardo, P. Marino, and G. Raimondo, "Robust and fast three-phase PLL tracking system," *IEEE Transactions on Industrial Electronics*., vol. 58, no. 1, pp.221-231, Jan. 2011.

[28] B. Indu Rani, C.K. Aravind, G. Saravana Ilango, and C. Nagamani "A three phase PLL with a dynamic feed forward frequency estimator for synchronization of grid connected converters under wide frequency variations", *Int.J. of Elect. Power Energy Syst*., vol. 41, pp. 63-70 , Mar. 2012.

[29] Saeed Golestan, Mohammad Monfared, Franciso D. Freijedo and Joseph M Guerrero "Advantages and Challenges of Type-3 PLL", *IEEE Transactions on Power Electronics*,vol.28, no.11, pp.4985-4997, Nov. 2013.

[30] Golestan, S.; Ramezani, M. and Guerrero, J.M., "An Analysis of the PLLs With Secondary Control Path,"*IEEE Transactions on Industrial Electronics*, vol.61, no.9, pp.4824-4828, Sept. 2014.

[31] B. Indu Rani, G. Saravana Ilango, and C. Nagamani "A three phase reference current generator for power electronic converters under distorted utility conditions", *Int. Conf. Computing, Electronics and Electrical Technologies [ICCEET]*21-22 March 2012, pp.267-272.

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