ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

8-BIT 1 GS/S ADC ARCHITECTURE AND 4-BIT FLASH ADC FOR +10 GS/S TIME INTERLEAVED ADC IN 65nm CMOS TECHNOLOGY

M.Sc. THESIS

Alper AKDİKMEN

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

+10 GS/S ZAMAN ARALIKLI ADC İÇİN 65nm CMOS TEKNOLOJİSİNDE 8-BIT 1 GS/S ADC YAPISI VE 4-BIT FLASH ADC

YÜKSEK LİSANS TEZİ

Alper AKDİKMEN
(504121385)

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Programı

Tez Danışmanı: Prof. Dr. Müştak Erhan YALÇIN

EKİM 2015

Alper AKDİKMEN, a M.Sc. student of ITU Graduate School of Science Engineering and Technology 504121385, successfully defended the thesis entitled "8-BIT 1 GS/S ADC ARCHITECTURE AND 4-BIT FLASH ADC FOR +10 GS/S TIME INTERLEAVED ADC IN 65nm CMOS TECHNOLOGY", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Prof. Dr. Müştak Erhan YALÇIN** Istanbul Technical University	.....
Jury Members :	**Assist. Prof. Dr. Tufan Coşkun KARALAR** Istanbul Technical University	.....
	Prof. Dr. Günhan DÜNDAR Bogazici University	.....

Date of Submission: 8 October 2015
Date of Defense: 16 October 2015

To my family and friends,

FOREWORD

This thesis work was done on my Erasmus+ Program Exchange Student period in Integrated Microsystems Laboratory (IMS) of University of Pavia under the supervision of Prof. Dr. Franco MALOBERTI as a collaborated project with his PhD candidate Dante Gabriel MURATORE. I would like to thank my advisor Prof. Franco MALOBERTI for his invaluable support and inspiration. I'm thankful to Dante MURATORE for being such a nice colleague. I would like to thank the members of the Integrated Microsystems Laboratory in Pavia, especially to Edoardo BONIZZONI, for their invaluable support in a year's period.
I'm grateful to Prof. Müştak Erhan YALÇIN for accepting to be my supervisor in ITU. I am also grateful to the members of ITU VLSI Labs for their support especially for the first half of my master studies. Last but not least, I'm grateful to Prof. Türker KÜYEL for his great contribution to my involvement in this area.
I dedicate this work, like all my achievements in this life, to my parents İzzet AKDİKMEN and Kadriye AKDİKMEN.

October 2015

Alper AKDİKMEN
(Electronics Engineer)

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ABBREVIATIONS

ADC	**:** Analog to Digital Converter
DAC	**:** Digital to Analog Converter
DNL	**:** Differential Non-Linearity
ENOB	**:** Effective Number of Bits
Gbps	**:** Giga Bit per Second
GS/s	**:** Giga Sample per Second
INL	**:** Integral Non-Linearity
LSB	**:** Least Significant Bit
MSB	**:** Most Significant Bit
SAR	**:** Successive Approximation Register
SDR	**:** Software Defined Radio
SFDR	**:** Spurious Free Dynamic Range
SNR	**:** Signal to Noise Ratio

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8-BIT 1 GS/S ADC ARCHITECTURE AND 4-BIT FLASH ADC FOR 10+ GS/S TIME INTERLEAVED ADC IN 65nm CMOS TECHNOLOGY

SUMMARY

Data rate of communication systems constantly increasing . Rapid scaling of digital semiconductor technologies has moved the signal processing of these systems to digital domain. Therefore high-speed ADCs are required to form the bridge to take the analog signals in digital domain.

Data rates exceeding 10 Gbps makes the use of single channel ADCs unfeasible on this purpose. A power efficient solution is time-interleaving. Time-interleaving relaxes the speed requirements on single channel ADCs and lets designers to focus on power efficiency of the ADC.

Channel mismatches in time-interleaved ADCs causes performance degradation. Errors arise mainly due to offset, gain and timing mismatch of channels. Among them, timing error is the most problematic since estimation of timing errors becomes more cumbersome in high-frequencies.

Estimation and correction of timing errors in time-interleaved ADCs are hot topics of research. Calibration of errors can be on background or on foreground. Background calibration is more desirable since it allows system to adapt to changing conditions while not hindering the operation of the ADC.

Time interleaving errors generate spurs on the spectrum. Spurs are problematic for the wireless communication systems, since they may block the input signal. In order to extinguish the spurs a channel randomization technique is proposed. Technique is based on randomly taking one of the ADC channels to make the errors of the channels noise-like term. It is advantageous since it works on background. Technique maintains a spur-free spectrum however does not improve the SNR of the system.

Estimation of channel mismatch errors and clock distribution in a time-interleaved ADC becomes tedious as the number of channels increase. In order to keep the channel number low, channels should be fast while being power efficient. To satisfy this task, an 8-bit 1 GS/s multi-bit per cycle ADC is proposed. ADC employs a

novel search algorithm based on redundancy. No calibration scheme required thanks to the algorithm therefore the power efficiency of the system can be increased. In order to realize the multi-bit per cycle structure, a multiple-threshold generation preamp is proposed.

Comparators are the most important part of an ADC. Comparator specifications such as speed, accuracy and power consumption directly affect the relative specifications of the whole ADC. A novel latch with embedded preamp is proposed. Novel structure has latch regeneration time, offset, power consumption and kickback noise improvements over the conventional structures.

8-bit 1 GS/s multi-bit per cycle SAR ADC employs a flash ADC to perform the coarse conversion benefit from its speed. Although flash ADCs are fast, offset and kickback noise of comparators can penalize their accuracy. Proposed latch with embedded preamp improves the offset performance. To solve the kickback issue, reference voltages of the flash ADC are sampled. This technique is based on equalizing the kickback for both input and reference voltages therefore eliminating the effect.

Sampling network of the ADC is critically important since any error made in the sampling phase directly passes to the ADC. Bootstrapped switches are used to improve the linearity of the switches. By using bootstrap switches, charge injection can be made signal independent. If it is combined with the reference sampling technique used in flash ADC, effects of charge injection can be diminished significantly.

ADC blocks are designed and laid out in ST Microlectronics 65 nm process. Post-layout simulations have proven the efectiveness of the proposed techniques and blocks. Tape-out was done in July 2015. Measurements is expected to take place in November 2015.

10+ GS/S ZAMAN ARALIKLI ADC İÇİN 65nm CMOS TEKNOLOJİSİNDE 8-BIT 1 GS/S ADC YAPISI VE 4-BIT FLASH ADC

ÖZET

Haberleşme sistemlerinin veri aktarım sıklıkları ve bant genişlikleri sürekli olarak artmaktadır. Sayısal yarıiletken teknolojilerindeki gelişmeler, haberleşme sistemlerindeki işaret işleme kısımlarını sayısal domenine almıştır. Sayısal işaret işlemenin avantajları, ideal olmayan durumlara yüksek tolerans, gerçekleme kolaylığı, bir fonksiyonu gerçeklemek için gereken alanın dolayısıyla maliyetin düşük olması ve yeni teknolojilere taşınabilme olarak sayılabilir. Bu avantajlardan faydalanmak için analog işaretleri sayısal domene almada köprü görevi görecek yüksek hızlı analog-sayısal dönüştürücülere(ADC) ihtiyaç vardır.

Kablolu ve kablosuz haberleşme teknolojilerinde 10 GHz'yi de aşan bant genişlikleri tek kanallı ADCleri bu iş için elverişsiz kılmaktadır. Zaman aralıklı ADCler gerek ulaşabilecekleri dönüştürme hızı gerek güç verimliliği açısından iyi bir aday olarak karşımıza çıkar. Zaman aralıklama, tek kanallı eş ADClerin sıra ile kullanılması esasına dayanmaktadır. Sıradaki örneği alan ADC, sıra tekrar kendisine gelene kadar bu örneği dönüştürür. Dolayısıyla toplam dönüştürme hızı, tek bir dönüştürücünün hızı ile kanal sayısının çarpımı kadar olmaktadır. Bu şekilde yüksek dönüştürme hızları elde edilebilir. Ayrıca bu şekilde tek kanal ADCler daha fazla hız elde etmek için güç bakımından verimsiz oldukları noktalara itilmez ve daha verimli yapılar ortaya çıkar.

Zaman aralıklı ADClerdeki kanal uyumsuzlukları performansı düşürmektedir. Bu hatalar temel olarak dengesizlik, kazanç ve zamanlama uyumsuzluklarından ileri gelmektedir. Zamanlama hataları kestirilmeleri ve düzeltilmeleri noktasında diğerlerinden daha zorludur ve bu durum yüksek frekanslarda daha da zorlaşmaktadır.

Zaman aralıklı ADClerdeki zamanlama hatalarının kestirilmeleri ve düzeltilmeleri güncel bir araştırma konusu teşkil etmektedir. Hataların kalibrasyonu ön planda veya arka planda yapılabilir. Arka planda yapılan kalibrasyon sistemin işlerliği ile ilgili

herhangi bir sıkıntı yaratmaması ve değişen çevre şartlarına uyum sağlayabilme esnekliği açısından daha avantajlıdır.

Zaman aralıklama hataları frekans spektrumunda çıkıntılar(spur) oluşturmaktadır. Bu çıkıntılar, güçlü olmaları durumunda alıcı kısmındaki devreleri sıkıştırma noktasına iterek modülasyonlu işaretlerin sezilmesini zorlaştırabilir veya giriş işaretini tamamen engelleyebilirler. Dolayısıyla kanal uyumsuzluk hataları özellikle kablosuz haberleşme sistemleri için sorun teşkil etmektedir. Bu sorunlardan kurtulmak için kanalları rastgele kullanmaya dayanan bir teknik önerilmiştir. Bu teknik ile kanallardan kaynaklanan hatalar çıkışa rastgele bir sırayla etki yaptıklarından gürültü gibi bir karaktere geçerler. Dolayısıyla frekans spektrumundaki çıkıntılar söndürülmüş olur. Tekniğin bir diğer avantajı arka planda çalışmasıdır. Ancak dikkat edilmelidir ki bu teknik bir hata düzeltme tekniği değildir, dolayısıyla sistemin işaret-gürültü oranını iyileştirmemektedir.

Kanal uyumsuzluk hatalarının kestirilmesi gibi, saat işaretlerinin dağıtılması da artan kanal sayısı ile zorlaşmaktadır. Ayrıca yüksek kanal sayısına sahip olan zaman aralıklı ADClerde saat işareti dağıtımının tükettiği güç yüksek seviyelere ulaşabilir. Belli bir dönüştürme hızı için kanal sayısını düşük tutmak ise kanal ADClerinin dönüştürme hızlarını arttırmak ile mümkündür. ADClerin hızları yüksek tutulurken aynı zamanda güç verimliliği de yüksek tutulmalıdır. Bu hedefler doğrultusunda 8-bit 1 GS/s bir çevrimde birden fazla bit dönüştüren bir SAR ADC yapısı önerilmiştir. Bir çevrimde birden fazla bit dönüştüren SAR ADCler, tek kanalda yüksek hızlara çıkmak konusunda sıkça kullanılan bir yöntem olarak karşımıza çıkmaktadır. Bunun yanında ilk üç en anlamlı bit bir flash ADC ile dönüştürüldüğünden önemli hız kazanımları elde edilir. Flash ADC çıkışında bir kod çözücü yapısı kullanılmaması da zaman kazanımında etkilidir.

Önerilen ADC yapısında özgün bir dönüştürme algoritması kullanılmaktadır. Algoritma temel olarak, dönüştürme fazlarına fazladan seviyeler eklemek ve fazların aralıklarını kesiştirmek sureti ile devre bloklarının hata toleranslarını arttırmasına dayanmaktadır. Bu nedenle herhangi bir kalibrasyon sistemine ihtiyaç duyulmaz dolayısıyla güç tüketimi azaltılabilir. Bu yapının gerçeklenebilmesi için çoklu seviye üreten bir ön kuvvetlendirici önerilmiştir. Önerilen ön kuvvetlendirici yapısı nedeniyle, algoritmadaki farklı fazlar için tek bir ön kuvvetlendirici kullanılabilmektedir. Bu sayede farklı ön kuvvetlendiricilerden kaynaklanacak dengesizlik uyumsuzluklarının da önüne geçilmiş olur.

Yüksek hızlı veri dönüştürücülerin gerçeklenmesindeki en etkili devre bloğu, kendisi de 1 bitlik bir ADC olarak sayılabilecek karşılaştırıcı devreleridir. Karşılaştırıcı devresinin hızı, doğruluğu ve güç tüketimi bir ADCnin ilgili performans parametrelerini doğrudan etkilemektedir. Yüksek karşılaştırma hızlı özgün bir gömülü ön kuvvetlendiricili karşılaştırıcı devre önerilmiştir. Yapı geleneksel dinamik sezme kuvvetlendiricisi devresi temel alınarak tasarlanmıştır. Ek olarak giriş farksal kuvvetlendirici bölümüne bir statik akım kaynağı bağlanmıştır. Bu şekilde dinamik karşılaştırıcı yapısına ön kuvvetlendirici gömülmüş olur. Yapı geleneksel yapılara nazaran, hız, dengesizlik, güç tüketimi ve geri tepme gürültüsü açısından iyileştirmeler içermektedir.

8-bit 1 GS/s bir çevrimde birden fazla bit dönüştüren SAR ADC yapısı, ilk 3 biti olabildiğince hızlı dönüştürmek için bir flash ADC yapısı kullanmaktadır. Flash ADC yapılarının önemli hız avantajlarına rağmen, karşılaştırıcı devrelerin dengesizlik ve geri tepme gürültüsü performansı düşürmektedir. Önerilen gömülü ön kuvvetlendiricili karşılaştırıcı devresi dengesizlik performansını ve geri tepme gürültüsünü iyileştirmektedir. Ancak geri tepme gürültüsünden kaynaklanan hataları tam olarak çözmek adına, referans gerilimleri de giriş işaretleri gibi örneklenebilir. Bu teknik ile karşılaştırıcı geri tepme gürültüsünün giriş ve referans gerilimi üzerindeki etkisi eşitlenmekte ve geri tepme gürültüsünün etkisi bertaraf edilmektedir.

ADC girişleri örneklenerek geldiğinden ve örnekleme devrelerindeki bir hata doğrudan ADCye iletileceğinden bu devrelerin performansı çok önemlidir. Çapraz bağlamalı anahtar tekniği kullanılarak anahtarların doğrusallığı iyileştirilmiştir. Aynı zamanda çapraz bağlama tekniği anahtar yük enjeksiyonu hatasını giriş işaretinden bağımsız hale getirmektedir. Bu durum, yukarıda bahsedilen referans örnekleme tekniği ile birleştirildiğinde flash ADC için önemli bir doğruluk iyileştirmesi sağlamaktadır.

ADC blokları ST Microelectronics 65 nm CMOS teknolojisinde tasarlanmış ve serimleri yapılmıştır. Serim sonrası benzetim sonuçları tasarımların ve kullanılan tekniklerin doğruluğunu göstermektedir. Tasarlanan ADC Haziran 2015'de üretime yollanmıştır. Kasım 2015'de ölçümlere başlanması planlanmaktadır.

1. INTRODUCTION

Communication systems are one of the main driving force behind the electronics industry. Advent of the semiconductor process technologies has paved the way for higher data rates in those systems. Therefore, not only wireless communication systems but also wireline communication systems should satisfy the speed demands while being accurate enough and power efficient.

Digital process technologies scale faster than analog, which shifted the bulk of the signal processing to the digital domain. Communication systems benefit from that approach too. In order to process high data rate signals on digital domain, high-speed ADCs are crucial.

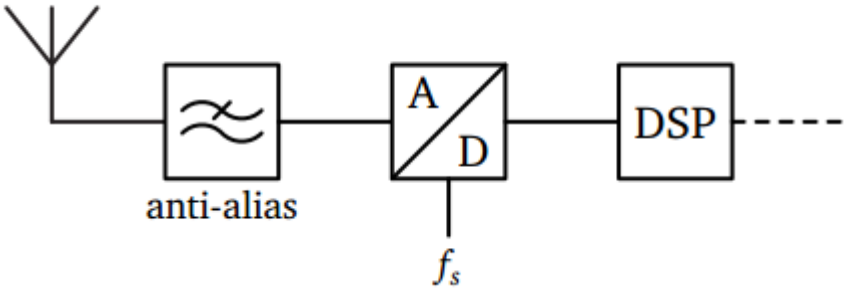

Figure 1.1: Generic software radio receiver front-end [1].

High-speed ADCs are present on software radio front-ends. Generic software radio structure is shown in Figure 1.1**.** The principle of software radio is to sample the RF input as close as possible to the antenna. In ideal case, the input is sampled right after the anti-aliasing filter following the antenna so that the operations such as demodulation, down-conversion can be done in digital domain. However as stated in [1], this approach is not currently realizable. Nevertheless, since it will allow easily realizable and portable multi-standard receiver and transceiver architectures, software radio concept is appealing and relies on high-speed, high-performance ADC architectures.

High-speed ADCs take part in wireline communication front-ends too. Wireline communication channels suffer from non-idealities such as channel loss, reflections and cross-talk. In order to overcome these effects complex equalization techniques are required which can be effectively realized with ADC-based receivers which is shown in Figure 1.2. As stated in [2], "the advantages of such ADC-based receiver include: better programmability and extensibility to different channel characteristics; better equalization robustness to process and coefficient variations; possibility of using more powerful signal processing techniques such as sequence detection to achieve lower BER; and potential of adopting complex modulation schemes beyond binary PAM".

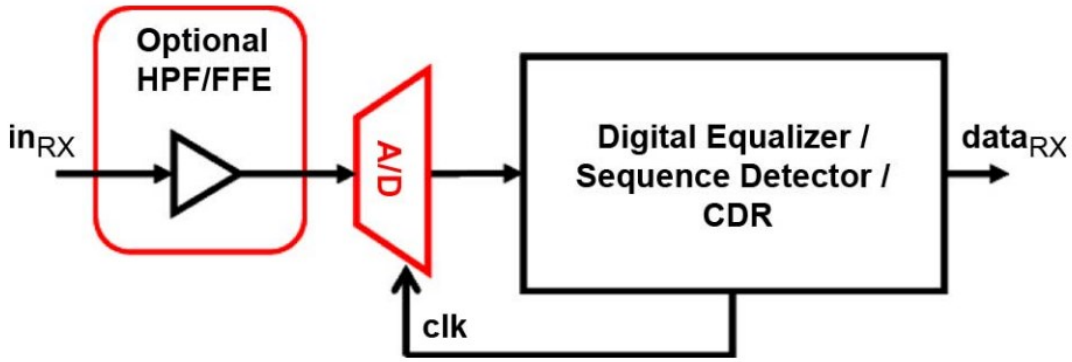

Figure 1.2: ADC-based serial I/O receiver [2].

With the data rates exceeding 10 Gbps, single channel ADCs are not able to provide a power efficient solution for these demands, which calls for time-interleaved ADCs which achieve tens of GS/s sampling rates with power efficiency in low-medium resolution.

1.1 Thesis Motivation

Interferers should be problematic for communication systems, especially for wireless. This makes spurs in the frequency spectra important. Time-interleaving errors cause spurs in the spectra. Therefore time-interleaved ADCs benefit from a technique, which decreases the magnitude of spurs. Hence in this thesis, studies of such a technique have been done.

Time interleaving is a power efficient solution for high-speed conversion demands of communication systems. However, calibration techniques used in single-channel

ADCs may diminish the efficiency gained by time interleaving. Therefore time-interleaved ADCs benefit from, single-channel ADCs based on search algorithms, which do not require calibration. In addition, channel number of a time-interleaved ADC should be kept low in order to maintain a power-efficient and non-complex clock distribution and to keep estimation and calibration of channel mismatch errors affordable. This calls for fast single-channel ADCs. Hence, in this thesis an 8-bit 1 GS/s single channel ADC architecture is studied and designed to be used in a +10GS/s time-interleaved ADC.

1.2 Thesis Organization

The organization of the thesis is as follows:

Chapter 2 explains the fundamentals of time interleaved ADCs and errors stem from channel mismatches. A technique to diminish the channel mismatch effects on SFDR is proposed.

Chapter 3 includes an overview of single-channel ADCs in state-of-the-art time-interleaved ADCs. Then a 8-bit multi-bit per cycle 1 GS/s single-channel ADC is proposed which combines a novel searching algorithm based on redundancy and novel multiple-threshold generation preamplifier.

Chapter 4 includes an overview of comparators used in state-of-the-art ADCs and main comparator specifications. Then a novel comparator architecture is proposed which embeds the preamplifier in latch. Comparison of novel architecture with conventional structures is presented and its advantages are explained.

Chapter 5 explains the design of comparators, flash ADC and bootstrapped switch to be used in the single-channel ADC. Layouts of the blocks are shown and results of post-layout simulations are presented in order to show the accuracy of design. Top-level layout as well as overall post-layout simulations of single-channel ADC is presented too.

Chapter 6 concludes the thesis and possible future work based on the thesis.

2. TIME INTERLEAVED ADC ARCHITECTURES

2.1 Introduction

Time interleaved ADC (TI-ADC) [3] is power efficient response to the demand for high-speed ADCs where technology limits the efficiency of a single channel ADC. Basic principle of operation and timing diagram are shown in Figure 2.1 for an n-bit, N channel time interleaved ADC. Whole ADC consists of N n-bit single channel ADCs (slices) which operate concurrently. Input is sampled with a frequency of $f_S = (1 / Ts)$ which is also the aggregate frequency of overall ADC. Sampled inputs are fed into one of the ADCs in a row. Therefore, each ADC has an operating frequency of f_s / N. When one of the slices finishes the conversion, its output is picked by a multiplexer and is given to output.

Following sections explain the advantages and disadvantages of time-interleaved architectures and interleaving errors due to the mismatches between channels. Then some of the existing solutions to these errors are summarized. In the end, a technique to diminish the effects of timing mismatch error is presented and design considerations over this architecture are discussed.

2.2 Time Interleaving Advantages and Disadvantages

Time interleaving offers several advantages over their single channel counterparts in terms of maximum speed, power consumption and metastability. Ideally, the overall speed can be increased just by increasing the channel number. As stated in [4], "Interleaving improves the FOM because, as the conversion speed of a single channel approaches the limits of the technology, the power-speed tradeoff becomes nonlinear, demanding a disproportionately higher power for a desired increase in speed". Interleaved ADC channels operate in slower frequencies in which they could be designed more power efficient. Since power consumption in dynamic circuits is proportional to operating frequency, clocking network benefit from slower operation

as well. Finally, metastability errors are reduced due to longer clock period of each channel so that comparators have more time to make a decision.

Time interleaving has disadvantages as well such as area penalty; complex clock distribution and channel mismatch errors. These errors are main factors, which limits the number of channels in a TI-ADC. More detailed explanation of channel mismatch errors are given in following sections.

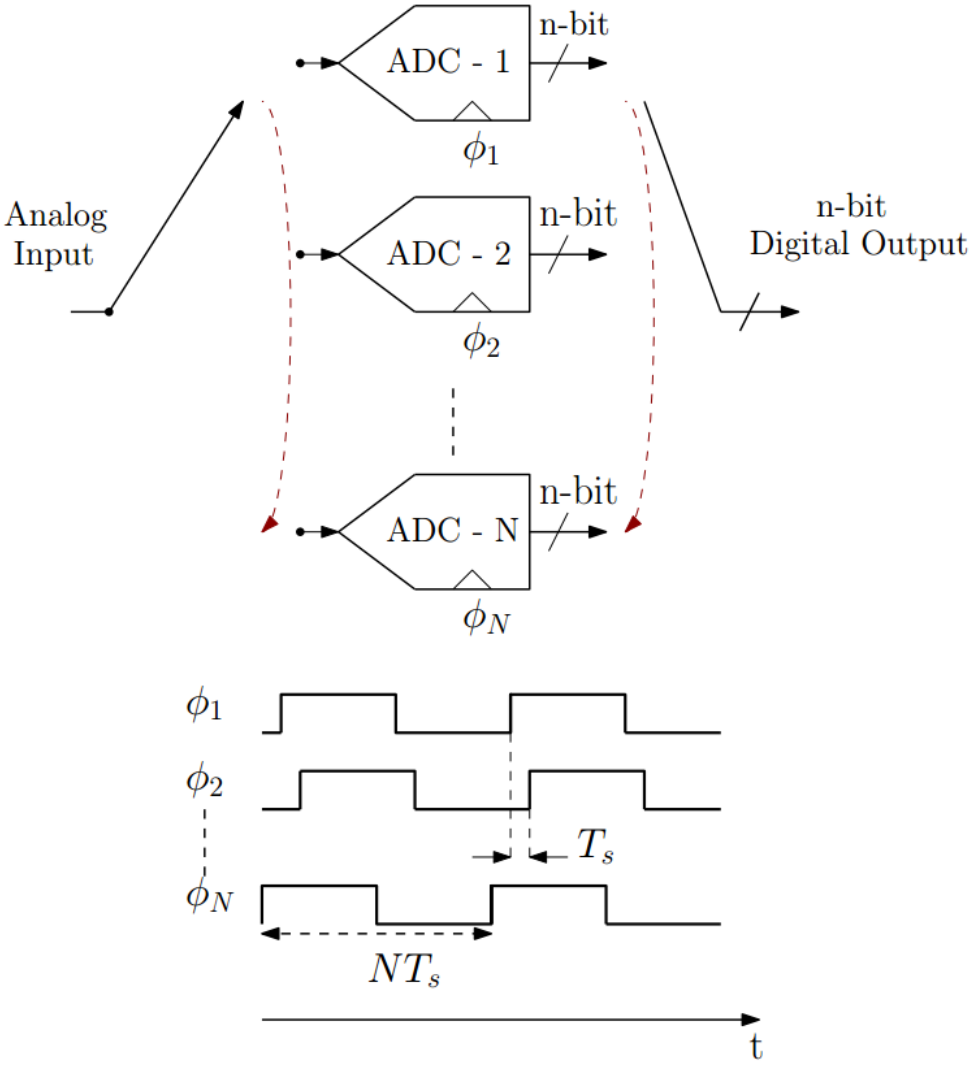

Figure 2.1: Time interleaved ADC operation principle.

2.3 Time Interleaving Errors

Offset, gain and timing mismatches of channels in a time-interleaved ADC are main factors, which limit the overall resolution of the ADC. Following sections explain main characteristics of those errors.

In order to observe the error patterns of mismatch errors in TI-ADCs and their effects on frequency domain, a behavioral TI-ADC model is created and shown in Appendix A. Model creates a sine wave whose points are picked concurrently, such as in TI-ADC, from non-ideal sine waves created with relative errors. For all the cases, f_s = 10 GHz and f_{in} = 127 MHz.

2.3.1 Offset mismatch

Considering different DC offsets of the ADC channels in a TI-ADC, during the concurrent operation, those offsets produce static errors with a frequency of (f_s / N). As DC offsets are independent from input frequency and amplitude, this errors as well frequency and amplitude independent. As stated in [5], offset errors produce spurs at:

$$f_{noise} = k\,(f_s\ /N)\,, \qquad k = 1,2,3,\ldots \tag{2.1}$$

SNR versus input frequency graph of a TI-ADC with only offset error is shown in Figure 2.2. This graph again shows that input frequency does not affect the SNR in presence of offset mismatch.

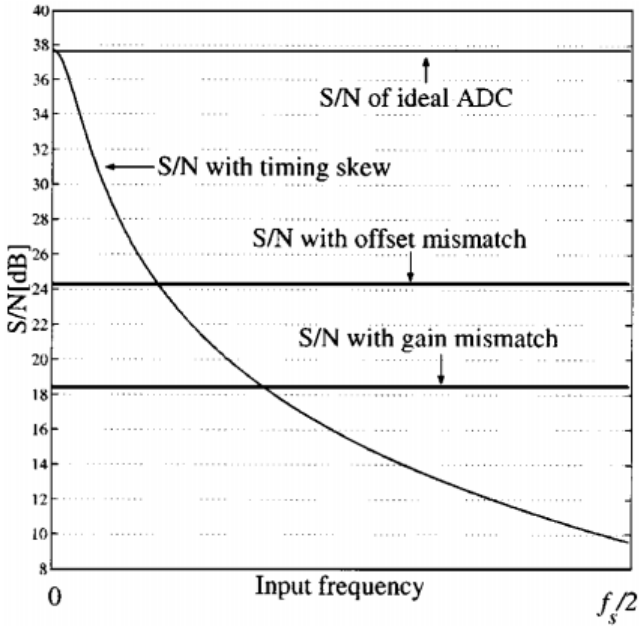

Figure 2.2: SNR versus input frequency graph of errors in a TI-ADC from [5].

For N=8, effects of offset mismatch in time-domain and frequency-domain is observed via TI-ADC model in MATLAB. Peak amplitude of sine wave is picked as

0.06 V and random offset errors with standard deviation of 4 mV were assigned to channels. Results in time-domain are shown in Figure 2.3. Note that, error has a constant envelope, which shows that the offset mismatch is amplitude independent. Frequency-domain results are shown in Figure 2.4. As anticipated, spurs due to offset mismatch appeared on $(f_s/8) = 0.125\ f_s$, $2(f_s/8) = 0.25 f_s$ and so on.

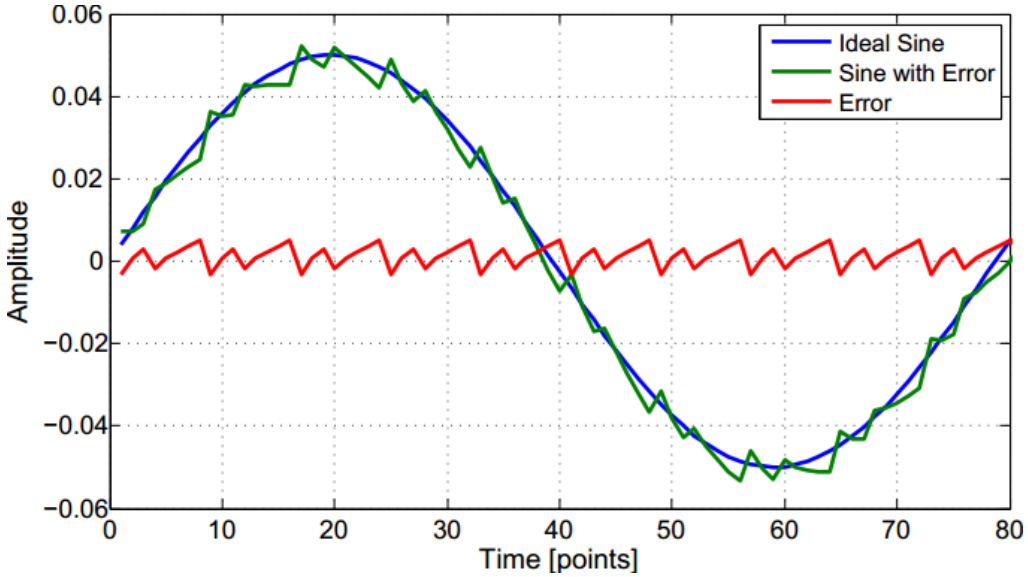

Figure 2.3: Ideal sine wave, sine wave with offset mismatch and error signal.

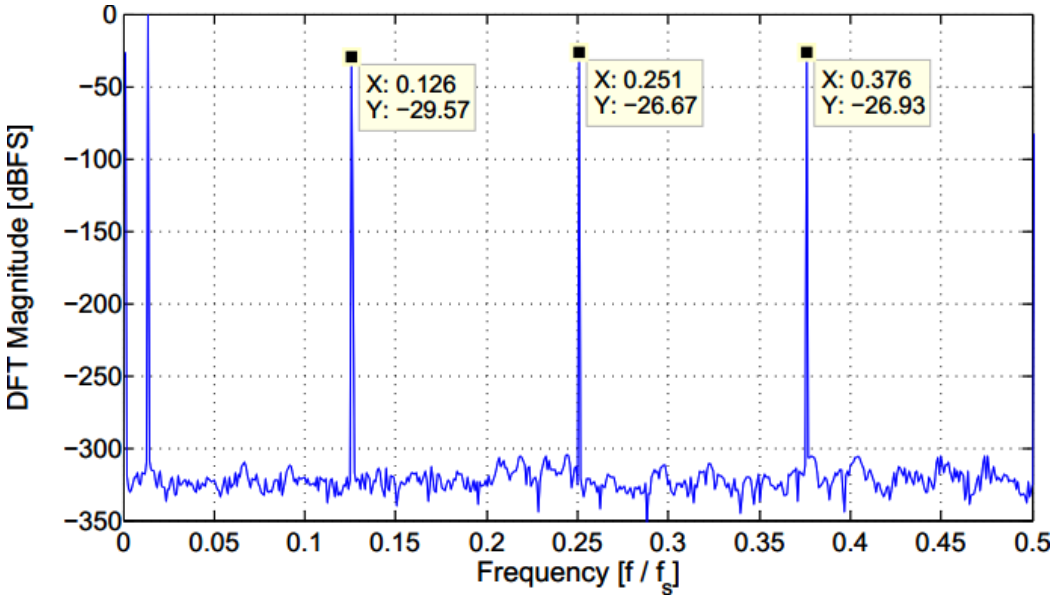

Figure 2.4: DFT of sine wave with offset mismatch in TI-ADC.

2.3.2 Gain mismatch

In order to observe effects of offset mismatch, non-ideal gain values were created with a standard deviation of 5%.

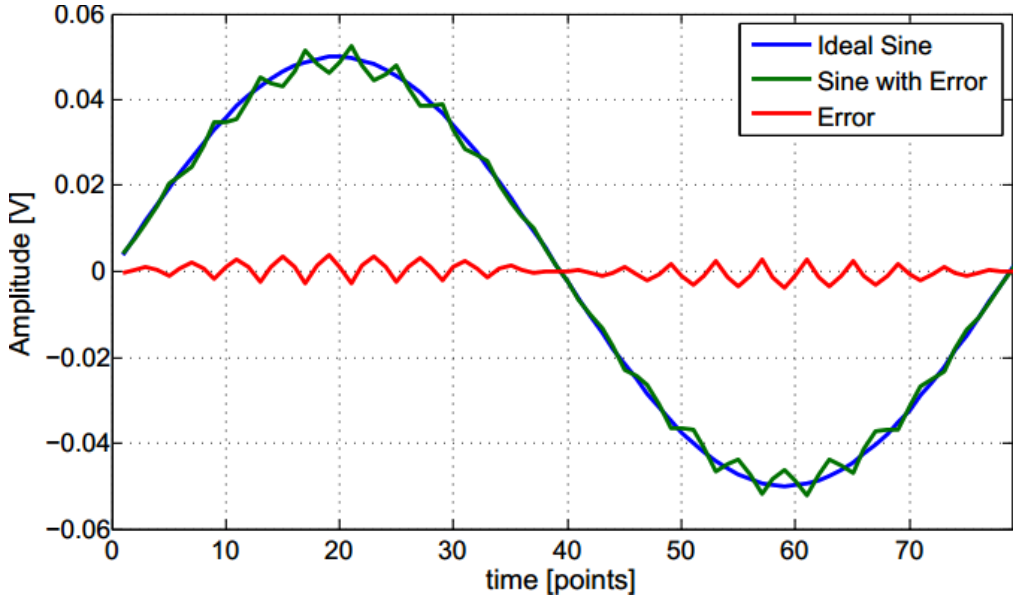

Figure 2.5: Ideal sine wave, sine wave with gain mismatch and error signal.

As shown in Figure 2.2, gain mismatch error does not depend on input frequency just like offset mismatch. However, as shown in Figure 2.5, error is low on zero-crossings meanwhile it increases close to the peaks of sine wave. Therefore, it can be said that gain mismatch error changes with input amplitude.

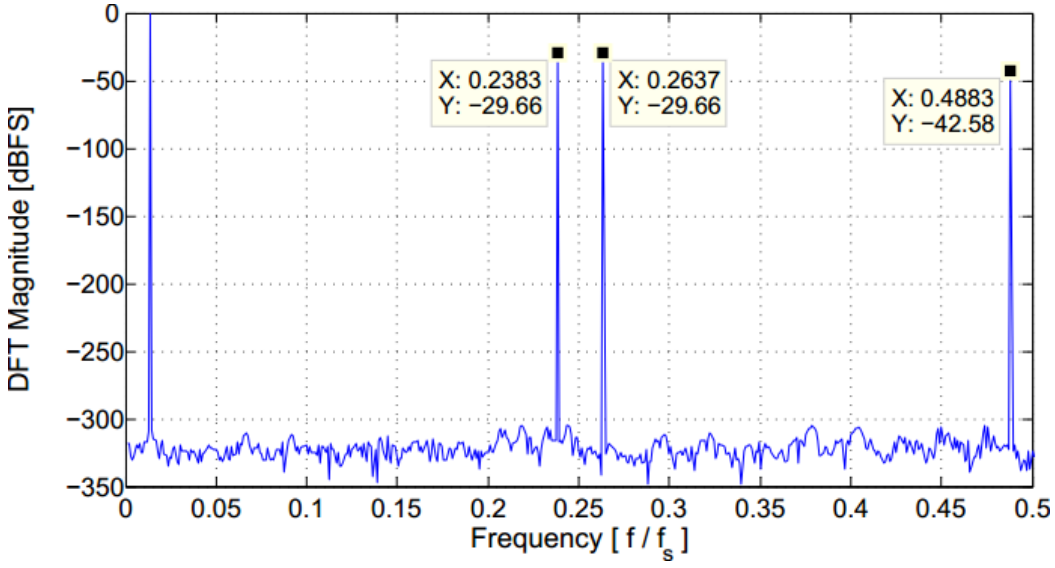

Figure 2.6: DFT of sine wave with gain mismatch in TI-ADC.

As stated in [5], spurs due to gain mismatch appear at:

$$f_{noise} = k\,(f_s\ /N\,), \qquad k = 1,2,3,\ldots \tag{2.2}$$

Effects of gain mismatch on frequency domain observed for N = 4. Frequency-domain results are shown in Figure 2.6. As expected for Equation 2.2, spurs appeared approximately at 0.0127 + 0.25 = 0.2627, (-0.0127) + 0.25 = 0.2373 and so on.

2.3.3 Timing mismatch

Proper clocking is one of the most challenging parts in of TI-ADC design. Timing errors in a TI-ADC can be random or systematic. Random timing error is jitter, which is unavoidable in practical cases. However, system can be made tolerant to jitter by the design. Systematic part of timing errors stems from the clock skew mismatch of channels. Those errors are much harder to estimate and correct compared to offset mismatch and gain mismatch. It is shown in Figure 2.2, degradation due to timing mismatch increases with input frequency, which makes timing errors more problematic.

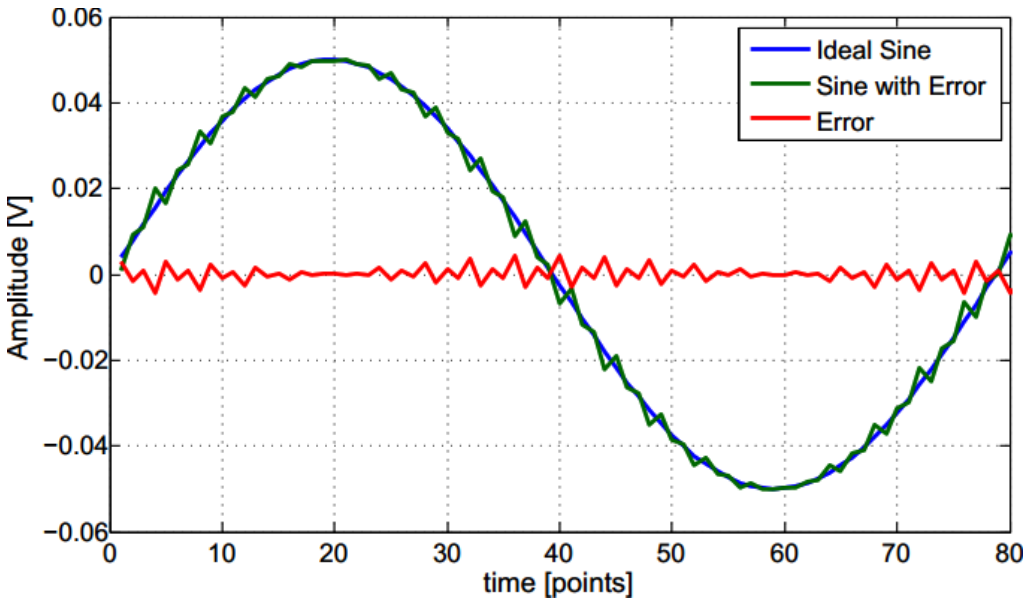

Figure 2.7: Ideal sine wave, sine wave with timing mismatch and error signal.

As stated in [5], spurs due to timing mismatch appear at:

$$f_{noise} = \pm f_{in} + \frac{k}{N} f_s, \qquad k = 1,2,3,\ldots \tag{2.3}$$

In order to observe the effects of timing mismatch on time and frequency domain, for N = 4, random timing skews were created with standard deviation of 100 ps and were assigned to channels. Figure 2.7 shows the time domain errors. Note that error increases on zero-crossings. Zero crossings are where the slope of the sine wave is at

its highest. This explains the performance degradation with increasing input frequency since high frequency sine waves has higher slope on zero-crossings.

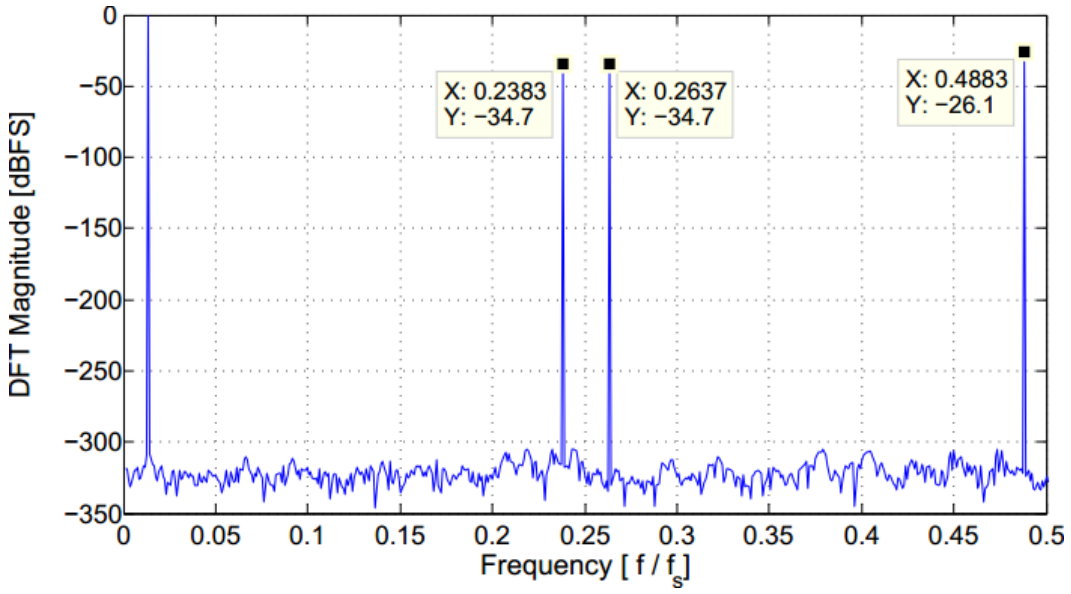

Figure 2.8: DFT of sine wave with timing mismatch in TI-ADC.

Effects of timing mismatch on frequency domain are shown in Figure 2.8. As expected from Equation 2.3, spurs appeared approximately at (0.0127 + 0.25 = 0.2627), (-0.0127 + 0.25 = 0.2373) and so on.

2.4 Existing Solutions to Time Interleaving Errors

Recent literature shows an increasing effort on solutions to timing mismatch errors in a TI-ADC since it is problematic to both estimate and correct. Two types of estimation and correction are present, namely background and foreground. During foreground estimation and correction, ADC is offline. A time is allocated to calibration, which can be problematic for some applications. On the contrary, for background estimation and calibration, the work is done on the fly. This type is more suitable for adapting the frequently changing conditions.

Correction approach is mostly similar considering a digitally controlled delay line is employed for most of the cases. However, estimation techniques are still a popular research topic. This section gives few examples from recent literature to solve the timing mismatch errors for TI-ADCs with conversion speed of 10 GS/s and more.

One approach is employing a master track-and-hold circuit [6]. In this approach, timing errors are prevented since there is only one clock signal needed for the master

track-and-hold, which eliminates any clock skew. The samples are distributed to the channels after they are sampled. Although it is a simple and effective solution, designing a track-and-hold circuit with a wide bandwidth is highly challenging. In [7], an on-chip sinusoidal test signal is generated on-chip and fed to each ADC channel. Subsequently, digital outputs are processed off-chip to decide on the correction values. A disadvantage of this approach is that it is foreground. In [8], errors are statistically estimated. In [9], timing skews are estimated by employing feed forward equalizers. In [10] an embedded time-to-digital converter is used to estimate the mismatch. All of the last three techniques are background calibration techniques.

2.5 Proposed Technique to Diminish the Effects of Timing Mismatch

Increasing conversion rates make dynamic specifications of ADCs much more prominent. Among them, Spurious Free Dynamic Range (SFDR), is defined in [11] as "the ratio of the root-mean-square signal amplitude to the root-mean-square value of the highest spurious spectral component in the first Nyquist zone".

SFDR is especially important for communication systems. Higher data rates makes the communication bands crowded and this make filtering of interferer signals cumbersome. If the SFDR is low for the ADC in the receiver side, spurs due to the strong interferer on the antenna may block the input signal itself.

In Section 2.3, it has shown that the time interleaving errors cause spurs in frequency spectrum, whose amplitudes can be significantly high. Although high data rate communication systems benefit from the significant speed advantage of TI-ADCs, spurs due to interleaving errors may be problematic for those systems.

Instead of estimation and correction approaches in Section 2.4, an approach just to diminish the effect of spurs may be taken. In order to achieve this, an approach called dynamic element matching, like proposed in [12] for DACs, can be adopted. As stated in [11], "The goal of the approach is to equal the elements on average instead of performing a static correction of the values". Principle of operation is as follows: Each ADC channel is selected randomly to convert the next sample. In this way, periodic nature of mismatch errors explained in Section 2.3 is no longer valid. Therefore, spurs are extinguished and the power of mismatch errors is spread across

frequency like in the case of quantization noise. This technique is a background method, which makes it appealing. An important point is that, since there is no error correction, signal-to-noise ratio (SNR) of the system does not increase with the technique.

2.6 Behavioral Simulation Results

Behavioral model is used for showing the effectiveness of the technique. Again, random timing skews were created with standard deviation of 100 ps and assigned to 8-channel regular TI-ADC and 12-channel TI-ADC with 8 main and 4 redundant channels. Comparison of two cases was given in Figure 2.9. Note that an SFDR improvement of 8 dB.

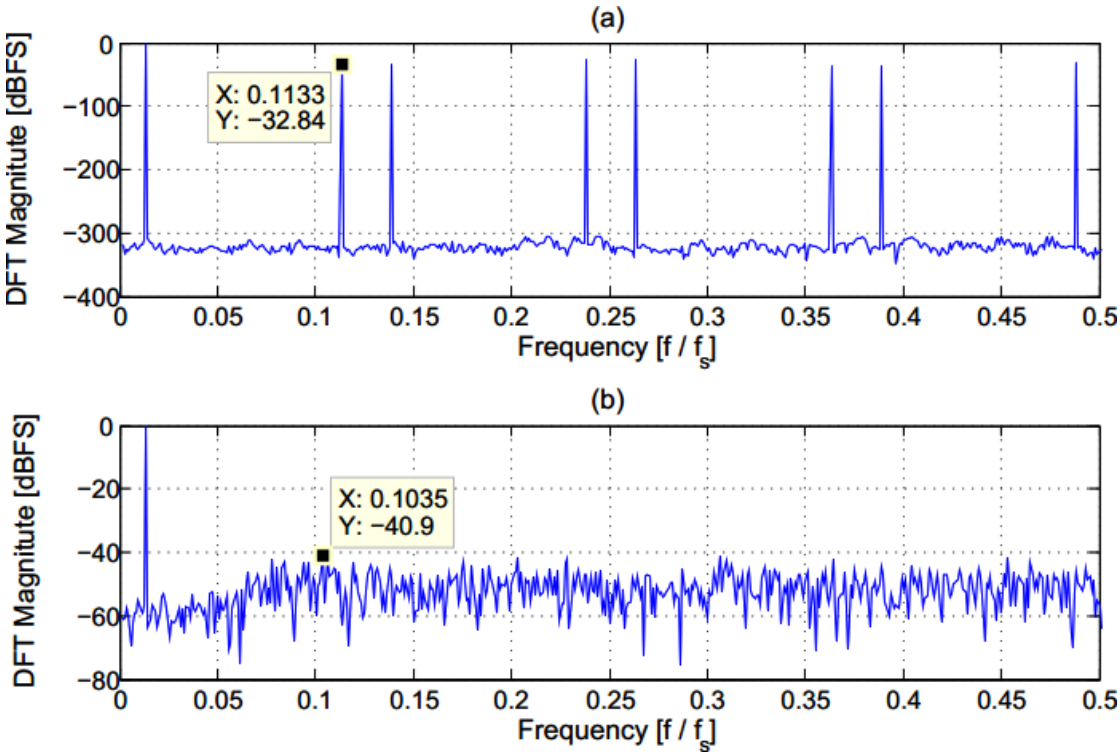

Figure 2.9: Comparison of Regular TI-ADC (a) and TI-ADC with randomization (b).

2.7 Implementation Considerations

Possible implementation of the technique is depicted in Figure 2.10. Here $M = N + R$ where N denotes the total main channel number and R denotes the number of redundant channels.

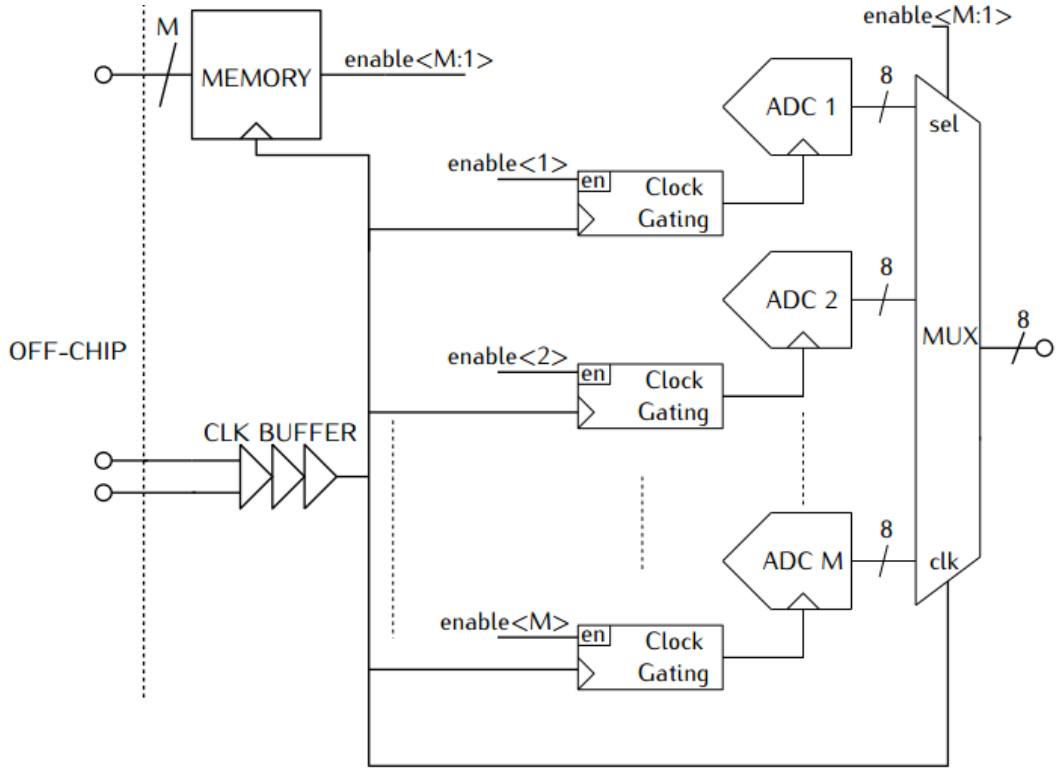

Figure 2.10: Possible implementation of proposed technique.

Main point where the implementation diverges from the theory is the impossibility of generating true random sequences. Pseudo-random sequences with finite length can be generated with circuits. Therefore, the sequence should be kept as long as possible.

Second issue arises due to the operation principle of TI-ADCs. A channel picked for conversion is not going to be ready to be picked for the next *(N/fs)* seconds. Therefore, the sequence should be generated keeping this point in mind, which makes the regular pseudo-random number generating circuits not available for this purpose.

Considering aforementioned issues, generating the sequence off-chip and writing it on an on-chip memory is a good solution for implementing the technique. Memory size should be chosen for the minimum sequence length, which improves the SFDR significantly.

In order to show the effect of the sequence length, random sequences with the lengths of 16 and 256 are generated and used on the behavioral model on MATLAB. Results are shown in Figure 2.11. Note that increasing the sequence length to 256 from 16 improves the SFDR performance by 6.4 dB.

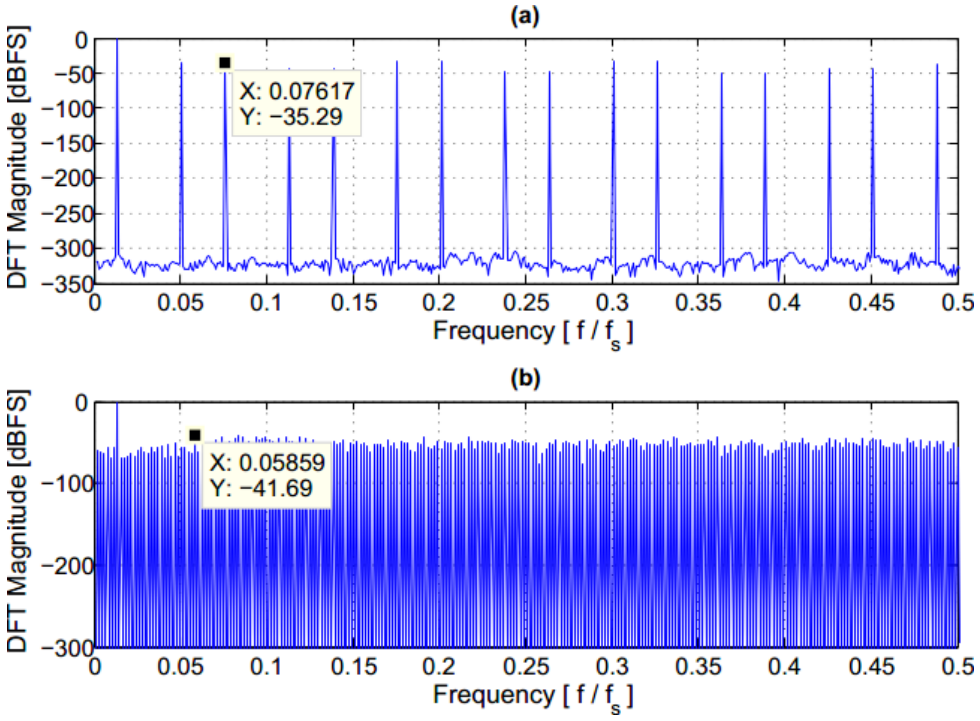

Figure 2.11: Comparison of randomization sequence lengths: 16 (a) and 256 (b).

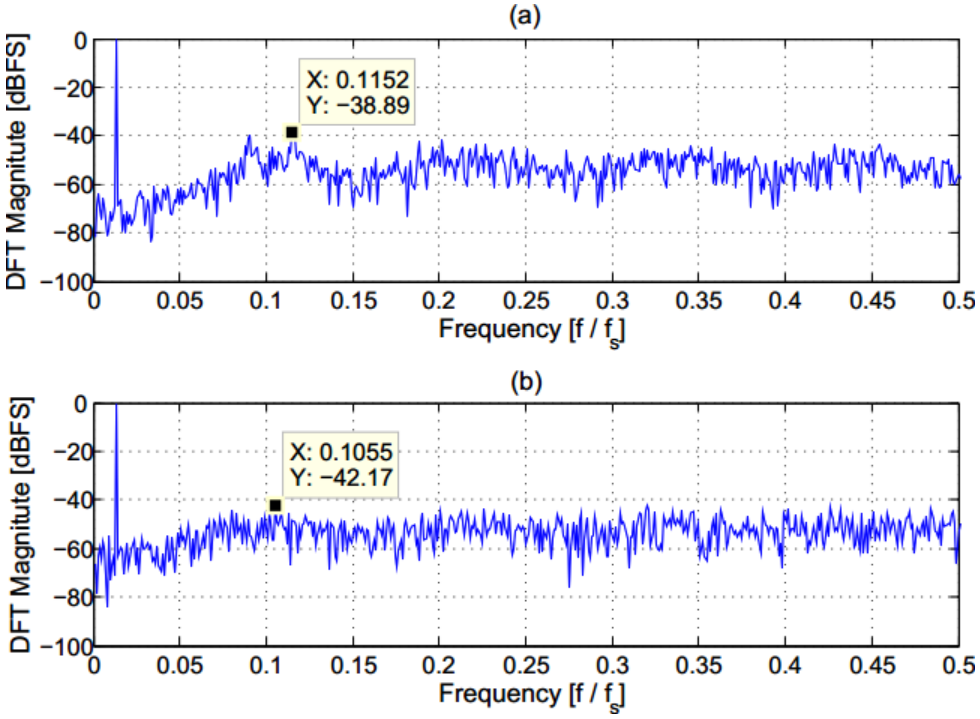

Figure 2.12: Comparison of redundant channel number for 8-channel TI-ADC: 2 (a) and 4 (b).

Number of redundant channels is another important design consideration. Using more redundant channels makes randomization more effective since it reduces the probability of periodicity. In order to prove the point, randomization with infinite-length sequence is applied to TI-ADC models with 2 and 4 redundant channels.

Results are shown in Figure 2.12. Note that by using 4 redundant channels, 4 dB of SFDR improvement is achieved. However, there is an area and complexity and SFDR tradeoff for the number of redundant channels in this case. Therefore, the number of redundant channels must be considered carefully.

3. SINGLE CHANNEL HIGH SPEED ADCS

Time-interleaved architectures provide an efficient solution to the speed - power consumption trade-off [4]. Ideally, the speed can be increased just by increasing the channel count. However as stated in the Chapter 2, offset, gain and timing mismatches between the interleaved ADC channels degrades the performance. Increasing the interleaving factor not only exacerbates the estimation and correction of the interleaving errors but also pushes the power consumption of the whole ADC far from the optimum. In addition, feasibility of the proposed technique mentioned in Section 2.5 depends on low interleaving factor since it relies on the redundant ADC channels. Therefore, it is more desirable to increase the speed of a single channel as much as possible in order to keep the interleaving factor low.

Following sections investigate the high-speed single channel ADCs used in state-of-the-art time interleaved ADCs and then proposes a novel single channel architecture suitable for 10 GS/s time interleaved ADC.

3.1 Architectures

In order to achieve more than 10 GS/s with an interleaving factor which lets power efficient design, single channel ADCs should reach the speeds greater than 1 GS/s.

Flash ADC is a good candidate since it lends itself for whole conversion in a single clock cycle. An n-bit flash ADC requires $[(2^n) - 1]$ comparators. Combined with reference generation and auxiliary circuits, this makes flash ADCs impractical for medium and high resolutions in terms of power consumption and area. In recent literature there are several +10 GS/s time-interleaved ADCs employing a flash ADC for single channel. For instance in [10], a 20 GS/s 6 bit time-interleaved ADC is presented. ADC employs 8-way interleaved 2.5 GS/s flash ADCs. In [8], a 12 GS/s 5-bit 8-channel time-interleaved architecture, which employs 1.5 GS /s flash ADCs, is presented. These examples prove the feasibility of flash ADCs for a single channel in low-resolution time-interleaved architectures.

SAR ADC is one of the commonly used ADC architecture in time-interleaved architectures with medium and high-resolution applications. As stated in [11], "the method aims to reduce the circuit complexity and power consumption using a low conversion rate by allowing one clock period per bit".

However, SAR ADCs resolve 1 bit at a time, which limits their speed. There are several approaches to circumvent this drawback. One of them is asynchronous successive approximation ADC [13]. As the name suggests, this type of SAR ADC does not employ a synchronous internal clock to proceed the approximations, periodic clock signal is only used for input sampling. Successive approximation algorithm suggests that, only one of the approximations falls into 0.5 LSB band of the input in which comparator is close to metastability. Therefore, except this metastable cycle, approximations will be faster. This makes the use of a synchronous clock whose period is adjusted for the worst case, unnecessary. In asynchronous SAR ADC, a ready signal is generated after resolving each bit to continue with the next one, which makes the whole conversion faster than the synchronous counterpart does. In [14], 90 GS/s 8 bit 64-way interleaved SAR ADC is presented. This ADC employs a 1.2 GS/s 8-bit asynchronous SAR ADC as a single channel.

One other approach to increase the speed of a single channel SAR is realized by resolving multi-bit per cycle. This approach is based on combining speed advantage of flash architecture and the energy efficiency of SAR architecture [15]. In [15], input is sampled on three identical SAR ADCs. Then in other phases, appropriate switches of these SAR are switched to generate reference voltages of 2-bit flash ADC. 3 comparators which are connected to those capacitive networks resolve 2-bits in each cycle.

3.2 Proposed Architecture

3.2.1 Search algorithm

As stated in previous section, SAR ADCs, which resolve multi-bit per cycle, can achieve considerably higher speeds compared to conventional SAR ADC architecture. A novel architecture, which combines multi-bit per cycle and redundancy to achieve 8-bit and 1GS/s, is presented.

Proposed technique uses a novel searching algorithm with redundancy that allows for relaxed accuracy in the first stages of conversion. The conversion is carried out by three successive approximations. A flash ADC is employed for the coarse conversion, whereas a multi-bit SAR ADC does the fine conversion.

Figure 3.1 depicts threshold placements of the proposed architecture. 14 level flash ADC is employed for the coarse conversion. In a standard 4 bit flash ADC, thresholds would be placed every 16 LSBs. Meanwhile in the proposed architecture, thanks to the redundancy used in the next stage, thresholds are placed at $V_{TH} = (8 + k \times 16)$ LSBs. It can be seen from the Figure 3.1 that the next SAR stage intervals overlap. This makes the 1 bit of coarse conversion redundant. This allows thresholds to be created with a reduced accuracy of ± 8 LSBs.

After the coarse conversion output of the capacitive DAC is given in Equation 3.1, where k_{flash} stands for the number of thresholds that is triggered during the coarse conversion.

$$V_{DAC,1} = \left(k_{flash} + 1\right) \times 16\, LSB - V_{IN} \tag{3.1}$$

Coarse conversion by the flash ADC is succeeded by an intermediate stage (SAR-1) which has intervals of [-16 ; +16] LSBs. Note that the intervals of this stage is larger than the flash stage. This relaxes the accuracy requirements of flash ADC.

SAR-1 stage is a multi-bit per cycle SAR ADC with redundant levels, which has thresholds at $V_{TH} = (2 + k \times 4)\, LSBs$ where $k = -\frac{N_{th}}{2} : +\frac{N_{th}}{2} - 1$ being $N_{th} = 6$. In this stage, redundant levels relax the threshold accuracy requirements by $\pm 2\, LSB$. Figure 3.1 demonstrates the placement of thresholds in this stage. Again, overlap of the intervals is leveraged to relax accuracy requirements. In this stage, 3rd, 4th and 5th MSBs are resolved and the output of the capacitive DAC becomes as given in Equation 3.2. Here k_{SAR1} stands for the number of thresholds that is triggered during the first fine conversion.

$$V_{DAC,1} = \left(k_{flash} \times 16\, LSB\right) + \left(k_{SAR1} + 1\right) \times 4\, LSB - V_{IN} \tag{3.2}$$

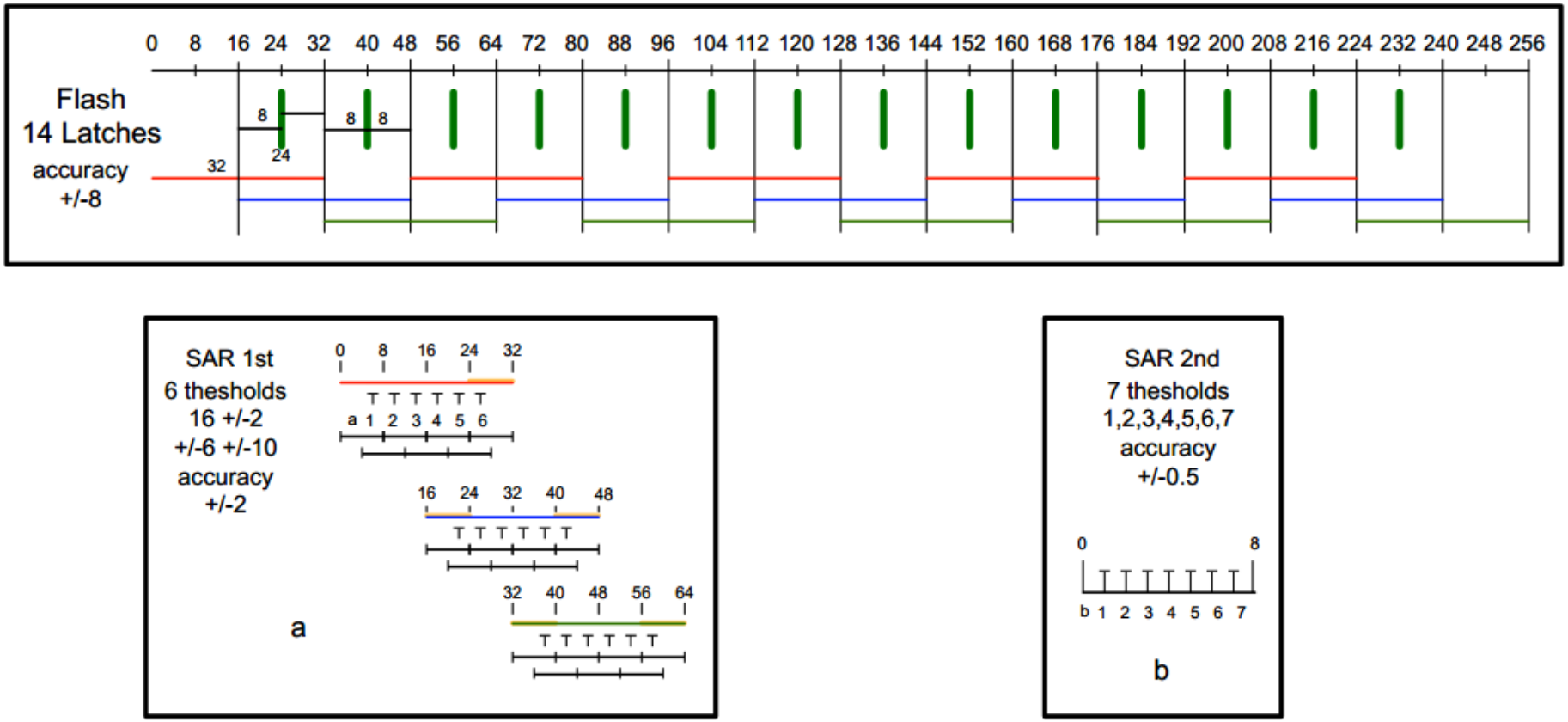

Figure 3.1: Threshold placement in the proposed architecture.

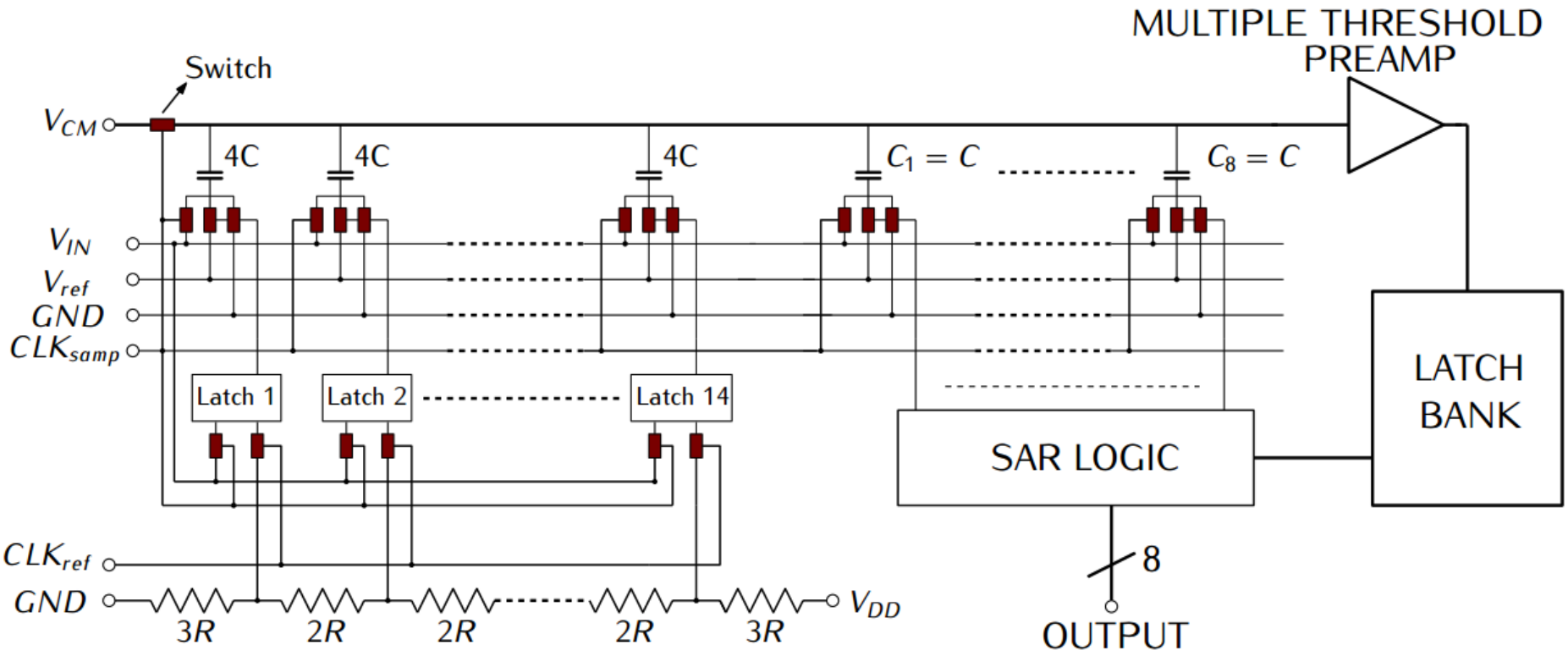

Figure 3.2: Proposed ADC architecture.

The second SAR stage (SAR-2) performs a standard 3-bit conversion in a cycle. This stage resolves 3 LSBs which requires maximum accuracy. As it will be explained later, these accuracy requirements perfectly match the way thresholds are implemented in the proposed architecture. In fact, it is easier in our solution to generate more accurate thresholds when the absolute interval to explore is reduced in term of LSBs as it is the case of the last stage, [-3 ; +3] LSBs.

Timing arrangement of the proposed architecture is given in Figure 3.3. 4 GHz master clock is used in the architecture. Sample window is 250 ps long and other phases are 125 ps long each.

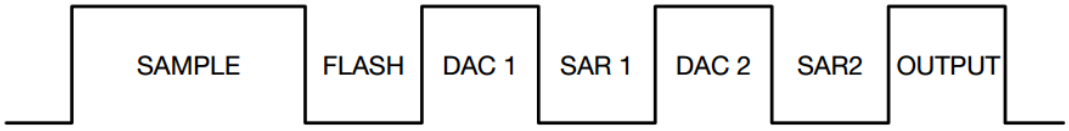

Figure 3.3: Timing arrangement of the proposed ADC architecture.

The effectiveness of the proposed searching path is explained with an example. In Figure 3.4(a), a decision process without an error is depicted. In Figure 3.4(b) decision errors have been made both of the first two stages. Note that, thanks to the redundancy, in both of the cases final decisions are same and correct. Figure 3.4 is important, too, for showing the strict accuracy requirements of the last stage.

3.2.2 ADC structure

Search algorithm mentioned in Section 3.2.1 is realized by the architecture shown in Figure 3.2. For the sake of compactness only the positive input half is shown. This half of the ADC includes the flash ADC to resolve the first 3 MSB whereas negative part does not employ a flash ADC. This is due to save area and power since it is not essential to use a differential to determine on the first 3 bits. As discussed in following sections, errors due to single-ended flash ADC doesn't affect the overall performance of ADC significantly as necessary measures have been taken to mitigate the effects.

Flash ADC is not succeeded by a decoder structure. Instead, a thermometric capacitive DAC is used. This is advantageous since this DAC also forms the MSB part of the SAR capacitive DAC.

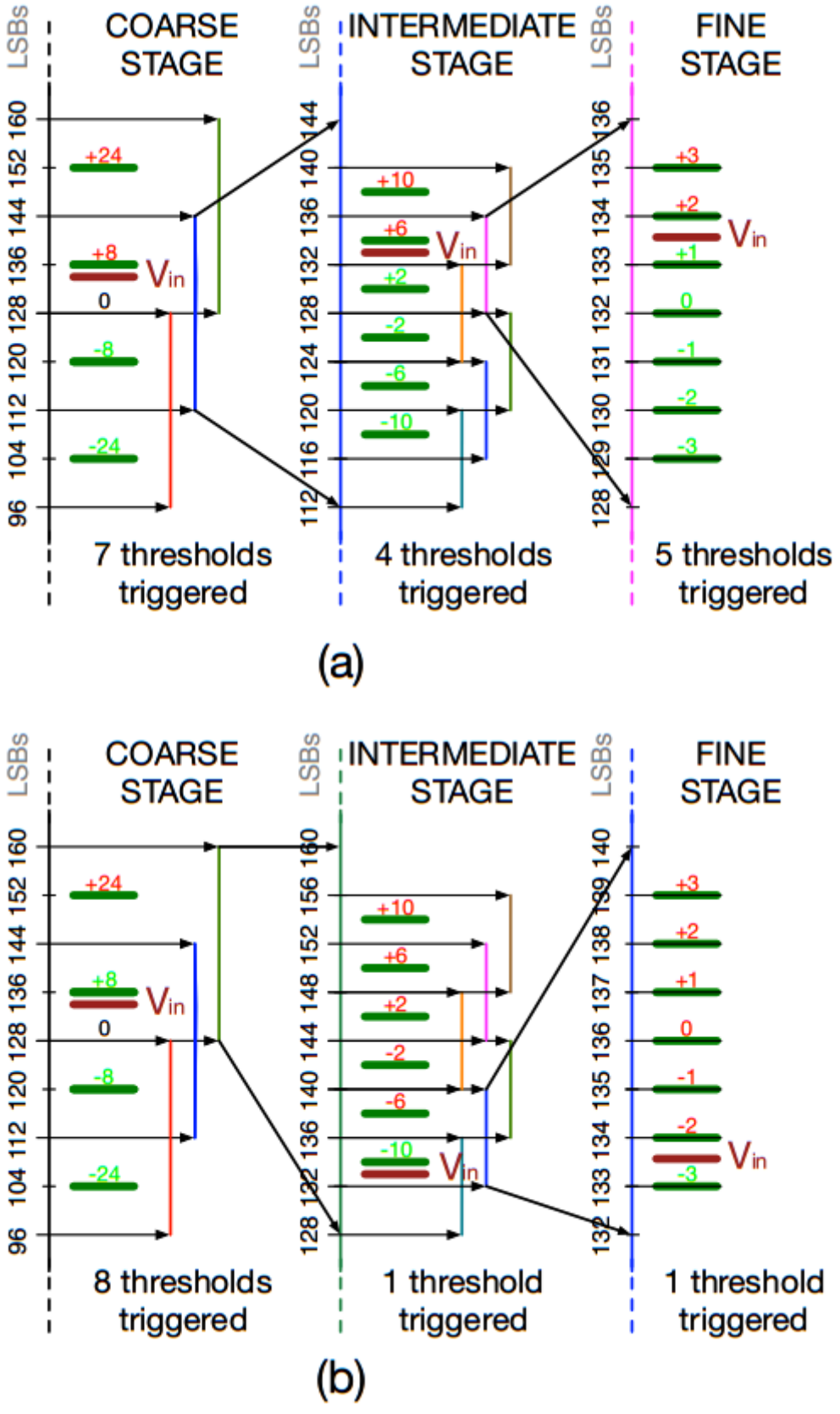

Figure 3.4: Example of proposed searching path: (a) correct, (b) with decision errors.

Conversion of the remaining 5 LSBs are carried out by the combination of a thermometric capacitive DAC and a multiple threshold generating preamplifier succeeded by a latch bank. Capacitive DAC of SAR-1 and SAR-2 stages are made thermometric for the same reason as in flash, in order to avoid a decoder. C-2C structure would be another option; however, simulations have shown that for the same linearity, C-2C structure requires more area than thermometric structure.

3.2.3 Multiple threshold generating preamp

In this solution, a single preamplifier realizes multi-bit per cycle structure, which is able to generate multiple thresholds and a latch bank. Thresholds are inherently generated in the preamplifier by selecting the combination of outputs from a resistive string. Applying a voltage shift to one of the outputs moves the crossing point of the characteristic either to a positive or negative value of the differential input. The shift is simply obtained by collecting the output at a higher point of the resistive string. This output is then sent to the latch together with the reference output of the other branch; and if the resistive string has been accurately designed, the imbalance required to the differential input to make the latch trigger is equivalent to the threshold required.

The multiple threshold generating preamp is presented in Figure 3.5 and generated thresholds are shown through a input DC sweep in Figure 3.6. Considering in coarse conversion stage one of the SAR-1 intervals is chosen where p_{mid} denotes the mid-point of the interval. As shown in Figure 3.1, thresholds of the SAR-1 intervals are placed on $(p_{mid} \pm 2)$, $(p_{mid} \pm 6)$ and $(p_{mid} \pm 10)$ LSBs. Suppose that a threshold of $(p_{mid} + 2)$ LSB is required. In this case, inputs of one of the latches on the succeeding latch bank must be connected to the preamp outputs V_{N0} and V_{P2}. Same principle applies for the rest of thresholds.

Interval width of SAR-1 is $\pm 16\,LSB$ whereas for SAR-2 it is $\pm 4\,LSB$. In addition, thresholds of the SAR-2 must be generated with maximum accuracy. This imposes a lower dynamic range for the SAR-2 preamp, which necessitates two different preamps. However, for two different preamps, offset mismatch can be problematic. Therefore, an improvement has been made on multiple threshold generating preamp, which is shown in Figure 3.7.

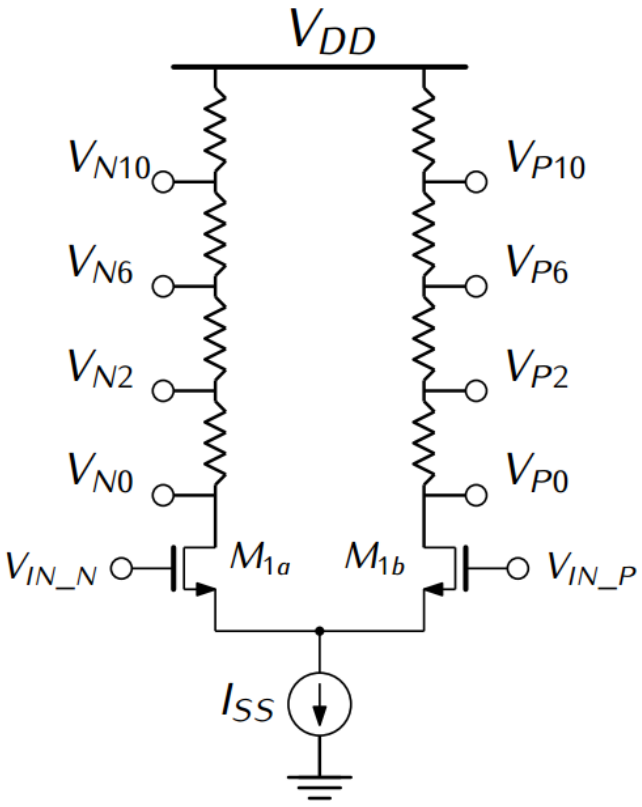

Figure 3.5: Multiple threshold generating preamplifier.

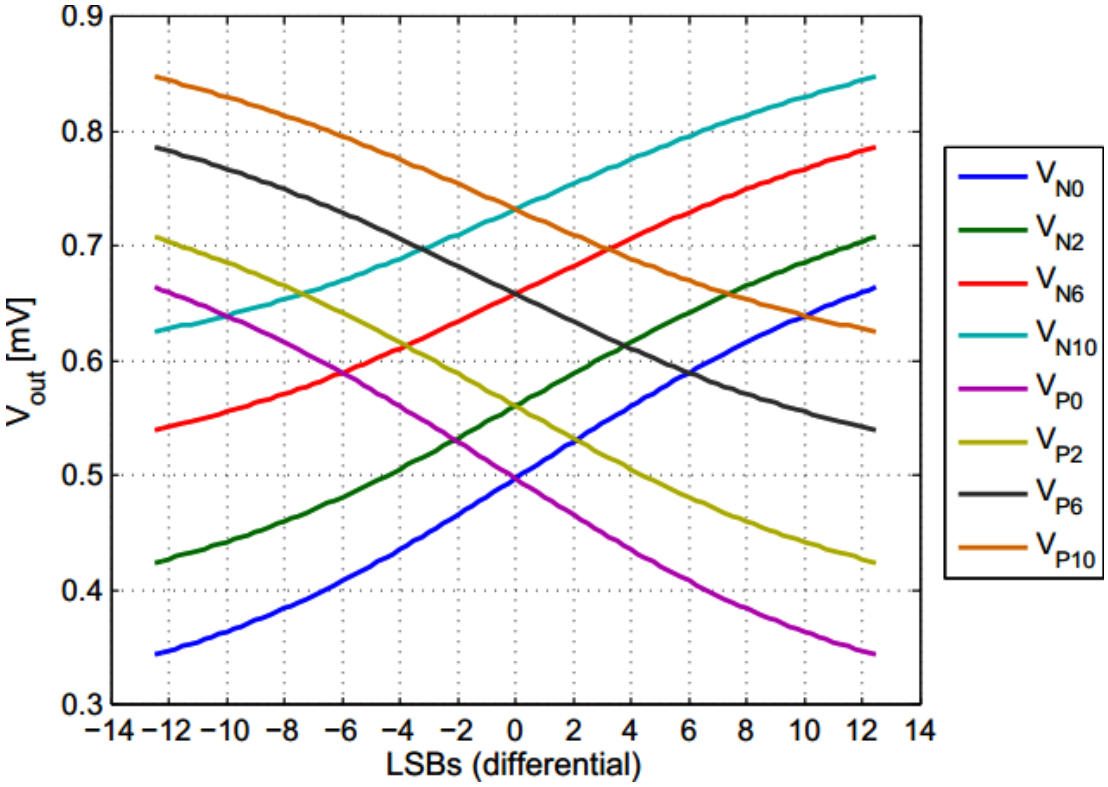

Figure 3.6: Input DC sweep of multiple threshold generating preamplifier.

Here, depending on the switch configuration, one of the resistor string couples is connected to the differential pair whereas the idle string couple is connected to dummy branch. In the case where there is not a dummy branch, nodes of idle resistor string get pulled to V_{DD}. This occupies some time for nodes to settle when the idle string is activated. Hence, dummy branch is employed to eliminate the recovery time of the idle resistor string. This approach is analogous to the approach utilized in current-steering DAC topologies.

Another significant benefit of using a preamp is that the offset of succeeding latches is divided by the gain achieved by the preamplifier when referred to the input.

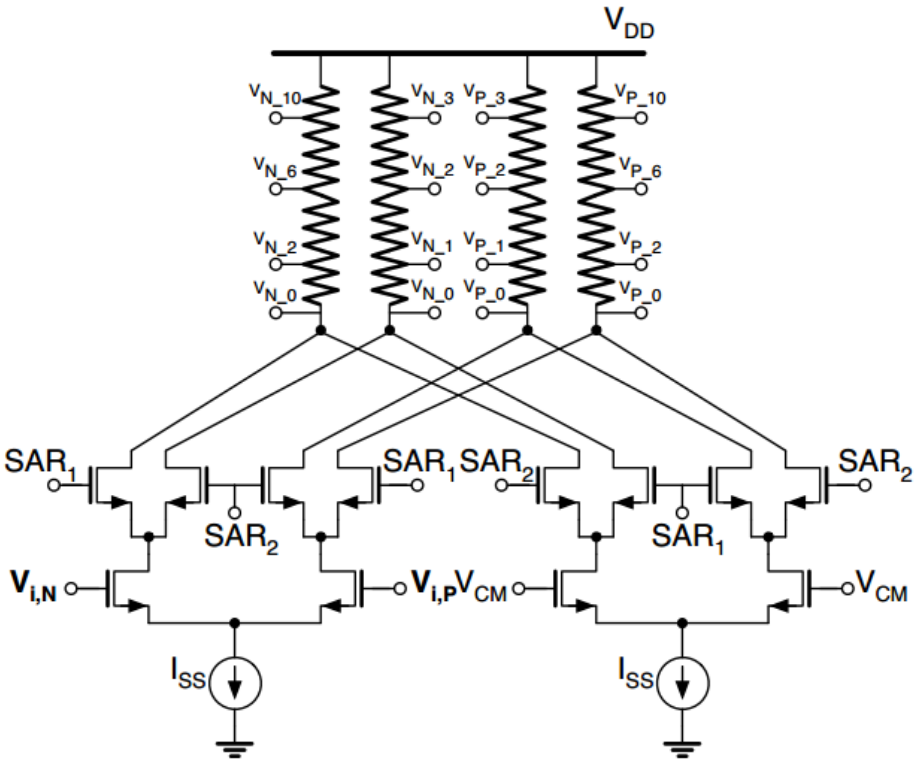

Figure 3.7: Improved multiple threshold generating amplifier.

4. COMPARATORS FOR HIGH SPEED ADCS

Ultra-high-speed data converters are used more and more in modern applications. Ultra wide band is an effective communication method that requires some processing at the receiver side. For this, it is necessary to use data converters with low resolution (3-5 bit) but conversion rate in the 3-5 GS/s range or more. Another application is the wireless USB that transmits data at a rate of 500 Mb/s or more. Ethernet and SERDES interfaces are two other examples of application that need ultra-high-speed data converters. They require ADC with medium resolution and conversion speed that can be as high as 10GS/s. It is expected that in the near future the requests of data conversion will become many ten of GS/s with resolutions in the 8-10 bit range. The data converter architectures for ultra-high speed applications depend on many factors such as technology, supply voltage and consumed power. However, all the solutions rely on the availability of ultra-fast comparator.

This section first analyzes various architectures of very fast comparators and studies features and limits. Then, it discusses techniques for further increase the conversion rate.

4.1 Comparator Architectures

Ultra-high-speed comparators use two possible general architectures, the cascade of a preamplifier and a latch or a simple latch. In the first case the gain of the preamplifier, normally low, reduces the kickback caused by the fast output transition and diminishes the probability of metastability. However, the complexity and the number of nodes in the schematic increase and this, possibly, limit the speed.

For low resolution, ADC the comparator can avoid the preamplifier and it is just made by a latch. Latches can be divided into dynamic and static. The former ones foresee a reset phase so they start the comparison with the output nodes at the same voltage level; while the latter ones are unbalanced during the preamplifier phase thus

increasing drastically the speed. Although being faster, they constantly consume power.

In order to assess the performance implication on the use of preamplifiers, we first analyze dynamic latch structures.

4.1.1 Dynamic latches

High-speed latches are typically based on two architectures: the dynamic sense amplifier [16] and the double tail latch scheme in [17]. There is another more complicated fast solution, the modified sense amplifier [18]. All these architecture are widely used in ADCs presented in [14], [6] and [19] achieving +10 GS/s conversion rate.

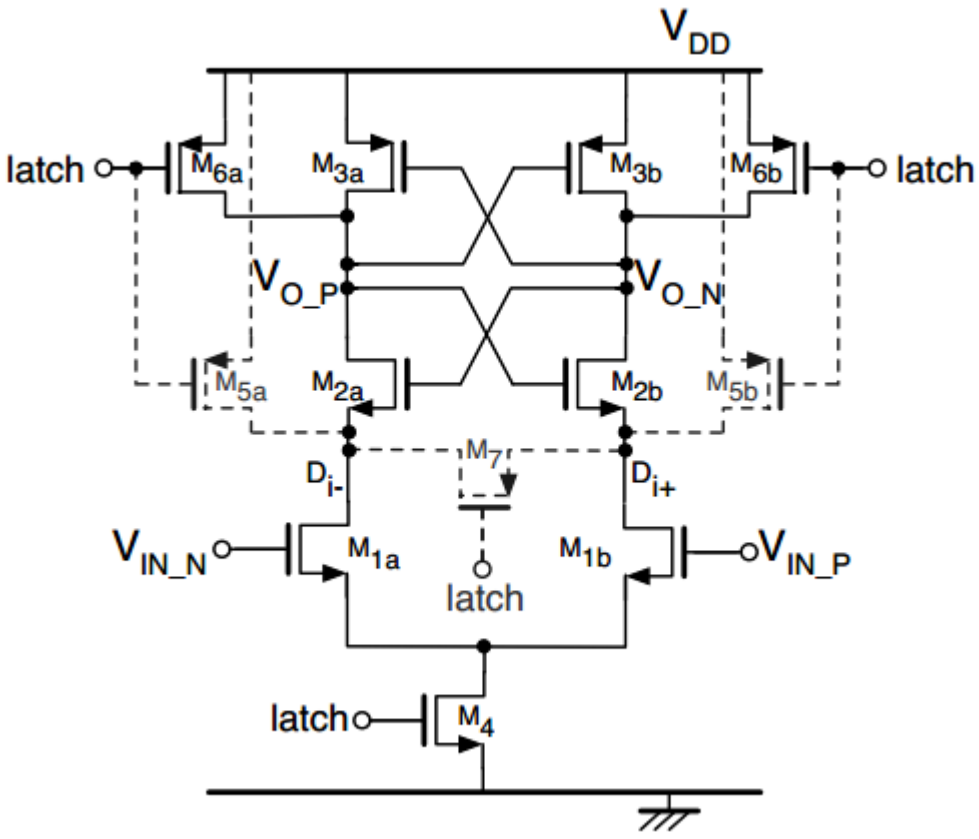

Figure 4.1: Conventional dynamic sense amplifier latch.

Figure 4.1 shows the dynamic sense amplifier latch. The solution is low power because it sinks current from the supply only when regeneration occurs. During the reset phase, output nodes are reset to V_{DD}. The drains of the input pair are either reset

to V_{DD} or shorted together. The former solution is preferred because there is no capacitive coupling between those nodes. Even if they are separated from the outputs by a transistor, the possible reset switches M_7, M_{5a} or M_{5b} degrade speed. The circuit is fast because the input current flows through the sources of the lower regenerative loop without needing to use connections to the output nodes. The rail-to-rail excursion of the drains of the differential pair causes kickback noise. Another possible limit is the used stack of four transistors. This constrains the common mode range of the input signal.

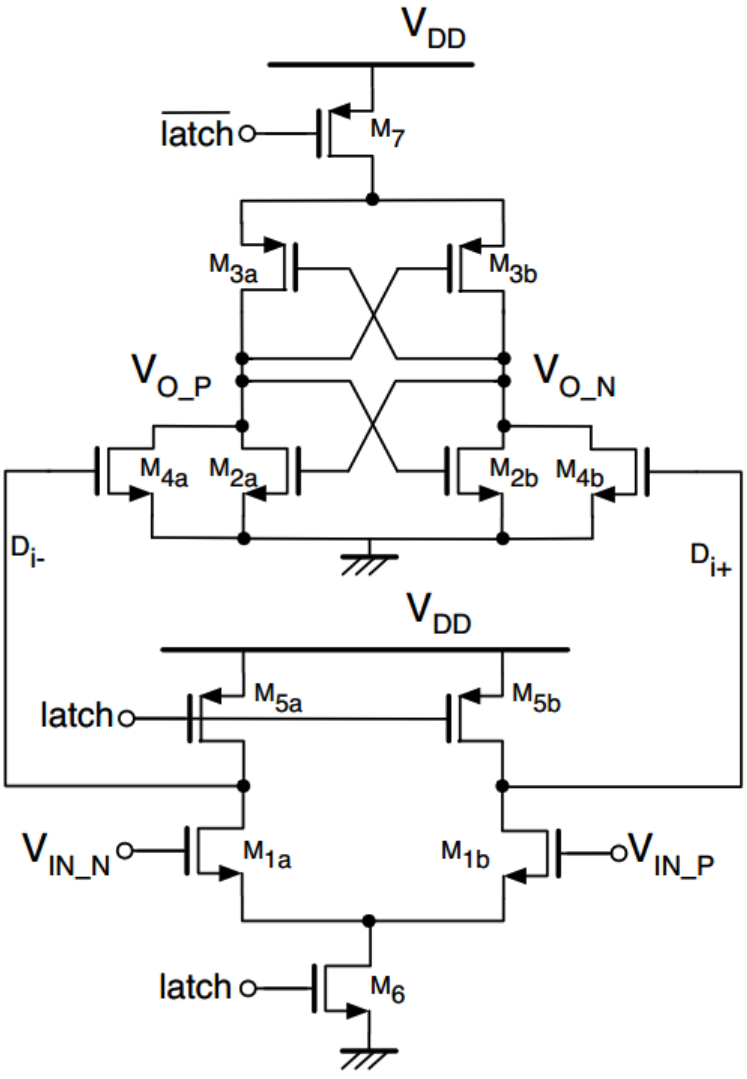

Figure 4.2: Double-tail configuration dynamic latch.

The double-tail dynamic latch configuration in Figure 4.2, reduces the number of transistors in the stack. It uses a double regenerative loop with current injection at the output. The signal current results from the double tail of current made by the pairs

M_{1a} and M_{1b} followed by M_{4a} and M_{4b}. It results in a separation between the input and the output nodes, which reduces the kickback noise. The more effective action of the double tail is contrasted by the extra load established by the drains of M_{4a} and M_{4b}. The balance of the two factors determines an increase or a slowing down of speed.

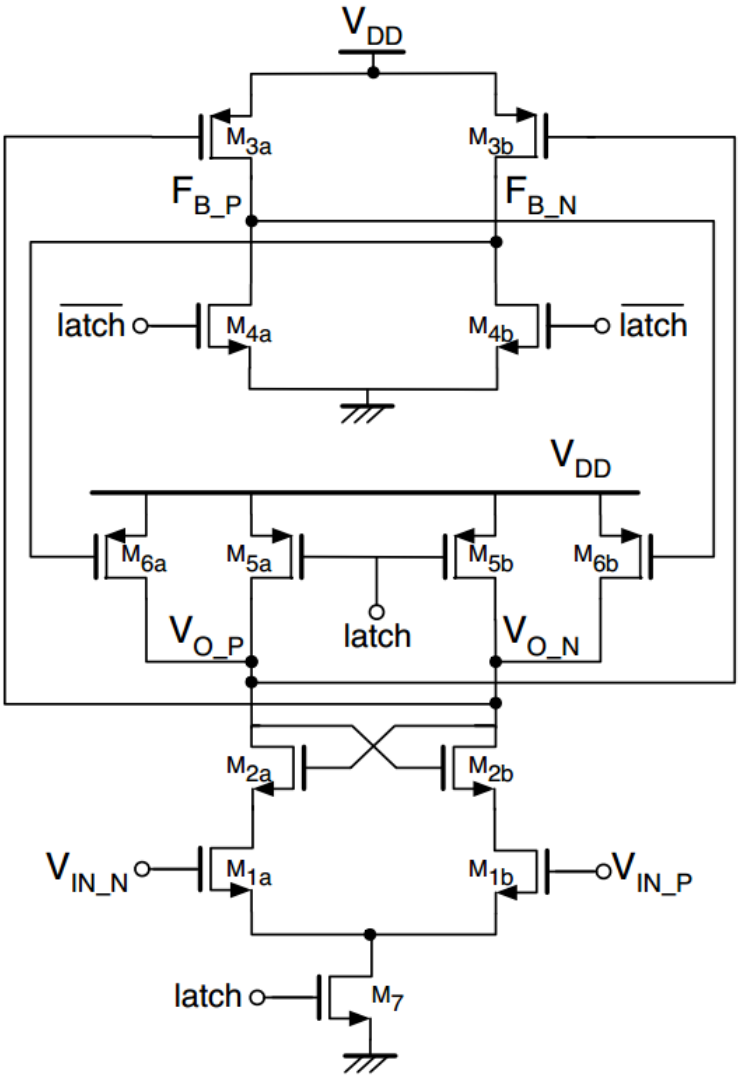

Figure 4.3: Modified dynamic sense amplifier latch.

Figure 4.3 shows a modified sense amplifier latch. It uses an auxiliary p-type latch to activate the p-type latch of the main section. This obtains a rail-to-rail output and increases the equivalent gain of the latch but as we will see shortly, the augmented complexity penalizes the conversion speed.

4.2 Preamplifiers

The speed improvement for larger input signal suggests using a preamplifier in front of the latch. This also reduces glitches caused by the kickback toward the input terminal and attenuates the input referred offset of the latch. The speed of the preamplifier, however, can limit the benefit of pre-amplification. The ADC architectures can distant a given time-slot for the preamp operation and within this time the outputs of the preamp must reach the stationary levels. Unfortunately, this is difficult for sampling rates of ten of GS/s and the actual gain is the one provided by the transient response at the end of the preamp period. For the above reason the preamplifiers in ultra-fast comparators are single stage with very large bandwidth and, consequently, relatively low gain.

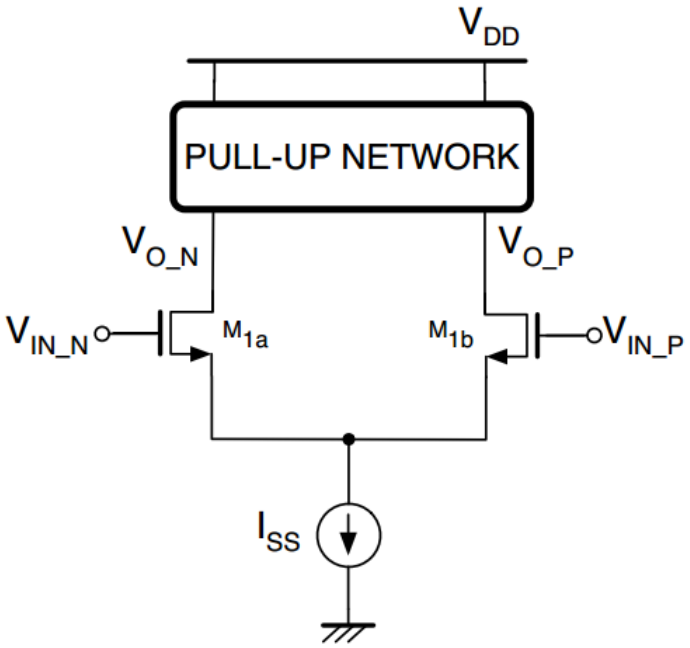

Figure 4.4: Basic preamplifier schematic.

Figure 4.4 shows the generic configuration with n-channel input differential pair. The use of a resistive pull-up network gives a very fast response; other schematics use a diode-connected load, possibly with a current source in parallel, Figure 4.5. Another solution is the one of Figure 4.6 with diode-connected loads and cross-coupled transistors that increases the output resistance [20]. For all the solutions the f_T is given by $g_{m,in}/C_L$, where C_L accounts for the parasitic capacitance at the output of the preamplifier and the input capacitance of the latch. Modern technologies reduce

the load capacitance to few tens of femto Farads; with a $g_{m,in}$ of 0.4 mA/V an f_T of tens GHz is achieved.

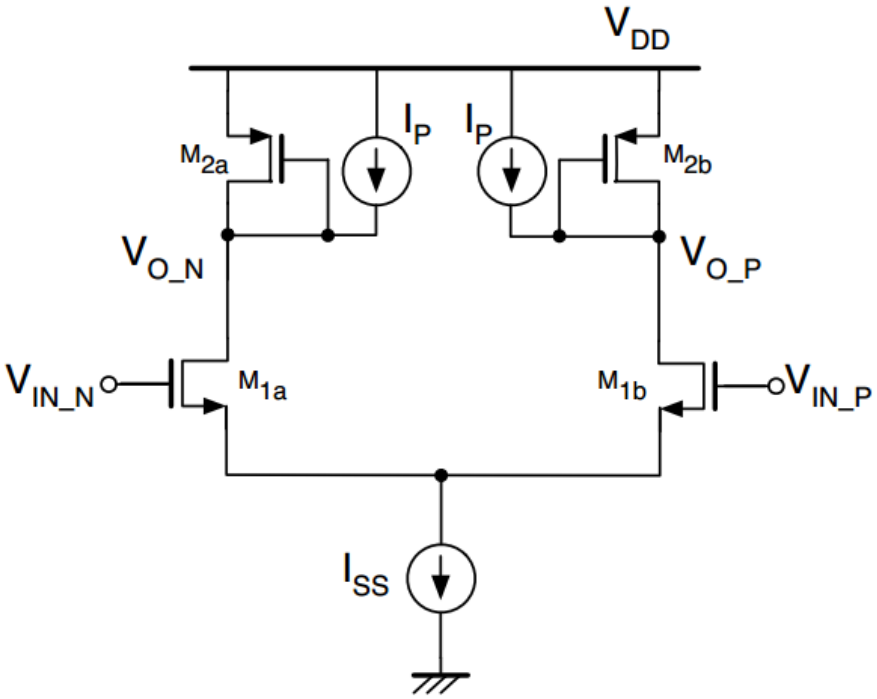

Figure 4.5: Preamplifier with diode-connected load.

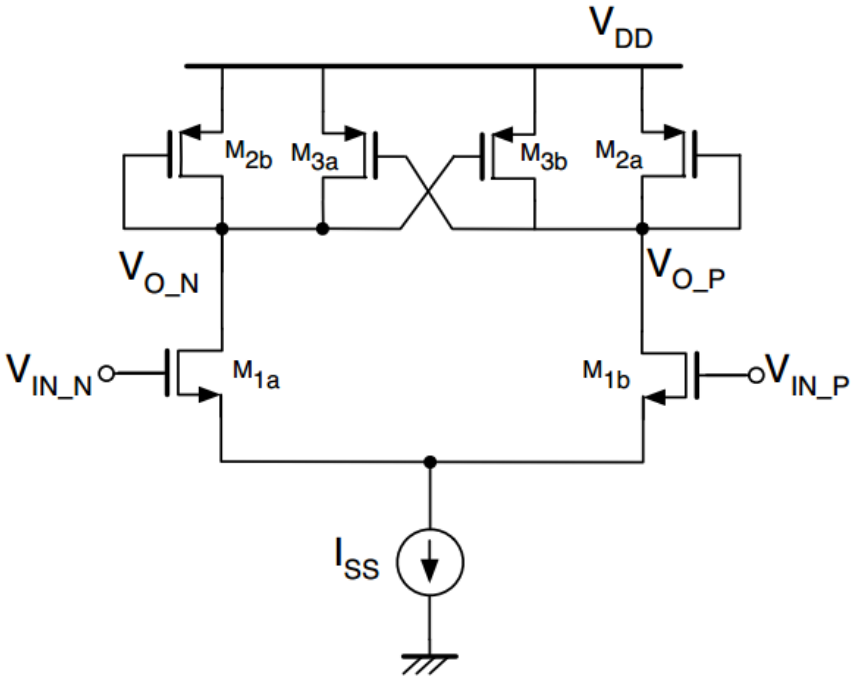

Figure 4.6: Preamplifier with regenerative loop.

All the above solutions work suitably for comparator speeds of few GS/s. The available time allows pre-amplification lasting hundreds of ps. For ultra-high speed (10 GS/s or more) the pre-amplification time is much shorter and the achieved dynamic gain is given in Equation 4.1.

$$A_0 = \frac{g_{m,in} \times T}{C_L} \tag{4.1}$$

Suppose to have $C_L = 20\,fF$ and a preamp time of 25 ps, in order to achieve a gain $A_0 = 4$ it is necessary to use a differential input pair with $g_m = 3.2\,mA/V$ a large value that requires a non-negligible static power.

4.3 Dynamic Latch with Embedded Preamp

The use of a preamplifier for ultra-high speed comparator is problematic due to reasons stated in previous sections. In order to secure the expected benefit it is necessary to use a preamp with a good dynamic gain. The parasitic capacitances of the preamplifier are normally dominated by the input transistors of the latch whose aspect ratio must be chosen large. A comparison of the input stage of a preamp and the input of the sense amplifier latch show that the circuits are equal. The difference is in the role of the transistor connected to the common sources. In one case, it is a current source in the other is a switch. This suggests merging the two functions to obtain the circuit of Figure 4.7. The dynamic latch integrates the pre-amplification function into the latch itself. Following sections explain the advantages of this architecture over the conventional sense amplifier.

4.3.1 Speed

The latch with embedded preamp, works in the same way as the conventional sense amplifier latch in the latch phase. In the reset phase, the current I_{SS} flows into the pair M_{1a}, M_{1b} while transistors M_{2a}, M_{2b} are diode connected by the reset. The result is a static amplification of the input signal equal to the square root of the aspect ratios of input transistors and diode connected load. The parasitic capacitance is significantly reduced because it is only due to the one at nodes D_{i+} and D_{i-} . This increases the speed of the comparator with respect to an equivalent latch preceded by a preamp.

In conventional sense amplifier, reset time depends on the output load and the sizes of the reset switches. In latch with embedded preamp, employed tail current source pulls down the output nodes in reset phase which opposes the action of reset switches. This effect gets stronger with the higher input common-mode voltage (for PMOS input comparators, lower common-mode voltage) since the current of tail current source increases due to the channel length modulation. Therefore, if a large input common-mode is required, it is necessary to employ bigger reset transistors, which loads the output and penalizes the regeneration time, as well as maximum clock frequency.

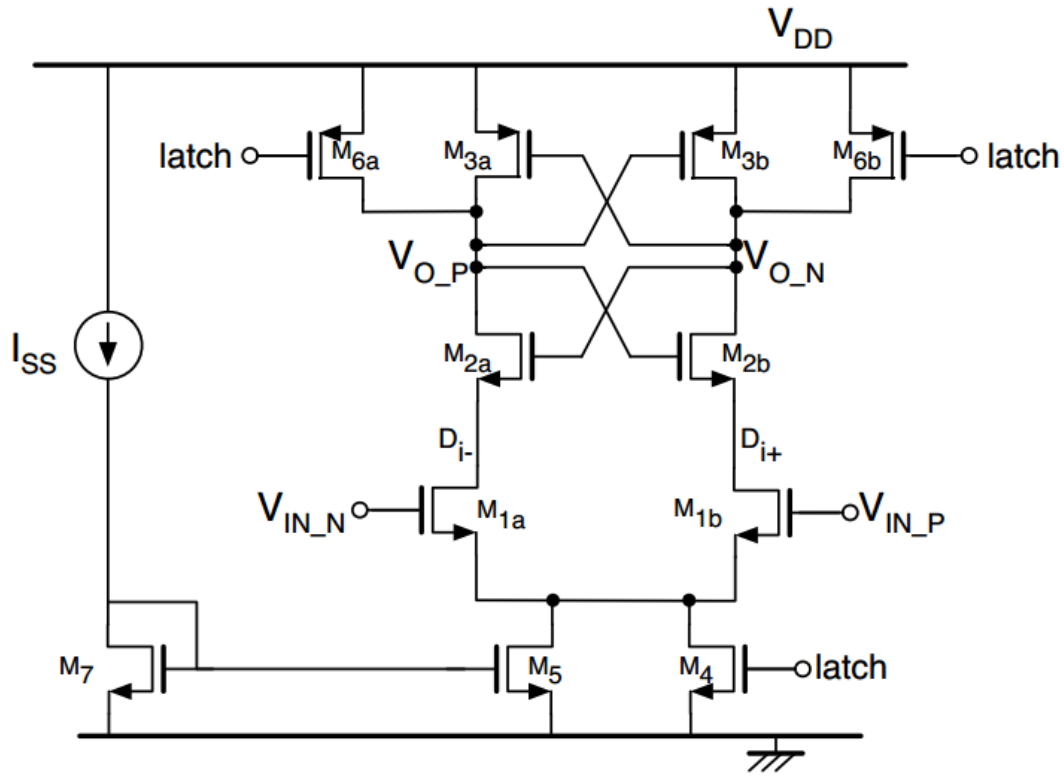

Figure 4.7: Proposed latch with embedded preamp.

4.3.2 Offset

Offset is one of the most critical design criteria of the comparators since it directly affects the yield and accuracy of the design. Two kinds of offset are present in the comparator structures; static offset and dynamic offset.

Static offset has both random and systematic nature. Random component is mainly due to the mismatch of transistors. As stated in [21], mismatch is inversely

proportional to the area of the transistors. Therefore, by using large transistors, static offset of the comparators can be reduced. However, this approach increases node capacitances and has two main disadvantages in return which are reduction in speed and increase in power consumption.

According to the analysis performed in [22] for conventional sense amplifier, "there is a significant influence of V_{INDC} on the yield" and "the yield increases inversely to V_{INDC}", where V_{INDC} represents the input common mode voltage. This can be explained on the structure shown in Figure 4.1 as follows: Lower V_{INDC} is equal to the lower drain current I_o of the switch transistor M_4. Initial voltage difference of outputs V_{OP} and V_{ON} is defined for the instant when one of M_{3a} or M_{3b} turns on. V_O is formulated in [22] as:

$$V_O = V_{thp} \sqrt{\frac{8\beta}{I_O}}\, \Delta V_{IN} \tag{4.2}$$

Therefore the initial voltage difference V_O increases with lower V_{INDC}. Higher V_O makes cross-coupled inverters less likely to make an error in the presence of mismatches. In this way, yield increases hence offset decreases.

Dynamic offset in a latch mainly stems from load capacitor mismatch. According to the analysis in [23], dynamic offset is given by the Equation 4.3. V_{OC0} denotes the initial common-mode of the outputs whereas V_S denotes the switching voltage of the inverters present in the regenerative loop of the comparator. According to the equation, dynamic offset can be reduced either by minimizing $(V_{OC0} - V_S)$ or minimizing ΔC_L. Since in the state-of-the-art comparators V_{OC0} is being either VDD or GND, ΔC_L mainly a systematic error and can be minimized by careful layout.

$$V_{OS,dynamic} = \frac{1}{2}\frac{\Delta C_L}{C_L}(V_{OC0} - V_S) \tag{4.3}$$

4.3.3 Kickback noise

Comparators are non-linear circuit elements and they give rail-to-rail outputs VDD or GND depending on the polarity of differential input signal. These rail-to-rail voltage swings on the nodes of a comparator get coupled through the parasitic

capacitances to the input nodes of the comparators. Charge variations on the input nodes of comparator, combined with non-zero output impedance of preceding stage, causes disturbances on those nodes. This effect is called kickback noise. Kickback noise can be problematic for flash ADCs, since it may disturb the reference voltages on resistor string.

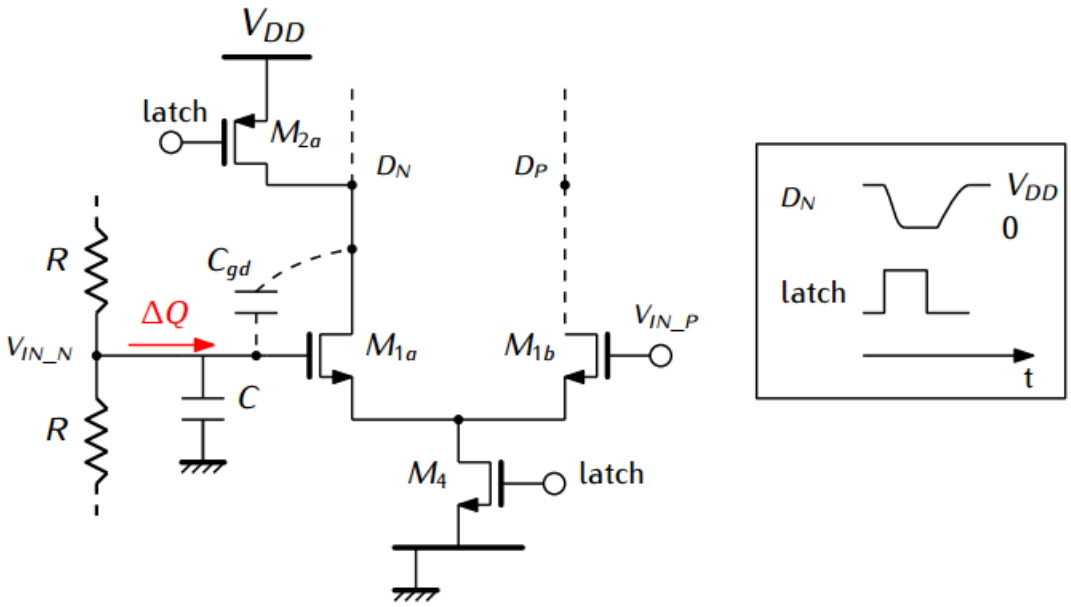

Figure 4.8: Kickback noise mechanism in conventional sense amplifier latch.

Power consumption is a major concern in modern electronic systems, therefore majority of state-of-the-art ADCs use dynamic latched comparators that are superior to the static and Class-AB latched comparators in terms of power consumption. However, as stated in [24], dynamic latched comparators generate more kickback noise, compared to static and class-AB counterparts. Kickback noise generation is qualitatively explained for the conventional dynamic sense amplifier \cite{arm} with a resistor ladder connected to one of the inputs. Figure 4.8 depicts the mechanism. When "latch" signal is low, latch is in reset mode where nodes D_P and D_N are pulled to V_{DD} from 0 V. In this phase as well kickback occurs but if there is enough time for references to go back their normal value, is not problematic. When "latch" goes high, M_4 turns on and pulls D_P and D_N to ground. This rail-to-rail voltage swings are coupled to relative input nodes via C_{gd} of input transistors. This charge variation creates a current, which passes through the resistors on the ladder and disturbs the input.

Another source of charge variation is the changing operation regime of input transistors. Charge variation can be reduced by using smaller transistors. However, this approach contradicts the one used for decreasing the static offset and therefore creates a trade-off between kickback noise and offset.

4.3.4 Power consumption

Power consumption is a major concern in ADC design. Considering that each ADC has at least one comparator, power efficiency of the comparator becomes important, especially for architectures such as flash ADC, which has several comparators.

Latches can be divided in three main categories in terms of their current consumption characteristic. In static latches, there is constant current consumption, which makes them power inefficient. In class-AB latches, there is static power consumption for input pair however; in latch part, current consumption is present only in regeneration phase. For dynamic latches, there is no static power consumption and power is only consumed in regeneration phase, which makes these structures the most power efficient among three.

4.4 Simulation Results

A comparative transistor level simulation of latches outlines features and benefits. For that it is necessary to have a definition of the switching time. As known, for any latch the output voltages start from the value established by the reset and immediately after outputs move in the same direction (down, if the reset is toward VDD) until the positive feedback separates them. One output returns back and the other switches to a complementary level, as Figure 4.9 shows. The threshold of the inverters used after the latch is critical for high-speed operation. If the threshold of the inverter is too low, a long delay occurs. If it is too high, a glitch in the digital signal occurs. In order to avoid glitches it is therefore necessary to set the threshold below V_{min} by a defined margin. Here we use 100mV. The resulting definition of switching time differs from the one conventionally used being specific for ultra-high-speed comparators. Latch regeneration time results in the following section are calculated according to that definition.

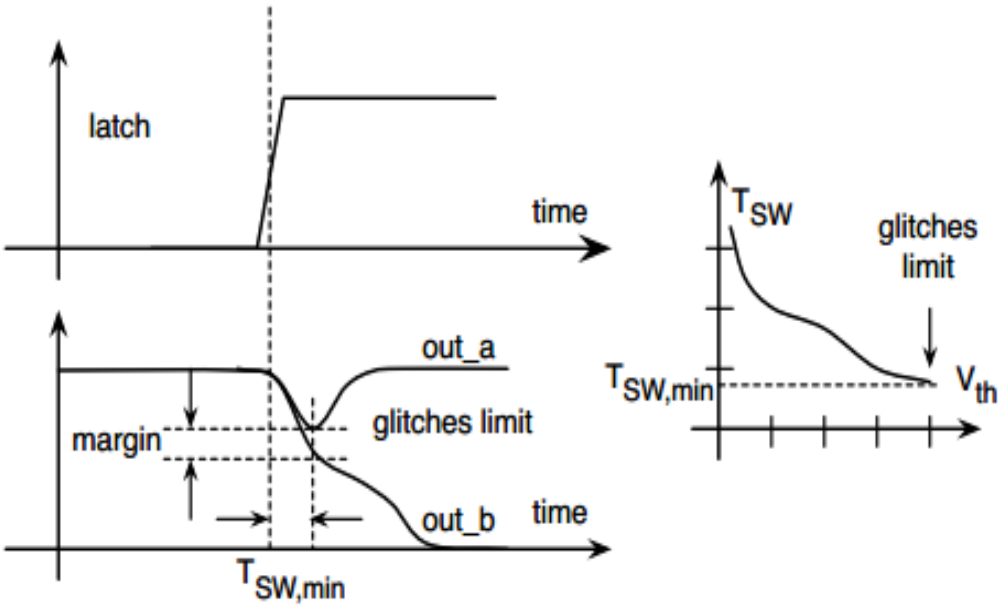

Figure 4.9: Waveforms at the output of the latch for switching time definition.

Most of the times comparator stage is succeeded by an inverter or buffer made by tapered inverter chain. In this case, the load of the comparator is a minimum size inverter to avoid excessive loading. Therefore in the simulations, a minimum size inverter is whose C_{in} is approximately equal to 0.6 pF added to outputs to model the load. Transistor sizes of the comparators are optimized for speed.

4.4.1 Speed

Firstly, regeneration time of the conventional comparator architectures are compared for various differential input voltages. Results are given in Figure 4.10. Note that conventional sense amplifier is superior to the other conventional architectures in terms of regeneration time.

Secondly, effect of coupling capacitance between the output nodes is observed in order to quantify the dependence of regeneration time to the layout effects. For this purpose, various capacitors are added between outputs. Note that according to the results given in Figure 4.11, conventional sense amplifier is more sensitive to parasitics than the double tail latch. This is due to the first stage of the double tail, which maintains the speed advantage while the second stage suffers from parasitics.

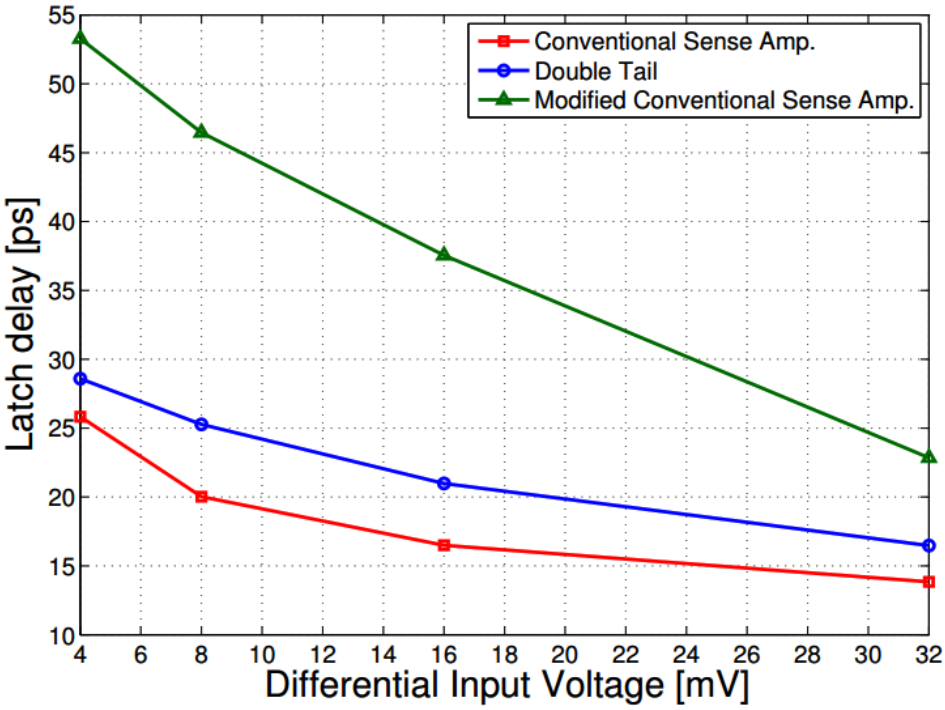

Figure 4.10: Latch regeneration time comparison of conventional comparator architectures.

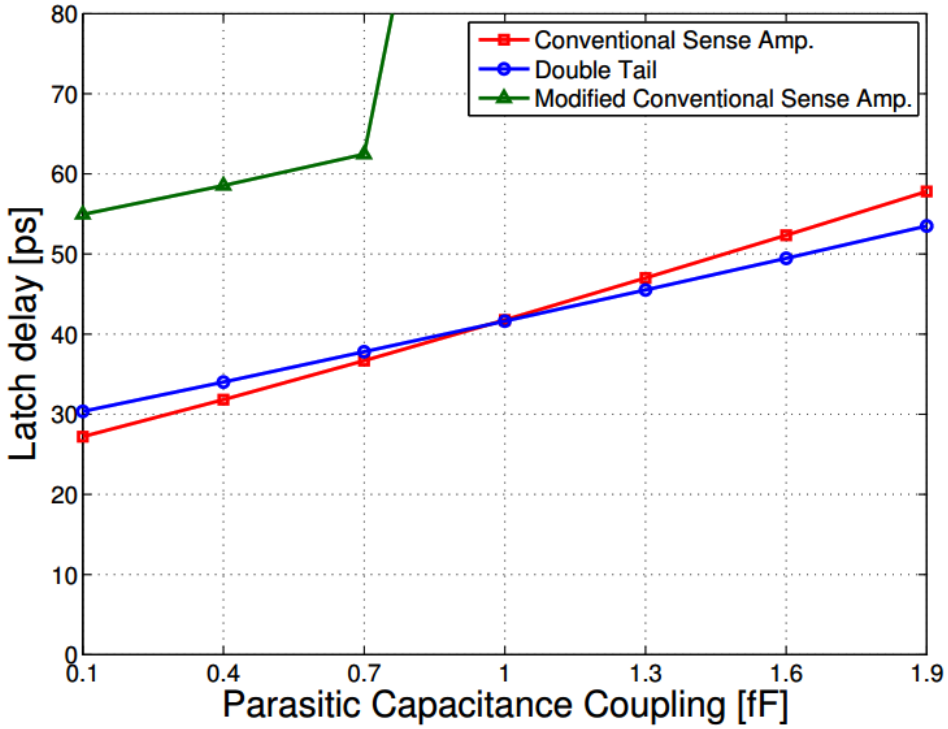

Figure 4.11: Latch regeneration time comparison of conventional comparator architectures in case of capacitive coupling between outputs.

Thirdly, the proposed solution was compared to a sense amplifier latch and the same sense amplifier latch with in front a preamplifier. The tail current used for the pre-amplifier and the proposed solution is the same. Figure 4.12 shows the results. The proposed solution shows an effective advantage in terms of speed. This is due to two main reasons. First, the preamplifier is embedded into the latch and this does not increase the parasitic capacitance that limit the dynamic gain. Second, the comparator starts the latch phase with its outputs already unbalanced like in the case of a static class AB comparator.

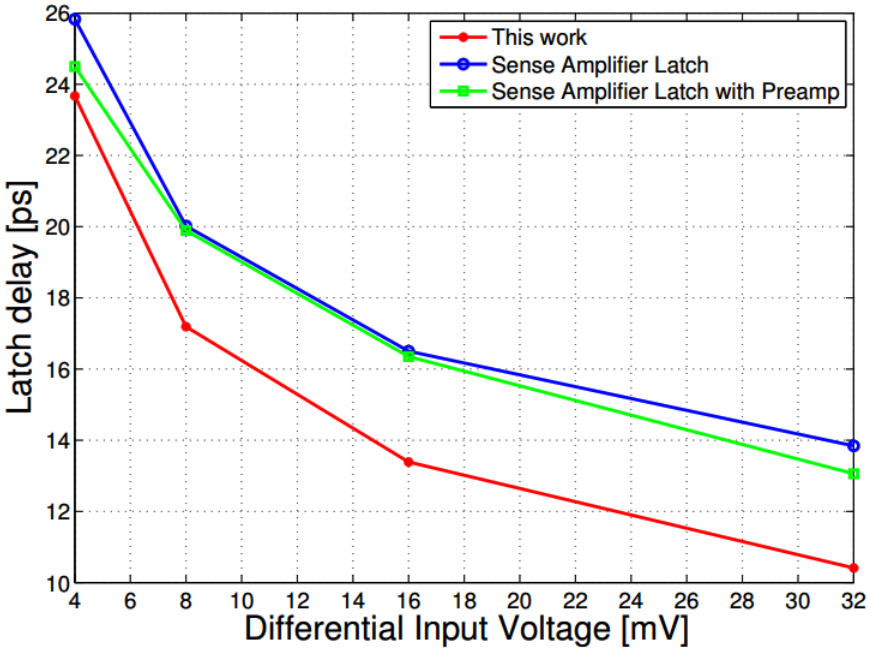

Figure 4.12: Latch time comparison of proposed latch, SA latch and SA latch preceded by preamp.

4.4.2 Offset

According to the analysis of Section 4.3.2 , if the drain current I_o of latch enable transistor M_4 in Figure 4.1 is decreased, the offset performance improves. It can be deduced from the analysis that proposed latch with embedded preamp benefits from the decrease in I_o with the help of auxiliary current source M_5 in Figure 4.7. In latch with embedded preamp structure, a fraction of dynamic drain current of input differential pair transistors M_{1a} and M_{1b} is provided by the static tail current source. Hence when the latch signal goes high, a smaller dynamic current I_o is sinked by M_4.

This points an improvement in systematic static offset performance for latch with embedded preamp over the conventional counterpart.

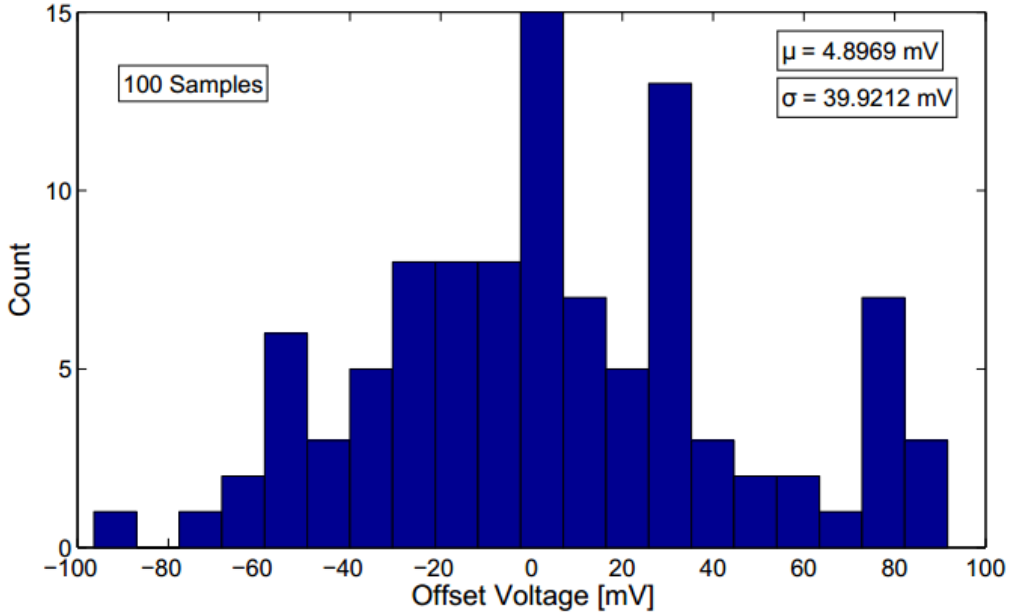

Figure 4.13: Histogram of offset voltage for conventional sense amplifier architecture.

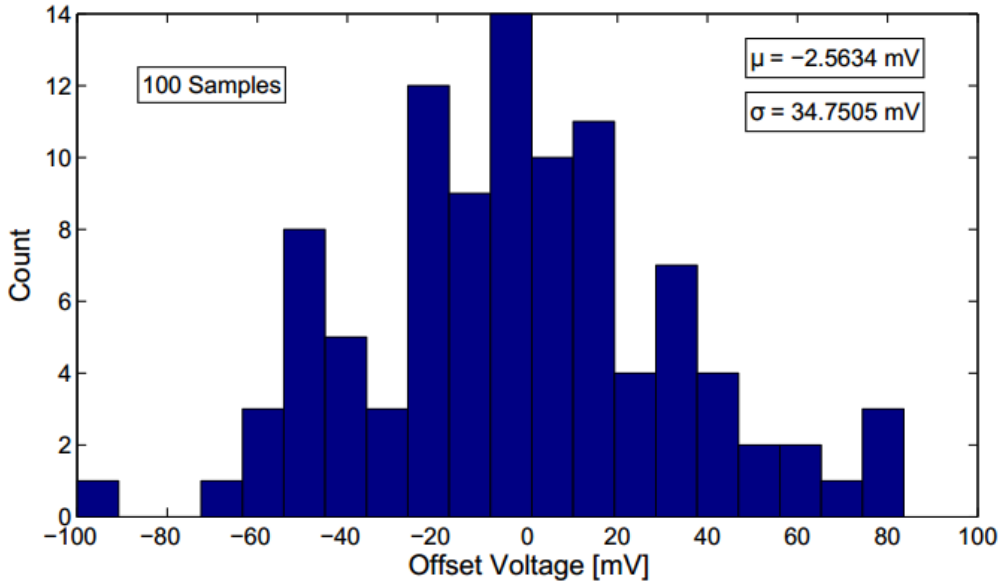

Figure 4.14: Histogram of offset voltage for proposed architecture.

In order to prove the aforementioned improvement, Monte-Carlo simulations run on speed optimized latch schematics. In order to see the worst case in terms of input common mode V_{INDC} picked as 900 mV. A slow input differential voltage ramp signal between -100 mV and +100 mV is applied to the inputs of latches. Results are

shown in Figures 4.13, 4.14 and 4.15. Note that σ_{os} of proposed latch with embedded preamp is approximately 5 mV less than conventional sense amplifier. For supply voltage of V_{DD} = 1 V and 8-bit ADC, this value is more than an LSB which is equal to 3.9 mV. This proves the significant advantage of proposed latch with embedded preamp in terms of offset.

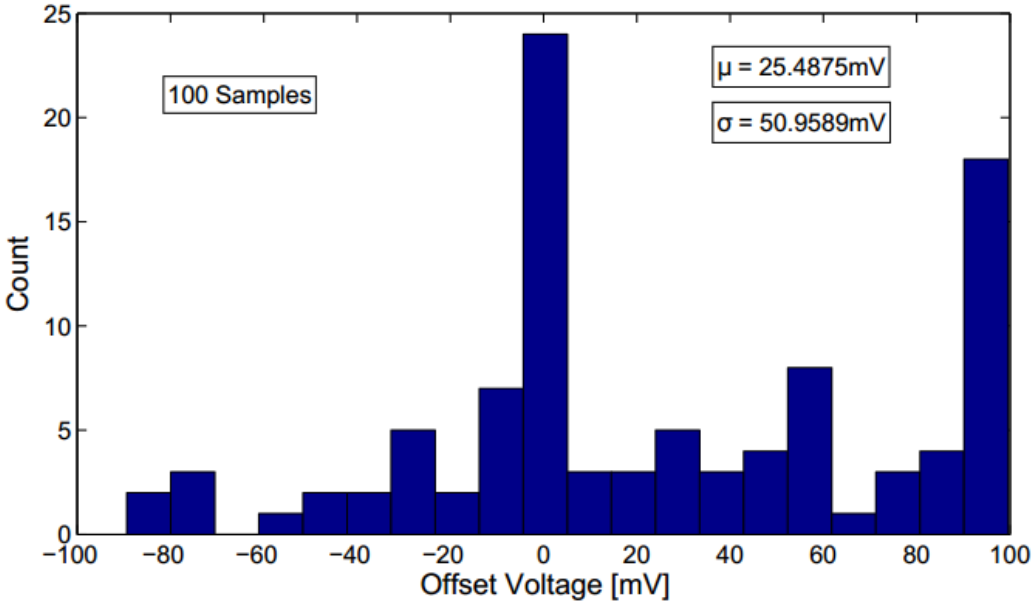

Figure 4.15: Histogram of offset voltage for double tail architecture.

4.4.3 Kickback noise

In Section 4.3.3 , kickback noise mechanism for conventional dynamic sense amplifier is explained. Proposed latch with embedded preamp designed based on this structure therefore it is convenient to compare the kickback noise performance based on conventional architecture. Main contributor to the kickback noise in conventional architecture is rail-to-rail swing of input transistor drain nodes. In latch with embedded preamp, reset transistors on drain nodes of input differential pair are omitted. In reset phase, these nodes are pulled down from V_{DD} in proportion to the tail current and the impedance seen looking in the source of cross-coupled NMOS transistors. Therefore, when "latch" signal goes high, a voltage swing less than V_{DD} is expected.

As shown in Figure 4.16, input differential pair drain nodes of proposed latch experience smaller voltage swing, in this case for V_{CM} = 0.5 V it is 700 mV. Then an

improvement in kickback noise performance is expected in this architecture. In order to prove the point, test bench shown in Figure 4.17 is utilized. Input V_{IN} is sampled by an ideal Verilog-A sample and hold, applied to the comparators which are operated by a 1 GHz clock and Vref<3> node is observed. Middle of the resistor string is chosen because it is where the equivalent resistance is higher so that the effects of the kickback can be seen clearly.

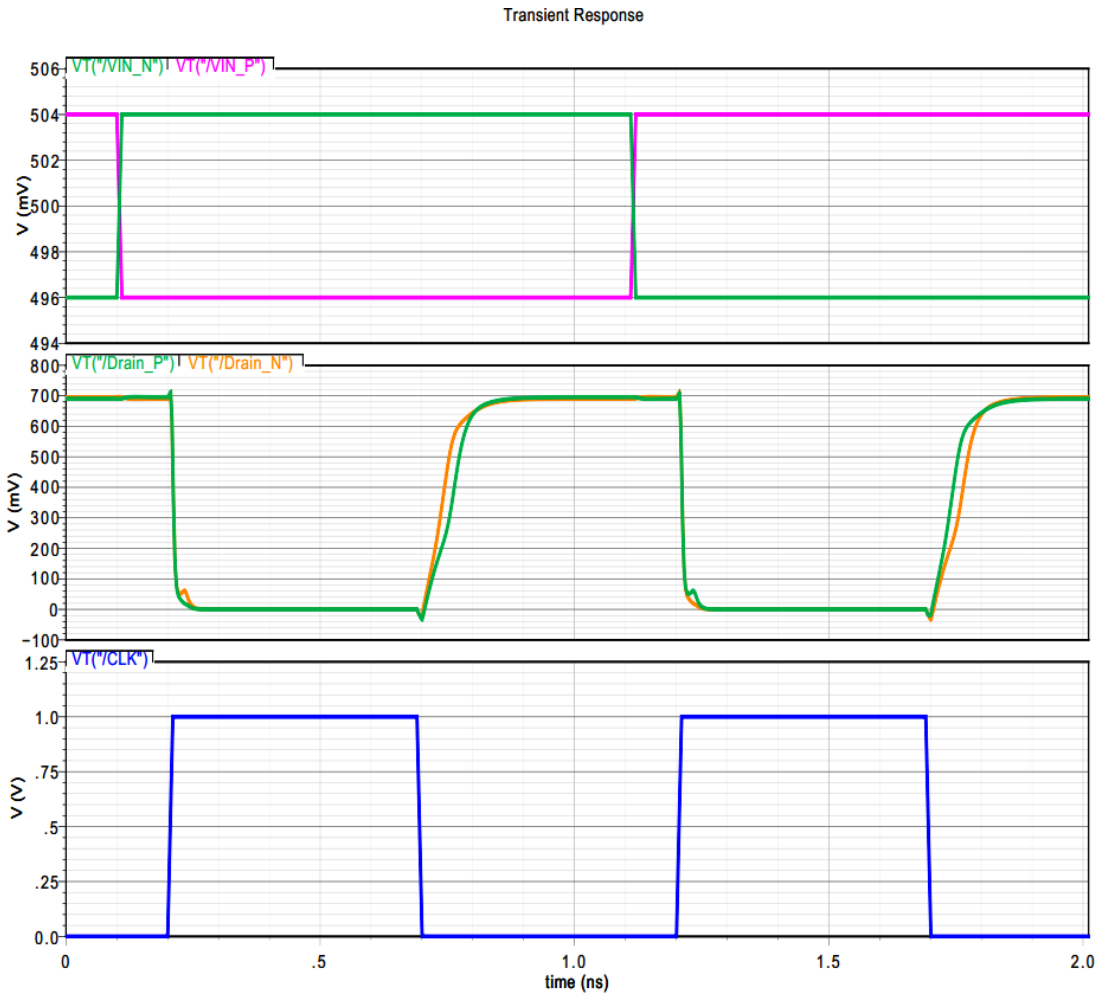

Figure 4.16: Transients of input differential pair drain nodes for proposed latch.

Simulations are performed for R = 100 Ω and R = 1 kΩ. Simulation results are presented in Figure 4.18 and Figure 4.19 respectively. Note that for R = 100 Ω, kickback noise is 40 mV less than conventional dynamic latch sense amplifier (ARM) in proposed latch with embedded preamp (Proposed). Difference goes up to 100 mV for R = 1 kΩ. Simulations have proved significant kickback noise reduction in proposed architecture.

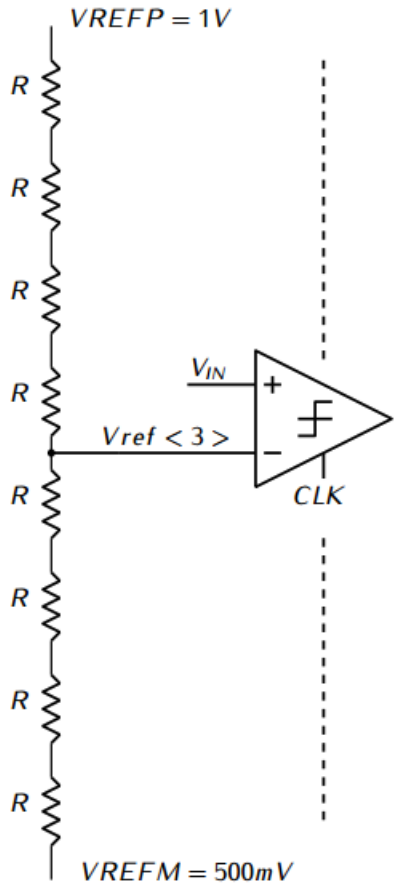

Figure 4.17: Test bench used in kickback noise simulations.

4.4.4 Power consumption

Power consumption is simulated for V_{INDC} = 500 mV, V_{INdif}= 4 mV and f_{clk} = 1 GHz. RMS power consumption of architectures are shown in Table 4.1. Note that, proposed latch with embedded preamp consumes 10% less than conventional dynamic sense amplifier latch even in the presence of static power consumption by tail current source and its mirror. Since the speed-optimized sizes are approximately equal for both architectures (reset switches in proposed architecture are larger), this improvement is due to two factors. First, the drain nodes of input differential pair transistors are not loaded since those reset transistors are omitted. Second, again, these nodes experience lower voltage swings which requires less current to discharge these nodes in regeneration phase.

Power consumption is simulated for V_{INDC} = 1 V too. Results have shown in Table 4.1. Note that the difference between the conventional sense amplifier and proposed latch decreased. This is due to the channel-length modulation which increases the

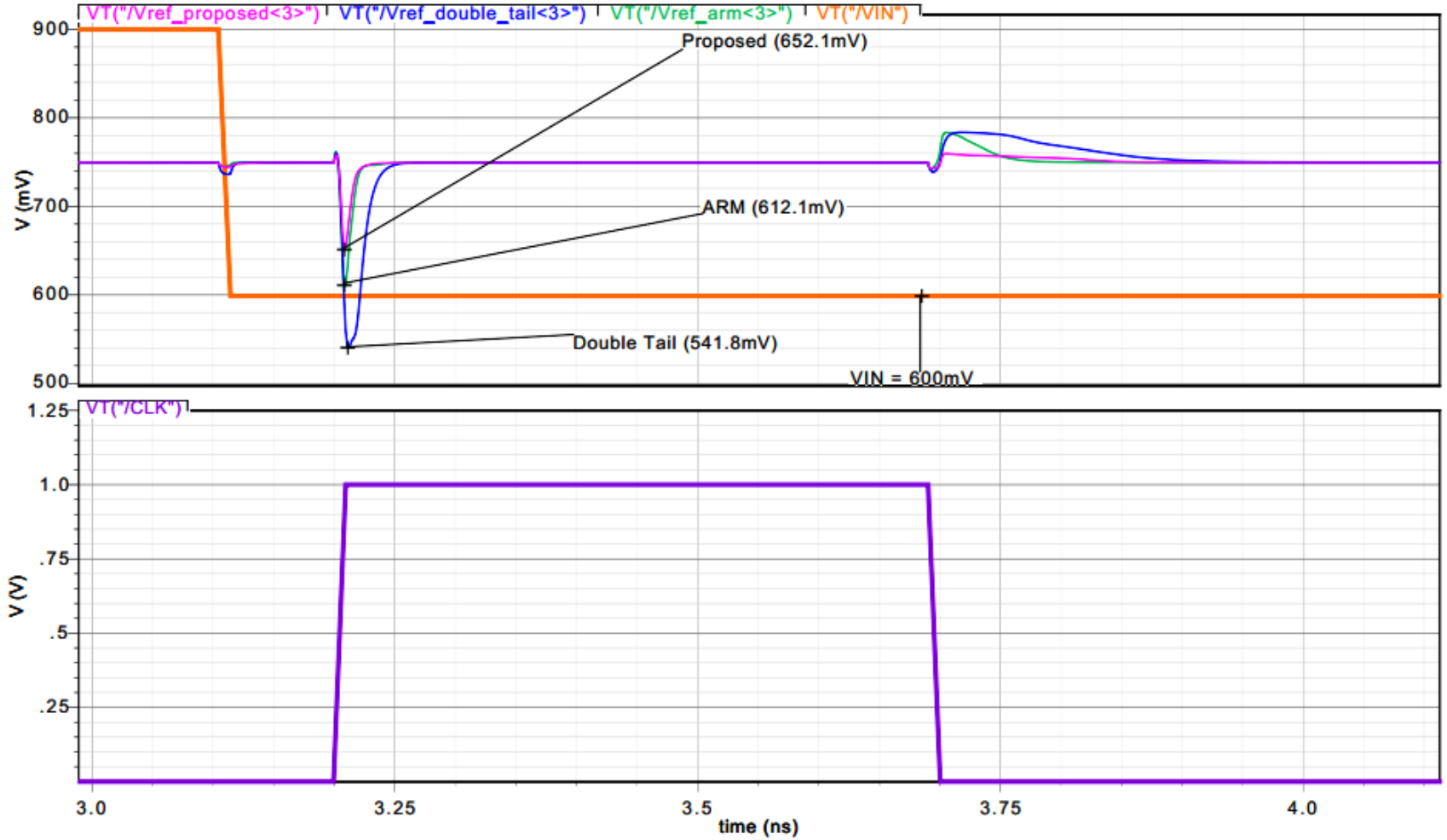

Figure 4.18: Kickback noise for reference ladder unit resistance of 100 Ω.

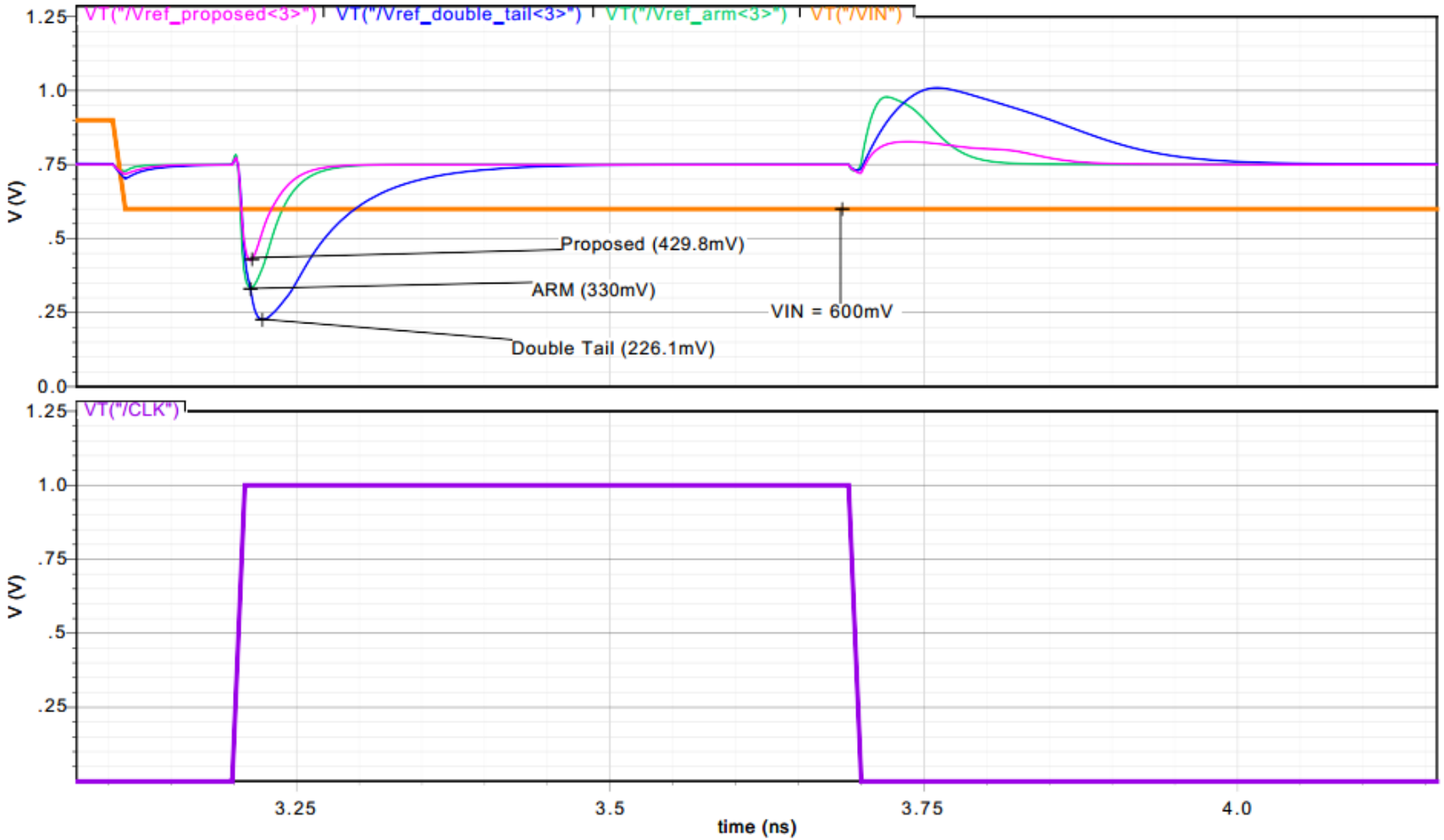

Figure 4.19: Kickback noise for reference ladder unit resistance of 1 kΩ.

static power consumption of the tail current source of proposed latch when the input-common mode increases. However, proposed latch still has a 5% of power consumption advantage over the conventional counterpart.

Table 4.1: RMS power consumption of the comparator architectures.

	Conventional Sense Amp.	Double Tail Latch	Proposed Latch
$V_{cm} = 0.5\ V$	35.44 µW	107.2 µW	31.46 µW
$V_{cm} = 1\ V$	41.9 µW	111.4 µW	39.9 µW

5. DESIGN, LAYOUT AND CHARACTERIZATION OF CIRCUIT BLOCKS FOR THE SINGLE CHANNEL ADC

Proposed 8-bit 1 GS/s single channel ADC employs a 14 level flash ADC to resolve first three MSBs and a bootstrapped sampling switch to sample and distribute the input signal to both flash ADC and capacitive DAC with an acceptable linearity imposed by the aggregate resolution of the single channel ADC. Following sections explain the design and layout considerations for bootstrapped sampling switch and flash ADC. In order to prove the validity of considerations, blocks are characterized through various simulations.

5.1 Design of the Bootstrapped Sampling Switch

Sampling switches are one of the most important circuit blocks in an ADC since the signal is fed into the ADC through them. For architectures such as flash ADC, input can be sampled by the comparators at the conversion instant. Therefore, sample and hold circuit may be omitted. However, this approach is not preferable since it makes clock skew between comparators critical. In order to avoid a design effort for the mitigation of clock skew in flash ADC a sampling circuit is employed.

Two of the important performance metrics of a sampling circuit are charge injection and tracking mode non-linearity. Charge injection is a phenomenon which occurs due to the division of channel charge between the source and drain terminal of the switch when it turns off. Since channel charge is proportional to gate-source voltage, amount of charge injection is signal dependent. Tracking mode non-linearity stems from the dependency of on resistance of switch to input voltage. Signal-dependent nature of both phenomenon makes them difficult to correct and significantly limits the performance of the switch.

Bootstrapping is a technique, which ideally removes the signal dependency of both issues. Main principle of bootstrapping is depicted in Figure 5.1 [25]. In the first clock phase (Phase 1) the switch is off and the offset capacitor C_{boot} is charged to V_{DD}. In the second phase (Phase 2) offset capacitor is connected between input and

gate terminals of the switch which ideally makes $V_{GS} = V_{DD}$ at all times. This in turn removes signal dependency of charge injection and keeps on resistance of switch constant for all inputs.

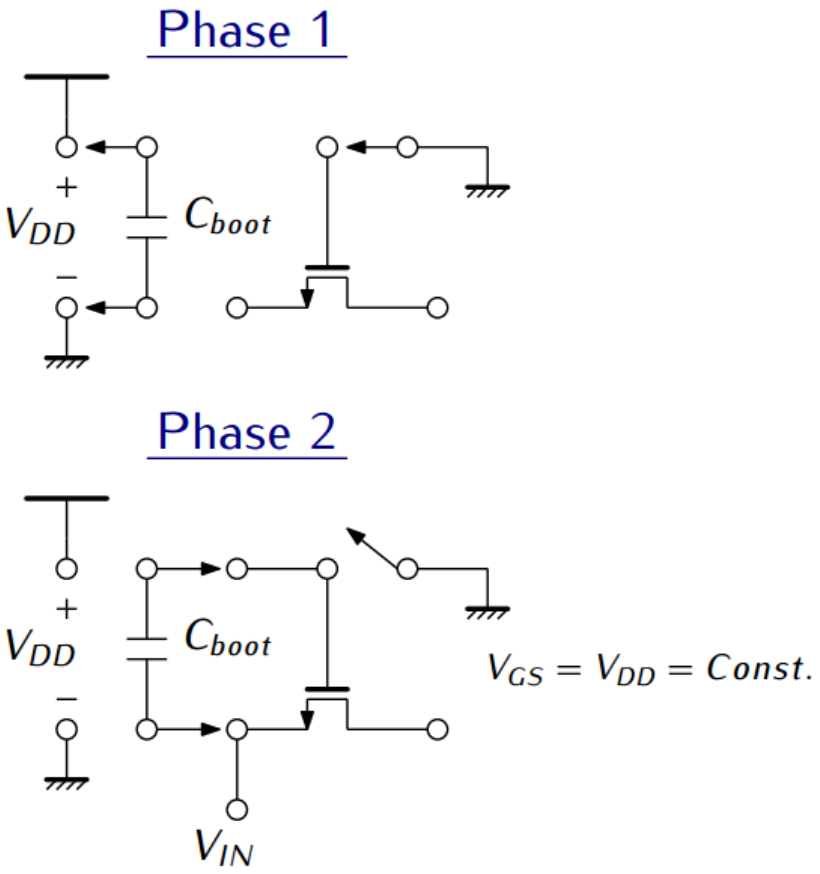

Figure 5.1: Bootstrapping principle.

A conventional bootstrap circuit is shown in Figure 5.2 [26]. During clock phase $\overline{\emptyset}$ switch is turned off via M_{10}. Bottom plate of offset capacitor C_3 is connected to ground through M_{12} and it is charged to V_{DD} with the help of clock multiplier formed by C_1, C_2, M_1 and M_2. During clock phase $\emptyset$, offset capacitor C_3 is disconnected from ground and clock multiplier and is connected between source and gate terminals of the switch so that gate voltage follows the input voltage with an offset of V_{DD} in track mode.

Conventional bootstrap circuit has two main drawbacks. First, on resistance of the switch has a signal dependent term due to back-gate effect, which reduces the linearity of circuit. Second is the parasitic capacitance at the top plate of the offset capacitor C_3. In Equation 5.1 effect of this parasitic capacitance C_p is formulated[26].

Equation 5.1 shows that the bootstrap voltage diminishes dramatically if C_p becomes large. This in turn gives a tracking bandwidth penalty due to higher R_{on}.

$$V_g = V_s + \frac{C_3}{C_3 + C_p} V_{DD} \tag{5.1}$$

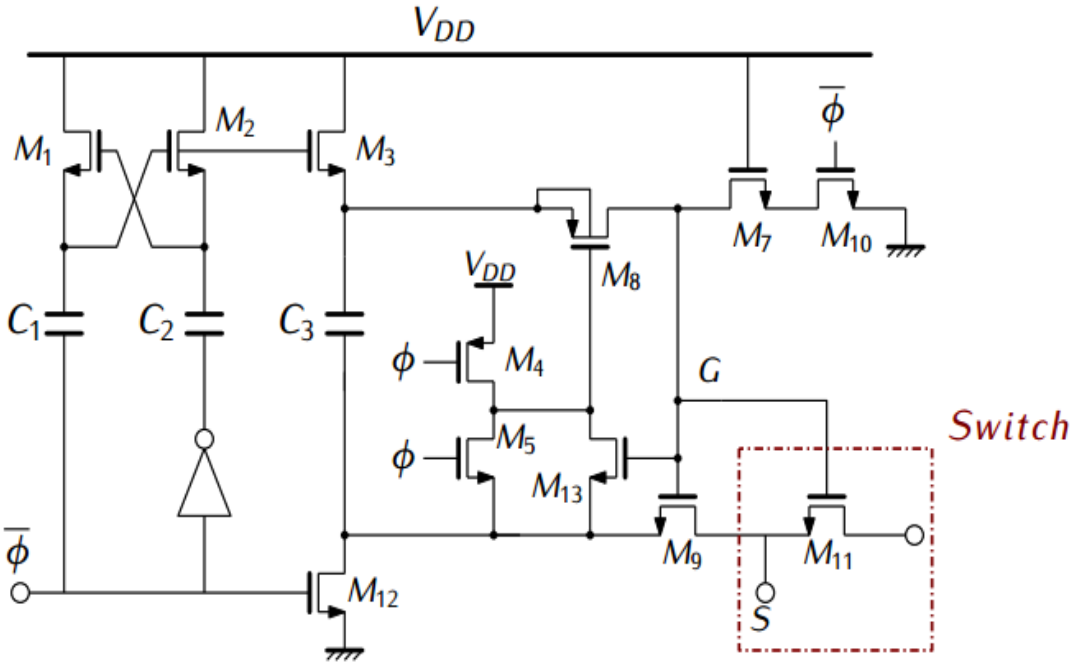

Figure 5.2: Conventional bootstrapped switch circuit [26].

A less complex yet effective bootstrapping circuit is proposed in [27]. Circuit is shown in Figure 5.3. This architecture, too, suffers from aforementioned drawbacks of the conventional bootstrapped switch circuit. However effect of parasitic capacitance is more emphasized since the top plate of capacitor C_{offset} sees well capacitance of both MP4 and MP2. Nevertheless, this circuit is less complex since it omits the clock multiplier. For the sake of compactness, this architecture is used in the design.

Single channel architecture allocates 250 ps to the sampling phase. This phase includes the settling of flash and SAR capacitive DAC settling times. That makes the closing delay of the switch critical. M_9 in Figure 5.3 should be kept large in order to pull gate of the switch as quick as possible.

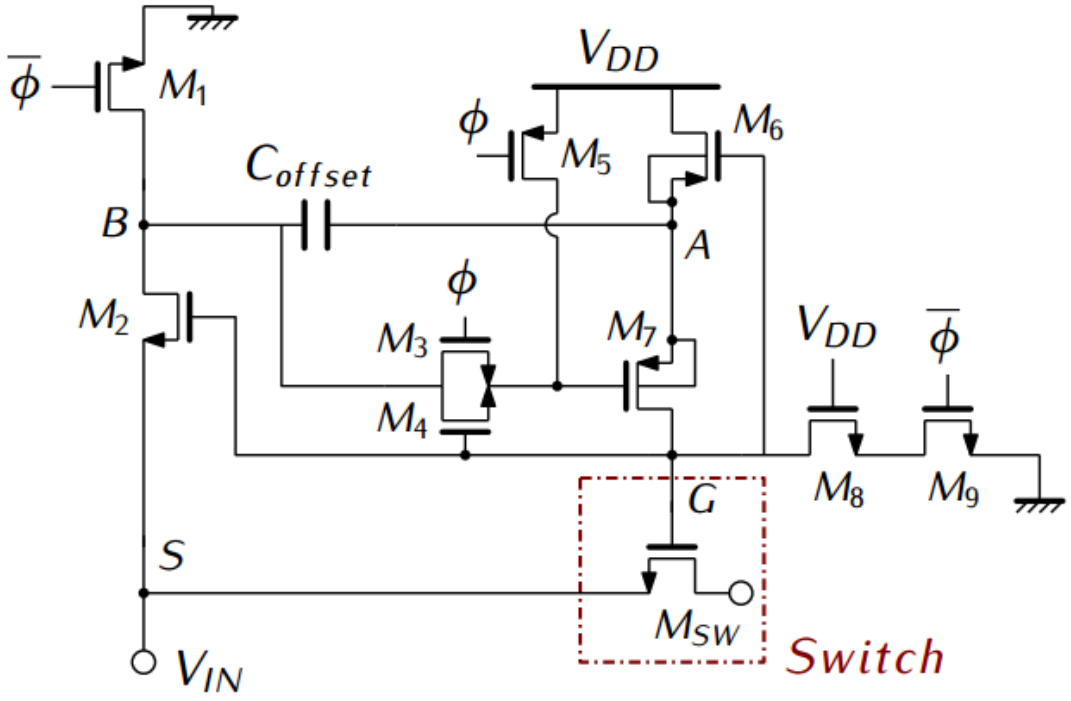

Figure 5.3: Bootstrapped switch structure from [27].

Rail-to-rail input swing mandates using bootstrapped input sampling switches for both flash ADC and SAR ADC. Since the same input is fed to both ADCs, only one bootstrap voltage generation circuit is placed for each input signal polarity and distributed to the related switches. Single channel ADC architecture employs only one flash ADC that takes positive input. This creates a mismatch between the loads of bootstrap voltage generators. In order to solve this issue, dummy switches were placed. Sampling network implicitly depicted in Figure 5.28.

Flash ADC employs 14 comparators. Therefore, magnitude of kickback noise to the sampled input becomes large. By using separate sampling networks for flash ADC and SAR ADC stages isolates the input of SAR stage from kickback noise of the flash ADC.

5.2 Design of the Flash ADC

According to the proposed single channel architecture, a 14-level flash ADC is designed. Since various redundancy techniques are used in the proposed ADC architecture, accuracy requirements become less stringent. Design efforts are focused on the issues encountered with resistor ladder and comparators. Since the outputs of the flash ADC are directly fed to capacitive DAC, no decoder structure is employed.

Flash ADC is not fully-differential due to the rail-to-rail input range of whole ADC. Input range of the flash ADC is rail-to-rail since SAR ADC input is rail-to-rail. In order to design fully differential comparators, either a preamplifier, which has input rail-to-rail range, i.e. with a complementary input stage, should be utilized. As emphasized in Section 4.2, preamplifiers reduce the conversion speed of a comparator.

5.2.1 Resistor ladder

In a flash ADC, conventional way to generate the reference voltages is by employing a resistor ladder. There is an important trade-off between power consumption and kickback noise present on the resistor ladder. Low ladder resistance reduces the effect of the kickback noise. However, it also increases the power consumption of the resistor ladder. Therefore, unit resistance of resistor ladder kept small.

As an additional measure, decoupling capacitors are added on resistor string taps. Sizes of these capacitors are picked according to the free spaces on the layout since their absolute sizes are not important because of the reference voltage sampling which is explained in following sections.

As stated in [28], "resistors for high precision analog design are formed by polysilicon or diffused n- or p-doped areas". 65nm process which is used in this work only provides polysilicon resistors. Hence, in the resistor ladder, unsilicided n+ polysilicon resistors are used. Unsilicided polysilicon resistors has lower sheet resistance compared to silicided counterparts which lets obtaining low resistance values. Monte-carlo simulations of the resistor ladder have shown that these resistors satisfy precision requirements.

5.2.2 Comparators

As in other types of ADCs, comparator is the backbone of designed flash ADC. Comparator performance directly affects the accuracy and conversion speed of flash ADC eventually the whole ADC. Main role of the flash ADC in the proposed single channel ADC is to provide first three MSBs while doing it as quick as possible. Therefore, two design criteria become prominent, first is the offset and second is the regeneration time.

As mentioned in Chapter 3, redundancy relaxes the requirements on the offset of the comparators by overlapping the intervals of coarse conversion and subsequent SAR conversion. In this case, offset spread of the comparators must be in the boundaries of the half LSB of flash ADC, which is 32.5 mV. This value should be achieved without the help of any calibration scheme, since the purpose of the proposed search algorithm is itself avoiding such schemes by employing redundancy. Therefore obtaining required offset values by sizing is convenient in this case. As stated in [21], matching performance of transistors improves with larger gate areas. Obviously, there is a tradeoff between offset power consumption and comparator speed since larger transistors have larger parasitic capacitors, which increases power consumption and penalizes the speed.

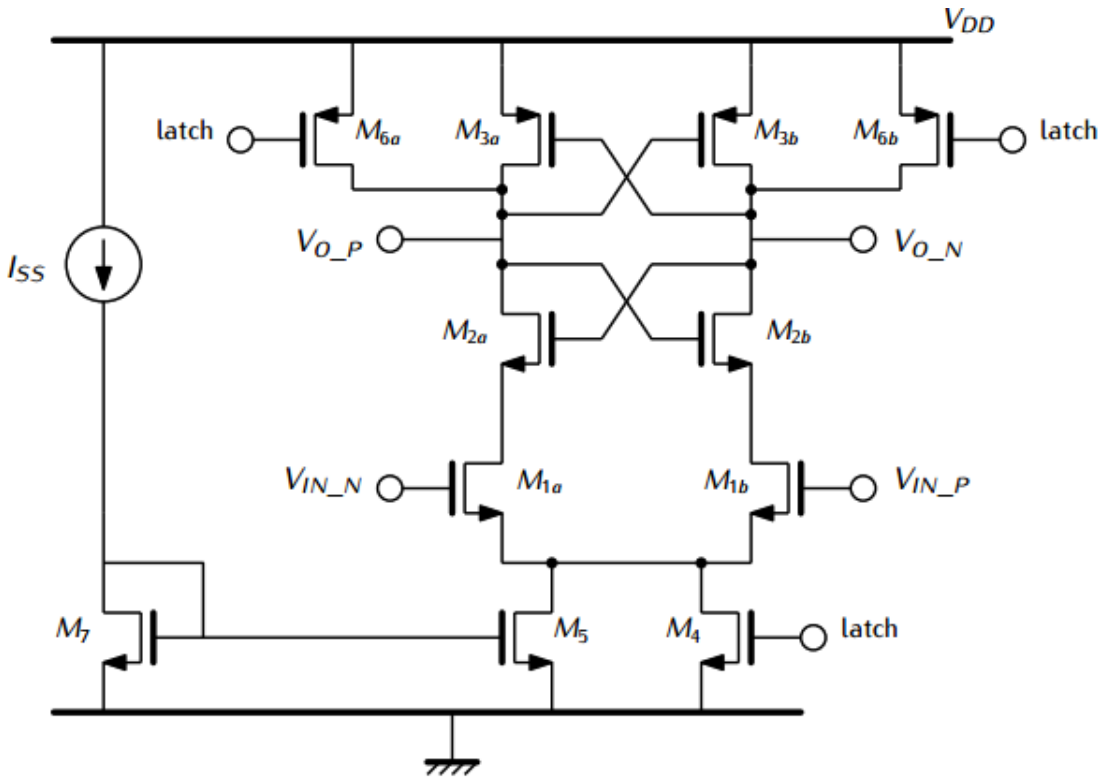

Figure 5.4: NMOS input comparator used in flash ADC.

In Section 4.4.2 it is shown that proposed comparator structure is superior to conventional sense amplifier in terms of offset and power consumption. Employing the proposed comparator architecture could help to relax aforementioned tradeoff of offset, speed and power consumption. Therefore, proposed comparators are utilized in the flash ADC. Transistors are sized to obtain 2σ offset voltage spread of 32.5

mV. Histograms of offset for NMOS and PMOS input transistors are given in Figure 5.6 and Figure 5.7 respectively.

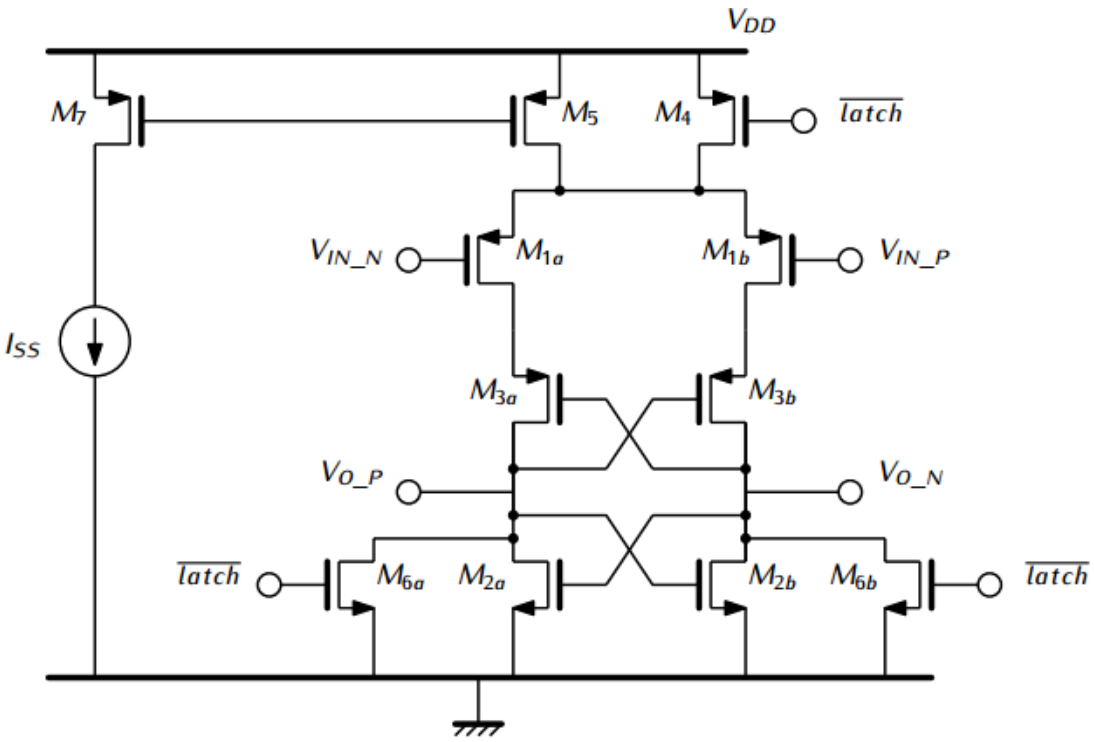

Figure 5.5: PMOS input comparator used in flash ADC.

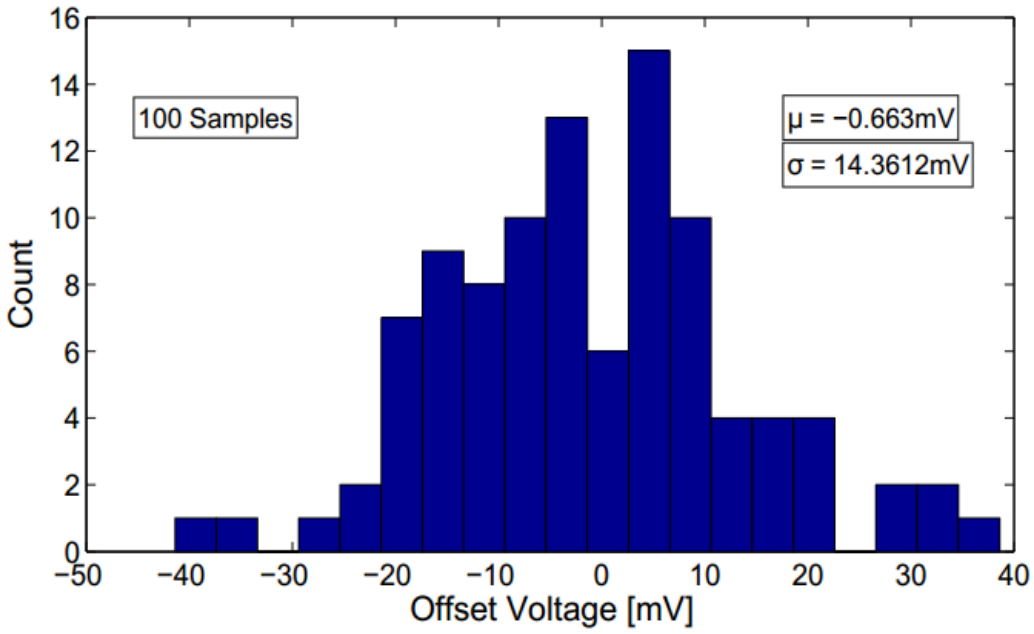

Figure 5.6: Histogram of offset voltage for NMOS input comparator.

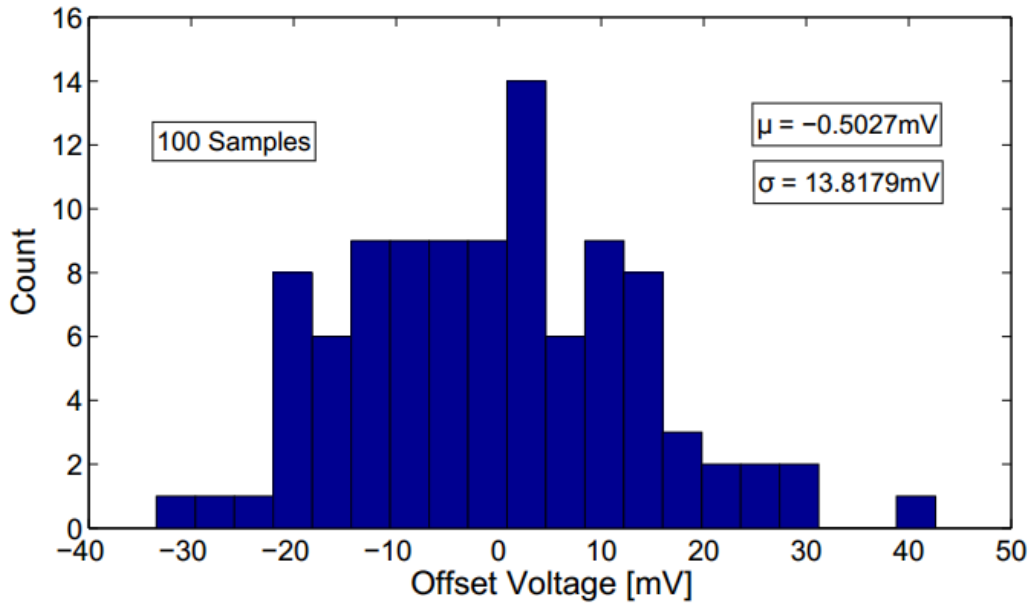

Figure 5.7: Histogram of offset voltage for PMOS input comparator.

Speed of the comparators are crucial as well since in the proposed ADC architecture, the flash ADC should give the outputs in 125 ps. Proposed single channel ADC has rail-to-rail input range, therefore flash ADC must be able to process rail-to-rail inputs as well. In this case, input common-mode voltage of comparators becomes important. In terms of speed, NMOS input comparators benefit from higher input-common mode voltage whereas PMOS input comparators benefit from lower input common-mode voltage. In order to cover the whole input range while satisfying timing requirements, PMOS input comparators should be used on first few bottom reference voltages. Allocated flash conversion time is 125 ps including the propagation delay of output buffers. Therefore, regeneration time of the comparators should be lower than 75 ps with a margin for layout effects.

For two NMOS input and PMOS input comparators which have same regeneration time, PMOS input comparator consumes more power due to larger parasitic capacitance on the nodes of comparator. This is due to lower mobility of holes, which mandates using large PMOS transistors in order to obtain same current drive capability. Therefore, it is convenient to use PMOS input comparators as few as possible. Simulations have been performed for parasitic extracted layouts of comparators to observe the lowest input common-mode voltage in which NMOS

input comparator still goes faster than PMOS counterpart. Results are shown in Figure 5.8. Based on the simulation results, for the reference voltages higher than 400 mV, NMOS input comparators are used in the design.

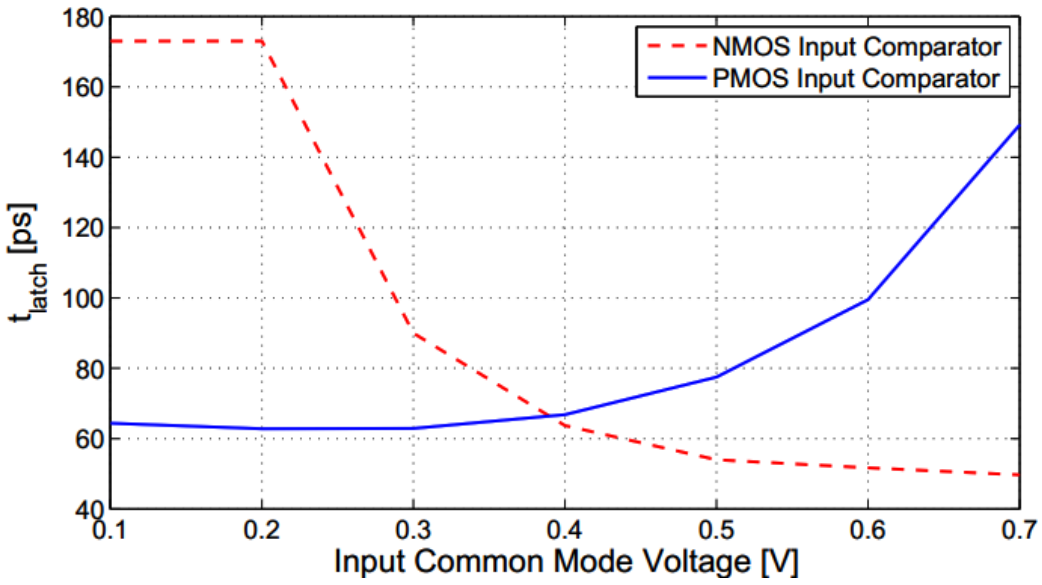

Figure 5.8: Latch regeneration time versus input common mode voltage for NMOS and PMOS input comparators with parasitics extracted.

5.2.3 Reference voltage sampling

In previous sections, mostly the effect of kickback on reference ladder is emphasized. However, since kickback noise affects both inputs of a latch, sampled input signal is disturbed as well. This effect is depicted on Figure \ref{refsmp1}. Sampled input signal gets disturbed by two phenomenons. First by charge injection and then by the kickback noise. The amount of change can be calculated via fundamental capacitor equation shown in Equation \ref{eq:deltaV}. Where V_{samp} is sampled input voltage, C_{samp} is sampling capacitance and ${\Delta}Q$ is the charge variation at the sampling node due to charge injection or kickback. C_{samp} is equal to the unit capacitor in SAR capacitive DAC and it is chosen as small as $\frac{kT}{C}$ noise allows in order to keep the bandwidth of sampling network wide and keep the occupied area of SAR ADC small. Therefore it can be deduced from the Equation \ref{eq:deltaV} that small capacitance means large voltage variation for a constant charge at that node.

$$V_{samp} = \frac{\Delta Q}{C_{samp}} \tag{5.2}$$

On the other hand, as stated in Section \ref{ch:ref_ladder}, in order to reduce the effect of kickback at the reference nodes, total resistance of the resistor ladder is kept small. This increases the inequality between sampled input voltage and reference voltage at the flash enable instant. One technique to mitigate this mismatch may be done by increasing the ladder resistance; however, this is not a precision technique and therefore not adopted.

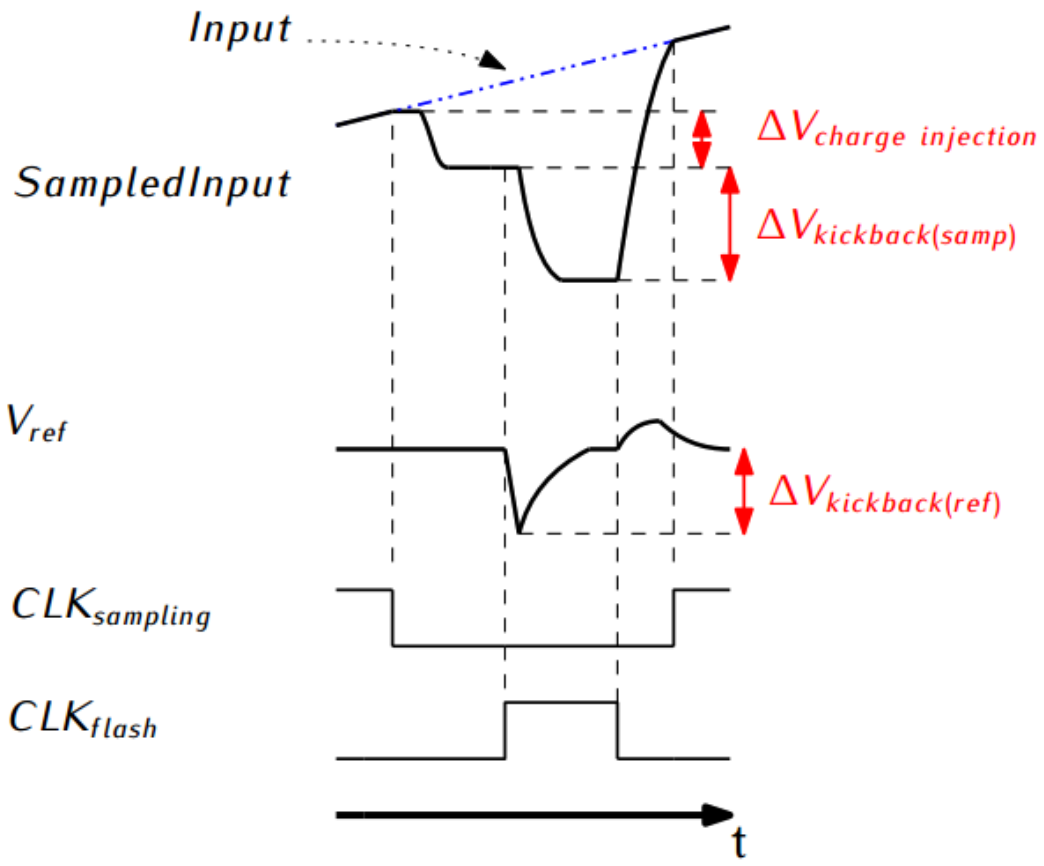

Figure 5.9: Sampled input voltage and reference voltage waveforms in regular case.

Aforementioned issues worsen since $\Delta V_{kickback(samp)}$ values of flash ADC inputs are approximately equal since all the switches, sampling capacitors and sizes of latch input transistors are same(except for the difference between NMOS and PMOS input latches). However, effect of kickback noise on the reference voltages varies since the equal resistance at a reference node is different for each reference. This inequality combined with the varying effect of kickback on reference voltages shifts the reference levels. This significantly reduces the accuracy.

An equalization approach can be used to circumvent these problems. In order to equalize the effects of kickback as well as charge injection, reference voltages are sampled too. The approach is depicted in Figure 5.10. Ideally, when the switches and sampling capacitors are identical, both reference and sampled input change by the same amount due to charge injection and kickback. In this way, V_{ref} is affected by charge injection too, which brings the sampled reference voltage close to sampled input voltage.

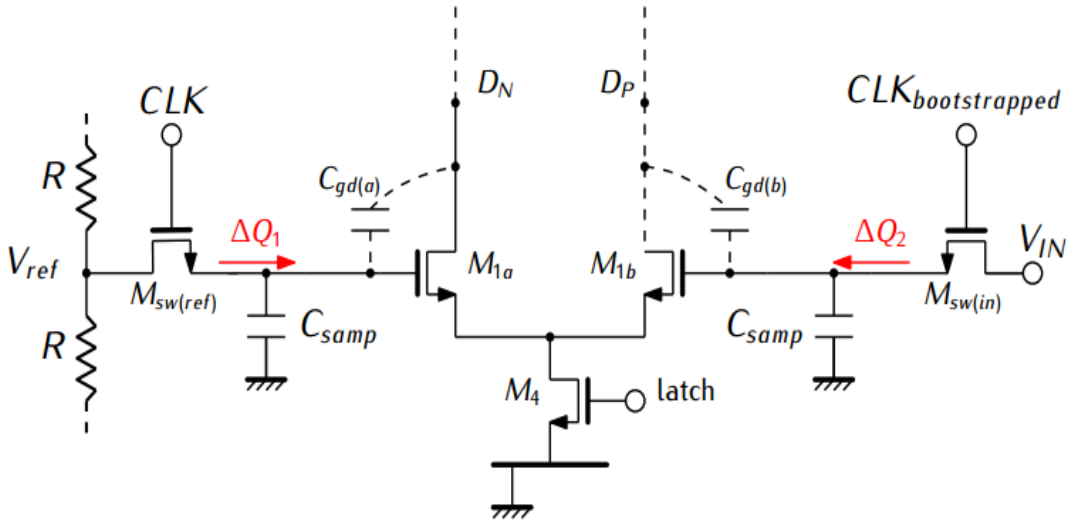

Figure 5.10: Reference sampling approach.

In Figure 5.10, one can see that regular clock signal is used for reference sampling whereas bootstrapped clock is used for input sampling. Reference voltages are ideally constant signals, therefore motivations to use bootstrapped switch is not valid for reference voltages. However, using two different types of clock contributes to mismatch in the charge injection between the two inputs of latches.

This error can be mitigated by fine-tuning. Fine-tuning can be done by two techniques. First technique is tuning by reference sampling capacitor. However, this technique causes mismatch between $\Delta V_{kickback(samp)}$ and $\Delta V_{kickback(ref)}$. Second technique is fine-tuning the sizes of reference voltage sampling switches. Channel charge formula is given in Equation 5.3 [29] where L_{eff} denotes the effective gate length.

$$Q_{ch} = W\, L_{eff}\, C_{ox}\, (V_{GS} - V_{th}), \qquad for\ V_{DS} = 0 \tag{5.3}$$

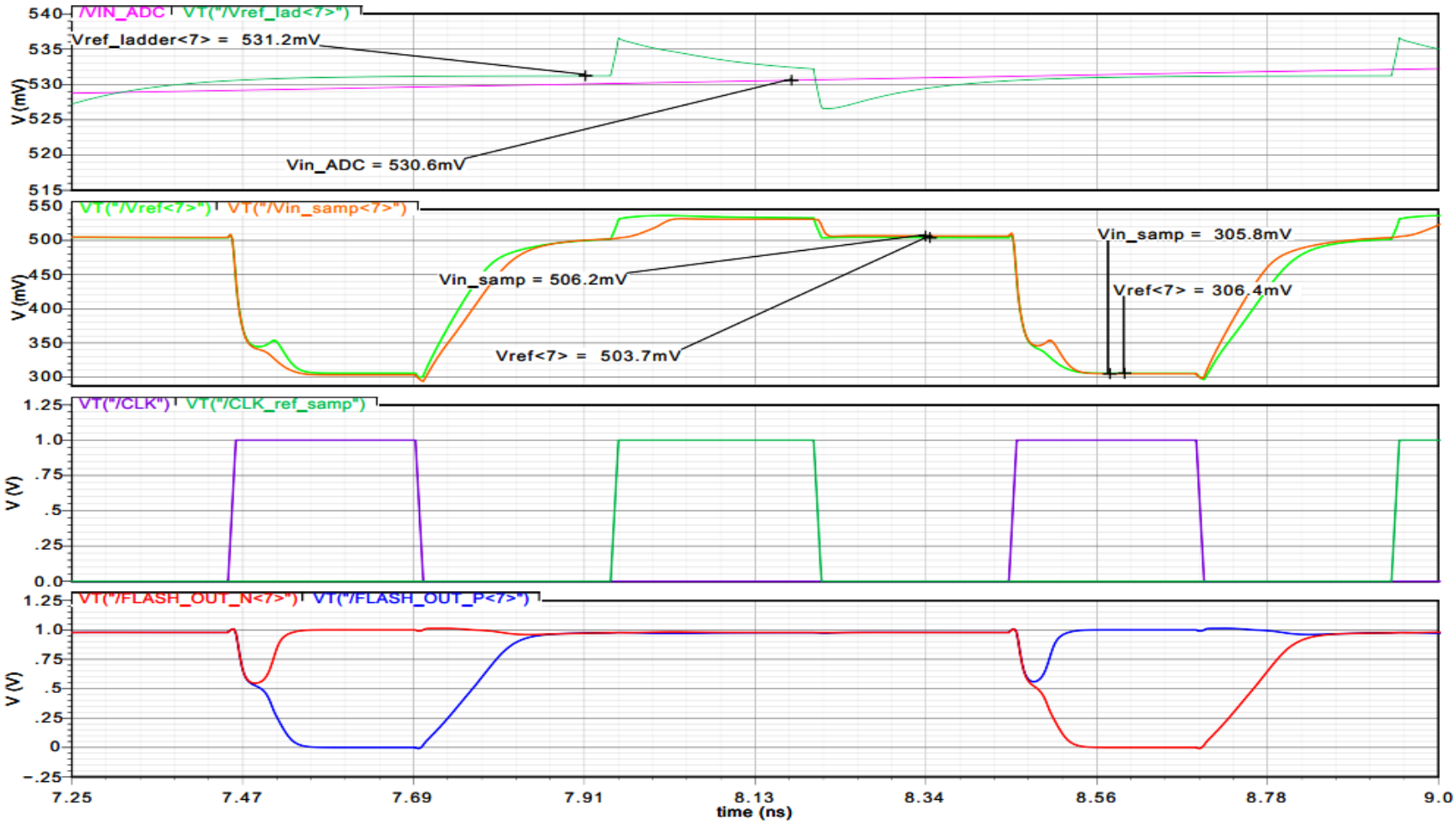

Figure 5.11: Transient response of input sampling and reference sampling.

One can see that the channel charge can be controlled by the sizes of switches. This technique is adopted in this work and switch sizes were tuned with the help of post-layout simulations.

On higher reference voltages, reference sampling switches become slower in settling. Therefore, PMOS switches are used for the three switches from the top. However, this changes the polarity of charge injection and destroys the technique for these reference levels. In order to solve the issue, CMOS switches are used. Here, PMOS switches are used for main sampling function whereas NMOS switches keeps the polarity of the charge injection same as the switches below.

Transient response of input and reference voltages are shown in Figure 5.11. One can see that the technique successfully equalizes the input and reference voltages and reduces the error due to charge injection and kickback down to 2.5 mV.

5.3 Layouts Of The Designed Blocks

5.3.1 Bootstrapped switch

Layout of the bootstrap circuit is shown in Figure 5.12 and layout sizes are given in Table 5.1. A compact layout is aimed in bootstrap circuit since it is important to decrease the interconnect parasitics. Note that reducing parasitics especially important for node A in Figure 5.3 due to its direct effect on bootstrap voltage. Effects of parasitics at node A on bootstrap voltage is analogous to conventional structure and is given in Equation 5.1. Fast response of the switch is important as well since the sampling window is narrow. Therefore reducing parasitics is also important on these terms.

Table 5.1: Layout sizes of blocks.

	Width	Length
Bootstrap circuit	25 µm	18 µm
Comparator (NMOS Input)	11 µm	7.6 µm
Comparator (NMOS Input)	11 µm	7.6 µm
Flash ADC	142 µm	40 µm

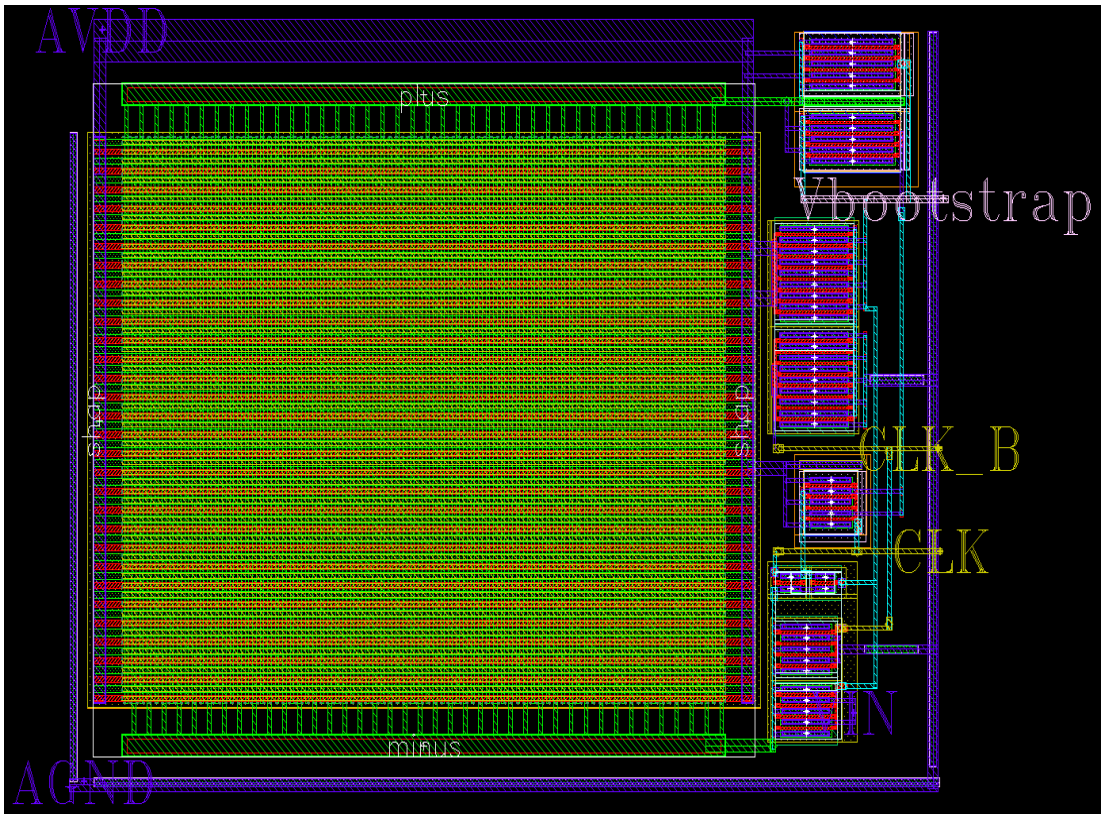

Figure 5.12: Layout of bootstrap voltage generator.

5.3.2 Comparator

Layout efforts are mostly made on comparators due to their importance on overall performance of the ADC. Accuracy of the comparator is highly dependent on layout effects. As stated in [30], "MOS transistors are vulnerable to gradients in temperature, stress and oxide thickness", therefore they should be placed as close as possible to each other. Another technique to diminish the effects of gradients is so-called common-centroid layout. As stated in [30], "pairs of matched transistors should be laid out as cross-coupled pairs to take advantage of the superior symmetry". Another source of mismatch in MOS is poly etch variations and dummy transistors should be used to diminish its effect. Aforementioned layout arrangements should be applied by using multi-finger transistors, which is also beneficial for reducing the junction parasitics by decreasing the junction areas.

In Section 4.3.2 it is stated that the dynamic offset can be minimized by careful layout. Therefore, comparators were laid out with the maximum symmetry.

Layout arrangement of the comparator is depicted in Figure 5.13 where aforementioned techniques have been used. Input differential pair and cross-coupled

inverter pairs have the maximum matching priority since they are directly related to the offset of comparator. Therefore, common-centroid layout is used in both. Note that cross-coupled PMOS transistors have the same arrangement as the cross coupled NMOS.

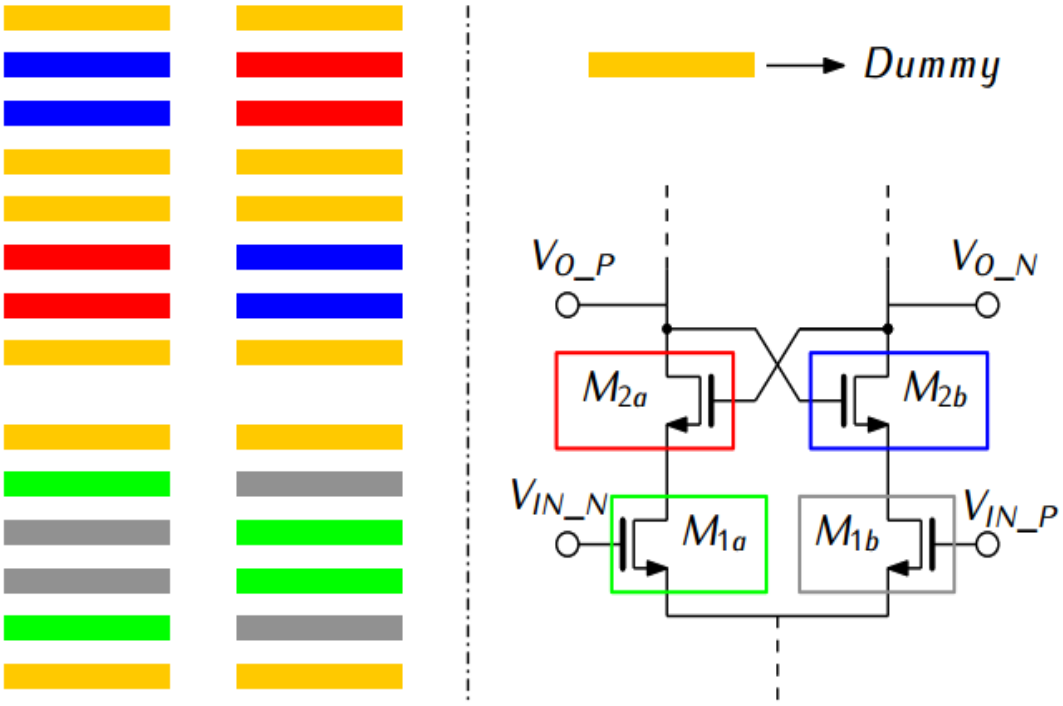

Figure 5.13: Layout arrangements in comparator layouts.

Layout of NMOS input comparator is shown in Figure 5.14 and PMOS input in Figure 5.15. Sizes of the layouts are given in Table 5.1.

5.3.3 Flash ADC

Flash ADC layout is shown in Figure 5.16 and layout sizes are given in Table 5.1. In order to avoid the effect of gradient effects comparator to comparator as well as on resistor string, flash ADC layout should be as short as possible. Therefore, most of the effort has been made on this issue.

Due to the floorplan shown in Figure 5.28, flash ADC is close to the inputs. Therefore, a delay mismatch between flash ADC and SAR ADC samplers arises. In order to equalize the delays, trace that connects the flash ADC input sampling switch to the sampling capacitor is laid out like a serpent. Detail is shown in Figure 5.17.

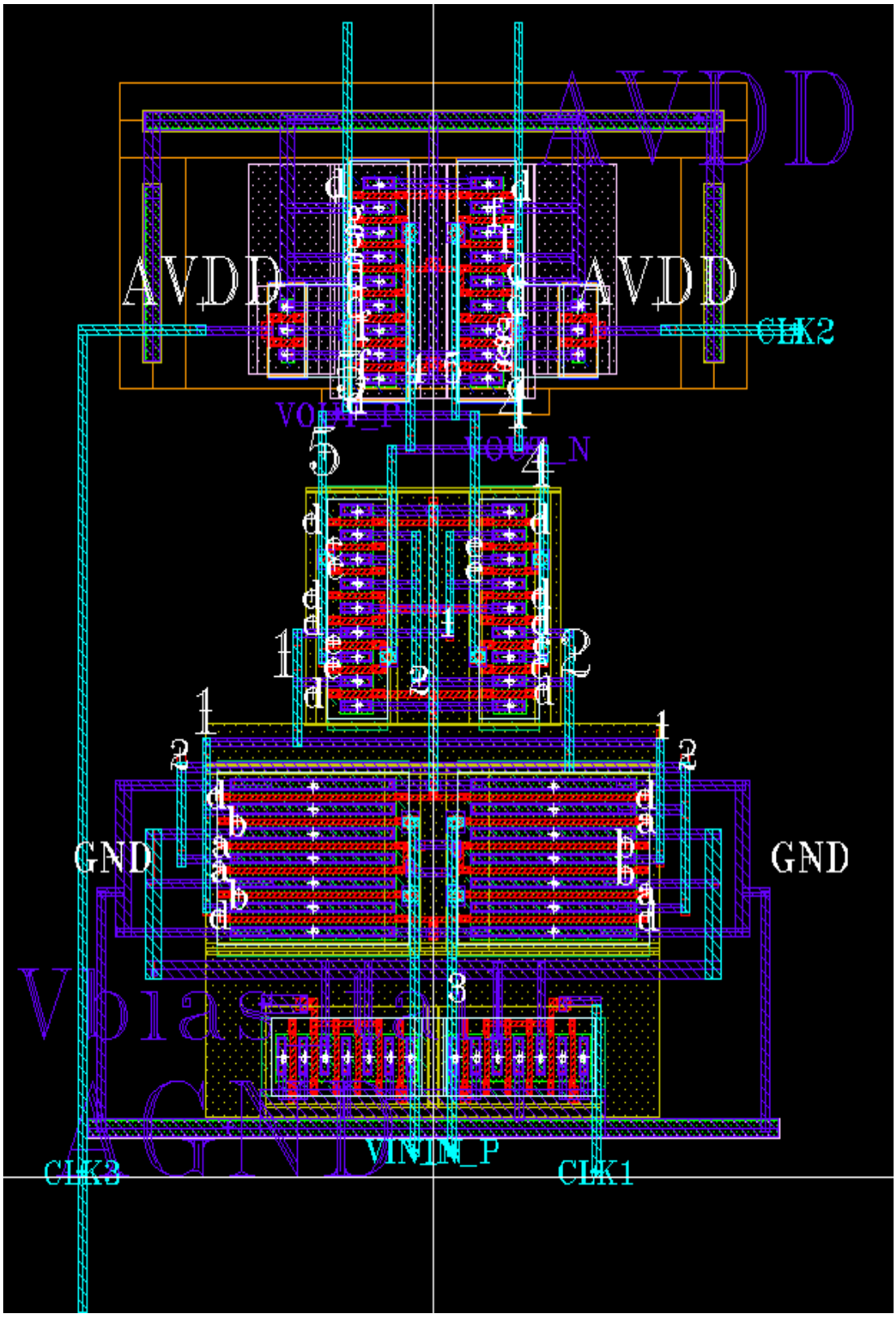

Figure 5.14: Layout of NMOS input comparator.

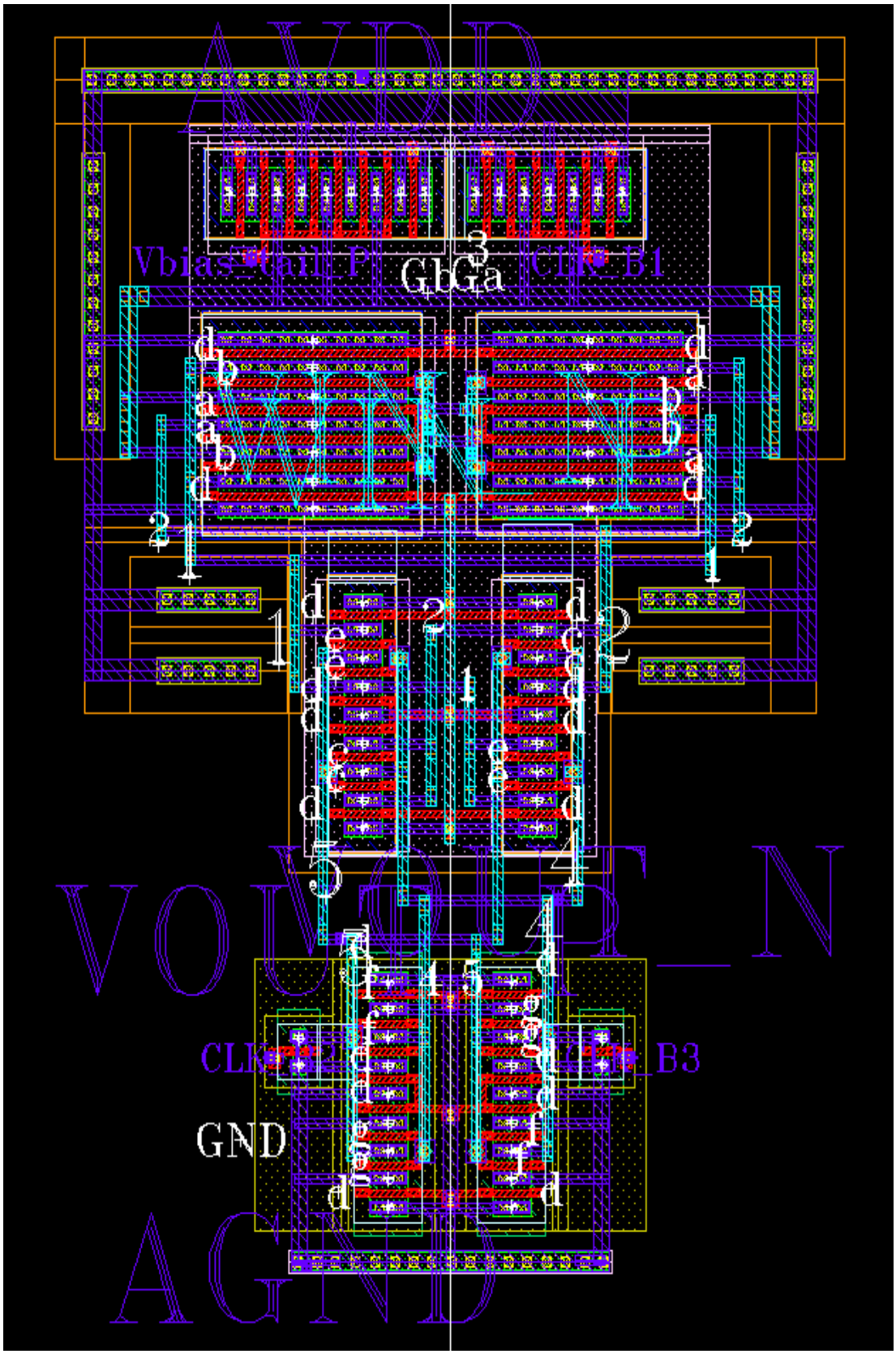

Figure 5.15: Layout of PMOS input comparator.

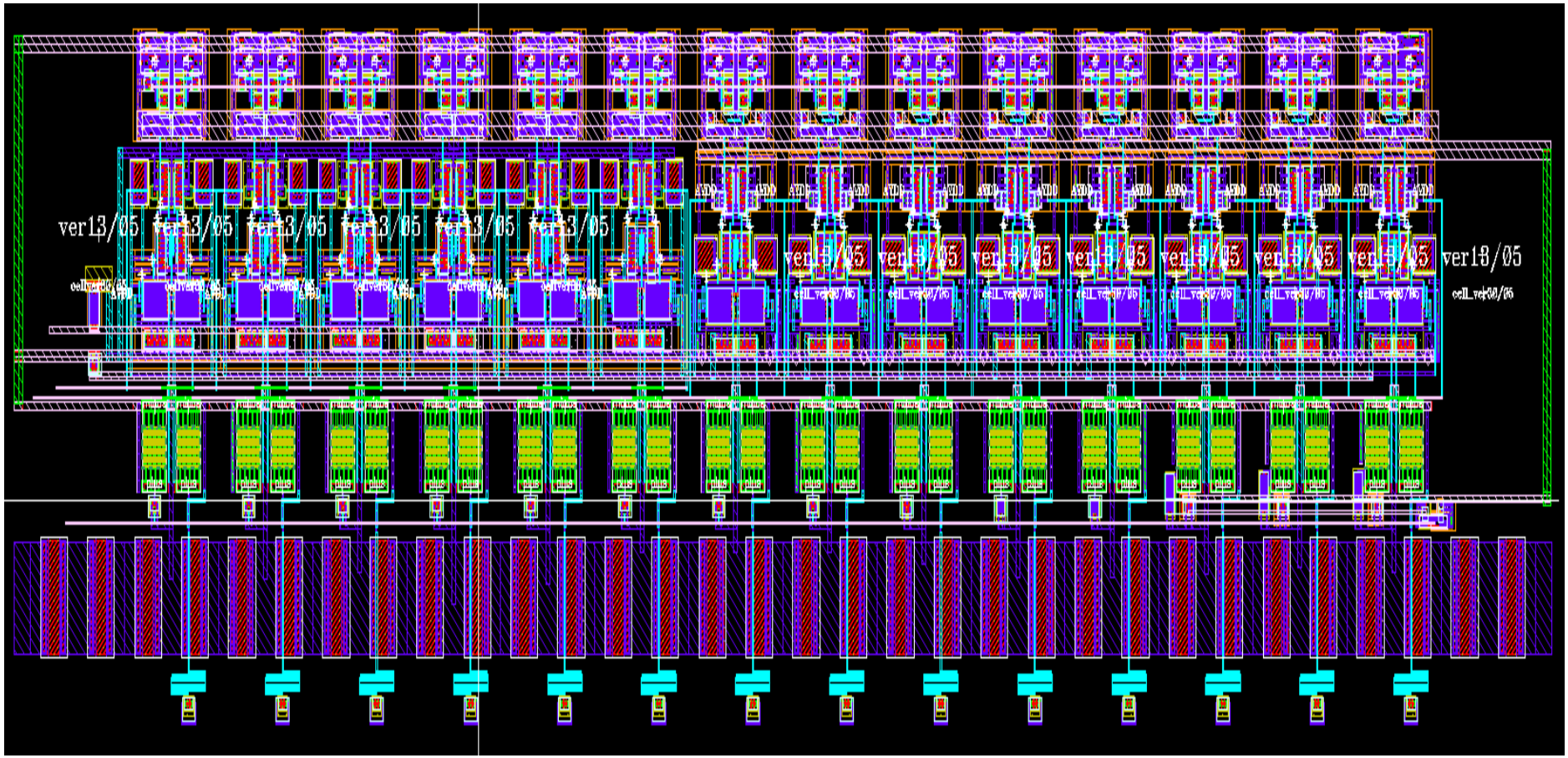

Figure 5.16: Top-level layout of flash ADC.

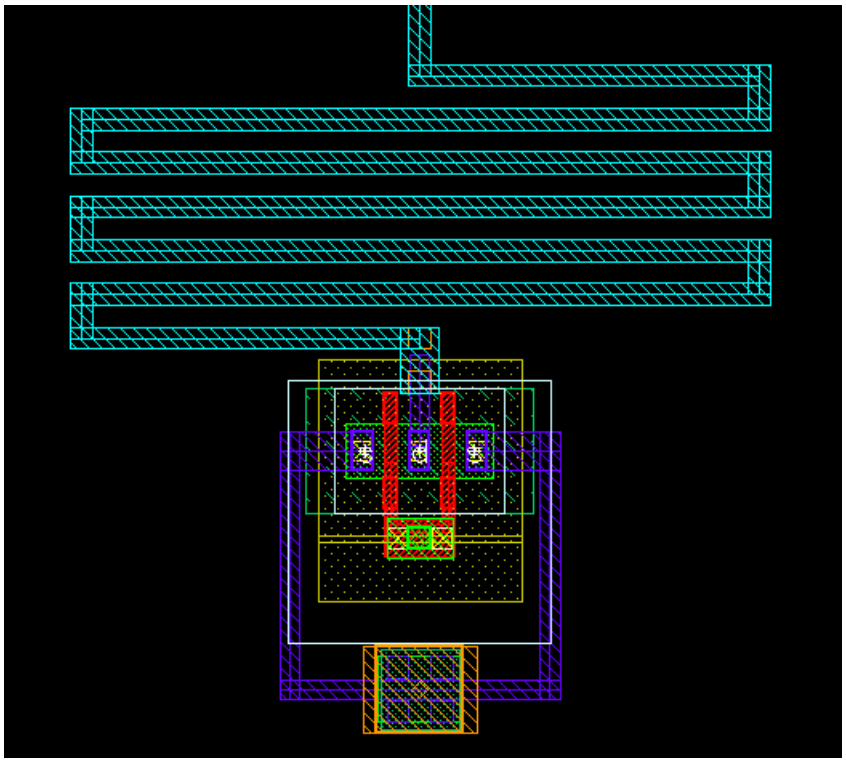

Figure 5.17: Detail of flash ADC layout which shows serpent trace to equalize delays.

5.4 Post-Layout Simulations

5.4.1 Comparator

Post-layout simulations of NMOS and PMOS input comparators have been done for latch time and RMS current consumption. Schematic and post-layout latch times versus input common mode voltage were compared and showed for NMOS and PMOS input comparators in Figure 5.18 and Figure 5.19 respectively. Post-layout values of RMS current consumption of comparators are shown in Figure 5.20.

5.4.2 Flash ADC

As shown in Section 5.4.1 , post-layout values of latch times are satisfying the 125 ps flash ADC response time requirement. In addition to that, post-layout accuracy of references is observed via simulations. Results are shown in Figure 5.21. Note that the absolute reference error is less than an LSB of 8-bit ADC (3.9 mV) at all times. Therefore, the accuracy requirements of flash ADC will be satisfied even when the error is combined with the offsets of comparators.

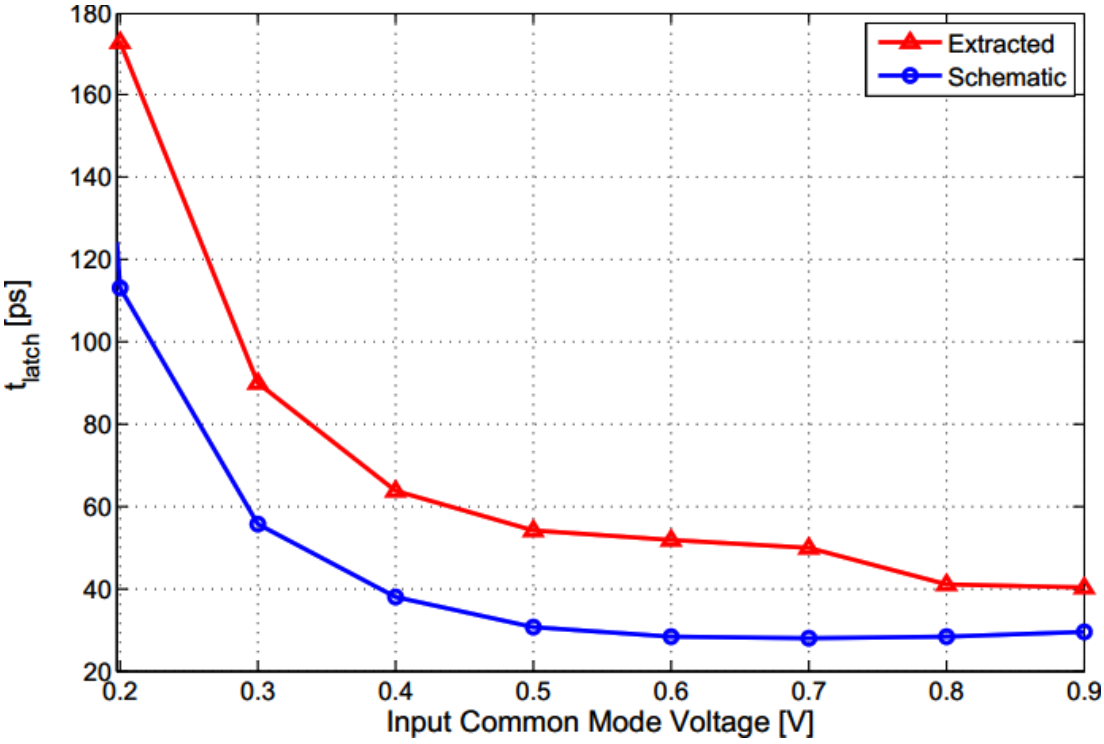

Figure 5.18: NMOS input comparator latch regeneration time comparison of schematic and post-layout ($\Delta V_{in} = 4$ mV).

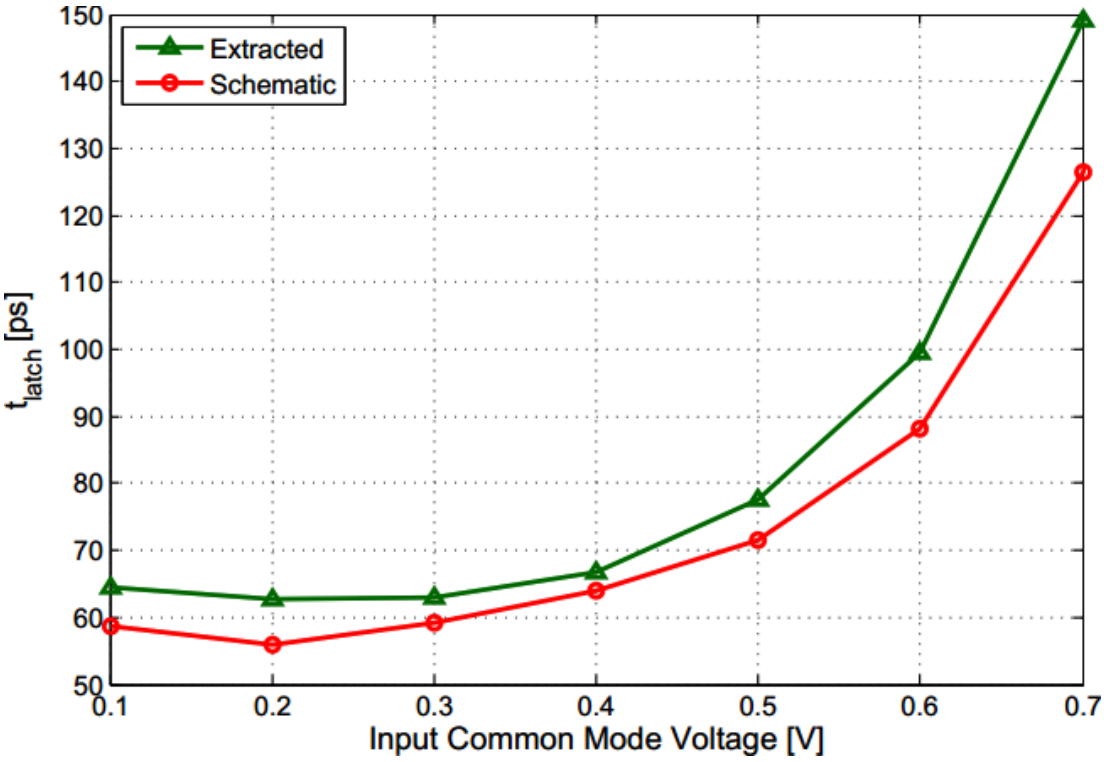

Figure 5.19: PMOS input comparator latch regeneration time comparison of schematic and post-layout ($\Delta V_{in} = 4$ mV).

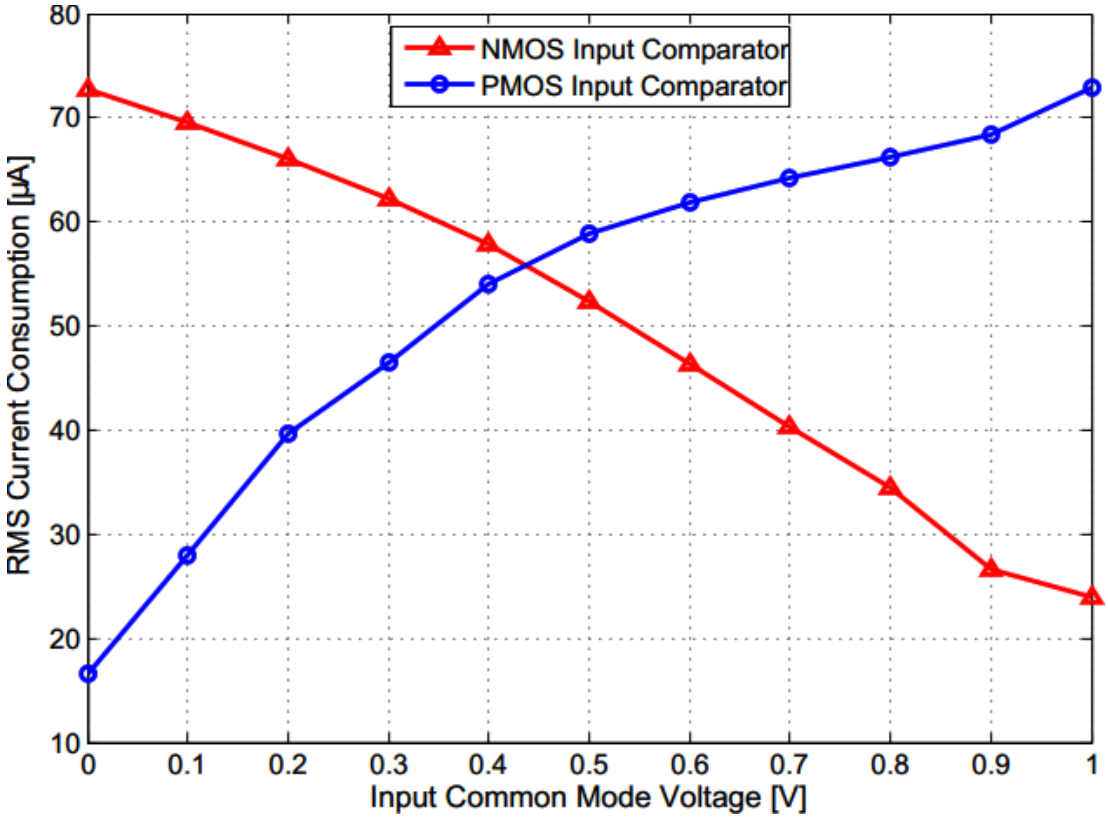

Figure 5.20: RMS current consumption of comparators versus input common-mode voltage.

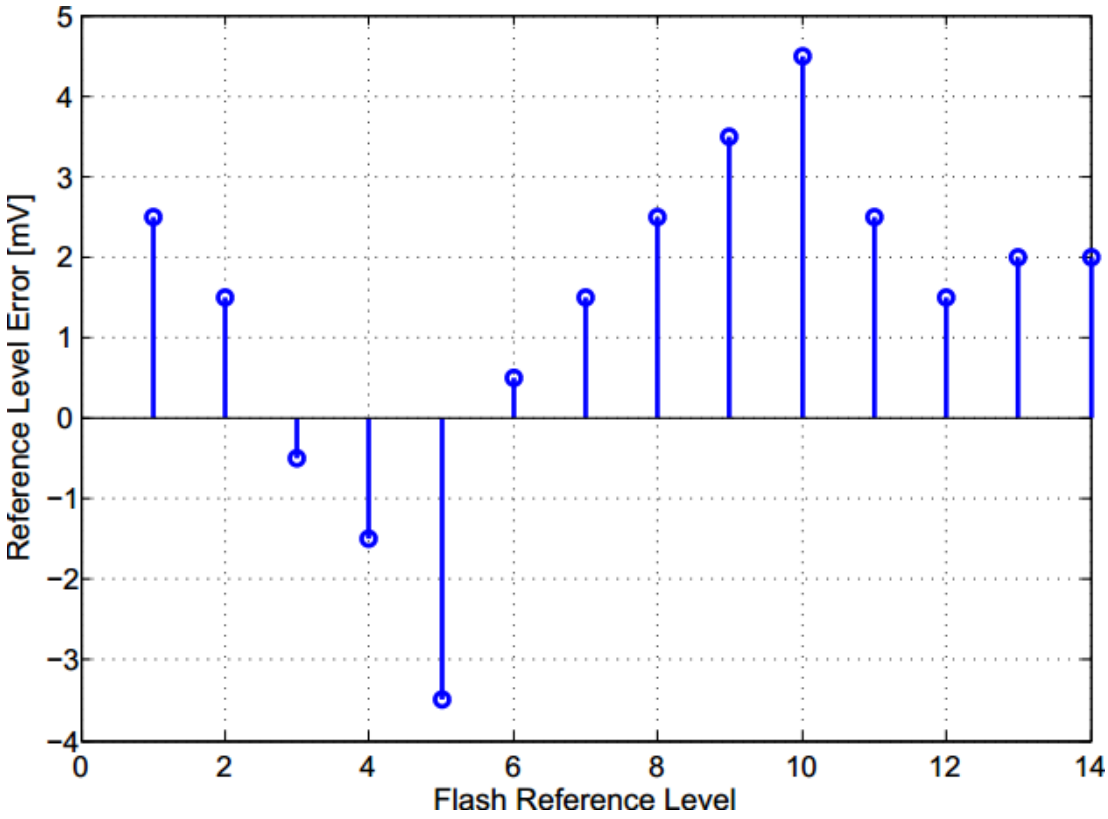

Figure 5.21: Post-layout reference level errors of flash ADC.

5.4.3 Bootstrapped switch

Post-layout characterization of bootstrapped switches has been done for an input frequency in the vicinity of Nyquist. Figure 5.22 shows the bootstrap voltage and input voltage.

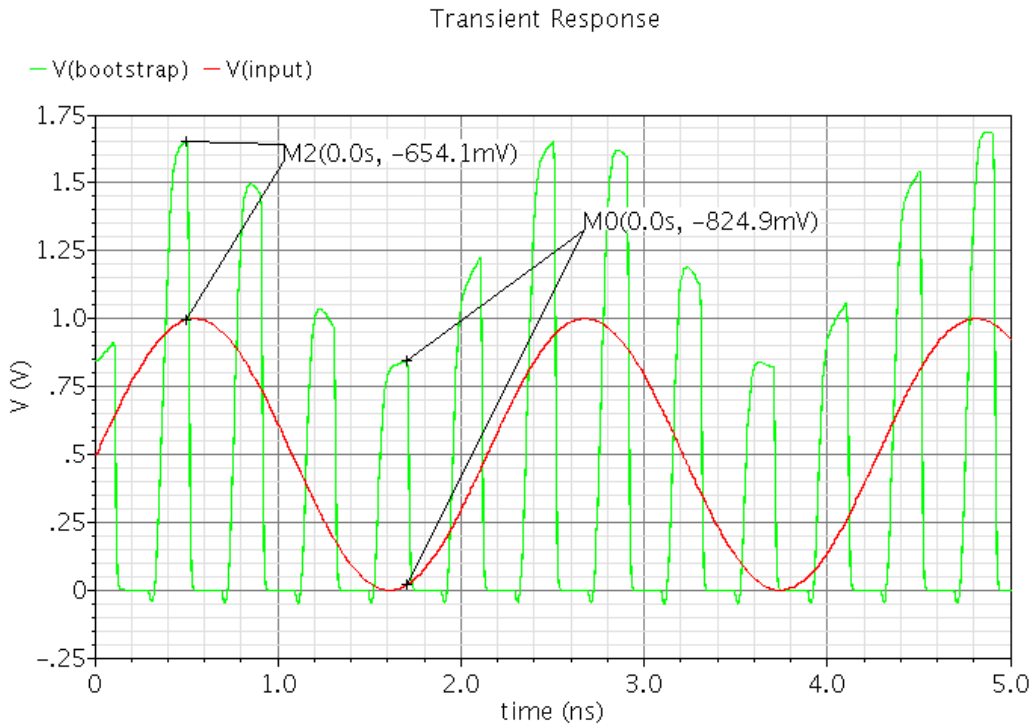

Figure 5.22: Post-layout waveforms of bootstrap voltage and input (f_{in} = 468.8 MHz).

Figure 5.23 shows the DFT of flash ADC input. Flash ADC inputs are single ended therefore the 2nd harmonic is high. However, harmonic distortion due to second harmonic (HD2) is -31 dBc which allows 5-bit resolution. Considering the flash ADC is 4-bit, sampling switch linearity performance is satisfactory.

Figure 5.24 shows the DFT of fully differential SAR ADC input. Here HD2 is -61 dBc and HD3 is -52 dBc. Therefore, switch linearity is approximately 8.5 bits, which satisfies the 8-bit requirement of SAR ADC.

5.5 Overall Simulations

Post-layout simulations of the overall ADC is done to see the performance of the blocks designed for this thesis along with the other blocks. INL graph of the ADC is shown in Figure 5.25. INL is found between ± 1 LSB.

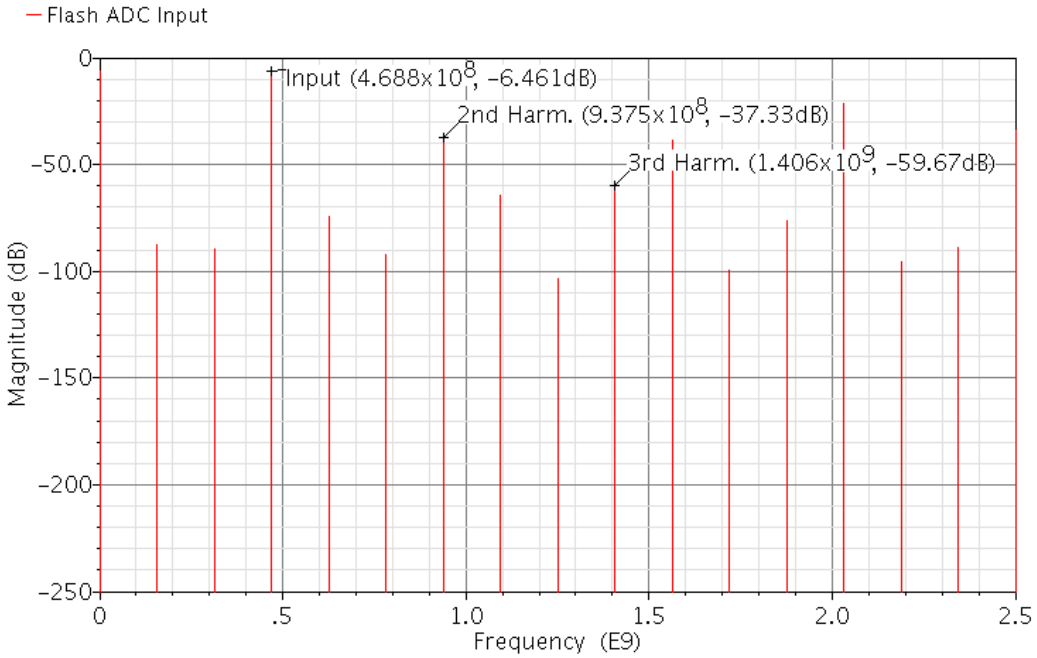

Figure 5.23: Post-layout DFT of flash ADC input (f_{in} = 468.8 MHz, single-ended).

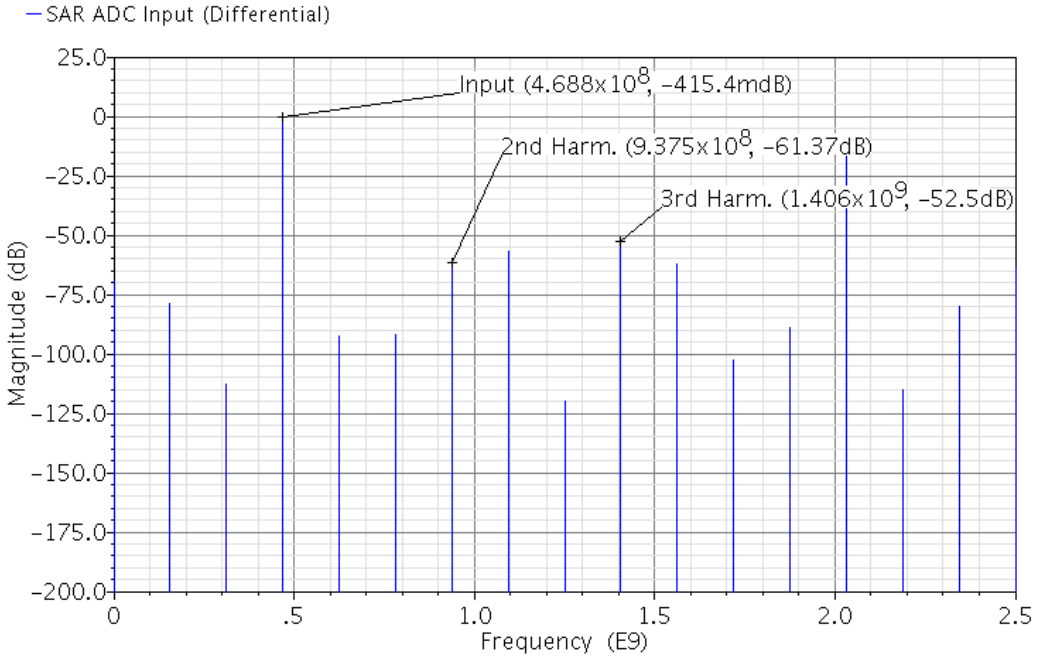

Figure 5.24: Post-layout DFT of SAR ADC input (f_{in} = 468.8 MHz, differential).

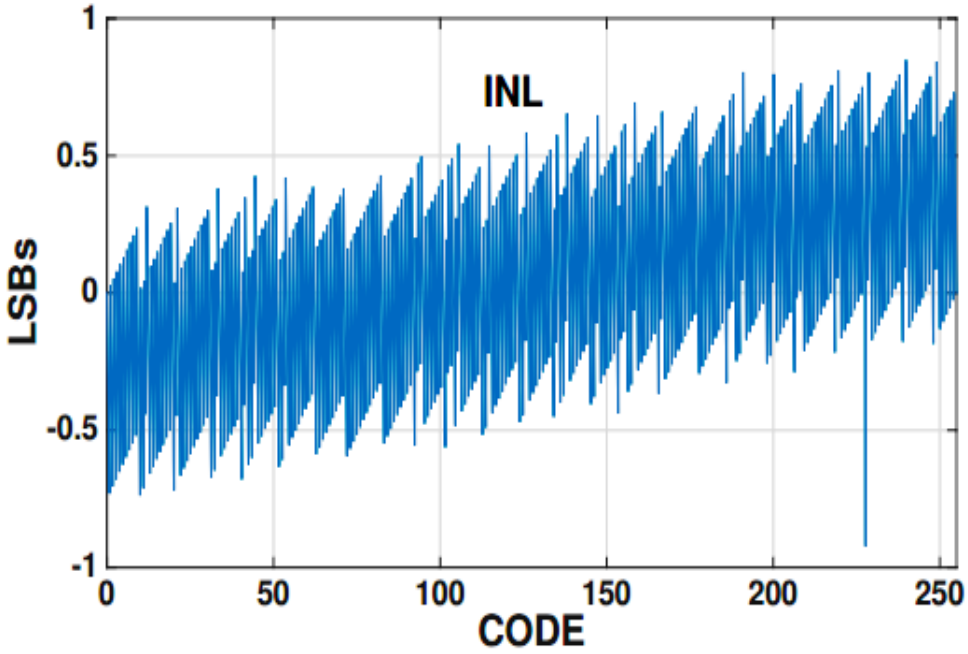

Figure 5.25: INL graph of the overall single channel ADC.

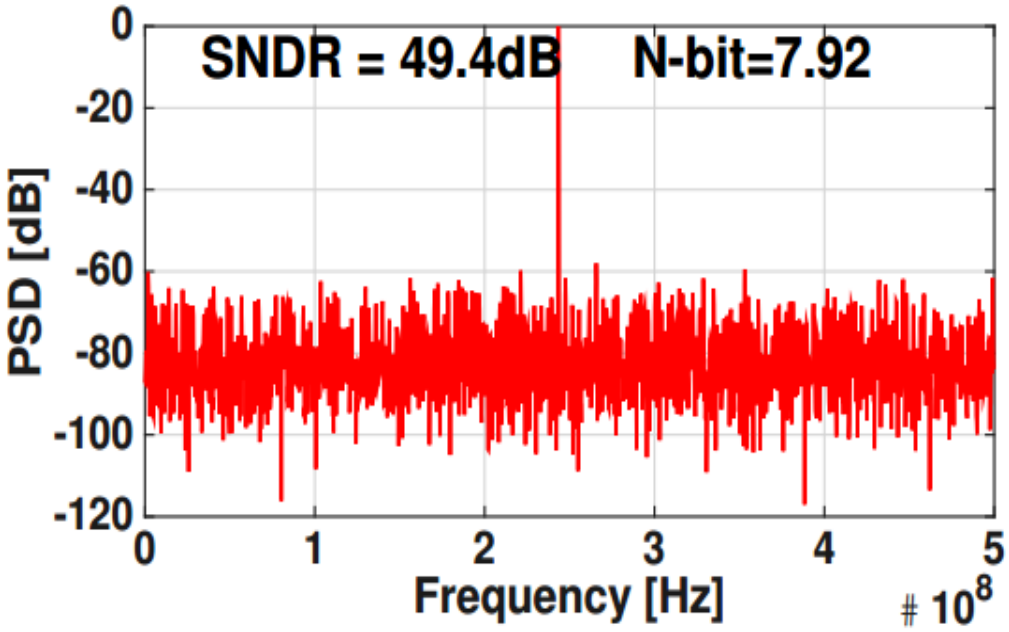

Figure 5.26: Output DFT of the overall single channel ADC (f_{in} = 243 MHz, f_s = 1 GHz).

In order to observe the dynamic performance, DFT of output is taken for $f_{in} = 243\ MHz$, $f_s = 1\ GHz$. Results are shown in Figure 5.26. Note that around $f_s/4$, SNDR of 49.4 dB and ENOB of 7.92 is obtained.

Total power consumption of overall ADC is 6.73 mW. Power consumption distribution of overall ADC is shown in Figure 5.27. Digital VDD consumes more than half of the whole ADC since all of the latches and logic connected to it.

Figure-of-merit (FOM) of an ADC is useful as a comparison tool. FOM of the ADC is calculated as shown in Equation 5.4.

$$FOM = \frac{Power}{2^{ENOB} f_{synq}} \tag{5.4}$$

FOM of ADC is calculated for $f_{in} = 243\ MHz$ and $f_s = 1\ GHz$. FOM of proposed ADC is found as 27.8 fJ/conv.-step.

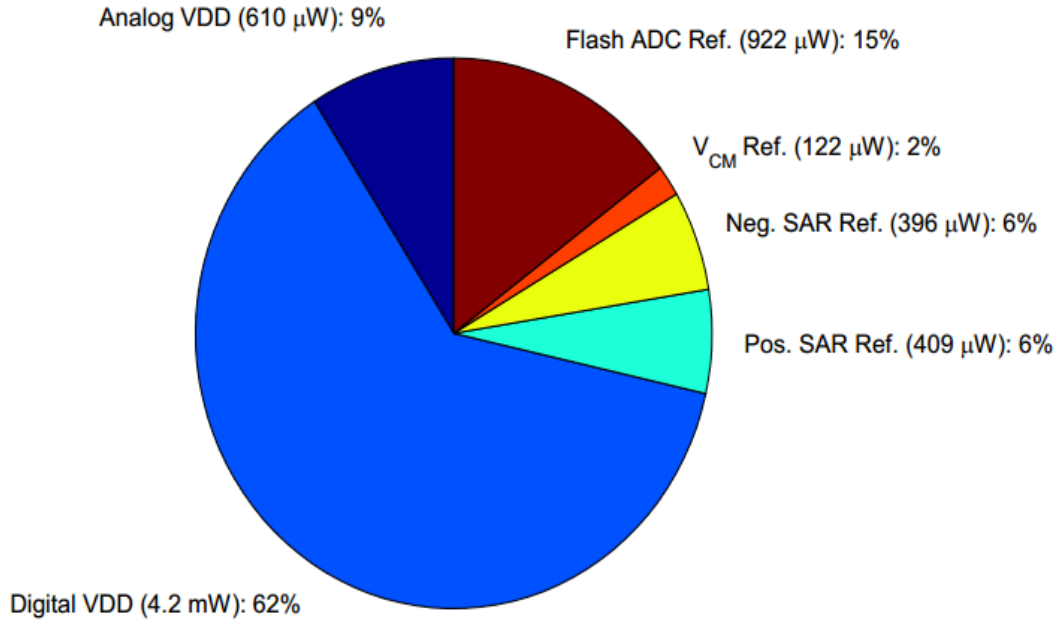

Figure 5.27: Power consumption distribution of single channel ADC.

5.6 Floorplan and Layout of Single Channel ADC

Floorplan of the 8-bit 1 GS/s single channel ADC is shown in Figure 5.28. Blocks are placed in accordance to the signal chain in order to reduce the interconnect delays. Top-level layout is shown in Figure 5.29. Size of layout is 250 µm x 200 µm.

Tape-out of the design was done in June 2015. Measurements are planned to take place in November 2015.

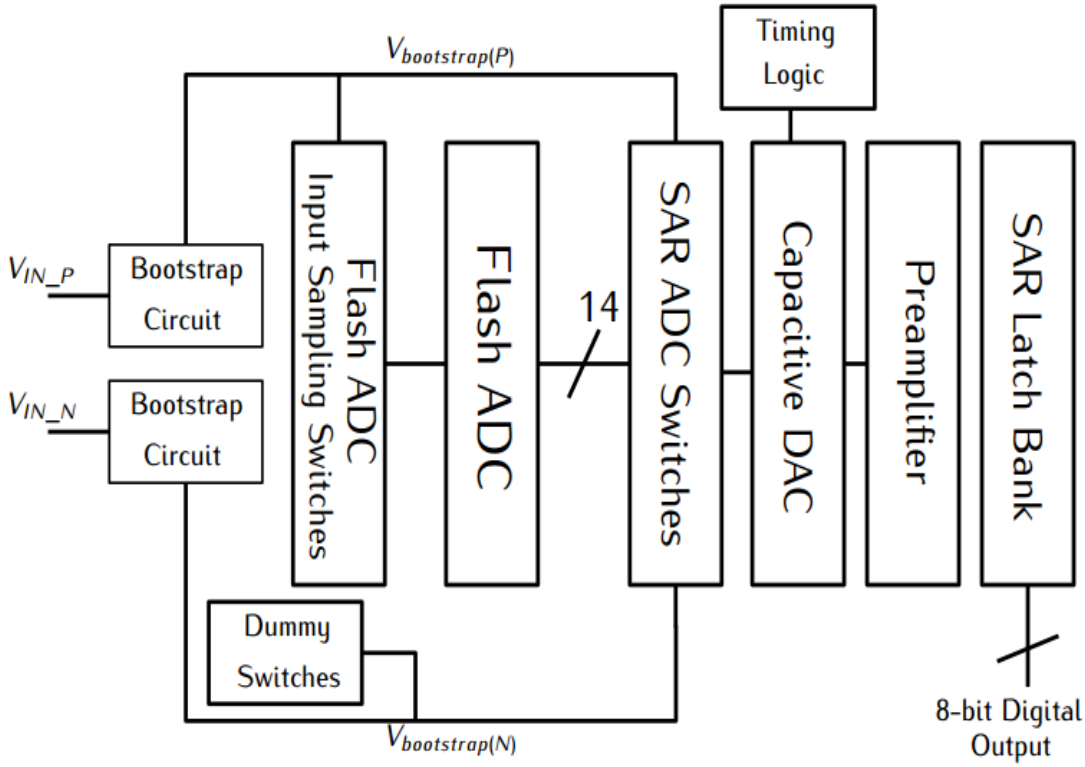

Figure 5.28: Floorplan of the ADC core.

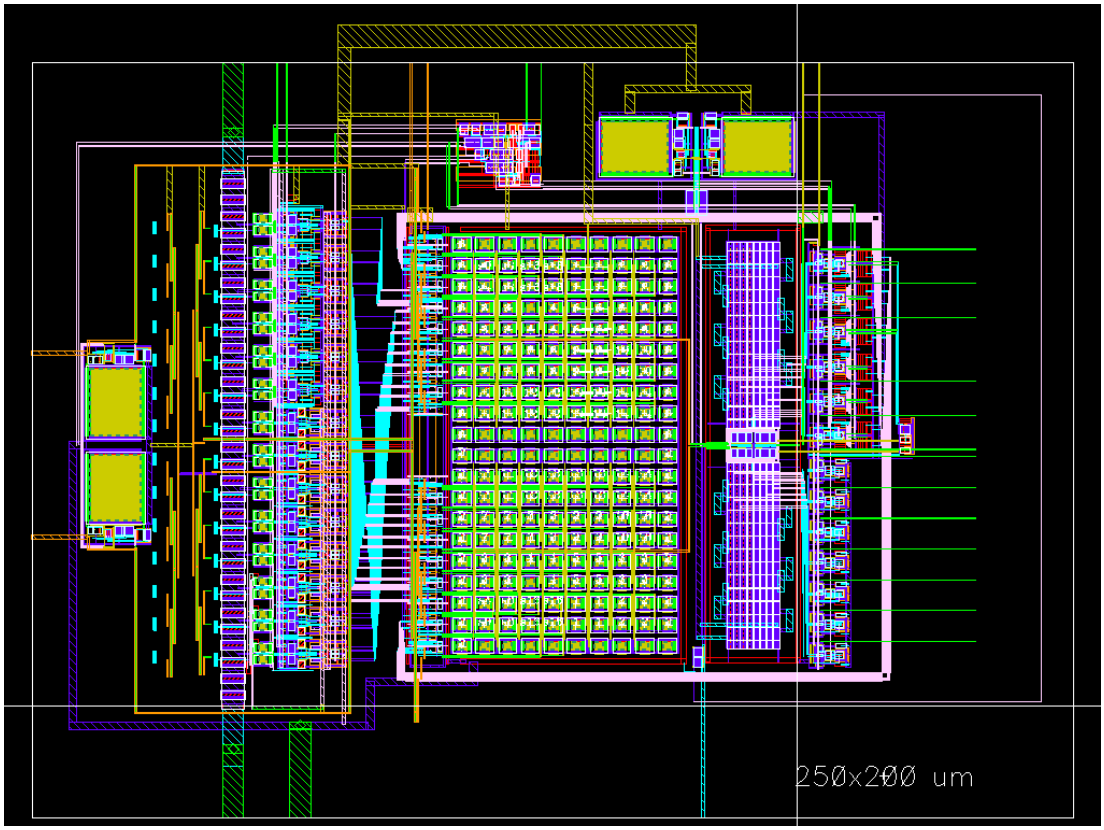

Figure 5.29: Top-level layout of ADC core.

6. CONCLUSIONS AND RECOMMENDATIONS

In this thesis, an 8-bit 1 GS/s multi-bit per cycle ADC is designed and laid-out on 65 nm CMOS process. Calibration schemes are avoided since ADC uses a novel search algorithm based on redundancy. Post-layout simulations have shown that the INL of the ADC is between ± 1 LSB and ENOB is 7.92 for $f_{in} = 243\ MHz$.

A novel latch with embedded preamp is proposed in Chapter 4. It has shown with simulations that this latch has a significant latch time, power and kickback noise advantage over the conventional sense amplifier latch. Latch is employed in the coarse conversion flash ADC as well as the intermediate and fine conversion SAR and results have shown the satisfying performance. As stated in Section 4.3.1 , maximum clock speed of the comparator is limited by the reset delay. Therefore this issue should be studied more to improve the maximum operation speed of the proposed latch.

A 14-level flash ADC is used for the coarse conversion of 3 MSBs. Post-layout simulation results have shown that designed flash ADC completes the conversion in 125 ps as projected. In order to increase the accuracy of the flash ADC, reference voltages have been sampled too. In result, reference levels of the flash ADC are ± 1 LSB(8-bit LSB) accurate, in post-layout. Benefits of this technique in power consumption should be studied, since it may allow using larger resistors in resistor ladder.

Since the ADC is intended to be used in a time-interleaved ADC, error mechanisms of time-interleaved ADCs are analyzed and a technique to improve SFDR is proposed. Behavioral simulations have shown that an SFDR improvement in the order of 10 dB can be achieved with this technique. As a next step, circuit level feasibility of the technique should be studied and technique should be improved in accordance with the circuit level implementation. As stated in Chapter 2, proposed randomization technique doesn't improve the SNR of the circuit. Therefore, technique should be combined with channel mismatch calibration schemes to be more effective.

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APPENDICES

APPENDIX A: MATLAB Code of TI-ADC Behavioral Model

APPENDIX A

```
% MAIN MODEL VARIABLES
nseries=1024
k=13;
fs=10e9;
fin=k/(nseries)*fs;
Ts=1/fs;
A=0.05;
Nch_cre = 16;
Nch = 8;
x_freq = zeros(nseries,1);
for i = 1:nseries
x_freq(i,1) = i * fs / nseries;
end
%dt = zeros(Nchannel,1);
x_chan = zeros(Nch,1);
x_chan_gain = zeros(Nch,1);
x_chan_skew = zeros(Nch,1);
%----------------------------------------%
%OFFSET ERROR
mu_off = 0;
sigma_off = 4e-3;
off = zeros(Nch, 1);
off = mu_off + sigma_off.*randn(Nch,1);
for i=1:nseries
 x_sig(i)=A*sin(2*pi*fin*i*Ts);
 for m=1:Nch
 x_chan(m,i)= off(m,1) + A*sin(2*pi*fin*i*Ts);
 end
 time(i)=i;
end
sp=20*log10(abs(fft(x_sig)));
spmax=max(sp);
sp=sp-spmax;
```

```
figure(1)
plot(sp)
title( 'Spectrum wout error' )
grid
% Pick samples in linear fashion (Standard TI-ADC)
for j=1:nseries/Nch
 for l=Nch:-1:1
 y(Nch*j-(l-1))=x_chan((Nch+1)-l,Nch*j-(l-1));
 end
end
error_off = x_sig - y;
figure(2)
plot(time,x_sig, time, y, time, error_off)

title( 'Waveforms ideal and w error (offset)' )
xlim([ 1 79])
ylim([ -0.06 0.06])
grid
spy=20*log10(abs(fft(y)));
spymax=max(spy);
spy=spy-spymax;
figure(11)
plot(x_freq./fs, spy)
grid
title( 'Spectrum of standard TI (offset error) - f
norm' );
%----------------------------------------%
%GAIN ERROR
mu_gain = A;
sigma_gain = 0.05*A;
A_chan = zeros(Nch,1);
gain = mu_gain + sigma_gain.*randn(Nch,1);
for i=1:nseries
 x_sig(i)=A*sin(2*pi*fin*i*Ts);
 for m=1:Nch
```

```
 x_chan_gain(m,i)= gain(m,1)*sin(2*pi*fin*i*Ts);
 end
 time(i)=i;
end
% Pick samples in linear fashion (Standard TI-ADC)
for j=1:nseries/Nch
 for l=Nch:-1:1
 y_gain(Nch*j-(l-1))=x_chan_gain((Nch+1)-l,
Nch*j-(l-1));
 end
end
error_gain = x_sig - y_gain;
figure(4)
plot(time,x_sig, time, y_gain, time, error_gain)
title( 'Waveforms ideal and w error (gain)' )
xlim([ 1 79])
ylim([ -0.06 0.06])
grid
spy_gain=20*log10(abs(fft(y_gain)));
spymax_g=max(spy_gain);
spy_gain=spy_gain-spymax_g;
figure(12)
plot(x_freq./fs, spy_gain)
%xlim([ 0 nseries/2])
grid

title( 'Spectrum of standard TI (gain error) - f norm' );
%----------------------------------------%
%TIMING ERROR
mu_skew = 0;
per = 1;
sigma_skew = per*Ts;
skew_chan = zeros(Nch_cre,1);
skew = mu_skew + sigma_skew.*randn(Nch_cre,1);
% Initialize the ideal and skewed sine waves
```

```
for i=1:nseries
 x_sig(i)=A*sin(2*pi*fin*i*Ts);
 for m=1:Nch_cre
 x_chan_skew(m,i)=A*sin(2*pi*fin*i*Ts)+skew(m,1)
*A*2*pi*fin*cos(2*pi*fin*i*Ts);
 %dt(m,1)*A*2*pi*fin*cos(2*pi*fin*i*Ts)
 end
 time(i)=i;
end
% Pick samples in linear fashion (Standard TI-ADC)
for j=1:nseries/Nch
 for l=Nch:-1:1
 y_sk(Nch*j-(l-1))=x_chan_skew((Nch+1)-l,Nch*j-
(l-1));
 end
end
error_sk = x_sig - y_sk;
figure(6)
plot(time,x_sig, time, y_sk, time, error_sk)
title( 'Waveforms ideal and w error (timing)' )
xlim([ 1 79])
ylim([ -0.06 0.06])
grid
spy_sk=20*log10(abs(fft(y_sk)));
spymax_s=max(spy_sk);
spy_sk=spy_sk-spymax_s;
figure(13)
plot(x_freq./fs, spy_sk)
%xlim([ 0 nseries/2])
grid
title( 'Spectrum of standard TI (timing error) - f
norm' );
%----------------------------------------%
%RANDOMIZATION (IDEAL) 8 + 2
Nch_main = 8;
```

```
Nch_red = 2;
Nchannel = Nch_main + Nch_red;

yscr = randomizer_parametric(Nch_main,Nch_red,nseries,
x_chan_skew);
spyscr=20*log10(abs(fft(yscr)));
smax=max(spyscr);
spyscr=spyscr-smax;
figure(8)
plot(spyscr)
grid
title( 'Spectrum of Proposed TI 8 +2 Random' );
xlabel('Frequency' );
ylabel('dBFS' );
figure(301)
subplot(2,1,1), plot(x_freq./fs,spyscr)
title( 'Spectrum of Proposed TI normal 8+2' );
xlabel('Frequency [f / f_s]' );
ylabel('DFT Magnitute [dBFS]' );
grid
%----------------------------------------%
%RANDOMIZATION (IDEAL) 8 + 4
Nch_main = 8;
Nch_red = 4;
Nchannel = Nch_main + Nch_red;
yscr_84 = randomizer_parametric(Nch_main,Nch_red,
nseries,x_chan_skew);
spyscr=20*log10(abs(fft(yscr_84)));
smax=max(spyscr);
spyscr=spyscr-smax;
figure(9)
plot(spyscr)
grid
title( 'Spectrum of Proposed TI 8 + 4 Random' );
xlabel('Frequency' );
```

```
ylabel('dBFS' );
figure(101)
subplot(2,1,1), plot(x_freq./fs,spy_sk)
title( 'Spectrum of Proposed TI normal' );
xlabel('Frequency [f / f_s]' );
ylabel('DFT Magnitute [dBFS]' );
grid
subplot(2,1,2), plot(x_freq./fs,spyscr)
title( 'Spectrum of Proposed TI 8 + 4 Random' );
xlabel('Frequency [f / f_s]' );
ylabel('DFT Magnitute [dBFS]' );
grid
figure(301)
subplot(2,1,2), plot(x_freq./fs,spyscr)

title( 'Spectrum of Proposed TI 8 + 4 Random' );
xlabel('Frequency [f / f_s]' );
ylabel('DFT Magnitute [dBFS]' );
grid
%----------------------------------------%
% PATTERN GENERATION
length = 16; % Pattern length
repeat = nseries / length;
Nch_tot = Nchannel;
pattern_matrix = zeros(Nch_tot, length);
flag_matrix = zeros(Nch_tot, length);
pattern_matrix(1,1) = 1;
flag_matrix(1,1:Nch_main) = 1;
pattern_matrix(2:Nch_tot,1) = 0;
for i = 2:length
 flag = 0;
 while flag == 0;
 ch = randi(Nch_tot,1);
 if flag_matrix(ch,i) == 0
 pattern_matrix(ch,i) = 1;
```

```
 flag_matrix(ch,i:(i+Nch_main)) = 1;
 flag = 1;
 else flag = 0;
 end
 end
end
pattern_matrix_long = pattern_matrix;
for u = 1:repeat-1
 pattern_matrix_long = [pattern_matrix_long,
pattern_matrix];
end
ADC_out = zeros(nseries,1);
for i = 1:nseries
 ADC_out(i,1) = pattern_matrix_long(:,i)' *
x_chan_skew(1:Nch_tot,i);
end
spyscr_lim=20*log10(abs(fft(ADC_out)));
smax_lim=max(spyscr_lim);
spyscr_lim=spyscr_lim-smax_lim;
figure(200)
subplot(2,1,1), plot(x_freq./fs, spyscr_lim)
title([ 'Randomization with a fixed pattern length
(Length =' ,num2str(length), ')' ], 'FontWeight' , 'bold' )
grid

%%% LONGER PATTERN
length = 256; % Pattern length
repeat = nseries / length;
Nch_tot = Nchannel;
pattern_matrix = zeros(Nch_tot, length);
flag_matrix = zeros(Nch_tot, length);
pattern_matrix(1,1) = 1;
flag_matrix(1,1:Nch_main) = 1;
pattern_matrix(2:Nch_tot,1) = 0;
for i = 2:length
```

```
 flag = 0;
 while flag == 0;
 ch = randi(Nch_tot,1);
 if flag_matrix(ch,i) == 0
 pattern_matrix(ch,i) = 1;
 flag_matrix(ch,i:(i+Nch_main)) = 1;
 flag = 1;
 else flag = 0;
 end
 end
end
pattern_matrix_long = pattern_matrix;
for u = 1:repeat-1
 pattern_matrix_long = [pattern_matrix_long,
pattern_matrix];
end
ADC_out = zeros(nseries,1);
for i = 1:nseries
 ADC_out(i,1) = pattern_matrix_long(:,i)' *
x_chan_skew(1:Nch_tot,i);
end
spyscr_lim=20*log10(abs(fft(ADC_out)));
smax_lim=max(spyscr_lim);
spyscr_lim=spyscr_lim-smax_lim;
figure(200)
subplot(2,1,2), plot(x_freq./fs, spyscr_lim)
title([ 'Randomization with a fixed pattern length
(Length =' ,num2str(length), ')' ], 'FontWeight' , 'bold' )
grid
```

CURRICULUM VITAE

Name-Surname: Alper AKDİKMEN

Place and Date of Birth: Çorum-TURKEY, 16.02.1988

E-Mail: alperakdikmen@gmail.com

EDUCATION:

- **B.Sc.:** Electronics Engineering / Istanbul Technical University

PROFESSIONAL EXPERIENCE:

- Researcher on TUBITAK (The Scientific and Technological Research Council of Turkey) Project at ITU VLSI Labs (Jan. 2013 – Sep.2014)
- Analog-Mixed Signal Design Engineer Intern at Hittite Microwave Corp. Istanbul Design Center (Mar. 2012 – June 2012)

PUBLICATIONS/PRESENTATIONS ON THE THESIS:

- Muratore, Dante Gabriel; Akdikmen, Alper; Maloberti, Franco, "Very high-speed CMOS comparators for multi-GS/s A/D converters," in *Ph.D. Research in Microelectronics and Electronics (PRIME), 2015 11th Conference on* , vol., no., pp.240-243, June 29 2015-July 2 2015.