ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

TUNABLE WINDOW COMPARATOR APPLICATIONS IN CURRENT-MODE CIRCUITS

M.Sc. THESIS

Melek KURNAZ

Department of Electronics and Communications Engineering

Electronics Engineering Master Programme

MAY 2014

ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

TUNABLE WINDOW COMPARATOR APPLICATIONS IN CURRENT-MODE CIRCUITS

M.Sc. THESIS

Melek KURNAZ
(504081214)

Department of Electronics and Communications Engineering

Electronics Engineering Master Programme

Thesis Advisor: Prof. Dr. Serdar OZOGUZ

MAY 2014

İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

AKIM MODLU DEVRELERDE AYARLANABİLİR PENCERE KARŞILAŞTIRICI UYGULAMALARI

YÜKSEK LİSANS TEZİ

Melek KURNAZ
(504081214)

Elektronik ve Haberleşme Mühendisliği Anabilim Dalı

Elektronik Mühendisliği Yüksek Lisans Programı

Tez Danışmanı: Prof. Dr. Serdar ÖZOĞUZ

MAYIS 2014

Melek Kurnaz, a **M.Sc.** student of ITU **Institute of / Graduate School of Science Engineering and Technology** student ID **504081214**, successfully defended the **thesis/dissertation** entitled "**TUNABLE WINDOW COMPARATOR APPLICATIONS IN CURRENT-MODE CIRCUITS**", which she prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

Thesis Advisor :	**Prof. Dr. Serdar OZOGUZ** Istanbul Technical University	.....
Jury Members :	**Yrd.Doç.Dr. Metin YAZGI** Istanbul Technical University	.....
	Prof. Dr. Cem GOKNAR Dogus University	.....

Date of Submission : 05 May 2014
Date of Defense : 30 May 2014

To my spouse and daughter,

FOREWORD

I would like to explain my sincere pleasure to my leading supervisor Serdar ÖZOĞUZ. Also, I appreciate that Cem GÖKNAR and Shahram MINAEI without their advice and unique support. Furthermore, I am grateful to all of my teachers in Doğuş University Electronics and Communications Engineering Department especially Merih YILDIZ.

Besides, I want to thank my whole family for their understanding and lovely support.

Finally, I have a heartful thank to my husband Deniz SERIFOGLU for his patience and support. Also, I dedicate to my cute daughter Ece SERIFOGLU whom has an important place in my life for six months.

May 2014

Melek KURNAZ
(Electronics and Communications Engineering)

TABLE OF CONTENTS

Page

ABBREVIATIONS

AMS	**:** Analog and Mixed Signal
BiCMOS	**:** Bipolar Complementary Metal Oxide Semiconductor
CC	**:** Core Circuit
CCII	**:** Second Generation Current Conveyor
CCO	**:** Current Controlled Oscillator
CMOS	**:** Complementary Metal Oxide Semiconductor
CVSL	**:** Cascode Voltage Switch Logic (CVSL)
FDE	**:** Functional Differential Equations
HDL	**:** Hardware Description Language
KCL	**:** Kirchhoff's Current Law
MOS	**:** Metal Oxide Semiconductor
MOSFET	**:** Metal Oxide Semiconductor Field Effect Transistor
MVCM	**:** Multiple Valued Current-Mode
NMOS	**:** N-Channel Mosfet
PMOS	**:** P-Channel Mosfet
PLL	**:** Phase Locked Loop
PWM	**:** Pulse Width Modulator
SC	**:** Switched Capacitor
SCMS	**:** Series Connected MOSFET Structure
SI	**:** Switched Current
SPICE	**:** Simulation Program for Integrated Circuits Emphasis
STA	**:** Static Timing Analysis
S-VCCS	**:** Subtraction Based Voltage Controlled Current Source
VCO	**:** Voltage Controlled Oscillator
VLSI	**:** Very Large Scale Integration

LIST OF TABLES

Page

LIST OF FIGURES

Page

TUNABLE WINDOW COMPARATOR APPLICATIONS IN CURRENT-MODE CIRCUITS

SUMMARY

In this thesis time delay calculations for current-mode circuits are investigated and equivalent circuit models for delay estimation are improved. This is one of the most important problems for us as Electronic Engineers. Many researches are already made for voltage-mode circuits, but our study is one of the few applications for current-mode circuits.

During this study, we used the CMOS Core Circuit in DU-TCC1209 which is designed and realized under Project 106E139 supported by the Scientific & Technological Research Council of Turkey (TUBITAK) in 2009 [5]. Primarily, a detailed literature survey was performed. Afterwards, missing in the literature identified and this work has continued on that topic. The first aim was to calculate time delay on current-mode circuits, then crosscheck the obtained results with simulation and bench tests. There are two phases in the calculation of the time delay: first, an equivalent circuit model has to be developed then analyzing the obtained equivalent circuit model, time delay formulae have to be extracted in terms of circuit elements' parameters. Some complicate calculation is performed with Wolfram Mathematica programme. Then simulations and bench tests have to be performed to confirm the theoretical analysis. To further verify the delay formulation in current-mode circuits, the CMOS Core Circuit in DU-TCC1209 [5] has been simulated, bench-tested and time delay results given for three different nodes.

After that with connecting two or four core circuits in a loop and a ring-oscillator circuit is proposed. The time delay of this ring-oscillator circuit is calculated. In the second step, the simulation results using SPICE Simulation Program are given and compared with theoretical ones. Finally, the ring-oscillator circuit is tested experimentally in the laboratory. That, calculated, simulated and measured delays agree quite well can be concluded. This application, which is obtained perfect results, throw light on the further suggestions such as phase detectors, modulators, clippers and comparators.

The publications and the presentations on the thesis are given end of the thesis.

AKIM MODLU DEVRELERDE AYARLANABİLİR PENCERE KARŞILAŞTIRICI UYGULAMALARI

ÖZET

Hazırlanmış olan bu tezde akım-modlu devrelerde zaman gecikmesi problemi ele alınmıştır. Üzerinde durmuş olduğumuz bu konu, biz Elektronik Mühendisleri için çok önemlidir. Öncelikli olarak detaylı bir literatür çalışması yapılmıştır. Bu sayede yapılan çalışmalardaki eksikler belirlenerek, çalışmalarımıza yön verilmiştir. Zaman gecikmesi hesapları ilk olarak 1964 yılında Burns tarafından gerilim-modlu devrelerde yapılmıştır. Devamında yapılan çalışmalarda ise gerilim-modlu devrelerle ilgili pek çok çalışma yapılmıştır. Ancak modern entegrasyon teknolojisinin yüksek hız, düşük güç tüketimi ve düşük güç kaynağı gibi ihtiyaçları artttığından akım modlu devrelerle ilgili çalışmalar önem kazanmıştır. Literatür araştırmasının gösterdiği gibi akım-modlu devrelerin, gerilim-modlu devrelerle kıyaslandığında hız, bantgenişliği, duyarlılık gibi pek çok avantajı vardır. Tüm bu ihtiyaçlar ışığında akım-modlu devrelerde zaman gecikmesi hesaplanması büyük önem kazanmaktadr. Belirtmek gerekirse, bu çalışma akım-modlu devrelerle yapılan çok az uygulamalardan biridir. Yapılan birkaç çalışmadan kısaca bahsedilmiş ve bizim çalışmamız yanındaki eksikleri de belirtilmiştir.

Birincil amacımız akım-modlu devrelerde zaman gecikmesini hesaplamak ve sonrasında elde edilen değerlerin benzetim ve test devresi ile sağlamasını yapmaktır. İkincil amacımız ise elde edilen formülleri kullanılarak ring osilatör uygulaması geliştirmektir.

Bu tezdeki temel amaç, akım-modlu bir devrede zaman gecikmesini hesaplayan basit bir formül elde etmektir. Zaman gecikmesi hesabı iki aşamadan oluşmaktadır. Birinci aşama, eşdeğer devre modeli tasarlamak ve sonrasında elde edilen eşdeğer devre modelinin analizini yapmaktır. Bunun için iki tane PMOS içeren basit akım aynasıyla oluşmuş bir devre seçildi ve gecikme tahmini yapabilmek için eşdeğer devre modeli geliştirilmiştir. Kirchhoff akım yasası ile elde edilen denklemden yola çıkarak akım değerinin %50'ye çıktığı andaki zaman elde edilmeye çalışılmıştır. Çünkü zaman gecikme problemlerinde giriş-çıkış akımlarının yarıya yükseldiği ya da düştüğü andaki fark zaman gecikmesini vermektedir. Ortalama gecikmeyi hesaplamak için ise düştüğü ve yükseldiği kenardaki gecikmelerin ortalaması alınarak bulunabilir. Bu bilgiler ışığında basit akım aynasından oluşan iki PMOS transistörlü devrenin zaman gecikmesi için çok basit bir denklem elde edilmiştir. Öncelikli olarak çıkış direnci eklenmeden yapılan bu hesaplar aynı şekilde çıkış direnci eklenerek de tekrarlanmıştır. Elde edilen formül çıkış direnci eklenmemiş hali kadar basit değildir. Ancak iki formülün de doğruluğunu görmek için, çıkış direnci sonsuz alınarak denklem çözülmüştür. Bu formüller benzer yapıdaki pek çok akım-modlu devreye uyum sağlamaktadır. Formüllerden görülebileceği gibi gecikmeyi yaratan en büyük etken parazitik kapasitelerdir. Bu kapasitelerin değerini düşürmek, gecikmeyi büyük ölçüde düşürecektir. Tezin diğer bir amacı ise, önerilen formülleri bir uygulamada kullanmaktır. 2009 yılında TÜBİTAK projesi olarak tasarlanan ve gerçeklenen DU-TCC1209 CMOS çekirdek devresi kullanılarak hesaplamaların doğruluğu gösterilmiştir. Kullanılan bu devre iki eşik devresi ve bir fark devresinden oluşmaktadır. Akım aynaları kullanılarak da kontrol akımları eşik devrelere aktarılmıştır. Giriş akımı I_{in} , I_1 ve I_2 akımlarının arasında bir değerde ise çıkış akımı

I_{out} ise I_H kontrol akımı kadardır. Diğer durumlarda ise çıkış akımı sıfırı göstermektedir. Kontrol akımları sayesinde ayarlanabilme özelliğine sahip bu devre pek çok uygulama için kullanılabilir.

Kullanılan çekirdek devrede, birinci düğüm için önerilen denklem kullanılarak zaman gecikme hesapları yapılmıştır. Formülden de görülebileceği gibi eşdeğer kapasitenin hesaplanması gerekmektedir. Bir MOS devredeki parazitik kapasiteler, transistorun çalışma aralığına göre değişiklik göstermektedir. Devredeki transistorların doymada çalıştığı düşünülerek hesaplamalar yapılmıştır. Transistor doymada çalıştığında ise C_{gs} ve C_{db} kapasiteleri ile overlap kapasiteleri hesaba katılmıştır. Kapasitelerin hesaplanmasında kullanılan değerler SPICE modelinden alınmıştır. Birinci düğüm için eş değer kapasite hesaplanarak çıkış direnci yokken ve varken zaman gecikmesi hesaplanmıştır. Elde edilen değerlerden görülebileceği gibi çıkış direnci eklendiğinde gecikmede %10'luk bir artış olmuştur. Zaman gecikmesi ile ilgili hesaplamalar yapılırken karmaşık denklemleri çözmek için Wolfram Mathematica programı kullanılmıştır. Yine de elde edilen formülleri daha iyi açıklamak için Ek-C'de matematiksel ifadeler detaylı olarak verilmiştir.

Çekirdek devrenin tamamının zaman gecikmesini hesaplayabilmek için girişten çıkışa olan katların hesaplarının ayrı ayrı yapılabilmesi gerekmektedir. Node 3 olarak kullandığımız ikinci farklı tipteki devre yapısı için benzer gecikme formülü elde edilmiştir. Yine parazitik kapasitelere bağlı basit bir denklem bulunmuştur. Üçüncü farklı tipteki devremiz ise Node 5 olarak belirtilen düğümdür. Her üç düğüm için bulunan formüllerden de anlaşılacağı gibi parazitik kapasite değerlerini düşürmek zaman gecikmesinin düşmesindeki en büyük etkendir. Tüm hesaplamaların yapılmasıyla çekirdek devrenin toplam gecikmesi hesaplanabilir. Devrenin girişinden çıkışına bakıldığında birinci ve ikinci düğüm için t_1, üçüncü düğüm için t_2, dördüncü düğüm için transistor boyutları üçüncü düğümdekinin dörtte biri olduğu için $0.25t_2$ ve beşinci düğüm için t_3, toplam gecikme ise bu beş düğümün art arda bağlı olduğu için toplanmasıyla bulunur.

Teorik analizi doğrulamak için SPICE benzetim programı kullanılmıştır. $0.35\mu m$ TSMC CMOS teknoloji parametreleri ile simülasyonlar gerçekleştirilmiştir. Her üç düğüm için ayrı ayrı hesaplar yapıldığı gibi simülasyonlar da yapılmıştır. Ayrıca birinci düğüm için yapılan bir analiz giriş akımı arttıkça, zaman gecikmesinin azaldığını da göstermektedir. Çekirdek devrenin tamamı için de simülasyon yapıldığında, hesaplamalarla elde edilen değerlerin büyük ölçüde birbirini doğruladığı gözlenmiştir. Teorik hesapların yanında simülasyon sonuçları ile de sağlaması yapılan bu çalışmada son aşama ise laboratuvarda deneysel olarak test edilmesidir. Öncelikli olarak iki PMOS'dan oluşan devre CD4007 kullanılarak test edilmiştir. Ardından DU-TCC1209 CMOS kullanılarak tüm çekirdek devrede test edilmiştir. Burada elde edilen değer teorik ve simüle edilen değerlerle büyük oranda benzerlik sağlamış olsa da ölçüm ucu kapasitelerinden ve parazitik etkilerden kaynaklı olarak iki katı bir fark görülmüştür. Laboratuvar ortamını iyileştirebilmek aradaki farkı azaltacaktır.

Tek bir çekirdek hücrenin tüm analizi yapıldıktan sonra, bu yapı ring osilatör uygulamasını önermek için kullanılmıştır. Ard arda iki tane çekirdek devrenin bağlanmasıyla basit bir ring osilatör oluşturulmuştur. Öncelikli olarak teorik analizi yapılan devrenin daha sonra simülasyon sonuçları ile karşılaştırılması yapılmıştır. Osilasyon frekansı teorik olarak hesaplandığı gibi yapılan benzetimlerle üç ayrı değerlerle test edilmiştir. Kontrol akım değerlerinin artmasıyla osilasyon frekansının

da arttığı görülmüştür. Üçüncü aşamamız ise DU-TCC1209 CMOS çekirdek devresi kullanarak laboratuvar ortamında testini sağlamaktır. Ancak bu şekilde ard arda bağlanmasıyla zaman gecikmesi arttığından osilasyon frekansı da düşmektedir. Benzer şekilde dört çekirdek devrenin peş peşe bağlanmasıyla dört bloklu ring osilatör devre yapısı önerilmiştir. İhtiyaç duyulan osilasyon frekansına göre iki ya da dört bloklu ring osilatör devresi kullanılabilir.

Yapılan çalışmayı genel olarak değerlendirmek gerekirse, elde edilen basit formüller akım-modlu pek çok devreye uyarlanabilir ve böylece hesaplamalar sayesinde gecikme minimum düzeye ingirgenebilir. Önerilen ring osilatör yapısı da çeşitli ihtiyaçlara göre kullanılabilir.

Hesaplanan, simüle edilen ve ölçülen gecikmeler birbirine çok yakın değerler vermiştir. Ölçüm sonuçlarının elde edilen değerlerin iki katı kadar farklı çıkması laboratuvar imkanlarının yetersizliği ve parazitik etkilerden kaynaklanmaktadır.

Elde edilen iyi sonuçlar sonraki çalışmalarımıza da ışık tutacaktır. Bu konu ile ilgili yapılabilecek sonraki çalışmalardan bazıları şöyle sıralanabilir: faz dedektörleri, modülatörler, karşılaştırıcılar ve kırpıcı devrelerdir.

Bu tezden türetilen bildiri ve yayınlar son bölümde verilmiştir.

1. INTRODUCTION

Nowadays, modern integration technologies are in a serious development stage, because of the requirements of higher speed, lower power consumption and lower power supply values. Due to the reduction in the dimensions of integration devices, maximum voltage ratings are reduced as well. The reduction in supply voltage values does not limit the design of digital circuits; but the design of high performance analog integrated circuits with low supply voltages becomes more complicated.

In this case, there is a small amount of integrated devices in digital integration technologies for circuit design. In the worst convenient scenario, there are only transistors suitable are in order to designing analog circuit. Infrequently, there might be capacitances and resistors. However, in this case there are disadvantages such as small values and parasitic components. Therefore, if it is desired quickest integration technologies suitable, it typically prevent to active components in the propose of integrated analog circuits [1].

Current-mode circuit design can be considered as a solution to design high-performance analog circuits with lower supply voltages. A literature survey shows that current-mode circuits have many advantages in comparison with voltage-mode circuits in terms of speed, bandwidth, accuracy, etc. In current-mode circuits, high voltage gain amplifiers, passive components with high sensitivity, summers are not required and that is why these circuits can be designed completely with transistors. This advantage provides the compatibility of current-mode circuits with digital processes as well [2,3].

Generally, in the literature, dynamic characteristics of CMOS inverter circuits are investigated; delay calculations of inverters were presented primarily by Burns in 1964 [4].

If it is needed to compare similar applications, the study provides the following advantages:

- has a simple mathematical expression.
- gives more physical comprehension about the current-mode circuits implement the existing core circuit in the ring oscillator application.

The motivation of these study as follows:

Secondary effect is a practical challenge. The expectation of these study dynamic performances of the system is developed. It is needed more realistic models. In the internal dynamics of many processes include second effect event. For examples of related studies biology, mechanics, physics. In addition, delays are presented by actuators, detectors and field networks in feedback loops. Thus, they are contained in communication area and information technologies such as service quality in MPEG video transmission or high-speed communication networks, computing times in robotics, etc. After all, delay times are used to reduce high order models.

1.1 Literature Survey

1.1.1 Delay models / Time delay

In literature, dynamic characteristics of the CMOS inverter circuit is investigated generally. CMOS inverter delay calculations was presented as primarily by Burns in 1964 [5].

One of the first studies on the time delay calculations is about series connected MOSFET structures (SCMS's) [6]. The usage of the new possible short channel MOS model provides analysis of CMOS gate delay. Including short channel effects, for CMOS inverters and SCMS's closed form time delay formulas are acquired. As is clear from here, the time delay of NAND/NOR compare with the time delay of inverter getting smaller in the area of submicrometer. The reason is that every MOSFET's V_{DS} and V_{GS} in the SCMS are lower than MOSFET inverter. In minimized MOSFET, the lower voltages respectively decrease and relieve the hard carrier speed saturation. This event support more extended use of NAND/NOR complex gates and Cascode Voltage Switch Logic (CVSL) which refers to a CMOS type logic family in the submicrometer circuit design [6].

In another study, for a different applications, CMOS inverter delay calculations and formulas are determined. In this embodiment, simple but practical α–power law

MOS model is suggested. This model is enclosed to containing the carrier velocity saturation effect caused by prominent in short channel MOSFET's. The model which operates in saturation region, is continuation of Shockley's square-law MOS model. By using this model for calculating delay, closed form statements are provided. If applications of this model is indicated as follows, closed form analytical statements are provided for calculating delay, short circuit power and logic threshold voltage of CMOS inverters. All applications were supported on the Shockley model, also all studies is essential to aware of the behaviour in submicrometer area. At the same time source and drain resistance is taken into consideration as delay statement. Source and drain resistance affect is play a significant role in assessment of delay retrogression a kind of parasitic diffusion resistance of MOSFET's and hot carrier retrogression affect [5].

In another application, timing jitter is investigated in CMOS ring oscillators. In CMOS ring oscillators, the consequences of thermal noise in transistors on timing jitter compiled of source coupled differential delay cells is inquired. Correlation between delay component design variable and implicit in thermal noise jitter of the generated waveform are studied. In this structure delay control is used with phase detection for designing ring oscillator. Time delay of this ring oscillator is formulated by first order timing jitter decomposition. This is found out by the number of stages in the ring and the delay for each stage. In this study voltage-mode circuit structure is used for calculating delay calculation [7].

Some studies have been conducted on current-mode circuits. In 2004, delay line with continous time offset compensation is discussed. For Laguerre adaptive filter structure, second order fully differential offset compensated current-mode delay line is recommended. Current state enable to use minimum length of the transistors which enlarge the bandwidth without considerable increasing the power consumption [8].

High speed timing recognition outline by using delay tables is recommended for a wide ranging Multiple Valued Current-Mode (MVCM). This application is proposed because of the necessity of high performance arithmetic VLSI, in a lot of application areas, such as multimedia processing and intelligent signal processing. The proposed recognition consists of two main stages. The first stage is logic verification using Verilog AMS which is a Hardware Description Language (HDL) conceived for

analog and mixed signal systems. The second stage is delay estimation based on parasitic capacitance occupier static timing analysis (STA) tool which is standard timing verification methodology [9].

In another implementation is about Pulse Width Modulator (PWM). This study consist of the stability of current-mode controlling with time delay model of PWM. As with many studies in recent years, also in this study, the structure of the current-mode circuit proved to be many advantages compared to the structure of the voltage-mode circuit. Firstly time delay model of PWM in voltage-mode control is represented, and then time delay model of PWM in current-mode control is designed with additional current loop inside the external voltage loop. But in here, duty ratio is no more argument however is controlled by the inductor current. Recommended model exposes some supremacy as a simpler mathematical expression, gives more physical insight into the sample and of current loop and obtain preferable prediction of the critical condition of the current loop stability without of slope compensation [1].

In another study, CMOS wireless temperature sensor is designed with integrated radiating element. For this wireless temperature there are two ring oscillators. It is known that a ring oscillator is a sensitive circuit because temperature variances reason adjustments of oscillation frequency. The relation between frequency and temperature is the delay of each stage. This technique was applied that solving the problem of unwanted dependence on the bias voltage of the ring oscillation frequency [10].

In [11] the analytic step response of an NMOS current mirror has been examined. The settling time of the current mirror has been derived analytically. However, the output resistances of the transistors were not taken into account.

1.1.2 Ring oscillator

A ring oscillator is a structure consisted of an odd number of NOT gates. Their output oscillates between two voltage levels [12].

In literature ring oscillators are extensively used in phase locked loops (PLL). This is utilized for frequency synthesizers for their small die size, clock synchronization in microprocessors, clock and data recovery and a lot of implementation of polyphase

sampling [7]. Another applications of ring oscillators are as follows; voltage controlled oscillator in most phase locked loops is built from a ring oscillator, many wafers include a ring oscillator as part of the scribe line test structures which is used during wafer testing to measure the effects of manufacturing process variety.

In one of the studies, 3-stage inverting ring oscillator is proposed to acquire a formula for its frequency. Designed circuit structure is shown in Figure 1.1. As can be seen from the figure, inverting stage uses an NMOS device driving a current source *I* with an output capacitor *C.* Therefore there is no V_{dd} supply current spike generally contained in a static inverter and consumption of power depends on *I.* As a result of work done, for large NMOS or small current, the frequency alters linearly with the load current [13].

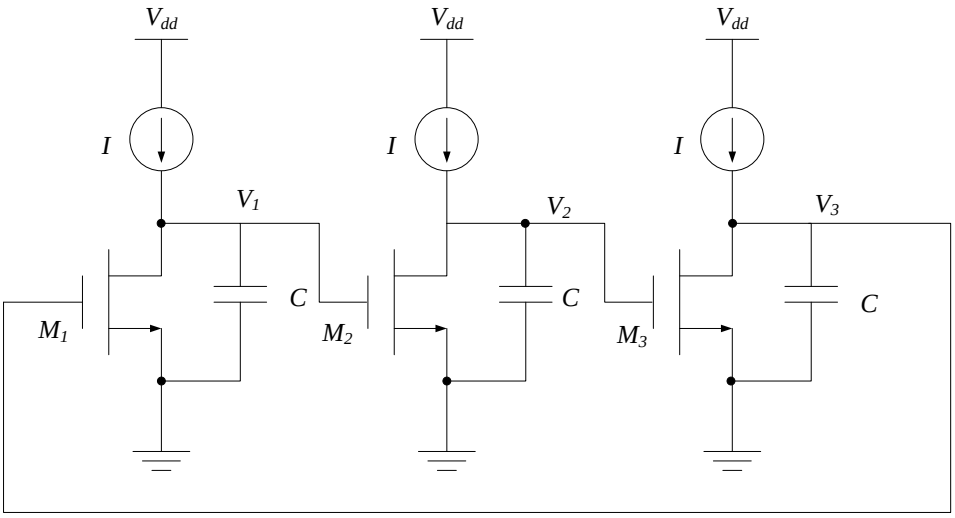


Figure 1.1 : A CMOS 3-stage inverting ring oscillator using current load [13].

A Dual Delay Path Ring Oscillator is presented by Chen and Lee. The designed structure which is shown in Figure 1.2 has two operation modes which mentioned as the diferential and common modes. The oscillation frequencies and output waveform characteristics help that distinguish each other the two operation modes. The main distinction among the operation modes is the output waveform characteristics. The tunning ranges are from 1.01 to 1.055 GHz for common-mode, 1.77 to 1.92 GHz for differential operations for differential four-stage dual delay path ring oscillator [14].

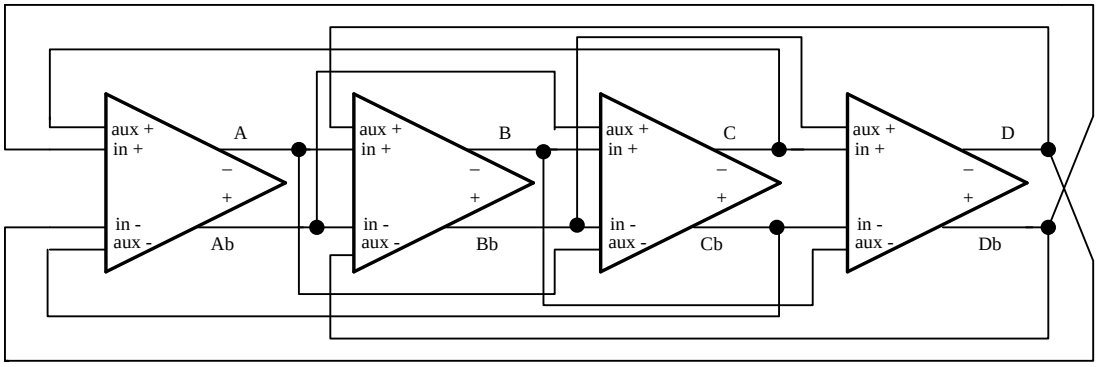


Figure 1.2 : Differential four-stage dual delay path ring oscillator [14].

One of the recent studies, VCO as is presented as a process variation compansated voltage controlled ring oscillator (VCO) with subtraction based voltage controlled current source (S-VCCS). In this study to compansate voltage controlled ring oscillators variation for process variations a simple methodolgy is proposed. The compensation is acquired by supplying the VCO with stable current which comes from S-VCCS. For implementing a current reference amplifier S-VCCS can be colligated to voltage to current converter. Also it can be used in differential ring VCOs, continous time filters and automatic gain control circuits to compensate corner variations [15].

1.2 Scope of Thesis

The aim of this thesis is to give a general calculation of time delay in current-mode circuits then to verify it by simulations and bench tests. There are two phases in the calculation of the time delay: first, an equivalent circuit model has to be developed then analyzing the obtained equivalent circuit model, time delay formulae have to be extracted in terms of circuit elements' parameters. A ring oscillator is proposed as two block and four block application. Its calculation is also extracted. Then simulations and bench tests have to be performed to confirm the theoretical analysis. To further verify the delay formulation in current-mode circuits, the CMOS Core Circuit in DU-TCC1209 [1] has been simulated, bench-tested and time delay results given for three different nodes.

The sequel of the thesis is organized as follows: in chapter 2, dynamic modelling of current mirror is clarified. Improvement of integration technologies, current-mode

building blocks and the advantages of current-mode circuits are explained. In chapter 3, design of equivalent circuit model is explained. There is a simple current-mode current-mirror circuit and its large-signal equivalent circuit model are given. The time delay formulation of the equivalent circuit model is extracted. In addition the effects of the parasitic capacitances on the delay calculations are considered. Time delay is calculated for three distinctive node and the total time delay is computed. SPICE simulations for three node and bench test results are presented. The time delay calculation is also computed in ring oscillator as two block and four block in chapter 4. As well, simulation results and bench test results provided theoretical consequence. Finally, some concluding remarks and further sugestion are given in chapter 5.

2. DYNAMIC MODELLING OF CURRENT MIRROR

2.1 Current-Mode Circuits

In recent studies, current-mode circuits present a better performance than voltage-mode structures in analog circuit design [8].

In Figure 2.1 process technologies are shown. These technologies effect on current-mode building blocks and systems. Besides, current-mode analog building blocks are shown in Figure 2.2.

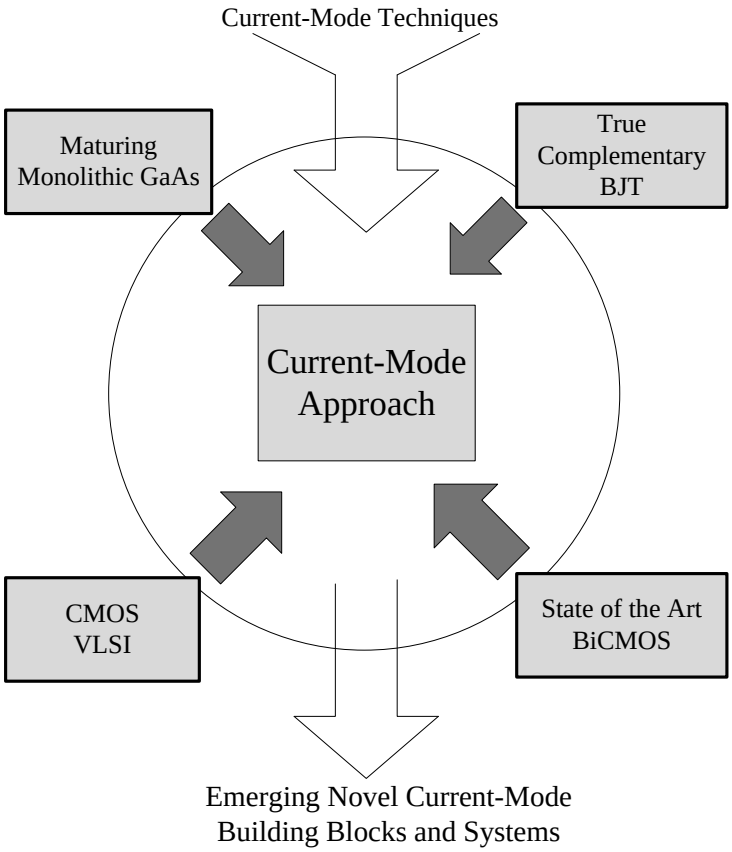


Figure 2. 1 : Process technologies and there impact on Current-Mode Building Blocks and Systems [2].

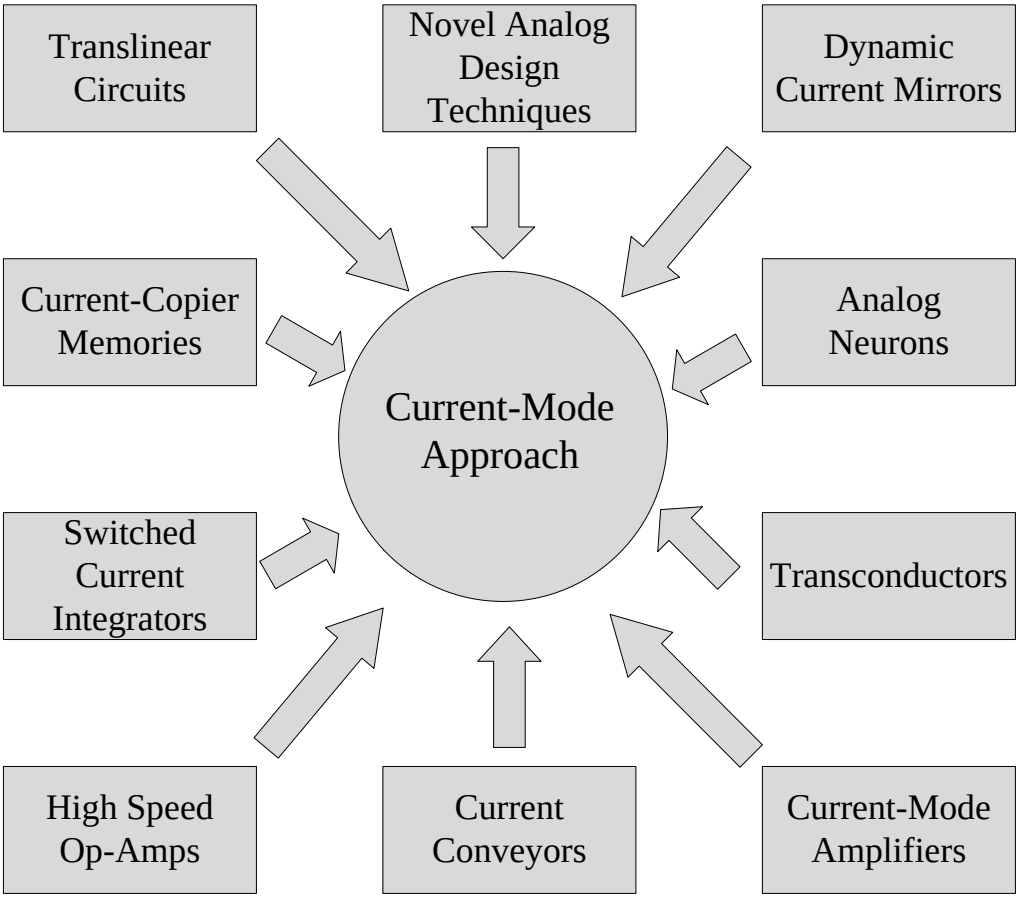


Figure 2.2 : Current-Mode Analog Building Blocks [2].

2.1.1 Improvement of integration technologies

Nowadays, the requirements of digital CMOS circuit design provide the improvement of modern integration technologies. While the size of the integrated devices reduction, the voltage ratings rapidly decrease. But the reduction of supply voltage do not constrain the design of digital circuits.

There are little integrated devices suitable for circuit design, in digital integration technologies. The worst case there will be analogue circuit design with only transistors. There may be resistors or capacitances, however their values may be small or there will be parasitic components. If desired that to optimize fastest integration technologies, there will be active components in analog circuits design.

The operational amplifier has attended as the basic constructing blocks in the analog circuit design while the innovation of integrated circuits. After that, the

execution necessities for analog circuits have been altered and new integrated analog circuit applications have came forth. At high closed-loop gain system acquires due to the stable gain-bandwidth product voltage-mode operational amplifier circuits have bounded bandwidth. Moreover, the fixed slew-rate of the operational amplifier involves the large-signal, high-frequency operation. That's why it is needed low voltage analog circuit techniques [16].

2.1.2 Stimulation for current-mode circuit design

There is a method for finding disjunctive; circuit implementation is to use current signals instead of voltage signals for signal processing. MOS transistors are more appropriate for manipulating currents rather than voltages just because common-source, common-gate and common-drain amplifier configurations have current at the output signal. In MOS current mirrors, base currents limit the accuracy so according to bipolar current mirrors, MOS current mirrors are more accurate and fewer sensitive to process configuration. Furthermore, MOS transistor circuits can be simplified by using current signals preferable to voltage signals. Therefore, integrated current-mode circuit actualizations nearer to the transistor level than the traditional voltage-mode actualizations and therefore simpler circuits and systems should result.

The parasitic capacitances are charged and discharged with voltage oscillation when signals are distributed as voltages. That limits the speed and increments the power consumption of voltage-mode circuits. Consequently, it is realizable to accomplish higher speed and lower dynamic power consumption with current-mode circuit processes. Current-mode connection circuits particularly display assuring performance.

The voltages in MOS transistor circuits are relative to the square root of the signal while the signal is carried for a current, whenever saturation region operation is acquired for the devices. Likewise, the voltages are proportional to the logarithm of the signal in bipolar transistor circuits. Hence, a decrease of supply voltage and a compressing of voltage signal swing are possible. This speciality is applied e.g. in log domain filters, switched current filters, and in non-linear current-mode circuits commonly. Unfortunately, because of the device mismatches this non-

linear procedure can yield an extravagant quantity of deformation for applications with high linearity demands. Therefore, to reduce the nonlinearity of the transistor transconductance, linearization methods are being applied. Thereby the voltage signal oscillation is not minimized.

Nevertheless, new results regular imply new problems. Sensitivity to mismatches is increment by the compressing of the voltage signal swing. Moreover, some current-mode techniques are very old such as the current feedback. They are used as developed voltage-mode signal processing building blocks instead of current-mode such as signal processing building blocks [16].

2.1.3 Evolution of current-mode building blocks

The first building block conceived for current signal processing is published in 1968 as current conveyor [17]. The improvement form of the current conveyor, which called the second-generation current conveyor CCII, is emerged in 1970. None of them became popular because of the integrated operational amplifier [18]. In forties, voltage-mode operational amplifiers notion had already been presented. In addition to this, integrated current conveyors were crucial to realize. In 1970s, PNP devices without high performance are used in the integration technologies [17-20].

In 1980's, fast PNP devices were presented in bipolar integration technologies. At that time, researchers realize that voltage-mode operational amplifier is not best solution to all analog circuit design problems. New surveys show that by using current conveyors, current-mode signal processing is presented. Additionally the current feedback operational amplifier can be produced as a commercial product [18-20].

Different circuit topologies and operation basis are essential for realizing current-mode circuits. In 1988, the fundamental of a MOS current copier was offered [21]. In 1989, the switched current (SI) principle was offered. Then switched capacitor (SC) circuits that do not need linear capacitors were presented as an alternative to the SI circuits [19].

Moreover, with a differential input and single ended output or with a single ended input and differential output, diverse suggestion for CMOS current-mode operational amplifier have been published [21].

2.1.4 Current-mode circuits advantages

A literature survey shows that current-mode circuits have many advantages according to the voltage-mode circuits. The current-mode circuits obtaining a better performance is these circuits usually are less complex and use less loop gain.

With regard to Schmid, the actual difference between current-mode circuits and voltage-mode circuits are arived from the distinctive studies of researchers [22].

Therefore, researchers who work on current-mode can give precious point of view to voltage-mode researchers while they try to design the circuits with low power, low voltage, high speed circuits [22].

If we want to summarily indicate the advantages of current-mode circuits according to the voltage-mode circuits, listed as follows:

- Lower power consumption**,**
- Smaller chip area,
- Higher gain variation,
- Circuit simplicity,
- Cost of higher distortion,
- Less loop gain,
- Faster.

2.2 Capacitances of the MOS Transistor

Switching rates are being limited with the lengths of the time interval required for charging and discharging capacitances contained in the MOS transistor. It is known that many of the capacitances in VLSI circuits are very small for measuring accurately. For circuit analysis, these parasitic capacitances must be calculated from device proportions and dielectric constants. The MOS transistor's significant capacitances are between the terminals of the transistor as shown in Figure 2.3. According to physical properties, these parasitic capacitances can be grouped under

three headings as thin oxide capacitances, junction capacitances and overlap capacitances [35].

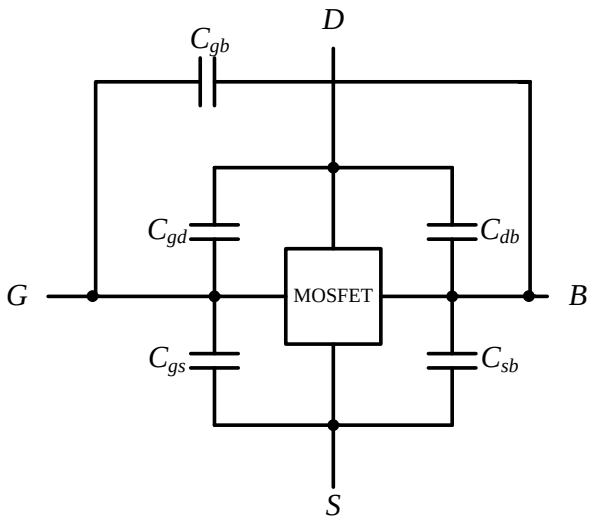


Figure 2.3 : Capacitances of the MOS transistor [9].

2.2.1 Thin oxide capacitance

In MOS transistors, the thin oxide capacitance is the most important capacitance. The thin oxide capacitances are consisted of C_{gs}, C_{gd}, and C_{gb} are symbolized by C_g. The two plates of the capacitances are defined as the gate and the channel. Among these two plates the dielectric material is the oxide. The gate capacitances C_g is found as the following equality:

$$C_g = C_{ox} \times W \times L \tag{2.1}$$

where C_{ox} is the capacitance per unit area of the gate dielectric is defined as:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \tag{2.2}$$

where t_{ox} is the gate oxide thickness and ε_{ox} is the permittivity of oxide can be found as:

$$\varepsilon_{ox} = 3.9 \times \varepsilon_o \tag{2.3}$$

where ε_o is the dielectric constant and the value of this constant is $8.85 \times 10^{-12} F/m$.

The gate capacitance is divided into three capacitances namely; the gate to source

capacitance C_{gs}, the gate to drain capacitance C_{gd}, and gate to bulk capacitance C_{gb}. These parasitic capacitances are calculated numerically depending on whether the device is in cut off, in linear or saturation regions as indicated in Figure 2.4.

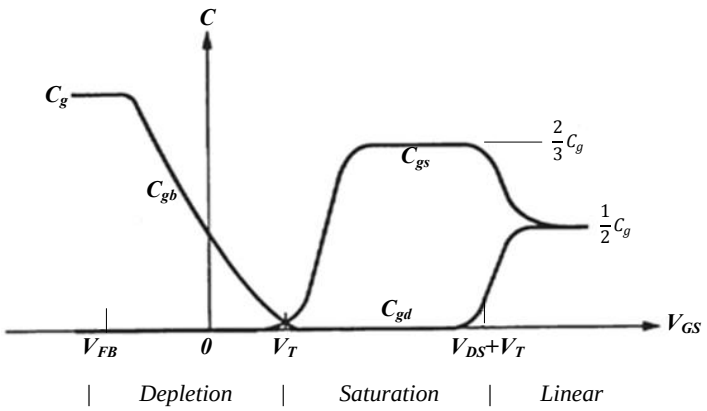


Figure 2.4 : MOS capacitance values with respect to region of operation [23].

when the device is in cut off the capacitances gate source and gate drain is equal to zero as shown in equality (2.4). The gate bulk capacitance is in (2.5).

$$C_{gs} = C_{gd} = 0 \quad \textbf{(2.4)}$$

$$C_{gb} = C_{ox} \times W \times L \quad \textbf{(2.5)}$$

when the device is in linear region the capacitances obtained as:

$$C_{gb} = 0 \quad \textbf{(2.6)}$$

$$C_{gs} \cong C_{gd} \cong ½\ C_{ox} \times W \times L \quad \textbf{(2.7)}$$

when the device is in saturation mode the parasiticic capacitances gate drain and gate bulk gives a value of zero as shown following equality:

$$C_{gd} = C_{gb} = 0 \quad \textbf{(2.8)}$$

The formula of the gate to source capacitance C_{gs} is given by:

$$C_{gs} = 2/3\ C_{ox} \times W \times L \quad \textbf{(2.9)}$$

where, C_{ox} is the capacitance per unit area of the gate dielectric, W and L are width and length of the transistor respectively.

2.2.2 pn junction capacitances

The source and drain regions and substrate form pn junctions that give rise to two additional capacitances. The junction capacitances are composed of source bulk and drain bulk capacitances respectively as symbolized C_{sb}, and C_{db}. Each of two capacitances is owing to the depletion charge of the source or drain diffusion area in substrate. These junction capacitances are very complicate to calculate by the three dimensional shape of the diffusion regions that constitute source substrate and the drain substrate junctions.

There are two types of junction capacitances calculate for NMOS device, in such a way that the bottom capacitance and the sidewall capacitance. The detailed junction capacitance (C_{db}) is found from the following equality:

$$C_{db} = \left(\frac{CJ}{\left(1+\frac{VDB}{PB}\right)^{MJ}} \times AD\right) + \left(\frac{CJSW}{\left(1+\frac{VDB}{PB}\right)^{MJSW}} \times PD\right) \quad \textbf{(2.10)}$$

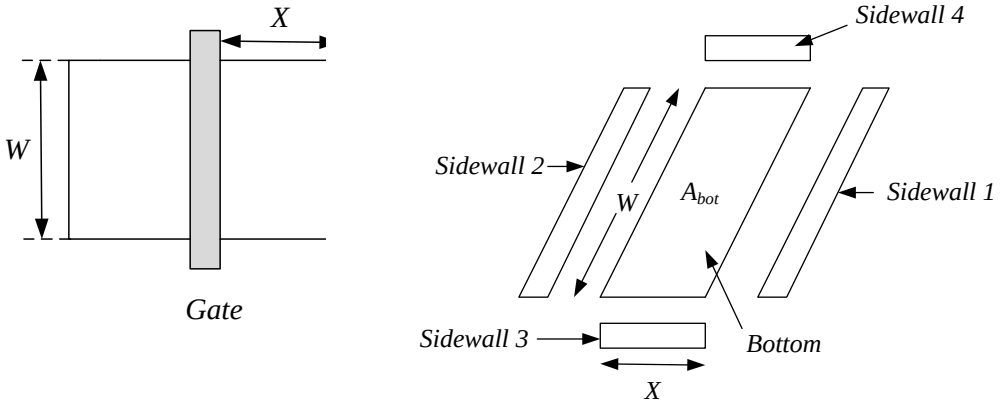
where CJ is the zero-bias body-junction capacitance per unit area over the drain-source region and $CJSW$ is the zero-bias body-junction capacitance per unit length along the sidewall (periphery) of the drain-source region. MJ is the grading coefficient for area component and $MJSW$ is the grading coefficient for the sidewall component; PB is the body-junction built in potential, AD is the area while PD is the perimeter of the drain region of MOSFET [24].

The formula AD as given by expression (2.11) where x_j called the junction depth and PD as given following equalities:

$$AD = 2(W * xj) + 2(X * xj)\ \ (X \cong L/2) \quad \textbf{(2.11)}$$

$$PD = 2 * (W + X) \quad \textbf{(2.12)}$$

The top view of the MOS transitor in Figure 2.5 defines the channel width W of the transistor and the extent X away from the gate of the region.



(a) Top view (b) Geometry

Figure 2.5 : Calculation of the MOS junction capacitance.

2.2.3 Overlap capacitance

The overlap capacitance is arising from lateral diffusion and fringing component. This voltage free capacitance is connected from gate to drain and from gate to source [22].

The capacitance due to lateral diffusion is computed as:

$$C_{ov}=W \times L_{ov} \times C_{ox} \qquad \textbf{(2.13)}$$

where L_{ov} is overlap length and typically, L_{ov} = 0.05 to 0.1L. C_{ox} is the capacitance per unit area as shown in Equation (2.2) and W is width of the transistor.

2.3 Time Delay

Time delay systems can be called a secondary effect or a dead-time system. In functional differential equations (FDEs) class, these systems can be included. Since 1963, there are lots of surveys and research papers [25].

The Input-Output (I-O) waveforms of the current-mirror circuit are shown in Figure 2.6. As can be seen from Figure 2.6, low to high time delay τ_{PLH} of MOS transistors can be defined as time duration between the initial time t_0 (the output current is at its minimum value) and the time t_1 (the output current increases to half of its maximum value). Similarly, high to low transition propagation delay τ_{PHL} is the time duration

required for the output to decrease to half of its maximum value from its maximum value. Thus, the propagation delay times τ_{PHL} and τ_{PLH} are found from Figure 2.6 as:

$$\tau_{PLH} = t_1 - t_0 \quad \textbf{(2.14)}$$

$$\tau_{PHL} = t_3 - t_2 \quad \textbf{(2.15)}$$

$$\tau_P = \frac{\tau_{PLH} + \tau_{PHL}}{2} \quad \textbf{(2.16)}$$

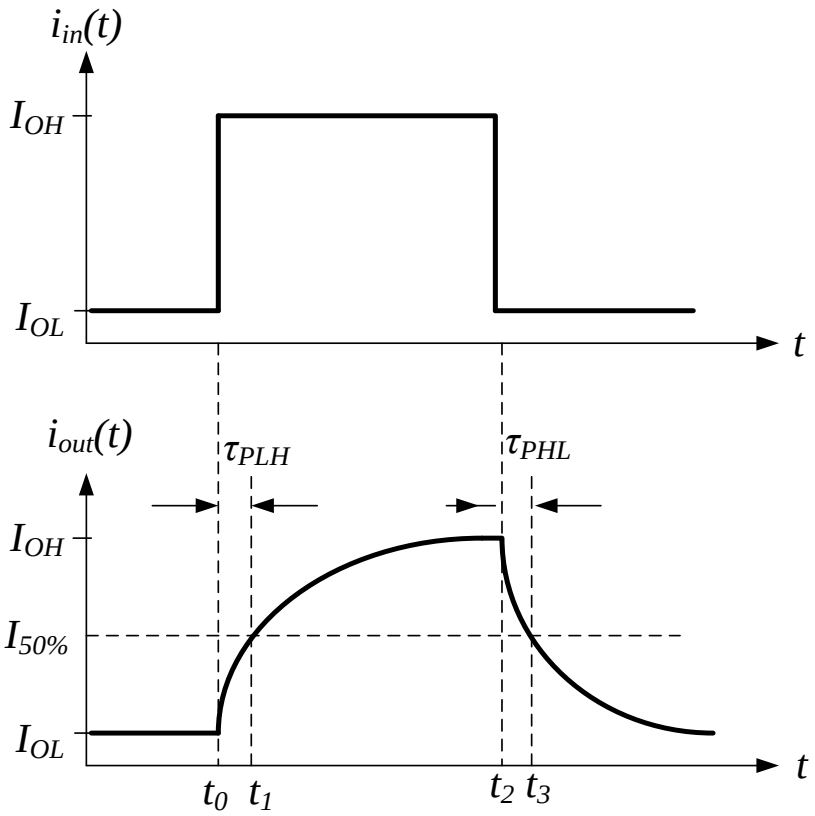


Figure 2.6 : I-O current waveforms.

There is another specification for output current rise and fall times as shown in Figure 2.7. τ_{fall} as called falling time can be clarified as the time necessary for the output current reduce from $I_{90\%}$ level to $I_{10\%}$ level. Similarly, τ_{rise} as called rising time can be clarified as the time necessary for the output current reduce from $I_{10\%}$ level to $I_{90\%}$ level. $I_{10\%}$ and $I_{90\%}$ current levels can be described as follows:

$$I_{10\%} = I_{OL} + 0.1(I_{OH} - I_{OL}) \quad \textbf{(2.17)}$$

$$I_{90\%} = I_{OL} + 0.9(I_{OH} - I_{OL}) \quad \textbf{(2.18)}$$

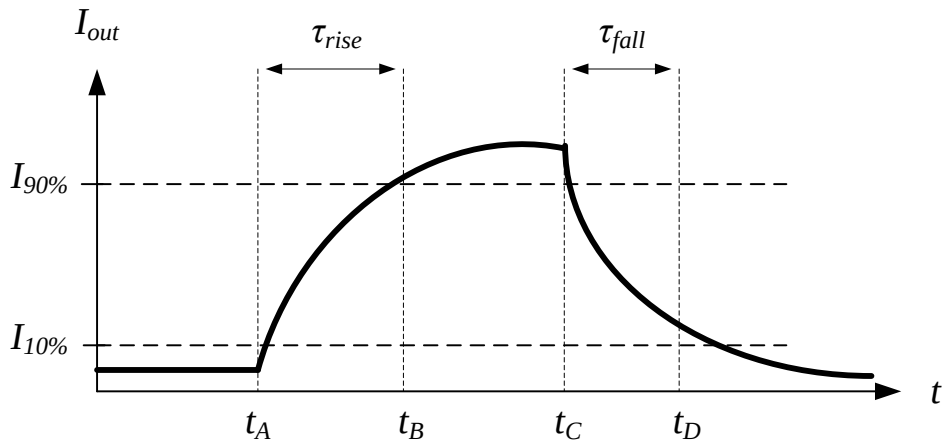


Figure 2.7 : Output current rise and fall times.

So that, the output τ_{fall} and τ_{rise} can be found from Figure 2.7 as the following equations:

$$\tau_{fall} = t_B - t_A \quad \textbf{(2.19)}$$

$$\tau_{rise} = t_D - t_C \quad \textbf{(2.20)}$$

2.4 Introducing Core Circuit

As an example for calculation of the time delay of the circuit, the CMOS Core Circuit which was developed as a classifier integrated circuit and manufactured as DU-TCC1209 in 2009 [13], has been used. The block diagram and the transfer characteristic of the core circuit are shown in Figure 2.8 and Figure 2.9, respectively.

The input-output transfer characteristics of the core circuit shown in Figure 2.9 can be expressed as:

$$I_{out} = \begin{cases} I_H & if \quad I_1 < I_{in} < I_2 \\ 0 & otherwise \end{cases} \quad \textbf{(2.21)}$$

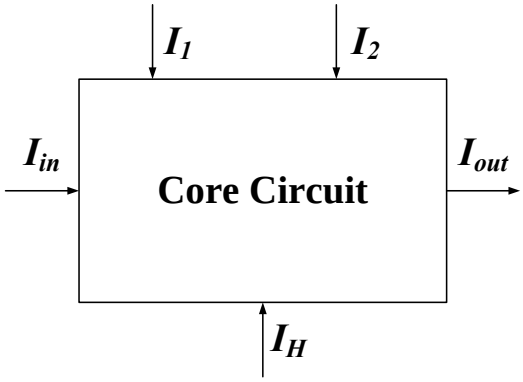


Figure 2.8 : Core circuit block diagram**.**

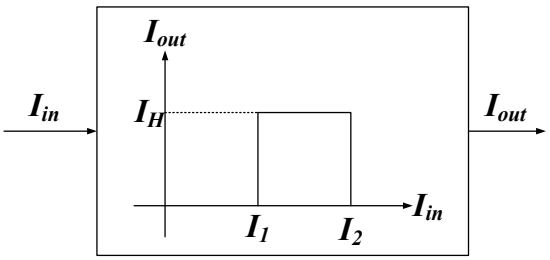


Figure 2.9 : Transfer characteristic of the core circuit.

The CMOS implementation of the classifier core circuit is shown in Figure 2.10. The core circuit is constituted with two threshold circuits and one subtructor circuit. I_1, I_2 and I_H called as external control currents. With simple current mirror structures, input currents are performed to the core circuit. The change of the output waveform in a horizantal position is provided by the currents I_1 and I_2, I_H describes the amplitude of the output waveform. The transistors M_1, M_2, M_4, M_5 and M_9, M_{10}, M_{12}, M_{13} create two threshold circuits shown in Figure 2.10. The transistors M_7 and M_8 are used to generate a subtractor circuit with simple current mirror structure. The transistors M_{15}, M_{16} and M_{17} are used to apply the same I_H current for the threshold circuits. Similarly, the transistors M_{18}, M_{19}, and M_{20} are used to apply the same I_{in} current to both of the threshold circuits.

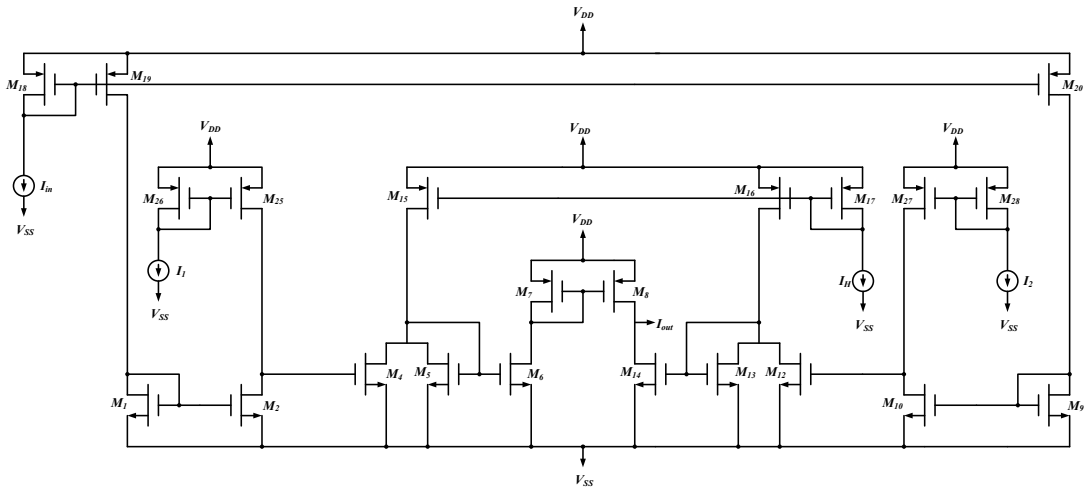


Figure 2.10 : CMOS implementation of the core circuit [26].

The core circuit in Figure 2.10 has been simulated with *0.35μm* TSMC CMOS technology parameters using SPICE simulation software. The supply voltages V_{DD} and V_{SS} were selected $\pm 1.65V$. The transistors dimensions are given in Table 2.1.

Table 2.1: Dimensions of the CMOS Transistors in Core Circuit.

MOSFET	W[μm]	L[μm]
M_1, M_2, M_9, M_{10}	42	1.05
M_7, M_8, M_{15}, M_{16}, M_{17}, M_{18}, M_{19}, M_{20}, M_{25}, M_{26}, M_{27}, M_{28}	21	1.05
M_4, M_5, M_6, M_{12}, M_{13}, M_{14}, M_{21}, M_{22}	10.5	1.05

3. TIME DELAY CALCULATION

The main aim of this paper is to give a general calculation of time delay in current-mode circuits. There are two phases in the calculation of the time delay: First, an equivalent circuit model has to be developed then analyzing the obtained equivalent circuit model, time delay formulae have to be extracted in terms of circuit elements' parameters.

3.1 Equivalent Circuit Model

As a simple current-mode circuit, a PMOS basic current mirror is selected for time delay investigation. In Figure 3.1(a), a PMOS current-mirror, which is widely used in complex current-mode circuits is shown. Both of the transistors are assumed to operate in saturation region. The large-signal equivalent circuit model of the PMOS transistor M_1 is shown in Figure 3.1(b); it consists of a capacitor in parallel with a non-linear resistor. The capacitor *C* in Figure 3.1(b) represents the total parasitic capacitances of MOS transistors (including the loading capacitors of M_2.) The non-linear resistor stems from the dependent current source of the MOS transistor model working in saturation region. r_o is the output resistance (not shown) which will be taken into account in Figure 3.2.

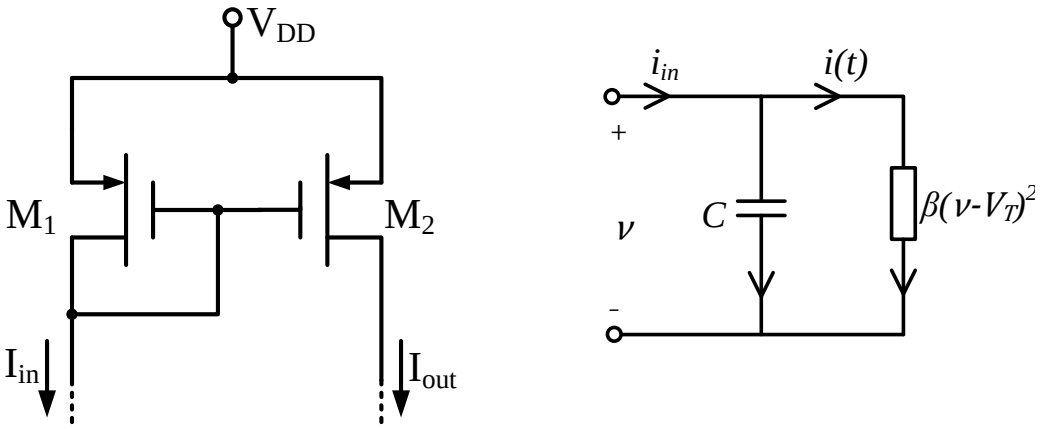


Figure 3.1 : **(a)** PMOS circuit model. **(b)** Large-signal Equivalent circuit model without r_o.

According to Kirchhoff's Current Law the following equation can be written for the circuit of Figure 3.1(b).

$$C\frac{dv(t)}{dt} = -\beta\,(v(t)-V_T)^2 + i_{in}(t) \qquad \textbf{(3.1)}$$

where $\beta = 1/2\mu_p C_{ox} W/L$ is the gain factor of MOS transistors, the parameters μ_p, C_{ox}, W, L have their usual meanings and V_T is the threshold voltage.

To see the effect of the output resistance of the transistors on time delay, similar analyses can be performed. The equivalent circuit model with transistor output resistance r_0 is illustrated in Figure 3.2.

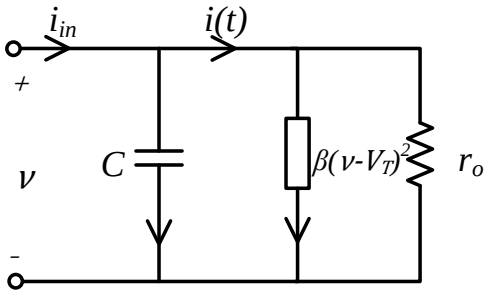


Figure 3.2 : Large-signal equivalent circuit model with r_o [27].

Adding the output resistance and writing the KCL at the input node, the Eq. (3.1) is modified as:

$$C\frac{dv(t)}{dt} = -\beta(v(t)-V_T)^2 + I_{OH} - \frac{v(t)}{r_o} \qquad \textbf{(3.2)}$$

3.2 Junction Capacitances Calculations

As mentioned before, the total parasitic capacitance has the main effect on the value of the time delay. Therefore, a precise calculation of these capacitances is an important issue for current-mode circuits. As an example for calculation of the total parasitic capacitances at the input node of the circuit, the CMOS Core Circuit which was developed as a classifier integrated circuit and manufactured as DU-TCC1209 in 2009 [26], has been used. The CMOS implementation of the classifier core circuit is shown in Figure 3.3.

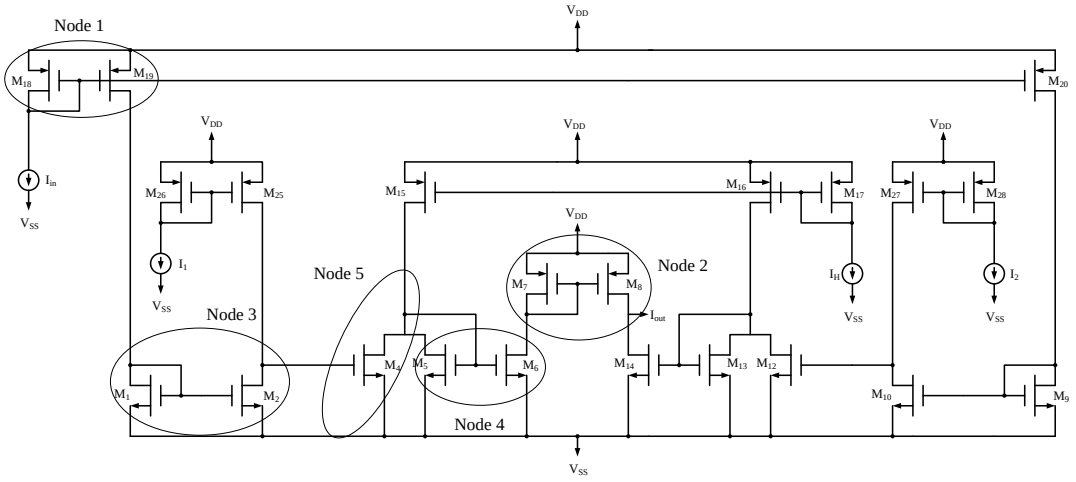


Figure 3.3 : CMOS implementation of the core circuit [26].

3.2.1 Junction capacitances calculations for Node 1

To calculate the total parasitic capacitances, the input section of the classifier core circuit with parasitic capacitances of each transistor is shown in Figure 3.4.

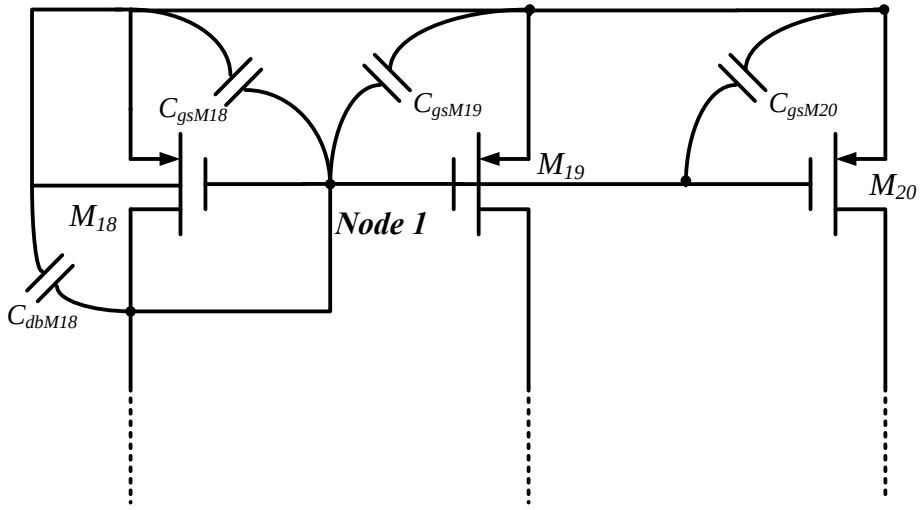


Figure 3.4 : Input section of the core cell with parasitic capacitances [27].

The parasitic capacitances C_{dbM18}, C_{gsM18}, C_{gsM19}, C_{gsM20} affecting Node 1 are all connected in parallel to each other hence the equivalent overall input capacitance is calculated approximately as shown in Eq. (3.3).

$$C_{eq} = C_{db}M_{18} + C_{gs}M_{18} + C_{gs}M_{19} + C_{gs}M_{20} + 7C_{ov} \quad \textbf{(3.3)}$$

The formula of the gate to source capacitance C_{gs} is given by:

$$C_{gs} = \frac{2}{3} \times C_{ox} \times W \times L \quad \textbf{(3.4)}$$

where, C_{ox} is the capacitance per unit area of the gate dielectric, W and L are width and length of the transistor respectively. In addition, C_{ov} in expression (3.3) is the overlap capacitance of each transistor effecting Node 1. The drain-bulk junction capacitance (C_{db}) is found from the following Eq. (3.5):

$$C_{db} = \left(\frac{CJ}{\left(1+\frac{VDB}{PB}\right)^{MJ}} \times AD\right) + \left(\frac{CJSW}{\left(1+\frac{VDB}{PB}\right)^{MJSW}} \times PD\right) \quad \textbf{(3.5)}$$

To find the numeric value of the the drain bulk capacitance of M_{18} transistor (C_{dbM18}) firstly the area of the drain region of MOSFET as called AD is calculated where $xj = 3 \times 10^{-7} m$ called the junction depth as shown in Eq. (3.6) and AD is found 12.915×10^{-12}.

$$AD = 2(W \times xj) + 2(X * xj) \; (xj = 3 \times 10^{-7} m) \quad \textbf{(3.6)}$$

$$AD = \left(2 \times (21 \times 3 \times 10^{-7})\right) + 2 \times \left((1.05/2) \times 3 \times 10^{-7}\right) = 12.915 \times 10^{-12} \quad \textbf{(3.7)}$$

Secondly, PD is calculated as called the perimeter of the drain region of MOSFET from following equalities:

$$PD = 2 \times (W + X), \; X = X + Lov \rightarrow X = L/2 \quad \textbf{(3.8)}$$

$$PD = 2 * \left(21 + (1.05/2)\right) = 43.05 * 10^{-6} \quad \textbf{(3.9)}$$

Current phase is finding the numeric value of drain bulk capacitance by using Eq. (3.4). The numerical values of parasitic capacitances of transistors shown in Figure 3.4 are given as follows for 0.35µm CMOS technology as shown in Table 3.1. These values are taken from the PSpice Model. By using these values C_{dbM18} is calculated 14.115fF.

$$C_{dbM18} = \left(\frac{1.419508 \times 10^{-3}}{\left(1+\frac{0.56}{0.8152753}\right)^{0.5}} \times (12.915 \times 10^{-12})\right) + \left(\frac{4.813504 \times 10^{-10}}{\left(1+\frac{0.56}{0.8152753}\right)^{0.5}} \times (43.05 \times 10^{-12})\right) = 14.115 \times 10^{-15} F \quad \textbf{(3.10)}$$

Table 3.1 : PSpice Model Parameters.

Symbols of source code	Description	Value
TOX	Gate oxide thickness	$7.9*10^{-9}$ (m)
CJ	Source-drain (S/D) bottom junction capacitance per unit area at zero bias	$1.419508*10^{-3}$ (F/m^2)
CJSW	S/D field oxide side wall junction capacitance per unit length at zero bias	$4.813504*10^{-10}$ (F/m)
PB	Bottom junction built in potential	0.8152753 (V)
MJ	S/D bottom junction capacitance grading coefficient	0.5
MJSW	S/D field oxide side wall junction capacitance grading coefficient	0.5
XJ	Junction depth	$3*10^{-7}$m
UO	Surface mobility	$212.2319801*10^{-4}$ (m^2/V.s)
THETA	Mobility Modulation	0.2020774 (1/s)
VTO	Zero-bias threshold voltage	-0.7140674 (V)

To find the gate to source of the capacitance of transistor M_{18}, M_{19} and M_{20} are found from Eq. (3.4). Three of the capacitances values are equal to each other because of the dimensions (W and L) of transistors are equal as following:

$$C_{gsM18} = C_{gsM19} = C_{gsM20} = \left(\frac{2}{3} \times 0.00436899 \times 21 \times 1.05 \times 10^{-12}\right) = 64.2242 \times 10^{-15} F \quad \textbf{(3.11)}$$

The overlap capacitance, which appears due to the fact that source and drain diffusions extend under the gate oxide, is computed as:

$$C_{ov} = W \times L_{ov} \times C_{ox} \quad \textbf{(3.12)}$$

where L_{ov} is overlap length and typically $0.1 \times L$. The value C_{ov} must be added to the C_{gs} and C_{gd} for each transistor. With a routine analysis and applying Miller effect it can be seen that a total number of $7C_{ov}$ appears in expression (3.3).

In the light of this information, overlap capacitance $2*C_{gdovM19} + 2*C_{gdovM20} + C_{gsov18} + C_{gsov19} + C_{gsov20} = 7C_{ov}$ (The factor 2 comes from Miller effect) can be found as:

$$C_{ov} = 21 \times 10^{-6} \times 0.1 \times 1.05 \times 10^{-6} \times 0.00436899 = 9.63362 \times 10^{-15} F \quad \textbf{(3.13)}$$

To sum up $C_{gsM18} = C_{gsM19} = C_{gsM20} = 64.22$ fF, $C_{dbM18} = 14.11$ f F, $C_{ov} = 9.6$ fF. So the equivalent capacitance is calculated in Eq. (3.14) and $C_{eq} = 274.223$ *fF*.

$$C_{eq} = 1.4115 \times 10^{-14} + (3 \times 6.42242 \times 10^{-14}) + (7 \times 9.63362 \times 10^{-15}) = 274.22294 \times 10^{-15} F \quad \textbf{(3.14)}$$

3.3 Time Delay Calculation for the Core Circuit

3.3.1 Delay calculations for Node 1

3.3.1.1 Time delay calculations without r_o

The Input-Output (I-O) waveforms of the current-mirror circuit are shown in Figure 2.6 and the average propagation delay is given in Eq. (2.16).

The next step is to calculate the time delay τ_{PLH} from the equivalent circuit model, which is given in Figure 3.1(b). To do this, the value of the current $i(t)$ at time t_1 must be equated to half of the value of the input current (I_{OH}). To find the time t_1 Eq. (3.1) must be used; that is at t_1 Eq. (3.15) must be satisfied [27].

$$i(t_1) = \frac{I_{OH}}{2} \Leftrightarrow C \frac{dv(t_1)}{dt} = \frac{I_{OH}}{2} \quad \textbf{(3.15)}$$

By substituting Eq. (3.15) into Eq. (3.1), the following set of equations can be reached.

$$C\frac{dv(t_1)}{dt} = -\beta (v(t_1)-V_T)^2 + I_{OH} = \frac{I_{OH}}{2} \quad \textbf{(3.16)}$$

$$\beta(v(t_1) - V_T)^2 = \frac{I_{OH}}{2} \quad \textbf{(3.17)}$$

$$v(t_1) - V_T = \mp\sqrt{\frac{I_{OH}}{2\beta}} \quad \textbf{(3.18)}$$

$$v(t_1) = V_T \mp \sqrt{\frac{I_{OH}}{2\beta}} \tag{3.19}$$

Eq. (3.19) shows the input node voltage at time t_1. Taking $t_0 = 0$ and solving Eq. (3.1) with initial value of $v(0) = V_T$, one can find the following expression for the voltage $v(t)$:

$$v(t) = V_T + \frac{\sqrt{I_{OH}}\tanh[\frac{\sqrt{I_{OH}}\sqrt{\beta}}{C}t]}{\sqrt{\beta}} \tag{3.20}$$

From Eq. (3.20), t can be found as:

$$t = \frac{\operatorname{arctanh}\left[\frac{v(t) - V_T}{\sqrt{I_{OH}/\beta}}\right]}{\frac{\sqrt{I_{OH}}\sqrt{\beta}}{C}} \tag{3.21}$$

Substituting $v(t_1)$ from (3.19) into (3.21) for $v(t)$, the time delay is obtained as:

$$t_1 = 0.8814 \times \frac{C}{\sqrt{I_{OH} \times \beta}} = \tau_{PLH} \tag{3.22}$$

Thus, with Eq. (3.22) a very simple time delay formulation is achieved for the current mirror. In fact, the propagation delay $\tau_{PLH} = t_1$ depends on the value of the total parasitic capacitances (C), the input current initial value I_{OH} and the parameter β. Thus, by minimizing the total value of the parasitic capacitances, the propagation delay can be reduced; another possibility would be to increase the ratio W/L increasing β at the denominator.

For calculating the time delay on Node 1, β must be calculated with using the following set of equations:

$$\mu = \frac{UO}{(1+THETA(VGS-VTO))} \tag{3.23}$$

where *UO* is surface mobility, *THETA* is mobility modulation, *VTO* is zero-bias threshold voltage. Their numerical values are given in Table 3.1 and μ is calculated as:

$$\mu = \frac{212.2319801 * 10^{-4}}{(1+0.2020774 \cdot (0.56-(-0.7140674)))} = 0.0168778 \quad \textbf{(3.24)}$$

C_{ox} is the capacitance per unit area of the gate dielectric is defined as:

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} \ , \ \varepsilon_{ox} = 3.9 \times \varepsilon_o \ \text{,where} \quad \varepsilon_o = 8.85 \times 10^{-12} F/m \quad \textbf{(3.25)}$$

By using Eq. (3.25) C_{ox} is found as $C_{ox} = 0.00436899$.

β is calculated using the values obtained in equation (3.24) and (3.25) as given by following expression and $\beta = 737.389$ ($\mu A/V^2$) is found:

$$\beta = \tfrac{1}{2} \mu Cox W/L \quad \textbf{(3.26)}$$

To sum up, $\beta = 737.389$ ($\mu A/V^2$), I_{OH} = 50μA and V_T = 0.714 V. Using these specified values in Eq. (3.22) the time delay is found to be τ_{PLH} = 1.26 ns as shown in Eq. (3.27).

$$t_1 = 0.8814 * \frac{2.7422294 \times 10^{-13}}{\sqrt{50 * 10^{-6} * 0.000737389}} = 1.26\, ns \quad \textbf{(3.27)}$$

3.3.1.2 Time delay calculations with r_o

The equivalent circuit model with transistor output resistance r_0 is illustrated in Figure 3.2 [28].

Solving the Eq. (3.2) differential equation for the time value t_1 at which $i(t_1) = \frac{I_{OH}}{2}$, results in:

$$t_1 = \frac{(ArcTan[\frac{-v(t_1)2r_o\beta-1+2r_oV_T\beta}{\sqrt{-1+4r_o(-I_{OH}r_o+V_T)\beta}}]-ArcTan[\frac{-1+2r_oV_T\beta-2r_o\beta V_T}{\sqrt{-1+4r_o(-I_{OH}r_o+V_T)\beta}}])2Cr_o}{\sqrt{-1+4r_o(-I_{OH}r_o+V_T)\beta}} \quad \textbf{(3.28)}$$

where;

$$v(t_1) = \frac{-1 + 2r_o V_T \beta \mp \sqrt{1 + 2r_o (I_{OH} r_o - 2V_T)\beta}}{2r_o \beta} \qquad \textbf{(3.29)}$$

Taking into account the output resistance of the MOS transistors (r_o = *100 kΩ*) and using equalities (3.28) and (3.29) the time delay value is found to be τ_{PLH}=*1.4 ns* which shows an increase of 10% in the time delay when r_o is considered.

3.3.2 Delay calculations for Node 3

To calculate the time delay of the second type circuit in the core circuit on Node 3, the total parasitic capacitances of each transistor are shown in Figure 3.5 [28].

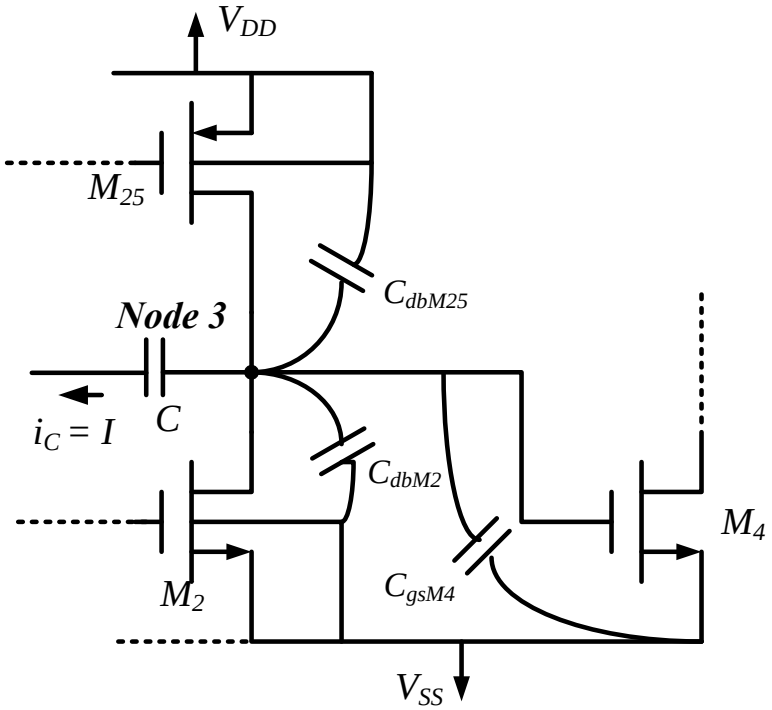


Figure 3.5 : MOS Model with parasitic capacitances for Node 3.

The parasitic capacitances C_{dbM25}, C_{dbM2}, C_{gsM4}, which influence Node 3 are all connected in parallel hence, the equivalent overall input capacitance is calculated approximately as given by expression (3.30).

$$C_{eq} = C_{dbM25} + C_{dbM2} + C_{gsM4} \qquad \textbf{(3.30)}$$

The formula of the gate to source capacitance C_{gs} and the drain-bulk junction capacitance C_{db} is found from the expressions (2.9) and (2.10) respectively.

The numerical values of parasitic capacitances of the transistors shown in Figure 3.5 are given as follows for the CMOS technology ($0.35\mu m$):

C_{gsM4} = 32.11fF, C_{dbM2} = 27.88fF, C_{dbM25} = 14.11fF. So the equivalent capacitance is C_{eq} = 74.1fF. In addition, I_1 = 20μA and V_{DD} = 1.65V, V_{SS} = -1.65V V_T = 0.545V. Using these specified values in equality (3.35) the time delay is found to be τ_{PLH} = 5.1ns.

In order to derive the expression (3.31) for the time delay on Node 3 the value of the current *I*, which is called I_1 in the core circuit, is the negative sum of the drain current of transistors M_{25}, M_2 and is constant:

$$I = i_C = -(i_{DM25} + i_{DM2}) \quad \textbf{(3.31)}$$

The gate voltage of transistor M_4 is shown in equality (3.32), where V_T = 0.545V.

$$V_{G4} = V_{SS} + V_T \quad \textbf{(3.32)}$$

To find the time delay t_2 on Node 3, the following set of equalities can be written:

$$\frac{1}{2}(V_{DD} - V_{G4}) = \frac{1}{C}\int_0^{t_2} I\, dt \quad \textbf{(3.33)}$$

$$\frac{1}{2}(V_{DD} - V_{G4}) = \frac{I \times t_2}{C} \quad \textbf{(3.34)}$$

then using equality (3.34) , the time delay τ_{PLH} is obtained as:

$$t_2 = \frac{C(V_{DD} - (V_{SS} + V_T))}{2I} \quad \textbf{(3.35)}$$

Hence, with expression (3.35) a very simple time delay formulation is obtained for the second type sub-circuit in the Core Circuit. Actually, the propagation delay on Node 3 $\tau_{PLH} = t_2$ depends on the value of the total parasitic capacitances (*C*), the input current value *I*, supply voltages V_{DD}, V_{SS} and gate voltage of M_4 (V_{G4}). Consequently, minimizing the total value of the parasitic capacitances the propagation delay can be decreased, as was the case for Node 1.

3.3.3 Delay calculations for Node 5

In order to calculate the time delay for the third type circuit on Node 5 of the Core Circuit, total parasitic capacitances of each transistor are shown in Figure 3.6 [28].

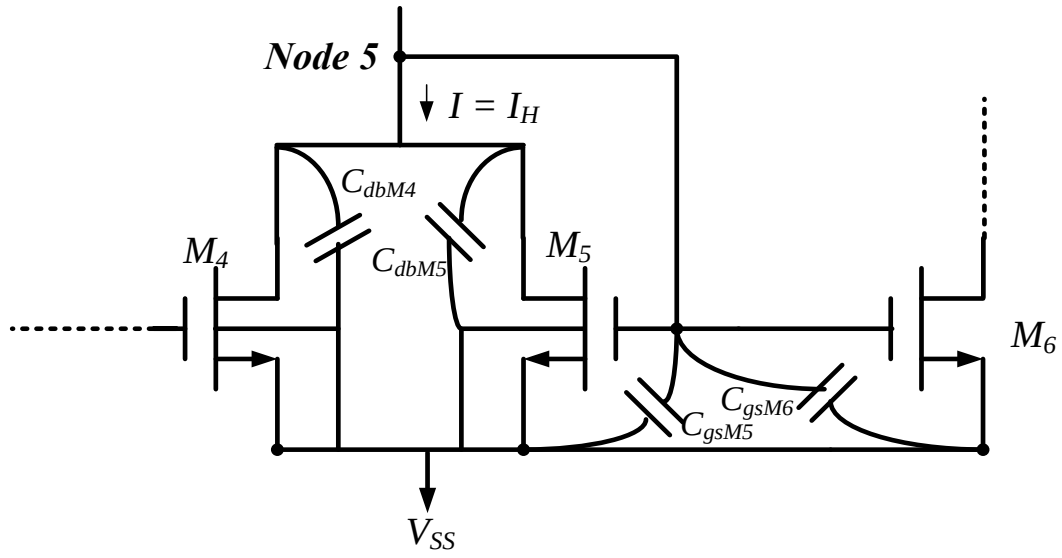


Figure 3.6 : MOS Model with parasitic capacitances for Node 5 [28].

The parasitic capacitances C_{dbM4}, C_{dbM5}, C_{dbM15}, C_{gsM5} and C_{gsM6} affecting Node 5 are also all connected in parallel and the equivalent overall input capacitance is calculated approximately as shown with equality (3.36).

$$C_{eq} = C_{dbM4} + C_{dbM5} + C_{gsM5} + C_{dbM15} + C_{gsM6} \quad \textbf{(3.36)}$$

The parasitic capacitances of the transistors shown in Figure 3.6 for the CMOS technology ($0.35\mu m$) are given as follows:

C_{dbM4} = C_{dbM5} = 7.22fF, C_{dbM15} = 14.11fF, C_{gsM5} = C_{gsM6} = 32.11fF. Hence, the equivalent capacitance is C_{eq} = 92.77fF. In addition, I_H = 50μA and V_{DD} = 1.65V, V_{SS} = -1.65V V_T = 0.545V. Using these specified values in Eq. (3.41) the time delay is found to be τ_{PLH} = 1.9ns.

In order to derive expression (3.41) the time delay on Node 5, the value of the current I being equal to I_H as can be seen from Figure 3.6:

$$I = (i_{DM4} + i_{DM5}) \quad \textbf{(3.37)}$$

is obtained. The drain voltage of transistor M_5 is shown in equality (3.38) with V_T = 0.545V.

$$V_{D5} = V_{SS} + V_T \quad \textbf{(3.38)}$$

To find the time delay t_3 on Node 5, the following set of equations can be written:

$$\frac{1}{2}(V_{D5} - V_{SS}) = \frac{1}{C}\int_0^{t_3} I\, dt \quad \textbf{(3.39)}$$

$$\frac{1}{2}(V_{D5} - V_{SS}) = \frac{I \times t_3}{C} \quad \textbf{(3.40)}$$

Using Eq. (3.40), the time delay $\tau_{PLH} = t_3$ is obtained as:

$$t_3 = \frac{C\mathrm{V_T}}{2I} \quad \textbf{(3.41)}$$

Hence, with equality (3.41) a very simple time delay formulation is obtained for the third type circuit in the core circuit. Actually, the propagation delay on Node 5 $\tau_{PLH} = t_3$ depends on the value of the total parasitic capacitances (C), the input current initial value I and threshold voltage V_T. Consequently, as for Node 1 and Node 2, by minimizing the total value of the parasitic capacitances the propagation delay can be decreased.

The total time delay of the core circuit can now be calculated analytically by adding delays of the stages from the input to the output considering that the subcircuit at nodes 1 and 2 are the same whereas the subcircuit at node 3 is four times wider than the one at node 4 that is, delays for Node 1: t_1, Node 3: t_2, Node 5: t_3, Node 2: t_1, Node 4: $0.25t_2$, as given with expression (3.42):

$$t_{d(total)} = 2t_1 + 1.25t_2 + t_3 = 11.1\text{ns}. \quad \textbf{(3.42)}$$

3.4 SPICE Simulation Results

The core circuit in Figure 3.3 has been simulated with *0.35μm* TSMC CMOS technology parameters using SPICE simulation software. The supply voltages V_{DD} and V_{SS} were selected as $\pm 1.65V$. The transistors' dimensions are given in Table 2.1.

3.4.1 Simulation of subcircuit at Node 1

First, the input section (Node 1) of the core cell has been simulated. Resulting input waveform and output waveform obtained from the drain of transistor M_{19} of the CMOS core circuit are shown in Figure 3.7. The resulting time delay τ_{PLH} is equal to *1.5ns* for an input current of 50μA. From calculations using expressions (3.22) and

(3.28), time delay without r_o effect is *1.26* ns and with r_o, *1.4 ns*, which are very close to the value obtained from the simulation; thus the simulation results verify well the proposed circuit model and the calculations.

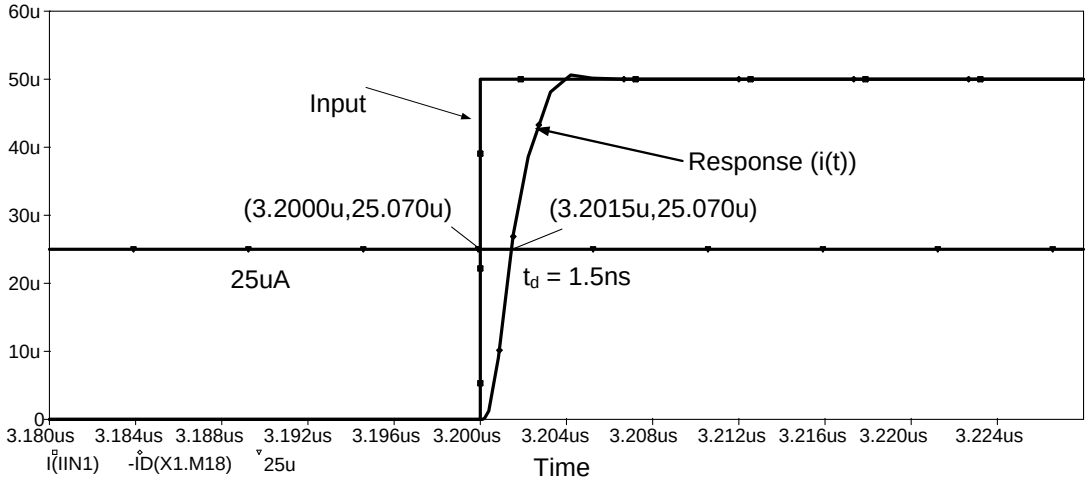


Figure 3.7 : Step response for the input stage of the core circuit of Figure 3.3.

Time delay versus input current graph is shown in Figure 3.8. By taking the input current values as *30μA, 40μA, 50μA, 60μA, 70μA*, the time delays τ_{PLH} are found as *2ns*, *1.7ns, 1.5ns, 1.3ns* and *1.2ns*, respectively. As indicated, the lower the input current of the circuit the higher is the time delay; as expected one way of reducing the time delay is to increase the input current.

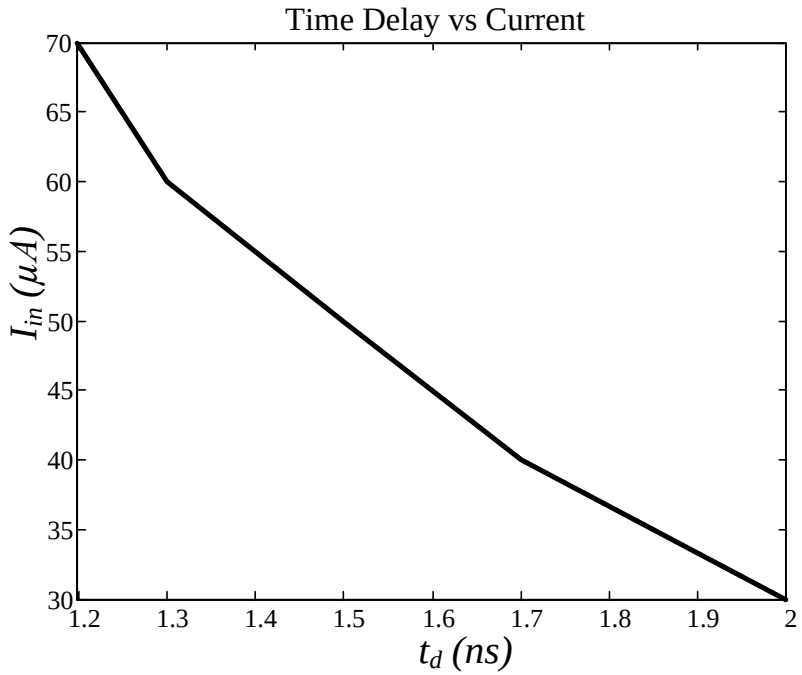


Figure 3.8 : Time delay versus input current graph.

3.4.2 Simulation of subcircuit at Node 3

Next, simulated currents obtained from the drain of transistors $M_{2,}$ $M_{6,}$ $M_{18,}$ $M_{19,}$ M_{25} of the CMOS core circuit are shown in Figure 3.9. Based on this description, by taking I_H = 50μA, I_1 = 20μA and I_2 = 80μA, the simulation can be interpreted as follows: in the first region, when $I_{in} < I_1$, the gate voltage of transistor M_4, V_{G4} is equal to the supply voltage V_{DD} ($V_{G4} \cong V_{DD} = 1.65V$). The transistors' operation regions are: M_{25} in triode region, M_2 is off, M_4 is in triode region. In the second region, when I_{in} is increased M_2 operates in triode and M_{25} is in the saturation region. In case of the third region, when the gate voltage M_4 is equal to sum of V_{SS} and V_T the transistor M_4 is off and M_{25} is on. Under these conditions drain current of M_6 (I_{DM6}) and output current (I_{out}) are equal to I_H. With these values, simulated time delay becomes $\tau_{PLH} = t_2 = 6$ns.

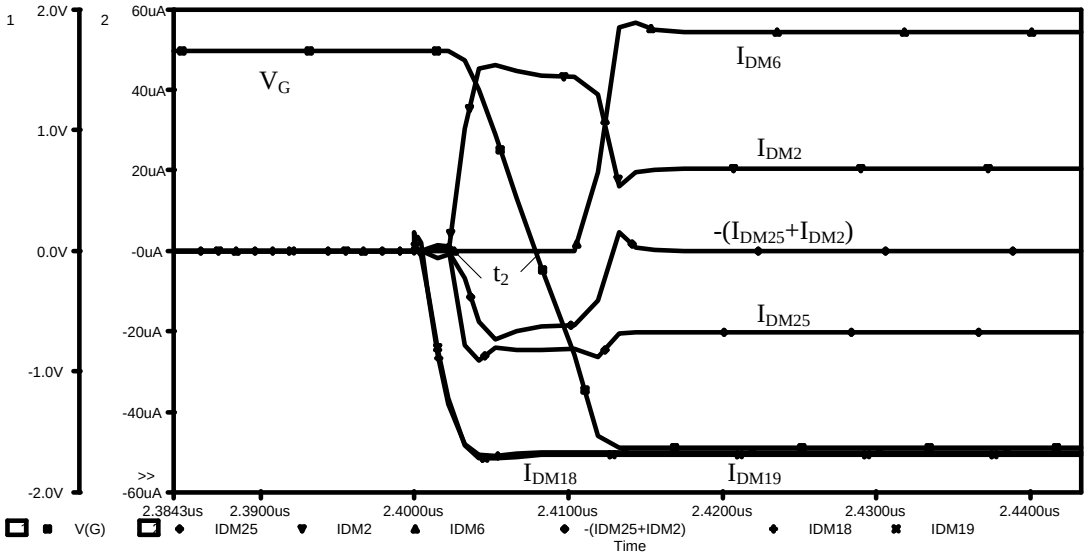


Figure 3.9 : Simulation Result for Node 3.

3.4.3 Simulation of subcircuit at Node 5

The following simulation for Node 5 is shown in Figure 3.10. Simulated currents obtained from the drain of transistors $M_{4,}$ $M_{5,}$ M_{15} of the CMOS core circuit are shown. Based on this condition, by taking I_H = 50μA, I_1 = 20μA and I_2 = 80μA. With these values simulated time delay becomes $\tau_{PLH} = t_3 = 1.9$ns and the total simulated delay is:

$$t_{d(total)} = 2t_1 + 1.25t_2 + t_3 = 12.4\text{ns}. \quad \textbf{(3.43)}$$

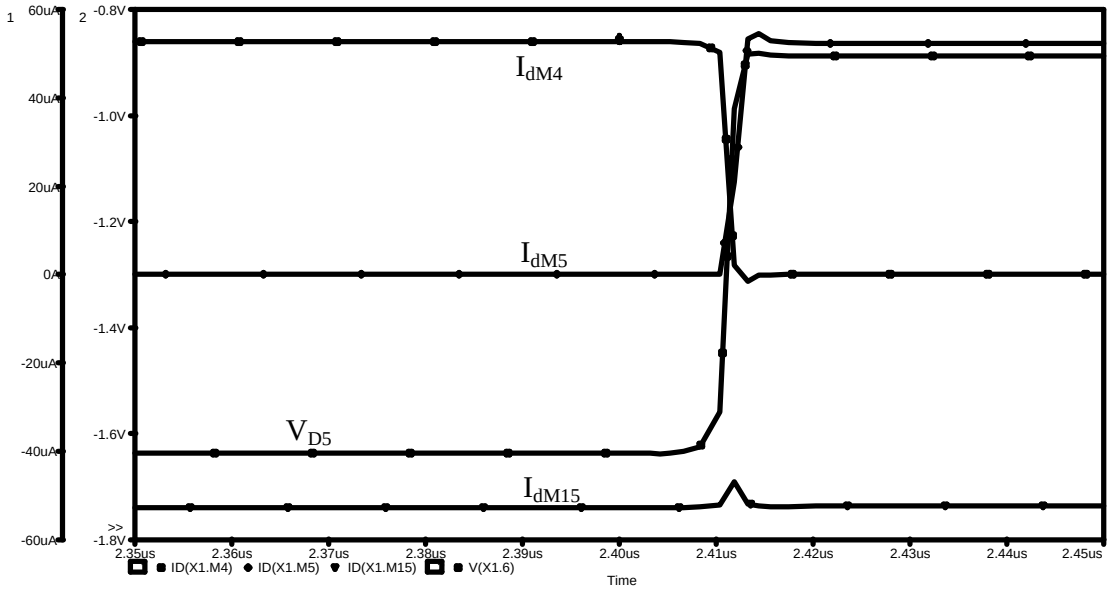


Figure 3.10 : Simulation Result for Node 5.

3.4.4 Simulation of the entire core cell

Simulated input waveform and output waveform of the entire core circuit given in Figure 3.3 is shown in Figure 3.11. By taking I_H = 50µA, I_1 = 20µA, I_2 = 80µA and I_{in} = 50µA the resulting time delay τ_{PLH} is equal to 13.1 ns.

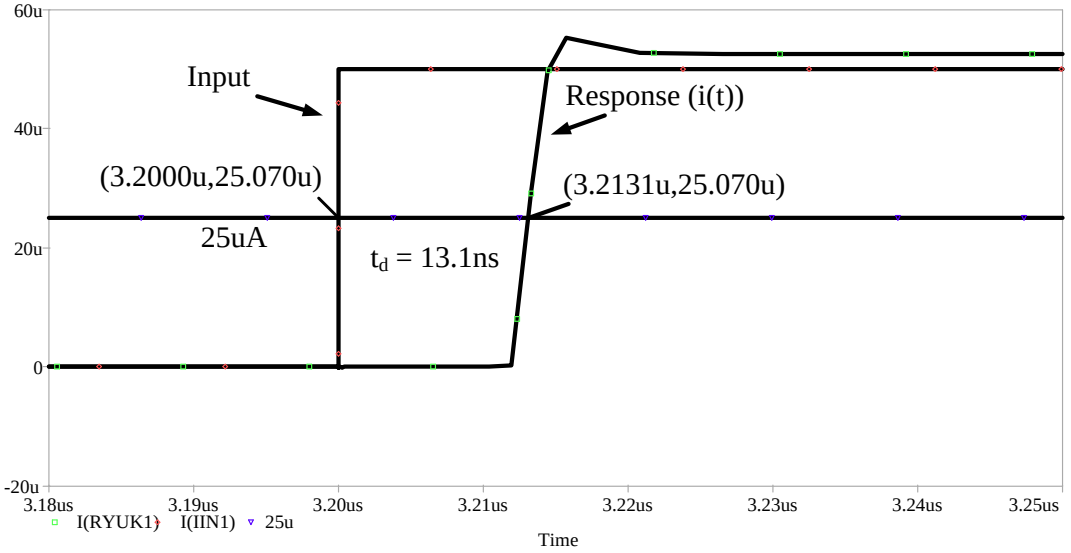


Figure 3.11 : Step response for the core circuit of Figure 3.3.

3.5 Comparison with Bench Test Results

In addition, the circuit in Figure 3.3 has been bench tested using the CMOS Core Circuit in DU-TCC1209 IC. The outcome of the measurements is shown in Figure 3.12. The input waveform and the resulting output waveform for I_H = 50μA, I_1 = 45μA, I_2 = 100μA and I_{in} = 60μA (for I_{in} a voltage of 300mV and a resistor of 5kΩ, for I_H 50mV and 1kΩ were used) show a good agreement with the simulated results, the measured time delay τ_{PLH} being approximately equal to 25 ns (this difference in measured delay can be explained with the existence of stray and probe capacitances).

In addition, the circuit in Figure 3.1(a), using CD 4007 CMOS array transistors with +5 V supply voltage was bench tested experimentally. The output current is taken from the drain of the transistor M_2.

From calculations time delay was found as 11.1ns, from simulations of Node 1, Node 3 and Node 5 as 12.4ns, from the simulation of the entire core circuit as 13.1ns and as 25ns (for I_H = 50μA) from the bench test of the entire core cell. That, calculated, simulated and measured delays agree quite well can be concluded.

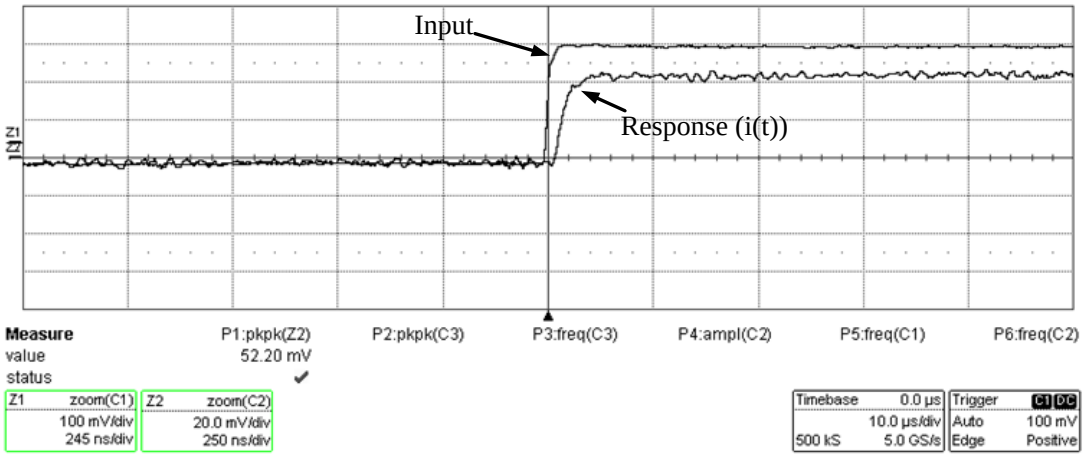


Figure 3.12 : Bench Test Results for Core Circuit.

4. RING OSCILLATORS CONSTRUCTED WITH CORE CIRCUIT

Ring oscillator is cascaded combination of delay stages which are connected in a close loop series. Ring oscillators can be designed with a chain of delay stages have created importance owing to their useful characteristics. If it is wanted to mention a few benefits can be listed as follows: ring oscillators can be designed smoothly with CMOS or BiCMOS integrated circuit technology. At low voltage ring oscillators can succeed its oscillation. Ring oscillators can obtain high frequency oscillation with low power. Ring oscillators can be adjustable electrically. Ring oscillators can be obtained wide tuning range. Through simple structure, ring oscillator can provide multiphase outputs. These features can be combined to achieved multiphase clock signals which are used in communication systems [29].

One way of realizing digital output MOS VCOs is to use a ring oscillator and voltage control can be added. An odd number of open loop inverting amplifiers in a feedback loop is placed for realization of ring oscillator. The easiest type of amplifier as shown in Figure 4.1 which is used simple digital inverter.

Assume that, in the circuit transitions some voltage, from a low voltage to a high voltage state [30]. Every half period, the transition will propagate around the loop with conversion. For instance, the first inverter output's changes to 1. This change will propagate properly in a time *T/2* for all five inverters at which time the output of the first inverter will change to 0. After a while time of *T/2*, the first inverter's output will change back to 1, and so fort. Suppose that t_d is the time delay of each inverter and there are *N* inverters. The half period of oscillation is considered as:

$$\frac{T}{2} = N \cdot t_d \qquad \textbf{(4.1)}$$

So that,

$$f_{osc} = \frac{1}{T} = \frac{1}{2\ N\ t_d} \tag{4.2}$$

To describe, Figure 4.1 exemplify as N = 5. Voltage Controlled Oscillator can be achieved. The ring oscillator shown in Figure 4.1 is a feedback circuit, it should be unstable for represent oscillations.

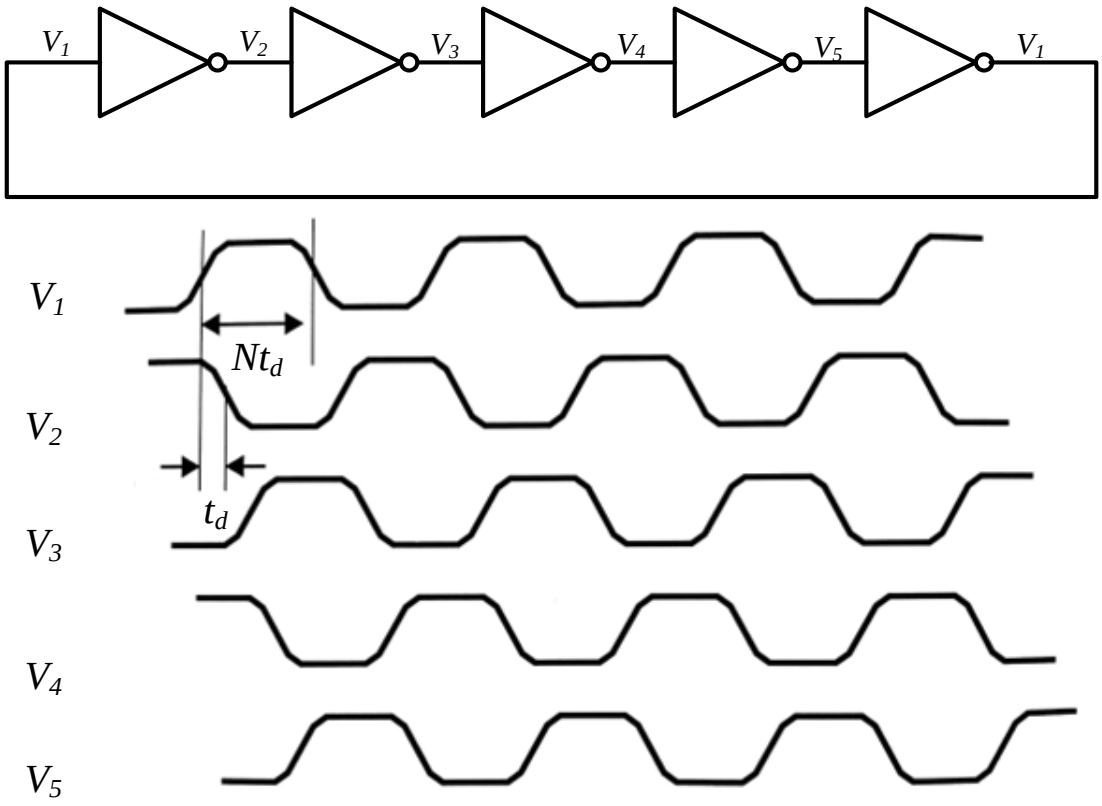


Figure 4.1 : Ring oscillator with N = 5 [30].

To a general ring oscillator with N level, performing first order model of the inverting amplifier is shown in Figure 4.2(a) which is a single inverting amplifier N = 1 with its input connected to its output. In Figure 4.2(b) shows a corresponding small signal model.

Hence, it is required that N must be odd, if single ended inverting amplifiers is used. To acquire better power supply fully differential inverters must be used.

The number of stages used is primarily determined by the power energy loss and the phase noise performance.

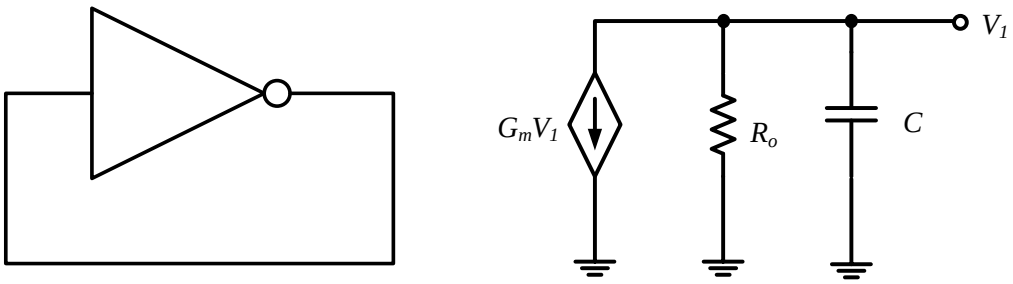


Figure 4.2 : (a) A single inverting amplifier **(b)** Small signal model [30].

There are two main oscillation criteria. First one of this criteria is a phase shift of 180˚. Each level subscribes with 180˚/N degrees of phase shift. The other oscillation criteria is a loop gain greater than 1 at ω_{osc}.

In this study comparison of Voltage Controlled Oscillator (VCO) versus Current Controlled Oscillator (CCO) should be explained:

VCO is a kind of electronic oscillator. VCO's oscillation frequency is controlled by a voltage input [31]. It can be said that for communication circuits VCO is important component.

If we want to sort out the advantages of these circuits [13]: tuning range is described in the way of maximum or minimum frequency ratio. Owing to the inner noise, phase jitter is in dealing with the impression on its frequency. Low jitter is preferred than high jitter. Tuning linearity can be defined as how linearity its frequency with respect to V.

4.1 Topologies of the Ring Oscillators:

There are two main caption for the ring oscillators:

4.1.1 Differential topology

The differential topology consist a load and an NMOS differential pair. In each node and the current through the load is set the delay in the cell. For PMOS devices, the load can originate of a resistor and this provide the oscillator tunable with a voltage. Accordingly, a short differential oscillator, such as the 3 stage ring oscillator as shown in Figure 4.4, is modeled using its equivalent small signal single ended counterpart in Figure 4.3.

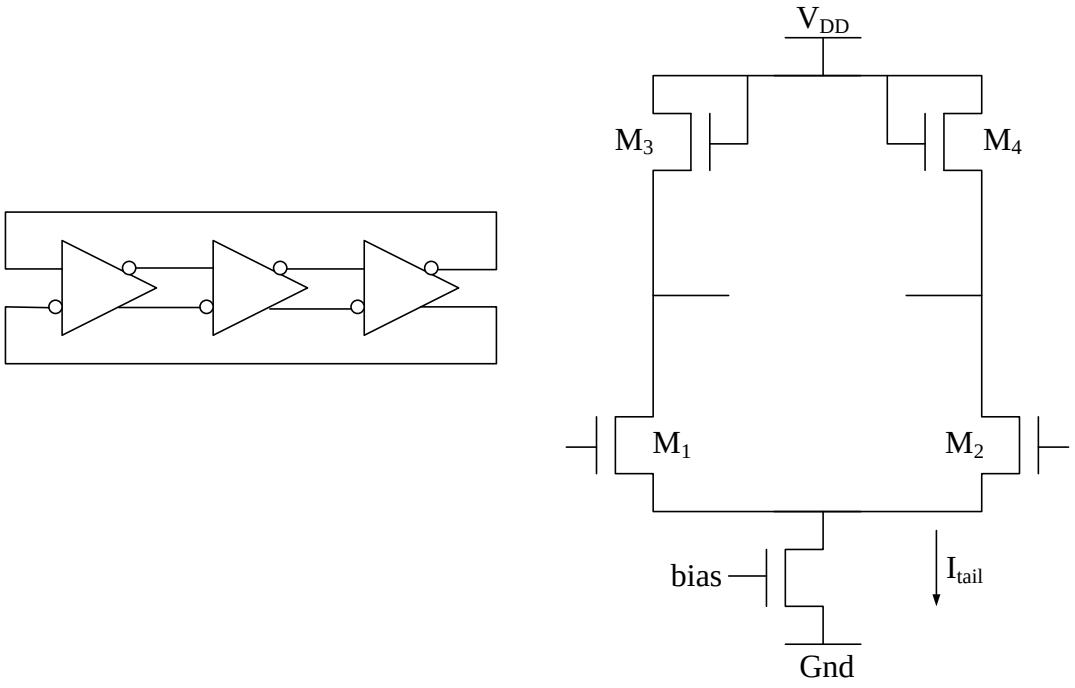


Figure 4.3 : Three stage differential ring oscillator [32].

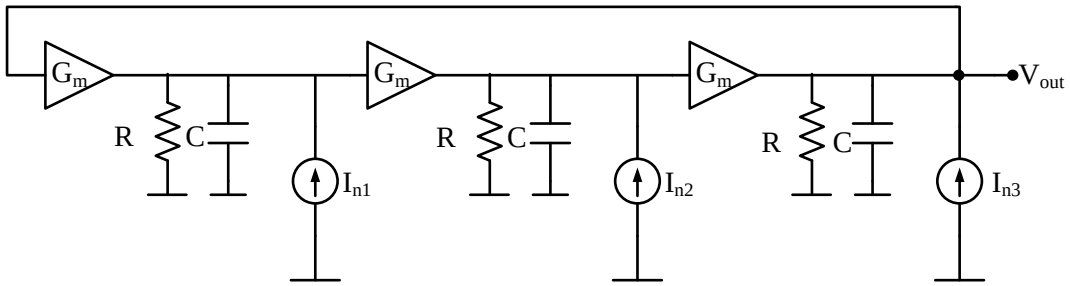


Figure 4.4 : The small signal single-ended equivalent for the ring of 4.3.

4.1.2 Single ended topology

The simplest ring oscillator designs use a single ended architecture which was already shown in Figure 4.1. The main single ended topology constitute of CMOS inverters. As from the CMOS inverter is a high small signal gain stage, the gain need is always achieved. The single ended topology has to be performed with an odd number of cells to acquire oscillation. This is because of a large signal phase shift of 180˚ of each delay cell has.

4.2 Proposed Ring Oscillator Constructed with Core Circuit

In this section, firstly a ring oscillator is proposed which is constructed using two CMOS core circuit designed and developed as a classifier integrated circuit and manufactured as DU-TCC1209 in 2009 as shown in Figure 4.5. Time delay of two block ring oscillator and phase shift is shown in Figure 4.6. The frequency of oscillation is found as:

$$f_{osc} = \frac{1}{2 \cdot N \cdot t_d} \qquad \textbf{(4.4)}$$

Here, N = 2 and t_d is the time delay of a single core circuit.

By cascading many of the core circuit time delay can be occurred. Taking advantage of the delay, ring oscillator is realized. On the way N is the number of core circuit, the oscillation frequency is adjustable with changing the control currents I_1, I_2 and I_H as shown in Eq. (4.4).

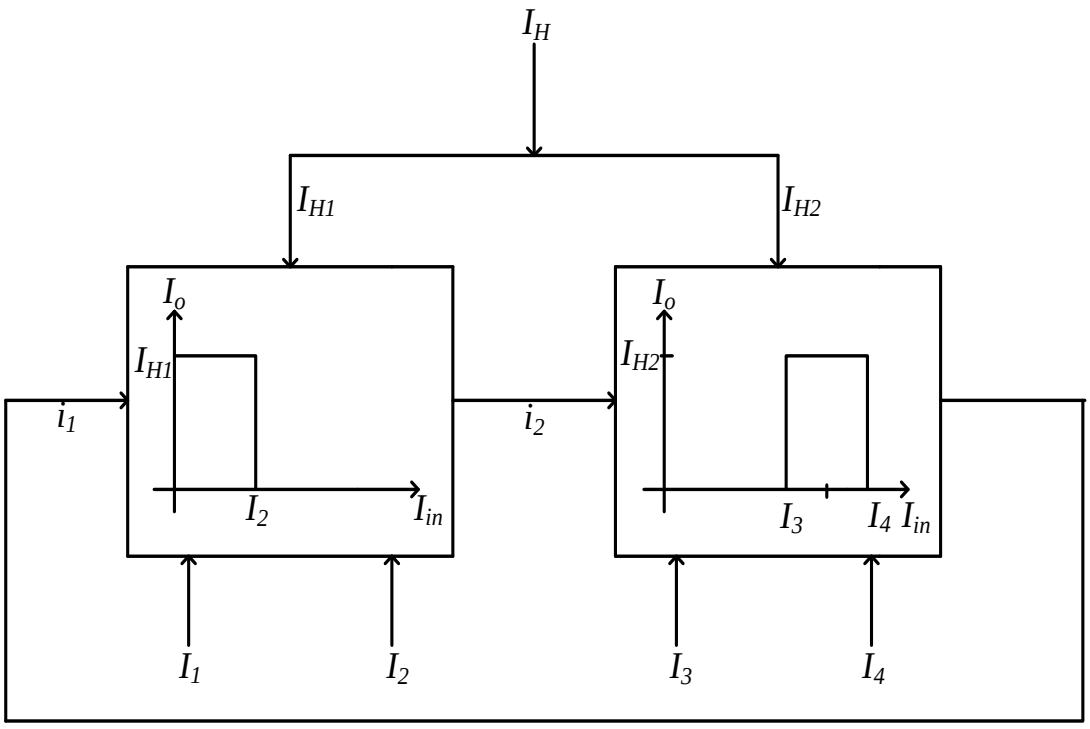


Figure 4.5 : Proposed Two Block Ring Oscillator.

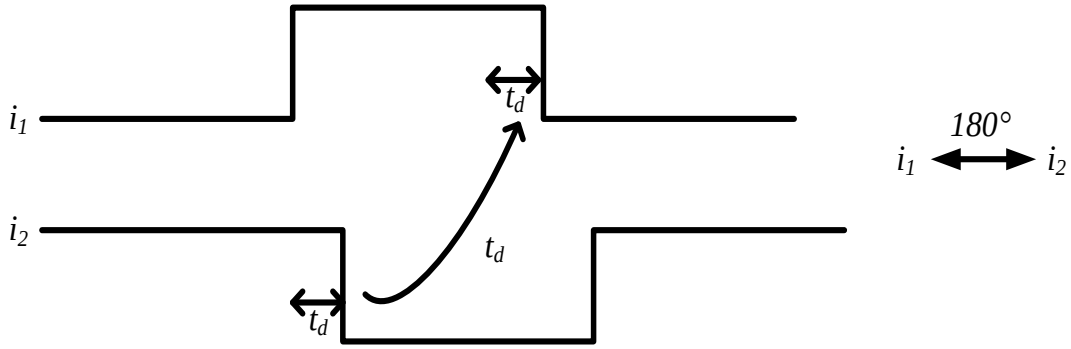


Figure 4.6 : Time Delay of Two Block Ring Oscillator.

Time delay of the core circuit was calculated by using Eq. (3.42) and $t_{d(total)} =$ 11.1ns. The next step is to calculate the delay of two block ring oscillator by using the following expression.

$$t_{d(RO)} = N \cdot t_{d(total)} \quad \textbf{(4.5)}$$

where N is the number of block. Time delay of the proposed ring oscillator is calculated as: $t_{d(RO)} = 22.2ns$.

Oscillation frequency of two block ring oscillator is calculated with using Eq. (4.4) as found $f_{osc} = 22.5\ MHz$.

To obtain the lower frequency of oscillation more core circuits can be cascaded in a ring. A ring oscillator which is constructed using four CMOS core circuit is proposed as shown in Figure 4.7. Time delay of four block ring oscillator and phase shift is shown in Figure 4.8.

Time delay of the proposed ring oscillator is calculated given expression in (4.5) where N = 4. By using theoretical results, time delay of four block ring oscillator is found as $t_{d(RO)} = 44.4ns$.

Frequency of oscillation in four block ring oscillator is calculated from Eq. (4.4) where N = 4 as found $f_{osc} = 11.2\ MHz$.

As is seen, increasing the number of blocks, the oscillation frequency is reduce. According to the frequency range of applications, the number of blocks can be increased or decreased.

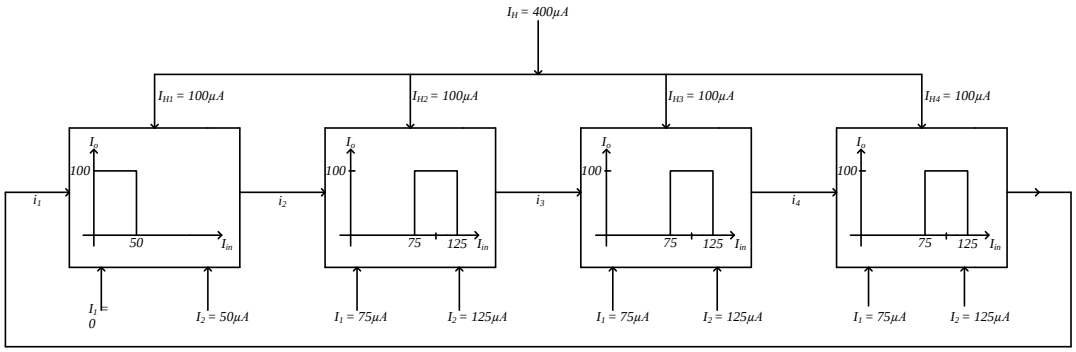


Figure 4.7 : Proposed Four Block Ring Oscillator.

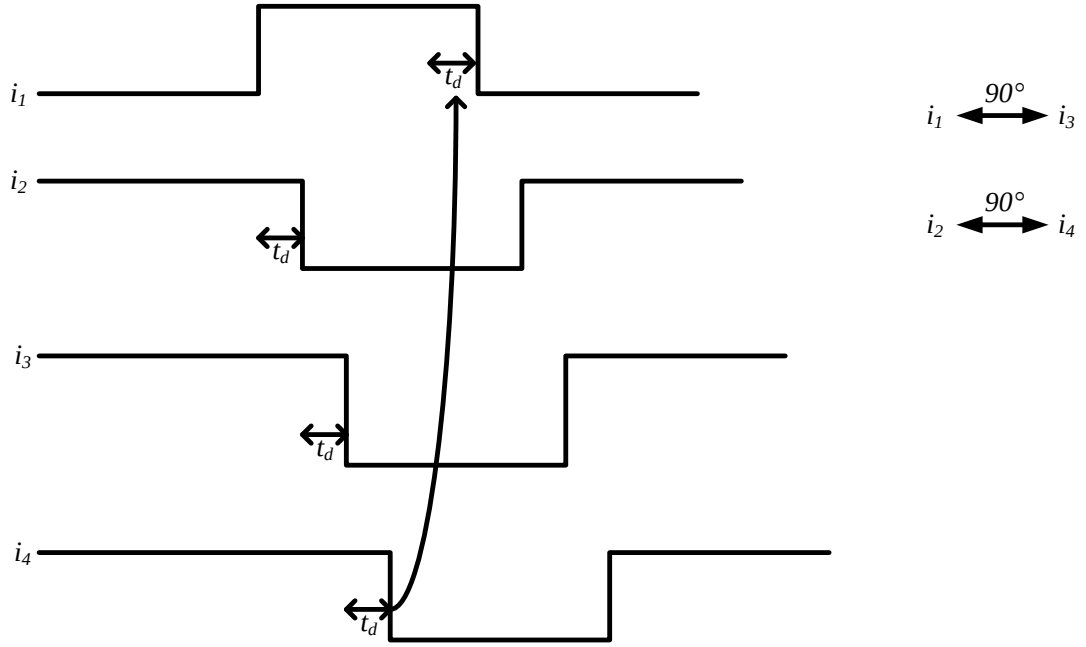


Figure 4.8 : Time Delay of Four Block Ring Oscillator.

4.3 SPICE Simulation Results

The simulation output of the two block ring oscillator in Figure 4.5 is shown in Figure 4.9. With different control current, how the output signal frequency is changed is given in Table 4.1. In classical ring oscillator circuits the frequency is changed by increasing or decreasing the number of stages used in design. In consequence of the constructed the integrated circuit, it is almost impossible to change the oscillation frequency. However, in the proposed ring oscillator shown in Figure 4.5, oscillation frequency can be tuned with using the control current. Through the control current I_1 and I_2 can be brought to the desired level of frequency, the amplitude of output signal can be adjustable with I_H.

Table 4.1 : Change of Two Block Ring Oscillator frequency with respect to control current.

Test	Control Current	Frequency
1st Test	I_1=0μA, I_2=50μA, I_{H1}=100μA I_3=75μA, I_4=125μA, I_{H2}=100μA	f_{osc}=53 *MHz*
2nd Test	I_1=0μA, I_2=100μA, I_{H1}=200μA I_3=150μA, I_4=250μA, I_{H2}=200μA	f_{osc}=87 *MHz*
3rd Test	I_1=0μA, I_2=150μA, I_{H1}=300μA I_3=250μA, I_4=350μA, I_{H2}=300μA	f_{osc}=100 *MHz*

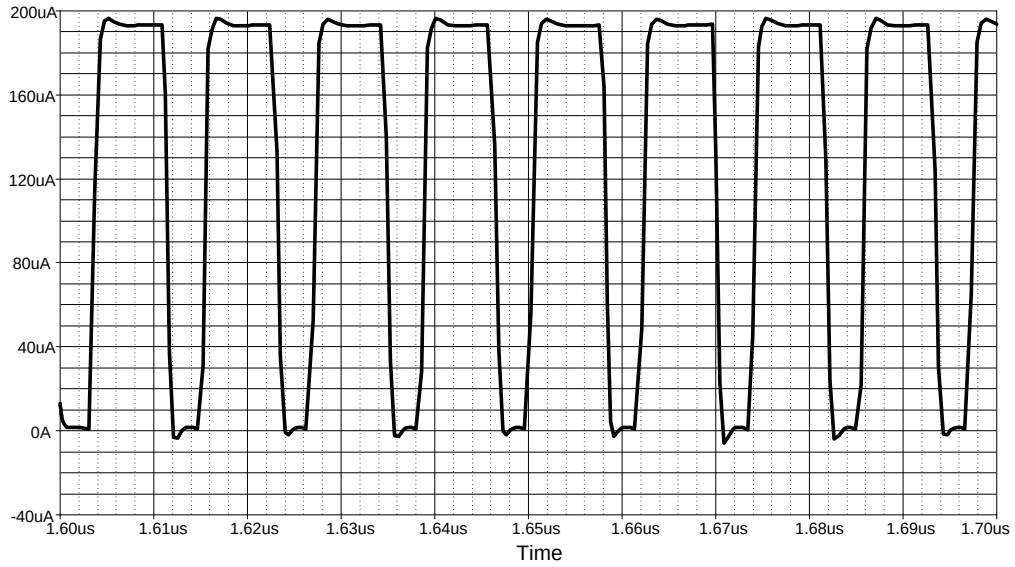


Figure 4.9 : Simulation Result of Two Block Ring Oscillator.

4.4 Comparison with Bench Test Results

In addition, the circuit in Figure 4.5 has been bench tested using the CMOS core circuit in DU-TCC1209 IC. The outcome of the measurements is shown in Figure 4.11. The input waveform and the resulting output waveform for the first block*;* I_{H1} = 100µA, I_1 = 0µA, I_2 = 50µA, for the second block*;* I_{H2} = 100µA, I_3 = 75µA, I_4 = 125µA (1kΩ were used) as shown in Figure 4.10 show quite a good agreement with the simulated results, the measured time delay τ_{PLH} being approximately equal to 60 ns (this difference in measured delay can be explained with the existence of stray and probe capacitances). The output resistance used in ring oscillator is 1kΩ.

To sum up for the proposed two block of ring oscillator; from calculations time delay was found as 22.2ns, and as 60ns (for I_H = 100µA) from the bench test of the entire core cell. Oscillation frequeny is found as roughly 16.6 MHz. That, calculated, simulated and measured delays agree quite well can be concluded. The difference in measured delay can be explained with the existence of stray and probe capacitances.

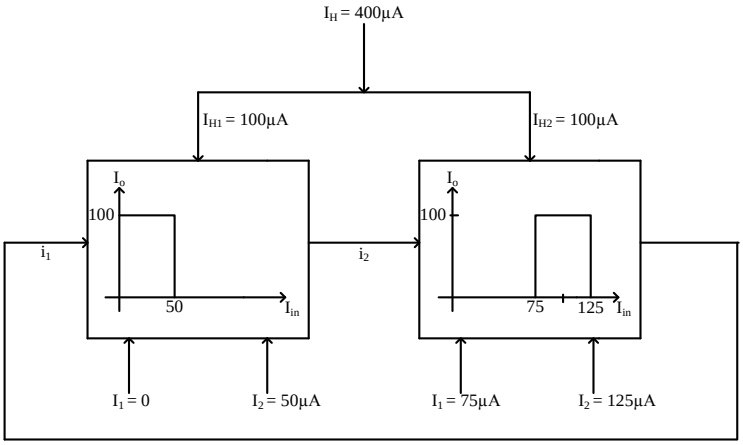


Figure 4.10 : Bench Tested Ring Oscillator.

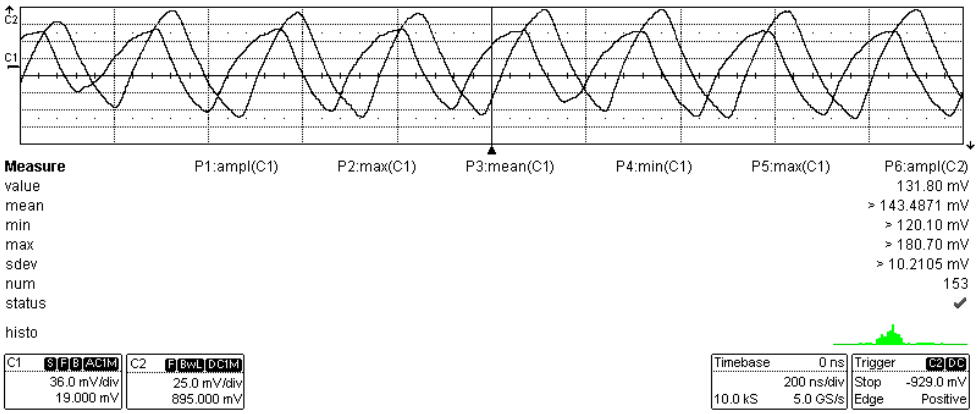


Figure 4.11 : Bench Test Results for Two Block Ring Oscillator.

With using two block of ring oscillator for different values of control current Table 4.3 is given. By means of this table I_{VDD} and power variation can be seen. If I_{IN} and I_{OUT} is decreased power is also decreased.

According to the needs, ring oscillator can be designed required number of blocks.

Table 4.3 : Measurement Results for Two Block Ring Oscillator.

I_1 [μA]	I_2 [μA]	I_H [μA]	I_{IN} [μA]	I_{OUT} [μA]	I_{VDD} [mA]	P [mW]
100	150	150	125	125	7.89	26
100	150	150	50	50	7.49	24.7
50	75	75	70	70	7.14	23.43
50	75	75	40	40	6.88	22.7

5. CONCLUSIONS AND RECOMMENDATIONS

In this thesis, the calculation of time delay in current-mode circuits has been investigated and analytical expressions are derived for calculating the time delay of MOS current mirrors. There were three types of circuit which was calculated the time delay. Accuracy of the expressions has been confirmed with SPICE simulations on the CMOS Core Circuit in DU-TCC1209 IC [26] as well as bench test results for the core circuit built with DU-TCC1209 IC.

Ring oscillator circuit was proposed with using two or four core circuit. Time delay calculations were obtained. In a similar vein, accuracy of the statement has been justified with SPICE simulations and bench test results also constructed.

One of the main uses of time delay calculations is concerned with the operation speed of the circuit under consideration. Building comparator, pulse width modulators, level crossing detectors using the Core Circuit in DU-TCC1209 IC has been presented as an application in [34]. As a future work under consideration, the delay calculations introduced here will constitute a basis for the computation of the operation frequency of such applications.

REFERENCES

[1] **Xu, Z., Xu, W., Yu,, Y., and Wu, Q.** (2008). "A Study on the Stability of Current-Mode Control Using Time-Delay Model of Pulse-Width-Modulator.

[2] **Toumazou, C., Lidgey, F.J., Haigh, D.G.** (1990). "Analogue IC Design: the Current-Mode Approach", IEE Circuits and Systems Series 2, London, United Kingdom.

[3] **Ferri, G., Guerrini, N.C.** (2003). "Low-Voltage Low-Power CMOS Current Conveyors", Kluwer Academic Publishers, Boston, London.

[4] **Burns, J.R.** (1964). "Switching Response of Complementary-Symmetry MOS Transistor Logic Circuits," RCA Rev., vol. 25, pp. 627-661, Dec. 1964.

[5] **Sakurai, T., and Newton, A.R.** (1990) "Alpha-Power Law MOSFET Model and its Applications to CMOS Inverter Delay and Other Formulas".

[6] **Sakurai, T., and Newton, A.R.** (1991). Delay Analysis of Series-Connected MOSFET Circuits.

[7] **Weigandt, T.C., Kim, B., and Gray, P.R.:** Analysis of Timing Jitter in CMOS Ring Oscillators.

[8] **Montero, M. C., and Sanchez, A.D.** (2004). A Current-Mode Delay-Line With Continuous-Time Offset Compensation., 1 st lntemational Conference on Electrical and Electronics Engineering.

[9] **Nagai, T., Onizawa, N., and Hanyu, T.** (2008). High-Speed Timing Verification Scheme Using Delay Tables for a Large-Scaled Multiple-Valued Current-Mode Circuit. DOI 10.1109/ISMVL.12

[10] **Zito, F., Aquilino, F., Fragomeni, L., Merenda, M., and Della, Corte F.G.** (2009). CMOS Wireless Temperature Sensor with Integrated Radiating Element.

[11] **Narin, D. G.** (1993). "Analytic Step Response of MOS Current Mirrors", IEEE Tr. on Circuits and Systems-I: Fundamental Theory and Applications, vol. 40, no. 2, pp. 133-135.

[12] **Url-1** <http://en.wikipedia.org/wiki/Ring_oscillator >, accessed at 20.04.2012.

[13] **Nugroho, P., Leelarasmee, E., Fujii, N.** (2006). "Tuning Analysis of a CMOS Current Controlled Ring Oscillator", The 21st International Technical Conference on Circuits/Systems, Computers and Communications, ISBN 974-94418-9-3 ©2006 ECTI.

[14] **Chen, Z. Z., Lee T.C.** (2011). "The Design and Analysis of Dual-Delay-Path Ring Oscillators", IEEE Transactions on Circuits and Systems-I : Regular Papers, vol. 58, no. 3.

[15] **Zhang, C., Lin, M.C. and Syrzycki, M.** (2011): Process Variation Compensated Voltage Controlled Ring Oscillator with Subtruction-Based Voltage Controlled Current Source. IEEE CCECE 2011.

[16] **Koli, K,.** (2000). CMOS Current Amplifiers: Speed versus Nonlinearity. Otamedia Oy.

[17] **Smith, K., Sedra, A.** (1968). "The current-conveyor-a new circuit building block," IEEE Proc., vol. 56, pp. 1368-69.

[18] **Sedra, A., Smith, K.** (1970). "A second-generation current-conveyor and its applications," IEEE Trans., vol. CT-17, pp. 132-134.

[19] **Hughes, J., Bird, N., Macbeth, I.**, (1989). "Switched currents - a new technique for analog sampled-data signal processing," in Proc. IEEE Int. Symposium on Circuits and Systems (ISCAS'89), Portland, USA, pp. 1584-1587.

[20] **Comlinear Corporation**, (1985). A new approach to op-amp design, Application Note 300-1.

[21] **Daubert, S., Vallancourt, D., Tsividis, Y.** (1988) "Current copier cells," Electronics Letters, vol. 24, pp. 1560-1561.

[22] **Schmid, H.** (2002). "Why the terms 'Current Mode' and 'Voltage Mode' neither divide nor qualify circuits", 0-7803-7448-7/02/$17.00 ©2002 IEEE.

[23] **Hodges, D.A., Jackson, H.G., and Saleh, R.A,** (2004). Analysis and Design of Digital Integrated Circuits. McGraw Hill.

[24] **Sedra, A.S., Smith, K.C.**, (2004). "Microelectronic Circuits", Fifth Edition, Oxford University Press, New York.

[25] **Richard, J.P.** (2003). Time-delay systems:an overview of some recent advances and open problems. Pergamon.

[26] **Yıldız, M., Minaei, S., and Goknar, I.C.** A flexible current-mode classifier circuit and its applications. International Journal of Circuit Theory and Applications. doi.10.1002/cta.677.

[27] **Kurnaz, M., Minaei, S., Goknar, I.C.** (2013). "Time Delay Calculation in Current-Mode Circuits" 8th International Conference on Electrical and Electronics Engineering (ELECO 2013), 28-30 Nov. 2013, Bursa, Turkey, pp.349-352.

[28] **Kurnaz, M. , Minaei, S., Goknar, I.C.** "Equivalent Circuit Models in Current-Mode Circuits for Time Delay Calculations", Analog Integrated Circuits and Signal Processing, accepted for publication for Springer.

[29] **Mandal, M.K., Sarkar, B.C.** (2010). "Ring Oscillators: Characteristics and applications", Indian Journal of Pure&Applied Physics, vol. 48, February 2010, pp.136-145.

[30] **Carusone, T. C., Johns, D., Martin, K.** "Analog Integrated Circuit Design", International Student Version, 2nd Edition, Wiley.

[31] **Url-1** <http://en.wikipedia.org/wiki/Voltage-controlled_oscillator>, accessed at 15.02.2013.

[32] **Lee, T.H.** (1999). The Design of Low Noise Oscillators. Kluwer Academic.

[33] **Iu, H. H. C., and Robert, B.** (2003). Control of Chaos in a PWM Current-Mode H-Bridge Inverter Using Time-Delayed Feedback. IEEE Transaction on Circuits and Systems—I: Fundamental Theory and Applications. VOL. 50, NO. 8.

[34] **Göknar, I.C., Minaei, S., Yildiz, M. and Akçakaya, E.** (2013). "Pulse Width Modulation Using a Recently Developed CMOS Core Circuit," Proceedings, 21st European Conference on Circuit Theory and Design (ECCTD 2013), Paper No. 109, Dresden, Germany.

[35] **Sung-Mo K., and Leblebici, Y.** (1996). CMOS Digital Integrated Circuits, Analysis and Design. McGraw-Hill.

[36] **Cheng, Y., and Hu, C.** (2003). MOSFET Modeling & BSIM 3 User's Guide. Kluwer Academic.

[37] **Liu, W.** (2001). MOSFET Models for SPICE Simulation including BSIM3v3 and BSIM4. Wiley.

[38] **Wan, K., and Ferdowski, M.** (2008). Reducing Computational Time Delay in Digital Current-Mode Controllers for Dc-Dc Converters.

[39] **Aboushady, H., de Lira Mendes, E., Dessouky, M. and Loumeau, P.** (1999). A Current-Mode Continuous-Time ΣΔ Modulator with Delayed Return-To-Zero Feedback**.**

[40] **Prodic, A., and Maksimovic, D.** (2000). Digital PWM Controller and Current Estimator for A Low-Power Switching Converter.

[41] **Cicekoglu, O., and Toker, A.** (1999). Current mode oscillator with linear period control over a wide range. International Journal of Electronics. 86: 12, 1453 — 1462.

[42] **Marsden, K., Lee, H.-J., Ha, D. S., and Lee, H.-S.** (2003). Low Power CMOS Re-programmable Pulse Generator for UWB Systems. International Conferance on Ultra Wideband Systems and Technologies. pp. 443-447.

[43] **Richard, J. P.** (2003). Time-delay systems:an overview of some recent advances and open problems.

[44] **Camacho, O., Rojas, R., and Garcia-Gabin, W.** (2007). Some long time delay sliding mode control approaches. doi:10.1016/j.isatra.2006.06.002.

[45] **Wu, L., and Zheng, W. X.** (2009). Passivity-based sliding mode control of uncertain singular time-delay systems, doi:10.1016/j.automatica.05.014.

[46] **Lin, G.R., and Lai, Y.** (2002). A novel phase-noise-suppressed and delay-time-tunable mode-locked erbium-doped fiber laser. Optics Communications 212 169–175.

[47] **Liu, T., Gao, F., and Wang, Y.** (2010). IMC-based iterative learning control for batch processes with uncertain time delay. Journal of Process Control 20 173–180.

[48] **Ali, M. H., Wu, B., Tamura, J., and Dougal, R.A.** (2010). Minimization of shaft oscillations by fuzzy controlled SMES considering time delay. Electric Power Systems Research 80 770–777.

[49] **Abdulhalim, I., and Moores, G.** (2004). Remote temperature and thermal expansion sensing using the time delay mode of position sensors. Sensors and Actuators A 111 245–251.

[50] **Finnstam, P., Söderlund, M.,** (2005). Design of CMOS ring oscillator, Master Thesis, Chalmers University of Technology, Göteborg.

[51] **Bruun, E.** (1995). "Bandwidth optimization of a low power, high speed CMOS current op amp," Int. J. Analog Integrated Circuit Design and Signal Processing, vol. 7, pp. 11-19.

[52] **Zele, R., Lee, S., Allstot, D.** (1992). "A high gain current-mode operational amplifier," in Proc. IEEE Int. Symposium on Circuits and Systems (ISCAS'92), San Diego, USA, IEEE, pp. 2852-2855.

[53] **Myshkis, A., Kolmanovskii, V.B.** (1992). "Applied theory of functional differential equations", Kluwer Academy, Dordrecht.

[54] **Mohammadi, A., Abrishamifar, A., Ayatollahi, A.** (2009). "A Novel CMOS All-Pass Tunable Phase Shifter", School of Electrical Engineering, Iran University of Science and Technology, Tehran, Iran, 2009.

[55] **Mourabit, A. E., Lu,G.N., Pittet, P., Birjali, Y., Lahjomri. F., Zhang, M.** (2012) "A new method to enhance frequency operation of CMOS ring oscillators", International Journal of Electronics, Vol. 99, No. 3, March 2012, 351–360.

[56] **Leblebici, D., Leblebici, Y.** "Fundamentals of High Frequency CMOS Analog Integrated Circuits"

[57] **Eken, Y. A.**(2003). "High Frequency Voltage Controlled Ring Oscillators in Standard CMOS", School of Electrical and Computer Engineerin Georgia Institute of Technology.

APPENDICES

APPENDIX A: PSPICE Model Parameter 0.35µm TSMC with LEVEL 3.

APPENDIX B: PSPICE Model Parameter 0.35µm AMC with LEVEL .7

APPENDIX C: Provide the mathematical expression of time delay.

APPENDIX A

PSPICE Model Parameter 0.35µm TSMC with LEVEL 3

*****0.35 TSMC MOSIS*****

.MODEL nmos NMOS (LEVEL = 3

+TOX=7.9E-9 NSUB=1E17 GAMMA=0.5827871

+PHI= 0.7 VTO=0.5445549 DELTA=0

+UO=436.256147 ETA=0 THETA = 0.1749684

+KP=2.055786E-4 VMAX=8.309444E4 KAPPA = 0.2574081

+RSH=0.0559398 NFS=1E12 TPG=1

+XJ=3E-7 LD=3.162278E-11 WD=7.046724E-8

+CGDO=2.82E-10 CGSO=2.82E-10 CGBO=1E-10

+CJ=1E-3 PB=0.9758533 MJ=0.3448504

+CJSW=3.777852E-10 MJSW=0.3508721)

.MODEL pmos PMOS (LEVEL= 3

+TOX=7.9E-9 NSUB=1E17 GAMMA=0.4083894

+PHI=0.7 VTO=-0.7140674 DELTA=0

+UO=212.2319801 ETA=9.999762E-4 THETA=0.2020774

+KP=6.733755E-5 VMAX=1.181551E5 KAPPA=1.5

+RSH=30.0712458 NFS=1E12 TPG=-1

+XJ=2E-7 LD=5.000001E-13 WD=1.249872E-7

+CGDO=3.09E-10 CGSO=3.09E-10 CGBO=1E-10

+CJ=1.419508E-3 PB=0.8152753 MJ=0.5

+CJSW=4.813504E-10 MJSW=0.5)

APPENDIX B

PSPICE Model Parameter 0.35µm AMC with LEVEL 7

```
.MODEL nmos NMOS LEVEL=7
* ----------------------------------------------------------------------
********** SIMULATION PARAMETERS **********
* ----------------------------------------------------------------------
* format    : PSPICE
* model     : MOS BSIM3v3
* process   : CS[ADFI]
* revision  : N/C;
* extracted : CSA C61417; 1998-10; ese(487)
* doc#      : 9933016 REV_N/C
* ----------------------------------------------------------------------
*                    TYPICAL MEAN CONDITION
* ----------------------------------------------------------------------
*       *** Flags ***
+MOBMOD =1.000e+00 CAPMOD =2.000e+00
+NLEV   =0
*       *** Threshold voltage related model parameters ***
+K1     =6.044e-01
+K2     =2.945e-03 K3     =-1.72e+00 K3B    =6.325e-01
+NCH    =2.310e+17 VTH0   =4.655e-01
+VOFF   =-5.72e-02 DVT0   =2.227e+01 DVT1   =1.051e+00
+DVT2   =3.393e-03 KETA   =-6.21e-04
+PSCBE1 =2.756e+08 PSCBE2 =9.645e-06
+DVT0W  =0.000e+00 DVT1W  =0.000e+00 DVT2W  =0.000e+00
*       *** Mobility related model parameters ***
+UA     =1.000e-12 UB     =1.723e-18 UC     =5.756e-11
+U0     =4.035e+02
*       *** Subthreshold related parameters ***
+DSUB   =5.000e-01 ETA0   =3.085e-02 ETAB   =-3.95e-02
+NFACTOR=1.119e-01
*      *** Saturation related parameters ***
+EM     =4.100e+07 PCLM   =6.831e-01
+PDIBLC1=1.076e-01 PDIBLC2=1.453e-03 DROUT  =5.000e-01
+A0     =2.208e+00 A1     =0.000e+00 A2     =1.000e+00
+PVAG   =0.000e+00 VSAT   =1.178e+05 AGS    =2.490e-01
+B0     =-1.76e-08 B1     =0.000e+00 DELTA  =1.000e-02
+PDIBLCB=2.583e-01
*       *** Geometry modulation related parameters ***
+W0     =1.184e-07 DLC    =8.285e-09
+DWC    =2.676e-08 DWB    =0.000e+00 DWG    =0.000e+00
+LL     =0.000e+00 LW     =0.000e+00 LWL    =0.000e+00
+LLN    =1.000e+00 LWN    =1.000e+00 WL     =0.000e+00
+WW     =0.000e+00 WWL    =0.000e+00 WLN    =1.000e+00
+WWN    =1.000e+00
*       *** Temperature effect parameters ***
+AT     =3.300e+04 UTE    =-1.80e+00
+KT1    =-3.30e-01 KT2    =2.200e-02 KT1L   =0.000e+00
+UA1    =0.000e+00 UB1    =0.000e+00 UC1    =0.000e+00
```

```
+PRT    =0.000e+00
*       *** Overlap capacitance related and dynamic model parameters   ***
+CGDO   =2.100e-10 CGSO   =2.100e-10 CGBO   =1.100e-10
+CGDL   =0.000e+00 CGSL   =0.000e+00 CKAPPA =6.000e-01
+CF     =0.000e+00 ELM    =5.000e+00
+XPART  =1.000e+00 CLC    =1.000e-15 CLE    =6.000e-01
*       *** Parasitic resistance and capacitance related model parameters ***
+RDSW   =6.043e+02
+CDSC   =0.000e+00 CDSCB  =0.000e+00 CDSCD  =8.448e-05
+PRWB   =0.000e+00 PRWG   =0.000e+00 CIT    =1.000e-03
*       *** Process and parameters extraction related model parameters ***
+TOX    =7.700e-09 NGATE  =0.000e+00
+NLX    =1.918e-07
*       *** Substrate current related model parameters ***
+ALPHA0 =0.000e+00 BETA0  =3.000e+01
*       *** Noise effect related model parameters ***
+AF     =1.400e+00 KF     =2.810e-27 EF     =1.000e+00
+NOIA   =1.000e+20 NOIB   =5.000e+04 NOIC   =-1.40e-12
*       *** Common extrinsic model parameters ***
+LINT   =-1.67e-08 WINT   =2.676e-08 XJ     =3.000e-07
+RSH    =8.200e+01 JS     =2.000e-05
+CJ     =9.300e-04 CJSW   =2.800e-10
+MJ     =3.100e-01 MJSW   =1.900e-01
+PB     =6.900e-01 TT     =0.000e+00
+PBSW   =9.400e-01

* ---------------------------------------------------------------------
.MODEL pmos PMOS LEVEL=7
* ---------------------------------------------------------------------
********** SIMULATION PARAMETERS **********
* ---------------------------------------------------------------------
* format    : PSPICE
* model     : MOS BSIM3v3
* process   : CS[ADFI]
* revision  : N/C;
* extracted : CSA C61417; 1998-10; ese(487)
* doc#      : 9933016 REV_N/C
* ---------------------------------------------------------------------
*                    TYPICAL MEAN CONDITION
* ---------------------------------------------------------------------
*       *** Flags ***
+MOBMOD =1.000e+00 CAPMOD =2.000e+00
+NLEV   =0
*       *** Threshold voltage related model parameters ***
+K1     =5.675e-01
+K2     =-4.39e-02 K3     =4.540e+00 K3B    =-8.52e-01
+NCH    =1.032e+17 VTH0   =-6.17e-01
+VOFF   =-1.13e-01 DVT0   =1.482e+00 DVT1   =3.884e-01
+DVT2   =-1.15e-02 KETA   =-2.56e-02
+PSCBE1 =1.000e+09 PSCBE2 =1.000e-08
+DVT0W  =0.000e+00 DVT1W  =0.000e+00 DVT2W  =0.000e+00
*       *** Mobility related model parameters ***
+UA     =2.120e-10 UB     =8.290e-19 UC     =-5.28e-11
+U0     =1.296e+02
*       *** Subthreshold related parameters ***
```

```
+DSUB   =5.000e-01 ETA0   =2.293e-01 ETAB   =-3.92e-03
+NFACTOR=8.237e-01
*       *** Saturation related parameters ***
+EM     =4.100e+07 PCLM   =2.979e+00
+PDIBLC1=3.310e-02 PDIBLC2=1.000e-09 DROUT  =5.000e-01
+A0     =1.423e+00 A1     =0.000e+00 A2     =1.000e+00
+PVAG   =0.000e+00 VSAT   =2.000e+05 AGS    =3.482e-01
+B0     =2.719e-07 B1     =0.000e+00 DELTA  =1.000e-02
+PDIBLCB=-1.78e-02
*       *** Geometry modulation related parameters ***
+W0     =4.894e-08 DLC    =-5.64e-08
+DWC    =3.845e-08 DWB    =0.000e+00 DWG    =0.000e+00
+LL     =0.000e+00 LW     =0.000e+00 LWL    =0.000e+00
+LLN    =1.000e+00 LWN    =1.000e+00 WL     =0.000e+00
+WW     =0.000e+00 WWL    =0.000e+00 WLN    =1.000e+00
+WWN    =1.000e+00
*       *** Temperature effect parameters ***
+AT     =3.300e+04 UTE    =-1.35e+00
+KT1    =-5.70e-01 KT2    =2.200e-02 KT1L   =0.000e+00
+UA1    =0.000e+00 UB1    =0.000e+00 UC1    =0.000e+00
+PRT    =0.000e+00
*       *** Overlap capacitance related and dynamic model parameters   ***
+CGDO   =2.100e-10 CGSO   =2.100e-10 CGBO   =1.100e-10
+CGDL   =0.000e+00 CGSL   =0.000e+00 CKAPPA =6.000e-01
+CF     =0.000e+00 ELM    =5.000e+00
+XPART  =1.000e+00 CLC    =1.000e-15 CLE    =6.000e-01
*       *** Parasitic resistance and capacitance related model parameters ***
+RDSW   =1.853e+03
+CDSC   =6.994e-04 CDSCB  =2.943e-04 CDSCD  =1.970e-04
+PRWB   =0.000e+00 PRWG   =0.000e+00 CIT    =1.173e-04
*       *** Process and parameters extraction related model parameters ***
+TOX    =7.700e-09 NGATE  =0.000e+00
+NLX    =1.770e-07
*       *** Substrate current related model parameters ***
+ALPHA0 =0.000e+00 BETA0  =3.000e+01
*       *** Noise effect related model parameters ***
+AF     =1.290e+00 KF     =1.090e-27 EF     =1.000e+00
+NOIA   =1.000e+20 NOIB   =5.000e+04 NOIC   =-1.40e-12
*       *** Common extrinsic model parameters ***
+LINT   =-8.14e-08 WINT   =3.845e-08 XJ     =3.000e-07
+RSH    =1.560e+02 JS     =2.000e-05
+CJ     =1.420e-03 CJSW   =3.800e-10
+MJ     =5.500e-01 MJSW   =3.900e-01
+PB     =1.020e+00 TT     =0.000e+00
+PBSW   =9.400e-01
* ----------------------------------------------------------------------
```

APPENDIX C

Provide the mathematical expression of time delay:

$$\frac{dv}{dt} = -\frac{\beta}{C}(v - V_T)^2 + \frac{I_o}{C} \quad \textbf{(C 1.1)}$$

$$\frac{dv}{dt} = -\frac{\beta}{C}\left[(v - V_T)^2 - \frac{I_o}{\beta}\right] \quad \textbf{(C 1.2)}$$

$$= -\frac{\beta}{C}\left[\left(v - V_T - \sqrt{\frac{I_o}{\beta}}\right)\left(v - V_T + \sqrt{\frac{I_o}{\beta}}\right)\right] \quad \textbf{(C 1.3)}$$

$$\frac{dv}{\left(v - V_T - \sqrt{\frac{I_o}{\beta}}\right)\left(v - V_T + \sqrt{\frac{I_o}{\beta}}\right)} = -\frac{\beta}{C} \cdot dt \quad \textbf{(C 1.4)}$$

Let's allocate the expression of denominator into simple fraction:

$$\frac{1}{\left(v - V_T - \sqrt{\frac{I_o}{\beta}}\right)\left(v - V_T + \sqrt{\frac{I_o}{\beta}}\right)} = \frac{v_1}{v - V_T - \sqrt{\frac{I_o}{\beta}}} + \frac{v_2}{v - V_T - \sqrt{\frac{I_o}{\beta}}} \quad \textbf{(C 1.5)}$$

$$v_1 = \frac{1}{\left(v - V_T + \sqrt{\frac{I_o}{\beta}}\right)} \Big|_{v = V_T + \sqrt{\frac{I_o}{\beta}}} = \frac{1}{2}\sqrt{\frac{\beta}{I_o}} \quad \textbf{(C 1.6)}$$

$$v_2 = \frac{1}{\left(v - V_T - \sqrt{\frac{I_o}{\beta}}\right)} \Big|_{v = V_T - \sqrt{\frac{I_o}{\beta}}} = -\frac{1}{2\sqrt{\frac{I_o}{\beta}}} = -\frac{1}{2}\sqrt{\frac{\beta}{I_o}} \quad \textbf{(C 1.7)}$$

In this case, the equation **(C 1.4)**, is as follows:

$$\frac{1}{2}\sqrt{\frac{\beta}{I_o}} \cdot \frac{dv}{v - V_T - \sqrt{\frac{I_o}{\beta}}} - \frac{1}{2}\sqrt{\frac{\beta}{I_o}} \cdot \frac{dv}{v - V_T + \sqrt{\frac{I_o}{\beta}}} = -\frac{\beta}{C}dt \quad \textbf{(C 1.8)}$$

$$\frac{dv}{v - V_T - \sqrt{\frac{I_o}{\beta}}} - \frac{dv}{v - V_T + \sqrt{\frac{I_o}{\beta}}} = -2\sqrt{\frac{I_o}{\beta}} \cdot \frac{\beta}{C} dt \qquad \textbf{(C 1.9)}$$

$$\ln\left(v - V_T - \sqrt{\frac{I_o}{\beta}}\right) - \ln\left(v - V_T + \sqrt{\frac{I_o}{\beta}}\right) + \ln S = -2\frac{\sqrt{\beta \cdot I_o}}{C} t \qquad \textbf{(C 1.10)}$$

$$\ln\left(\left[\frac{v - V_T - \sqrt{\frac{I_o}{\beta}}}{v - V_T + \sqrt{\frac{I_o}{\beta}}}\right] S\right) = -2\frac{\sqrt{\beta \cdot I_o}}{C} t \qquad \textbf{(C 1.11)}$$

$$\frac{v - V_T - \sqrt{\frac{I_o}{\beta}}}{v - V_T + \sqrt{\frac{I_o}{\beta}}} S = e^{-2\frac{\sqrt{\beta \cdot I_o}}{C} t} \qquad \textbf{(C 1.12)}$$

Starting Condition is shown as following equalities:

$$v(t_1) = \sqrt{\frac{1}{2} \cdot \frac{I_o}{\beta}} + V_T \qquad \textbf{(C 1.13)}$$

$$\frac{\sqrt{\frac{1}{2} \cdot \frac{I_o}{\beta}} - \sqrt{\frac{I_o}{\beta}}}{\sqrt{\frac{1}{2} \cdot \frac{I_o}{\beta}} + \sqrt{\frac{I_o}{\beta}}} S = e^{-2\frac{\sqrt{\beta \cdot I_o}}{C} t_1} \qquad \textbf{(C 1.14)}$$

$$\frac{\sqrt{\frac{1}{2}} - 1}{\sqrt{\frac{1}{2}} + 1} S = e^{-2\frac{\sqrt{\beta \cdot I_o}}{C} t_1} \qquad \textbf{(C 1.15)}$$

$$S = \frac{1 + \sqrt{2}}{1 - \sqrt{2}} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C} t_1} \qquad \textbf{(C 1.16)}$$

Satisfying the solution of the starting condition:

$$\frac{v - V_T - \sqrt{\frac{I_o}{\beta}}}{v - V_T + \sqrt{\frac{I_o}{\beta}}} S = \frac{1-\sqrt{2}}{1+\sqrt{2}} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)} \quad \textbf{(C 1.17)}$$

$$v - V_T - \sqrt{\frac{I_o}{\beta}} = \frac{1-\sqrt{2}}{1+\sqrt{2}} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)} \cdot \left(v - V_T + \sqrt{\frac{I_o}{\beta}} \right) \quad \textbf{(C 1.18)}$$

$$v \left[1 - \frac{1-\sqrt{2}}{1+\sqrt{2}} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)} \right]$$

$$= \left[1 - \frac{1-\sqrt{2}}{1+\sqrt{2}} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)} \right] \cdot V_T + \left[1 + \frac{1-\sqrt{2}}{1+\sqrt{2}} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)} \right] \quad \textbf{(C.19)}$$

$$\cdot \sqrt{\frac{I_o}{\beta}}$$

$$v \left[1 - \frac{\left(1-\sqrt{2}\right)^2}{-1} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)} \right]$$

$$= \left[1 - \frac{\left(1-\sqrt{2}\right)^2}{-1} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)} \right] \cdot V_T \quad \textbf{(C.20)}$$

$$+ \left[1 + \frac{\left(1-\sqrt{2}\right)^2}{-1} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)} \right] \cdot \sqrt{\frac{I_o}{\beta}}$$

$$v = V_T + \frac{1 - \frac{3-2\sqrt{2}}{1} \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)}}{1 + \left(3-2\sqrt{2}\right) \cdot e^{-2\sqrt{\beta \cdot I_o}(t-t_0)}} \cdot \sqrt{\frac{I_o}{\beta}} \quad \textbf{(C.21)}$$

$$v = V_T + \frac{1 - \left(3-2\sqrt{2}\right) \cdot e^{-2\frac{\sqrt{\beta \cdot I_o}}{C}(t-t_1)}}{1 + \left(3-2\sqrt{2}\right) \cdot e^{-2\sqrt{\beta \cdot I_o}(t-t_1)}} \cdot \sqrt{\frac{I_o}{\beta}} \quad \textbf{(C.22)}$$

Proof of the calculation:

$$v(t_1) = V_T + \frac{1 - (3-2\sqrt{2})}{1 + (3-2\sqrt{2})} \cdot \sqrt{\frac{I_o}{\beta}} \quad \textbf{(C.23)}$$

$$= V_T + \frac{-2 + 2\sqrt{2}}{4 - 2\sqrt{2}} \cdot \sqrt{\frac{I_o}{\beta}} \quad \textbf{(C.24)}$$

$$= V_T + \frac{-2\left(1 - \sqrt{2}\right) + 2\sqrt{2}}{2\left(2 - \sqrt{2}\right)} \cdot \sqrt{\frac{I_o}{\beta}} \quad \textbf{(C.25)}$$

$$= V_T - \frac{\left(1 - \sqrt{2}\right)\left(2 + \sqrt{2}\right)}{4 - 2} \cdot \sqrt{\frac{I_o}{\beta}} \quad \textbf{(C.26)}$$

$$= V_T - \frac{2 - 2 - \sqrt{2}}{2} \cdot \sqrt{\frac{I_o}{\beta}} \quad \textbf{(C.27)}$$

$$= V_T + \frac{1}{\sqrt{2}} \cdot \sqrt{\frac{I_o}{\beta}} \quad \textbf{(C 128)}$$

We have seen that statement **(C 1.28)** which we found by using Wolfram Mathematica Programme is implemented.

$$\frac{dv}{dt} = \sqrt{\frac{I_o}{\beta}} \cdot \frac{a\left(3 - 2\sqrt{2}\right) \cdot e^{-a(t-t_1)}\left[1 + \left(3 - 2\sqrt{2}\right) \cdot e^{-a(t-t_1)}\right] + a\left(3 - 2\sqrt{2}\right) \cdot e^{-a(t-t_1)}\left[1 - \left(3 - 2\sqrt{2}\right) \cdot e^{-a(t-t_1)}\right]}{\left(1 + \left(3 - 2\sqrt{2}\right) \cdot e^{-a(t-t_1)}\right)^2} \quad \textbf{(C 1.29)}$$

$$\frac{dv}{dt} = \frac{a\left(3 - 2\sqrt{2}\right) \cdot e^{-a(t-t_1)}[2]}{\left(1 + \left(3 - 2\sqrt{2}\right) \cdot e^{-a(t-t_1)}\right)^2} \qquad \text{Formula as } +2\frac{\beta I_o}{C} \quad \textbf{(C 1.30)}$$

$$\frac{dv}{dt} = \frac{4\frac{\sqrt{\beta I_o}}{C} \cdot \left(3 - 2\sqrt{2}\right) e^{-2\frac{\sqrt{\beta I_o}}{C} \cdot (t-t_1)}}{\left[1 + \left(3 - 2\sqrt{2}\right) \cdot e^{-2\frac{\sqrt{\beta I_o}}{C} \cdot (t-t_1)}\right]^2} \cdot \sqrt{\frac{I_o}{\beta}} = \frac{4 \cdot I_o}{C} \quad \textbf{(C 1.31)}$$

$$(v - V_T)^2 = \frac{I_o}{\beta} \cdot \frac{\left[1 - \left(3 - 2\sqrt{2}\right) \cdot e^{-2\frac{\sqrt{\beta I_o}}{C} \cdot (t-t_1)}\right]^2}{\left[1 + \left(3 - 2\sqrt{2}\right) \cdot e^{-2\frac{\sqrt{\beta I_o}}{C} \cdot (t-t_1)}\right]^2} \quad \textbf{(C 1.32)}$$

$$-\frac{\beta}{C} \cdot (v - V_T)^2 + \frac{I_o}{C} = -\frac{I_o}{C} \cdot \frac{\left(1 - \left(3 - 2\sqrt{2}\right) \cdot e^{-a \cdot (t-t_1)}\right)^2}{\left(1 + \left(3 - 2\sqrt{2}\right) \cdot e^{-a \cdot (t-t_1)}\right)^2} + \frac{I_o}{C} \quad \textbf{(C 1.33)}$$

$$-\frac{\beta}{C}\cdot(v-V_T)^2+\frac{I_o}{C}=$$

$$=\frac{I_o}{C}\cdot\left[\frac{\left(1+\left(3-2\sqrt{2}\right)\cdot e^{-a\cdot(t-t_1)}\right)^2-\left(1-\left(3-2\sqrt{2}\right)\cdot e^{-a\cdot(t-t_1)}\right)^2}{\left(1+\left(3-2\sqrt{2}\right)\cdot e^{-a\cdot(t-t_1)}\right)^2}\right] \quad \textbf{(C 1.34)}$$

$$=\frac{I_o}{C}\cdot\frac{2\cdot\left[2\cdot\left(3-2\sqrt{2}\right)\cdot e^{-a\cdot(t-t_1)}\right]}{\left(1+\left(3-2\sqrt{2}\right)\cdot e^{-a\cdot(t-t_1)}\right)^2}=\frac{4I_o}{C} \quad \textbf{(C 1.35)}$$

CURRICULUM VITAE

Name Surname:	Melek KURNAZ
Place and Date of Birth:	Samsun – 25.02.1984
Address:	Aşık Veysel Mah. Buğday Sok. Atapark 1 Apt. No: 32 Daire: 22 Ataşehir-ISTANBUL
E-mail:	melekkurnaz@gmail.com
B.Sc.:	Doğuş Üniversitesi – Computer Engineering Doğuş Üniversitesi – Electronics and Communication Engineering

Professional Experience and Rewards:

Melek Kurnaz received her B.S. degree in Computer Engineering with double major program Electronics and Communication Engineering from Dogus University in 2008. She joined ERASMUS program in 2006 in FH-Wedel University. She is already student M.Sc. of Istanbul Technical University, Istanbul, Turkey. She is currently assistant in Electronics and Communications Engineering Department of Dogus University. Her research interest includes current-mode circuits and analog signal processing.

PUBLICATIONS / PRESENTATIONS ON THE THESIS

- **M. Kurnaz, S. Minaei, I.C. Goknar,** "Equivalent Circuit Models in Current-Mode Circuits for Time Delay Calculations", *Analog Integrated Circuits and Signal Processing*, accepted for publication for Springer.
- **M. Kurnaz, S. Minaei, I.C. Goknar**, "Time Delay Calculation in Current-Mode Circuits" 8*th International Conference on Electrical and Electronics Engineering (ELECO 2013)*, 28-30 Nov. 2013, Bursa, Turkey, pp.349-352.