ISTANBUL TECHNICAL UNIVERSITY ★ GRADUATE SCHOOL OF SCIENCE ENGINEERING AND TECHNOLOGY

DESIGN OF AN X-BAND SIGE DRIVER AMPLIFIER

M.Sc. THESIS

Hasip TERLEMEZ

Department of Electronics and Communications

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İSTANBUL TEKNİK ÜNİVERSİTESİ ★ FEN BİLİMLERİ ENSTİTÜSÜ

X-BANT SIGE SÜRÜCÜ KUVVETLENDİRİCİSİ TASARIMI

YÜKSEK LİSANS TEZİ

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Hasip Terlemez, **a M.Sc.** student of ITU **Graduate School of Science Engineering And Technology** student ID **504111205,** successfully defended the **thesis** entitled "**Design of An X-Band SiGe Driver Amplifier**", which he prepared after fulfilling the requirements specified in the associated legislations, before the jury whose signatures are below.

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To Melinda and Thor,

FOREWORD

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May 2014

Hasip TERLEMEZ
Engineer

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ABBREVIATIONS

BiCMOS : Bipolar Complementary Metal Oxide Semiconductor
EHF : Extremely High Frequency
CMOS : Complementary Metal Oxide Semiconductor
G : Gain
GaAs : Gallium Arsenide
GPS : Global Positioning System
HBT : Heterojunction Bipolar Transistor
MOS : Metal Oxide Semiconductor
NF : Noise Figure
NMOS : N Channel Metal Oxide Semiconductor
OIP3 : Output Third Order Intercept Point
OP1dB : Output Power at 1-dB Compression Point
PAE : Power-Added Efficiency
RFID : Radio Frequency Identification
RI : Reverse Isolation
RL : Return Loss
SiGe : Silicon Germanium
VLF : Very Low Frequency

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LIST OF SYMBOLS

β	: Common emitter current gain
C_{π}	: Base-emitter capacitance
C_{μ}	: Base-collector capacitance
C_{JC}	: Collector junction capacitance
C_{JE}	: Emitter junction capacitance
f_T	: Cut-off frequency
f_{max}	: Maximum oscillation frequency
g_m	: Transconductance of a transistor
k	: Boltzmann constant
I_B	: Base current
I_C	: Collector current
I_E	: Emitter current
q	: Elementary charge
R_B	: Base resistance
R_C	: Collector resistance
τ_F	: Forward transit time
T	: Temperature
V_{BE}	: Base-emitter voltage
V_{CE}	: Collector-emitter voltage

DESIGN OF AN X-BAND SIGE DRIVER AMPLIFIER

SUMMARY

In this work, RF amplifier theory is examined for operation modes, amplifier architectures and performance parameters. The requirements and specifications of an RF amplifier are also investigated. Driver amplifier concept and its place in an RF transceiver system are studied. Integrated RF amplifier design methodology and measurement procedures for a manufactured amplifier to examine its performance parameters are explained. Silicon-germanium BiCMOS technology is described and an X-Band driver amplifier designed in a SiGe BiCMOS technology is presented with simulated and measured performance parameters.

SiGe BiCMOS technology offers high performance silicon-germanium heterojunction bipolar transistors with high transition frequency, low noise and high level of process integration with basic CMOS technology. It is possible to implement SiGe high frequency transceivers and CMOS digital functions, power management circuits on the same die with SiGe BiCMOS technology.

Many RF transceivers have an output power in excess of 2 watts. Any power amplifier, last stage for a transmitter, with a gain around 20 dB, requires high input power from a source with good output impedance matching to ensure stability and to increase overall performance. Driver amplifiers are used as building blocks in RF transceivers for such purposes. High gain, linearity, good input and output impedance matching are the main performance parameters of driver amplifiers.

An X-Band SiGe driver amplifier is designed as a part of this study. The amplifier utilizes push-pull architecture and consists of two stages. It shows a measured maximum gain of 19 dB, output power of 12 dBm at the 1-dB compression point, good input and output impedance matching for relevant frequency band. The amplifier is modified to achieve higher performance as a follow up study. Second iteration of the amplifier shows a measured maximum gain of 26 dB, output power of 14 dBm at the 1-dB compression point, good input and output impedance matching.

X-BAND SİGE SÜRÜCÜ KUVVETLENDİRİCİSİ TASARIMI

ÖZET

Radyo frekans teknolojisi modern bilimsel araştırmalar ve endüstriyel ürünler anlamında bir yapı taşı konumundadır. RF teknolojisi yirminci yüzyıl başından itibaren televizyonlarda, radarlarda ve iletişim sistemlerinde kullanılmaktadır. Yüksek frekans RF teknolojisi radyo astronomisi gibi üst düzey bilimsel araştırmalara da öncülük etkmektedir. Tümdevre teknolojilerinin ve tümdevre tranzistörlerin gösterdiği yüksek performans, düşük güç tüketimi ve entegrasyon kapasiteleri radyo frekans teknolojisinin tümdevre bazlı üretimine öncülük etmiştir. Günümüzde yüksek frekans haberleşme sistemleri, radarlar, havacılık uygulamalarında yoğun olarak tümdevre RF sistemler kullanılmaktadır. Bu sistemlerin artan bant genişlikleri ve merkez frekansları çok sayıda sistem için katı hal RF devre tasarımını zorunlu hale getirmektedir. GaAs, SiGe gibi heterojonksiyon bipolar tranzistörler RF tümdevrelerin düşük gürültü, yüksek performans ve entegrasyon kabiliyeti gibi özelliklerinin ön plana çıkmasının sağlamıştır. Bu tranzistörler başta RF kuvvetlendiriciler olmak üzere pek çok devre için önemli aktif elemanlar olarak kullanılmaktadırlar.

Tümdevre RF kuvvetlendiriciler karmaşık radyo frekans sistemlerinin geliştirilmesinde önemli bir basamak oluşturmaktadırlar. RFID, otomobil çarpışma önleme sistemleri, uydu televizyon yayını, uydu takip sistemi, kablosuz yerel ağlar, radar sistemleri karmaşık RF sistemlere örnek gösterilebilir. Farklı sistemler ve farklı uygulama alanları için RF kuvvetlendirici isterleri değişiklik göstermektedir. Bu isterler merkez frekans, bant genişliği, doğrusallık, kazanç, çıkış gücü, verimlilik ve güç tüketimi olarak sınıflandırılabilir. RF kuvvetlendiriciler belirli isterler için farklı topolojiler ve/veya teknolojiler kullanılarak tasarlanabilirler.

RF kuvvetlendiricilerin modern uygulama alanları farklılık göstermektedirler. Frekans bazlı olarak VLF bandından EHF bandına kadar iletişim, navigasyon ve yayın amaçlı uygulama alanları bulunmaktadır. Bu uygulama alanları frekans haricinde çıkış gücü bazlı olarak da farklılık göstermektedirler. Kısa menzilli sistemlerin çıkış gücü genellikle 20 mW altında olmasına karşın, geniş menzilli kablosuz sistemler için çıkış gücü 1 MW üstünde olabilmektedir. Gürültü ve doğrusallık gereksinimleri de farklı sistemleri için değişiklik gösteren isterlerdir. Uydu takip sistemi kuvvetlendirici düşük gürültü isterleri, radar kuvvetlendiricileri yüksek doğrusallık isterleri için örnek gösterilebilir. Kuvvetlendiricilerin alıcı veya verici bazlı kullanımı da bu isterleri etkilemektedir.

Bu çalışmada RF kuvvetlendirici teorisi çalışma modları, kuvvetlendirici mimarileri ve performans parametreleri üzerinden incelenmiştir. RF kuvvetlendiricinin sahip olması gereken özellikler ve isterler belirtilmiştir. Sürücü kuvvetlendiricisi kavramı anlatılmış ve RF alıcı-verici sistemindeki yeri açıklanmıştır. Tümleşik RF kuvvetlendirici tasarım metodolojisi ve üretilmiş bir kuvvetlendiricinin performans karakteristiklerini belirleyici ölçüm yöntemi anlatılmıştır. Silisyum-germanyum

BiCMOS teknolojisi anlatılmış, SiGe BiCMOS teknolojisi kullanılarak tasarlanan X-Band bölgesinde çalışan bir sürücü kuvvetlendirici tasarımı benzetim ve ölçüm sonuçları ile birlikte verilmiştir.

SiGe teknolojisi ucuz, hafif ve yüksek performanslı kişisel iletişim cihazlarının gelişimini hızlandıran bir etmendir. Bu teknoloji küresel konumlandırma sistemi, direkt uydu yayını, yüksek hızlı senkron optik ağ alıcı/vericiler, otomobil çarpışma sistemleri, faz ötelemeli radar sistemleri gibi çeşitli elektronik muharebe, kişisel eğlence ve iletişim sistemleri için de belirleyici bir role sahiptir. SiGe teknolojisi başlangıçta yüksek performanslı hesaplama ihtiyaçları için geliştirilmesine karşın yüksek statik güç tüketimi nedeniyle bu pazarda başarısız olmuştur. Fakat bu teknoloji kablosuz iletişim sistemlerinde benzer güç tüketimleri için CMOS benzerlerinden daha yüksek performans göstermektedir. SiGe heterojonksiyon bipolar tranzistör teknolojisi düşük gürültü, yüksek doğrusallık ve hız gibi önemli RF performans kriterlerini CMOS benzerlerine göre daha az alan kullanarak ve daha düşük maliyetle sağlamaktadır. SiGe HBT teknolojisinin diğer heterojonksiyon bipolar teknolojilerinden ayrılma noktası ise CMOS teknolojisi ile entegrasyon kabiliyetidir. SiGe BiCMOS teknolojisi düşük gürültülü, yüksek geçiş frekanslı silisyum-germanyum heterojonksiyon bipolar transistorler ile temel CMOS teknolojisini aynı kırmık üzerinde üretilebilmesini sağlamaktadır. SiGe BiCMOS teknolojisi ile yüksek frekans SiGe düşük gürültü kuvvetlendiricileri, karıştırıcılar, frekans yükselticiler, gerilim kontrollü osilatörler, güç kuvvetlendiricileri, frekans sentezleyicileri, analog-sayısal ve sayısal-analog işaret dönüştürücüleri ile CMOS sayısal işaret işleme, güç yönetim devreleri aynı kırmık üzerinde yer alabilmektedirler.

Kablosuz RF iletişim sistemleri günümüz elektronik tasarımlarının önemli kısmını oluşturmaktadırlar. Bu tür RF iletişim sistemlerinin yüksek menzil ihtiyaçları alıcı-verici devrelerinin isterlerini belirlemektedir. RF alıcı-verici devrelerinin çıkış katlarının güç isterleri çoğunlukla 2 watt üzerinde olmaktadır. RF alıcı-verici devresinin çıkış katı olan güç kuvvetlendiricisinin kazancı 20 dB yakınlarında ise kuvvetlendirinin yüksek performans göstermesi ve kararlı olması için bu kuvvetlendiricinin yüksek giriş gücü ile iyi çıkış empedans eşleşmesine sahip bir kaynak tarafından sürülmesi gerekmektedir. Sürücü kuvvetlendiriciler RF alıcı-vericilerde bu amaçla kullanılan devrelerdir. Yüksek kazanç, doğrusallık, iyi giriş ve çıkış empedans eşleşmesi sürücü kuvvetlendiricilerin önemli performans karakteristikleridir.

Bu çalışmada X-Band frekans aralığında çalışan bir SiGe sürücü kuvvetlendiricisi tasarlanmıştır. Bu kuvvetlendirici push-pull devre mimarisine sahip olup, iki kattan oluşmaktadır. Push-pull mimarisi tümdevre tasarımındaki kırmık için metal bağlantılar, kırmık-sistem ara bağlantı telleri, çeşitli jonksiyon kapasiteleri, uzun bağlantı endüktansları, besleme hattı dirençleri gibi parazitiklerin devre tasarımına olan etkisinin minimal olmasını sağlamaktadır. İki kattan oluşan tasarımın ilk katı kazanç elde etmek için oluşturulup yüksek performanslı SiGe heterojonksiyon bipolar tranzistörler kullanılarak tasarlanmıştır. İkinci kat sürücü kuvvetlendiricinin kazanç ve güç amaçlı olarak tasarlanan bölgesidir. Bu katta orta gerilime dayanan SiGe heterojonksiyon bipolar tranzistörler kullanılmıştır. Push-pull kuvvetlendiricinin çalışması için gerekli işaretler devredeki entegre transformatörlerin tek uçlu giriş işaretini farksal işarete dönüştürmesi ile sağlanmıştır. Benzer bir transformatör çıkışta bu farksal işaretin RF sistem ihtiyaçlarına uygun tek uçlu işarete dönüştürülmesi için kullanılmıştır. Devrede

kullanılan transformatörler ilgili SiGe BiCMOS teknolojisinin sağladığı en üst iki kalın metal kullanılarak tasarlanmıştır. Transformatörler simetrik iki sarımdan oluşmakta olup yüksek bağlaşma katsayısı ve farksal sinyal açısından yüksek faz ve genlik eşleşmesi göstermektedirler. Devrenin giriş ve çıkış eşleşmesi, transformatör sarım endüktansları, bağlantı telleri endüktansları ve tranzistör giriş/çıkış kapasiteleri ile oluşturulan rezonanslar ile sağlanmıştır.

Devrenin tasarım aşamasındaki şematik gösterimi, benzetim sonuçları, tümdevre serimi tez kapsamında verilmiştir. İlgili kuvvetlendiricinin üretim sonrası kırmık fotoğrafları, ölçüm için kullanılacak test modülü, çeşitli ölçüm düzenekleri ve ölçüm sonuçları tezin devamında gösterilmiştir.

Yapılan ölçümler sonrası kuvvetlendiricinin en yüksek kazanç değerinin 22 dB ve 1-dB bastırma noktasındaki çıkış gücünün 12 dBm olduğu görülmüştür. Çalışmanın devamında kuvvetlendiricinin performansının yükseltilmesi için devre yapısında değişiklikler yapılmıştır. Yapılan ölçümler sonrasında ikinci kuvvetlendiricinin en yüksek kazanç değerinin 26 dB ve 1-dB bastırma noktasındaki çıkış gücünün 14 dBm olduğu görülmüştür. Her iki kuvvetlendirici ilgilenilen frekans aralığı için iyi giriş ve çıkış empedans eşleşmesi göstermektedir.

1. INTRODUCTION

Radio frequency technology is one of the most important technologies of modern scientific world. Starting with the twentieth century radio frequency technology was used in televisions, radars and all telecommunication systems. Improvement of radio frequency equipment in higher frequencies enabled many research projects in radio astronomy field. As the integrated transistors improved over years, communication systems, radio frequency aerospace applications and radars were dominated by solid-state RF circuits with ever increasing frequencies. Gallium arsenide technology was a start for developing transistors showing better performance and operating in high frequencies. These transistors were developed to be used in RF systems, mainly RF amplifiers.

Solid-state RF amplifiers played an important role in development of complex radio frequency systems, such as global system for mobile communications, wireless local area networks, satellite television, global positioning system, RFID, automobile collision avoidance systems and maritime radars. Different systems with different applications have many unique requirements for frequency, bandwidth, linearity, gain, power, efficiency, etc. RF amplifiers can be designed for specific requirements with many different architectures, techniques and solid state technologies.

Modern applications of RF amplifiers are highly varied. Different frequencies from VLF to EHF are used communication, navigation and broadcasting. Their output powers are also vary with applications. While short range wireless systems requires around 10 mW of power, long range broadcast transmitters usually need over 1 MW output power [1]. RF amplifiers are also being used in radars, RF heating, plasmas, magnetic resonance imaging and laser drivers. Noise and linearity requirements are other important factors to be taken into consideration depending on the usage of RF amplifier. Many GPS modules have a very low noise RF amplifier as a first stage of their receivers. Cellular RF transceiver modules performs the RF front end transmit/receive function in time-division-duplex or frequency-division-duplex communication systems. They operate over a wide frequency range and their

transmitters usually include a driver amplifier that requires high linearity. This work focuses on the driver amplifiers but includes general knowledge about RF amplifiers as a whole literature abstract in the second chapter.

Silicon-germanium technology is the driving force behind the exponential development of low cost, lightweight, personal communications devices as well as other entertainment, information and electronic warfare technologies like direct broadcast satellite, global positioning system, automobile collision avoidance systems, high speed synchronous optical network transceivers and phased arrayed radars [1]. Silicon-germanium technology was originally developed for the high-end computing market but failed due to the high static power consumption of the SiGe HBTs. Interestingly, for RF communications circuits, silicon-germanium technology is more suitable than conventional CMOS technology as SiGe HBTs consume much less power than CMOS to achieve the same level of performance. Silicon-germanium technology offers SiGe HBTs with low noise, high linearity and high speed than their conventional CMOS equivalents for lower production cost and size. It is also quite important that SiGe BiCMOS technology offers the advantages of both SiGe HBTs and basic CMOS transistors on the same die. A vast range of RF and mixed-signal circuits can be designed with SiGe BiCMOS technology, such as low noise amplifiers, power amplifiers, mixers, voltage controlled oscillators, synthesizers, high speed analogue to digital and digital to analogue converters. It is also possible to implement SiGe high frequency transceivers and CMOS digital functions, power management circuits on the same die with SiGe BiCMOS process. These, multifunction, system on chip solutions can be found in cordless phones, mobile phones, wireless local area networks, satellite communications and automotive navigation and toll systems [2]. Third chapter focuses on silicon-germanium technology, aspects and fabrication of SiGe HBTs.

RF amplifier design is vital to our current technological advancement trend of wireless communications, broadcasting and electronic warfare. Transmitters of such systems require high output power to operate over a long range. RF power amplifiers provide these high output power levels. Any power amplifier with a gain around 20 dB and output power around 2 watts requires high input power to drive the antenna with maximum output power. Many power amplifiers also require input power to be sourced from a known, specified impedance to ensure stability and to

improve performance. Driver amplifiers are used as building blocks in RF transceivers for such purposes. High gain, linearity, good input and output impedance matching are the main performance parameters of driver amplifiers. Last chapter focuses on design methodology and measurement procedures for RF driver amplifiers, presents an X-Band SiGe driver amplifier design and a second iteration with better performance.

2. RF AMPLIFIER THEORY

This chapter consists of general information about RF amplifier theory. Performance parameters and main characteristics of RF amplifiers are explained. Different amplifier architectures, conventional, overdriven and switching mode amplifiers are also examined. This section covers requirements, specifications and architectures for an integrated driver amplifier design but definitions can applied to all RF amplifiers.

2.1 Performance parameters

RF driver amplifiers are used as gain stages with medium output power capabilities. They are expected to provide good gain, input and output return loss over an application specific frequency range. A driver amplifier usually needs to be linear and its output power level should be high enough to saturate following power amplifier. Driver amplifiers are the last stage for many integrated RF transceiver systems [3-6] and their efficiency plays a role to determine power consumption, hence thermal characteristics of integrated RF transceiver systems. Almost all of these performance parameters are part of a trade-off and they should be optimized for requirements of different applications. Frequency range, gain, input return loss, output return loss, reverse isolation, stability, 1-dB compression point, intercept point, power-added efficiency, noise figure are main performance parameters of a driver amplifier and they are explained in this chapter. It should be noted that an RF amplifier can be modelled as a two port network and S parameters can be used to define some of the stated performance parameters. This work references gain, input return loss, output return loss, reverse isolation and stability to their corresponding S parameters and related equations with input terminal of the amplifier as port 1, output terminal of the amplifier as port 2.

2.1.1 Frequency range

RF driver amplifiers are designed to operate for certain frequencies. Frequency range of an amplifier defines bandwidth of a transceiver system and wide band amplifiers

can be used in multiple systems for different applications. Many of performance parameters of an amplifier are given for a certain frequency range.

2.1.2 Gain

Gain of a driver amplifier is defined as power gain. Gain is the ratio of output power delivered to load and input power applied to the amplifier. It is expressed in decibels. The magnitude of the square of S_{21} is equal to the power gain in decibels. The bandwidth of the amplifier is defined as the frequency range between 3 dB drop points of the gain. The ripple of the gain over a certain frequency range defines gain flatness. The gain equation is shown below.

$$G = 10\log_{10}(|S_{21}|^2) = 20\log_{10}|S_{21}| \quad \textbf{(2.1)}$$

2.1.3 Input return loss

Input return loss is the ratio of the input power applied to the amplifier and the power reflected back to the source. It is expressed in decibels. The magnitude of the square of S_{11} is equal to the input return gain in decibels and its adverse is equal to the input return loss. The input return loss equation is shown below.

$$RL_{input} = -10\log_{10}(|S_{11}|^2) = -20\log_{10}|S_{11}| \quad \textbf{(2.2)}$$

2.1.4 Output return loss

Output return loss is the ratio of the output power delivered to the load and the power reflected back to the amplifier. It is expressed in decibels. The magnitude of the square of S_{22} is equal to the output return gain in decibels and its adverse is equal to the output return loss. The output return loss equation is shown below.

$$RL_{output} = -10\log_{10}(|S_{22}|^2) = -20\log_{10}|S_{22}| \quad \textbf{(2.3)}$$

2.1.5 Reverse isolation

Reverse isolation is the ratio of the power applied to the output of the amplifier and the power delivered to the load connected at the input of the amplifier. It is expressed in decibels. The magnitude of the square of S_{12} is equal to the reverse gain in decibels and its adverse is equal to the reverse isolation. Reflected signals can pass through the amplifier in the reverse direction. This unwanted reverse transmission can cause the reflected signals to interfere with the desired fundamental signal

flowing in the forward direction. Therefore, reverse isolation is important to quantify. The reverse isolation equation is shown below.

$$RI = -10\log_{10}(|S_{12}|^2) = -20\log_{10}|S_{12}| \quad \textbf{(2.4)}$$

2.1.6 Stability

Stability of an amplifier is an indication of the immunity of the amplifier to causing spurious oscillations, so that it does not generate a signal at its output without an input signal. The oscillations can be large-signal problems causing disturbance at the output of the amplifier or more subtle spectral problems causing disturbance to the system. A common indicator that is used to measure stability is the K-factor. If K-factor of an amplifier is over 1, that amplifier is unconditionally stable. If it is greater than zero but less than 1 the amplifier is only conditionally stable and it can oscillate under certain source or load impedances. The equation for the K-factor is given below.

$$K = \frac{1-|S_{11}|^2-|S_{22}|^2-|S_{11}S_{22}-S_{12}S_{21}|^2}{2|S_{21}S_{12}|} \quad \textbf{(2.5)}$$

2.1.7 1-dB compression point

The linearity of an amplifier refers to a constant gain indifferent to input power level. However, in practice there is a drop in gain as the input power applied to the amplifier increases. 1-dB compression point is defined as the input or output power level that decreases gain by 1 dB. The gain decreases quickly after this input level and the change in output power will not be linear with changes in the input power level. Saturation point is defined as the input power level where the gain of the amplifier is zero. Figure 2.1 shows the 1-dB compression point. Output power at the 1-dB compression point is a key performance parameter for RF driver amplifiers.

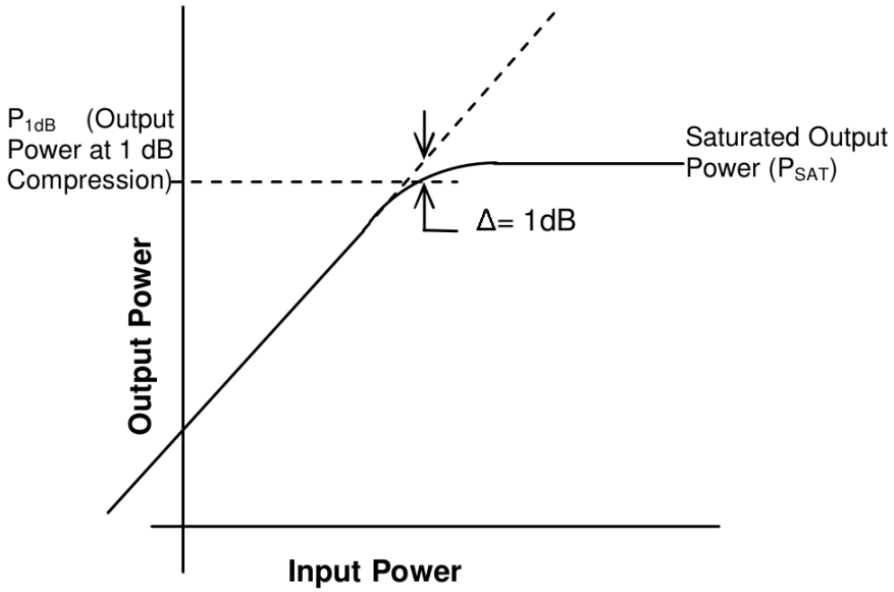

Figure 2.1 : 1-dB compression point of an RF amplifier.

2.1.8 Intercept point

Due to the inherent non-linearity of the RF amplifiers, two or more signals arriving simultaneously at the input of an amplifier produce additional unwanted signals at the output. This is called as intermodulation distortion. These additional signals are called as intermodulation products. Interaction of two input signals with different frequencies produces intermodulation products at the sum and difference of integer multiples of the original frequencies. Sum of the frequency multiplier integers gives the order of the intermodulation product. 2nd, 3rd and 4th order intermodulation products for input signal frequencies of f_1 and f_2 is shown in Figure 2.2.

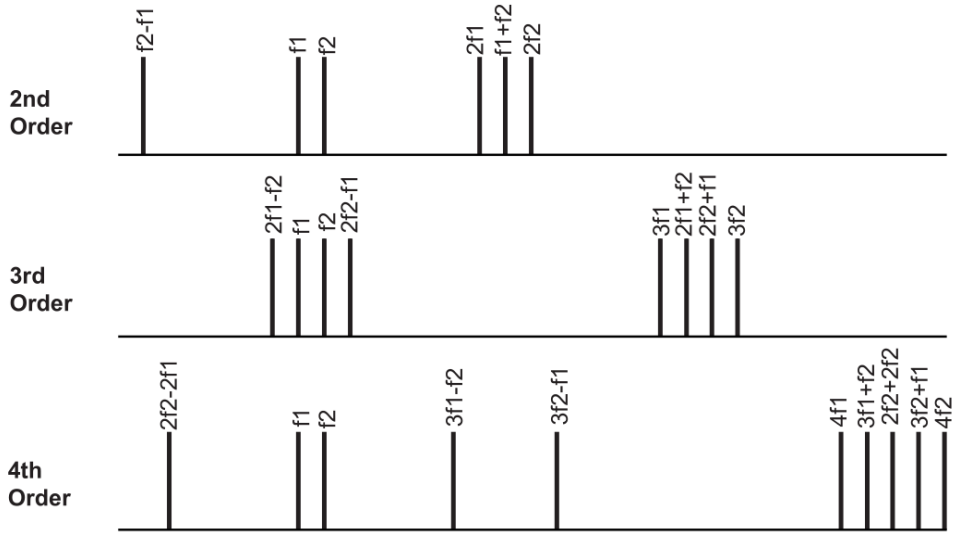

Figure 2.2 : Intermodulation products for input signal frequencies of f_1 and f_2.

Third order intermodulation products have an amplitude proportional to the cube of the input signal and second order components have an amplitude proportional to the square of the input signal. Intercept point is defined as the crossing point of fundamental signal and N-th order intermodulation product for increasing input power levels. Figure 2.3 shows the concept of intercept point with extrapolation of fundamental signal, second order and third order intermodulation product.

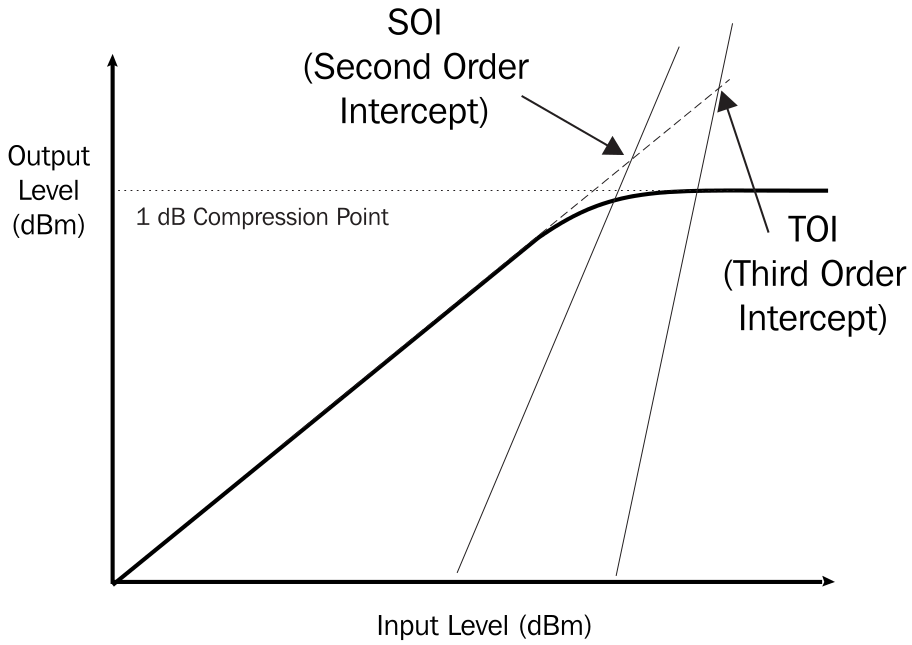

Figure 2.3 : Intermodulation products for input signal frequencies of f_1 and f_2.

2.1.9 Power-added efficiency

The efficiency of an amplifier is its ability of converting DC power to the output RF power. Power consumed by the amplifier reduces its efficiency. Output power of an amplifier increases as its input power is increased below saturation point. After saturation, increased input power only generates heat for the amplifier. Power-added efficiency is a measure of the efficiency of an amplifier that considers input RF power as well as DC power and output RF power to exclude such effects. The equation for power-added efficiency is given below.

$$PAE = \frac{100(P_{output} - P_{input})}{V_{DC} I_{DC}} \quad \textbf{(2.6)}$$

2.1.10 Noise figure

Noise factor of an amplifier is defined as the ratio of signal to noise ratio at the input and signal to noise ratio at the input. Noise figure is a measure of how much an

amplifier degrades the signal to noise ratio of an RF system. Noise figure is equivalent of noise factor in decibels. Equations for noise factor and noise figure can be seen below.

$$F = \frac{SNR_{input}}{SNR_{output}} \quad \textbf{(2.7)}$$

$$NF = 10\log_{10}\left(\frac{SNR_{input}}{SNR_{output}}\right) \quad \textbf{(2.8)}$$

2.2 Operation Modes

Operation mode of an amplifier mainly determines output power, efficiency and linearity. Different modes or classes of operation usually do a trade-off between these performance parameters. Amplifier classes are defined by their bias points, therefore by their conduction angles. Conduction angle is described as the interval that amplification transistor is conducting current. The current of an amplification transistor without an input signal is called as quiescent current. As quiescent current of a transistor increases, power consumption and heat dissipation also increases by default. Heat dissipation could be problem for the amplifier by causing a thermal runaway or it could be problem for system-on-chip by creating heat gradients and reducing performance overall. This section gives general information about operation modes or classes of RF amplifiers. It should be noted that multi stage amplifiers usually employs two or more operation modes to find the best point for output power, efficiency and linearity trade-off.

2.2.1 Class A

Class A amplifier is defined as an amplifier with an operating point that allows output current for whole amplification process. Input power of a class A amplifier should be low enough to make sure that the amplifying transistor never goes into cut-off region. This means that conducting angle of a class A amplifier is 360 degrees. Output current waveform of a class A amplifier can be seen in Figure 2.4.

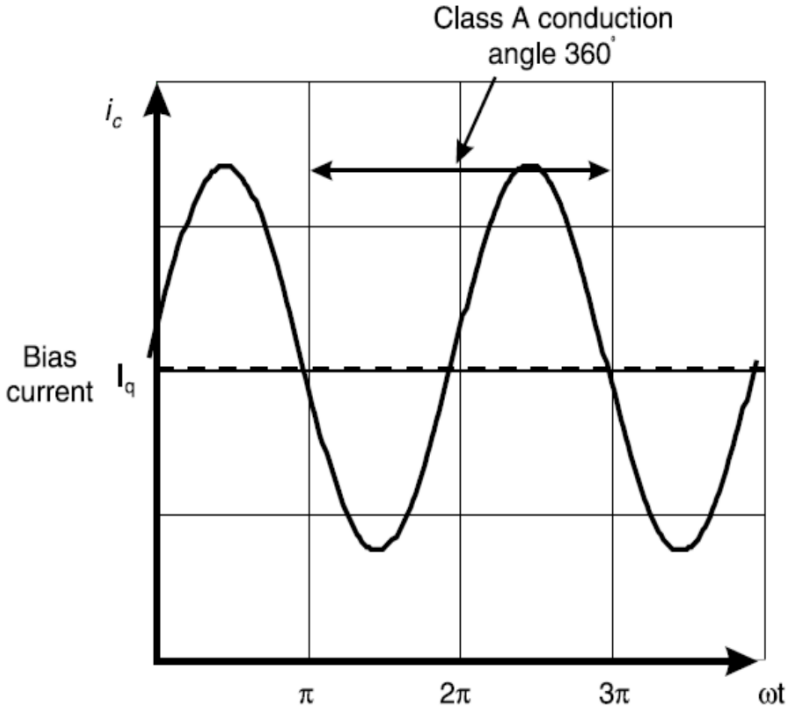

Figure 2.4 : Output current waveform of a class A amplifier.

Quiescent current of a class A amplifier is at least half of the maximum output current of the amplifying transistor. Output current could be collector or drain current, depending to the type of output transistor. Class A mode is the most linear one of all amplifier operation modes. Output signal of a class A amplifier is not deformed by a transistor cut-off or overdrive. Class A mode also has the highest gain of all amplifier operation modes, due to input signal being amplified for conduction angle of 360 degrees. Since the quiescent current of a class A amplifier is high, efficiency of this mode is low. An ideal class A amplifier has an efficiency of 50%.

2.2.2 Class B

Class B amplifier is defined as an amplifier with an operating point that allow output current for half of the amplification process. This means that conducting angle of a class B amplifier is 180 degrees. Output current waveform of a class B amplifier can be seen in Figure 2.5.

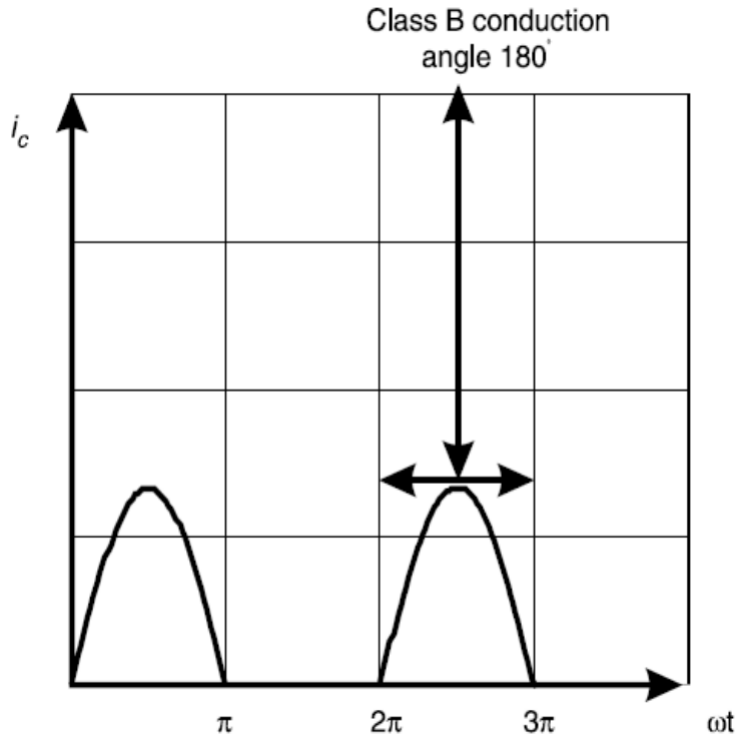

Figure 2.5 : Output current waveform of a class B amplifier.

Quiescent current of an ideal class B amplifier is zero. However, quiescent current of a class B amplifier is usually around 5% of the peak output current of the transistor. This current is adjusted to minimize crossover distortion and transistor nonlinearities at low output current values. Class B amplifiers requires more input drive level for the same output power level of class A amplifiers. Class B mode provides lower gain than class A mode, due to input signal being amplified for only half of the duration. Class B amplifiers are more efficient than their class A counterparts. An ideal class B amplifier has an efficiency of 78.5%.

2.2.3 Class AB

Class AB amplifier is defined as an amplifier with an operating point between class A mode and class B mode. Class AB amplifiers have conduction angles between 180 degrees and 360 degrees. Output waveform of a class AB amplifier can be seen in Figure 2.6.

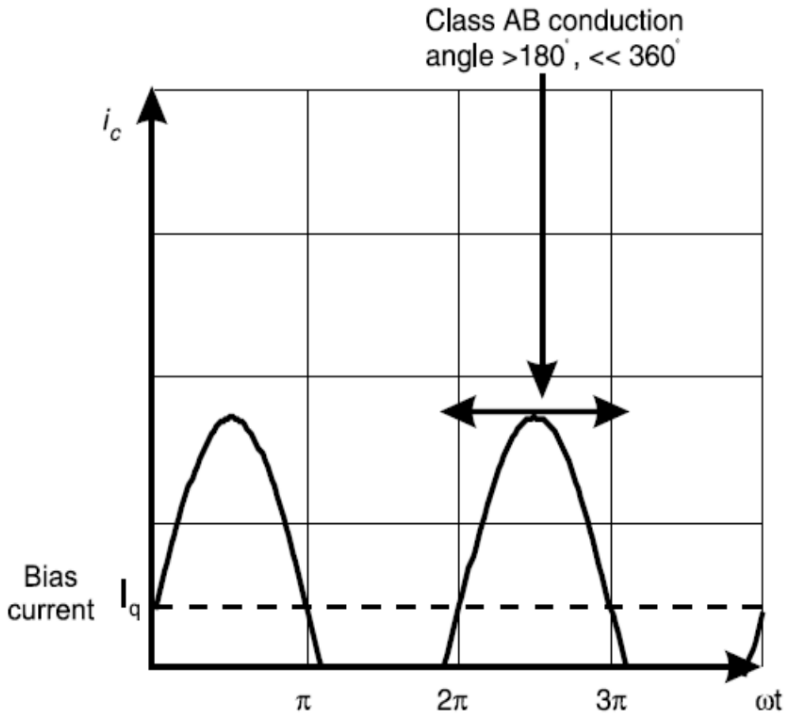

Figure 2.6 : Output waveform of a class AB amplifier.

Class AB amplification mode is a compromise between class A and class B modes in terms of gain, output power and linearity. Class AB amplifiers are more efficient than their class A counterparts as a trade-off of their linearity. As a consequence of their conduction angle between 180 degrees and 360 degrees, the efficiency of class AB amplifiers are between 50% and 78.5%.

2.2.4 Class C

Class C amplifier is defined as an amplifier with an operating point that allows amplification less than half of the input signal cycle. This means that conducting angle of a class C amplifier is less than 180 degrees. Output waveform of a class C amplifier can be seen in Figure 2.7.

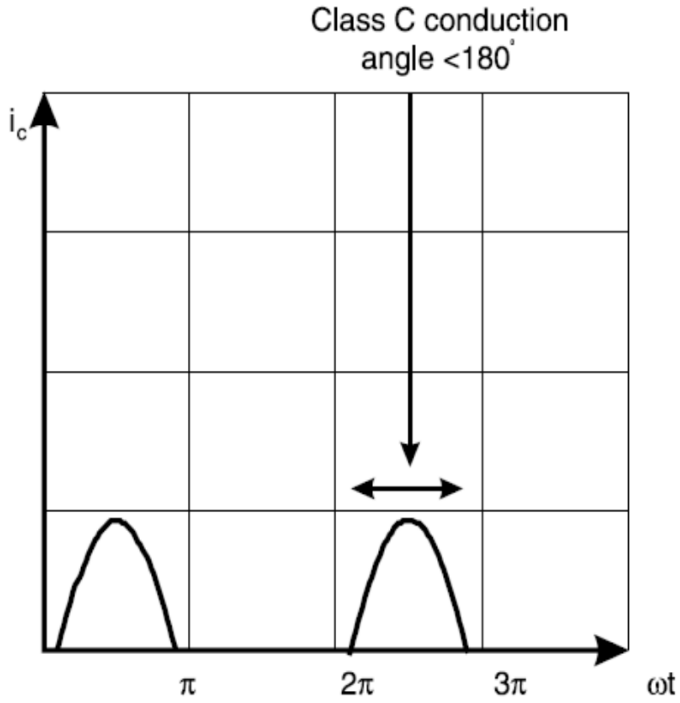

Figure 2.7 : Output current waveform of a class C amplifier.

Class C amplifiers biased at a point that idle behaviour of the amplification transistor is cut-off and no drain or collector current flows. Linearity of a class C amplifier is worse than class A and class B amplifiers due to reduced conduction angle and its effects on producing a signal with modulated envelope [7]. Efficiency of a class C amplifier can approach to 90% depending on the bias point and conduction angle.

2.2.5 Class D

Class D amplifier is defined as a switching mode amplifier that uses transistors as switches to generate square waveform at the output. A tuned filter at the output is also required to pass only the fundamental frequency to the load. Class D amplifiers can be voltage mode or current mode depending on the application and output filter characteristics. Output waveform of a voltage mode class D amplifier can be seen in Figure 2.8.

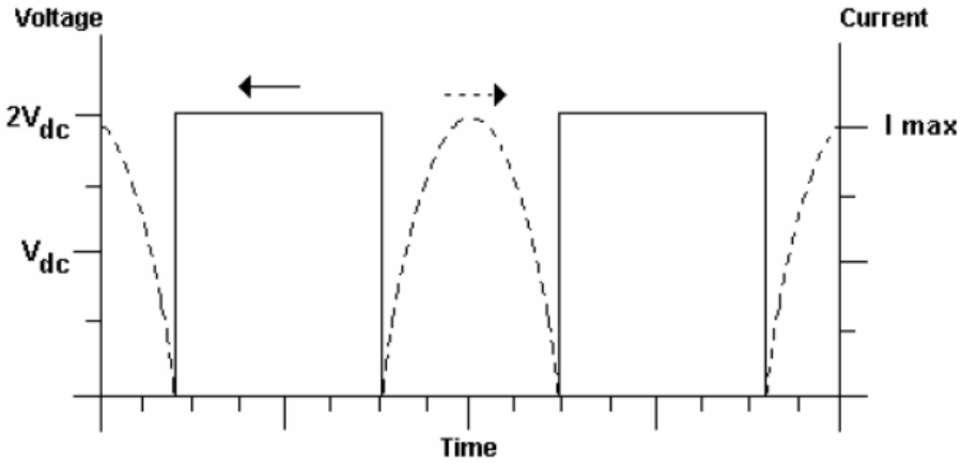

Figure 2.8 : Output waveform of a class D amplifier.

Efficiency of an ideal class D amplifier theoretically approaches to 100%. However, device parasitics such as drain-source capacitances, collector-emitter capacitances, interconnect inductances and non-zero switch resistances limit efficiency of the class D amplifiers to a lower value.

2.2.6 Class E

Class E amplifier is basically a single transistor operated as a switch. Class E amplifiers are switching mode amplifiers that generate output voltage by charging parasitic output capacitance. Class E amplifiers employ RF choke and tuned load network to operate properly. When switch is on collector or drain voltage is zero and when it is off collector or drain current is zero. Efficiency of class E amplifier is higher than similar class D switching mode amplifiers because parasitics can be included to tuned load network and overall switching losses are lower than class D mode.

2.2.7 Class F

Class F amplifiers are very similar to class E amplifiers but they employ harmonic resonators in the output matching network. These harmonic resonators are tuned to provide open circuit to odd harmonics and short circuit to even harmonics. This process generates a square shaped output voltage with sharp edges, resulting in reduced overlap between current and voltage waveforms and increased efficiency.

2.3 Architectures

RF amplifiers can be designed in many ways for different applications regarding their needs. Many RF amplifiers are consists of multiple gain, driver and power stages. If an application needs high output power, there might be a power combining network. This section covers push-pull and balanced configurations, multistage amplifier design.

2.3.1 Push-pull amplifiers

The basic push-pull amplifier architecture consists of two RF amplifiers that are driven differentially so that they operate in different phases. Output load of these amplifiers also connected differentially between these amplifiers with a balun. These RF amplifiers are also driven by a balun to ensure anti-phase operation. Since baluns are matched to a specific impedance value, push-pull amplifiers have an impedance matching network at their inputs. Baluns that used in the output are also matched to a specific impedance value and RF amplifiers have optimum load impedance that gives best gain or power results. Therefore, push-pull amplifiers also have impedance matching networks at their outputs. Single stage push-pull amplifier is shown in Figure 2.9.

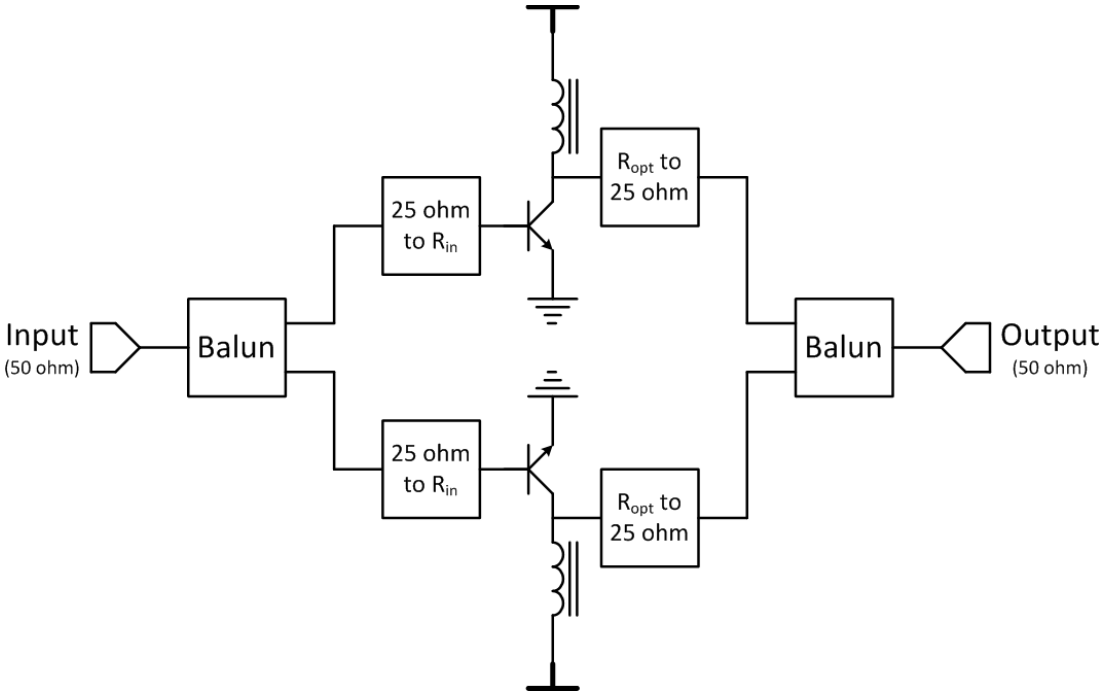

Figure 2.9 : Single stage push-pull amplifier.

Push-pull amplifiers have the efficiency as two single-ended amplifiers that used in the design. Differential operation allows push-pull amplifiers to have higher gain and output power than their single-ended counterparts. Insertion loss of baluns and impedance matching networks should be minimized to have a gain advantage over single-ended amplifiers. Differential operation allows push-pull amplifier to have a good second harmonic performance. Push-pull operation ensures both amplifiers to have their voltage and current values equally different from idle state with opposite signs. Therefore, voltage drops affecting ground and supply nodes in single-ended amplifiers will be eliminated in push-pull amplifiers. It is also known that push-pull architecture is robust against parasitics and bondwire inductances [8,9].

2.3.2 Balanced amplifiers

Push-pull amplifiers are a subset of balanced amplifiers but balanced amplifiers have a more specific definition in RF amplifier theory. Balanced amplifiers are defined as two identical amplifiers with an input signal from an input power splitter which produces two signals in phase quadrature and the outputs are combined using an output power combiner. Input power splitter and output power combiner are usually quadrature 3-dB couplers. The main advantage of this architecture is any reflection, due to imperfect impedance matching, pass back through the couplers and cancel each other [10]. Balanced amplifier configuration is shown in Figure 2.10.

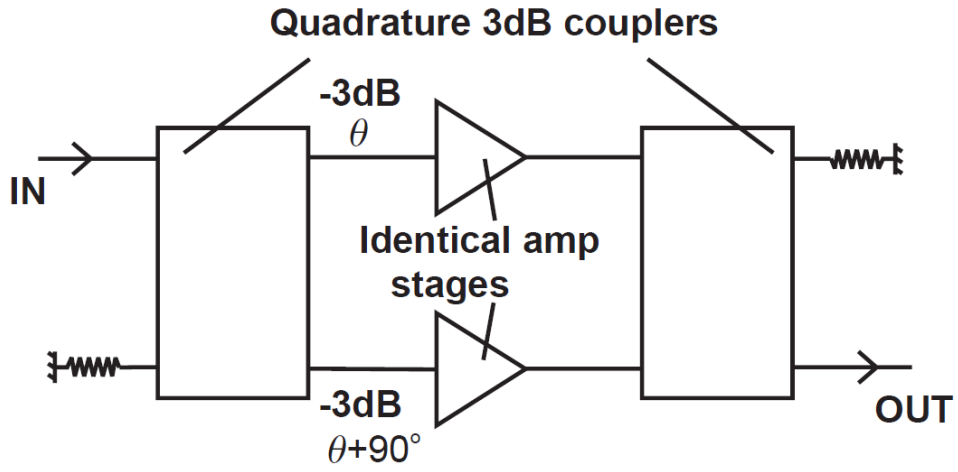

Figure 2.10 : Balanced amplifier configuration.

A balanced amplifier cannot be designed without a good power splitter and combiner. Balanced operation of the amplifier requires quadrature 3-dB coupler. 3-dB quadrature coupler is a well-known component, usually designed with a pair of

coupled quarter wave transmission lines. A generic quadrature coupler and its frequency response are given in Figure 2.11.

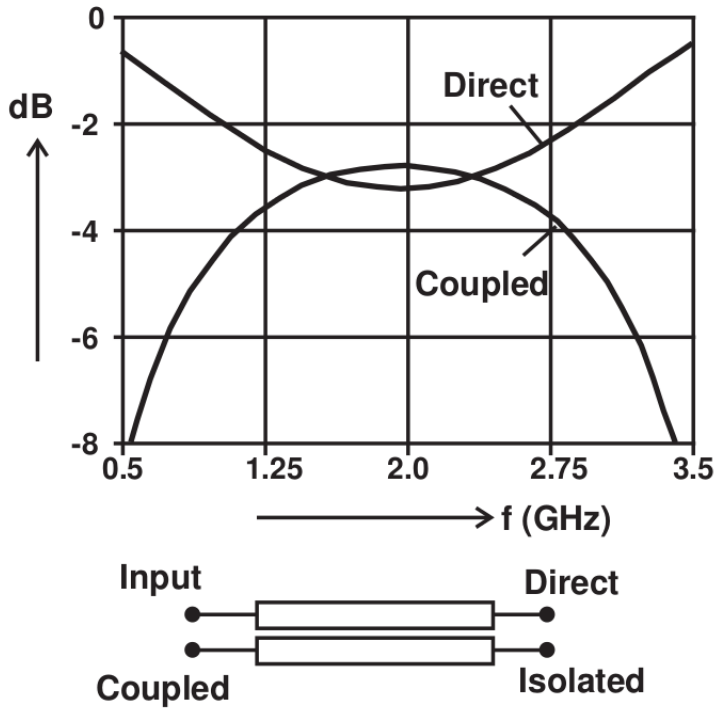

Figure 2.11 : Quadrature coupler and frequency response.

2.3.3 Multistage amplifiers

RF amplifiers usually need multiple stages with different purposes. Gain, linearity and output power requirements of the amplifier define the number and the purpose of these stages. Gain stage is used when input power of the amplifier is low and gain requirement of the amplifier is high. Driver stage is used when output power of the amplifier should be high enough to saturate next stage. Power stage is used when output power requirement of the amplifier is high. Efficiency of the gain stage and the driver stage is usually negligible due to high power consumption of the power stage. Overall linearity of the amplifier is limited by each stage of the amplifier chain. Linear amplifier design requires a balance between gain and output power at 1-dB compression point of corresponding stage. Since every stage has different optimum load impedance for their operation, interstage impedance matching networks are placed in between. Interstage matching networks could include some elements to provide bias or supply voltage and to help with the stability of the amplifier.

3. SILICON-GERMANIUM TECHNOLOGY

Silicon-germanium heterojunction bipolar transistors are high performance transistors with maximum transition, oscillation frequencies over 300 GHz. They also extremely low values of noise figure. SiGe HBTs can be easily integrated with MOS transistors in a BiCMOS technology, allowing high performance SiGe HBTs to be used in RF side and CMOS transistors to be used in digital gates on the same integrated circuit. These features make SiGe BiCMOS technology an ideal process for RF system design.

SiGe HBT is a revolution for bipolar transistor design. Before emergence of SiGe heterojunction bipolar transistor, compound semiconductor technologies, such as GaAs, was used to produce heterojuction bipolar transistors. Heterojunction forming was thought to be difficult between silicon and germanium due high lattice mismatch between them. Research made on semiconductor materials showed that a good heterojunction can be formed between silicon and germanium only if the SiGe layer is thin and germanium content is below 30 percent. It is possible to grow SiGe layer that fits onto the silicon lattice without dislocations and imperfections under these conditions [2]. Figure 3.1 shows cross-sectional view of integrated basic planar bipolar transistor, self-aligned double polysilicon bipolar transistor and silicon-germanium heterojunction bipolar transistor.

As it can be seen from the cross-section of SiGe HBT, p+ SiGe base layer is grown after silicon dioxide isolation formation. It is followed by p+ type silicon side layer growth. Polysilicon layers formed to construct base in a similar way that has been used in self-aligned double polysilicon bipolar technology. RF performance of SiGe heterojunction bipolar transistors are enhanced by these heavily doped layers. Collector is formed by n+ type growth of single-crystal materials. Emitter is constructed by heavy n+ type doping of polysilicon once again helping to improve RF performance [11].

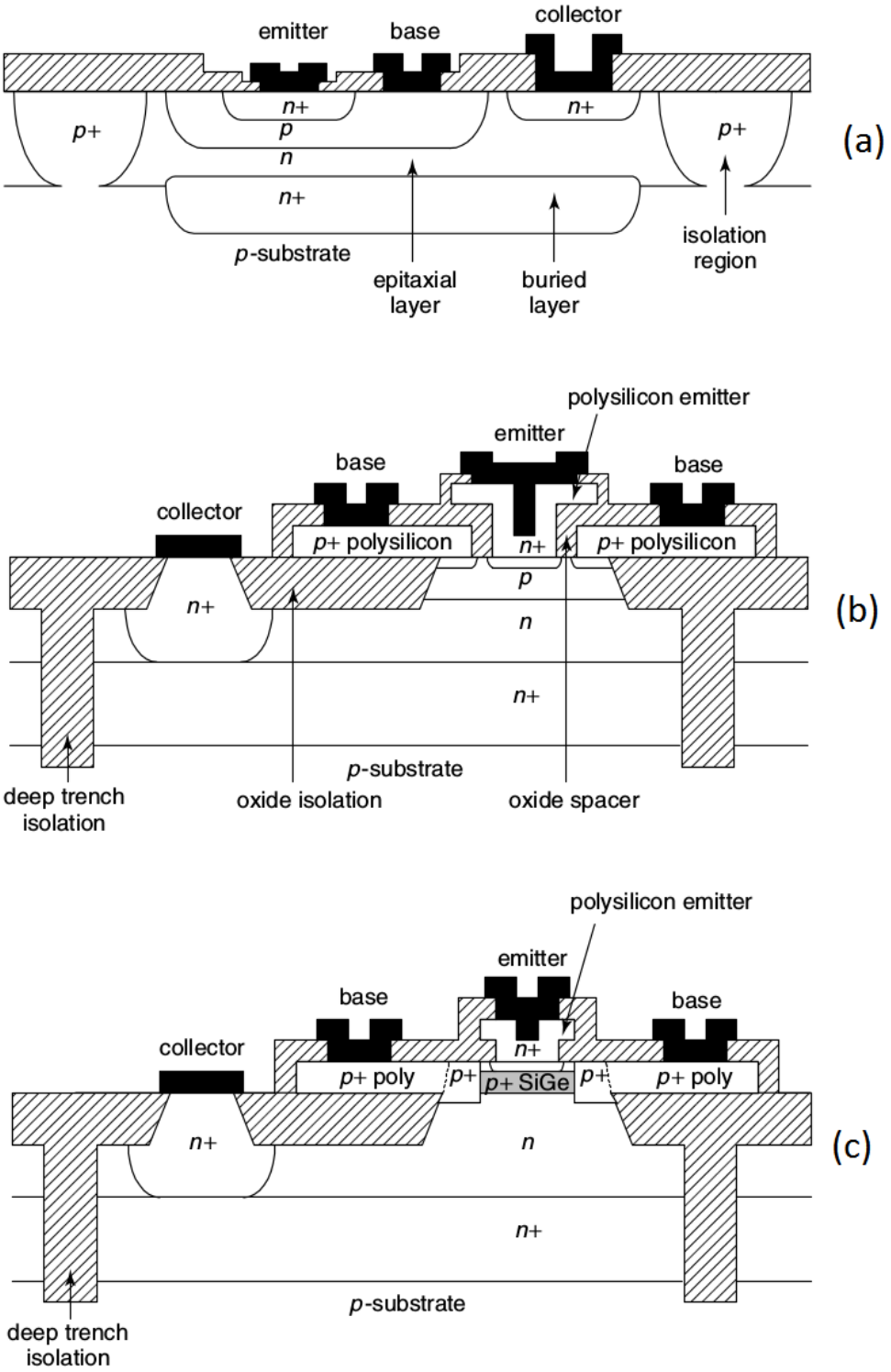

Figure 3.1 : Cross-sectional view of integrated basic planar (a), self-aligned double polysilicon (b), SiGe heterojunction (c) bipolar transistors.

3.1 Operating Principles of SiGe HBTs

SiGe HBTs need bias voltage applied to the emitter/base and collector/base junctions. All possible bias configurations can be constructed by biasing these junctions. Operating modes of SiGe HBTs are shown in Figure 3.2.

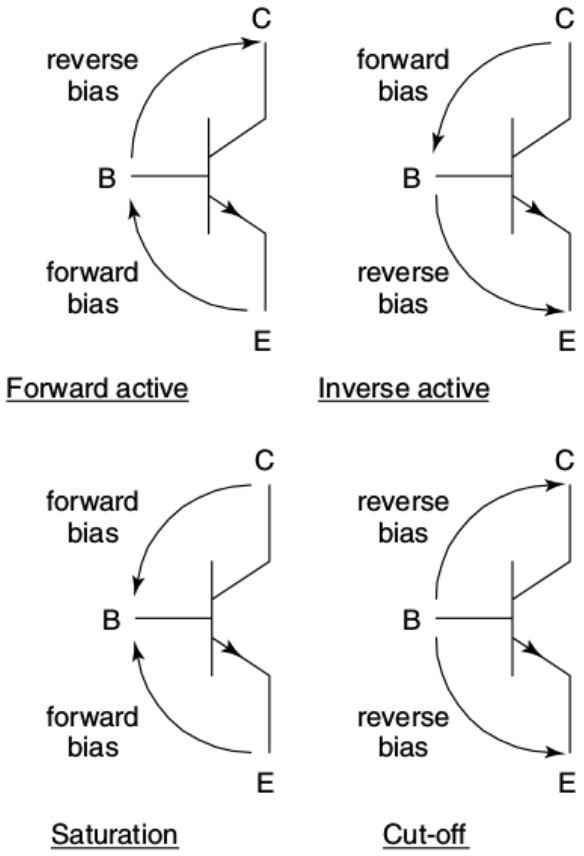

Figure 3.2 : Operating modes of SiGe HBTs.

The current gain of the transistor can be utilized in forward active operation mode. Base-emitter junction is forward biased and collector-base junction is reverse biased in this operation mode. Forward bias voltage depends on base layer formation and overall doping of active regions. It is usually around 0.8 V for SiGe HBTs. Inverse active operation mode also provides some gain but it is much lesser than forward active operation mode. Reverse bias is applied to base-emitter junction and forward bias is applied to collector-base junction in this mode. Cut-off operation mode is used to configure the transistor as an open switch by applying reverse bias to both junctions. Saturation operation mode allows current flow between collector and emitter and the transistor operates as a short switch by applying forward bias to both junctions.

One of the most important electrical properties of SiGe HBTs is the common emitter current gain of the transistor. It is defined as the ratio of collector current to base current, equation can be seen below.

$$\beta = \frac{I_C}{I_B} \tag{3.1}$$

The current gain is valid for forward active operation mode. The forward bias applied to the base-emitter junction supplies the base with a large number of electrons from the emitter. The electron concentration of the base becomes gradient with the forward bias. This gradient encourages the electrons to diffuse to the collector. Since the base of the SiGe HBT is narrow, the most of the injected electrons diffuse to the collector-base junction and reach to the collector due to reverse bias of the collector-base junction. The small base widths of the SiGe HBTs, essentially all bipolar transistors, are what distinguish them from two back to back connected diodes. The base width of the transistor should be smaller than the diffusion length of electrons in the base. The heavy doping of emitter allows the emitter current to be much higher than the base current [2,11].

Common emitter configuration is the most popular circuit configuration of the SiGe HBTs. There are other configurations called common base and common collector. These configurations are named by their common terminal shared by input and output. These three circuit configurations are shown in Figure 3.3.

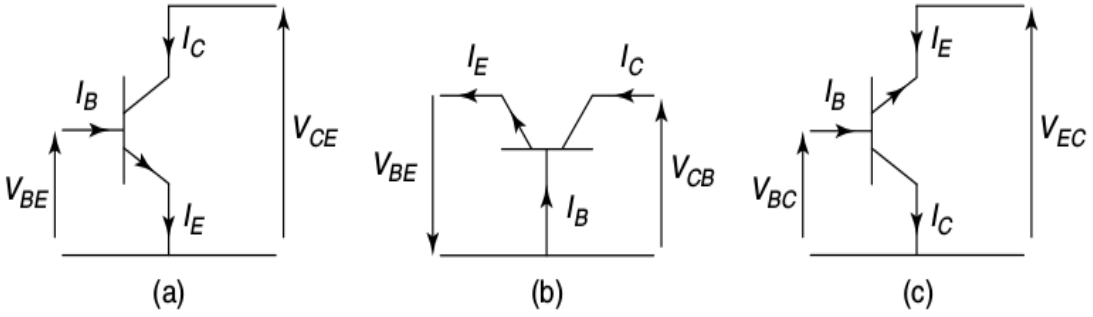

Figure 3.3 : Three circuit configurations of SiGe HBTs.

3.2 Junction Breakdown

Reverse bias voltage that applied to collector-base junction has an upper limit. High reverse bias voltage causes the junction to break down and allows a high current between the collector and the emitter. This upper limit voltage is called as breakdown voltage and the incident is called as junction breakdown. The general operation principles of SiGe HBTs are not valid for breakdown region.

There are several physical mechanisms that causes junction breakdown or allows high current at high voltages. These mechanisms are punch-through, zener breakdown and avalanche breakdown. An illustration of different breakdown mechanisms with a changing reverse bias voltage can be seen in Figure 3.4.

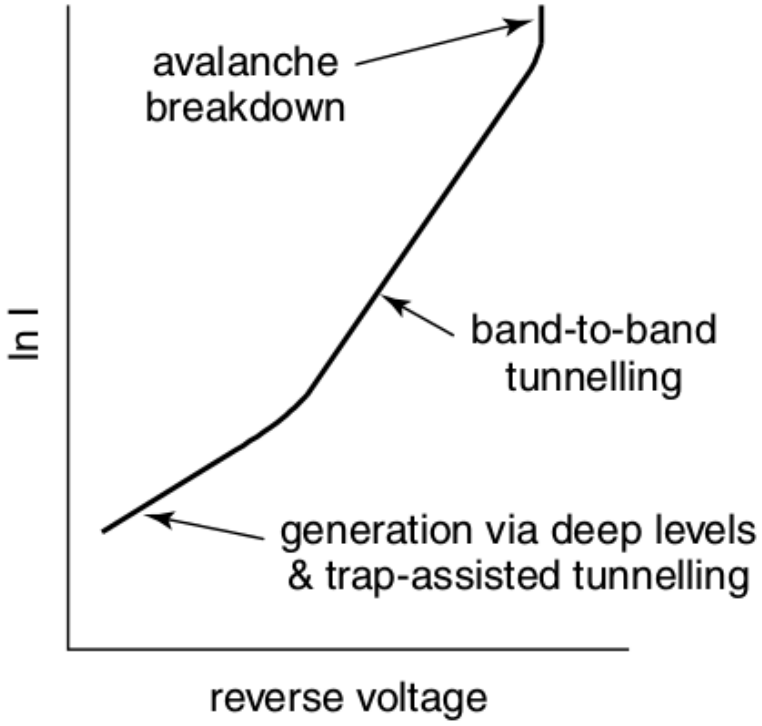

Figure 3.4 : An illustration of different breakdown mechanisms.

3.2.1 Punch-through

The reverse bias voltage of collector-base junction causes the collector-base depletion region to extend into the base and modulate the base width. As the reverse bias voltage gets higher the collector-base depletion region extends further, across the whole width of the base, and merges with the emitter-base depletion region. The event that connects the emitter and collector by a merged depletion region is called

as punch-through. Punch-through allows large current flow between collector and emitter.

3.2.2 Zener breakdown

Zener breakdown is a physical mechanism that allows large number of electrons to move from valence band to conduction band by a tunnelling mechanism due to high electric field and thin energy barrier of the semiconductor. Zener breakdown is most likely to occur in the very heavily doped regions. SiGe HBTs have heavily doped base and emitter regions; therefore zener breakdown is most likely to occur in the reverse bias of emitter-base junction. The tunnelling mechanism could be trap assisted or direct band-to-band tunnelling.

3.2.3 Avalanche breakdown

Avalanche breakdown is the most common breakdown mechanism for SiGe HBTs and probably for all bipolar transistors. Electron-hole pairs are generated in a reverse biased pn junction. These electron-hole pairs move in the opposite directions by the effect of electric field due to reverse bias of pn junction. This is called as leakage current. As the voltage gets higher, the generated carriers gain enough kinetic energy to collide and shatter the silicon-silicon bond. This mechanism is called as impact ionization. After the breakdown voltage, the generated carriers gain enough kinetic energy between collisions and cause a positive feedback by generating more carriers to accelerate and continue the process. This process is called as avalanche multiplication. Avalanche breakdown generates a large number of carriers and therefore enables a large leakage or breakdown current. The doping concentration of the pn junction and the critical electric field that corresponds to this doping concentration sets an upper limit to the reverse bias voltage of the pn junction.

3.3 High Frequency Performance

SiGe HBTs are known for their high frequency performances and they are mostly used in RF integrated circuits. The minority carrier charge that stored in the different regions of the transistor limits high frequency performance. The minority carrier charge has to be removed to turn the transistor off, therefore limiting the maximum frequency of operation for the transistor. The ratio of the stored charge and collector

current is transit time. Forward transit time, τ_F, is defined as transit time of the transistor operating in forward active operation. Forward transit time limits switching speed, hence limits maximum frequency of operation.

3.3.1 Cut-off frequency

Cut-off frequency, f_T, is the frequency that the common emitter current gain of the transistor drops to unity. It is the most important parameter for high frequency operation of SiGe HBTs. SiGe HBTs cannot be used at higher frequencies than cut-off frequency as amplifying or switching devices. Variation of current gain with frequency and cut-off frequency is shown in Figure 3.5.

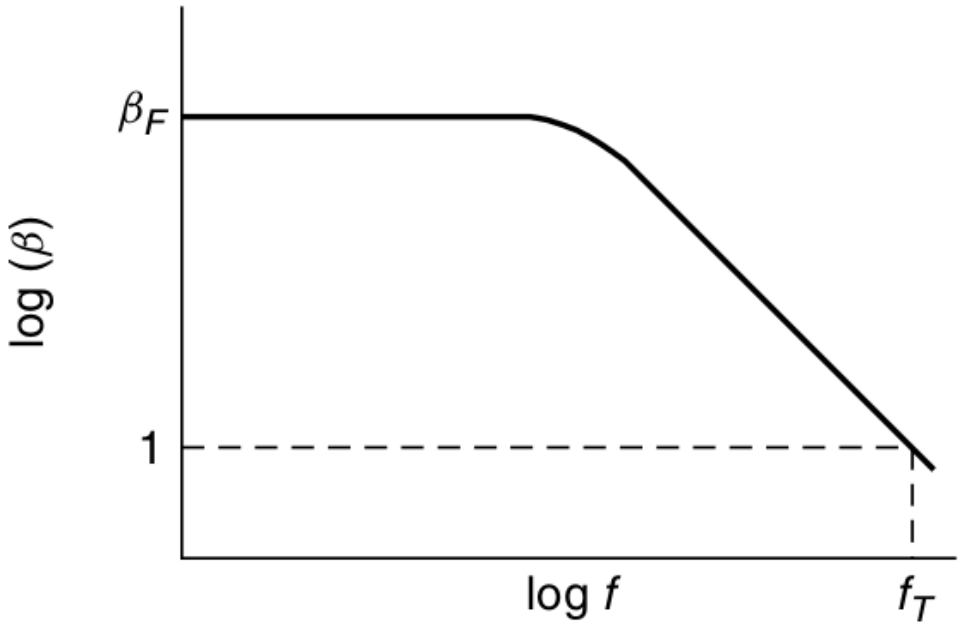

Figure 3.5 : Variation of current gain with frequency and cut-off frequency.

As it can be seen from variation of current gain with frequency, current gain of SiGe HBTs drops gradually as operating frequency approaches to cut-off frequency. It becomes challenging to design RF integrated circuits operating at frequencies close to cut-off frequency.

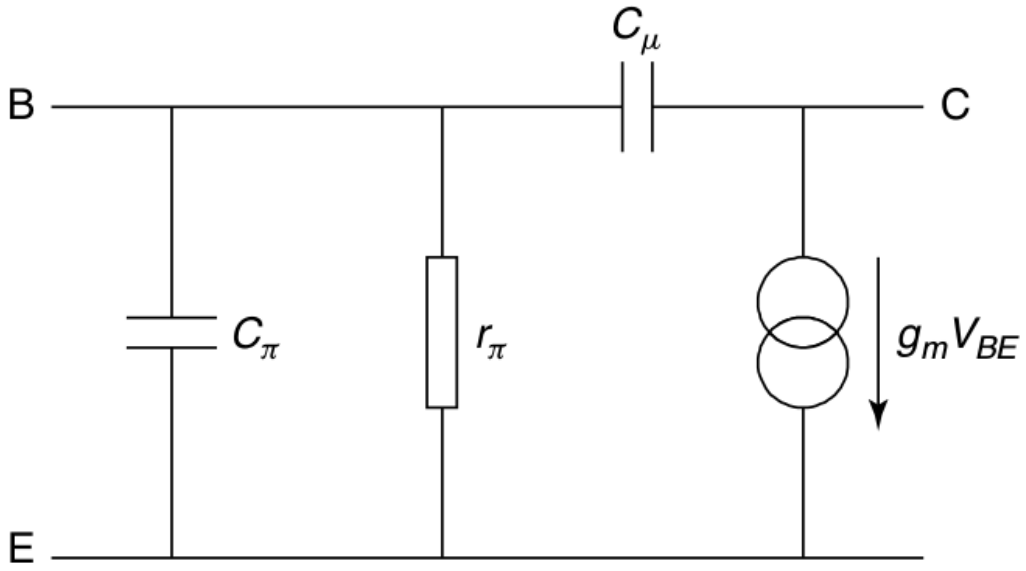

Figure 3.6 : Small signal hybrid-π model of a generic bipolar transistor.

The hybrid-π model of a generic bipolar transistor is shown in Figure 3.6. This small signal model is used to derive an expression for the cut-off frequency. Common emitter configuration is used to derive the cut-off frequency expression. The derivation is not given in this work, however it should be noted that small-signal current equations of base and collector, junction capacitances, RC delay due to series collector resistance is used to derive the expression. The equation for the cut-off frequency is given below.

$$f_T = \frac{1}{2\pi\left(\tau_F + R_C C_{JC} + \frac{kT}{qI_C}\left(C_{JE} + C_{JC}\right)\right)} \quad \textbf{(3.2)}$$

The given equation clearly shows that the cut-off frequency of the SiGe HBT is related to the collector current. The cut-off frequency rises with increasing collector current until depletion capacitance becomes larger than other terms of the equation. As the depletion capacitance term becomes comparable or smaller than forward transit time, the cut-off frequency does not change with increasing collector current. At high collector currents, the effective base width of the transistor increases due to current dependent accumulation of the minority carriers. After a certain collector current, base region expands into collector, degrades forward transit time and therefore cut-off frequency. Variation of the cut-off frequency with collector current can be seen in Figure 3.7.

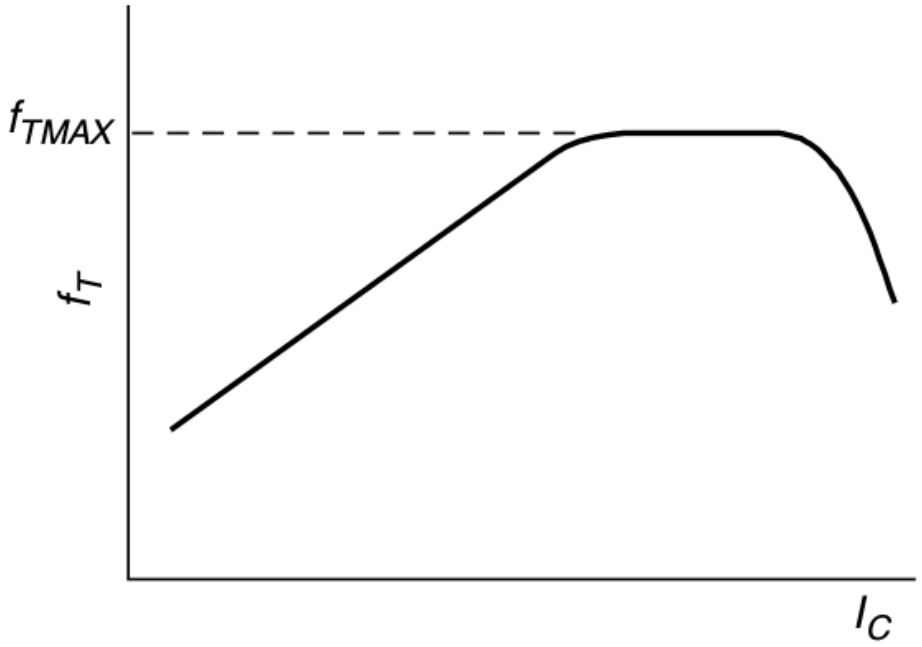

Figure 3.7 : Variation of the cut-off frequency with collector current.

3.3.2 Maximum oscillation frequency

Maximum oscillation frequency, f_{max}, is the frequency that the power gain of SiGe HBT drops to unity. It is another important high frequency parameter for SiGe HBTs and bipolar transistors. Maximum oscillation frequency depends on cut-off frequency, base-collector junction capacitance and base resistance of the transistor. The expression for maximum oscillation frequency is given below.

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{JC} R_B}} \tag{3.3}$$

3.3.3 Base, collector and emitter resistance

Base, collector and emitter of the SiGe HBTs are builded by silicon and silicon-germanium layers with different doping profiles. Different doping profiles mean that series resistance of these terminals varies. Heavily doped emitter shows small resistance, less heavily doped base shows moderate resistance and lightly doped collector shows high resistance. These resistances limit both operation current and frequency. High frequency performance of the transistor is degraded by the combined effect of these parasitic resistances and junction capacitances of the transistor. The effects of base and collector resistances to cut-off and maximum oscillation frequencies are given in earlier sections. Base resistance also degrades the

charging speed of input capacitance and creates a secondary effect on forward transit time of the transistor.

Another degradation caused by parasitic resistance is quasi-saturation. High collector current creates a voltage drop at collector terminal due to collector resistance. If this voltage drop is high enough to forward bias base-collector junction, quasi-saturation occurs. It is usually seen as a soft transition to saturation at low collector-emitter voltages. Variation of collector current for different collector-emitter voltages is given in Figure 3.8, showing quasi-saturation and saturation.

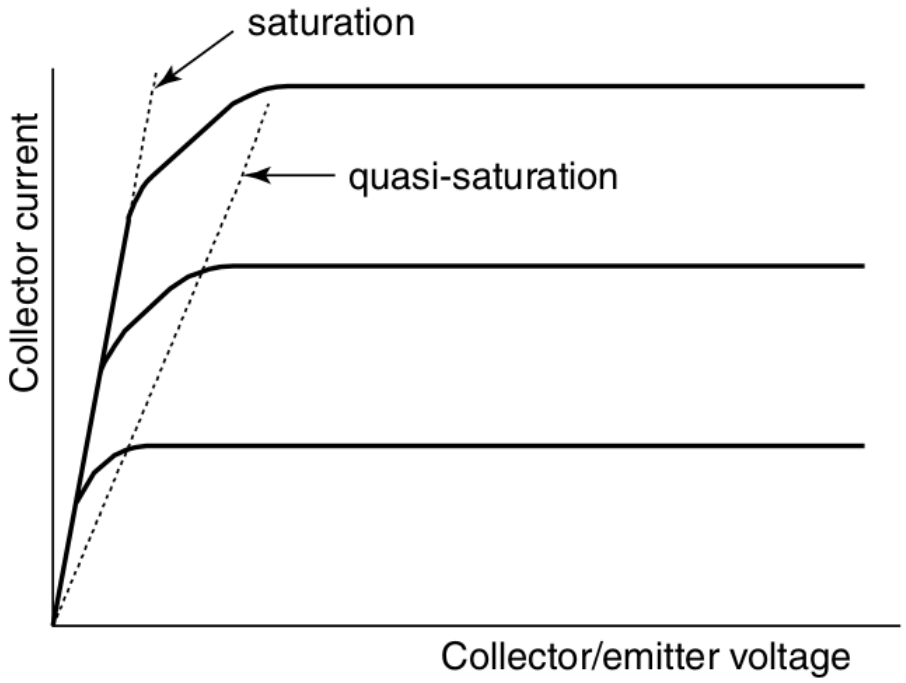

Figure 3.8 : Variation of collector current for different collector-emitter voltages.

3.4 Silicon-Germanium BiCMOS Process

Digital integrated circuit design is dominated by CMOS technology. CMOS technology offers many advantages like low power, small area and ease of design. However, high frequency performance of MOS transistors is limited. SiGe HBTs offer better high frequency performance than their CMOS counterparts. High transconductance of SiGe HBTs also allows these transistors to have higher gain, lower noise and larger drive capability than MOS transistors [2]. SiGe HBTs and MOS transistors can be produced on a single chip by BiCMOS processes.

BiCMOS processes offer many benefits to analogue and mixed-signal designs. SiGe HBTs and MOS transistors can be employed to the best of their abilities to provide

a better overall performance. Digital circuits such as processors, memories and analogue/mixed signal circuits such as data converters, amplifiers, mixers, oscillators can be integrated on a single chip to build a complex system.

The development of the BiCMOS technology started with success of N-well, self-aligned silicon gate CMOS processes. Since N-well was a good candidate to build the collector of the bipolar transistor, integration of MOS transistors and NPN bipolar transistors became possible. Cross-sectional view of a generic BiCMOS process can be seen in Figure 3.9.

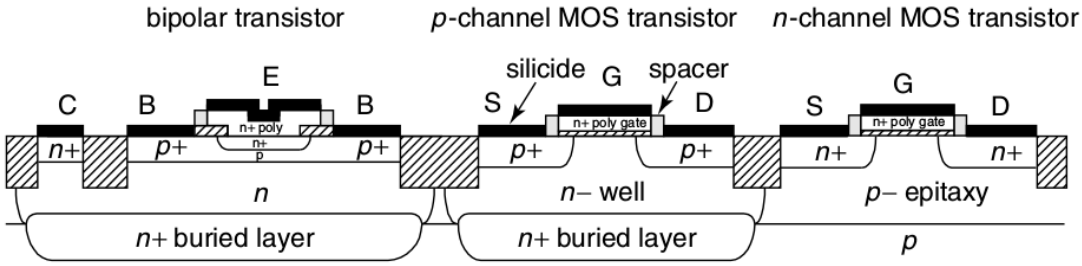

Figure 3.9 : Cross-sectional view of a generic BiCMOS process.

The use of buried layer and epitaxy reduced collector resistance, allowed better current drive and high frequency performance of the bipolar transistors. The buried layer also reduced the gain of the parasitic PNP bipolar and gave MOS transistors robustness against parasitic effects such as latch-up.

MOS transistors and SiGe HBTs might share process steps depending on the technology. p+ source and drain implant of the PMOS could be used to connect SiGe base to terminal. Similarly, n+ source and drain implant of the NMOS could be used to build collector contact. Polysilicon gate also could be used to build polysilicon emitter. Polysilicon emitter layer must be builded before gate oxide growth to ensure connection. These shared process steps reduce both cost and time to market span of BiCMOS integrated circuits [12]. BiCMOS processes usually include many metal layers with additional thick metal layers to provide ease for digital circuit interconnections and to enable building of passive RF elements such as inductor, transmission lines and transformers.

4. AN X-BAND SIGE DRIVER AMPLIFIER

Driver amplifier is an essential part of transmitter chain. Many RF systems require high output power to operate over a long range. These high output power levels are provided by RF power amplifiers. Any power amplifier with gain around 20 dB and output power around 2 watts requires high input power to drive the antenna with maximum output power. Many power amplifiers also require precise source impedance to ensure stability and efficiency. Driver amplifiers employed in such conditions.

4.1 Amplifier Design

This section presents a SiGe driver amplifier to be used as a building block for an X-Band transceiver module. The amplifier utilizes push-pull architecture with input/output transformers providing single-ended to differential signal conversion and input/output impedance matching. Push-pull architecture is known for its good second harmonic suppression and robustness against parasitics. Push-pull configuration requires differential input signals to operate properly. Integrated transformers have been used as baluns at X-Band amplifiers [13-15]. Similarly, the driver amplifier uses two integrated transformers which are utilized as input and output baluns. The circuit diagram of the driver amplifier is given in Figure 4.1.

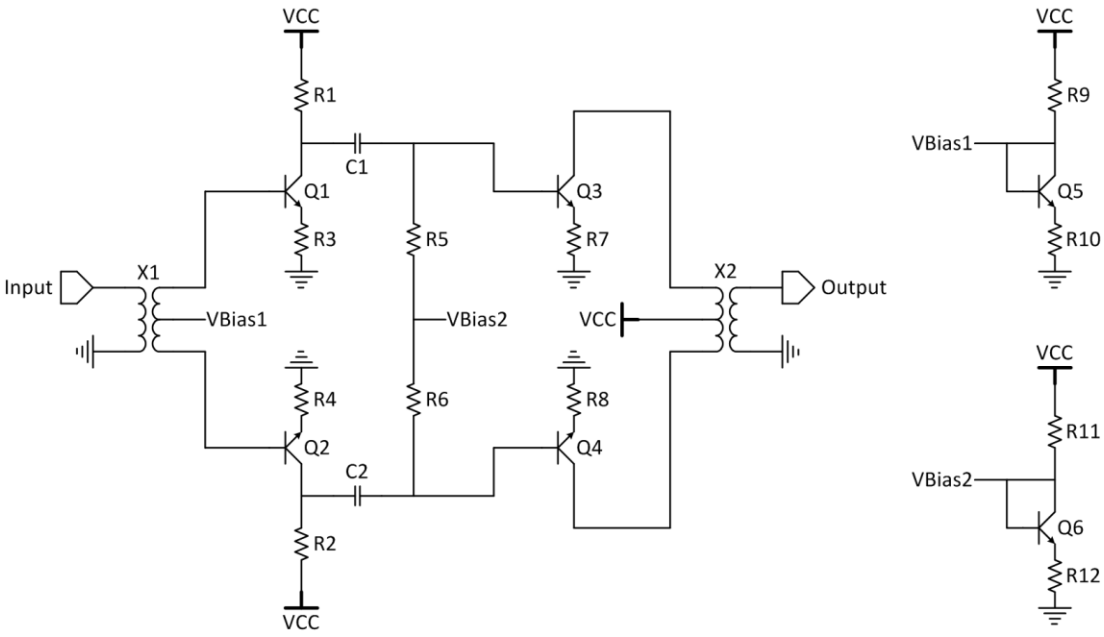

Figure 4.1 : The circuit diagram of the amplifier.

4.1.1 Technology

In this work, Innovations for High Performance Microelectronics 0.25-µm SiGe BiCMOS process is used. This process offers three different types of SiGe HBTs with different cut-off frequencies and breakdown voltages. The first stage employs the high performance transistors with peak transition frequency, f_T=110 GHz and maximum oscillation frequency, f_{max}=180 GHz. The collector-emitter breakdown voltage of the high performance transistor is 2.3 V. Second stage is designed using the medium voltage transistors with peak f_T=45 GHz and f_{max}=140 GHz. The collector-emitter breakdown voltage of the medium voltage transistor is 5 V [16]. The common-emitter current gain of both transistors is 150. Passive devices such as poly resistors and metal-insulator-metal capacitors are available in the process. This technology also offers five metal layers, top two metal layers being thick metal layers to build passive elements such as inductors, transmission lines, transformers, etc.

4.1.2 Input and output transformers

The two uppermost thick metal layers are used to build X1 and X2 transformers. Input transformer X1 provides single-ended to differential conversion of the input signal and the impedance matching. Similarly, output transformer X2 provides

differential to single-ended conversion of the output signal and the impedance matching. 3D view of the transformer can be seen in Figure 4.2.

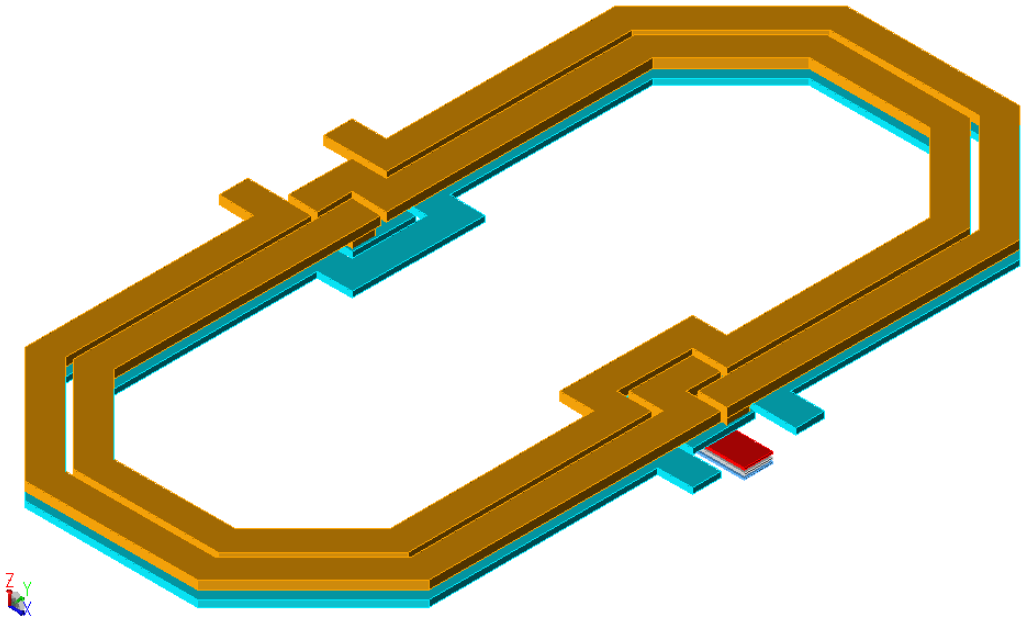

Figure 4.2 : 3D view of the transformer.

X1 and X2 transformers are identical in terms of structure, size and specifications. They have symmetrical structures that allow precise 1:1 turn ratio with minimal disturbance. Electromagnetic simulations are done to characterize the transformer. Momentum engine provided by Advanced Design System is used for electromagnetic simulations. The simulated inductance and quality factor of primary and secondary windings are shown in Figure 4.3.

The input capacitance of the first stage, the output capacitance of the second stage and the coupling between transformers are used to generate necessary resonances for input and output impedance matching. Bondwire inductances and pad capacitances are also taken into account. Simulated insertion loss of both transformers is below 1.5 dB and it is affected by the insulator thickness between the two uppermost metal layers. The structure of the transformer allows primary and secondary windings to be coupled with both top-down and side-by-side proximity. The simulated coupling coefficent of the transformer is given in Figure 4.4.

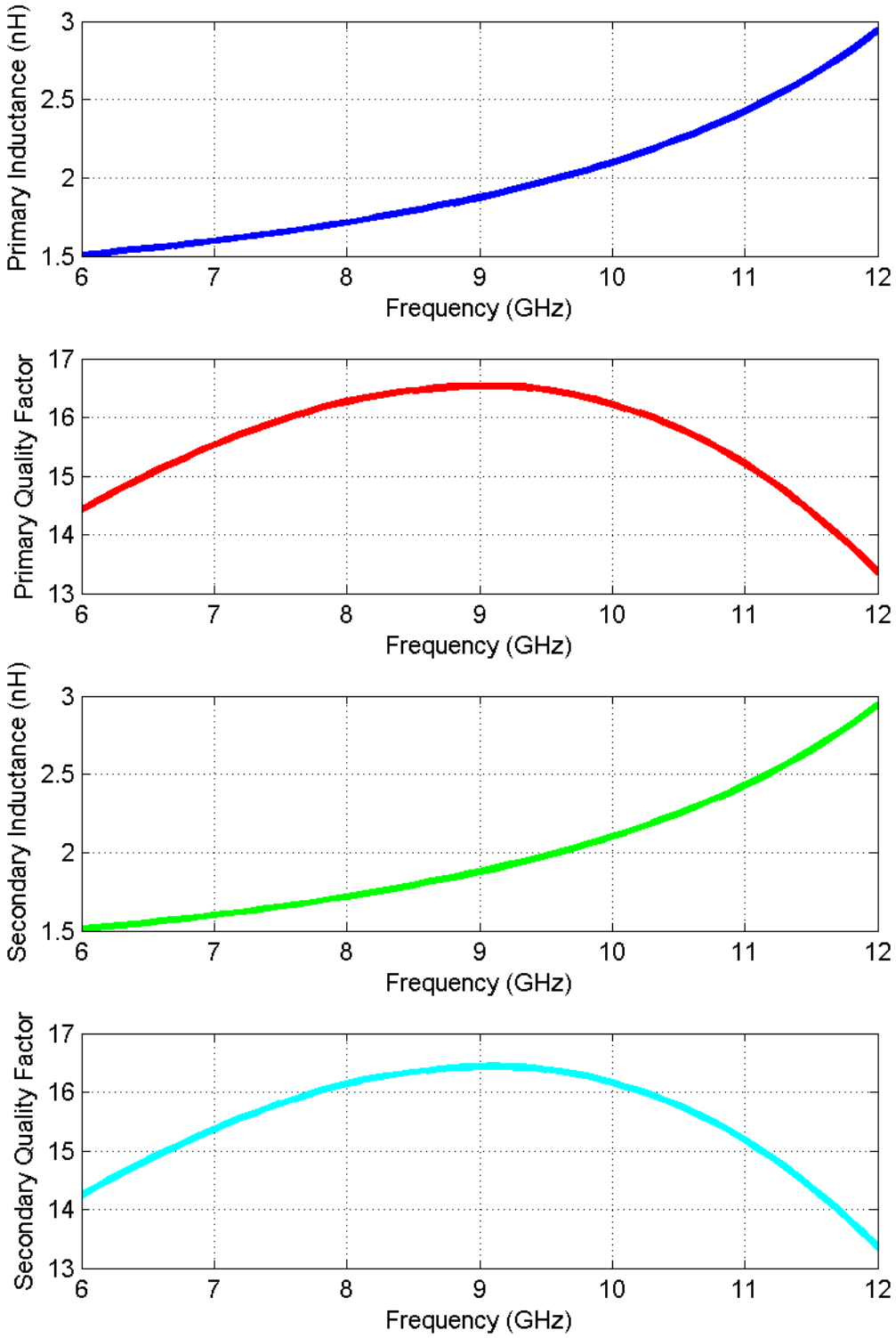

Figure 4.3 : The inductance and quality factor of primary and secondary windings.

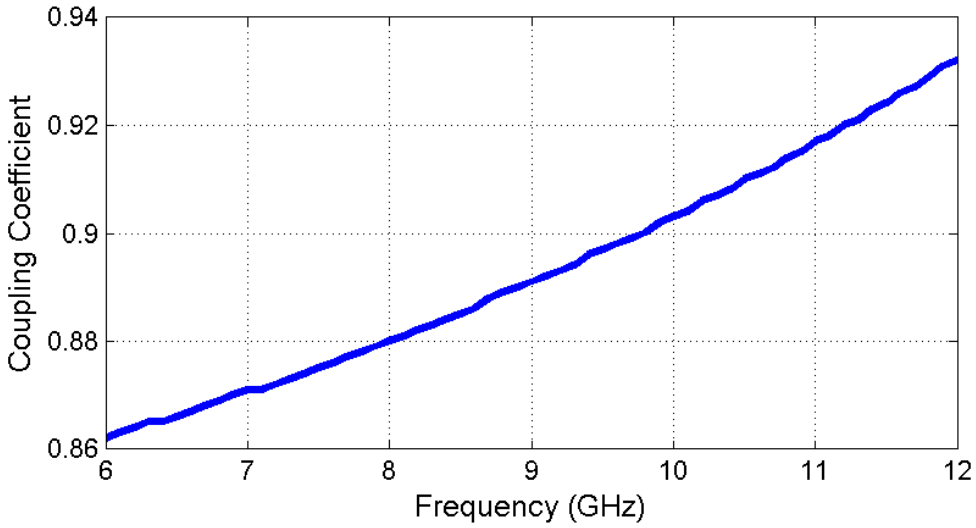

Figure 4.4 : The coupling coefficent of the transformer.

4.1.3 Circuit design

The circuit diagram in Figure 4.1 shows that the driver amplifier consists of two stages. Both stages utilize common emitter configuration. First stage is designed using high performance SiGe transistors, Q1 and Q2, with load resistors, R1 and R2. Differential output of the first stage is connected to the second stage via ac-coupling capacitors, C1 and C2. Second stage employs medium voltage SiGe transistors, Q3 and Q4, with inductive load from primary winding of X2. Both stages of the amplifier have emitter degeneration resistances, R3, R4, R7 and R8, to improve linearity, stability and to prevent thermal runaway. Biasing circuits of both stages are simple current mirrors with their corresponding transistors and emitter degeneration resistances. Supply voltage of both stages is 3.3 V. First stage is biased in class-A mode of operation with bias voltage applied to center tap of X1. It draws 32 mA of current. Second stage is biased in class-AB mode of operation with bias voltage applied through resistors, R5 and R6. It draws 16 mA of current. The bias voltages of both stages can be adjusted externally. Decoupling capacitances for bias and supply voltages are not given in circuit diagram for clarity. The layout of the amplifier is given in Figure 4.5.

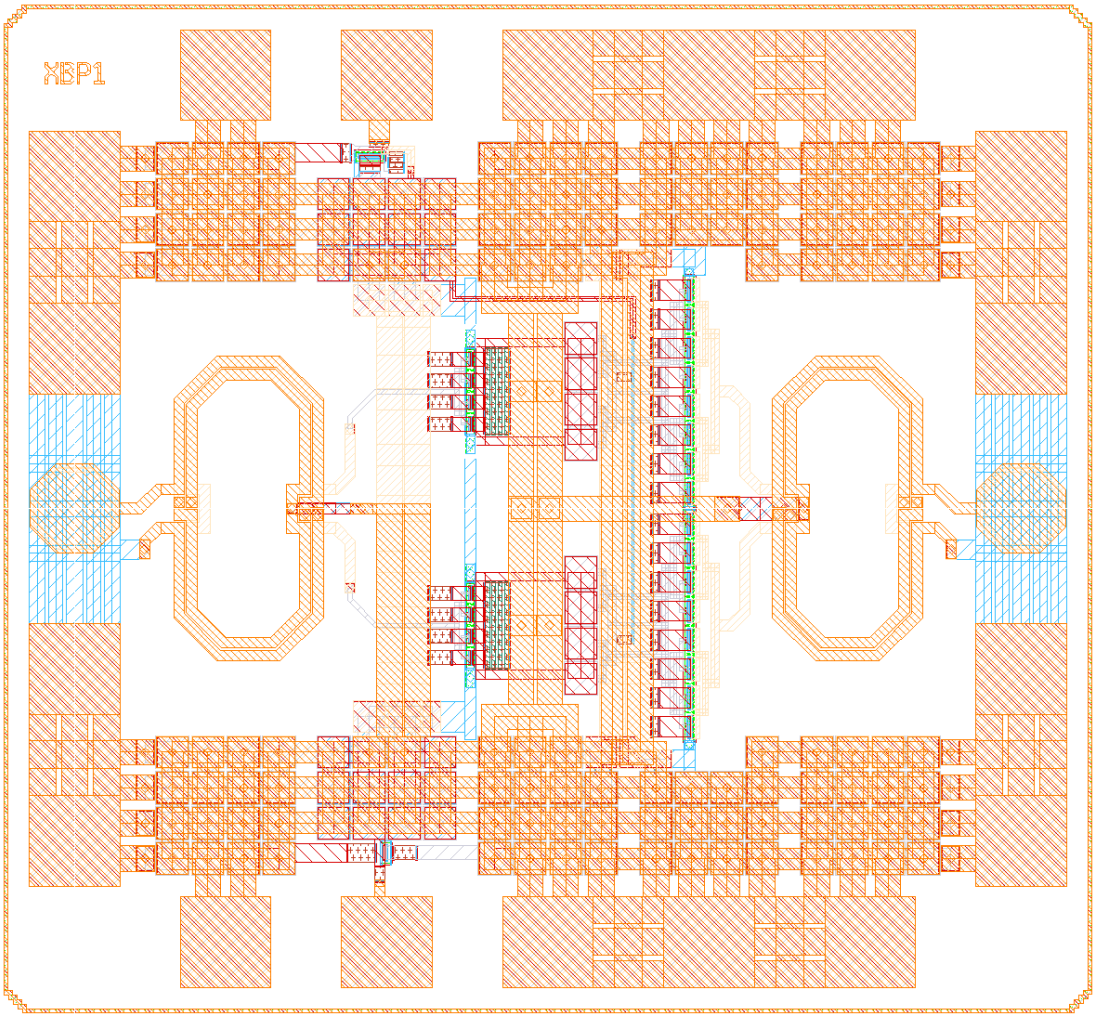

Figure 4.5 : The layout of the amplifier.

4.1.4 Simulation results

The circuit is designed and simulated in Advanced Design System. Large signal S parameter simulation is performed to observe input return loss, output return loss, gain and reverse isolation of the amplifier. S parameter simulation results are given in Figure 4.6. Stability factor, K, is also calculated from simulated S parameters and given in Figure 4.7.

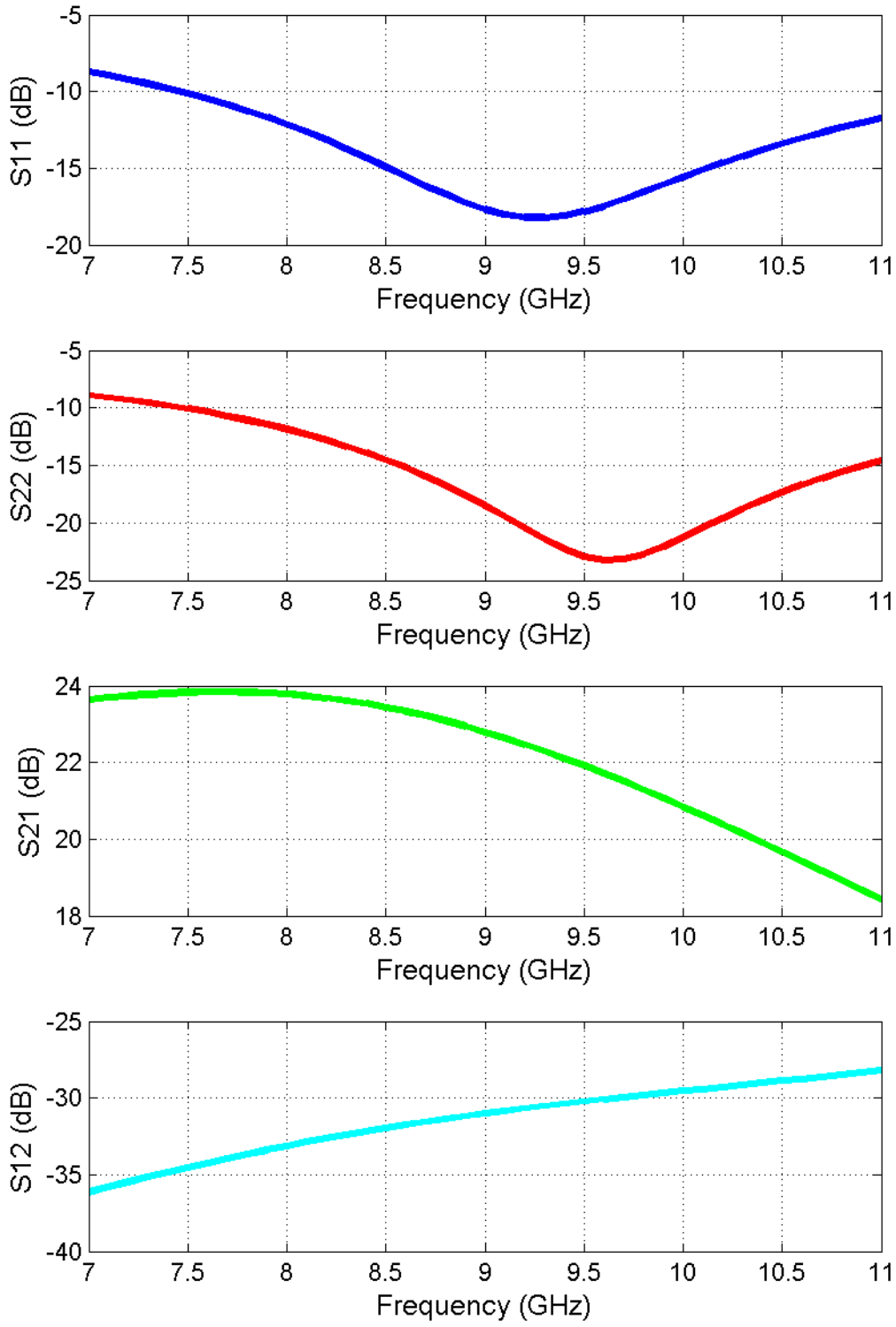

Figure 4.6 : S parameter simulation results of the amplifier.

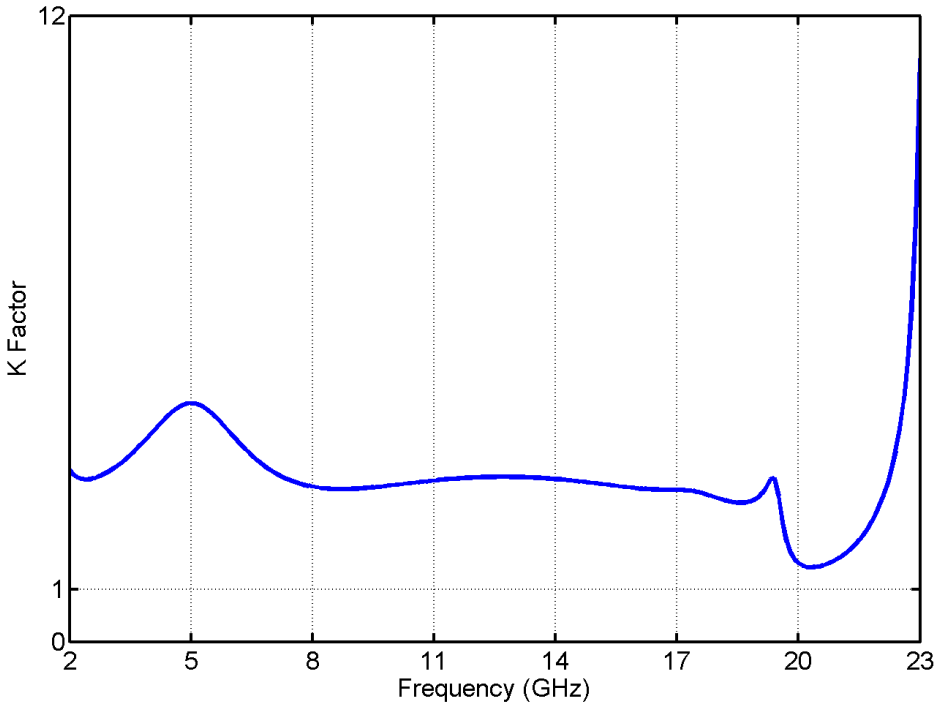

Figure 4.7 : Stability factor of the amplifier.

S parameter simulation shows that amplifier has a maximum gain of 24 dB with 3 dB drop points covering 7-10 GHz band. The input and output return loss of the amplifier is better than 10 dB for 7.5-11 GHz band. Stability factor shows that the amplifier is unconditionally stable.

Harmonic balance simulation is done to observe noise figure, output third order intercept point, output power at 1-dB compression point for different frequencies. It is also repeated to observe power-added efficiency, gain and output power of the amplifier for different input power levels. Noise figure, output third order intercept point and output power at 1-dB compression point of the amplifier is shown in Figure 4.8, Figure 4.9 and Figure 4.10, respectively. Power-added efficiency, gain and output power of the amplifier for different input power levels is given in Figure 4.11.

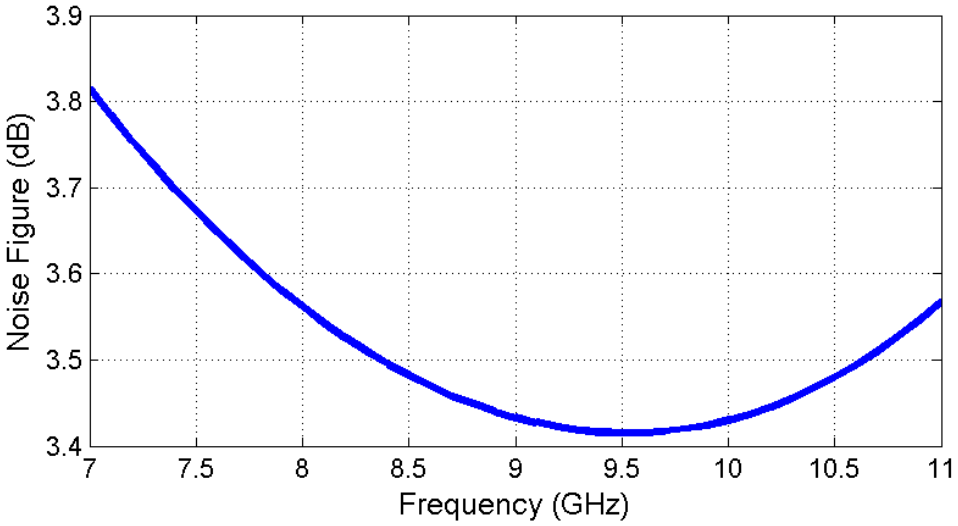

Figure 4.8 : Simulation results showing noise figure of the amplifier.

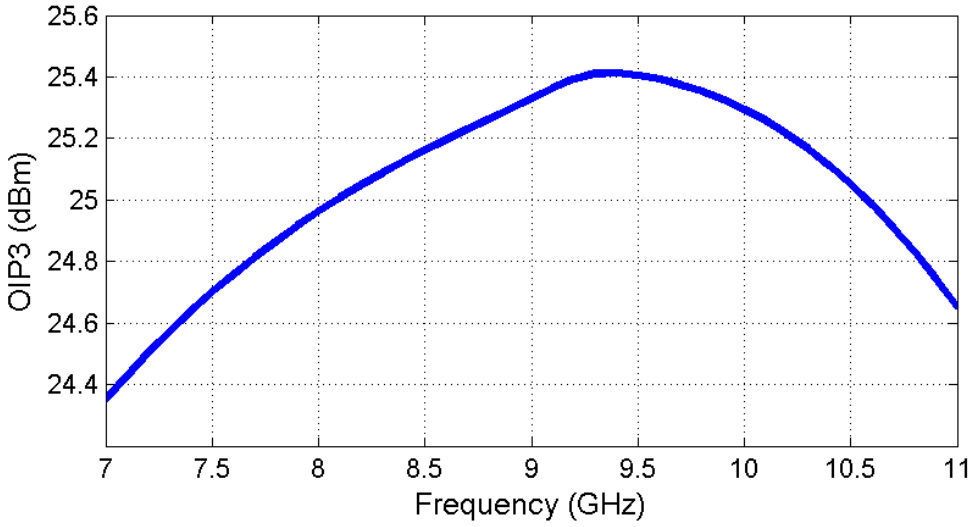

Figure 4.9 : Simulation results showing OIP3 of the amplifier.

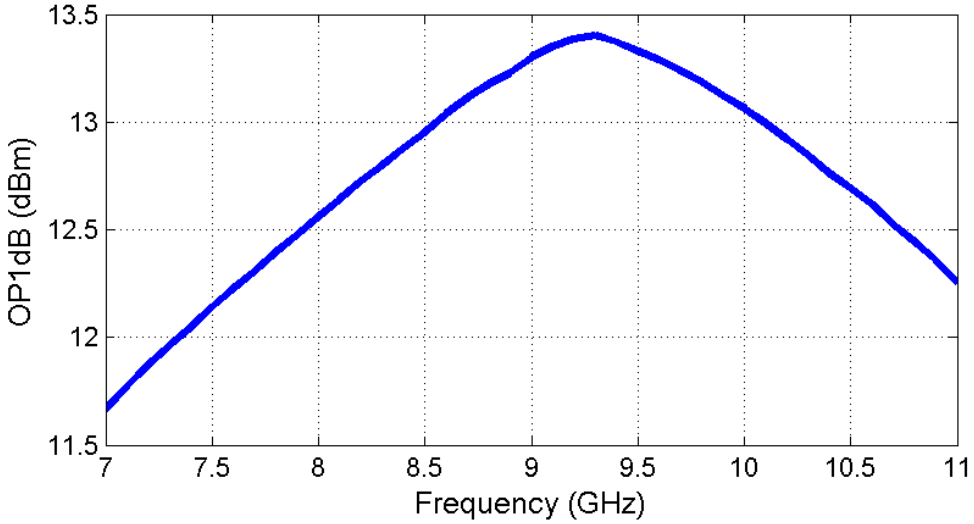

Figure 4.10 : Simulation results showing OP1dB of the amplifier.

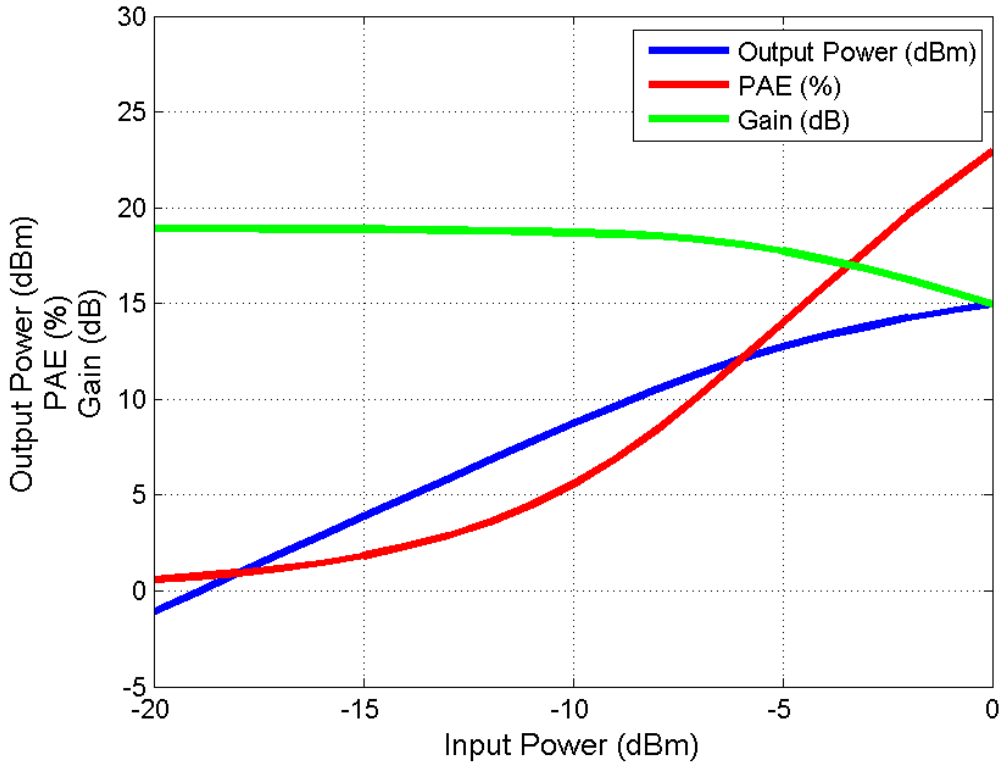

Figure 4.11 : Simulation results showing PAE, gain and output power of the amplifier for different input power levels.

The amplifier shows below 4 dB noise figure for 7-11 GHz band. Output third order intercept point and the output power at 1-dB compression point of the amplifier is above 24 dBm and 12 dBm respectively for the same bandwidth. Power added efficiency of the amplifier is over 14% at 1-dB compression point and it is over 24% at saturation for an input signal at 10 GHz.

4.1.5 Measurement results

Figure 4.12 shows the die photo of the manufactured driver amplifier. The die area is 1×1 mm^2 and the size of the amplifier core without pads is 0.8×0.8 mm^2. The test module size is 58×25 mm^2 including RF connectors. Input and output of the test module are connected to the amplifier via 50-Ω conductor-backed coplanar waveguides. No external components are used for the input and the output impedance matching. Thin-film capacitors are placed near the amplifier die for decoupling purposes. The test module is shown in Figure 4.13.

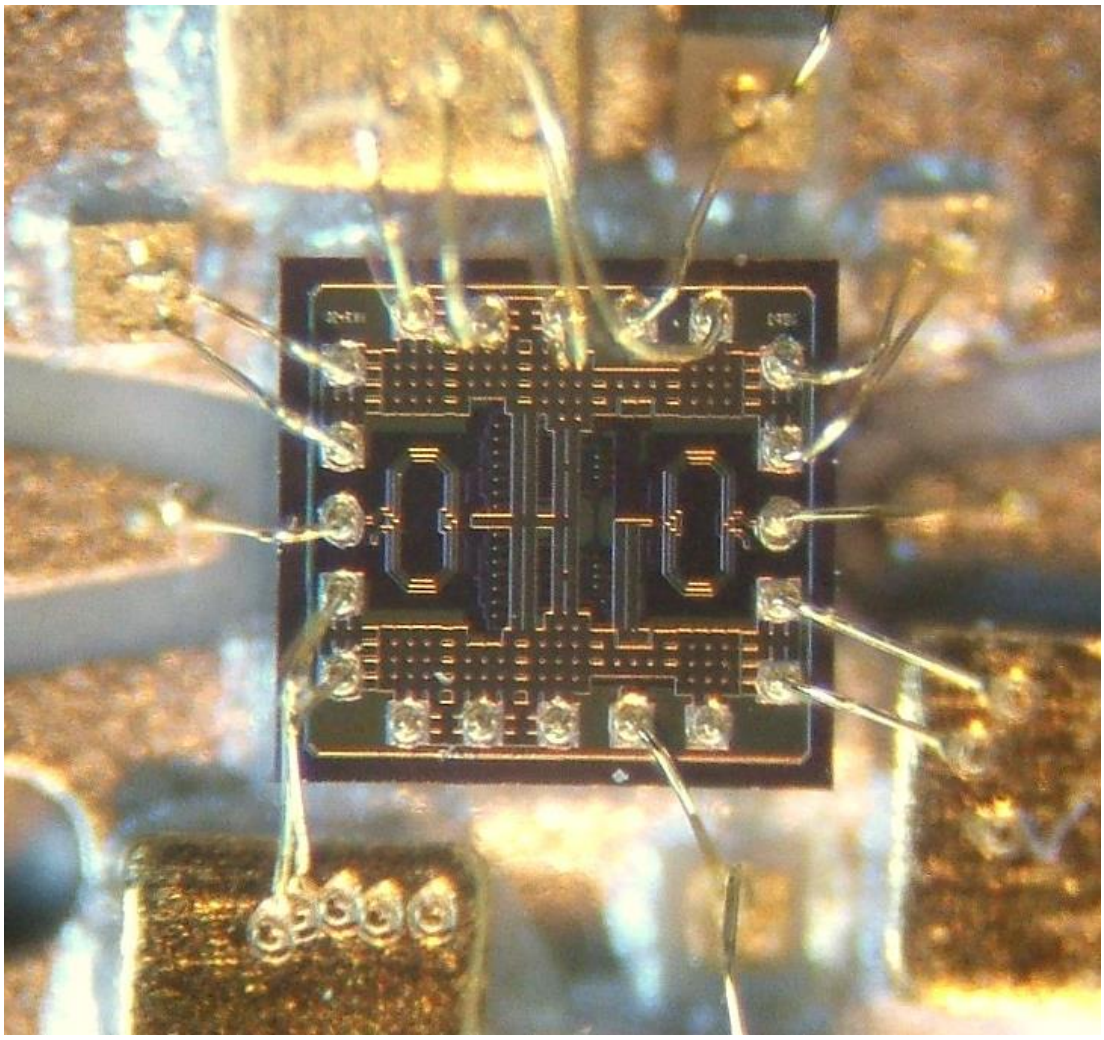

Figure 4.12 : Die photo of the amplifier.

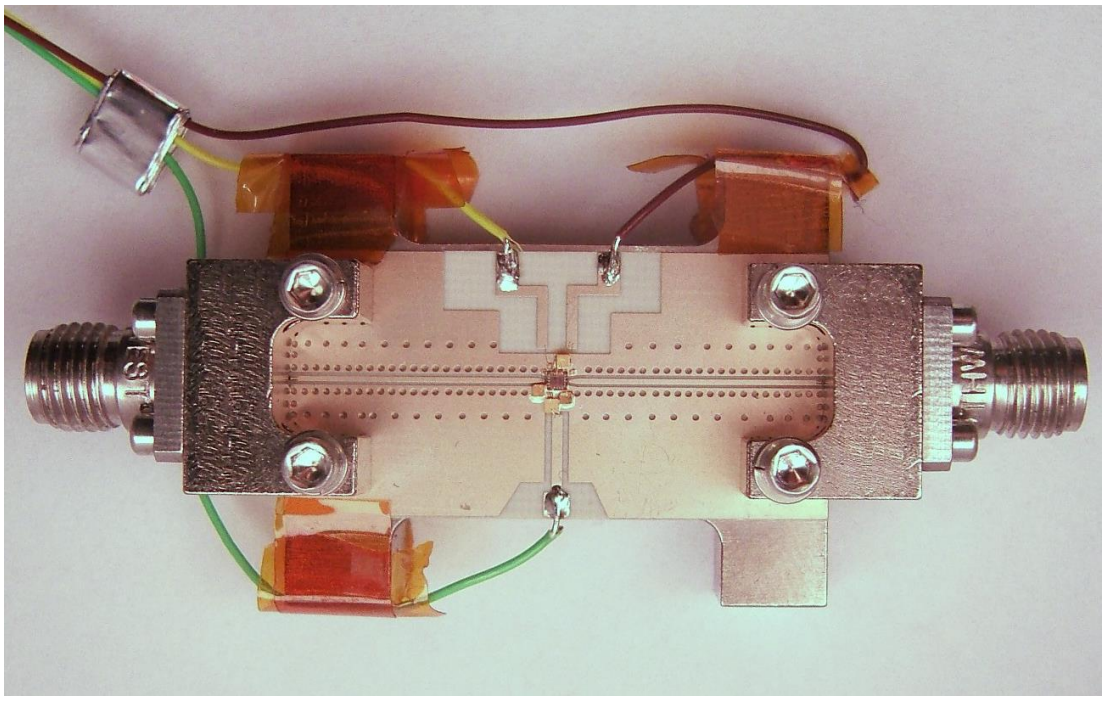

Figure 4.13 : Test module of the amplifier.

Measurements of the amplifier are done in ITU VLSI Labs. It should be noted that all given results are from calibrated measurements without cable and equipment losses. S parameter measurement setup can be seen in Figure 4.14. Photograph of the S parameter measurement setup is shown in Figure 4.15 to give general idea of the measurement environment.

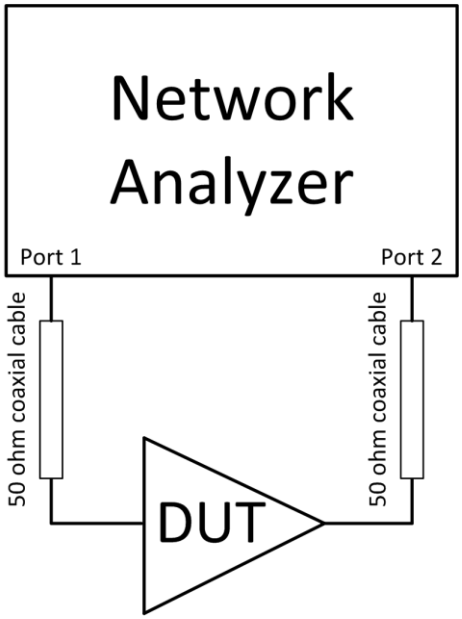

Figure 4.14 : S parameter measurement setup.

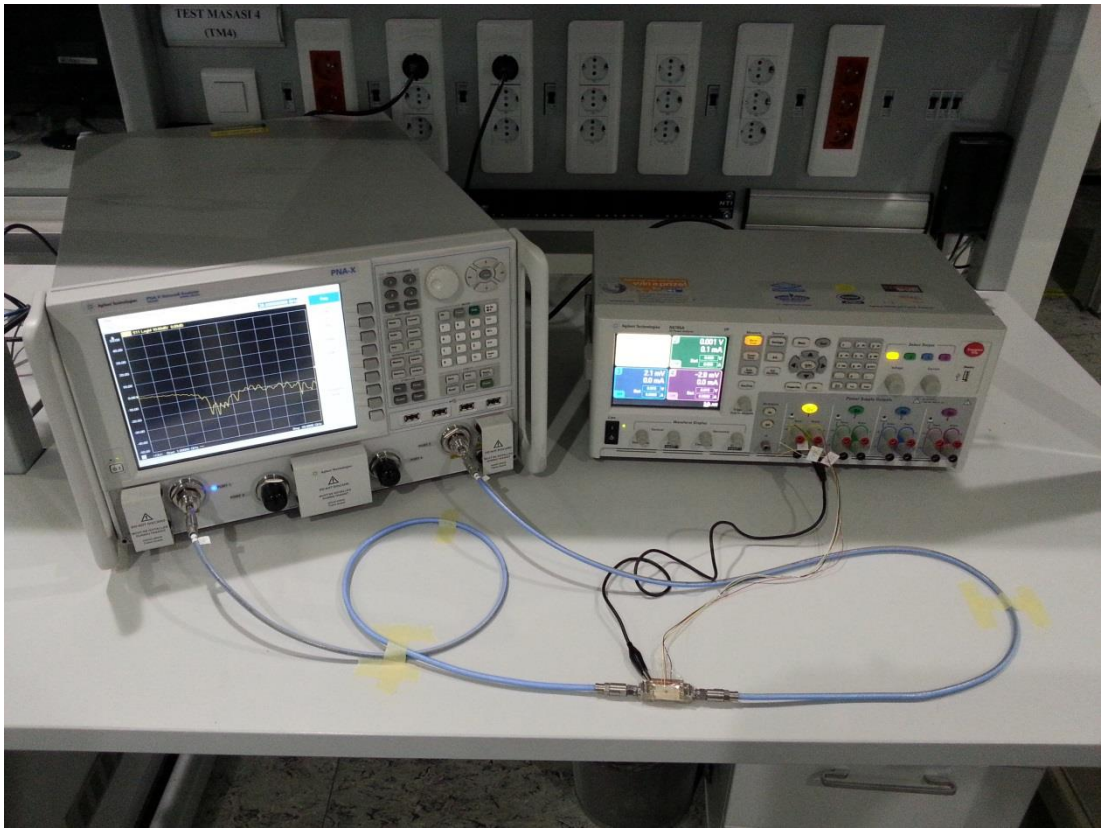

Figure 4.15 : Photograph of the S parameter measurement setup.

S parameter measurement results of the driver amplifier are given in Figure 4.16. The maximum gain of the amplifier is 22 dB at 7.8 GHz with 3-dB drop points covering 7-10 GHz band. The plot also shows better than 10 dB input and output return loss for the 8-10 GHz band.

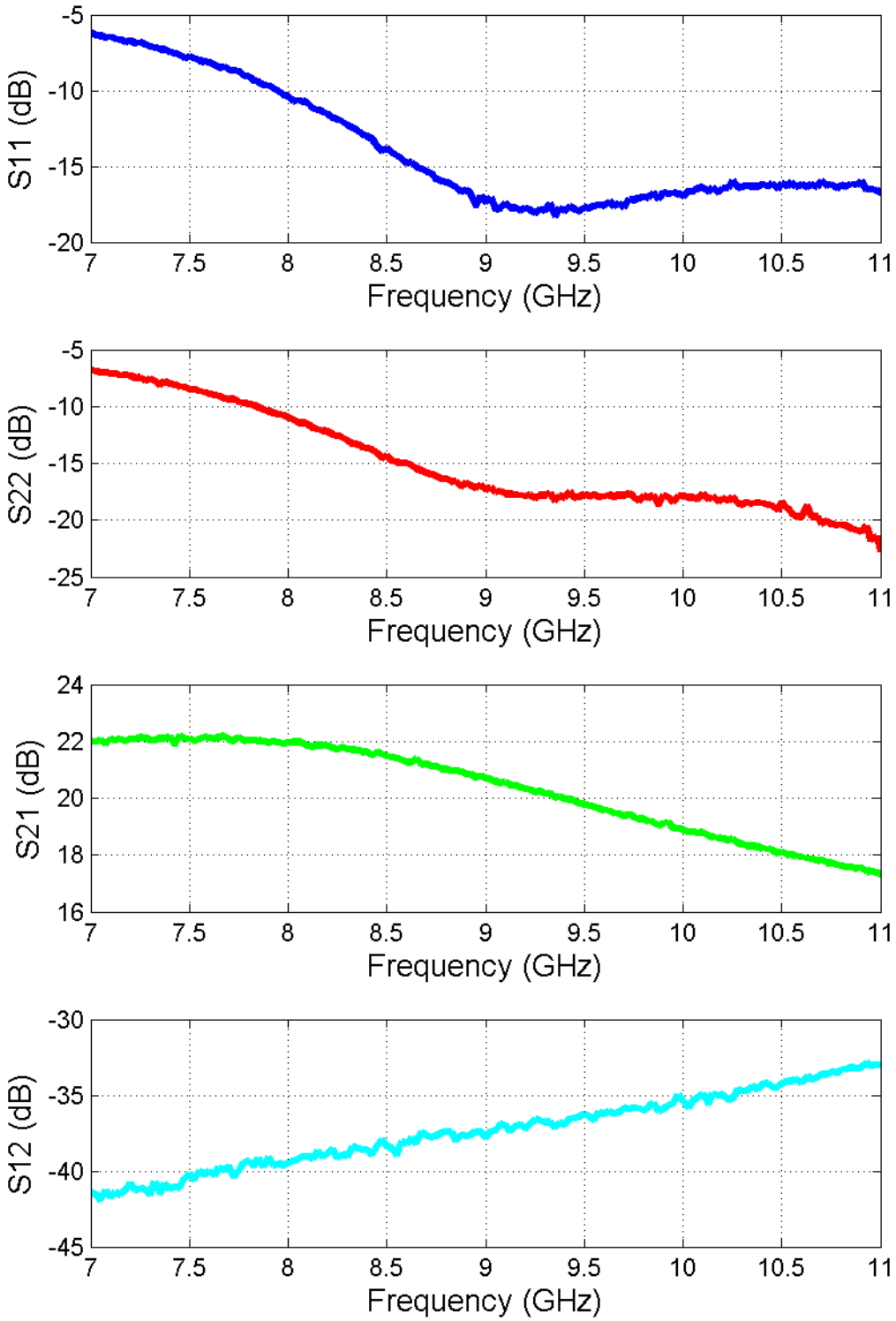

Figure 4.16 : S parameter measurement results.

Noise figure measurement setup is given in Figure 4.17. It should be noted that ambient temperature and interferers present in the measurement environment could affect noise figure result, especially for low noise devices.

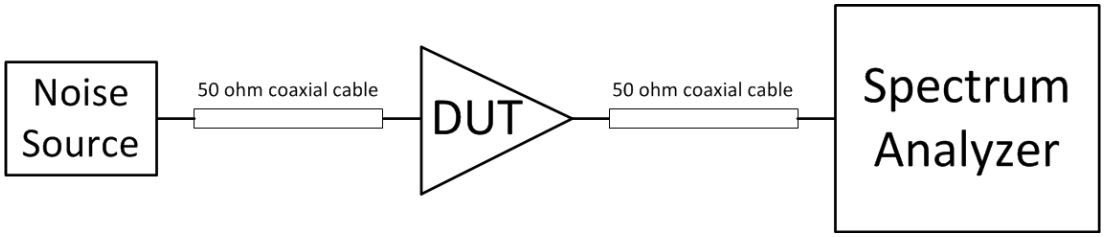

Figure 4.17 : Noise figure measurement setup.

Noise figure measurement result of the amplifier is shown in Figure 4.18. The noise figure of the amplifier is below 5 dB for 7-11 GHz band.

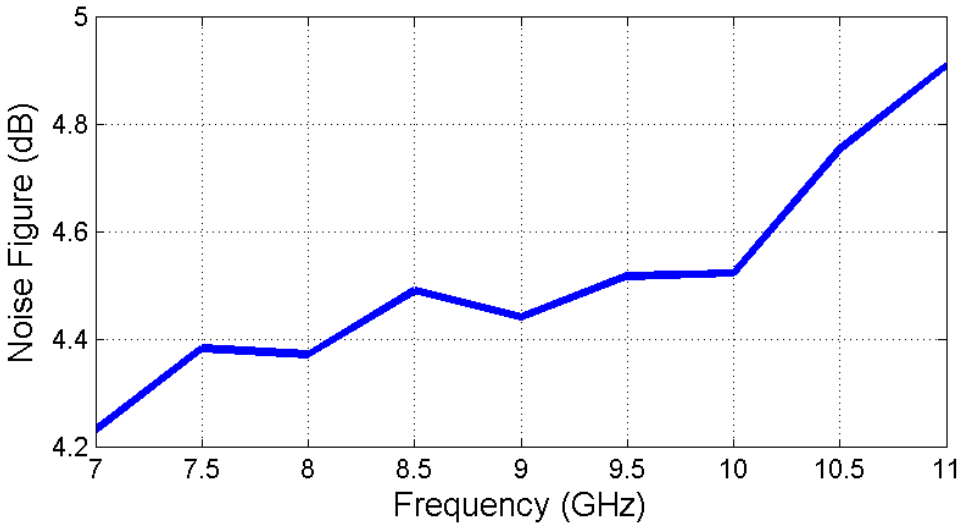

Figure 4.18 : Noise figure measurement results.

One tone measurements are done to observe overall harmonic performance and output power for different frequencies and input power levels. One tone measurement setup can be seen in Figure 4.19.

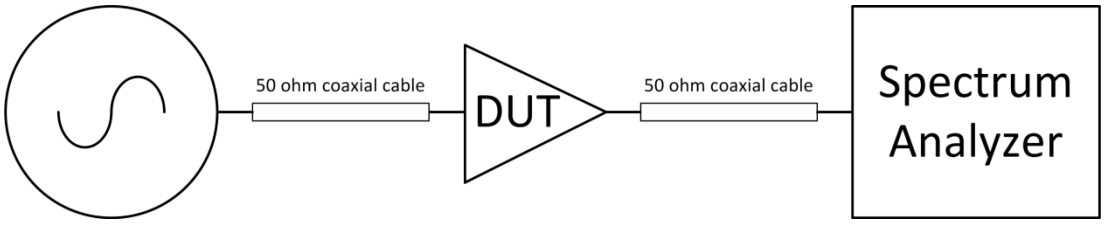

Figure 4.19 : One tone measurement setup.

Output power of the amplifier at 1-dB compression point over the 7-11 GHz band can be seen in Figure 4.20. The amplifier achieves a maximum output power of

14 dBm at 1-dB compression point. Figure 4.21 shows the power-added efficiency, gain, and output power of the amplifier versus increasing input power at 10 GHz. The driver amplifier achieves a power-added efficiency of 11% at 1-dB compression point, increasing to a maximum of 17% at saturation.

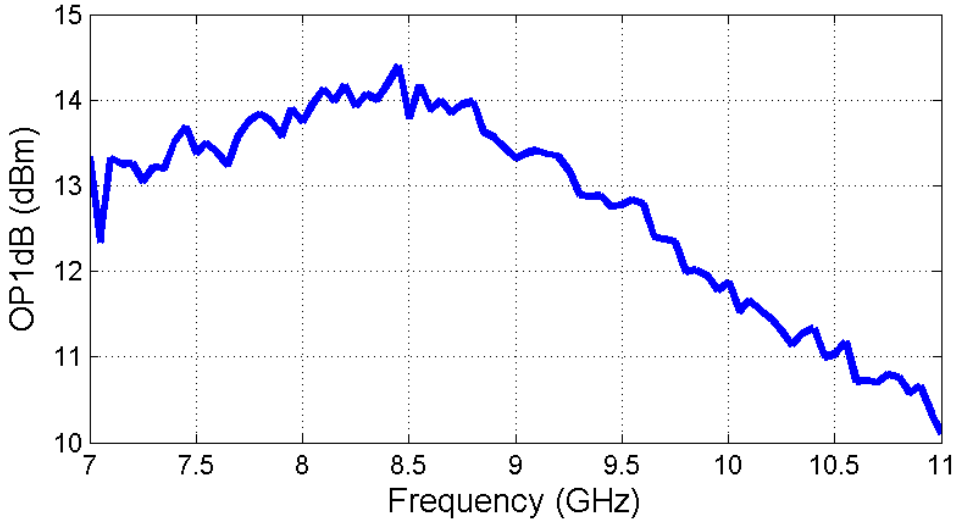

Figure 4.20 : Measurement results showing OP1dB results for 7-11 GHz band.

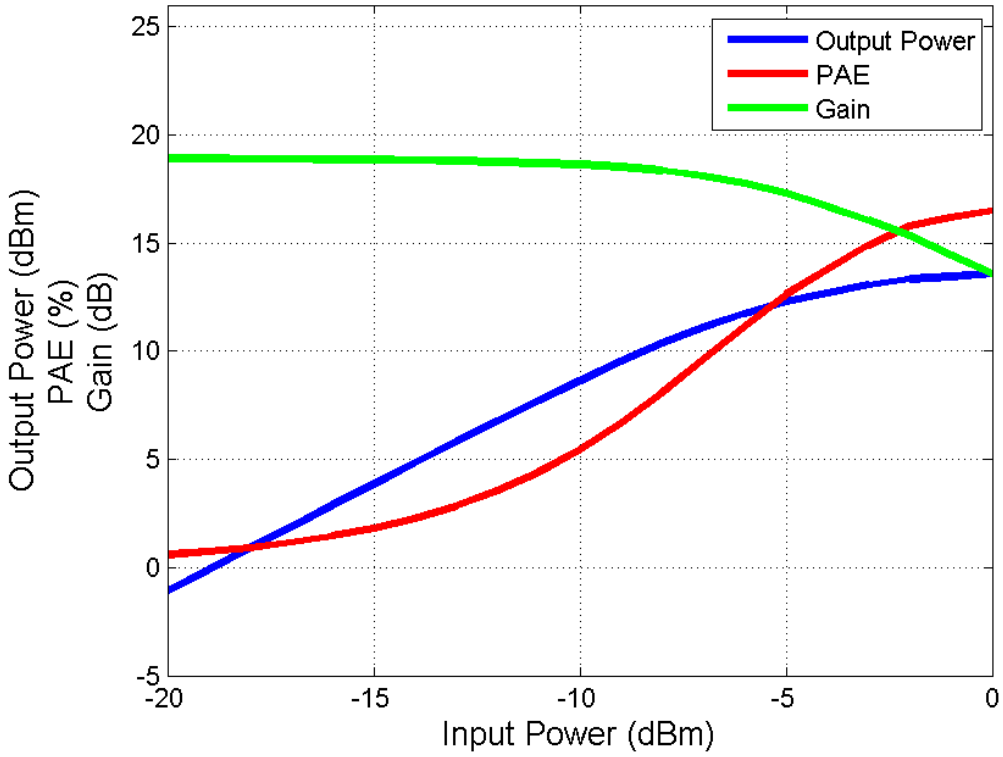

Figure 4.21 : Measurement results showing PAE, gain and output power with increasing input power at 10 GHz.

Two tone measurements are done to observe intermodulation products and third order intercept point of the amplifier. Two tone measurement setup can be seen in Figure 4.22.

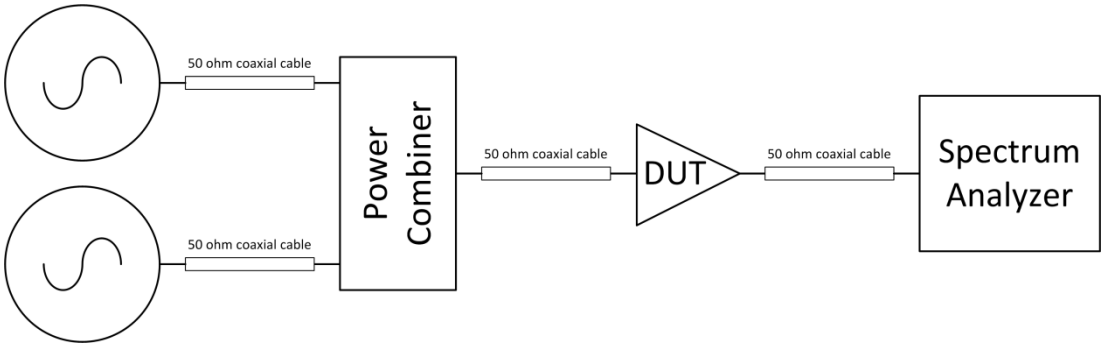

Figure 4.22 : Two tone measurement setup.

Measured third order intercept point of the amplifier for 7-11 GHz band is given in Figure 4.23. It can be seen that the amplifier shows a maximum 24 dBm output third order intercept point performance.

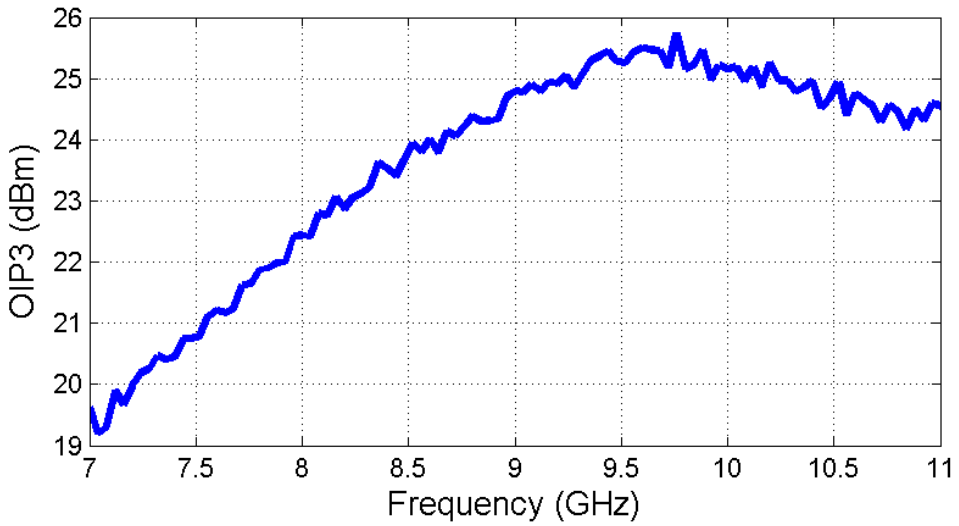

Figure 4.23 : Measurement results showing OIP3 for 7-11 GHz band.

4.2 Amplifier Design Second Iteration

The measurements of the first amplifier showed inferior results from the simulations in terms of both gain and linearity. Modelling of the medium voltage transistors in the second stage is found to be inaccurate for high current levels. The input impedance of the second stage also could be lower than initially thought due to high current of the second stage. Second iteration of the amplifier is designed with these observations from first iteration.

The second amplifier also utilizes push-pull architecture with input/output transformers providing single-ended to differential signal conversion and input/output impedance matching. The first stage changed to a common emitter stage cascoded by an NMOS transistor. Interstage impedance matching is added to increase gain and linearity performance of the first stage. The circuit diagram of the second driver amplifier is given in Figure 4.24.

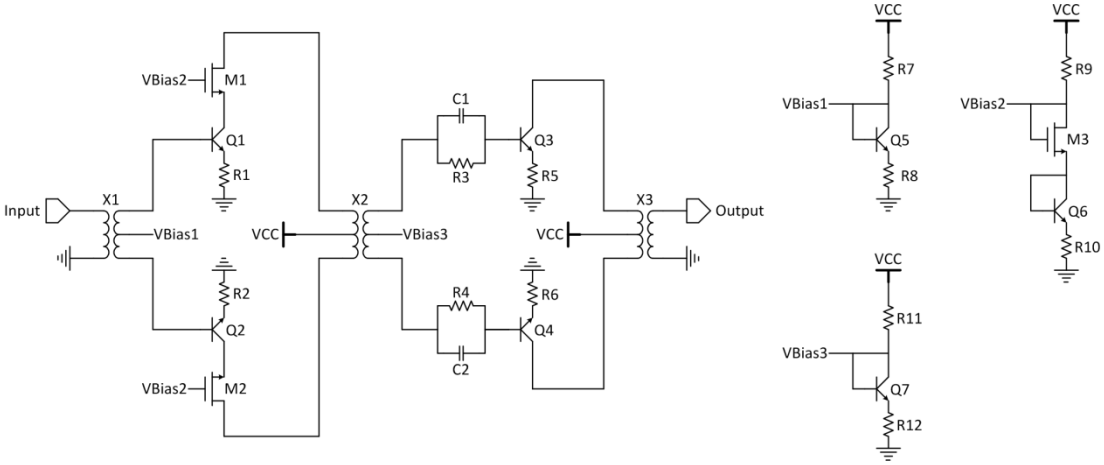

Figure 4.24 : The circuit diagram of the second amplifier.

4.2.1 Interstage impedance matching transformer

The interstage impedance matching transformer X2 is identical to input and output transformers. Initial simulations of the second amplifier with ideal elements indicated that a transformer with 1:2 turn ratio could be better for interstage impedance matching. However, electromagnetic simulations showed that high coupling factor, symmetrical design and low insertion loss of the initial transformer outweighs the benefit of other 1:2 transformer builds. All transformers of the second amplifier are scaled according to changes in transistor sizes and configurations.

4.2.2 Circuit design

The circuit diagram in Figure 4.24 shows that the second driver amplifier consists of two stages. Both stages utilize common emitter configuration. First stage is designed using high performance SiGe transistors, Q1 and Q2, cascoded by NMOS transistors, M1 and M2, with inductive load from X2. A high pass network consists of resistances, R3, R4, and capacitances C1, C2, is placed to input of second stage to stabilize the amplifier. Second stage employs medium voltage transistors, Q3 and Q4, with inductive load from primary winding of X3. Both stages of the amplifier

have emitter degeneration resistances, R1, R2, R5 and R6, to improve linearity, stability and to prevent thermal runaway. Biasing circuits of both stages are simple current mirrors with their corresponding transistors and emitter degeneration resistances. The sizes of SiGe transistors are reduced for first stage and increased for second stage. Supply voltage of both stages is 3.3 V. First stage is biased in class-A mode of operation with bias voltage applied to center tap of X1. It draws 24 mA of current. Second stage is biased in class-AB mode of operation with bias voltage applied to center tap of X2. It draws 14 mA of current. The bias voltages of both stages can be adjusted externally. Decoupling capacitances for bias and supply voltages are not given in circuit diagram for clarity. The layout of the second amplifier is given in Figure 4.25.

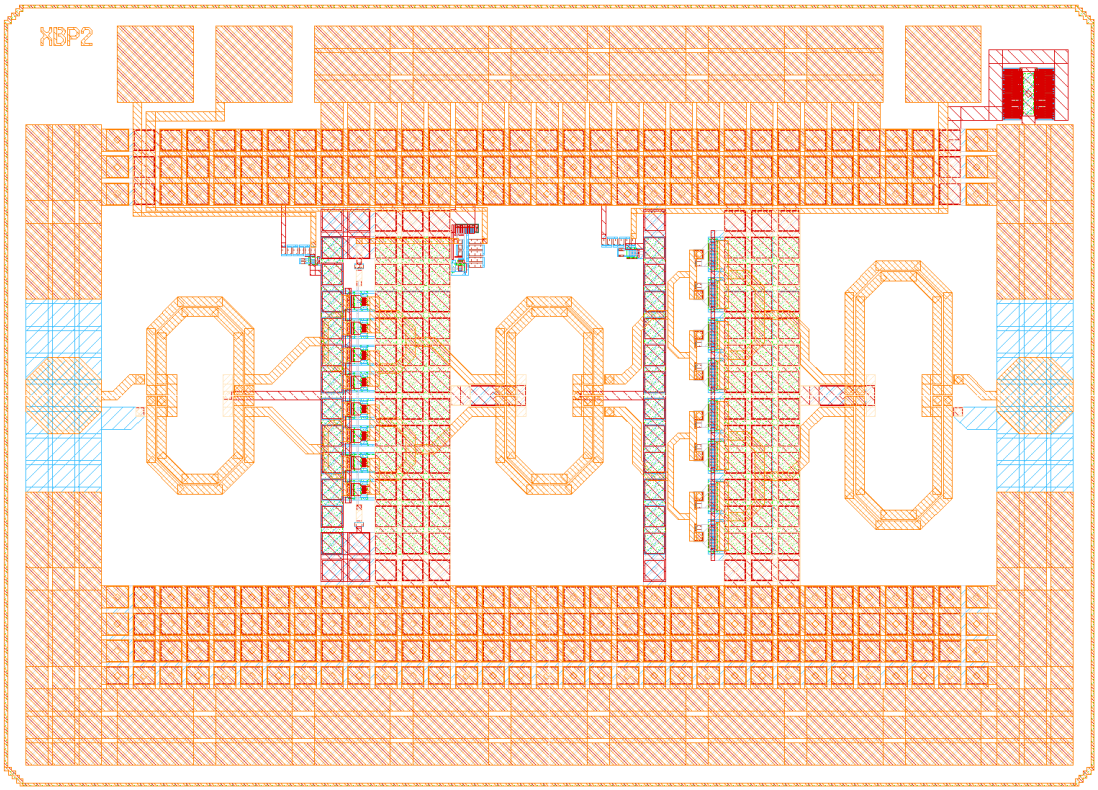

Figure 4.25 : The layout of the second amplifier.

4.2.3 Simulation results

The second circuit is also designed and simulated in Advanced Design System. Large signal S parameter simulation is performed to observe input return loss, output return loss, gain and reverse isolation of the amplifier. S parameter simulation results are given in Figure 4.26. Stability factor, K, is also calculated from simulated S parameters and given in Figure 4.27.

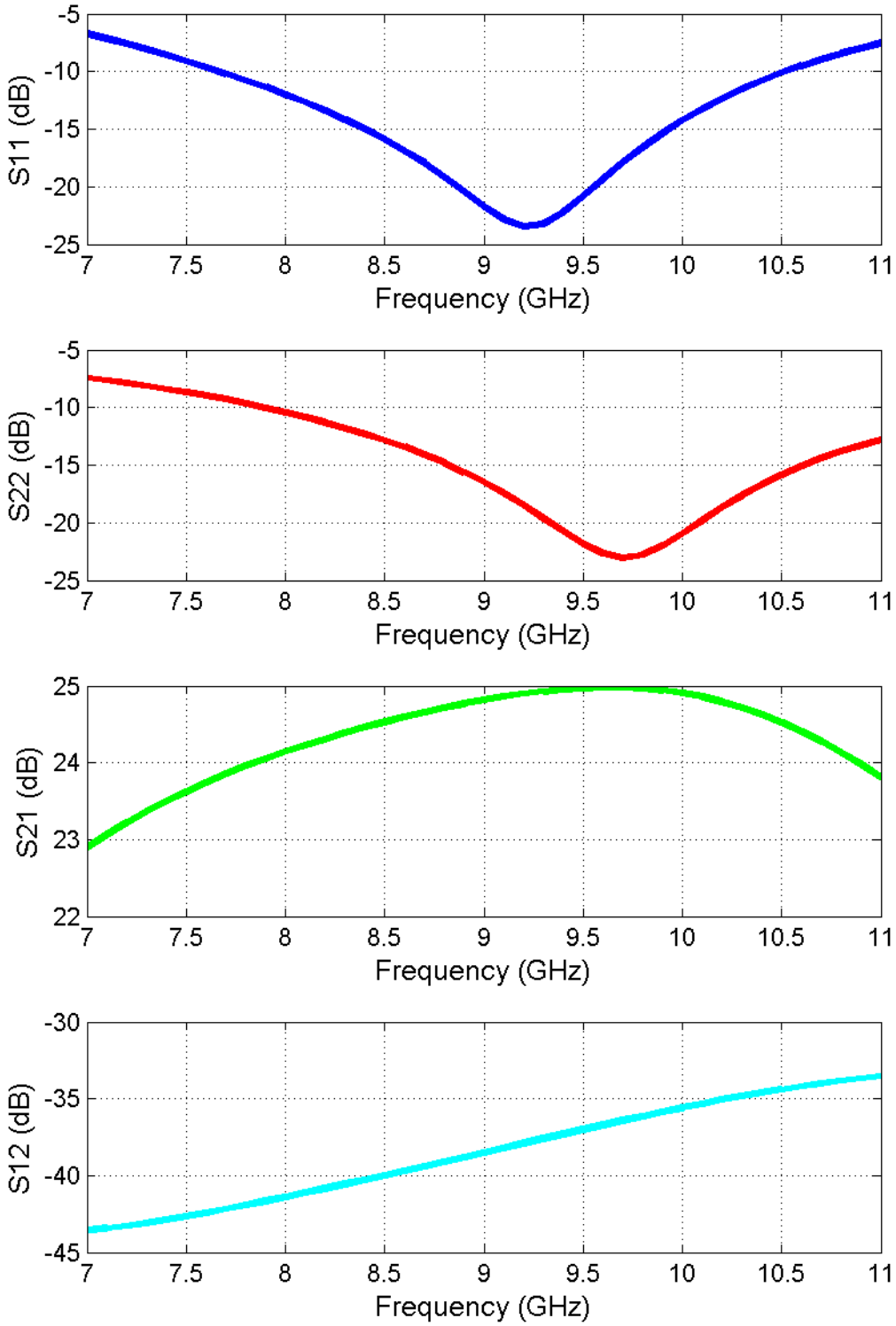

Figure 4.26 : S parameter simulation results of the second amplifier.

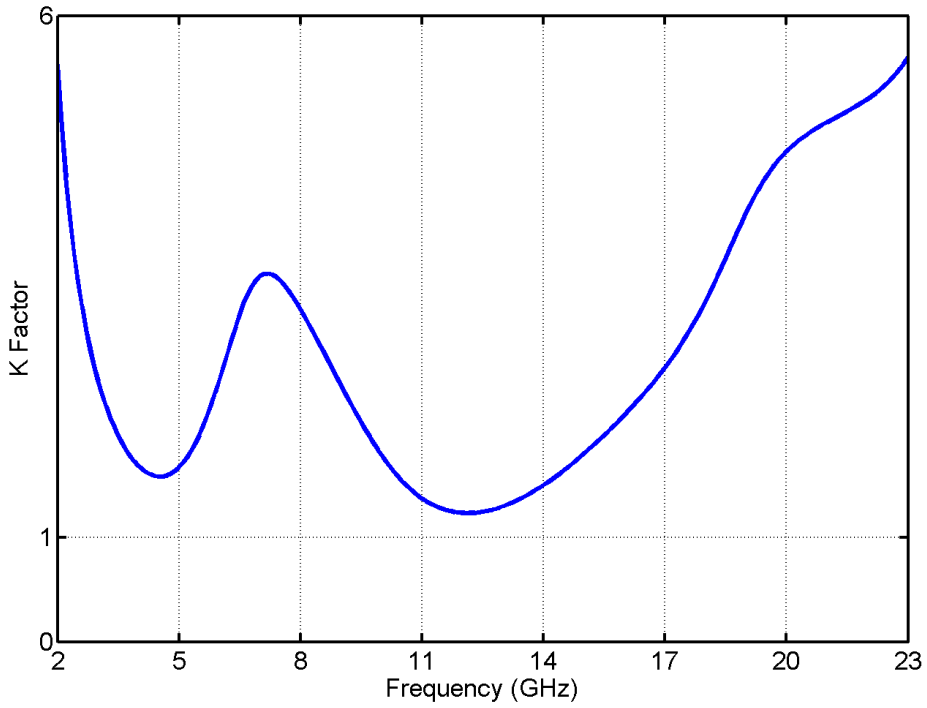

Figure 4.27 : Stability factor of the second amplifier.

S parameter simulation shows that amplifier has a maximum gain of 25 dB with 3 dB drop points covering 7-11 GHz band. The input and output return loss of the amplifier is better than 10 dB for 8-10.5 GHz band. Stability factor shows that the amplifier is unconditionally stable.

Harmonic balance simulation is done to observe noise figure, output third order intercept point, output power at 1-dB compression point for different frequencies. It is also repeated to observe power-added efficiency, gain and output power of the amplifier for different input power levels. Noise figure, output third order intercept point and output power at 1-dB compression point of the amplifier is shown in Figure 4.28, Figure 4.29 and Figure 4.30, respectively. Power-added efficiency, gain and output power of the amplifier for different input power levels is given in Figure 4.31.

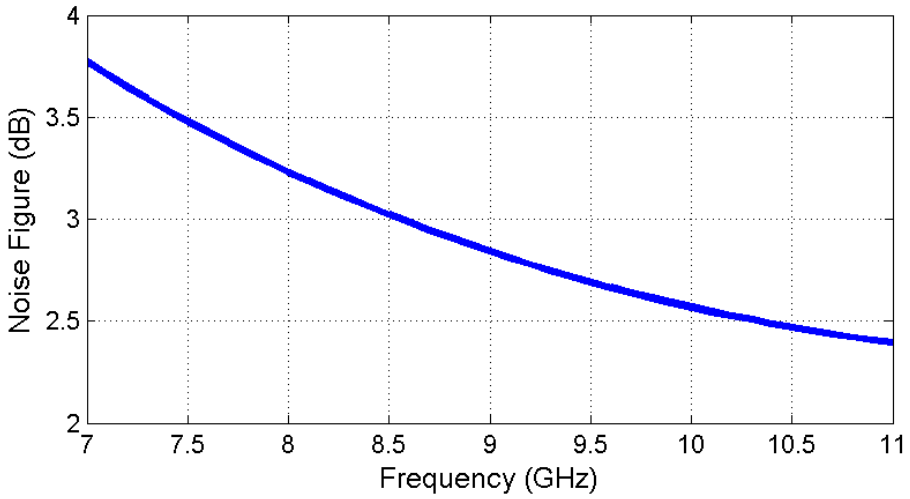

Figure 4.28 : Simulation results of the second amplifier showing noise figure.

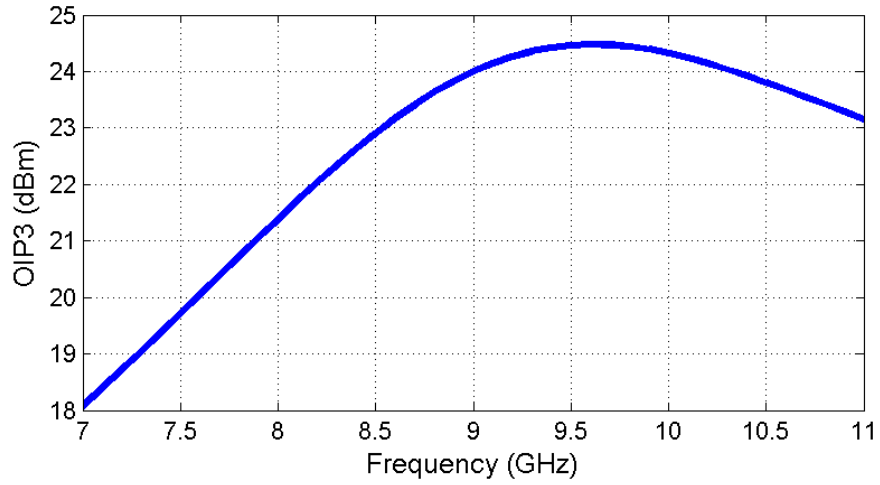

Figure 4.29 : Simulation results of the second amplifier showing OIP3.

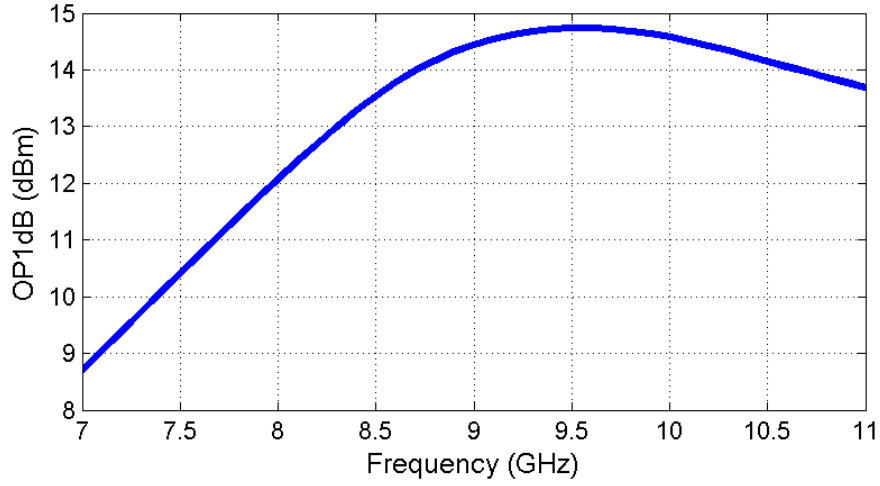

Figure 4.30 : Simulation results of the second amplifier showing OP1dB.

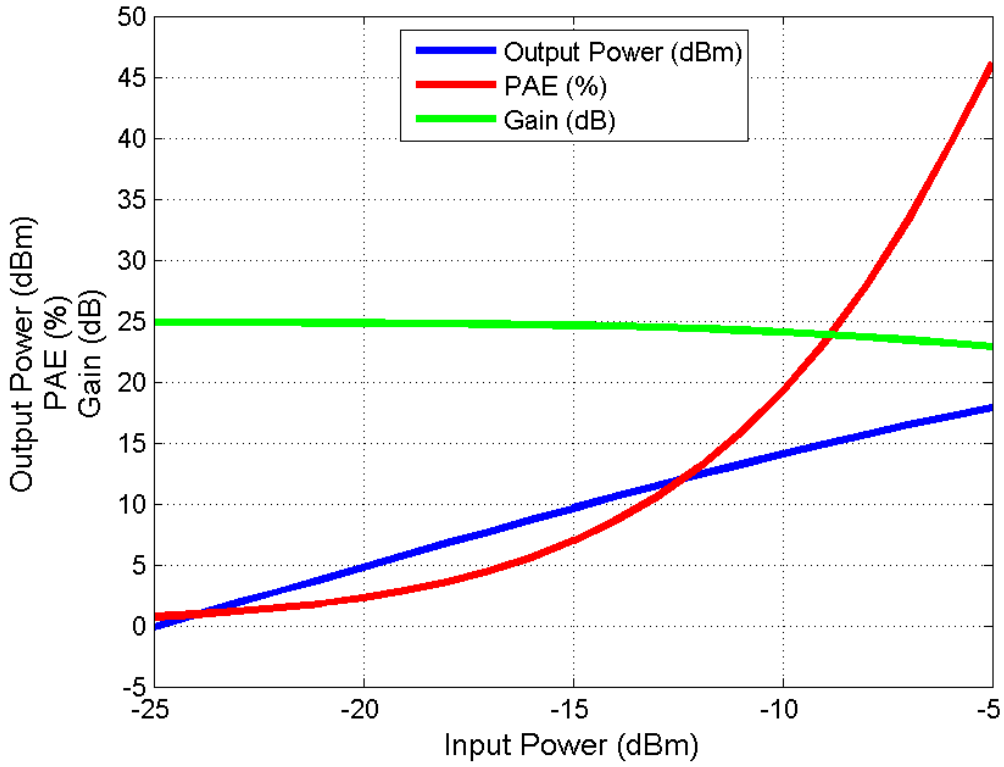

Figure 4.31 : Simulation results of the second amplifier showing PAE, gain and output power for different input power levels.

The amplifier shows below 4 dB noise figure for 7-11 GHz band. Output third order intercept point and output power at 1-dB compression point of the amplifier is above 24 dBm and 14 dBm respectively for the same bandwidth. Power added efficiency of the amplifier is over 20% at 1-dB compression point and it is over 40% at saturation.

4.2.4 Measurement results

Figure 4.32 shows the die photo of the manufactured driver amplifier. The die area is 1×1.2 mm^2 and the size of the amplifier core without pads is 0.8×1 mm^2. The test module size is 58×23 mm^2 including RF connectors. Input and output of the test module are connected to the amplifier via 50-Ω conductor-backed coplanar waveguides. No external components are used for the input and the output impedance matching. Thin-film capacitors are placed near the amplifier die for decoupling purposes. The test module is shown in Figure 4.33.

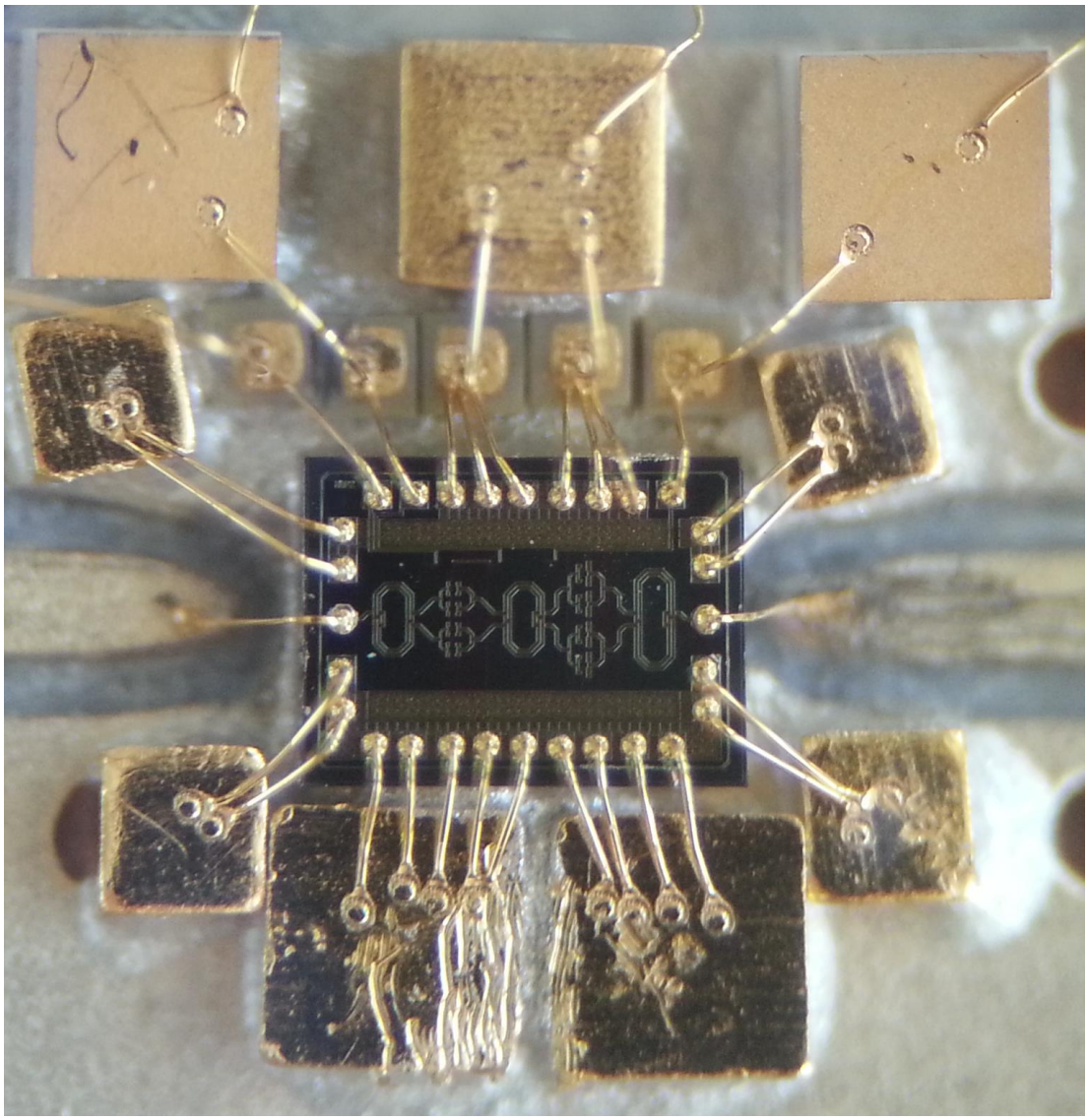

Figure 4.32 : Die photo of the second amplifier.

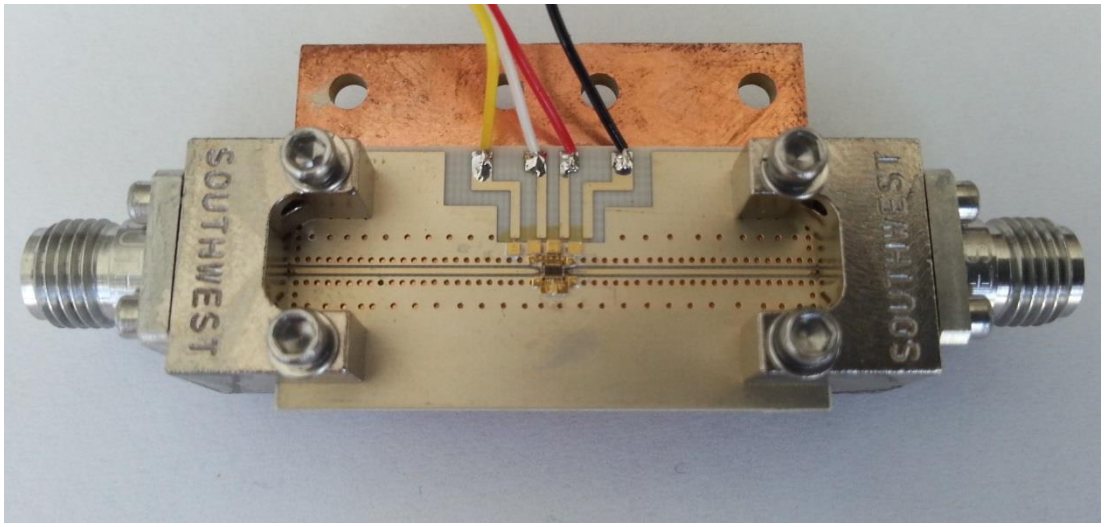

Figure 4.33 : Test module of the second amplifier.

Measurements of the second amplifier are also done in ITU VLSI Labs. S-parameter measurement results of the second amplifier are given in Figure 4.34. The maximum gain of the second amplifier is 26 dB at 9 GHz with 3-dB drop points at 7.5 and 10.5 GHz. The plot also shows better than 10 dB input and output return loss for the 7.5-10.5 GHz band.

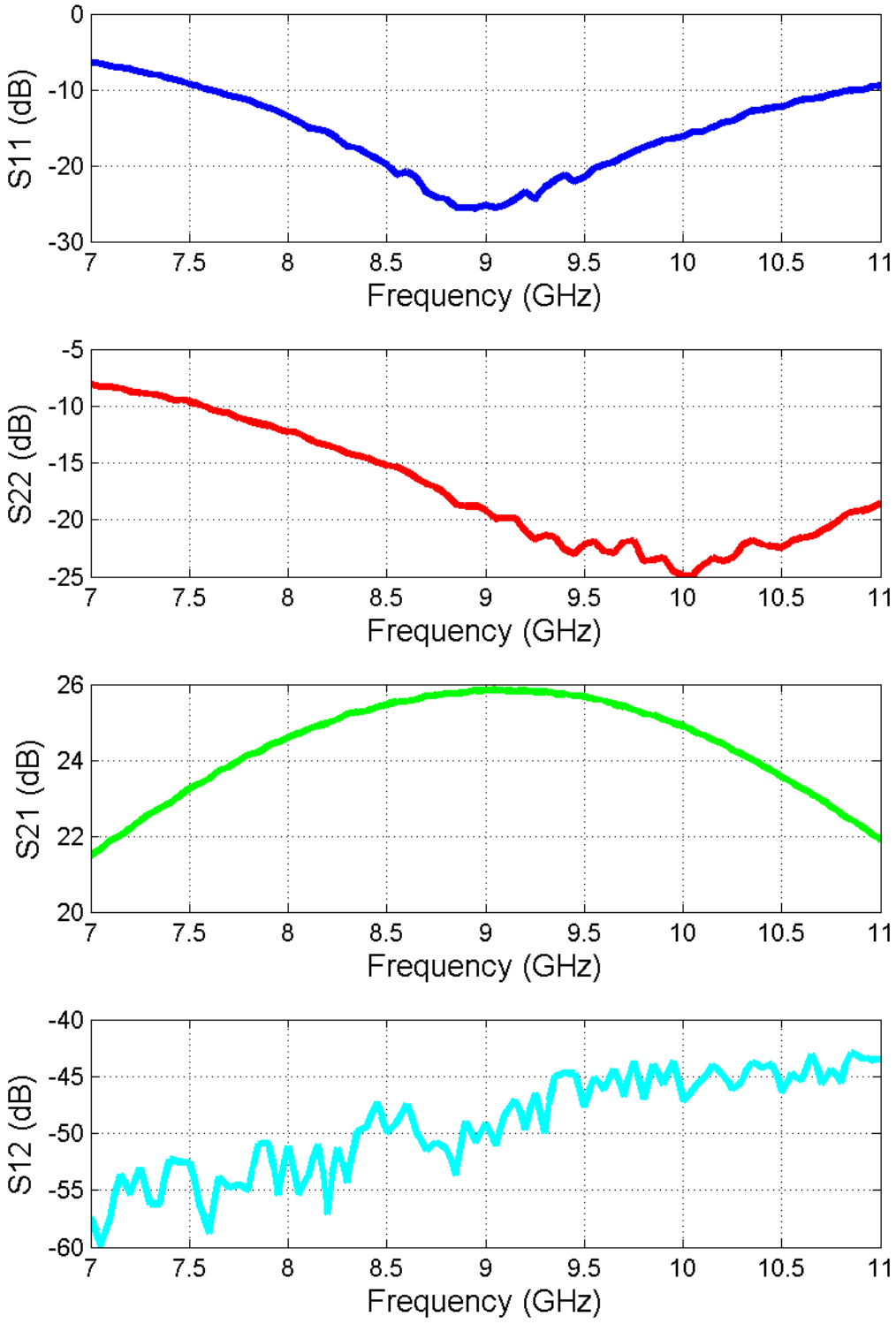

Figure 4.34 : S parameter measurement results of the second amplifier.

Noise figure measurement result of the second amplifier is shown in Figure 4.35. The noise figure of the second amplifier is below 5 dB for 7-11 GHz band.

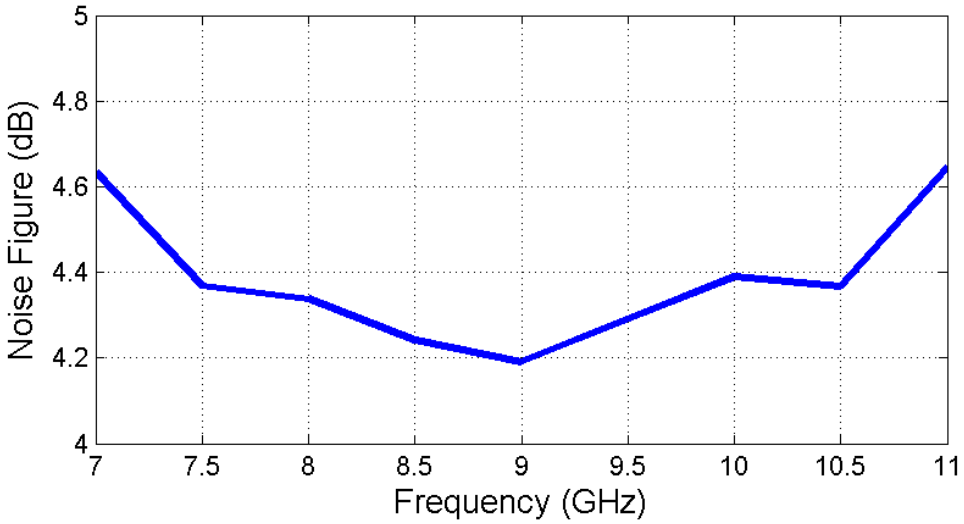

Figure 4.35 : Measurement results of the second amplifier showing noise figure.

Output power of the second amplifier at 1-dB compression point over the 7-11 GHz band can be seen in Figure 4.36. The second amplifier achieves a maximum output power of 14.8 dBm at 1-dB compression point. Figure 4.37 shows the power-added efficiency, gain, and output power of the second amplifier versus increasing input power at 10 GHz. The second amplifier achieves a power-added efficiency of 18% at 1-dB compression point, increasing to a maximum of 27% at saturation.

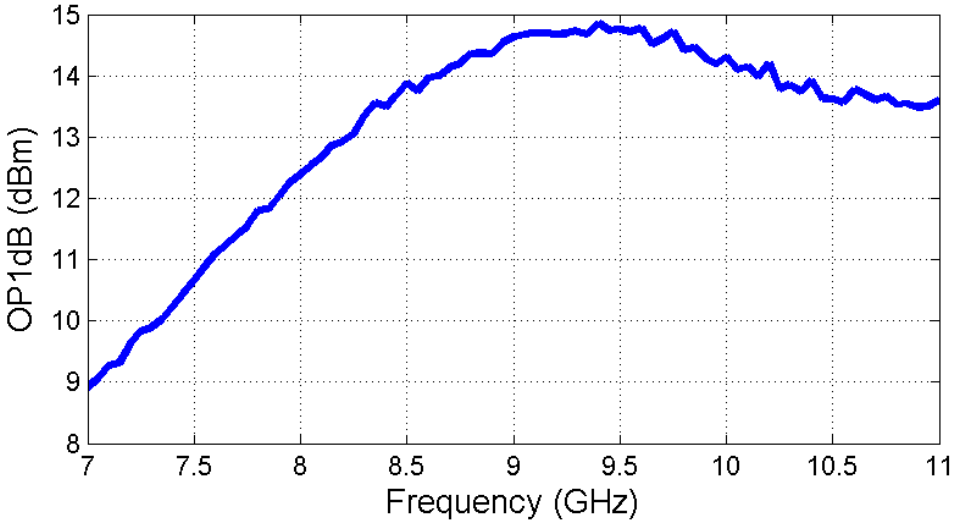

Figure 4.36 : Measurement results of the second amplifier showing OP1dB.

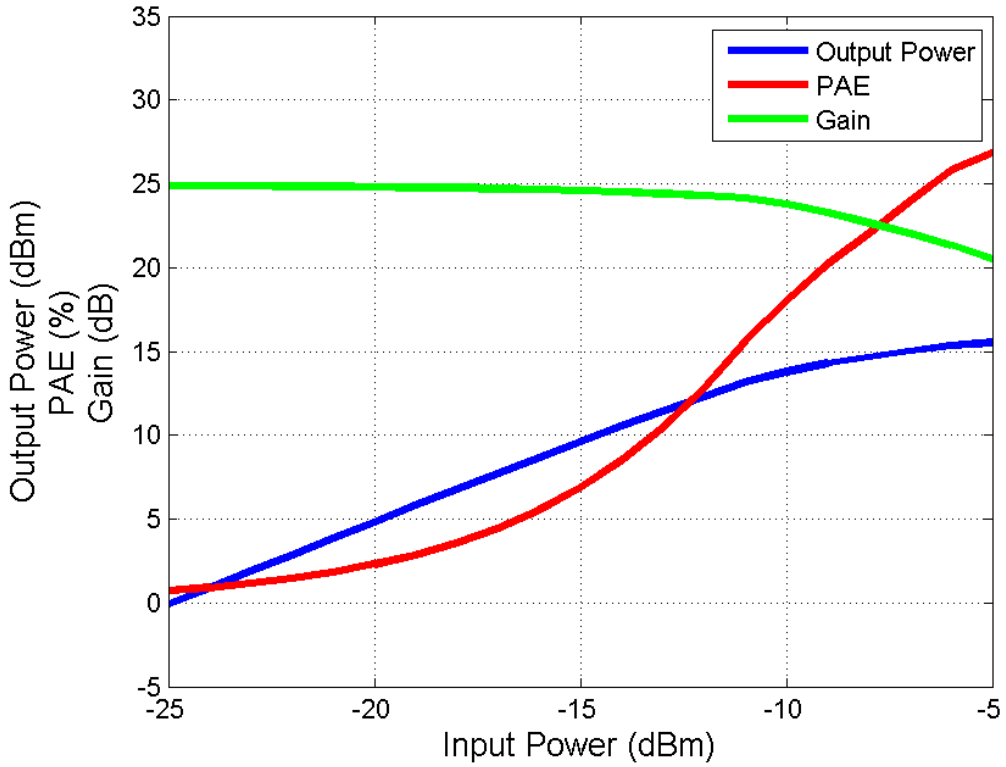

Figure 4.37 : Measurement results of the second amplifier showing PAE, gain and output power with increasing input power at 10 GHz.

Measured third order intercept point of the second amplifier for 7-11 GHz band is given in Figure 4.38. It can be seen that the second amplifier shows a maximum of 25 dBm output third order intercept point performance.

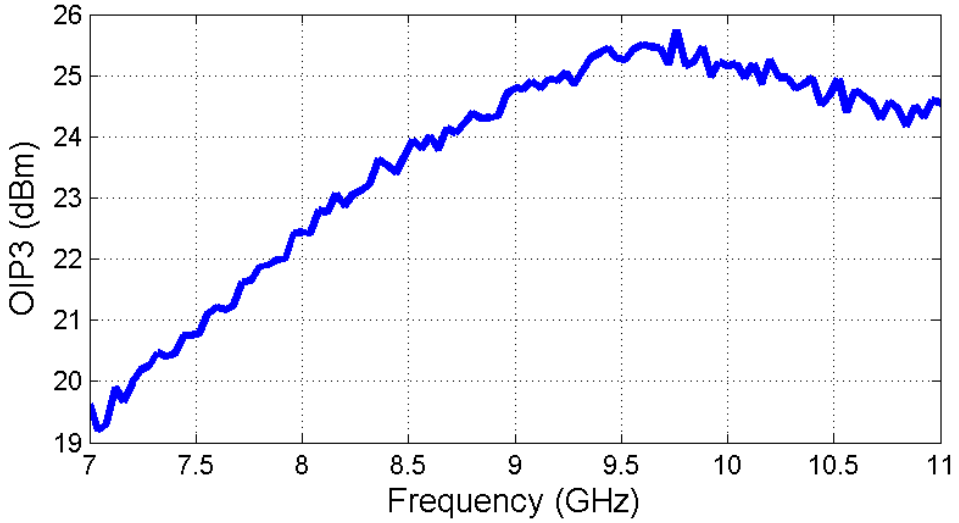

Figure 4.38 : Measurement results of the second amplifier showing OIP3.

5. CONCLUSION

SiGe BiCMOS technology continues to achieve higher performances and integrated RF solutions offered by this technology are the driving force behind practically every wireless system. The wireless range of such systems is extending by increasing input sensitivity and/or output power levels. High output power levels create need for gain and driver stages. In this thesis, an X-Band SiGe driver amplifier is designed to be used in an RF system as a gain and driver stage.

The simulated driver amplifier shows better than 10 dB input and output return loss for 7.5-11 GHz band. The amplifier shows a maximum gain of 24 dB with 3-dB drop points covering 7-10 GHz band. For an increasing input signal at 10 GHz, the amplifier shows output power levels of 13 dBm and 15 dBm with PAE of 14% and 23% at 1-dB compression point and saturation, respectively. Measurements show slightly inferior performance than simulations with better than 10 dB input, output return loss for 8-11 GHz band and a maximum gain of 22 dB with 3-dB drop points covering 7-10 GHz band. For an increasing input signal at 10 GHz, the measurements shows output power levels of 12 dBm and 14 dBm with PAE of 11% and 17% at 1-dB compression point and saturation respectively.

A second driver amplifier is designed to increase gain and linearity performance. Same simulations are also run for the second amplifier with results showing better than 10 dB input, output return loss for 8-10.5 GHz band and a maximum gain of 25 dB with 3-dB drop points covering 7-11 GHz band. For an increasing input signal at 10 GHz, the second amplifier shows output power levels of 14 dBm and 18 dBm with PAE of 20% and 45% at 1-dB compression point and saturation respectively. Measurements of the second amplifier show better than 10 dB input, output return loss for 7.5-11 GHz band and a maximum gain of 26 dB with 3-dB drop points covering 7.5-10.5 GHz band. For an increasing input signal at 10 GHz, measurements show output power levels of 14 dBm and 16 dBm with PAE of 18% and 27% at 1-dB compression point and saturation respectively.

As a follow up to this study, a third stage can be designed and added to the current circuit as a power stage. A three stage amplifier consisting of gain, driver and power stages can offer an absolute solution as a final stage of a transmitter system. However, three stage amplifier design and high power levels in an integrated circuit have many challenges with stability, thermal conditions, breakdown voltages and efficiency.

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