Available online at www.sciencedirect.com

ScienceDirect

Procedia Engineering 168 (2016) 1651 – 1654

Procedia Engineering

www.elsevier.com/locate/procedia

30th Eurosensors Conference, EUROSENSORS 2016

A General Purpose Lock-In Amplifier Enabling Sub-ppm Resolution

G. Gervasoni, M. Carminati, G. Ferrari

Dipartimento di Elettronica, Informazione e Bioingegneria, Politecnico di Milano, Piazza Leonardo da Vinci, 32, Milano 20133, Italy

Abstract

A novel architecture for digital lock-in amplifiers (LIAs) able to overcome the resolution limit of standards implementations is proposed. The slow gain fluctuations of both the DAC and ADC of the generation and acquisition stages of the LIA are compensated using two ADCs alternately acquiring the signal coming from the device under test (DUT) and the stimulus (STIM) signal. Experimental results demonstrate a resolution enhancement of more than an order of magnitude with respect to state of art LIAs, enabling sub-ppm resolution measurements with an instrument working up to 5 MHz without imposing any constraint to the DUT or to the experimental setup.

Peer-review under responsibility of the organizing committee of the 30th Eurosensors Conference

Keywords: Lock-in amplifier; ppm resolution; low-noise; FPGA; sensors.

1. Introduction

Lock-in amplifiers (LIAs) are extensively used for synchronous (phase-sensitive) AC signals detection and measurement in a wide range of scientific fields, from Atomic Force Microscopy (AFM), Raman spectroscopy, to sensors and actuators (e.g. MEMS), just to name a few [1]. Two main reasons justify such wide application of LIAs. Firstly, the idea of moving signals in frequency (signal modulation), instead of performing static measurements, arises from the ubiquitous presence of 1/f noise, given by electronics circuits, devices, sensors or others elements taking part in experiments. Secondly, the physics itself of the experiment can impose an AC measurement, as in the case of impedance measurements, capacitance measurements or resonant phenomena. In both cases, the frequency selectivity of the LIA allows a measurement of the AC signal with an optimal signal-to-noise ratio.

The minimum detectable signal of a lock-in amplifier depends on its input equivalent noise (at the working frequency) and on the chosen filtering bandwidth. State-of-the-art instruments show an input equivalent noise as low as few nV/√Hz with an input range of few mV. For some applications, it is necessary to detect very small variation of a relatively big signal. This is the case of certain sensors where it is necessary to measure very tiny variations in

Peer-review under responsibility of the organizing committee of the 30th Eurosensors Conference

doi:10.1016/j.proeng.2016.11.482

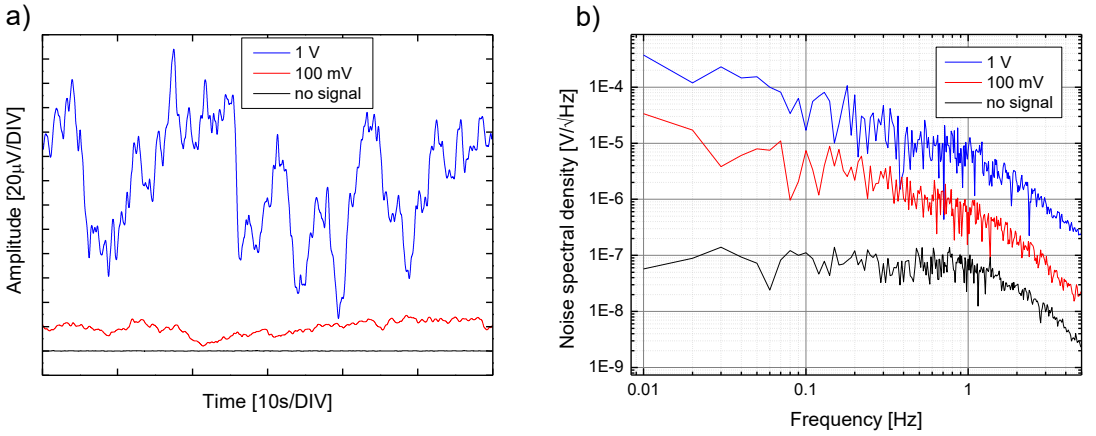

Figure 1: Minimum detectable signal and minimum detectable signal variation.

the DUT electrical properties (like resistance, capacitance or both). Ideally, we would be able to measure a signal variation given by the instrument input equivalent noise and the chosen filtering bandwidth as for the minimum detectable signal. Here, we show that digital lock-in amplifiers have an additional 1/f output noise proportional to the measured signal. Consequently, the minimum detectable signal variation results proportionally dependent to the total signal itself and orders of magnitude greater than the minimum detectable signal, allowing resolutions not lower than few tens of ppm. Section 2 and 3 analyze the additional noise of digital LIAs and in section 4 we propose a technique to overcome this limitation. The new technique is experimentally demonstrated in section 5.

2. Experimental results with state-of-the-art lock-in amplifier

Three experimental measurements, shown in Fig. 1, help clarifying the difference between the minimum detectable signal and the minimum detectable signal variation, and highlight the limit in the performance of a commercial instrument. These experiments have been done using the state-of-the-art lock-in amplifier HF2LI, from Zurich Instruments, the output and the input have been connected through a BNC cable and a 1 MHz sinusoidal stimulus has been generated. The input and output range have been set to 1.1 V and 1 V respectively, the filter bandwidth to 1 Hz.

Fig. 1(a) shows three different experiments, in the first (no signal) we obtain the minimum detectable signal, about 90 nV with a SNR = 1. In the second measurement we acquire a signal of 100 mV, but differently from what expected, the rms noise is much more than 90 nV, about 4.7 µV. Finally, we acquire a signal of 1 V, obtaining a rms noise of 43 µV. In conclusions, the noise increases with the signal amplitude and in particular, from the noise spectral analysis (Fig. 1(b)), an additional signal-proportional 1/f noise appears. From the ratios 4.7 µV / 100 mV and 43 µV / 1V we obtain a minimum achievable resolution of about 43 ppm, which cannot effectively benefit from narrower low-pass filtering because limited by 1/f slow fluctuations.

The large input signal can be reduced using a differential configuration of the device under test. The additional noise of LIA becomes proportional to the small unbalanced differential signal allowing sub-ppm measurements [2]. However, in many cases a differential configuration requires a precise calibration of a dummy path making the experimental setup more complex and limiting the measurement frequency to the calibrated one.

3. Gain fluctuations sources

The measured signal-proportional additional noise is due to slow gain fluctuations that the modulated signal experiences from the generation stage to the acquisition one. In particular, the DAC and ADC used for signal generation and acquisition, as well as the analog stages, introduce these gain fluctuations. As shown in Fig. 2, a random variation of the voltage references used by DAC and ADC results in signal amplitude modulation, i.e. the

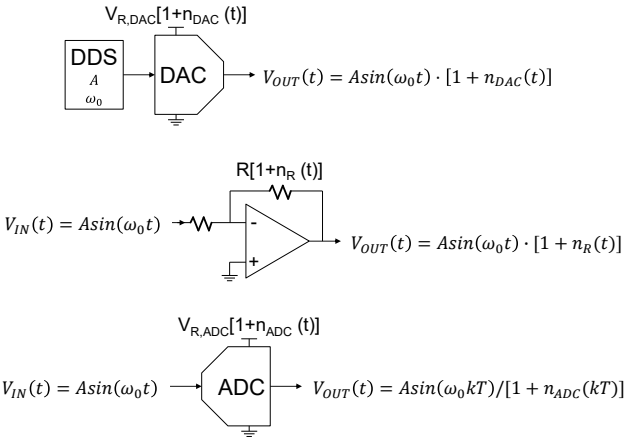

Figure 2: Gain fluctuations sources and effect on the demodulated signal

signal experiences gain fluctuations. In fact, if the DAC reference voltage increase, the DAC gain increase, differently if the ADC reference voltage increase, the ADC gain decrease. Similar effects can originate from converters internal circuits and, regarding the analog stages, gain fluctuations can be due to resistors value variations, given by intrinsic 1/f noise or temperature fluctuations. This amplitude random modulation is successively down-converted through demodulation, causing random fluctuations of the LIA output. In agreement with the experimental data, these fluctuations are proportional to the signal amplitude and independent from the modulation frequency. To compensate these fluctuations, a novel technique based on two ADCs alternately acquiring the signal coming from the DUT and the stimulus (STIM) signal has been implemented. The idea is that both DUT and STIM signals should experience the same gain fluctuations (due to DAC and ADC), which can be successively removed by means of a division on the outputs of the synchronous demodulation. Regarding the analog stages, we choose to implement resistors characterized by low temperature coefficient (< 5 ppm/K) and low 1/f intrinsic noise as already done for low frequency lock-in amplifier [3].

4. The Enhanced Lock-In Amplifier (ELIA) Scheme

The Enhanced-LIA (ELIA) scheme is shown in Fig 3(a). Two switches SW1 and SW2 are added in front of the ADCs (operating at 80 MS/s) to alternatively acquire the DUT and STIM signals with each ADC. The signals are

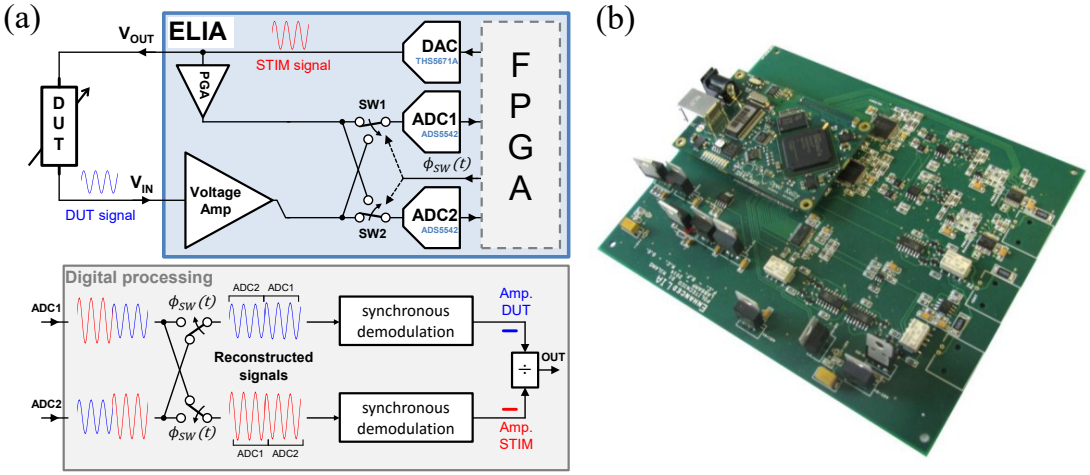

Figure 3: (a) Enhanced Lock-In Amplifier (ELIA) architecture; (b) Realized board.

reconstructed in real-time using a FPGA (Spartan 6 running at 80 MHz) to obtain their time evolution with continuity in the digital domain. The following demodulation and averaging are performed as in a standard dual-phase LIA obtaining amplitude and phase of the DUT and REF signals. The switching frequency f_{SW} of SW1 and SW2 is chosen of hundreds of Hz that is faster than the slow random gain fluctuations of the instrument. As a consequence, the equivalent gain in a period $1/f_{SW}$ experienced by the two reconstructed signals is the same and is equal to the mean of the two ADC gains. The effect of the gain fluctuations is finally canceled out by performing the ratio between the amplitudes of the DUT and REF signals. Note that also the gain fluctuations of the DAC are included in both signals and therefore are removed as well, allowing a high-resolution measurement of the DUT response.

5. Results

As an example of the ELIA performance, Fig. 4 shows the tracking of a time-varying resistance of 250 Ω periodically changed of ΔR = 1.25 mΩ. The measurement has been performed in three different conditions: (1) using the commercial state-of-the-art HF2LI by Zurich Instruments; (2) using the custom ELIA as a standard lock-in (i.e. only measuring the DUT signal); (3) using ELIA with the new technique (f_{SW} = 1 kHz). The signal amplitude applied to the time-varying resistance is 300 mV and the filtering bandwidth of 1 Hz. The resolution enhancement of more than an order of magnitude (from 9 to 0.6 ppm), obtained compensating the gain fluctuations of the LIA,

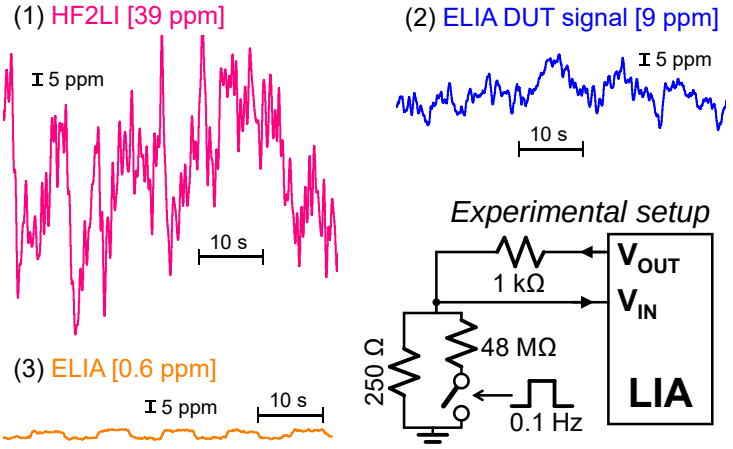

Figure 4: Experimental results during the tracking of a time-varying resistance.

allows a clear detection of tiny (5 ppm) steps of resistance modulation. Similar resolutions (< 0.8 ppm) have been achieved using a complex impedance as DUT demonstrating an operation insensitive to the signal phase and to the measurement frequency up to 6 MHz. Thus, ELIA is a high-resolution replacement of a standard LIA in sensor and in device characterization applications without requiring changes in the experimental setup nor calibration.

References

[1] A. Chighine et al, An FPGA-based lock-in detection system to enable chemical species tomography using TDLAS, 2015 IEEE International Conference on Imaging Systems and Techniques (IST) (2015) 1-5.

[2] M. Carminati et al, Note: differential configurations for the mitigation of slow fluctuations limiting the resolution of digital lock-in amplifiers, Review of Scientific Instruments 87 (2015).

[3] G. Gervasoni et al, A 12-channel dual-lock-in platform for magneto-resistive DNA detection with ppm resolution, 2014 IEEE Biomedical Circuits and Systems Conference (BioCAS) Proceedings (2014) 316-319.