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Pulse Shape and Timing Dependence on the Spike-Timing Dependent Plasticity Response of Ion-Conducting Memristors as Synapses

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Ion-conducting memristors comprised of the layered materials Ge_2Se_3/SnSe/Ag are promising candidates for neuromorphic computing applications. Here, the spike-timing dependent plasticity (STDP) application is demonstrated for the first time with a single memristor type operating as a synapse over a timescale of 10 orders of magnitude, from nanoseconds through seconds. This large dynamic range allows the memristors to be useful in applications that require slow biological times, as well as fast times such as needed in neuromorphic computing, thus allowing multiple functions in one design for one memristor type—a "one size fits all" approach. This work also investigated the effects of varying the spike pulse shapes on the STDP response of the memristors. These results showed that small changes in the pre- and postsynaptic pulse shape can have a significant impact on the STDP. These results may provide circuit designers with insights into how pulse shape affects the actual memristor STDP response and aid them in the design of neuromorphic circuits and systems that can take advantage of certain features in the memristor STDP response that are programmable *via* the pre- and postsynaptic pulse shapes. In addition, the energy requirement per memristor is approximated based on the pulse shape and timing responses. The energy requirement estimated per memristor operating on slower biological timescales (milliseconds to seconds) is larger (nanojoules range), as expected, than the faster (nanoseconds) operating times (~0.1 pJ in some cases). Lastly, the memristors responded in a similar manner under normal STDP conditions (pre- and post-spikes applied to opposite memristor terminals) as they did to the case where a waveform corresponding to the difference between pre- and post-spikes was applied to only one electrode, with the other electrode held at ground potential. By applying the difference signal to only one terminal, testing of the memristor in various applications can be achieved with a simplified test set-up, and thus be easier to accomplish in most laboratories.

Keywords: memristor, ion-conductor, non-volatile memory, ReRAM, STDP

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INTRODUCTION

Bioinspired neuromorphic computing has the potential of becoming realizable through the application of memristors (Chua, 2015) as artificial synapses (Jo et al., 2010; Chang et al., 2011; Erokhin and Fontana, 2011; Rose et al., 2011a,b; Gaba et al., 2013; Serrano-Gotarredona et al., 2013a; Subramaniam et al., 2013; Thomas, 2013; Mahalanabis et al., 2016). The spike-timing dependent plasticity (STDP)

synaptic learning rule, inspired from the behavior of the biological neural system (Dayan and Abbott, 2001) and dominant in the brain, has been proposed and experimentally demonstrated with memristors acting as synapses by several groups over the past few years in many material systems, such as oxides (Yu et al., 2011; Wang et al., 2012a,b, 2016; Wu et al., 2012; Pickett et al., 2013; Mandal et al., 2014; Kim et al., 2015), chalcogenides (Li et al., 2013b; Mahalanabis et al., 2014a,b, 2016; La Barbera et al., 2015), silicon (Jo et al., 2010; Subramaniam et al., 2013), organic materials (Alibart et al., 2012; Li et al., 2013a; Cabaret et al., 2014; Luo et al., 2015), and even magnetic tunnel junctions (Krzysteczko et al., 2012). Illustrations of memristor effectiveness have also been shown in simulation and with transistor and/or complementary metal oxide semiconductor (CMOS)-based memristors (Rachmuth et al., 2011; Rose et al., 2011a,b; Cruz-Albrecht et al., 2012; Noack et al., 2015) and graphics processing units (Snider et al., 2011). The exploration of new memristor materials systems is driven by the advantage of analog, memristor-based learning implementations compared to the digital-based learning, where the analog, memristor-based learning was shown to provide an improvement of at least a factor of 10 for power and density (Rajendran et al., 2013) over digital-based learning. The larger area and power requirement for CMOS-based memristors have driven the research into novel material-based memristor STDP to find a lower power/area alternative for neuromorphic computing.

Some of the issues with previous experimental implementations of memristors in the synaptic role in the STDP application (Chang et al., 2011; Rose et al., 2011a,b; Li et al., 2013a; Subramaniam et al., 2013; Luo et al., 2015; Mahalanabis et al., 2016) include the lack of analog programmability of the memristor, high power requirements, and requirement of very specific programing spike shapes in order to effectively program the synaptic weights. Recent work, using a TaO_x memristor as a synapse has demonstrated incremental switching in memristors, through the use of repetitive pulses and a pulse train with increasingly higher amplitudes. However, the pulses used in this study were limited to 100 ns pulse width (Wang et al., 2016). A similar TaO_{5-x} memristor was also used (Kim et al., 2015) to demonstrate the effects of incremental pulses on the memristor resistance tuning, as well as use of pulses in the range of 100 ns to 10 μs to demonstrate the STDP response. It should be noted that the incremental resistance programing response was also demonstrated in a chalcogenide-based memristor based on a phase-change mechanism, using 30 ns pulses in a five pulse train with increasing pulse amplitude from 1 to 1.8 V to increase resistance and −0.6 to −0.8 V to decrease resistance (Li et al., 2013b).

The memristor used in this work is based on the ion-conducting self-directed-channel (SDC) memristor, which has demonstrated lifetime endurance greater than one billion cycles, operation at temperatures of 150°C without degradation, and analog programmability (Campbell, 2017). This device is comprised of chalcogenide material layers (**Figure 1**) (Campbell, 2008a,b, 2017). It uses a Ge_2Se_3 chalcogenide layer, which is activated for analog resistance tuning operation by Sn ions that migrate from an adjacent SnSe layer during the initial forming process (Campbell and Anderson, 2007; Devasia et al., 2010, 2012). A layer of ternary GeSeAg is the ion source during operation.

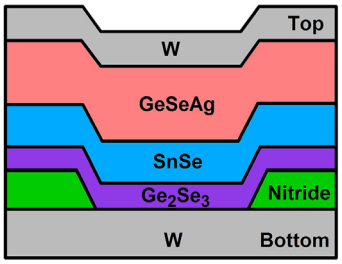

FIGURE 1 | Memristor device structure showing (from bottom to top) the bottom tungsten (W) electrode, the insulating nitride layer which defines the active layer contact area to the bottom electrode, the active layer (Ge_2Se_3) followed by the SnSe, GeSeAg, and top tungsten electrode layers. The function of each layer is described in Campbell (2017).

In contrast to other Ag-based GeSe or GeS ion-conducting device types (Mitkova and Kozicki, 2002; Kozicki and Mitkova, 2006; Kamalanathan et al., 2009; Waser et al., 2009; Wang et al., 2011; Mahalanabis et al., 2014a,b; Rajabi et al., 2015; Ielmini and Waser, 2016), no photodoping or thermal annealing steps are required, simplifying the fabrication steps, and producing more consistent device operation. These differences also enable the device used in this work to withstand higher fabrication (at least 300°C) and operating temperatures (operation at 150°C is routinely performed). Additionally, this device can be integrated into a back-end-of-line (BEOL) CMOS process (Regner et al., 2009) making it compatible with CMOS architectures (Serrano-Gotarredona et al., 2013b).

The advantage of the SDC memristor used in this work, over all of the memristors described to date in the STDP application is that it is the only memristor that has been shown to be simultaneously capable of (1) operation over nanoseconds to seconds timescale in STDP; (2) analog programmability over at least four orders of magnitude of resistance; (3) operation at high temperature (150°C); (4) cycling in excess of one billion times; and (5) demonstrated incorporation into a BEOL CMOS process. The scalability is predicted to be easily below 20 nm due to the one dimensional aspect of device operation (based on success at 27 nm node of CuTe-based 16 Gb memory; Fackenthal et al., 2014).

The analog resistance programing capabilities of the SDC memristor used as a synapse are demonstrated in this work through the memristor's synaptic weight change induced during the STDP experiment over the nanoseconds to seconds timescale, and the response to four different synaptic pulse shapes (**Figure 2**). These pulse shapes were used to explore the effects of the spike shape on the STDP response. As has been previously noted (Zhu et al., 2014; Qu et al., 2016), the ion-conducting memristive devices are logical candidates for this purpose since they have functional similarities to biological synapses in that both synapse types have a dependence on ion species to alter the synaptic strength.

In addition to the STDP pulse shape tests, the memristor response to only the resultant waveform applied to one electrode

while the other electrode was held at ground potential was also measured.

MATERIALS AND METHODS

Device Fabrication

Ion-conducting devices were fabricated with a *via* structure and top and bottom electrodes, as shown in **Figure 1**. The active switching layer is the 300 Å Ge_2Se_3 layer adjacent to the bottom electrode.

Devices were fabricated on 100 mm p-type Si wafers with the bottom electrode of 250 Å Cr/500 Å W already deposited *via* chemical vapor deposition on the wafers (purchased from Encompass Distribution Services, Tracy, CA, USA). The bottom electrode was patterned, followed by 800 Å sputtered nitride (AJA International ATC Orion 5 UHV Magnetron sputtering system). A *via* etched through this nitride layer (Oxford Plasma Etcher) defines the device contact area. *Via* sizes for this work were 4 μm in diameter and there were at least 200 devices per wafer.

Wafers were pre-sputtered with Ar^+ to remove any oxide species from the bottom electrode, followed by *in situ* sputter deposition of all of the remaining device layers and top tungsten electrode layer, using an AJA International ATC Orion 5 UHV Magnetron sputtering system. The target layer thicknesses were (from bottom to top): Ge_2Se_3 (300 Å)/SnSe (800 Å)/Ge_2Se_3 (150 Å)/Ag (500 Å)/Ge_2Se_3 (100 Å)/W (400 Å). The top three layers below the tungsten top electrode, corresponding to Ge_2Se_3/Ag/Ge_2Se_3, mix during fabrication, becoming one conductive layer. Final device etching was performed with a Veeco ME1001 ion-mill. The active switching layer is the 300 Å Ge_2Se_3 layer deposited adjacent to the bottom electrode. The SnSe layer provides Sn ions and isolates the Ge_2Se_3 layer from direct contact with the Ag layer.

Device Operation

Devices are initially in a high resistance state (megaohms to gigaohms range) following fabrication. The first programing operation applies a positive potential to the top electrode and forces Sn ions from the SnSe layer into the active Ge_2Se_3 layer (Campbell and Anderson, 2007; Devasia et al., 2010, 2012; Campbell, 2017). For the devices used in this work, in addition to Sn ions from the SnSe layer, Ag^+ ions from the GeSeAg layer are also incorporated into the active layer during this first programing operation. A conductive pathway, likely comprised of multiple conductive channels (Banerjee and Chakravorty, 1999; La Barbera et al., 2015), forms due to incorporation of these ions into the active layer, resulting in a resistance drop. The resistance can be increased by application of a potential across the device that places the top electrode at a lower potential than the bottom electrode, thus forcing ions out of the conductive channel toward the top electrode. The resistance of a device is related at any time to the resultant conductivity of the active switching layer, which is in turn related to the amount of incorporated metal and organization of conductive channels within the active layer (Banerjee and Chakravorty, 1999; La Barbera et al., 2015). A description of SDC device operation and differences between the SDC device and other ion-conducting devices, such as the conductive bridged random access memory, is in Campbell (2017).

A DC (quasi-static) measurement of a typical memristor used in this work exhibits the current–voltage (IV) curve shown in **Figure 3**. The IV curve shows a device initially in a high resistance state, which is switched to a low resistance with the application of a positive potential and switched to a high resistance through application of a negative potential. To see this in **Figure 3**, the measurement starts at $V = 0$ and follows the direction of the arrows toward +0.5 V, and then sweeps backwards through $V = 0$ to −0.5 V and back to $V = 0$ V. The transition from a high to low resistance occurs when a threshold voltage is reached (marked with ‡ on IV curve). The transition from low to high resistance occurs at a reverse threshold voltage (marked with # on the IV curve). To prevent the device from being overheated after it switches to a low resistance, a compliance current of 100 μA is used to limit the current. Thus, when the current through the device reaches 100 μA as it switches from high to low resistance, it is clamped at that value. This appears as a flat line in the IV curve at current = 100 μA. This general "bowtie" IV response is characteristic of the SDC device.

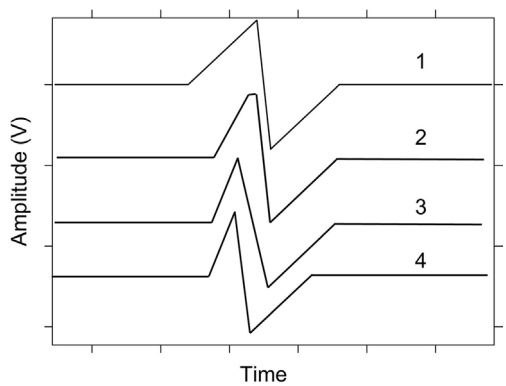

FIGURE 2 | **Spike shapes 1–4 used during spike-timing dependent plasticity testing**.

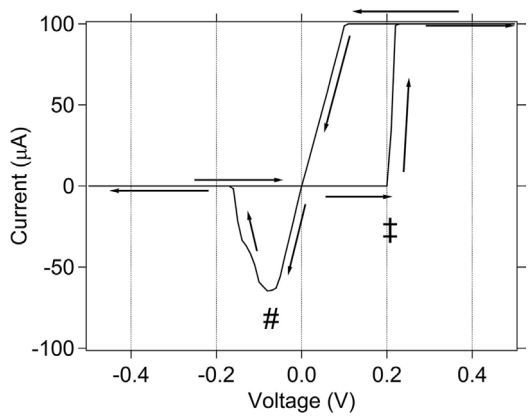

FIGURE 3 | **DC (quasi-static) IV curve for memristor used in this work**. ± denotes the threshold voltage for switching from high to low resistance. # denotes the threshold voltage for switching from low to high resistance. The compliance current used is 100 μA.

The SDC memristor is classified as a "generic" memristor (Chua, 2015) as shown by the sinudoidal input frequency response IV curves for the memristor (**Figure 4**). As the frequency of the sinusoidal input is increased from 1 Hz toward 100 kHz, the IV curve shows positive and negative lobes that collapse into a straight line through the IV origin as the frequency is increased. This is one of the hallmark features of the generic memristor. It should be noted clearly that this does not indicate that the frequency response of the device is poor, as is often the misinterpretation when one sees this sinusoidal response. In fact, the device can respond quite well to short (nanoseconds) pulses, as is demonstrated in this and previous (Campbell, 2017) work.

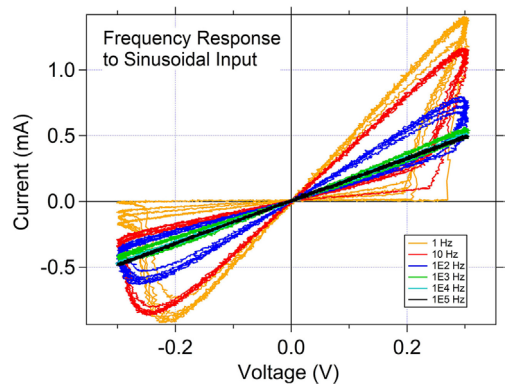

FIGURE 4 | **Response of the memristor to a sinusoidal input signal as a function of frequency**. The response of the memristor to the sinusoid as a function of input signal frequency indicates that this is a generic memristor.

Electrical Measurements

All electrical measurements were performed at the wafer level using a Micromanipulator 6200 microprobe station and an Agilent B1500A Semiconductor Device Parameter Analyzer equipped with two 2-channel waveform generator/fast measurement units (WGFMUs). Each WGFMU was connected to an electrode on the memristor and used to generate the pre- and postsynaptic spikes. Device resistance was read immediately before and after each ΔT test by measuring the current during application of 20 mV DC potential across the memristor. A DC potential of 20 mV is low enough to avoid perturbing the state of the device. **Figure 5** shows the STDP measurement set-up.

Each spike shape (**Figure 2**) function was separately created in software using the HP33250A arbitrary waveform generator drawing/creation program (BenchLink Arb) and exported as a waveform file. This function was then included in a C^{++} program, along with the B1500 measurement commands for the STDP tests (described in Section "STDP Experiment") for each given experiment. This program then controlled the B1500 for the duration of the STDP measurements and then it saved the data from the B1500 in the form of a csv file. Once created, the STDP testing program could be altered for each different pulse shape by simply creating a new spike shape and including that in the command code. **Table 1** lists the measurement parameters for the pulse shape tested, the maximum ΔT achieved during the test, the time step size for the pulse (resolution between points on the spike), the amplitude of the pulse, and the number of devices tested with those conditions.

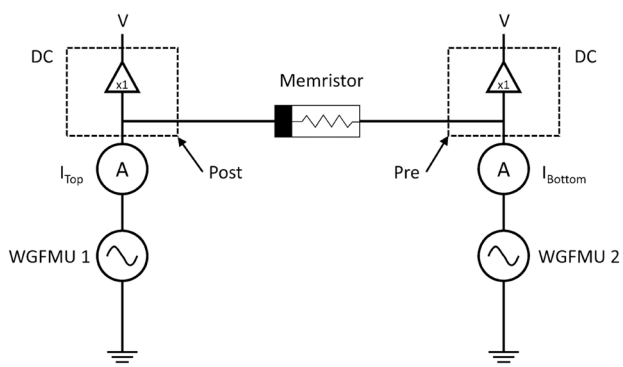

FIGURE 5 | **Electrical measurement test set-up**. The waveform generator/fast measurement units produce the pulses, whereas the RSU channels provide the DC measurement of resistance after every ΔT test.

STDP Experiment

In STDP, the difference in time between the firing of pre- and postsynaptic neurons determines whether the "strength" of the connection between those neurons increases or decreases. Biologically, this is caused by a change in the ion concentration in the intracellular space between the neurons making it more or less conductive. It was shown (Bi and Poo, 2001) for a biological synapse that when the presynaptic spike arrives before the postsynaptic spike ($\Delta T > 0$), the synapse exhibited increased synaptic weight ($\Delta w > 0$) and when the presynaptic spike arrives after the postsynaptic spike ($\Delta T < 0$) that the synapse exhibited decreased synaptic weight ($\Delta w < 0$). If the two neurons fire close in time, they will have a larger influence on the change in the synapse strength.

To illustrate the STDP concept, **Figure 6A** shows an example of an action potential presynaptic spike function. Five postsynaptic spikes with the same function, just separated in time from the presynaptic spike (**Figure 6A**) by $\Delta T \in \{-20, -10, 0, 10, 20\}$, are shown in **Figure 6B**. The corresponding difference signals (often referred to as resultant waveforms) between the presynaptic spike and each of the five postsynaptic spikes (plotted against ΔT and time) are shown in **Figure 6C**. Note how the shape, magnitudes, and polarity of the resultant signal changes as a function of ΔT. The difference signals are completely dependent on the shapes of the individual spikes. There are many potential pulse shapes that could be used in spiking neural networks that rely on STDP for learning [see examples in Zamarreño-Ramos et al. (2011)]. Four shapes inspired by these were used in the work described here (**Figure 2**).

In neuromorphic computing, the memristor acts as the synapse and is connected at the two electrode terminals to the pre- and postsynaptic neurons. The STDP experiment emulates nature by applying simple action potentials of the same pulse shape to the two electrodes of the memristor and varying the time

TABLE 1 | Spike-timing dependent plasticity ΔT timescales and pulse shapes tested.

Test type	Pulse shape tested	ΔT max/ step size	Full-width-half-maximum	Amplitude (V)	# Devices tested	Estimated energy requirement per memristor (assuming resistance range of 1 kΩ–1 MΩ)
Long	1	1 s/50 ms	137.5 ms	±0.2	5	0.5 μJ–5 nJ
	2	400/10 ms	104 ms	0.2/−0.1	26	0.4 μJ–0.1 nJ
Med	1	10 ms/500 μs	1.375 ms	±0.35	5	17–0.1 nJ
	2, 3,4	40/1 ms	10.4 ms	0.3/−0.2	10	93–0.1 nJ
Short	1	100/5 μs	13.75 μs	±0.7	5	0.6 nJ–60 pJ
	2	4 μs/100 ns	1.04 μs	0.4/−0.3	10	16–0.9 pJ
Ultra short	1	1 μs/50 ns	137.5 ns	±0.9	10	11–0.1 pJ

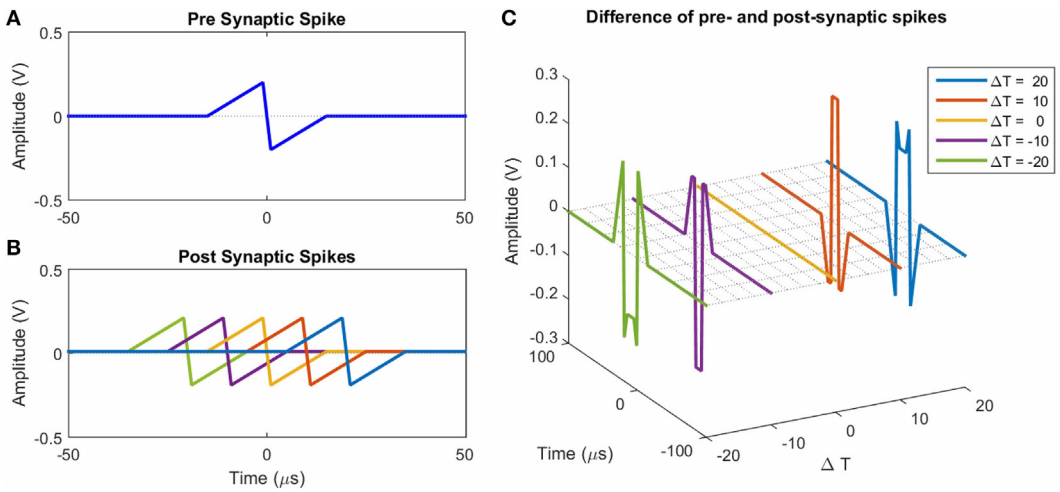

FIGURE 6 | **(A)** An example of a presynaptic spike. **(B)** Examples of postsynaptic spikes. They are at time offsets $\Delta T \in \{-20, -10, 0, 10, 20\}$ from the presynaptic spike in **(A)**. Here they have the same shape as the presynaptic spike. **(C)** Examples of the net (difference) spike for the five cases in **(B)**.

between application of these action potentials, ΔT, rather than engineering specific pulse shapes in order to achieve desirable resistance programing. The resultant potential waveform across the memristor is the difference between the potentials applied separately to each electrode, resulting in a unique effective programing pulse shape for every ΔT. These unique programing pulses will change the resistance of the memristor to an extent that depends on the resultant pulse shape, allowing for a continuous (analog) range of programed resistances over a wide range of pulse widths.

In the STDP experiment performed in this work, a voltage pulse ("spike") is applied to both electrodes of a memristor synapse at varying times, separated by ΔT. The resultant potential difference across the device is the actual programing potential. The STDP synaptic weight change, $\Delta w\%$, is calculated from the initial (R_1) and final (R_2) resistance:

$$\Delta w\% = \frac{\left(\frac{1}{R_2} - \frac{1}{R_1}\right)}{\frac{1}{R_{\min}}} \cdot 100 \qquad (1)$$

where $R_{\min}$ is the minimum resistance (or maximum conductance) measured for the device over all ΔT conditions and is used to normalize the maximum synaptic weight change to 1. The resistances R_1 and R_2 were measured before and after, respectively, a given ΔT test. Thus, a decrease in device resistance with application of the STDP pulses corresponds to $+\Delta T$ in this experiment, and a $+\Delta w\%$. This means that a pulse is applied to the bottom electrode at a time $+\Delta T$ before a pulse is applied to the top electrode.

The four spike shapes used in this work (**Figure 2**) differed by the slope of the rising pulse edge, the slope between negative and positive peaks, and by adding flatness to the positive peak. The tested ΔT time ranges spanned from a maximum ΔT of 1 s to a minimum of 50 ns. **Table 1** provides a summary of the ΔT timing used for each pulse shape. Responses on between 5 and 26 devices were measured for each pulse shape and timing test (as provided in **Table 1**). The results are reported at each ΔT measurement showing the average weight% change over the devices tested with the error bar corresponding to the SD of the data set. Error bars extend from ±½ SD. To clarify, if five devices were measured at every ΔT for pulse shape 1, then the average of the weight% change at a given ΔT (one weight% change at that ΔT for each device, corresponding to a total of five values) was calculated from the five values. The SD was calculated from those five values and used to generate the error bar at that ΔT point on the STDP graph.

Figure 7 shows an example of a resultant waveform produced by application of spikes with shape 1 applied to the top and bottom electrodes of a memristor, separated in time by $\Delta T = 250$ ns. The full-width-half-maximum (FWHM) pulse width is defined on the positive-going portion of each waveform. ΔT is defined as the time between the peaks of the positive-going waveform on the top and bottom electrodes. Note that while there is a large positive peak in the center of the resultant waveform, it is followed by a negative peak, labeled trailing pulse, in **Figure 7**. For the ion-conducting memristors used in this work, the change in resistance is dependent on the electric field induced movement of metal ions within the active device layer. Thus, any portion of the resultant waveform with a potential higher than the minimum value needed move ions within the conductive pathway will change the resistance. Thus, in many ΔT cases, this trailing pulse can have a significant impact on the final device state and is, in fact, responsible for achieving an STDP response. An example of the resultant waveform for pulse shape 2 waveforms for the case of four ΔTs is given in the Supplementary Material, highlighting the regions that are above the switching voltage threshold for increasing or decreasing the resistance of the device.

The STDP test sequence used for each test type starts with $\Delta T = 0$. ΔT is then incrementally increased and cycled between $-\Delta T$ and $+\Delta T$ (thus cycling between an increase and decrease in resistance) up to the maximum ΔT. Between programing steps, the resulting resistance is read. The next programing pulse is then applied to reprogram the memristor. To illustrate, in the Long test (**Table 1**), a portion of the test sequence from the starting point is: $\Delta T = 0$, Read, $\Delta T = -10$ ms, Read, $\Delta T = +10$ ms, Read, $\Delta T = -20$ ms, Read, $\Delta T = +20$ ms, and so on, where the Read is the 20 mV DC measurement to determine device resistance. No attempt is made to reset the memristor to an "initial" state before the next programing sequence is begun.

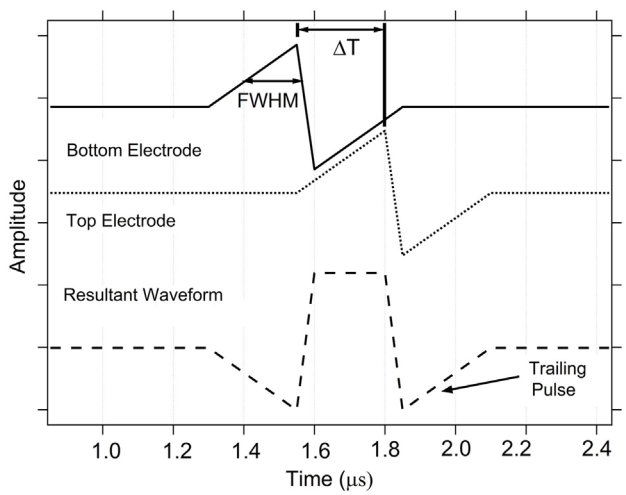

FIGURE 7 | Example spike-timing dependent plasticity action potential spike pair for shape 1 showing the definitions for ΔT and full-width-half-maximum. ΔT defines the time between the peaks of the action potential signals applied to the memristor top and bottom electrodes.

The change in resistance is the desired measurement, and when in operation in a network, the effect of the next pulse pair will be on a memristor that is already in an intermediate state.

In addition to the STDP tests, single-sided spike tests were performed where instead of applying the spike potentials to both electrodes, only the resultant potential difference waveform for a given ΔT was created, and then applied to the top electrode with the bottom electrode held at ground. The purpose of these tests was to verify the dependence of the resultant potential waveform on device programmability and to compare with the STDP test results at the ΔT corresponding to the tested resultant potential waveform. The single-sided tests included a "trailing edge cancelation" test in which the resultant potential amplitude on the last portion of the waveform was reduced (in 25% increments to 100% reduction/cancelation) in order to demonstrate a way to increase the Δw% by a simple pulse modification at a given ΔT.

RESULTS

STDP Spike Shape and Timescale Tests

Time Tests with Pulse Shape 1

Figure 8 shows average STDP test results for five different devices (except for the 50 ns minimum ΔT case which uses 10 devices) using spike pairs with pulse shape 1 over a timescale with a minimum ΔT of 50 ns (upper left graph) and a maximum ΔT of 1 s (lower right graph). The ΔT increment between spike pairs is varied from 50 ns to 50 ms, depending upon the time resolution (**Table 1**). The overall width of the synaptic weight (Δw%) signal corresponds to the ΔT maximum that will still provide overlap between the spikes. Outside of that range, the spikes do not overlap, resulting in a null change in the device resistance.

The STDP results for pulse shape 1 (**Figure 8**) demonstrate the device not only performs well at the biological timescales (milliseconds range), but has similar performance at the computational timescales (nanoseconds range). This demonstrates the versatility of this memristor for a range of applications, including neuromorphic computing. Error bars on the graph correspond to 1 SD and show good device-to-device repeatability, especially at the shorter programing times. As the programing time increases (bottom two graphs in **Figure 8**), there is more variation in the device response and the SD is larger. Two possible factors that may contribute to that observation are: (1) increased Joule heating in the device as a function of current through the device for longer times; and (2) increased times allow more mass movement and thus create a larger distribution of resistances due to differing amounts of moved Ag in the device. In general, the devices respond more consistently to shorter pulses when pulse shape 1 is used.

Time Tests with Pulse Shape 2

Application of spikes with pulse shape 2 over three different timescales produces the STDP results shown in **Figure 9**. Overall the Δw% response curve shape is similar at the different time scales. Spike shape 2 has a flat portion on the top of the positive side of the spike, which produces a different global response of the memristor than was seen for pulse shape 1, **Figure 8**. The flat portion of

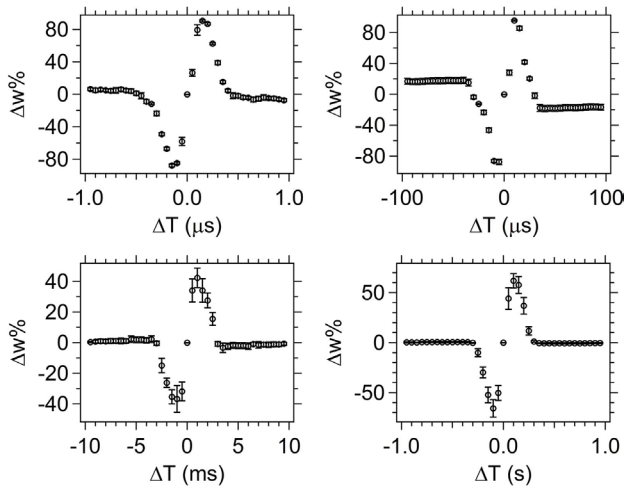

FIGURE 8 | Spike-timing dependent plasticity results for pulse shape 1 with Δ*T* steps sizes of 50 ns, 5 μs, 500 μs, and 50 ms (starting at top left, clockwise). The average weight% change is shown across the set of devices tested (for five different devices, except the 50 ns test which used 10 different devices) with the error bars corresponding to the SD of the data set.

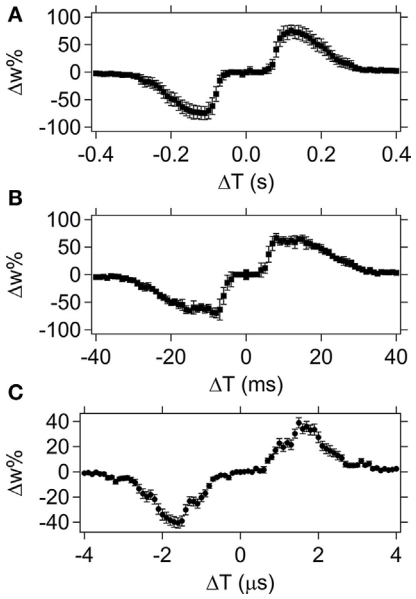

FIGURE 9 | Spike-timing dependent plasticity results for spike shape 2. The Δ*T* increment varies from 10 ms to 100 ns in **(A–C)**. The average weight% change is shown across the set of devices tested [26, 10, and 10 different devices **(A–C)**, respectively] with the error bars corresponding to the SD of the data set.

the spike creates a region around $\Delta T = 0$ for which $\Delta w\% = 0$. This null region is created by the resultant spike difference waveform having a zero potential difference value when the flattened peak on the bottom and top electrode waveforms overlap. This overlap occurs around $\Delta T = 0$ and yields a $\Delta w\% = 0$ segment duration that corresponds to the duration of the flat region on the spike waveform.

The error bars for the shape 2 STDP response are again larger for the longer time measurements (**Figure 9A**), but in general the $\Delta w\%$ response curves are not as well-defined as in the case of pulse shape 1, which is a consequence of the differences in the resultant waveforms.

Unlike pulse shape 1, if pulse shape 2 was used in a computational setting, the pre- and postsynaptic neurons firing within a short time of each other would not change the synapse behavior. This could be an advantage if one needed to suppress a response; simply modify the spike slightly by "clipping" the pulse positive peak and the output would go to zero for the cases of $\Delta T =$ duration of the flattened waveform portion.

Pulse Shape Tests on the Same Timescale

Figure 10 compares the STDP $\Delta w\%$ response curves for pulse shapes 2, 3, and 4. Similar to pulse shape 2, pulse shape 3 creates a $\Delta w\% = 0$ region around $\Delta T = 0$ (compare **Figures 10A,B**). In the case of pulse shape 3, the null region is due to the decreased slope of the transition between the positive and negative peaks compared to the slope that is present in pulse shape 1. This smaller slope again creates a null region in the resultant waveform that corresponds to a $\Delta w\% = 0$ segment during overlap of the spike pairs.

An increase in the slope between peaks for pulse shape 4, compared to pulse shape 1, causes the null region around $\Delta T = 0$ to disappear, and instead a sharp increase in $\Delta w\%$ appears around $\Delta T = 0$ compared to the surrounding ΔT regions (**Figure 10C**). The intensity of the sharp increase in $\Delta w\%$ is directly related to the increase in the slope between peaks.

STDP Single-Sided and Trailing Pulse Suppression Tests with Pulse Shape 1

The resultant pulse for most ΔT has a symmetric shape with a positive (negative) peak, a negative (positive) peak, or zone followed by another positive (negative) peak (see **Figures 6C** and **7**). The memristor will experience a state change if any of the peaks in the resultant waveform exceeds the threshold voltage for writing or erasing. These multiple pulses in the resultant contribute ultimately to the overall STDP response, but it is possible to alter the overall STDP response curve by controlling the potential allowed beyond a threshold voltage. It thus might be desirable for the combined system (neurons and synapses) when doing learning and computation to not experience the later reprograming steps. If a pair of pulses could be found that did not produce multiple peaks, the system could have a more desirable global behavior. The effect of the trailing pulse, which is present in the spike pair resultant waveforms for the case of pulse shape 1 (**Figure 7**), was investigated by choosing one ΔT case and applying the resultant waveform to the top electrode, with varying amounts of suppression in the trailing pulse amplitude.

To investigate the effect of the resultant pulse shape on memristor programing, first it was verified that applying a signal with the same potential shape as the resultant waveform to the top electrode, while keeping the bottom electrode grounded would have the same overall effect as applying the pre- and postsynaptic pulses to the two terminals. The results of this test, **Figure 11**, show the expected similarity in shape and approximate $\Delta w\%$

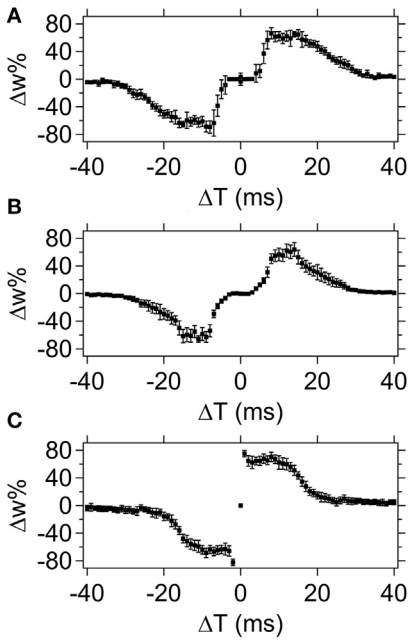

FIGURE 10 | Comparison of spike-timing dependent plasticity results for spike shapes 2 (A), 3 (B), and 4 (C). The average weight% change is shown across the set of devices tested (10 different devices) with the error bars corresponding to the SD of the data set.

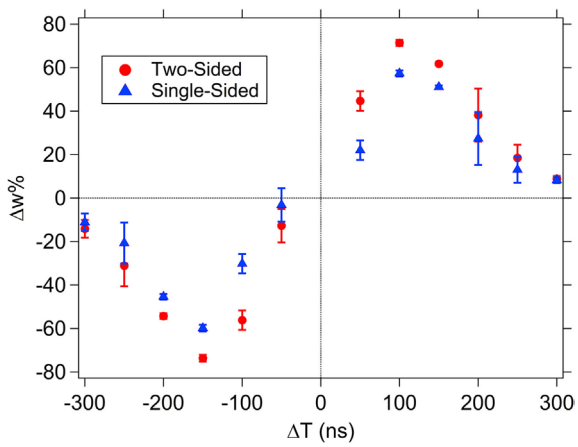

FIGURE 11 | Spike shape 1 single-sided, resultant-only results compared to the spike-timing dependent plasticity (STDP) results using a spike 1 pair (two-sided). The resultant used in each ΔT case of the single-sided test is the resultant waveform expected from the STDP test. The average weight% change is shown across the set of devices tested (10 different devices for the two-sided test and 3 for the single-sided test) with the error bars corresponding to the SD of the data set.

between the normal (two-sided) STDP test with a spike pair and the resultant-only (single-sided) test.

To evaluate the effect of changing the trailing pulse amplitude, a fixed value of $\Delta T = \pm 250$ ns was selected based on the data in **Figure 11**, since they both correspond to regions of low, but non-zero, $\Delta w\%$ so that the effect of altering the amplitude of the

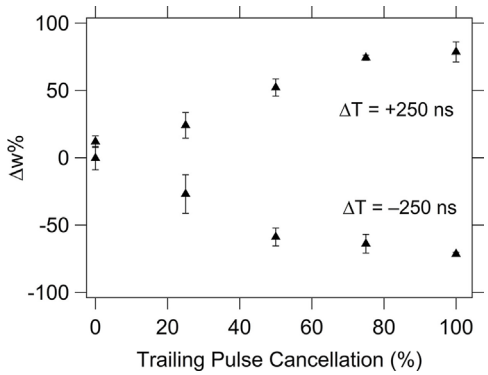

FIGURE 12 | Effects of reducing the amplitude of the trailing edge pulse on the %Δξ for $\Delta T = \pm 250$ ns. The average weight% change is shown across the set of devices tested (10 different devices) with the error bars corresponding to the SD of the data set.

trailing pulse will be obvious. For pulse shape 1, the resultant waveform has values that exceed the device's threshold switching value in both the positive and negative threshold directions (see **Figure 7**), resulting in changes of resistance both higher and lower values during the application of the pulse. The final portion of the pulse, the "trailing edge", sets the total $\Delta w\%$. The full effect of the trailing edge pulse can be seen in **Figure 12** where a suppression of 100% (i.e., the last pulse segment is reduced to 0 V) results in a $\Delta w\%$ that is as high as in the maximum $\Delta w\%$ value during the STDP test (**Figure 11**; this occurs at about $\Delta T = 100$ ns). Partial suppression of the trailing edge pulse results in incremental changes to the $\Delta w\%$.

Energy Requirements

An estimate of the energy required to change the state of the memristor during STDP requires knowledge of the resistance of the device before, during, and at the conclusion of an applied pulse. Additionally, the resultant waveforms do not have simple pulse shapes. Therefore, an estimate of energy necessary to perform a spike induced change on a memristor is difficult for three major reasons: (1) the device resistance is changing during the application of the resultant waveform, both to higher and lower resistances; (2) the energy per pulse is different for every ΔT; and (3) the device resistance can be high initially and change between values of high resistance (lower energy) or it can be low and change between values of low resistance (higher energy).

To get a rough estimate of the energy per memristor, a range was calculated with the worst case assumption that the pulse was a rectangular pulse with an amplitude and pulse width (FWHM) as given in **Table 1**. It was next assumed that the device resistance was constant in a high resistance range of 100–500 kΩ, or a low resistance range of 1–10 kΩ, both ranges that are reasonable for the SDC device (Campbell, 2017). Using these values, the energy per memristor was estimated and is shown in **Table 1**. In all cases, these are most likely overestimates of the energy required. However, they do provide a quick look at the potential order of magnitude energy requirements.

DISCUSSION

Spike-timing dependent plasticity, as developed from Hebbian learning, requires that if the presynaptic spike arrives before the postsynaptic spike that the synapse exhibits long-term potentiation or increased synaptic weight and that if the presynaptic spike arrives after the postsynaptic spike that the synapse exhibits long-term depression or decreased synaptic weight. This effect has been shown for all of the pulse shapes and all the time scales presented in this paper. These change in weight plots do not perfectly match the plots experimentally measured for biologic systems (Bi and Poo, 2001), but since they contain regions of both potentiation and depression, they will be suitable for neuromorphic learning. Through the experiments in this paper, the nature of the potentiation and depression response of this memristor relative to different pulse shapes can be seen.

Neither the null region observed for pulse shapes 2 and 3 nor the spiking region for pulse shape 4, near $\Delta T = 0$ was initially expected since the differences between the pulse shapes are subtle. However, the differences are significant enough to impact the STDP results. This "tunability" of the STDP outcome, based on a slight change in the spike pulse, can be both beneficial and detrimental. Since electronics can be prone to noise, stray capacitance and to device mismatch during fabrication, among other possible interferences, it is possible that the spike pulse generated by the circuit could alter the STDP outcome in an undesirable way. Alternatively, one may be able to use this feature to, for example, suppress a circuit output by adding a slight slope or flat peak to the spike. Either way, this result demonstrates the significant influence the pulse shape can have on the STDP outcome and could prove to be a useful feature for circuit designers.

Because there are essentially an infinite number of possible pulse shapes, and the pre- and postsynaptic pulses are not required to be identical in shape, this study provides guidance to allow the design of pulse shape pairs that will have the desired response. For some applications continuing learning (change in synapse resistance) when there is a large ΔT is desirable, and the range of ΔT to which this continues will depend on the rest of the design components. This was clearly shown in the "trailing edge cancelation" test. In this test, it was shown that a larger ΔT is possible by modification of the resultant waveform so that the trailing edge was completely suppressed. In the event that a circuit designer wants to maintain a higher Δw% in a longer ΔT, suppression of the trailing edge would provide that opportunity. Additionally, partial suppression of the trailing edge pulse could achieve incremental weight changes if desired.

Compared to a pure CMOS implementation of the STDP learning rule, memristor synapses require significantly less area on a chip than an equivalent CMOS-based synapse and are suitable for use in a cross bar array architecture. For example, a switched-capacitor realization of synapses in 28 nm CMOS was developed (Noack et al., 2015), which minimizes the leakage current problems present when CMOS-based architectures are scaled down in size. However, this system requires 0.36 mm^2 area and a power consumption of 1.9 mW for only 128 presynapses and 8,192 "stop-learning" synapses which corresponds to roughly 2.27×10^4 synapses/mm^2 and an energy requirement of 0.23 nJ to 0.23 mJ per synapse. By contrast, 16 Gb ReRAM ion-conducting, chalcogenide-based memory chips have been fabricated at the 27 nm node (Fackenthal et al., 2014) which have a total area of 168 mm^2, including all periphery circuits required of a memory chip, as well as the memory elements. The memory elements on this chip, CuTe-based ion-conducting devices, are actually memristors, thus providing a good analogy to a high density memristor array. Using this entire chip area, a worst case approximation for synapse density would be at least 9.52×10^7 synapses/mm^2, or a factor of 1,000 more synapses per mm^2 than the CMOS-based architecture, even taking into account all of the CMOS circuitry incorporated into the memory chip (periphery circuits and access transistors).

Without knowing the power requirement of the 16 Gb ReRAM chip, it is not possible to know the energy requirement per memristor directly for this chip. However, an estimate of the energy requirements for the memristors used in this work, which are also chalcogenide ion-conductors, is provided in **Table 1** for each experiment conducted and is a reasonable approximation to the energy requirements of the memristors in the 16 Gb ReRAM chip given that they are both chalcogenide-based ion-conducting device types. For pulse timing ranging from seconds to nanoseconds and considering the pulse shapes used in this work, the memristor displays lower energy requirements than the CMOS counterpart. In fact, as the memristor is driven with faster pulses, the overall energy requirement decreases even more (nanojoules to picojoules per memristor). From this, it can easily be seen that two major advantages of the memristor in the STDP application are: (1) denser area achievable and (2) lower energy requirements. In fact, from the energy requirements, it is clear that one of the advantages of operating a memristor on the faster timescale (nanoseconds), even though it is not a biological timescale, is that artificial synapses are not limited to slow, biological speeds and can therefore take advantage of the greatly reduced energy requirements of the memristors at fast speeds.

Even though to date there has been no report of large scale integration of memristors as synapses, it is promising that there has been demonstrated a large scale memory chip which uses memristors (Fackenthal et al., 2014). While this report focused on the ion-conducting CuTe device as a binary memory, this device is a memristor and thus the memory chip does demonstrate the large scale feasibility of memristor incorporation into a large scale CMOS-based integrated circuit. Given this example, the major challenges of integration of new memristor device technologies into large scale integrated circuits can be overcome. These challenges include how to repeatably achieve novel material deposition for device-to-device and lot-to-lot consistency, as well as fundamental issues with trying to access a variable resistance device with transistors which, in the traditional architecture with the memristor in the source of the transistor, do not allow a constant switching voltage across a device due to a voltage divider between the access transistor ON resistance and the memristor.

CONCLUSION

Ge_2Se_3/SnSe/Ag-based ion-conducting memristive devices perform over the seconds to nanoseconds timescale as synapses in an

STDP experiment. STDP tests were performed with four different spike wave shapes in order to demonstrate the influence of the resultant waveforms on the STDP response. This wave shape analysis can be used to help choose the pulse shape to be used in future circuit designs. Furthermore, the ability of the memristor to operate on a large dynamic range timescale, allows for one memristor type to be used for applications requiring short or long timescales. This provides an opportunity for a single integrated circuit to include both long and short timescale applications and to have only one type of memristor that needs to be integrated with the circuit during fabrication. Without this possibility, it would be unlikely that multiple memristor types which catered to different timescales could be fabricated together on one integrated circuit.

The data retention measurements, or lifetime of a particular resistance state after the application of a spike pair, are currently in progress.

AUTHOR CONTRIBUTIONS

KC designed and fabricated the memristor devices, designed the STDP experiments, analyzed the data, and wrote the manuscript; KD performed measurements, wrote instrument control and data collection programs, and analyzed data; ES analyzed data, performed pulse shape simulations, and assisted in writing the manuscript.

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SUPPLEMENTARY MATERIAL

The Supplementary Material for this article can be found online at http://journal.frontiersin.org/article/10.3389/fbioe.2016.00097/full#supplementary-material.

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Conflict of Interest Statement: The authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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