Design and Measurement of Integrated Converters for Belt-Driven Starter-Generator in 48 V Micro/Mild Hybrid Vehicles

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Abstract:
With reference to a 48 V belt-driven starter-generator used in micro/mild hybrid vehicles, this paper shows the design and measurement of an integrated H-bridge and of a compact dc/dc converter, both fabricated in low-cost high voltage-metal oxide semiconductor (HV-MOS) technology. The H-bridge is in charge of rotor excitation and, thanks to a direct copper bonding of the HV-MOS devices on a ceramic substrate, it ensures a full-integrated solution with low on-resistance values. The compact dc/dc converter interfaces the 48 V power domain with the lower voltage domain of sensing and control electronics, such as 5 and 1.65 V in this case study, without using cumbersome inductors and transformers. The latter are difficult to integrate into silicon technology. The converter has a multistage architecture where each stage implements a switched capacitor regulation. Multiple voltage outputs are supported with a configurable regulation factor sustaining an input voltage variation from 6 V (in case of cranking) up to 60 V. Specific design techniques have been implemented to reduce electromagnetic interference (EMI), typical of switching converters. Experimental measurements on fabricated prototype chipsets confirm the suitability of the presented designs for low-EMI 48 V applications.

SECTION I.

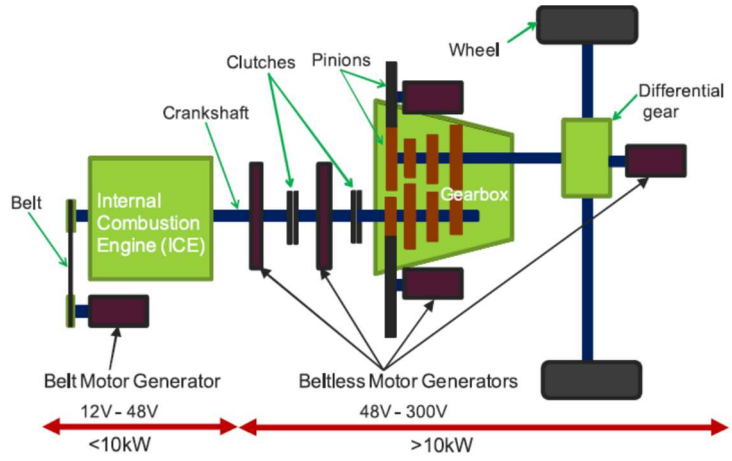
Introduction

To decrease the emission of pollutant gases (CO_2, NOx) emitted in the air, the trend in vehicle industry is the electrification of the power train [1] –[10]. For example, Toyota has recently announced that by 2050, they will cut by 90% all petrol/diesel vehicles. The "dieselgate" in Europe and US [11], on top of restrictive regulations about greenhouse gases, is accelerating the evolution toward electric/hybrid mobility. However, full electric vehicles are expensive, mainly due to battery cost and autonomy. Consequently, their widespread diffusion on the market has still to come. The hybridization of the internal combustion engine (ICE) represents the most viable solution, ensuring a smooth transition.

Electrical machines are used on-board vehicles with a power level ranging from few kWs to hundreds of kWs, such as depicted in Fig. 1. Hybrid vehicles may be realized combining a downsized ICE with a relatively high-power, from ten to hundreds of kW, electric motor. The latter is combined with proper high-voltage drive circuits. The benefit is fuel saving, which is directly linked to CO_2 reduction. However, this approach entails additional costs vs. conventional powertrains. A promising alternative is the design of low voltage micro/mild-hybrid powertrains (<60 V). According to this approach, an electrical machine provides power up to 10 kW [3]–[5] to implement several fuel saving functions: start-and-stop, torque assistance, regenerative braking, fully electric steering, and electrically controlled air-conditioning compressors, to name just a few.

Fig. 1.

Vehicle hybridization trend.



In this scenario, a belt motor generator [also called belt-driven starter generator (BSG)] replaces the conventional alternator without a drastic mechanical change. This BSG approach has a low impact on the ICE compartment layout. Even in the BSG case, the conventional 12 V automotive dc technology is pushed at its limit, since the supplied current would be in the range of 600 A peak current for cranking, thus requiring cables with a high cross section. Since dc voltages below 60 V do not require shock protection, then there is a trend toward the adoption of 48 V (52 V in generator mode) for hybrid vehicles, thus reducing by a factor of 4 the drawn current at equivalent power. To reduce the cost of migrating from ICE-based vehicle generation to new hybrid, or pure electric generations, most of automotive components will be reused. Therefore, one key issue for the electronics of new hybrid vehicle generation is the design of compact dc/dc converters [12]–[20], able to interface the 48 V dc bus to the low voltage supply required by low-power functions/components, with isolation in case of malfunction. These functions/components include sensors, memories, processors, and so on. The design of an integrated H-bridge for rotor excitation is also an issue to reduce the use of discrete devices, thus saving space and cost.

To address these issues this paper first presents in Section II, a BSG architecture for a 48 V micro/mild hybrid vehicle. Section III details the functioning of the 48 V H-bridge for rotor drive and shows experimental results. In Section IV, specifications for the compact dc/dc converter, in charge of supplying low power loads, are discussed. Section V presents the compact dc/dc architecture design, whereas Section VI reports experimental measurement results. Specific electromagnetic interference (EMI) reduction design techniques are presented in Section VII. A comparison of the proposed circuits vs. the state-of-art and the conclusion are drawn in Sections VIII and IX , respectively.

SECTION II.

48 V Power System for Micro/Mild Hybrid Vehicles

Fig. 2 shows the vehicle electrical architecture including the BSG unit, which receives the power from the 48 V battery pack subsystem and receives proper command/configuration signals, through local interconnect network (LIN) and/or controller area network (CAN), from a low-voltage low-power electronic control unit (ECU). The latter is connected

through a backbone vehicle network, e.g., CAN or Flexray, to the other vehicle ECUs. The core of the BSG is a synchronous machine and its dedicated electronics (see Figs. 3–9). As reported in the scheme of Fig. 3, the electrical machine features a double three-phase stator and a wounded rotor. It has been implemented, within the Athenis3D EU project, with different levels of integration, see prototype in Fig. 7. The power range of the current BSG machine is 0–8 kW with a peak of 15 kW. For the electronics, there are two powers parts.

1. The stators connected to power modules, including six MOSFETs transistors for each stator, which can act as inverter or rectifier. They are used for synchronous rectification in case the power system is working in generator mode and as pulse-width modulation/full wave (PWM/FW)-based dc/ac inverter in case the power system is working in motor mode.

2. The rotor current control, which in Fig. 3 is managed by an H-bridge using two power MOSFETs and two diodes (often replaced by MOSFETs, as in Fig. 4), with PWM control signals applied on the gates of the transistors. A full H-bridge is necessary for rotor current control for fast demagnetization in case of load dump, and also to ensure safety against overvoltage in case of component failures. To this aim, in the final schematic of the fabricated BSG machine, a full H-bridge solution with four MOSFETs has been adopted, see further details in Section III.

Fig. 2.

48 V starter alternator interfaced to the in-vehicle network.

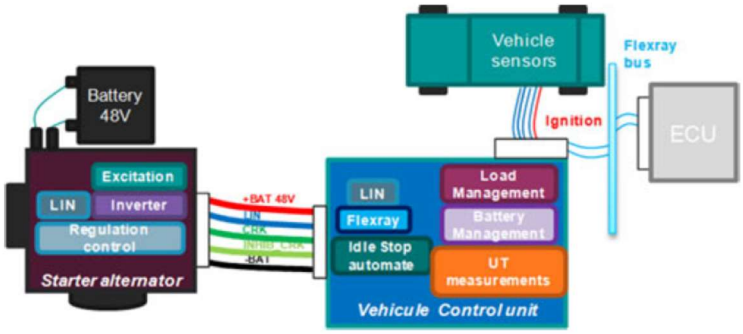


Fig. 3.

Electronic circuitry for the 48 V belt-driven starter generator.

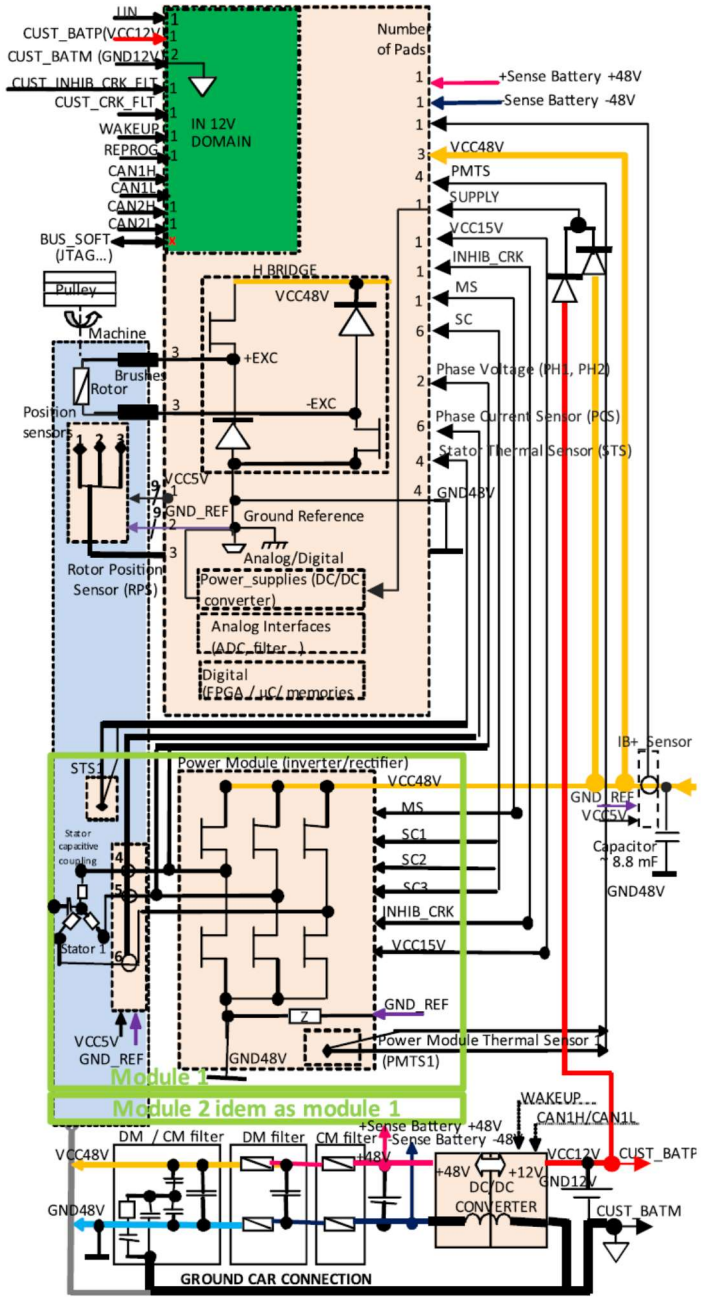
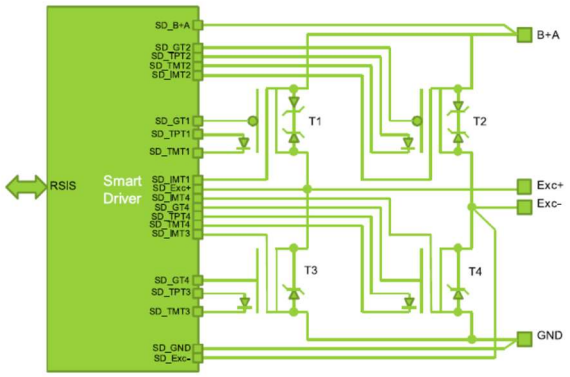


Fig. 4. Rotor control.



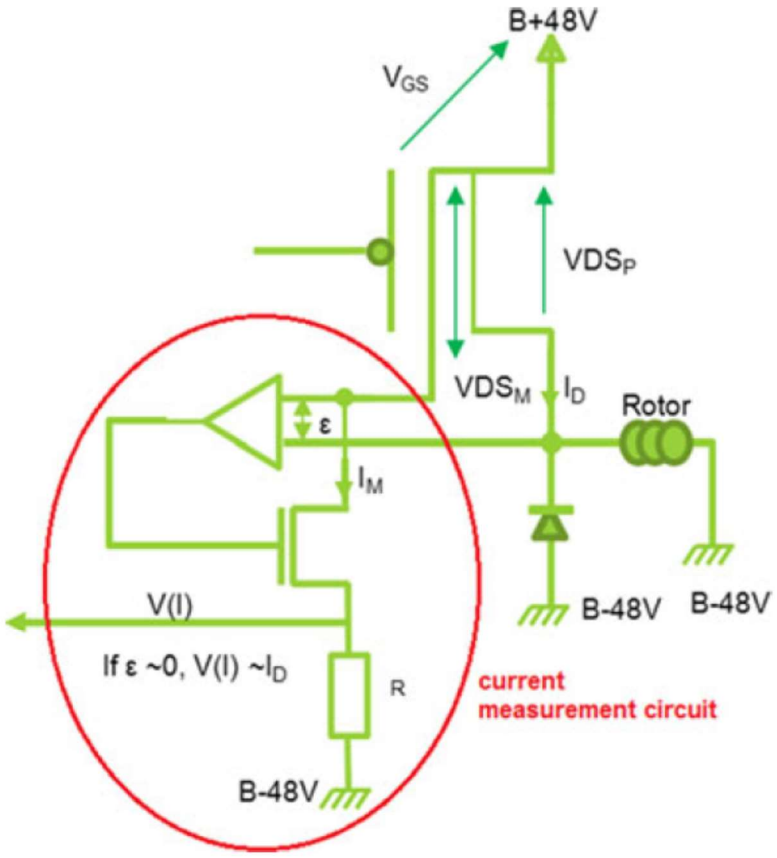


Fig. 5. Power MOSFETs current measurement principle.

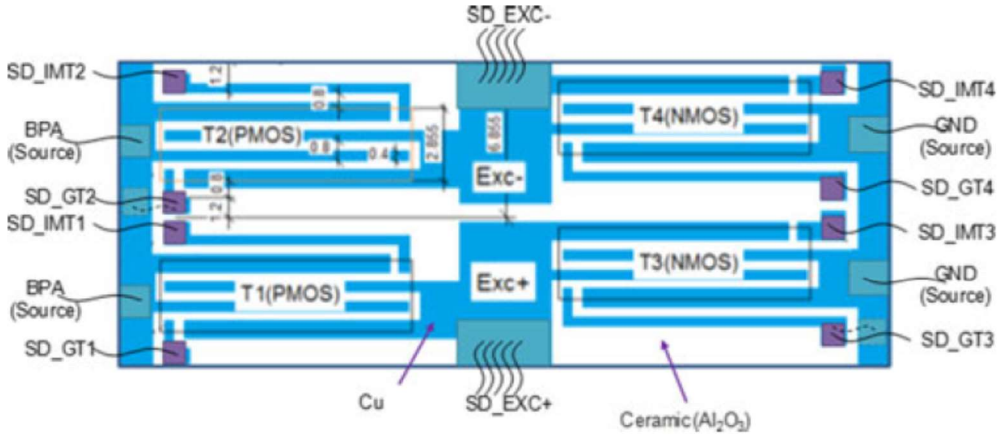


Fig. 6. Layout of the DCB board.

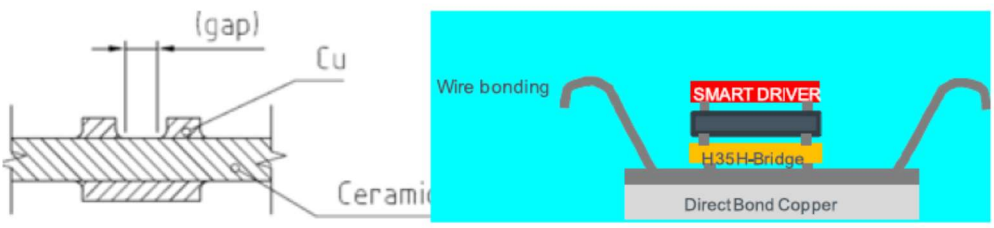


Fig. 7. Distribution of Cu on both front/back side of the DCB board and 3-D stacking aim on direct bond copper.

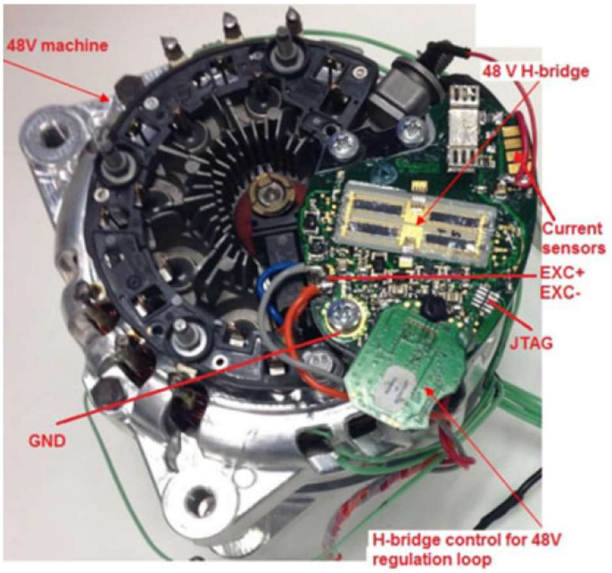


Fig. 8. Implementation of the 48 V belt-driven starter generator electrical machine plus control and sensing electronics.

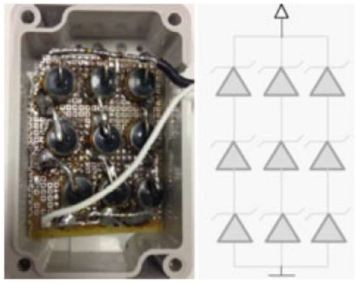


Fig. 9. Diode bridge for 63 V clamping (machine protection).

In Fig. 3, the control electronic is split in two domains: the 48 V domain dedicated to the rotor and stator control and the 12 V domain used for the ECU. The controller in the 48 V domain generates all signals needed to drive the 12 power MOSFETs of the two rectifier/inverter stages for the two three-phase stators. It also generates the command signals for the power MOSFETs used in the H-bridge to control the rotor current. To be noted that the 48 V part also includes analog and digital circuits used to interface all sensors in stator and rotor control such as: stator thermal sensors, phase current sensors, phase voltage sensors, rotor position sensors, and power module thermal sensors.

From an algorithmic point of view, the electrical machine, whose scheme is proposed in Fig. 3, can be controlled either with standard voltage loop control, as in [9], or by a closed-loop flux vector control [8]. To implement the selected control algorithm in the scheme in Fig. 3, a field programmable gate array (FPGA) is used. With respect to classic microcontroller solutions, the use of FPGA as control processor offers a better trade-off between computational flexible capability, area, and power consumption. FPGAs are also available as AECQ-100 automotive qualified devices. Analog, digital, and power devices have to be also integrated into the same platform, realizing an embedded mechatronic system.

In our study, the focus is on the control module composed of MOSFETs, which controls the current through the rotor of the electrical machine. The principle described in Fig. 4 is to control each transistor (Tx) during switching and off/on modes taking into account temperatures (TPTx–TMTx) and currents (IMTx). The smart driver in Fig. 4 is also able to detect leakage, transistor failures, over-currents, and over-voltages and acts to avoid any failure or unsafe behaviors.

The principle of the direct current measurement on each transistor of the H-bridge is implemented through the circuit in Fig. 5, which exploits a current mirror with a V_{DS} control loop. This is possible by using power MOSFETs (a P-MOS for example in Fig. 5) where a part of the drain is connected to the current measurement circuit where a current I_M (proportional to the power MOSFET current I_D) is flowing.
Another innovation in this work is the use of direct copper bonding (DCB) approach for the 48 V H-bridge. Indeed, within the Ahenis3D EU research project supporting this work, at system level stringent requirements have been defined on the on-resistance of the H-bridge switches. The on-resistance should be reduced at least by a factor 5 vs. the H-bridge of the previous Athenis EU project in [21] [implemented using the same Austria Micro Systems (AMS) high voltage-metal oxide semiconductor (HV-MOS) 0.35 μm technology of this work] where a 12 V electrical machine was designed. To achieve low on -resistance values, it is not only a matter of increasing the silicon area of the MOSFETs to reduce the relevant drain source resistance when the transistor is ON (RDSON), but reducing the resistance of the connections among the transistors and the electronic board on which the power and control circuits are assembled is also important. In this work, to realize the low ohmic 48 V H-bridge transistor connections, a DCB board has been realized, whose layout is shown in Fig. 6. This interconnect plate uses an Al_2O_3 ceramic substrate with electroplated copper. The board thickness is about 0.38 mm while the copper thickness is about 0.3 mm with a surface plating for die stacking with a 5 μm Ni and 0.03 μm Au layer. In the layout of Fig. 6, each transistor chip is connected with four lines (two source lines and two drain lines) to the board. A stress analysis carried out on the 48 V H-bridge (transistors in 0.35 μm HV-MOS technology with DCB connection to the board) to operate at high temperatures (up to 175 °C) shows that the uniform distribution of Cu on both front and back sides of the DCB board is important. This has been realized as shown in Fig. 7 with the objective of the final product to have a stacking for components. Based on the different developments, a synchronous machine mock-up in Fig. 8 is assembled, made of rectifying diodes, four MOSFETs on DCB, controlled by a simple FPGA acting as a smart driver.

To protect the BSG machine in case of overvoltage, the 63 V clamping circuit in Fig. 9 has been realized, using three serial 21 V zener diodes. The new BSG machine has been integrated for test on a Peugeot 308 hybrid vehicle. The main differences of the proposed BSG machine vs. the conventional car's alternator in [9], [21] are as follows:

1. use of a six-phase-synchronous 48 V machine, with 12 Ω wounded rotor;

2. voltage regulation loop at 48 V instead of 12 or 14 V;

3. use of external zener diodes clamp for protection at 63 V;

4. Different machine control strategies can be implemented by proper FPGA programming; and

5. with two stators there is less current in each stator allowing smaller copper winding; moreover, the two stators are electrically shifted by 30° with the consequence of less ripple on the output rectification.

SECTION III.

Measurements of 48 V H-Bridge Rotor Drive

In order to verify the H-bridge circuit in Fig. 10, a simple PWM control signal is applied on T1, while T4 is on and the load connected on EXC+ and EXC– is a pure rheostat. In Fig. 10, the T2's gate is always connected to B+A node, thus acting as a diode. The switching voltage and current in Fig. 11 are measured to verify Ohm's law, and RDSONs are also evaluated in order to comply with dissipated power capability.

Fig. 10.

H-bridge schematic.

Fig. 11.

Measured example waveforms for 48 V rotor control.

To be noted that the H-bridge supply voltage is nominal 48 V (52 V in generator mode) whereas the rotor currents are in the range 0–12 A (up to 17 A transient). The four transistors of the H-bridge in Fig. 8 are realized in AMS HV-MOS 0.35 μm technology, with DCB on ceramic substrate, as two P-MOSFETs for the high side devices (T1 and T2) and two N-MOSFETs for the low side devices (T3 and T4). The minimum on-resistance, with a 5 V gate–source supply for the transistors, is 8 mΩ for N MOSFETs and 11 mΩ for P MOSFETs. Using P-MOSFETs as high side devices in the H-bridge entails a higher on-resistance vs. N-MOSFETs, but avoids the use of complex charge-pump circuitry.

The performance parameters of the integrated H-bridge well compare to state-of-art of integrated devices for rotor coil drive, see Table I. The sustained current is increased by a factor of 2.5, the sustained voltage is increased by a factor 4, and the on-resistance is reduced by a factor 6 vs. the H-bridge of the previous Athenis EU project in [21], implemented using the same HV-MOS technology. The improved performance of the H-bridge vs. [21] (×2.5 higher current, ×4 higher voltage, and ×6 lower on-resistance) has been achieved by increasing the transistor area and by adopting the DCB approach, missing in [21]. With DCB the transistors are assembled on top of the ceramic substrate. Hence, DCB allows a reduction of the printed circuit board (PCB) size with respect to board layouts where large conductive plates are placed around the chip to achieve low-ohmic contacts [21] . Since in this work the electronics is tightly coupled with the 48 V BSG electrical machine (see Fig. 8), and the adopted 0.35 μm technology is a low-cost one, and the DCB approach allows a reduction of the PCB size, then the increased transistor area is not an issue.

TABLE I H-Bridge for Rotor Drive, From Athenis to Athenis3D Project

Instead of a rheostat, a rotor is connected for the test in Figs. 12–16. Fig. 12 shows measured magnetization (1) and demagnetization (2) configurations during rotor control with the designed H-bridge. To generate the current into the rotor, the magnetization mode is activated when T1 is put on at high duty cycle and T4 is always on (red plain path in Fig. 10). To maintain the required current in the rotor, the H-bridge is set on

freewheeling diode (FWD) phase: T1 is put off at low duty cycle, T3 acts like a diode, T4 is always on (red dashed path in Fig. 10). If the losses are small compared to the magnetic power, the current has few variations around the average. The fast demagnetization acts with reverse B+A voltage applied on the rotor. In the first step T1 is off, T3 acts like a diode or T3 transistor is on, T4 is on. In the second step, T4 is put off then T2 diode acts as on as shown by the green path in Fig. 13 . Fig. 14 depicts the fast demagnetization (3) where the current reaches zero. When fast demagnetization stops and the demagnetization remains (4), the current re-increases due to internal magnetic field still present. Fig. 15 shows another configuration. With T1 on there will be first a magnetization of the rotor, then a freewheeling phase. To decrease the losses in T3, and hence its temperature, the FWD improved low-losses path can be activated when T1 is off at duty cycle, T4 always on, T3 on (orange path).

Fig. 12.

Rotor current control (magnetization).

Fig. 13.

Fast demagnetization path.

Fig. 14.

Rotor current control (fast demagnetization).

Fig. 15.

Improved losses.

Fig. 16.

Rotor current control (improved free-wheeling diode).

In Fig. 16, when T3 diode is on (2, 2a), T3 transistor is activated and T3 diode is shorted (2b) by RDSON. Note that the condition is: RDSON$*I^2$ smaller than Vforward$*I$, i.e., RDSON$*I$ smaller than V forward. This condition is true in our case since RDSON is limited to 11 mΩ for the MOSFETs. With a rotor current of 10 A the voltage drop will be 110 mV.

From a thermal point-of-view, the BSG thermal range is from –40 to 125 °C (ambient), whereas the stator has been tested up to 250 °C, the rotor up to 180 °C, the power electronics up to 175 °C, and the low-power electronics (e.g., sensors, control unit) up to 150 °C.

SECTION IV.

Compact dc/dc Converter Specifications

To provide power supply to the sensors, and to the hardware implementing the control unit, in the scheme discussed in Section II, a dc/dc converter is needed. It converts 48 V in lower values, such as 5 or 1.65 V. Since electronic devices are placed near the power electric machine, there is the need of a strong integration to keep low the size and the cost of the final product while increasing reliability. Beside high-density of integration, also

other constraints have to be considered [22]– [34] for operation in harsh automotive environment, such as vibrations, temperature, EMI, over-voltages, and over-currents.

The state-of-art of dc/dc converters is dominated by switching converters, using large off-chip inductors to filter the undesired switching frequency, thus reducing distortions and ripple at the dc output. Large transformers are also used to provide galvanic isolation between input and output domains.

The lower the output ripple and harmonic distortion specification, the higher the inductor values to be used. Large inductors lead to systems with a large size, weight, and cost, since they cannot be integrated into semiconductor devices and require ferromagnetic cores.

Another issue, due to safety requirements, is to avoid 48 V propagating in case of failure, weeding out the use of dc/dc converters without transformers. Moreover, in case of cranking at the key "on," the battery voltage may drop from 48 to 6 V. Due to over-voltage, the battery voltage can also increase to about 60 V (the protection circuit in Fig. 9 clamps the maximum voltage to 63 V). The required output currents in the considered case study are 20 mA, for the 1.65 V loads, and 0.3 A for the 5 V loads. Inductorless linear regulators, also known as low drop-out (LDO), since are typically used with low Vout/Vin ratios, have a poor efficiency ($\eta \leq V$ out/Vin) when trying to regulate a low output voltage from a 48 V input voltage. The efficiency η is lower than 3.5% and 10% when supplying 1.65 and 5 V output loads, respectively.

To address all the above-mentioned issues, Section V presents an innovative architecture with an inductorless dc/dc converter where power efficiency is kept high by using a cascade of switched-capacitor circuits. Developed by an industry-academia collaboration within the Athenis3D EU funded project, the work has been patented in [35]. Since automotive regulation poses stringent constraint on radiated EMI in the frequency range above 100 kHz, then a main switching frequency of 90 kHz has been specified. Prototype samples of the dc/dc converter integrated circuit (IC) have been fabricated in 0.35 μm HV-MOS technology. The IC samples have been tested through experimental measurements in real automotive environment. Section VI reports the measurement results.

SECTION V.

Compact dc/dc Converter Architecture

A. Cascade of Switching Capacitor and LDO Stages

An innovative 48 V dc/dc converter architecture is proposed in this work, using a switching technique to keep high the power efficiency, but avoiding inductors and transformers and adopting specific techniques to limit EMI issues. The 48 V dc/dc converter adopts the multistage architecture shown in Fig. 17. It is composed by three switching capacitors (SC) stages: dcdc1, dcdc2, and the isolator block. At the end of this cascade, two final linear converters are used (LDO blocks in Fig. 17). The whole circuit has been first designed and simulated in all process-voltage-temperature corner cases, at layout level, in Cadence CAD environment. Then, the dc/dc converter IC has been fabricated in 0.35 μm HV-MOS AMS technology with transistors operating up to 70 V at a main switching frequency of 90 kHz. The frequency value has been derived after the EMI analysis in the automotive environment. The isolator block works according to the circuit in Fig. 18, whose principle of operation is inserting one or several serial capacitors voltage to ensure proper insulation. In Fig. 18, the isolation between input and output voltages is

done with the two capacitors in series (C1 and C2) instead of using a transformer, as in the flyback dc/dc converter used in the state-of-art 14 V StARS and 48 V i-StARS designs [9], [10]. The behavior of the circuit in Fig. 18 is based on two clock cycles: 1) when the red switches G0, G2, G4, and G6 are on; and 2) then C1 is loaded by the battery and C2 supplies the load. In this case, input and output have no connection and in case of a malfunction at the input there is no risk of overvoltage at the output. Instead, when black switches G1, G3, and G5 are on, the charge is transferred from C1 to C2. In this case, C1 is not connected to input and C2 is not connected to the output. Hence, input and output have no connection and in case of a malfunction at the input there is no risk of overvoltage at the output. Summarizing, in Fig. 18, if at least one switch (or more) fails, there is no possibility to have overvoltage at the output. To be noted that the buffer capacitor C3 in Fig. 18 is used to ensure a stable output voltage.

Fig. 17.

Multistage architecture of the 48 V dc/dc converter.

Fig. 18.

Insulated dc/dc converter principle.

To keep the power efficiency comparable to that of conventional dc/dc switching converters using inductors, in our design the jump between input and output voltages is realized in multiple cascade stages, see Fig. 17. Indeed, in switched capacitor power converters the use of large ratios between input and output voltages would lead to poor efficiency values. The aim of the first three stages in Fig. 17 (dcdc1, dcdc2, and the isolator block) is regulating the input voltage to an output value of about 6 V. From this value, thanks to point of load LDO regulators, the desired low voltage outputs, 5 and 1.65 V in this case, are obtained. The output linear regulators provide optimal performance in terms of ripple, line, and load regulation capability, low power supply rejection ratio (PSRR). Since this work uses a switching approach to regulate from high voltage (48 V nominal) down to 6 V, the low efficiency of linear regulators is avoided. Regulating from 6 V, the linear regulator for the 5 V output has a theoretical efficiency of about 83.3%. The linear regulator for the 1.65 V output has a theoretical efficiency of 27.5%. To be noted that in the 1.65 V case, the current to be drawn, 20 mA, is one order of magnitude lower than the 300 mA delivered at 5 V. Hence, in terms of efficiency of the overall dc/dc converter, the main contribution is due to the 5 V LDO. Considering also the losses in the switching converter stages and in the LDOs, the expected measured efficiency, as confirmed by measurements reported in Section VI, is 60% at maximum. Therefore, from a theory point-of-view, the proposed design is suitable for the conversion of 48 V automotive power supply to low voltage outputs (typical of sensors, processors, memories used for sensing and control tasks on-board a vehicle) and requiring limited power budget (e.g., 1.5 W that is to say 0.3 A at 5 V). Under such conditions, the proposed design offers much higher efficiency than linear regulators (see Fig. 28), and much lower size than the inductor-based switching converter. For example, in the state-of-art, the inductor-based PT4667 dc/dc switching converter in [22] regulates an input of 48–5 V (75 mV ripple) and 1.8 V (50 mV ripple) at the output with an efficiency of 70% (at 1 A output current). Its PCB area occupation is 2 in^2, i.e., about 13 cm^2. Instead, the proposed switched cap dc/dc converter design avoids the use of inductors, and relies only on capacitors of few μF. As proved by implementation data in Section VI, this allows for a compact PCB realization with a ×5 area saving using surface mount device (SMD) capacitors mounted beside the dc/dc converter chip directly bonded on the PCB. The proposed design also enables future system-on-package implementations with an area occupation below 0.5 cm^2 (one order of magnitude lower

than [22]) where trench capacitors are integrated into passive interposers [36], assembled in three-dimensional (3-D) fashion with the dc/dc converter chip.

With reference to the cascade architecture in Fig. 17, while the isolator block exploits the circuit schematic in Fig. 18, the dcdc1 and the dcdc2 blocks work according to the circuit schematic in Fig. 19. This circuit implements a two-phase serial–parallel inductorless converter. The switches from S0 to S4 are realized through HV-MOS transistors in the AMS 0.35 μm technology, sized to sustain a voltage drop up to 70 V. By proper controlling the switches from S0 to S4, and exploiting the flying capacitor C_{fly} , the possible regulation factor K is 2, 1, 1/2 for dcdc1 stage, or 1, 1/2, 1/3 for the dcdc2 stage. The isolator block instead is controlled to reach conversion factors 1 or 1/2.

Fig. 19.

Basic circuit of the switching capacitor stage.

The regulation capability of the implemented switching converter stages is modeled by (1). This equation derives by the fact that a switched capacitor converter, under stationary conditions, can be seen as an ideal dc/dc converter with a conversion ratio K (i.e., Vout = K·Vin) plus an equivalent output resistor, Rout=1/(Cfly·n·fsw), that represents all losses. Such losses, in a switched capacitor converter, depend on the value of the flying capacitor Cfly (in the isolator block the role of Cfly is managed by the series of C1 and C2 in Fig. 18), on the switching frequency fsw, and on a parameter n depending on the selected topology and circuit implementation. The conversion ratio K depends on the selected topology too. As consequence, the overall conversion ratio of the cascaded architecture in Fig. 17 can assume discrete values according to the product of the conversion ratios of each stage. To be noted that the parameter n in (1) does not influence the conversion ratio, but rather the losses. For example, with reference to the architecture in Fig. 17, the stage dcdc1 (implemented through the circuital scheme in Fig. 19) can implement the conversion ratios K indicated in Table II, which also reports the switch status. At the end of each switching stage a buffer capacitor, Cbuffer in Fig. 19, C3 in Fig. 18, is used to improve line/load regulation performance. In Fig. 17, by cascading the multistage dc/dc switching core with the LDOs, the regulation performances of the conversion system are further improved. For the LDOs, integrated architectures we already proposed in the literature have been adopted

$$\text{Vout} = \text{K}\cdot\text{Vin} - \text{Iout}/\text{left}(\text{C\_rmfly cdot n cdot f\_rmsw right}). \quad (1)$$

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TABLE II Switch Status for DCDC1 Stage

B. Control Algorithm

The switching phases are generated by an on-chip control unit, starting from a ring oscillator operating at 32 MHz (not shown in Fig. 17). The control system plays an important role by changing the operative mode of the converter. Two control algorithms are implemented to keep a high efficiency and to control the desired output voltages: 1) conversion ratio reconfiguration; and 2) skip-mode control (SKIP).

The conversion ratio reconfiguration technique changes the value of K for each stage in function of the input voltage. For example, the first stage can be driven to implement the ratios ×2, ×1, ×1/2. Considering a constant output current, the maximum request of input charge is when the converter (dcdc1 in this case) works as step-up (K = 2).

The control system drives each switch of the converter with a synchronous digital signal according to system condition and input voltage. These control signals change to obtain the different converter topologies and so the different values of *K*. The SKIP algorithm works independently from the converter topology and basic switch control (as for example in Table II). When the output voltage of each stage in the cascade of Fig. 17 is above a fixed value, then the duty cycle of the signals used to drive that stage stops following the usual timing (e.g., that reported in Table II and following two phases each of equal duration). Instead, the switches are forced to be off in all phases. The SKIP control works independently for each stage. Integrated comparators are used to detect out-of-range voltage values at the output of each stage. Using two different nested algorithms (conversion ratio configuration and SKIP-mode) it is possible to control the output voltage keeping a high efficiency.

The effect of the SKIP algorithm is expanding the spectrum components in a wider frequency range, reducing the harmonic peaks. By spreading the generated electromagnetic noise, the EMI performance of the circuit is improved. This effect is displayed in the MATLAB simulation results reported in Fig. 20 (without the SKIP technique, but using only conversion ratio configuration) and Fig. 21 (with the SKIP technique). The harmonic values are reduced using the SKIP control technique: the first harmonic value in Fig. 20 is reduced 6.536 dB vs. that in Fig. 21, whereas the second 5.803 dB and so on. This effect is also observed with experimental measurements.

Fig. 20.

Simulation results obtained without the SKIP algorithm.

Fig. 21.

Simulation results with the SKIP algorithm.

C. Soft-Start

Beside the control algorithms discussed in Section V-B, a soft-start technique has also been integrated within the dc/dc converter. One of the most critical phase of a switching converter is the wake up phase. At wake up, the capacitors of the switched capacitor stages in Fig. 17 (dcdc1, dcdc2, and the isolator) are discharged. This situation, combined with the low resistances of MOS switches, leads to high current peaks that create high disturbance values. These currents can be one order of magnitude higher than steady-state currents, e.g., 5.6 A in the considered case study vs. steady-state currents which are below 0.5 A. These current peaks, during the converter-awakening phase, lead to high levels of disturbance on the power line. As consequence, all the other devices connected at the same power source suffer from this effect. Additionally, these so high current spikes can damage the converter reducing its reliability. To realize a soft-start of the converter, in the proposed design, we increase the resistance of the switching elements during the awakening phase. The idea is realizing the power switches of the converter stages as multiple MOSFETs working in parallel. By proper controlling the number of transistors that are activated, we can control the resistance value of each switching element. The resistance value is increased at the starting phase, to reduce high current peaks, and is decreased at the steady-state, to improve the converter efficiency. The lower the number of parallel transistors activated, the lower the current in the wake-up phase. Therefore, the gates of the MOSFETs are driven separately and only some of them are enabled at the converter wake-up. The control of the number of active MOSFETs, and of the transition

from soft-start to normal mode, is done as a function of the input current, measured through a shunt resistor, and compared to proper thresholds.

SECTION VI.

Compact dc/dc Converter Measured Results

The whole dc/dc converter in Fig. 17 has been integrated into the 0.35 μm HV-MOS technology requiring an area of 6 mm × 6 mm. The chip area is pad limited. Indeed, big pads are used to easy a direct bonding of the chip on the testing PCB, see Fig. 22. To avoid the influence that different packages have on the measures, a bare glued chip is bonded directly on the PCB. The chip is also available with a 24-pin ceramic dual in line package. On the testing board in Fig. 22 some external passive components are used: C_{fly} and C_{buffer} capacitors of the switching stages, capacitors of the isolator block, capacitors of the output low-pass filter of the integrated output linear regulators. The values of these capacitors are from 50 nF to maximum 10 μF. In addition, a removable input filter (components C _filter, C_filter2, L_filter, and R_filter in Fig. 22), designed to reduce conducted EMI, is inserted with some measure points. Particularly, according to (1), the value of C_{fly} can be determined as a trade-off between its size and the losses. Indeed, the higher the C_{fly}, the lower the losses in (1). In this work, f_{sw} was set at 90 kHz due to EMI considerations done by Valeo (to avoid irradiative EMI issues a value below 100 kHz has been selected). Hence, with a conversion ratio ×1/2, a voltage drop of about 50 mV (when the output load current is 100 mA) is obtained with C_{fly} of 5 μF. To be noted that the board in Fig. 22 is bigger and with more measurement points than required, since it is a testing prototyping board. In case of production, its size can be reduced at about 2.5 cm^2.

Fig. 22.

dc/dc converter test board with direct bare chip bonding.

In the dc/dc converter chip, a sleep mode has been inserted to increase the efficiency. The current consumption in sleep mode is below 5 μA. To test this feature, two power supplies are used during experimental measurements, see Fig. 23. One power supply is used to simulate the 48 V battery system, whereas the other is used to generate the digital signal, Power_On (0–12 V), that wakes the converter from the sleep mode. When the Power_On signal is set, then the internal oscillator, the digital control block, and the converter stages are activated and a digital signal, dc/dc_Status, indicates that the output voltages are regulated and meet the constraints. Figs. 24 and 25 show for the 5 and 1.65 V outputs the results achieved in terms of line regulation, when the input voltage changes from 6 to 60 V around the nominal 48 V value. Different current load conditions are considered: 0–0.3 A for the 5 V output, 0–20 mA for the 1.65 V output. The strange behavior for input voltages below 9 V in Fig. 24 is justified by the fact that the reported figure was obtained controlling the Vin range from 6 to 9 V with a conversion ratio ×2/3 (×2 the dcdc1, ×1/3 the dcdc2). This way 6 V becomes nominally 4 V and 9 V becomes nominally 6 V at the input of the LDOs. Due to losses in the LDO and in the dc/dc converter, see (1), the output voltage can further drop down: e.g., 3 V at 6 V input with 300 mA in Fig. 24. This issue does not appear in Fig. 25 for the 1.65 V output. The battery drop from nominal 48 to 6 V is an exceptional case, but still our converter is able to regulate an output voltage higher than 4 V (instead of 5 V nominal) if the current load is up to 150 mA. By selecting a different regulation factor for the dcdc2 stage (e.g. ×1/2) the input range 6–9 V becomes nominally 6–9 V at the input of the LDOs. Hence, the output voltage drop in Fig. 24 is

reduced, but at the cost of a lower efficiency (since we have up to 9 V at the input of the 5 V LDO and of the 1.65 V LDO).

Fig. 23.

Testing set up for the dc/dc converter.

Fig. 24.

Measured line regulation for 5 V output.

Fig. 25.

Measured line regulation for 1.65 V output.

Figs. 26 and 27 show for the 5 and 1.65 V outputs the results achieved in terms of load regulation, when the current load is varied within the above discussed ranges and *V*in is stable. Three different *V*in values, of interest for automotive applications, are considered: 12, 24, 48 V. The results in Figs. 24 and 25 show the capability of sustaining a large voltage sweep, one order of magnitude from 6 to 60 V. Figs. 26 and 27 show a 2% maximum output voltage variation vs. nominal value (at 48 V *V*in) under every current condition.

Fig. 26.

Measured load regulation for 5 V output.

Fig. 27.

Measured load regulation for 1.65 V output.

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The efficiency of the converter has been determined as the ratio between measured output power and input power. Fig. 28 shows the achieved efficiency as a function of input voltage for different load currents. The efficiency of an ideal linear regulator is also reported for comparison. The behavior in Fig. 28 is typical for switched capacitor converters, where every peak represents the changing of the conversion ratio, which, as discussed in Section V-B , assumes discrete values. The efficiency values are higher for higher output current levels, between 40% and 60%. These values are lower than those achievable with inductor-based converters. This is also due to the presence of the integrated LDOs. However, the achieved efficiency is much higher than that of ideal linear regulators, below 10% for an input voltage above 48 V. The proposed converter can be seen as a trade-off between inductor-based switching converters and linear ones. It is suitable to regulate 48 V to low output voltages with load currents below 1 A.

Fig. 28.

Converter efficiency results.

The PSRR of the converter is measured under real operative conditions in an automotive environment. The frequency of the electric engine, in hybrid/electric vehicles, changes with the velocity but it is around 300 Hz under normal condition, so a sine disturb of big value (10 Vpp) at that frequency is added to the input voltage. This is made using a

waveform generator and an amplifier, designed to work at high voltage with an offset upper 45 V. The PSRR results in Table III highlight that the converter has a very good PSRR performance, for wide input voltage range and considering typical automotive disturb frequency. In Fig. 29, temperature measurements in a Thermostream thermal chamber show that under typical operating conditions (48 V input voltage, total current delivered to the 1.65 and 5 V loads up to 0.4 A) there are no thermal dissipation issues. Indeed, in Fig. 29, the chip temperature (measured by directly contacting the naked chip in Fig. 22) is below 45 °C with nominal 48 V conditions (T1 in Fig. 29) and always below 60 °C when operating under 60 V overvoltage conditions (T2 in Fig. 29).

TABLE III PSRR Result in Automotive Conditions

Fig. 29.

Chip temperature measurements vs. load current under different conditions: nominal 48 V input (T1) and overvoltage 60 V input (T2).

SECTION VII.

EMI Reduction Techniques and Measurements

In the proposed dc/dc converter, three main techniques are implemented to reduce the EMI: the design of an anticonductive EMI filter, the soft-start technique, and the skip-mode control algorithm. The sizing of the anti-EMI filter, whose topology is presented in Fig. 30, has been detailed by Saponara *et al.* [37] and has been implemented on the testing board of Fig. 22. C_filter and C_filter2 are two capacitors of 10 and 44 μF, respectively, with an equivalent series resistance (ESR) below 20 mΩ. L is an inductor of 1 μH with an ESR of 20 mΩ, whereas the resistor is 0.5 Ω. Table IV reports the measured worst case of conductive EMI, whose peaks, thanks to the designed filter, are below −70 dBV under nominal 48 V conditions. In Table IV each row shows, for a different input voltage, and for three different load current values, the EMI measurement result and the frequency at which the peak has been revealed. Instead, Fig. 32 displays the reduction of the input current vs. Fig. 31, thanks to the use of the soft-start technique. In the converter, wake up phase the current peaks are reduced by at least three times. Hence, the converter switching activity will not disturb the components connected to the same power source.

Fig. 30.

Proposed anticonductive EMI filter topology.

TABLE IV EMI Conductive Results After Filtering

Measurements of EM radiation emission are carried out in an anechoic chamber and in a shielded room using dedicated EMI instrumentation. The measures from 0 Hz to 100 kHz have been made in a shielded room with the *EHP-50C E-H-field Analyzer*.

Fig. 31.

Input current without soft-start modality (the green signal is the input current request from the converter).

Fig. 32.

Input current with soft-start modality (the current peaks, represented by green signals, are reduced by 3 times vs. Fig. 31).

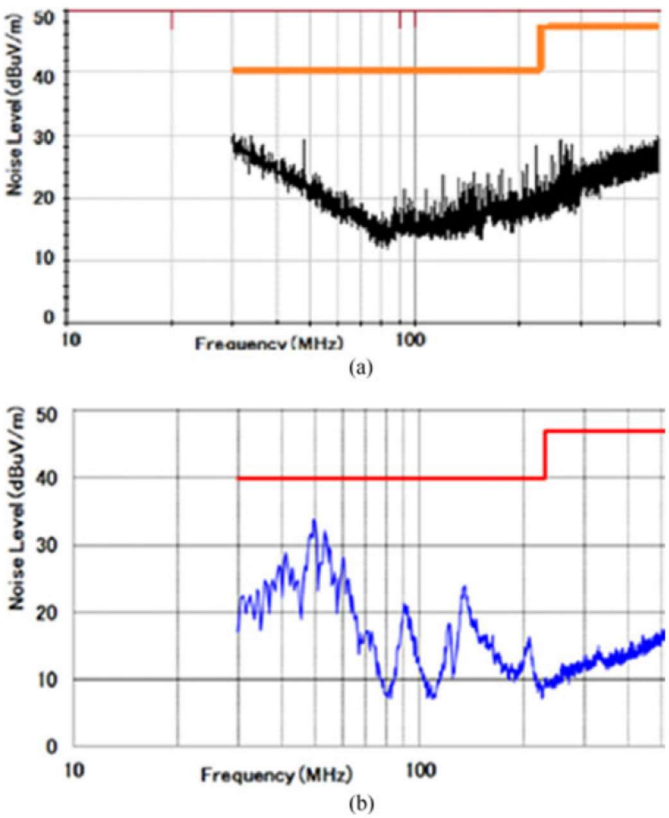
This test set-up allows the measurement of the near electric/magnetic fields radiated by the dc/dc converter. The measures are made under different operative conditions. The measures from 10 kHz to 1 GHz have been made with a near electric field sensor *Hameg HZ530 (mono-pole),* in anechoic room, at a distance of 1 m from the board. The results in Fig. 33 show that the radiated power is concentrated in the odd harmonics of the switching frequency. The first peak is 90 kHz but this is not the highest peak. Thanks to the spreading effect of the SKIP-mode control, the highest peaks are at the third, fifth, and seventh harmonics. The different operative conditions of the converter do not influence the EMI. A test of EMI emission has been carried out to verify that CISPR22 [27] law limits are met. The test is carried out in anechoic room at 3 m from the converter with a Biconical antenna EM-6917-1. This test compares the emissions from 30 to 500 MHz with standard limits [red line in Fig. 34(A)]. For comparison, Fig. 34(B) reports the same EMI test for a 48 V dc/dc converter in [14] using inductors. As shown in Fig. 34(A), the proposed design does not entail EMI issues (emissions are always lower than 30 dB μV/m).

Fig. 33.

High frequency measure of electric field at 1 m from board.

Fig. 34.

EMI test according to CISPR22 normative [27]. (a) Our dc/dc converter and (b) converter in [14].



SECTION VIII.

State-of-Art Comparison

When compared to the state-of-art, the compact dc/dc converter design stands for the following aspects.

1. To the best of authors' knowledge, this is the first dc/dc design for 48 V machines avoiding the use of cumbersome inductors, which instead are up to 12 μH in [14].

2. EMI of the proposed converter are lower than state-of-art designs (see comparison in Fig. 34 vs. [14]).

3. With respect to other inductorless switching converter, the proposed design sustains an input range from 6 to 60 V, whereas other works at the state-of-art, addressing similar load voltage and currents, e.g., the LTC3245 dc/dc [13] converter with 250 mA and 5 V, are limited to max 38 V.

Moreover, this work extends the contribution in [12], which was limited to a preliminary simulation analysis only. Instead, in this work, implementation and experimental measurement of both the BSG electrical machine in Sections II and III and of the dc/dc converter in Sections V and VI are presented. This work also presents EMI reduction techniques and measurements in Section VII, completely missing in [12].

The advantages of the designed BSG machine vs. the 12 V alternator of a car with conventional ICE have been discussed in Section II. Instead, when comparing the proposed BSG machine vs. similar works in the literature [21], [38] , [39], the following advantages can be highlighted:

1. no mechanical layout modifications vs. classic 12 V alternator in conventional ICE cars;

2. 3-D integration of electronics control avoiding discrete components (H-bridge MOSFETs implemented in HV-MOS technology with DCB on a ceramic substrate);

3. PCB mounted as mezzanine and downsizing of all electronics allowing integration at power modules level;

4. new functionalities such as direct current measurement on each transistor of the H-bridge;

5. H-bridge for rotor drive with increased managed levels for voltage and current, but decreased on-resistance, vs. H-bridge solutions in the same HV-MOS technology [21].

SECTION IX.

Conclusion

With reference to an electrical belt-driven starter-generator unit for micro/mild hybrid vehicles, the paper presented the design of a 48 V H-bridge for rotor driving, and of a compact dc/dc converter to supply sensors and control unit. The electrical machine is a

six-phase 48 V synchronous machine, with 0–8 kW power range (up to 15 kW peak) with a double tri-phases stator and a wounded rotor. Tested in a real hybrid vehicle, the advantages vs. classic alternator solutions have been discussed. The schematic of the sensing and control electronics of the 48 V electrical machine has been analyzed, with a focus on the design and measurements of the 48 V H-bridge for rotor excitation and of the compact dc/dc converter for low-power loads supply. The whole electronics can sustain over-voltages of at least 70 V, with extended temperature ranges from −40 °C to 175 °C (ambient). Integrated into low-cost 0.35 μm HV-MOS technology, with DCB on a ceramic substrate, the H-bridge allows a compact installation with increased current (×2.5) and voltage (×4) levels, and decreased on-resistance (×6), vs. the previous rotor drive generation in the same technology. Using the same technology, with respect to the state-of-art, the compact dc/dc converter avoids the use of cumbersome isolated inductors and generates multiple voltage outputs with a configurable regulation factor (acting in step down or up modes). The proposed converter sustains an input voltage variation of one order of magnitude, from 6 to 60 V, with a PSRR of at least 60 dB. By adopting a SKIP-mode control plus an integrated soft-start technique and the design of anticonductive EMI filter, the EMI issues are avoided.

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