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65 nm Technology for HEP: Status and Perspective

PoS(Vertex2014)043

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The RD53 Collaboration †

The development of new experiments such as CLIC and the the foreseen Phase 2 pixel upgrades of ATLAS and CMS have very challenging requirements for the design of hybrid pixel readout chips, both in terms of performances and reliability. To face these challenges, the use of a more downscaled CMOS technology compared to previous projects is necessary. The CERN RD53 collaboration is undertaking a R&D programme to evaluate the use of a commercial 65 nm technology and to develop tools and frameworks which will help to design future pixel detectors. This paper gives a short overview of the RD53 collaboration activities and describes some examples of recent developments.

The 23rd International Workshop on Vertex Detectors,
15-19 September 2014
Macha Lake, The Czech Republic

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1. Motivations

The success of many experiments in High Energy Physics have shown the importance of high performance pixel tracking. Extrapolations of hybrid pixel technology, however, looking at the requirements for future experiments, present major challenges for the detectors. These include higher pixel density, more complex logic for triggering or on-chip data analysis, lower power consumption and higher bandwidth. Using a more downscaled CMOS process will help face these challenges and many projects, such as HL-LHC and CLIC among others, are converging on studying the feasibility of using a commercial 65 nm CMOS technology for their pixel detectors.
The particular choice of 65 nm was done due to a number of factors. First of all it allows for considerably higher density and lower power consumption designs compared to technologies used in current projects (mainly 250 nm and 130 nm). It is a mature technology, being first introduced in the market in 2007 and it will be available for the foreseeable future, as it's widely used in the semiconductor industry. Moving to a new technology will cause an increase in the non-recurrent costs, which is a reason why even more downscaled technologies (45 nm or smaller) were not considered. In addition, the radiation hardness of CMOS processes using high-K dielectrics is still not well studied.

1.1 The RD53 collaboration

In order to address the many challenges of making readout integrated circuits for future experiments, a new R&D collaboration, RD53, has been established[1]. A combined effort between ATLAS, CMS and CLIC was found to be the most efficient manner to resolve the common challenges ahead. This collaboration of 19 institutes and ∼100 members will over the next years develop the methods and design foundation needed to produce a new generation of pixel detectors that can deliver the higher performance required by future projects.
RD53 is split in six different working groups:

- Radiation Tolerance
  Radiation test and qualification of 65 nm technologies
- Simulation
  Develop simulation and verification framework for complex pixel chips
- Analog
  Evaluation, design and test of analog Front-Ends
- Top level
  Global architecture and floor-plan issues for large mixed signal pixel chip
- IP Blocks
  Build a library of shared IP blocks (PLLs, Bandgaps...)
- I/O interfaces
  Develop high-bandwidth I/O interfaces for chip communication

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Particle flux	500 MHz/cm^2
Pixel hit rate	2 GHz/cm^2
Trigger rate	1 MHz
Readout Bandwidth	4 Gbps/chip
Pixel size	~50x50 μm^2
Total Radiation Dose	10 MGy

Table 1: Some of the preliminary requirements for ATLAS and CMS phase 2 pixel detectors

Each group will specialize on various aspects of detector design, working together towards a series of common Multi-Project Wafers (MPW) submissions in 2015 - 2016 to test IP blocks and new architectures. A full demonstrator for CMS/ATLAS pixel upgrades is scheduled for 2016.

2. New challenges

Requirements for future HEP experiments present multiple challenges in the design of pixel detectors. The first example is the ATLAS and CMS upgrades for High-Luminosity LHC. While the final design of the experiments is not finalized, most specifications can already be calculated. Interaction between chip design, sensor R&D, and trigger and data acquisition will help shape the final requirements. A summary of the main HL-LHC specifications can be found in Table 1.

The pixel detectors for the CLIC project have different requirements from the ones developed for HL-LHC, but they are also very challenging. The main specifications of the CLIC detector include a small pixel size (25x25 μm^2), simultaneous energy and timestamp measurement (with a 10 ns accuracy), while keeping the material budget low. In order to have as little material as possible, an air cooling solution is envisioned. This limits the total power consumption of the vertex detectors to about 50 mW/cm^2, due also to the geometry of the system[2]; both high density and low power consumption will also benefit from an upgrade to a 65 nm technology.

2.1 Radiation hardness

The 65 nm CMOS process seems to be promising for the future pixel readout chips in term of high integration density but it have to be extensively tested and qualified for the irradiation, which in HL-LHC will reach unprecedented levels. Simulations show that its pixel detectors will integrate a fluence (1 MeV neutron equivalent) of about $10^{16} n/cm^2$ and a Total Ionizing Dose (TID) of 10 MGy (1 Grad). The radiation damage on the proposed 65 nm technology, due to both total dose and single event effects, has been studied by the RD53 Radiation Working Group[3].

Tests were done on single transistors with different geometries. A large current driving loss was observed for the minimum size P-channel device. This tends to slow down digital circuits as observed on the ring oscillator implemented with the same process. Testing on devices for digital design having a width varying from 120 nm to 1 μm were done up to 10 MGy and showed that the leakage current degradation does not seem to be the main issue with this process. However, we observed an important performances degradation for both N and P channels devices starting from a dose level of 2 MGy and particularly for the narrow PMOS devices. At a dose level of 10 MGy, the pmos transconductance loss is near 100% for narrow channel devices (measured at

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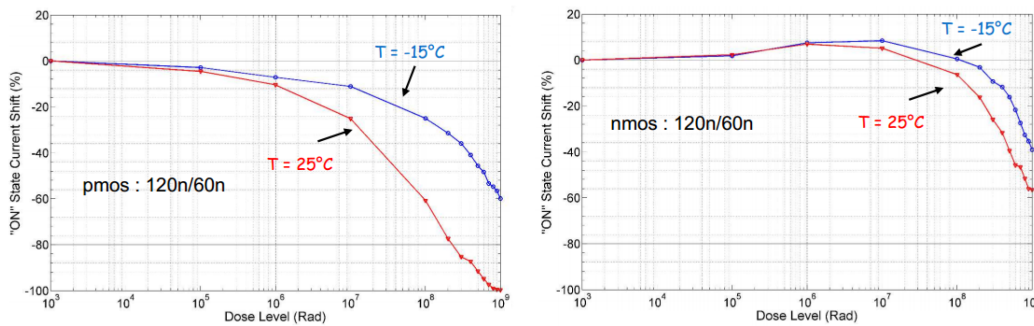

Figure 1: ON state current versus TID for narrow devices (120 nm width, 60 nm length), at two different temperatures

room temperature) which turns the device completely off (see Figure 1). The functionality of the devices are partially recovered with annealing. The effect is less noticeable in wider devices, so further studies are in progress to better characterize the radiation damage and to produce a set of recommended rules (mostly on transistor size) to follow for radiation hard design.
Tests were also conducted at low temperature and results were compared to the tests performed at room temperature. At -15 °C the degradation of the PMOS ON state current for a minimum size transistor reaches 60% at 10 MGy, a considerably better result than at 25 °C. Also in this case annealing allows to partially recover their performances.

2.2 New architectures for Digital/Analog integration

One of the tasks of RD53 is to design novel architectures that can take advantage of a more downscaled CMOS process. Analog performances of this technology have been already validated and found to be good for HEP applications[4]. The much higher density in digital designs and the requirement for more and more "intelligence" in the pixels, on the other hand, creates the challenge of integrating digital and analog domains and how to exploit the possibility of improving analog structures using digital logic.
On the front of physical integration between analog and digital, different layouts have been proposed. The current trend in pixel detectors is to organize pixels in columns, alternating digital and analog circuits. This provides good isolation between the two, to minimize cross-talk and easy access to the chip periphery, where digital control blocks are situated. With higher bandwidth requirements and more complex digital designs, one of the proposed layout is having a "digital sea with analog islands" with digital logic all around the analog front-ends (see Figure 2).
In this approach analog structures can be shared among adjacent pixels and the contiguous digital logic can act as a distributed memory, with input ports in each analog pixel cluster.
Despite the arrangement of the pixel logic, though, the required bandwidth for a pixel chip in the case of HL-LHC is still very high. With the expected luminosity and trigger rate, each chip would need to send data at up to 4 Gbps. One of the ways to reduce the bandwidth requirement is to use an on-chip compression. Compression schemes has already been demonstrated in other HEP projects, such as FEI4[5], Timepix3[6] and CLICpix[7], which will be detailed in the next session. Similar solutions, which might include on-chip clustering and data reduction, can be adapted for the HL-LHC experiments as well.

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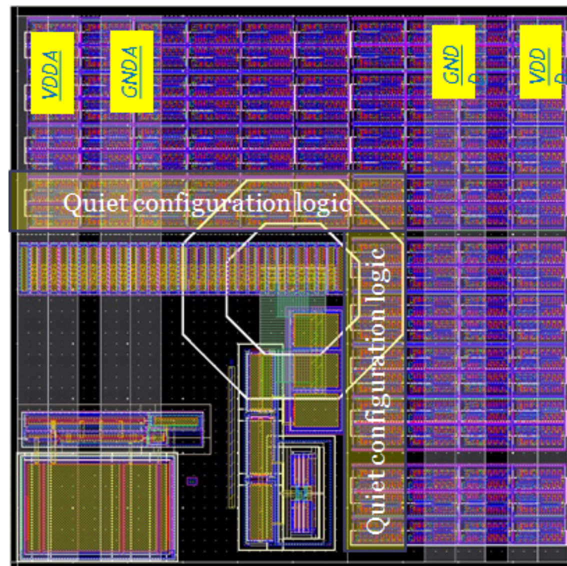

Figure 2: Proposed pixel layout. A cluster of four pixels (each rotated by 90 degrees) would constitute a regular structure where the analog part is completely surrounded by digital logic.

All the efforts by the various RD53 Working Groups in developing novel designs in 65 nm will also benefit from a common IP blocks repository that will greatly decrease development time for future projects and will increase their success, by using blocks which were already tested and validated.

3. A first prototype: CLICpix

As an example of a project designed using this commercial 65 nm CMOS technology, CLICpix will be presented in this section[7]. CLICpix is a hybrid pixel detector for the CLIC experiments and a prototype of the readout ASIC has been designed and characterized.
The CLICpix prototype includes a 64x64 pixel matrix, working in a *single event detection* mode. Each pixel measures 25x25 μm^2. The pixel matrix is divided in 32 double columns (grouping arrays of 32x2 pixels). Pixels in a double column have their digital part merged together to optimize the area of the digital circuitry. A "periphery block" is included to manage I/O and to provide biasing and global configuration. A picture of the chip is in Figure 3

Each pixel implements an analog and digital front-end, shown in Figure 4. Current pulses coming from the sensor or from a test capacitor are amplified and shaped by the preamplifier and feedback network and compared to a global threshold. This threshold is locally adjusted with a 4-bit Digital-to-Analog Converter (DAC) to compensate for pixel-to-pixel threshold mismatch. The result of the comparison is used for the counting clocks of both the Time-over-Threshold (ToT) and Time-of-Arrival (ToA) counters. The content of the 4-bit ToA and 4-bit ToT counters forms the 8-bit data acquired by each pixel with a valid hit.
The pixel array also implements a data compression scheme. This is done by adding a flag for every pixel, that is set to 1 if the pixel registered some hits during the shutter time. A multiplexer controlled by this flag causes the pixels with no information to be skipped during the readout phase.

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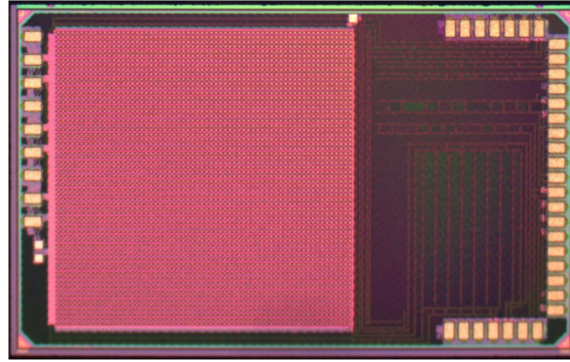

Figure 3: The CLICpix prototype chip

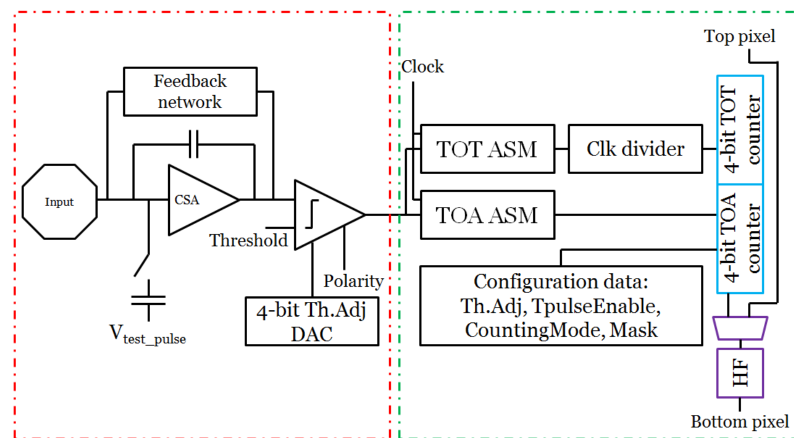

Figure 4: Block diagram of the pixel circuits in the CLICpix prototype. The left part is the analog front-end, with the preamplifier, the discriminator and the threshold equalization DAC. The right part shows the digital one, with Asynchronous State Machines generating enable signals for the ToT and ToA counters and configuration latches.

This means that each pixel has one additional bit that needs to be read out (9 bits instead of 8) but pixels without a valid hit only contain a single bit of data. Pixels are grouped together in 2 by 8 pixel clusters (or "superpixels") and 8 superpixels form a double column.
Due to cooling constraints, the average power consumption of the detector must be lower than 50 mW/cm^2, which motivates the use of a power pulsing technique. This is possible because of the time between bunch crossings in CLIC (20 ms), which allows for a duty cycle of 30 μs every 20 ms. The power pulsing is implemented by having two DACs in the periphery to program each state of the most power-consuming pixel analog blocks (the preamplifier and the discriminator). One DAC is used to control the nominal biasing during data acquisition. The other one is added to provide a stand-by biasing current within a range of values several times lower than the first one. A multiplexer for each double column in the periphery can switch the biasing of the pixels from the nominal value to this "low-power" state, decreasing the power consumption of the analog part by more than one order of magnitude. Not all structures in the analog pixel are switched off, so the reduction in power consumption doesn't match the duty cycle, but it is still sufficient to respect the power budget. The power consumption measured with power pulsing is basically only the power

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Parameter	Simulated Value	Measured Value
ToA Accuracy	< 10 ns	< 10 ns
Gain	44 mV/ke^-	40 mV/ke^-
Dynamic Range	up to 40 ke^-	up to 45 ke^-
Equivalent Noise (bare chip)	$\sigma = 60\,e^-$	$\sigma = 51\,e^-$ (with 10% r.m.s.)
Threshold Spread (uncalibrated)	$\sigma = 160\,e^-$	$\sigma = 128\,e^-$
Threshold Spread (calibrated)	$\sigma = 24\,e^-$	$\sigma = 22\,e^-$
Minimum threshold	388 e^-	417 e^-
Analog power cons. w/o power pulsing	6.5 μW/pixel	7 μW/pixel
Analog power cons. with power pulsing	0.25 μW/pixel	0.25 μW/pixel

Table 2: Comparison between simulation results and measurement of the CLICpix prototype.

consumption of the threshold equalization DAC, as it cannot be switched off. The other circuits, due to the low duty cycle, add a negligible contribution.
The chip was tested and a summary of the characterization results compared to simulated values can be found in Table 2. The only significant issue found is a higher than expected minimum threshold for pixels in odd-numbered columns (which can be higher than 1 ke^-). This is due to a layout issue that causes a crosstalk between the input pad and the discriminator output in the affected pixels. Despite this routing problem, the architecture and the technology was found to perform as expected, within the processing tolerance.
The chip was also tested for radiation hardness, even though the test was not necessary for CLIC applications. The chip was irradiated up to 800 Mrads. Until 200 Mrads, no significant change in the chip performances was found. Above 200 Mrads, the chip gradually turned off, as the PMOS switches used for biasing structures stopped being able to conduct the nominal amount of current. Despite this issue, all I/O interfaces and digital structures did not show any significant degradation during irradiation, even after the analog front-end stopped working. The chips regained some functionality after two week of annealing at room temperature (the total power consumption went back to pre-rad value), but analog performances of the measured chip were found to be considerably degraded.

4. Conclusions and other projects

The main activities of the RD53 collaboration has been shortly summarized here, along with some of the main activities of some of its working groups. This paper does not want to be a comprehensive list of everything the collaboration is currently working on: only a few results have been shown to motivate the choice of using a 65 nm technology for future pixel detectors.
ATLAS, CMS and CLIC are not the only projects studying the feasibility of 65 nm technologies in HEP. Other noticeable examples include Belle-II, which uses a gigabit data transmitter which was developed using the same technology[8]. This chip features high speed links running at 1.6 Gbit/s, with a total bandwidth of up to 6.4 Gbit/s, used to read out DEPFET modules in the detectors. The choice of a 65 nm technology was due to the speed requirements. The same technology will tentatively be used also in for the front-end ASICs, due to its radiation hardness.

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Another project developed at CERN is the Lp-GBT, a low-power redesign of the GBT chip[9]. A prototype of this ASIC was already submitted and tested. It features a 4.8 Gbit/s serializer, which is SEU robust. The use of a 65 nm process allows the circuit to be very power efficient: its power consumption is less than 20 mW, which is better than 1/4 of the power used in state-of-the-art serializers.
The same technology is also used in the MPA chip[10], a front-end for the CMS tracker upgrade with with local p_T discrimination. This ASIC includes long pixels of 1.5 mm by 0.1 μm. The main challenge of this design is the power budget of around 200 mW per chip, which led to the choice of a 65 nm low power CMOS process. A prototype of this chip is currently being tested.
CERN is actively contributing to help the HEP community develop projects using downscaled nodes such as 65 nm. It is working together with manufacturers to more easily allow institutes and collaborations to access foundry services and to provide a unified infrastructure to help researchers collaborate and share their designs.
Of course there is still a lot of work to do before a new technology will become widely used by the community, but tests and prototypes so far have validated its performances in HEP applications; many institutes are receiving access to the design tools at the time of writing and there is a strong interest in 65 nm.

References

[1] M. Garcia-Sciveres and J. Christainsen, *RD Collaboration Proposal: Development of pixel readout integrated circuits for extreme rate and radiation*, *CERN-LHCC-2013-008*, *http://cds.cern.ch/record/1553467/*

[2] F. Duarte Ramos et al., *CLIC inner detectors cooling simulations*, *LCD-Note-2013-007*

[3] M. Menouni et al., *10 MGy Total Dose Evaluation of 65 nm CMOS Technology for the High Luminosity LHC Upgrades*, presented at *TWEPP 2014*, publication pending

[4] G. Traversi et al., *Perspectives of 65nm CMOS Technologies for High Performance Front-End Electronics in Future Applications*, presented at *VERTEX 2012*

[5] M. Garcia-Sciveres et al., *The FE-I4 pixel readout integrated circuit*, *Nuclear Instruments and Methods in Physics Research Section A*, *Vol. 636*, *April 2011*

[6] T. Poikela et al., *Timepix3: a 65K channel hybrid pixel readout chip with simultaneous ToA/ToT and sparse readout*, *Journal of Instrumentation*, *Vol. 9*, *May 2014*

[7] P. Valerio et al., *A prototype hybrid pixel detector ASIC for the CLIC experiment*, *Journal of Instrumentation*, *Vol. 9*, *Jan. 2014*

[8] T. Kishishita et al., *Prototype of a gigabit data transmitter in 65 nm CMOS for DEPFET pixel detectors at Belle-II*, *Nuclear Instruments and Methods in Physics Research Section A*, *Vol. 718*, *Aug. 2013*

[9] D. Felici et al., *A 20 mW, 4.8 Gbit/sec, SEU robust serializer in 65nm for read-out of data from LHC experiments*, *Journal of Instrumentation*, *Vol. 9*, *Jan. 2014*

[10] D. Ceresa et al., *Macro Pixel ASIC (MPA): The readout ASIC for the pixel-strip (PS) module of the CMS outer tracker at HL-LHC*, *Journal of Instrumentation*, publication pending

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