High-power thermoelectric generators based on nanostructured silicon

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Abstract

The low thermal conductivity of silicon nanowires and nanostructures opens interesting opportunities for energy harvesting through the direct, high-efficiency, conversion of waste heat into electrical power. We present solutions for the fabrication and interconnection of a high number of suspended silicon nanostructures, within CMOS compatible top-down processes. Mechanical stability and thermoelectric properties of these devices will be analyzed by means of finite element simulations, and opportunities for practical applications will be discussed. It will be shown that, despite the reduced dimensions needed for a strong suppression of thermal conductivity, a considerable amount of electrical power can be delivered to the load as a result of the presence of many interconnected devices on the same chip.

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I. INTRODUCTION AND DEVICE FABRICATION

Direct conversion of heat into electrical power, through the thermoelectric effect, is a very promising approach for harvesting energy from any heat source, and in particular from those that are not exploitable with other techniques, because of the reduced thermal drop or of low power levels, such as as waste heat of industrial plants, residual heat of car engines, low temperature thermal sources. Current research is focusing on materials that are cheap, sustainable, and compatible with standard technological processes, and at the same time exhibit a large electrical conductivity σ together with a small thermal conductivity k_t, so that devices with high conversion efficiency can be fabricated. Silicon, the standard material used for device fabrication, has a large conductivity σ and a good Seebeck coefficient S, but, as a thermoelectric material, has the disadvantage of a high k_t, that is 148 W/(m K). Recently, it has been shown[1–3] that rough silicon nanowires and nanostructures show a strong reduction of k_t: values below 10 W/(m K) have been demonstrated[4–7]. Theoretical analyses[8–11] have shown that this strong reduction is due to phonon scattering on the nanowire surfaces, which is enhanced in structures with surface roughness. Devices based on silicon nanostructures can be fabricated both by means of bottom-up[12–14] and by means of top-down approaches[15–17]. A device, to be suitable for practical applications, must be capable of handling a considerable electrical power, and for this reason it must consist of a huge collection of parallel nanostructures. Electron beam lithography and etching can be used for the fabrication of a highly interconnected nanowire array[18–20] on the top silicon layer of a SOI (Silicon On Insulator) substrate, which is commonly used in integrated circuit fabrication. However, the effect of the parallel

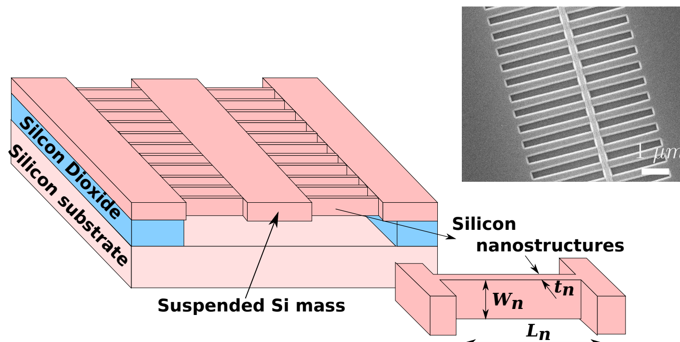

FIG. 1. Sketch of the proposed device. In the top-right inset: a SEM photo of a prototype nanostructure.

thermal conduction of the silicon substrate must be avoided to achieve the maximum device performances in terms of conversion efficiency. Solutions based on a suspended silicon mass, connected by nanowires obtained with bottom-up techniques, have been proposed in the past[21, 22]. Figure 1 shows a sketch of a device, based on a silicon mass suspended by top-down fabricated silicon nanostructures. The SEM image (top right) shows a first prototype fabricated on a SOI wafer, by using electron beam lithography and silicon etching. The central mass and the nanostructures are suspended between the left and right ends. The process is based on standard CMOS fabrication techniques. In particular, even though for the device shown in Fig. 1 e-beam lithography has been used for rapid prototyping, optical lithography can be used for industrial production because it has been shown[17, 23] that a reasonable tradeoff between good electrical conductivity and low thermal conductivity is obtained with nanowire widths between 50 and 100 nm, that is well within the capabilities of optical lithography used for present integrated circuit fabrication. A noticeable increase of the mechanical stability of the device, as well as of the deliverable electrical current (and power), can be achieved by using narrow vertical membranes, instead of nanowires, oriented perpendicularly to the silicon substrate, as shown in the sketch of Fig. 1. The nanostructure thickness t_n depends on the available lithographic capabilities. Selective vertical etching, such as dry Reactive Plasma Etching (RIE), can be used for nanostructure definition. The aspect ratio achievable during this step determines the maximum membrane height (width W_n). Standard RIE can achieve an aspect ratio as large as 10:1, that means $W_n = 1$ μm for $t_n = 100$ nm. Using advanced Deep-RIE (DRIE) an aspect ratio as large as 100:1 can be achieved[24–26]. Suspension of the nanostructures and of the central mass is achieved by means of underetching of the buried oxide underneath. For delivering significant power, many devices per square millimeter must be fabricated, as shown in the sketch of Fig. 2. In principle there is no limit to the number of parallel nanostructures holding the silicon central mass. Therefore, the device width W can be very large. In addition it is possible to fabricate an array of many devices for high power production. A top layer (see Fig. 2) will act as a heat collector. It can eventually be fabricated using silicon micromachining techniques, and flip-chip bonded to the central masses of the devices. This top layer can also provide suitable electrical interconnections among the devices, so that a series (or parallel) circuit configuration can be easily achieved. The top and bottom layers act as external interfaces with the hot and the cold sources. As shown in the inset of Fig. 2, heat flows from the top

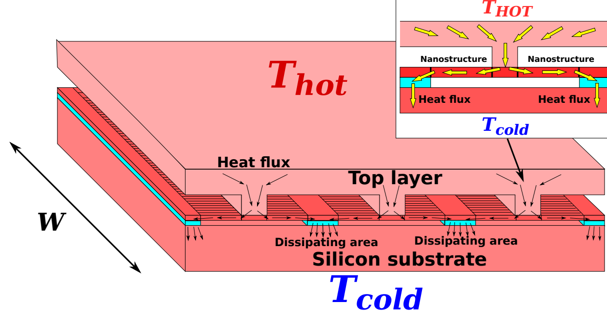

FIG. 2. Sketch of a few devices (as in Fig. 1) on the same chip. The top layer is flip-chip bonded onto the suspended masses. Arrows show the heat flux, from the top layer to the silicon substrate, through the suspended masses (see the top right inset).

layer through the the suspended mass and the nanomembranes, and it is then dissipated to the sides of the device, toward the bottom silicon substrate. The device density, which determines the total output power per unit of surface, is limited by the distance between neighboring devices, needed for proper heat transfer toward the substrate.
We will first report on the Finite Element (FEM) simulations performed to determine the mechanical stability of suspended silicon nanostructures (see Section II), that depends on the membrane geometry and number. Then, the heat conduction through the nanostructures will be investigated: it will be shown that if the area between the devices is sufficiently large, the temperature drop is concentrated within the nanostructures (nanomembranes). Section III shows FEM thermoelectric simulations of the device, and reports the maximum electrical power and conversion efficiency that can be achieved with the device. Finite element simulations have been performed by means of FEniCS[27], with the fundamental modules Dolfin[28] and FFC[29].

II. MECHANICAL AND THERMAL SIMULATIONS

A very critical issue for devices based on suspended masses held by nanostructures is their mechanical stability. We have investigated this issue with FEM simulations that have been performed on a small portion, 10 μm wide, of the device, as shown in Fig. 3: the central silicon mass is suspended by means of vertical silicon membranes 100 nm thick and 1 μm wide. In the left panel of Fig. 3, a typical deformation for an applied load of 5 mN is shown, assuming a membrane length of 10 μm. We assume a clamped-surface boundary condition at

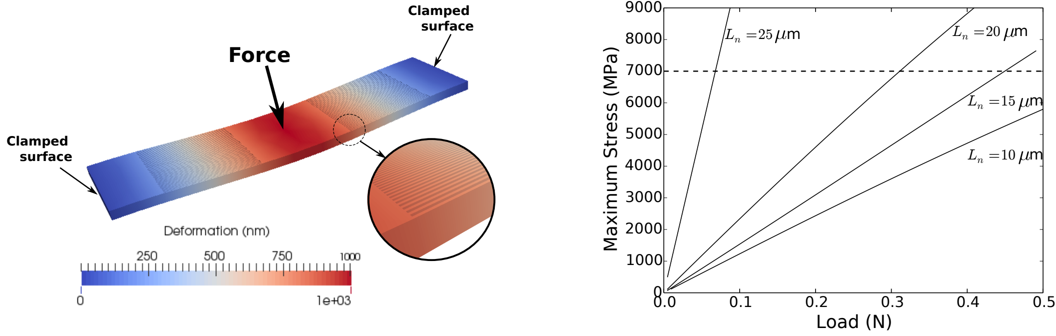

FIG. 3. Left panel: mechanical deformation of a portion of the device. Right panel: maximum Von Mises stress as a function of the load, for a device 1 mm wide. We report also the silicon ultimate tensile strength (maximum strain before breakage), which is 7000 MPa.

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the ends of the structure. The plot in the right panel of Fig. 3 shows the maximum Von Mises stress, for the whole structure, as a function of the total load applied to the suspended mass of a device with $W = 1$ mm. Several curves are reported for different nanomembrane lengths L_n. We report also the maximum tensile strength of silicon, which is about 7000 MPa. On the basis of these results, each device can withstand a load of fractions of a newton. The maximum force that can be applied on the top layer depends on the number of devices that can be integrated underneath, which in turn depends on the minimum distance between the devices resulting from the heat dissipation requirements. Since the device is fabricated on the top silicon layer of a SOI wafer, heat must be dissipated to the silicon substrate through the buried silicon dioxide layer, which is a good thermal insulator. This layer can however be chosen to be sufficiently thin: the thickness, corresponding to the empty space underneath the suspended mass and the nanostructure array at the end of the fabrication process, must be just enough to allow the expected deformation. The area of the surfaces outside the active region of the device must allow a sufficient heat flux toward the substrate, under the SiO_2 buried layer, in such a way that most of the temperature drop is localized between the ends of the nanomembranes. The high thermal conductivity of the bulk silicon substrate makes the heat flow toward the sink easy. In Fig. 4 we show a FEM result of the temperature distribution in a longitudinal section of the device (2D simulation). The top layer temperature is 900 K and that of the bottom layer is 300 K. We have assumed that the device is kept in vacuum (therefore there is no heat conduction due to air) and

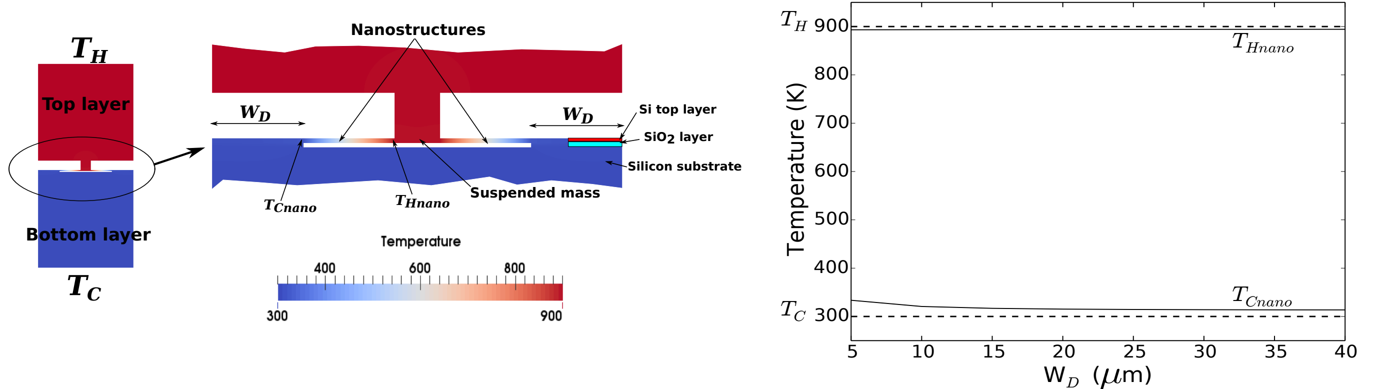

FIG. 4. Left panel: temperature map for the device. The FEM simulation takes into account the top and the bottom layers, both assumed to be 100 μm thick. The temperatures were chosen to be $T_H = 900$ K on the top and $T_C = 300$ K on the bottom. Right panel: the temperatures T_{Hnano} and T_{Cnano} at the ends of the nanostructures are shown as a function of the width of the heat sink areas W_D. Even for W_D as small as 5 μm, the temperature drop between the ends of the nanomembranes is comparable with that between the hot and cold sources.

we have neglected radiation effects, which can be minimized by means of a suitable coating (for aluminum the heat loss by radiation is of the order of 1 mW/mm^2 at 900 K). The silicon dioxide layer [with a thermal conductivity $k_t = 1$ W/(m K)] is assumed to be 1 μm thick. The value of $k_t = 10$ W/(m K) has been taken for the thermal conductivity of the nanomembranes (a more detailed discussion about the choices we have made for the value of k_t for the nanomembranes is provided in Sec. III), while the bulk thermal conductivity of silicon has been assumed for the top layer, the suspended mass and the bottom substrate. In the figure, a simulation with nanomembranes 20 μm long, 1 μm wide and 100 nm thick is shown; the width of the heat-sink areas on the sides of the device is $W_D = 10$ μm. In the plot on the left of Fig. 4, the temperatures T_{Hnano} and T_{Cnano} at the ends of the nanostructures are reported as a function of the width of the heat sink areas W_D. Even for small values of W_D, the temperatures at the ends of the nanomembranes turn out to be very close to those of the hot (T_H) and cold (T_C) sources. The difference between T_H and T_{Hnano} is always less than 10 degrees, and the difference between T_C and T_{Cnano} is below 15 degrees for $W_D > 20$ μm.

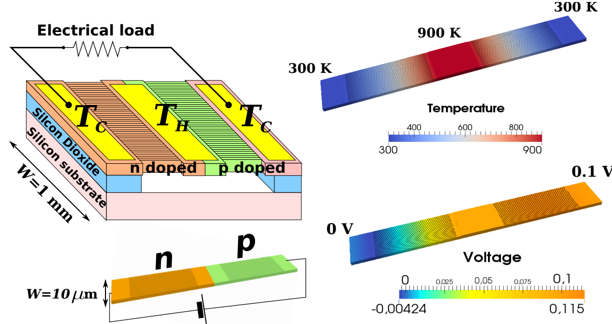

FIG. 5. Sketch of the thermoelectric generator (left panel); FEM simulations of temperature and voltage distribution are reported in the right panel.

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III. THERMOELECTRIC SIMULATIONS

The electrical power delivered by the device and its thermoelectric conversion efficiency have been determined solving standard electrical and thermal transport equations (thermoelectric equations), applied to the device shown in Fig. 1. The equations are reported in the Appendix, together with a quick summary of the finite element method applied to their solutions. The temperature variation of the Seebeck coefficient $S = S(T)$ of the electrical conductivity $\sigma = \sigma(T)$ and of the thermal conductivity $k_t = k_t(T)$ has been considered, as reported in the Appendix. A small portion of the device, similar to that treated in mechanical simulations, has been considered, and results have been scaled for a device width of $W = 1$ mm. As shown in the sketch of Fig. 5, the nanomembranes on the left of the suspended mass are n doped, those on the right are p doped, so that the device is just a basic module of a thermoelectric generator, with n and p legs. This is convenient for the simulation of the device, because in this way the physical properties of both n and p silicon, such as S_n, S_p, σ_n and σ_p, can be taken into account. However, in real applications the presence of junctions between silicon regions with different doping should be avoided because of doping interdiffusion that can occur at the operating temperatures. Therefore it will be more appropriate to fabricate devices having both sides with the same doping (n or p) and to obtain the pn generator module by means of suitable interconnections between devices with opposite doping. The left panel of Fig. 5 contains a sketch of the generator module, completed with electrical contacts. In the right panel we report results of a FEM simulation

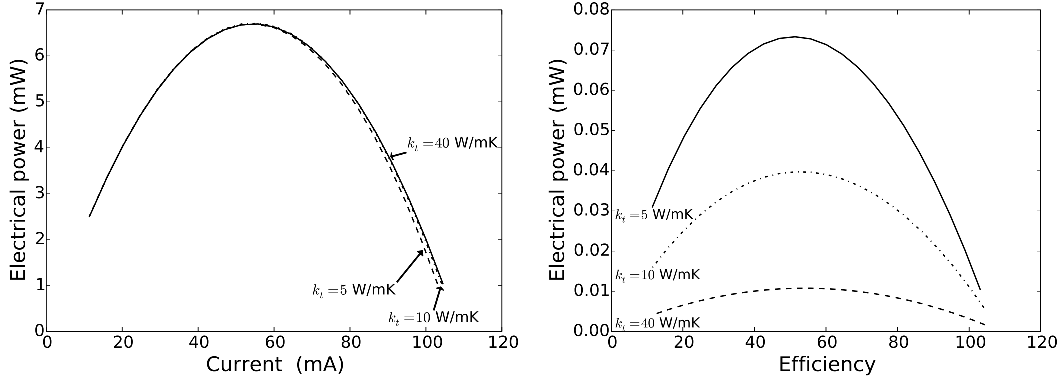

FIG. 6. Output electrical power (left panel) and efficiency (right panel) for $T_H = 900$ K and $T_C = 300$ K.

of the device operating with a voltage bias, for characterization purposes. In particular we show the temperature distribution (top) and the voltage distribution (bottom) for a small portion of the generator module 10 μm wide, with $T_H = 900$ K, $T_C = 300$ K, and an applied voltage of 0.1 V. The n and p doping concentrations are both 5×10^{19} cm^{-3}. As it has been previously demonstrated [23], the optimal doping concentrations depend on the device geometry and on the nanostructure thermal conductivity, and for this structure they are very close to the just mentioned values. In Fig. 6 we report the electrical power output (left panel) and the efficiency (right panel) as a function of the load current for $T_H = 900$ K and $T_C = 300$ K. This is the case of hot surfaces in automotive internal combustion engines or in some high-temperature industrial plants. The device is based on nanomembranes 20 μm long. Several curves are shown, for different values of the nanostructure thermal conductivity k_t. The values that we have selected for k_t are 40 W/(m K), 10 W/(m K), and 5 W/(m K): 40 W/(m K) is the result (close to the Casimir limit) reported in [30] for 100 nm thick nanomembranes, while the other values (10 and 5 W/(m K)) are extrapolations (currently there are no data in the literature of the thermal conductivity of nanomembranes as a function of surface roughness) based on an analogy with results for very rough nanowires and the encouraging data for holey nanomembrane [31].

The achievable thermal power, of about 7 mW, does not show a strong dependence on the thermal conductivity, as long as it does not become so large that the temperature drop is no more localized across the nanostructures. As expected, the thermal conductivity has instead a very strong effect on the maximum conversion efficiency, which reaches about 7%

for the optimistic value of $k_t = 5$ W/(m K). It is to be noted that the maximum efficiency is obtained for a different current, with respect to the maximum output power.

IV. FINAL CONSIDERATIONS

Our results demonstrate the opportunities offered by a thermoelectric generator based on top-down fabricated nanostructures. From the results of a finite element simulation, the power output of the model device that we have studied is of about 7 mW for a temperature drop of 600 K ($T_H = 900$ K, $T_C = 300$ K). The number of devices that can be fabricated on a square millimeter depends on the nanomembrane length and on the separation between the devices needed for heat dissipation at the cold ends of the nanostructures. If we assume the length of 20 μm considered in the simulations and separation between devices of 40 μm, more than 10 devices, 1 mm wide, can be integrated in a square millimeter. An estimated power of about 70 mW can be obtained from a chip of such a size, which corresponds to about 7 watts per cm^2. The achievable power depends only slightly on the nanostructure thermal conductivity, which should just be small enough to localize the temperature drop within the nanostructures. A low value of thermal conductivity is essential if high efficiency is to be pursued. Further theoretical and experimental activity is needed to establish the minimum achievable k_t for silicon nanomembranes and it will also be important to develop processes for inducing a controlled and reproducible roughness in such nanostructures in large scale production.

V. APPENDIX

For FEM simulation of thermoelectric transport the following equations have been used:

$$\vec{J} = \sigma\vec{\mathcal{E}} - S\sigma\nabla T$$

$$\vec{\phi} = ST\vec{J} - k_t\nabla T$$

where T is the absolute temperature, $\vec{J}$ is the current density, $\sigma = \sigma(T)$ is the electrical conductivity, $S = S(T)$ is the Seebeck coefficient, $\vec{\phi}$ is the heat flux, $k_t = k_t(T)$ is the thermal conductivity and $\vec{\mathcal{E}}$ is the electric field, which can be written as a function of the electrical potential V:

$$\vec{\mathcal{E}} = -\nabla V \quad (1)$$

The parameters S and σ depend on the doping: $S = S_n(n,T)$, $\sigma = \sigma_n(n,T)$ in the n part of the device, and $S = S_p(p,T)$, $\sigma = \sigma_p(p,T)$ in the p part. The thermal conductivity k_t is different for device sections made up of bulk silicon (suspended mass, heat-sink regions at the nanostructures ends), and for the nanostructures. The finite element method has been applied considering the two divergence equations for $\vec{J}$ and for $\vec{\phi}$, that are the continuity equation for current density, without generation-recombination, and the heat equation, respectively:

$$\nabla \cdot \vec{J} = 0$$
$$\nabla \cdot \vec{\phi} = \frac{\partial Q}{\partial t}$$

where $\partial Q/\partial t$ ($Q = C_V T$, C_V being the volume thermal capacity) is the rate of the generated heat in the solid. In the thermoelectric transport, the generated heat is due to the Joule effect:

$$\frac{\partial Q}{\partial t} = \vec{\mathcal{E}} \cdot \vec{J} = -\nabla V \cdot \vec{J} \tag{2}$$

Continuity equations can be rewritten as:

$$\nabla \cdot \vec{J}(V,T) = 0$$
$$\nabla \cdot \vec{\phi}(V,T) = -\nabla V \cdot \vec{J}(V,T)$$

where the scalar fields V and T are the unknown. Given the test functions t_V and t_T for potential and temperature, and integrating over the domain Ω (Ω is the whole device volume) we can derive the following equations:

$$\textstyle\int_\Omega \nabla \cdot \vec{J}(V,T)\, t_V \, dx = 0$$
$$\textstyle\int_\Omega \left[\nabla \cdot \vec{\phi}(V,T) - \nabla V \cdot \vec{J}(V,T) \right] \, t_T \, dx = 0$$

Dirichlet boundary conditions have been considered for the electrical potential V, so that integrating by parts the first equation we obtain:

$$\int_\Omega \nabla \cdot \vec{J}\, t_V \, dx = -\int_\Omega \vec{J} \cdot \nabla t_V \, dx \tag{3}$$

Heat sources have been considered at a constant temperature (T_H and T_C), by imposing Dirichlet boundary conditions on the corresponding surfaces. Neumann boundary conditions have been considered on all the other surfaces. Integrating by parts, we obtain:

$$\int_\Omega \nabla \cdot \vec{\phi}\, t_T \, dx = -\int_\Omega \vec{\phi} \cdot \nabla t_T \, dx \tag{4}$$

The Seebeck coefficient has been evaluated with the Stratton equation. The curves $S_n(n,T)$ and $S_p(p,T)$, for n and p doping, have been calculated (as a function of temperature), and a third-order polynomial fit has been used in the FEM simulation. Curves for the electrical conductivity $\sigma_n(n,T)$ and $\sigma_p(p,T)$ have been obtained with the semi-empirical formulas proposed by Arora[32], and fitted by means of third-order polynomials, whose coefficients have then been used in FEM simulations. A simple model[33, 34] has been used for taking into account the variation of the thermal conductivity k_t with respect to the temperature. Once given the room temperature value $k_t(300)$, at any temperature T:

$$k_t(t) = \frac{k_t(300.0)}{\left(\frac{T}{300.0}\right)} \tag{5}$$

This simple expression has been directly implemented in FEM simulations.

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