A sub-*kT*/*q* voltage reference operating at 150 mV

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***Abstract*—We propose a subthreshold CMOS voltage reference operating with a minimum supply voltage of only 150 mV, which is 3 times lower than the minimum value presently reported in the literature. The generated reference voltage is only 17.69 mV. This result has been achieved by introducing a temperature compensation technique that does not require the drain-source voltage of each MOSFET to be larger than 4*kT*/*q*. The implemented solution consists in 2T voltage reference with two MOSFETs of the same threshold-type and exploits the dependence of the threshold voltage on transistor size. Measurements performed over a large sample population of 60 chips from two separate batches show a standard deviation of only 0.29 mV. The mean variation of the reference voltage for V_{DD} ranging from 0.15 V to 1.8 V is 359.5 µV/V, while the mean variation of V_{REF} in the temperature range from 0 to 120 °C is 26.74 µV/°C. The mean power consumption at 25 °C for V_{DD}=0.15 V is 26.1 pW. The occupied area is 1200 µm².**

***Index Terms*— Voltage reference, subthreshold circuits, low-power design, low-voltage design.**

I. Introduction

REDUCING the minimum operating voltage is at the forefront of digital circuit research. Several works have reported the implementation of digital circuits operating with supply voltage lower than 200 mV [1]-[4]. Indeed, operation at the minimum supply voltage represents the most effective way to reduce power in a digital circuit. This concept cannot be extended tout-court to analog circuits where scaling the supply voltage does not ensure a reduction of power consumption [5]. However, it is worth noting that digital and analog circuits are usually used together in mixed-signal integrated circuits. Apparently, analog blocks represent a bottleneck for supply voltage scaling of such systems. In addition, in some emerging battery-free applications the minimum operating voltage is even a more important target than power consumption, as in the case of systems powered by energy harvesting devices (i.e. thermoelectric generators) or fuel cells [4]. In these applications, the energy harvested from machines or body heat can be considered an unlimited power supply [6], but only a limited voltage is available for the different building blocks.

To meet the requirements of power and supply voltage scaling, subthreshold operation has been intensely pursued by digital and analog designers. The fundamental limit to supply voltage scaling in circuits is represented by the voltage necessary to ensure a proper operation for all the employed transistors [8]. Since the bias required in the subthreshold regime is considerably less than in other operating conditions, it follows that this regime is the most promising for supply voltage scaling. In addition, the low current of subthreshold transport ensures a significant reduction in power consumption. Despite the apparent energy benefits, circuits biased in subthreshold pose several challenges related to speed limitations, temperature and process variability.

Among the different building blocks, voltage references are widely used in all analog, digital and mixed-signal systems. This circuit ideally generates an output voltage independent of supply voltage, temperature and process variations. It has been introduced in 1971 by Widlar [9], and it has been revised several times with the main purpose of meeting the requirements of power and supply voltage scaling. The classical solution to obtain a voltage reference in CMOS technology consists in implementing the configuration proposed in [9], the bandgap voltage reference (BGR), by exploiting the parasitic vertical BJTs of MOS transistors [10]-[12]. Alternatively, MOSFET-based voltage references with all transistors working in strong inversion regime have been proposed [13]-[14]. To reduce power consumption and supply voltage, voltage references with MOSFETs partially biased in subthreshold have been presented [15]-[18].

Ultra low-voltage, low-power voltage references have been obtained by biasing all MOSFETs in the subthreshold regime [19]-[20]. Both designs [19]-[20] use two MOSFET types with different threshold voltage in order to obtain a temperature-compensated voltage reference, and represent the state of the art in terms of minimum power consumption and supply voltage. The solution proposed in [20], the 2T (two transistors) voltage reference, exhibits a supply voltage as low as 0.5 V and a power consumption of only a few picowatts, while the solution reported in [19] shows a proper operation for a minimum supply voltage of only 0.45 V by consuming a power of 2.6 nW.

The configuration reported in [20] represents the best solution for the future low power applications since it allows a significant reduction in power consumption and occupied area. However, this solution exhibits degraded performance when

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the threshold voltages difference (equal to about V_{REF}) goes below $7.5V_T$, where V_T is the thermal voltage (26 mV at 300 K). As a result the minimum operating supply voltage for the 2T voltage reference presented in [20] is predicted to be about 12-13 V_T, which corresponds to slightly less than 450 mV as in the case of [19]. Hence, it is crucial to understand if the solution of the 2T voltage reference is appropriate also for the future scenario of chips biased at V_{DD} lower than 450 mV. However it is apparent that for supply voltage scalability of this solution a new temperature compensation technique and new design considerations are simultaneously required.

In this work we propose a reference voltage based on the 2T architecture capable to operate at the minimum supply voltage of only 150 mV while consuming 26.1 pW. The implemented solution consists of two MOSFETs of the same type and exploits the dependence of the threshold voltage on the transistor size to generate a temperature-compensated reference voltage with a magnitude around the thermal voltage V_T. This makes our circuit a valid solution to process the voltage generated by a thermoelectric generator (TEG) [6] - [7]. The validity of the proposed solution has been tested over a set of 60 samples from two different batches. The rest of the paper is organized as follows: we report in Section II the proposed operating principle and in Section III we report the measurement results and compare them with the solutions in the literature. In Section IV, we draw the conclusion.

II. Operating Principle and Design Considerations

The temperature compensation technique presented in this work is developed on 2T voltage reference proposed in [20]. In our solution, however, we use two MOSFETs of the same type, while MOSFET types of different threshold voltage are required in the reference presented in [20]. Fig.1 reports the schematic of the circuit considered in this work. The I-V characteristic of an nMOSFET operating in subthreshold regime is expressed as [19]:

$$I_{DS} = \mu_n C_{ox}\left(\frac{W}{L}\right) V_T^2 \exp\left(\frac{V_{GS}-V_{TH}}{nV_T}\right)\left[1-\exp\left(-\frac{V_{DS}}{V_T}\right)\right]. \quad (1)$$

μ_n is the electron mobility, C_{ox} the oxide capacitance per unit area, W and L the channel width and length respectively, $V_T=kT/q$ the thermal voltage (with k Boltzmann's constant, T the absolute temperature and q the elementary charge), V_{GS} the gate-source voltage, V_{TH} the threshold voltage, n the subthreshold swing factor and V_{DS} the drain-source voltage. In all references proposed so far the term in square brackets in (1) is neglected for all MOSFETs working in subthreshold regime [15]-[19]. This approximation is true if $V_{DS}>4V_T$ which is equal to about 100 mV at room temperature.

However it is evident that this assumption is a strong limitation for supply voltage scaling. For this reason it is crucial to understand when this condition can be removed without any penalties in other design specifications.

By considering the contribution of the drain-source voltages on the currents I_1 and I_2 (in M_1 and M_2, respectively) we obtain

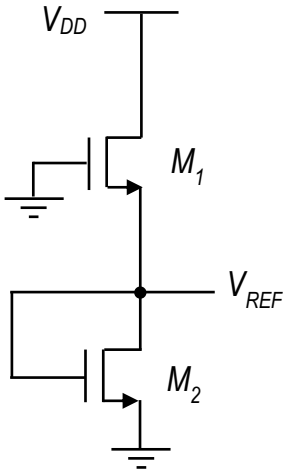


Fig. 1. Operation principle of the implemented voltage reference.

the following expressions:

$$I_1 = \mu_{n,1} C_{ox,1}\left(\frac{W}{L}\right)_1 V_T^2 \exp\left(-\frac{V_{REF}+V_{TH,1}}{n_1 V_T}\right)\times \left(1-\exp\left(-\frac{V_{DD}-V_{REF}}{V_T}\right)\right), \quad (2)$$

$$I_2 = \mu_{n,2} C_{ox,2}\left(\frac{W}{L}\right)_2 V_T^2 \exp\left(\frac{V_{REF}-V_{TH,2}}{n_2 V_T}\right)\times \left(1-\exp\left(-\frac{V_{REF}}{V_T}\right)\right). \quad (3)$$

Since we use two MOSFETs of the same type we have $C_{ox,1}\approx C_{ox,2}=C_{ox}$ and $n_1\approx n_2=n$.

In the 2T voltage reference transistor M_1 works as a current source. As pointed out in [19] when the reference voltage is coincident with the gate-source voltage of a diode-connected nMOS transistor, the stability of the generated reference voltage with respect to supply voltage depends mostly on the stability with respect to V_{DD} of the current injected into the load transistor. This condition provides the only constraint for supply voltage scaling in the 2T voltage reference, thus to ensure the best stability against V_{DD} variations, the drain-source voltage of M_1 has to be higher than $4V_T$, which means that V_{DD} has to be higher than $V_{REF}+4V_T$. On the other hand, the magnitude of the reference voltage, and consequently of the drain-source voltage of M_2, does not affect both supply voltage and temperature stability of the considered configuration. The latter observation suggests us the possibility to obtain in the 2T voltage reference a V_{REF} lower than $4V_T$ and consequently a minimum supply voltage lower than $8V_T$. However, as observed in the previous section, when V_{REF} scales below $4V_T$ the temperature compensation technique proposed in [20] cannot be applied. As a result a new temperature compensation technique becomes necessary.

By assuming $V_{DD}\geq V_{REF}+4V_T$ and by equating I_1 and I_2, the

following expression is obtained:

$$\ln\left\{\left(\frac{W}{L}\right)_R \frac{\mu_{n,1}}{\mu_{n,2}}\right\} = \frac{2V_{REF} + V_{TH,1} - V_{TH,2}}{nV_T} + \ln\left(1 - \exp\left(-\frac{V_{REF}}{V_T}\right)\right) \quad (4)$$

where $(W/L)_R=(W/L)_1/(W/L)_2$. Although equation (4) has not explicit solution for V_{REF}, we can find an approximate solution by replacing the logarithmic term with its linear approximation

$$\ln\left(1 - \exp\left(-\frac{V_{REF}}{V_T}\right)\right) \approx A + B\frac{V_{REF}}{V_T}, \quad (5)$$

where the two fitting parameters A and B depend only on the chosen interval of V_{REF}. Since in this work we are interested to exploit the minimum achievable value of V_{REF}, we choose to obtain V_{REF} in the range from $V_T/2$ to V_T. The corresponding fitting parameters at room temperature are equal to $A\approx$-1.35 and $B\approx$0.92. However, the proposed operating principle can be extended to a generic interval of $V_{REF}<4V_T$, by evaluating the corresponding values of A and B. As well known, the threshold voltage depends on the temperature according to the following linear equation [21]:

$$V_{TH}(T) = V_{TH}(T_0) - k_T(T - T_0), \quad (6)$$

where $V_{TH,0}(T_0)$ represents the threshold voltage at room temperature T_0 and $k_T<0$ the temperature coefficient for the threshold voltage. By replacing (5) and (6) in (4) we can express the reference voltage with the following expression:

$$V_{REF} = \frac{nV_T \ln\left\{\left(\frac{W}{L}\right)_R \frac{\mu_{n,1}}{\mu_{n,2}}\right\} + V_{TH,2}(T_0) - V_{TH,1}(T_0)}{2+nB} + \frac{|k_{T,1}|(T - T_0) - nV_T A - |k_{T,2}|(T - T_0)}{2+nB} \quad (7)$$

Differentiating the (7) with respect to temperature and setting $\partial V_{REF}/\partial T=0$ the value of $(W/L)_R$ for temperature compensation can be extracted as

$$\left(\frac{W}{L}\right)_R = \frac{\mu_{n,2}}{\mu_{n,1}} \exp\left\{\frac{q}{nk}\left[|k_{T,2}| - |k_{T,1}|\right] + A\right\}. \quad (8)$$

Replacing (8) into (7) we obtain the following expression of the temperature-compensated reference voltage

$$V_{REF} \approx \frac{V_{TH,2}(T_0) + |k_{T,2}|T_0 - V_{TH,1}(T_0) - |k_{T,1}|T_0}{2+nB}. \quad (9)$$

In (9) the two threshold voltages at room temperature $V_{TH}(T_0)$ depend on drain-source voltage V_{DS} and body-source voltage V_{BS} according to equation [22]

$$V_{TH}(T_0) = V_{TH0} - \lambda_{DS}V_{DS} - \lambda_{BS}V_{BS}, \quad (10)$$

where V_{TH0} is the threshold voltage at $V_{DS}=V_{BS}=0$ V, while λ_{DS} and λ_{BS} are the DIBL and body coefficients, respectively. Replacing (10) into (9) we obtain the following expression

$$V_{REF} \approx \frac{V_{TH0,2} + |k_{T,2}|T_0 - V_{TH0,1} - |k_{T,1}|T_0}{(2+nB)(1+\lambda_{DS,1}+\lambda_{DS,2}+\lambda_{BS,1})} \approx \frac{V_{TH0,2} + |k_{T,2}|T_0 - V_{TH0,1} - |k_{T,1}|T_0}{(2+nB)(1+2\lambda_{DS}+\lambda_{BS,1})}. \quad (11)$$

In analogy with [20], we can see from (11) that the reference voltage is proportional to the difference between the two threshold voltages at room temperature. As a consequence, to obtain a specific value of V_{REF}, we have to obtain a specific difference between the two threshold voltages. Since we have chosen two MOSFETs of the same threshold type we can obtain a significant difference between the two threshold voltages by using the dependence of the threshold voltage on transistor size. In Fig. 2 the simulated threshold voltage as a function of channel length and width for an nMOSFET in 0.18 μm CMOS technology is reported. The simulation shows a substantial difference between the threshold voltage of a long and short channel nMOSFET. In order to satisfy the approximation reported in (5) we choose a combination for L_1 and L_2 that gives a value of $V_{TH,2}$-$V_{TH,1}$ in the range for V_{REF} (i.e. from $V_T/2$ to V_T in our case). From Fig.2, imposing L_1=25 μm and L_2=2 μm, the difference between the two threshold voltages is equal to about 39 mV, which means a rough value of V_{REF} equal to about 18 mV (by neglecting nB in (9)). After imposing the channel length of both transistors, W_1 and W_2 are chosen in order to compensate the temperature dependence of V_{REF}. By selecting W>30 μm for both transistors, V_{REF} depends only on the selected transistor length (from Fig.2 V_{TH} is almost independent of

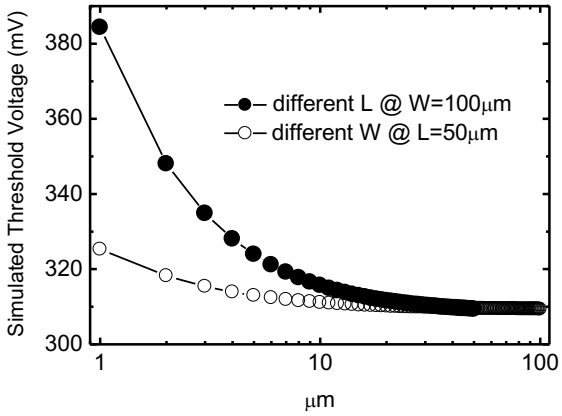


Fig. 2. Simulated threshold voltage as a function of channel length and width.

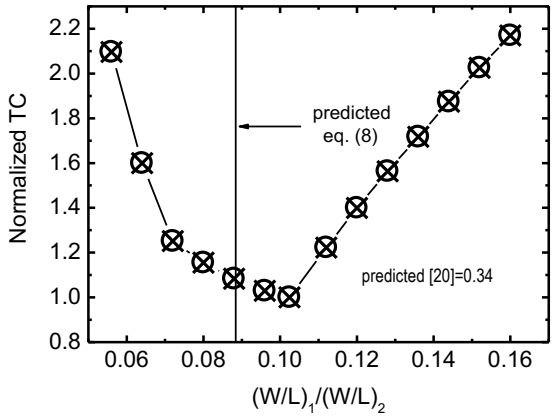
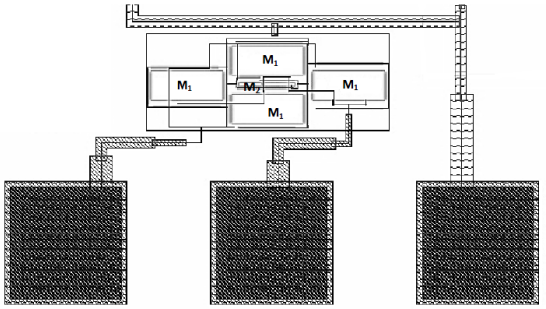
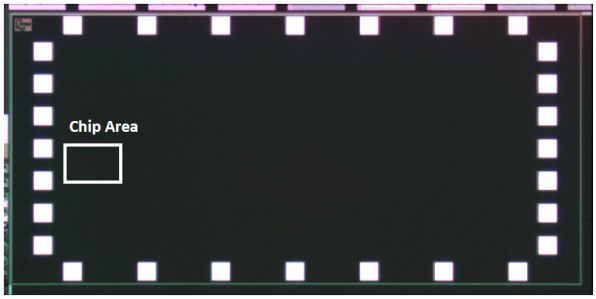


Fig. 3. Simulated normalized TC as a function of transistor size ratio. The simulated optimal transistor size ratio is equal to 0.10. According to (8) the predicted optimal transistor ratio is 0.088 while a value of 0.34 is evaluated in according to the temperature compensation technique proposed in [20].



(a)



(b)

Fig. 4. Layout (a) and chip photo (b) of the implemented voltage reference.

transistor width for W>30 µm). From the approximated expression (8) we obtain an optimal transistor size ratio for temperature compensation is 0.09 very close to the optimal transistor size ratio of 0.1 obtained with circuit simulation. In Fig. 3 the simulated normalized temperature coefficient (TC) as a function of the transistor size ratio is reported. The simulation was performed by imposing L_1=25 µm and L_2=2 µm and W_2=50 µm. As a result, the optimal value of W_1 provided by circuit simulation is 63.9 µm, quite close to the optimal value of 56.2 µm provided by the simplified expression (8). Note that the optimal transistor size ratio evaluated in according to the temperature compensation technique reported in [20] would be 0.34, corresponding to W_1= 212.5 µm. These results confirm the necessity of a new temperature compensation technique for the 2T with respect to the technique proposed in [20] when V_{REF} scales below $4V_T$ and confirm, at the same time, the validity of the proposed operating principle.

Since in our design the reference voltage is obtained by using the threshold voltage dependence on transistor size, L_2 has to be notably lower than L_1. This choice does not affect significantly the robustness of the reference voltage against supply voltage since the line sensitivity (LS) of the implemented solution has a second order dependence on L_2. On the other hand, large area MOSFETs can help to reduce the dispersion against intra-die process variations. However, since in our design the difference in the threshold voltages of the two MOSFETs is simply obtained by using different geometries and not by using different process variables (e.g. oxide thickness, substrate doping) such as in previous works [19]-[20], we expect our solution to have a lower dispersion. The power consumption of the proposed solution is also a function of transistor sizing mostly because in the 2T voltage reference the power consumption depends on the magnitude of the generated voltage reference.

The current flowing in the circuit depends exponentially from V_{REF} according to the following equation:

$$I_{DD} \approx \mu_{n,1} C_{ox,1} \left(\frac{W}{L}\right)_1 V_T^2 \exp\left(-\frac{V_{REF}+V_{TH,1}}{n_1 V_T}\right), \qquad (12)$$

consequently, the power consumption of the considered circuit is given by

$$P \approx V_{DD} \times \mu_{n,1} C_{ox,1} \left(\frac{W}{L}\right)_1 V_T^2 \exp\left(-\frac{V_{REF}+V_{TH,1}}{n_1 V_T}\right). \qquad (13)$$

From (13) the minimum power consumption can be obtained by reducing V_{DD}, however since $V_{DD} \approx V_{REF}+4V_T$, a reduction in V_{DD} causes an increase in the exponential term in (13) and consequently an increment in power consumption. For this reason the best choice to reduce V_{REF} (V_{DD}) without significant penalty in power consumption consists in the use of two high threshold voltage transistors for M_1 and M_2.

III. Measurement Results

The performances of the proposed sub-kT/q voltage reference have been tested over a set of 60 samples of two separated batches fabricated in UMC 0.18-µm, 1.8 V/3.3 V, CMOS process.

The layout and the chip photo of the proposed circuit are reported in Fig.4(a) and Fig.4(b) respectively. In order to improve the process stability against systematic mismatch due to stress and temperature, transistor M_1 is divided in four parts placed in a common centroid configuration [23]. This solution results in an active area of 1200 µm^2. The on-wafer electrical measurements have been performed by using a probe station

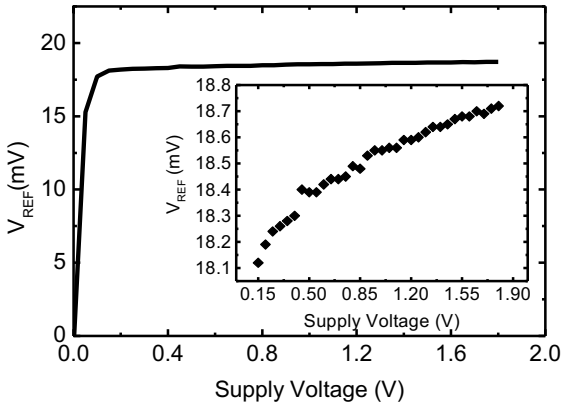


Fig. 5. Measured V_{REF} as a function of supply voltage at 25 °C and its zoom in the operating range. The measured mean value of V_{REF} is 17.69 mV against a simulated value of 15.33 mV.

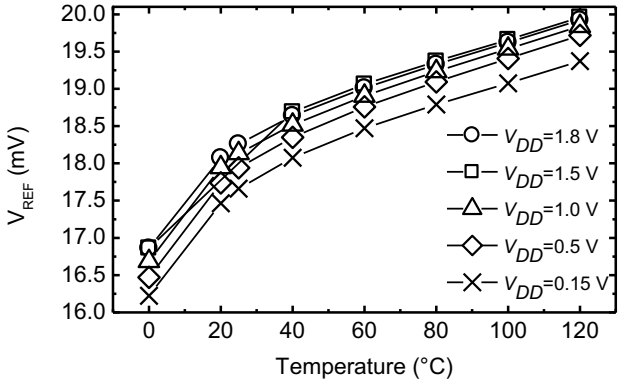


Fig. 6. Measured V_{REF} versus temperature for different supply voltages.

TABLE I
STATISTICAL ANALYSIS OVER 60 SAMPLES

	μ	σ
V_{REF} [mV]	17.69	0.29
TC [ppm/°C]	1462.4	324
Temp. variation [µV/°C]	26.74	5.57
LS [%/V]	2.03	0.11
Supply Voltage var. [µV/V]	359.46	21.19
Power [pW]	26.08	1.27

SUMMIT 11861B with Temptronic thermal controller and a Keithley 4200-SCS parameter analyzer. Figs. 5-8 show the measured performance of a typical device. Fig. 5 shows the reference voltage as a function of the supply voltage at the temperature of 25°C. It is worth noting that the circuit starts to work properly from only 150 mV. The temperature dependence of V_{REF} for different supply voltages is reported in Fig.6. Fig.7 gives an overview of the measured V_{REF} values in the 2D domain of operating temperatures and supply voltages. The power consumption for different temperatures and supply voltages is reported in Fig.8. The results of the statistical analysis performed over a set of 60 samples are summarized in Fig. 9 and Table I, where the mean (μ) and the standard deviation (σ) of the reference voltage, the temperature variation, the supply voltage variation and the power consumption are reported in detail. In Fig 9(a) we report the measured value of V_{REF} at the temperature of 25°C for V_{DD}=0.15 V. The mean value of V_{REF} is 17.69 mV, against a simulated value of 15.33 mV, with a standard deviation of only 0.29 mV. In Fig. 9(b) the variation of the reference voltage in the temperature range from 0 to 120 °C is reported. The measured mean variation of V_{REF} against temperature is 26.74 µV/°C, with a standard deviation of 5.57 µV/°C.

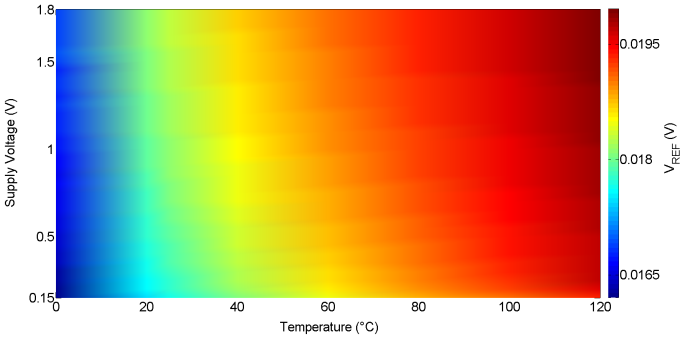


Fig. 7. Measured V_{REF} versus temperature and supply voltage.

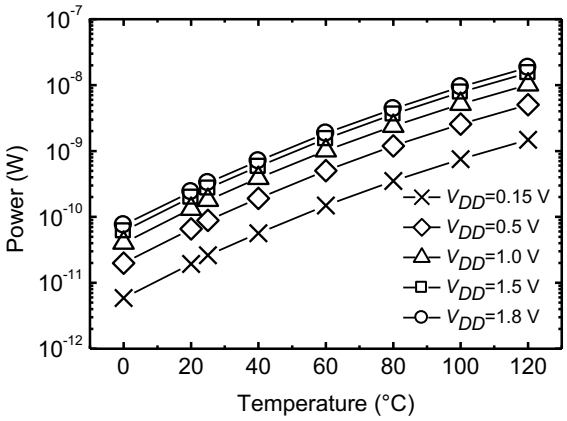


Fig. 8. Measured power consumption as a function of temperature for different supply voltages.

By normalizing for V_{REF}, we obtain TC=1462.4 ppm/°C with a standard deviation of 324 ppm/°C. In Fig. 9(c) the distribution of the variation of V_{REF} versus V_{DD} variations is reported. The mean variation of V_{REF} for V_{DD} ranging from 0.15 V to 1.8 V, at the temperature of 25°C, is equal to 359.46 µV/V with a standard deviation of 21.19 µV/V. By normalizing for V_{REF}, we obtain LS=2.03%/V with a standard deviation of 0.11 %/V. The statistical analysis of power consumption at V_{DD}=0.15 V and T=25°C is reported in Fig. 9(d). The mean power consumption is 26.08 pW with a standard deviation of 1.27 pW. The simulated PSRR without any filtering capacitor, for V_{DD}=0.15 V, is reported in Fig. 10.

The PSRR is equal to about -64 dB at low frequencies and -124 dB at 10 MHz. This because, as also reported in [20], the 2T voltage reference acts as a low-pass filter, so the PSRR

improves at higher frequencies. In Fig.11, the simulated referred output noise for different frequencies is reported. Thanks to the subthreshold operation and to the use of large area transistors, the gate- and drain-referred flicker noise is suppressed. The output referred noise is mostly thermal and it is attenuated in frequency through the sum of all capacitances connected from the output node to ground. The simulated output noise without any output capacitor is 0.31 μV/√Hz at low frequency and falls to 0.01 μV/√Hz at the frequency of 100 KHz. In Table II the performances of the proposed solution are compared with the two best low power, low voltage solutions reported in literature [19]-[20]. The proposed circuit starts to work properly from 150 mV, which improves by 350 mV the result obtained in [20] and by 300 mV the solution proposed in [19], which represents so far the best solution in terms of minimum V_{DD}.

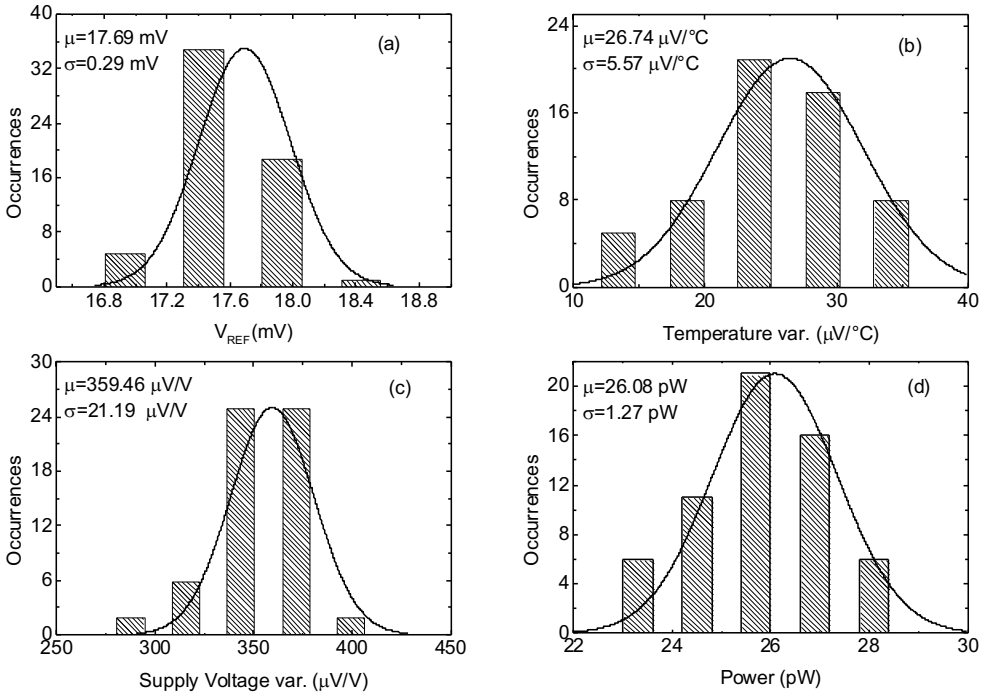


Fig. 9. Measured distribution over 60 samples of: (a) reference voltage @ 25°C; (b) absolute temperature variation of V_{REF}; (c) supply voltage variation versus V_{DD}; (d) power consumption @ 25°C and V_{DD}=0.15 V.

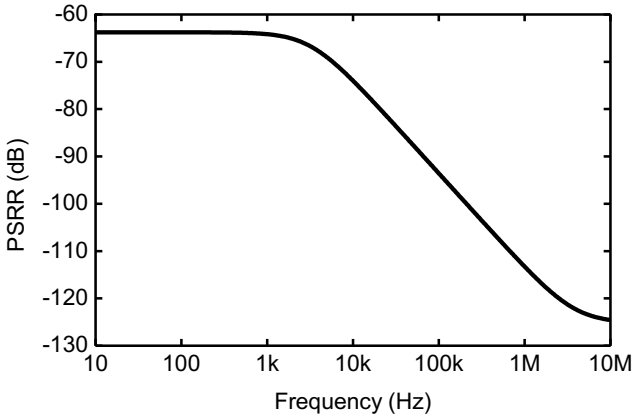


Fig. 10. Simulated PSRR at V_{DD}=0.15 V.

The power consumption at room temperature for the minimum operating supply voltage is about one order of magnitude larger than in [20] and about two orders of magnitude smaller than the solution proposed in [19]. The mean values of TC and LS are significantly higher than the other solutions [19]-[20]. This is due because both parameters are obtained by normalizing for V_{REF}, which in our design is significantly lower than the other solutions. Therefore, we compare in Table III the principal performance indicators in terms of absolute variations.

From this comparison, our solution exhibits better temperature stability with respect to the other solutions and a supply voltage stability better than the one reported in [19], but worse than the one reported in [20]. In Table II we report the comparison with [19]-[20] also in terms of dispersion of the main figures of merit. The relative standard deviation σ/μ of the reference voltage are 1.6% compared to 0.72 % of [20] and 3.9% of [19]. Nevertheless, the absolute variation of V_{REF} is better compared to the other solutions. The standard deviation of V_{REF} is only 0.29 mV, compared to about 1.3 mV of [19] and 10 mV of [20] (see Table III). The stability of the generated reference voltage against intra- and inter-die variations has been investigated by means of Monte Carlo simulations.

The simulated relative standard deviation of V_{REF} over 1000 samples is about 0.9 %. The proposed solution overcomes the other low-power, low-voltage voltage references in terms of

dispersion of TC, LS and power consumption. The relative standard deviation of TC is 22 % which is about 3 times smaller than the compared solutions, while the relative standard deviation of LS and power consumption is respectively about 2 and 5 times smaller than in [19] ([20] does not reports dispersion data on these two parameters). The lower dispersion of the main figures of merit observed in the proposed reference voltage is ascribed to the use of the same threshold-type of MOSFETs, whereas the voltage reference design presented in [19]-[20] are based on two different threshold-types of MOSFET.

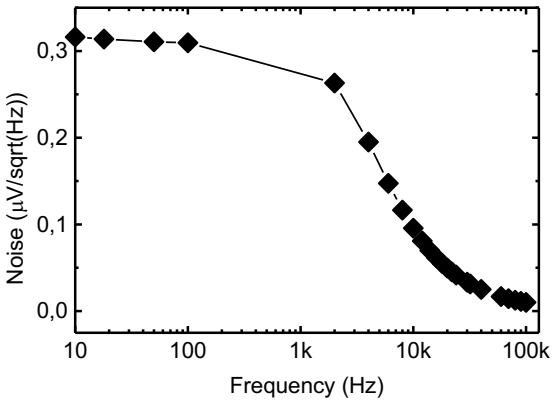


Fig.11. Simulated output referred noise for different frequencies.

TABLE II
COMPARISON WITH LOW-VOLTAGE LOW-POWER CMOS VOLTAGE REFERENCES

		This work	*Ref.* [20] *(no trimming)*	*Ref.* [19]
Technology		0.18µm CMOS	0.13µm CMOS	0.18µm CMOS
Supply voltage (V)		0.15 to 1.8	0.5 to 3.0	0.45 to 2
Power ***@ room temperature***		26.1 pW@0.15V 342.3 pW@1.8V	2.2pW@0.5V -	3.15nW@0.45V 14.4nW@1.8V
V_{REF} ***(mV)***		17.69	176.1	263.5
TC (ppm/°C) ***T range(°C)***		1462.4 (average) [0:120]	62 (average) [-20:80]	142.1 [0:100]
LS (%/V)		2.03	0.033	0.44
PSRR (dB) ***Low freq [≤100Hz]*** ***High freq [≥10MHz]***		V_{DD}=0.15V -64 (sim.) -124(sim.)	- -53 -62	V_{DD}=0.45V -49.4 (-12.2 sim.)
Process Sens.σ/µ	V_{REF}	1.6%	0.72%	3.9%
	TC	22%	66%	60.6%
	LS	5.4%	-	13.1%
	Power	5%	-	26.9%
Die area (mm²)		1200 μm^2	1350 μm^2	0.0430

TABLE III
ABSOLUTE VARIATION OF THE PRINCIPAL FIGURES OF MERIT FOR THE COMPARED VOLTAGE REFERENCES

		This work	*Ref.* [20] *(no trimming)*	*Ref.* [19]
Temperature var. (µV/°C)		26.74	35	37.6
Supply voltage var. (µV/V)		359.5	57.72	1185.2
Process variations	σ_{VREF} ***(mV)***	0.29	1.3	10

IV. CONCLUSION

In this work we proposed a sub-kT/q voltage reference capable of operating with a minimum supply voltage of only 150 mV. Although the proposed voltage reference is based on the same 2T architecture proposed in [20], it presents two fundamental features of novelty. The first one is that our design is based on different equations since it works at operating voltages significantly lower than the solution reported in [20]. The second one is that our design does not require two different threshold-types of MOSFET, since it exploits the dependence of the threshold voltage on transistor size. Measurements performed over a set of 60 samples from two separated batches show a mean reference voltage of 17.69 mV with a standard deviation of only 0.29 mV. The temperature variation in the range from 0 to 120°C is 26.74 µV/°C, which is lower than the best values reported in low-power, low-voltage solutions proposed so far. The line sensitivity of the reference voltage for supply voltage ranging from 0.15 to 1.8 V is 359.46 µV/V. The power consumption at room temperature for V_{DD}=0.15 V is 26.08pW. The occupied area is 1200 µm^2. In addition, the dispersion of the temperature coefficient, supply voltage sensitivity, and power consumption are smaller than the state-of-the-art solutions. The extremely low-voltage operation and the decapicowatt power consumption make our solution very attractive for battery-free, energy-harvesting applications.

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