A low-power interface for capacitive sensors with PWM output and intrinsic low pass characteristic

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Abstract— A compact, low power interface for capacitive sensors, is described. The output signal is a pulse width modulated (PWM) signal, where the pulse duration is linearly proportional to the sensor differential capacitance. The original conversion approach consists in stimulating the sensor capacitor with a triangular-like voltage waveform in order to obtain a square-like current waveform, which is subsequently demodulated and integrated over a clock period. The charge obtained in this way is then converted into the output pulse duration by an approach that includes an intrinsic tunable low pass function. The main non idealities are thoroughly investigated in order to provide useful design indications and evaluate the actual potentialities of the proposed circuit. The theoretical predictions are compared with experimental results obtained with a prototype, designed and fabricated using 0.32 μm CMOS devices from the BCD6s process of STMicroelectroncs. The prototype occupies a total area of 1025×515 mm^2 and is marked by a power consuption of 84 μW. The input capacitance range is 0-256 fF, with a resolution of 0.8 fF and a temperature sensitivity of 300 ppm/°C.

Index Terms—Capacitive sensor interface, chopper modulation, current mode, low power.

I. INTRODUCTION

CAPACITIVE sensors represent an important sector of the sensor market. They consist of one or more sensing capacitors, whose capacitance is a function of the quantity to be sensed. The mechanism of capacitance variation can be either geometry variation produced by relative displacement of the capacitor plates [1], as in inertial [1-2] and pressure [3]

sensors, or effective dielectric permittivity variation, as in the majority of chemical sensors [4-5]. Recently, capacitive sensing is finding new interesting applications in the field of biosensors [6] where it is being investigated as a promising technique for label-free detection of DNA strands and proteins [7].

Figure 1 shows the equivalent circuit of a capacitive sensor, where parasitic capacitances related to interconnections with the readout interface are also represented. The sensing element is capacitor C_X. As the quantity to be measured is swept across its whole input range, capacitance C_X varies from C_{X0} (offset capacitance) and C_{XM}. Typically, C_{X0} is much larger than the total excursion $C_{XM}-C_{X0}$. The temperature and process dependence of C_{X0} introduces uncertainties that degrade the sensor accuracy. In order to obtain an output quantity that is free of C_{X0} contribution, a reference capacitor C_R (shown in Fig.1) is often included in the sensor (differential sensor). The reference capacitor is nominally equal to C_{X0} and, when possible, should present the same temperature and process dependence as C_X. In many practical cases C_X and C_R have a common terminal (labeled with 3 in Fig.1). In balanced capacitive sensors, such as in most accelerometers, C_X and C_R are both dependent on the input quantity and their variation are opposite. The interface should be designed to read the difference $\Delta C = C_X - C_R$ (differential interface).
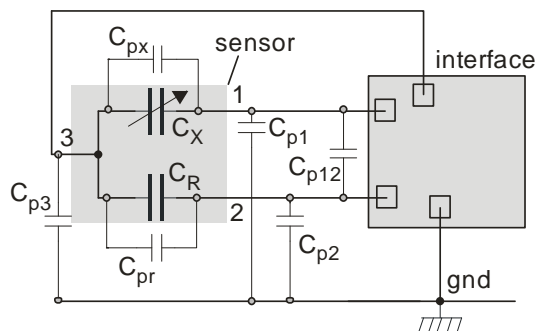

Fig. 1. Parasitic capacitances arising from the connection of a differential capacitive sensor to a readout interface.

Parasitic capacitances are present across all sensor terminal pairs and from all terminals and the interface ground. Using a proper interface configuration it is possible to reject the contributions from all parasitic capacitances, with the

exclusion, clearly, of C_{px} and C_{pr},. These capacitances can be effectively reduced by limiting the interconnection length and/or individually shielding the sensor leads.

Capacitive sensors can be read with several different approaches. In last decades, considerable effort has been focused on the development of compact and low power integrated interfaces, due to the growing commercial relevance of battery powered devices.

The most common approach to capacitive sensor interfacing is to convert the capacitance (or capacitance difference) to be acquired into a voltage (C-to-V interfaces). The typical circuits used to obtain C-to-V conversion are: the trans-impedance amplifier (TI) [7-9], the switched capacitor (SC) charge amplifier [10-11,13] and the chopper (CH) amplifier [11,12]. SC and CH amplifiers are widely used for fully integrated CMOS interfaces, since they do not need generation and demodulation of sinusoidal waveforms and represent the best option when the highest accuracy and resolution have to be achieved. On the down side, the discrete nature of SC circuits makes them prone to noise fold-over, which, for a given noise specifications, results in increased power consumption. Charge injection, deriving from non ideal switch operation, is generally reduced using fully differential architectures that require additional circuits, (e.g. input common mode controls) to eliminate specific gain and offset errors [13]. Interfaces based on the CH amplifier are virtually immune to noise fold-over but should be followed by a time continuous low pass filter that seriously increases the occupied area.

In order to obtain a digital output, C-to-V interfaces have to be combined with an ADC, involving extra power and complexity. Sigma-delta (Σ-Δ) ADCs represent the optimal choice, since they can be easily embedded into the SC interfaces [13-17] and need minimal analog circuitry with respect to Nyquist rate converters. This advantage is partially compensated when on-chip high order decimation filters are used. As far as power consumption is concerned, the required high oversampling ratios make Σ–Δ ADCs a power efficient option only when low sampling rates are required.

A simpler alternative is represented by interfaces producing "quasi digital" signals [18], i.e. two-level signals where the information is given by either the frequency or pulse duration. Quasi digital signals are receiving a renewed interest, due to the simplicity of the related interfaces, the possibility of direct transmission over relatively noisy or non linear channels and the facility to convert them into real digital signals (coded) using only counters.

Capacitance-to-frequency (C-to-F) converters are probably the simplest interfaces for capacitive sensors [19,20]. Their compactness allows several distinct interfaces to be placed on the same chip [21]. Capacitance to pulse duration interfaces (C-to-D) are typically slightly more complex than C-to-F circuits [22,23], but provide easier interfacing to a microcontroller (MCU), since the frequency of the PWM signal can be synchronized to the MCU clock. Furthermore, a PWM signal can be converted into an analog voltage with a simple low pass filter.

The limit of the proposed C-to-F and C-to-D converters is mainly related to inaccuracy issues. In most cases the interface sensitivity is strongly dependent on the absolute value of one or more device parameters (such as a resistance) leading to unavoidable dependence on temperature [19-23]. Interesting methods to cancel the temperature dependence are proposed in [24-25,26] However, in order to extract the capacitance value, these circuits require algebraic operations involving the duration of distinct pulses, partly offsetting the simplicity of a pure PWM signal.

Recently, a fully integrated interface capable of producing a PWM signal with pulse duration linearly proportional to a capacitance has been presented [27]. The circuit, based on a double slope integration approach, exhibits intrinsically low temperature drift and low dependence on parasitic capacitances, but requires a relatively high supply current (nearly 5 mA), mainly due to bandwidth and stability requirements deriving from an OTA-based complex closed loop approach. An improved double slope interface, with much lower power consumption but requiring a grounded terminal for C_X and then much prone to parasitic capacitance interference was proposed in [28].

In this work, we present the analysis of a C-to-D converter that maintains the same advantages of [27] with two orders of magnitude lower power consumption. The circuit uses a compact architecture that uses only local feedback loops and incorporates chopper modulation to mitigate the effect of flicker noise and device mismatch. The circuit was initially proposed in [29], showing the effectiveness of the approach by means of simulations. A prototype has been designed and fabricated using devices from the 0.32 μm CMOS subset of the BCD6s process provided by ST Microelectronics. Preliminary measurements of the prototype characteristics were described in [30].

In this work, we present a deepened analysis of the proposed approach in order to show the impact of various circuit parameters on the system performances. The intrinsic low pass characteristic of the interface and its beneficial effect on the overall jitter is also highlighted. These important aspects were not dealt with in [29,30], while a very simplified noise analysis was described in [31], where a slightly improved circuit was also proposed. In addition to rigorous theoretical analysis of non idealities, this work includes also the results of new measurements regarding noise spectra and characteristic spread.

II. INTERFACE ARCHITECTURE AND OPERATION

The circuit topology and ideal operating principle was described in [29, 30] and will be briefly recalled here. The block diagram of the system is shown in Fig. 2, where the sensor has the same configuration as in Fig.1, while ck is a clock signal with 50 % duty cycle. The clock frequency is $f_{ck} = 1/T$.

The interface is designed to read positive ΔC values

($C_X > C_R$.). The output PWM signal, is indicated with p. Block RG (ramp generator) produces a triangular waveform, $V_S(t)$, of peak-to-peak amplitude ΔV_S, synchronous with the clock, while CA is a differential current amplifier with gain 1/2. Blocks SA1 and SA2 are switch arrays that connect their input port to the output port in a straight or crossed fashion depending whether the digital input (indicated by the inward arrow) is high or low, respectively. CMP is a low hysteresis comparator.
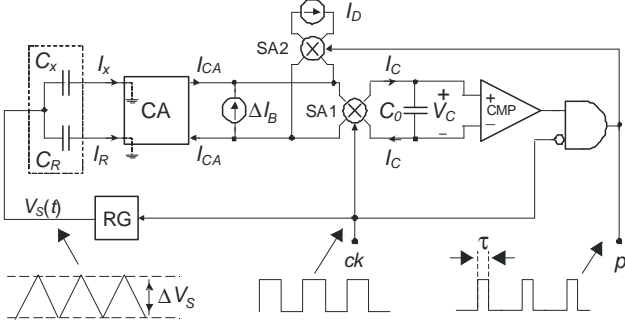

Fig. 2. Schematic block diagram of the proposed interface.

Current I_C, flowing into capacitor C_0, is the sum of contributions from currents I_{CA}, I_D and ΔI_B, which should satisfy the following design conditions:

$$\Delta I_B > I_D + \max|I_{CA}|; \qquad I_D > \max|I_{CA}|; \qquad (1)$$

Considering zero input impedance for the CA, current I_{CA} is given by:

$$I_{CA} = \frac{1}{2}(I_X - I_R) = \frac{1}{2}\frac{dV_S}{dt}\Delta C \qquad (2)$$

Depending on the logical values of ck and p, three different intervals, A, B, C can be distinguished, as shown in Table I. The case $ck=1$, $p=1$ is made impossible by the AND gate. The expression of current I_C, as resulting from the state of SA1 and SA2, is indicated for each interval. The first inequality in (1) guarantees that V_C increases in the first clock half-cycle (interval A) and decreases in the second half-cycle (intervals B,C). We have supposed that $V_C>0$ at the end of interval A, so that p turns high at the beginning of the second clock half-cycle, starting the output pulse. When V_C gets negative, p turns low, ending the output pulse. It can be easily shown that the system reaches the steady condition regardless of the initial state. More details are given in [29,30].

TABLE I
CONTRIBUTION TO I_C OF CURRENTS I_A, I_D, ΔI_B

Interval	Duration	ck	p	I_C	I_{CA}
A	$T/2$	1	0	$-I_D+\Delta I_B+I_{CA}$	$\Delta V_S \Delta C/T$
B	τ	0	1	$-I_D-\Delta I_B-I_{CA}$	$-\Delta V_S \Delta C/T$
C	$T/2-\tau$	0	0	$+I_D-\Delta I_B-I_{CA}$	$-\Delta V_S \Delta C/T$

Note that the signs of both I_{CA} and ΔI_B contributions to I_C are reversed at each clock transition for the effect of SA1. However, the I_{CA} sign is also alternated as a result of the V_S

slope reversal (see the rightmost column in Table I), so that the I_{CA} contribution is always positive across the whole clock period. Clearly, for the waveform V_C to be stationary, the net charge accumulated into C_0 over a clock period should be zero. The current ΔI_B gives a null contribution, due to the sign alternation produced by SA1. The charge contribution of I_{CA} is given by:

$$Q_{CA} = \frac{\Delta C}{2}\int_0^{\frac{T}{2}}\frac{dV_s}{dt}dt - \frac{\Delta C}{2}\int_{\frac{T}{2}}^{T}\frac{dV_s}{dt}dt = \Delta C \cdot \Delta V_S \qquad (3)$$

From Table I, the contribution of I_D is given by:

$$Q_D = -2\tau I_D \qquad (4)$$

Equating the total charge accumulated over a period (i.e Q_D+Q_{CA}) to zero, we obtain the pulse duration:

$$\tau = \Delta C \cdot \frac{\Delta V_S}{2I_D} \qquad (5)$$

Since $\Delta C\Delta V_S$ is equal to $|I_{CA}|T$, the second inequality in (1) guarantees that τ does not exceed $T/2$.

An aspect that is important to point out is that SA1 applies chopper modulation to the output current of the CA. This shifts the offset and flicker noise components across the clock frequency and its harmonics. These components are then strongly attenuated by integration of the currents in C_0. The overall result is the rejection of offset and flicker noise components introduced by the current amplifier. A rigorous investigation about the actual residual noise and its effect on the output pulse jitter is presented in Sect. III.

A simplified schematic view of block RG is shown in Fig. 3(a). The circuit is based on a Miller integrator, made up of the inverting amplifier M_{3M}-M_{6M} (dashed box in Fig.3), and feedback capacitor C_M. Two current sources, M_{1M} and M_{2M}, can be connected to the integrator input through M_{1S} and M_{2S}, respectively. V_{stop} is a reference voltage that sets the upper limit of the V_S waveform.
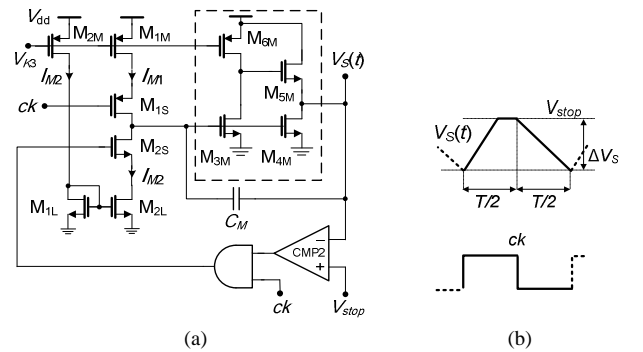
Fig. 3 Schematic view of the RG block (a) and output waveform (b).

In the first clock half-cycle, I_{M2} is integrated producing the increasing phase of V_S. The decreasing phase occurs in the second clock half-cycle, when I_{M1} is integrated. Stability of the DC value is obtained by making the increasing slope slightly larger than the decreasing one ($I_{M2}>I_{M1}$) and terminating I_{M2} integration when V_S reaches V_{stop}. The resulting waveform, shown in Fig.3(b) is reliably synchronous with the clock but not perfectly triangular. However, it can be easily shown that

Eqns. (3) and (5) are still perfectly valid and that:

$$\Delta V_S = \frac{T \cdot I_{M1}}{2C_M} \implies \tau = \frac{\Delta C}{C_M} \frac{I_{M1}}{4 I_D} T \tag{6}$$

In this way, we have obtained that the pulse width τ is proportional to the clock period and to ΔC, as desired. Note that only current and capacitance ratios appear in (6), thus a very small sensitivity to temperature can be expected, provided that a precise clock frequency is used.
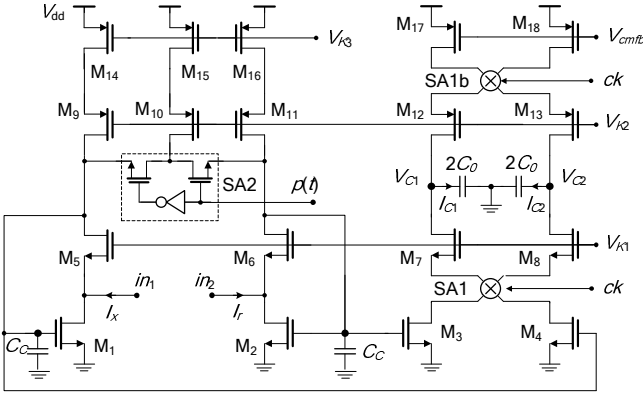

Fig. 4. Schematic view of the current amplifier CA, including also the function of I_D and ΔI_B current sources and switch arrays SA1, SA2.

Fig. 4 shows the circuit designed to perform the functions of blocks CA, SA1, SA2, and of current sources I_D and ΔI_B. Currents I_X and I_R enter the CA at the points indicated in Fig.4 with in_1 and in_2. The required low input impedance is provided by local feedback loops, involving only M_1, M_5 in one branch and M_2, M_6 in the other. The feedback loops are compensated by capacitors C_C.

The currents in M_1 and M_2 are mirrored with unity gain to M_4 and M_3, respectively. Therefore:

$$I_{D3} = I_r + I_{D16} + p \cdot I_{D15}$$
$$I_{D4} = I_x + I_{D14} + \overline{p} \cdot I_{D15} \tag{7}$$

The integrating capacitor, C_0 in Fig. 1, is replaced by two grounded capacitors of value $2C_0$. Due to stabilization of the output common mode voltage, $I_{C2} = -I_{C2}$, so that:

$$I_C \equiv I_{C1} = \frac{I_{D8} - I_{D7}}{2} \tag{8}$$

Finally, considering that $I_{D8} - I_{D7}$ is equal to $\pm(I_{D4} - I_{D3})$, depending on the configuration of switch SA1, i.e. on the clock value, we can substitute Eqns. (7) into (8), obtaining:

$$I_{C1} = I_C = m_1 \cdot \left(\frac{I_x - I_R}{2} + \Delta I_B + m_2 \cdot I_D \right) \tag{9}$$

where m_1 is -1 or 1 when ck is a logical "0" or "1", respectively, while $m_2 = -1$ when p is 0 and $m_2 = 1$ when p is 1. Furthermore, the following substitutions have been operated: $2\Delta I_B = I_{D14} - I_{D16}$, $2I_D = I_{D15}$. It is easy to show that (9) represents also the behavior of the block diagram in Fig. 2. It is worth noting that ΔI_B is obtained by making M_{14} and M_{16} (i.e. I_{D14} and I_{D16}) different by design. Switch array SA1b has been added to extend chopper modulation to the currents

produced by M_{18} and M_{17}.

III. ANALYSIS OF NON IDEALITIES

The main sources of non-idealities are (i) finite input impedance of the current amplifier and (ii) noise. The effect of the former is an increased sensitivity to temperature and process variations, while noise is responsible for the jitter on the output pulse duration.

A. Finite input impedance.

The small signal representation of one CA input port (in_1) is shown in Fig. 5. The output resistance of the cascode mirror providing the bias current (M9-M14 in Fig.4) has been considerate infinite with respect to r_{d5}. Capacitances C_X and C_R are substituted by their maximum value (C_{XM}) to represent the worst case.
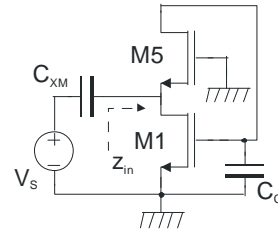

Fig. 5. Small signal representation of the CA input port.

Analysis of the circuit yields the following simplified expression for the frequency dependent input impedance (z_{in}):

$$z_{in} = \frac{1}{g_{m5}} \frac{1}{g_{m1} r_{d5}} \left(1 + j\omega C_C r_{d5} \right) \cong j\omega \frac{1}{g_{m5}} \frac{C_C}{g_{m1}} \tag{10}$$

where the approximation in the rightmost hand is valid for frequencies much higher than $(2\pi C_C r_{d5})^{-1}$. This condition is reasonably valid at the frequency of the input waveform, which is of the order of several kHz. If z_{in} is not negligible with respect to the minimum sensor impedance (represented by $1/j\omega C_{XM}$) then expression (2) should be modified to include a term dependent on z_{in} itself. As a result, due to the dependence of z_{in} on MOSFET transconductances, the sensitivity to temperature and process variations would be degraded. To minimize this problem, we will impose that:

$$|z_{in}| \cong \omega \frac{1}{g_{m5}} \frac{C_C}{g_{m1}} = \frac{1}{\alpha_Z} \frac{1}{\omega C_{XM}} \tag{11}$$

with $\alpha_z \gg 1$. Expression (11) can be further transformed by considering stability of the local feedback loops used in the input ports just to reduce z_{in}. Simple investigation of the circuit in Fig. 5 shows that unity gain angular frequency (ω_0) of the loop and its first non-dominant pole frequency (ω_2) are given by $\omega_0 = g_{m1}/C_C$ and $\omega_2 = g_{m5}/C_{XM}$, respectively. Imposing that $\omega_2 = 3\omega_0$ to get a reliable phase margin (about 70°), equation (11) becomes:

$$\frac{g_{m5}}{C_{XM}} = \sqrt{3\alpha_Z} \, \omega \tag{12}$$

Expressing g_{m5} as $2I_{D5}/(V_{GS}-V_t)_5$, and considering that $I_{D5} = I_{BIAS}$, the following expression can be derived:

$$I_{BIAS} = \sqrt{3\alpha_Z}\,(V_{GS} - V_t)_5\, C_{XM}\,\pi f_{ck} \tag{13}$$

Equation (13) can be used in the design phase to calculate the required amplifier bias current for a given sensor impedance to input impedance ratio (α_Z). This will be recalled at the end of this section to simplify the expression of the jitter. Note that a low input impedance, establishing virtual ground at the CA inputs, is also important to reject the effect of parasitic capacitances between the sensor terminals and ground.

B. Mechanism of noise generation

As far as noise is concerned, the clock signal will be considered ideal, so that the fluctuation on the pulse width will be ascribed only to the jitter on the trailing edge. In order to determine the mechanism of jitter generation, it is convenient to focus on the measurement cycle, defined as the time interval between two successive trailing edges of the output pulse. Fig 6 shows the behavior of voltages ck, p and V_C in the n-th measurement cycle, beginning and ending at instants t_1 and t_2, respectively. The origin of the time axis is chosen as shown in Fig.6, so that the n-th pulse starts at nT. The sequence formed by the durations of the output pulses is treated as a discrete time signal, indicated as $\tau(n)$. The three intervals A, B, C, forming the measurement cycle, have been named coherently with Table I.

Noise on the comparator threshold, V_{cmp}, causes the measurement cycle to begin and end at two different values of voltage V_C, as clearly represented in Fig.6.
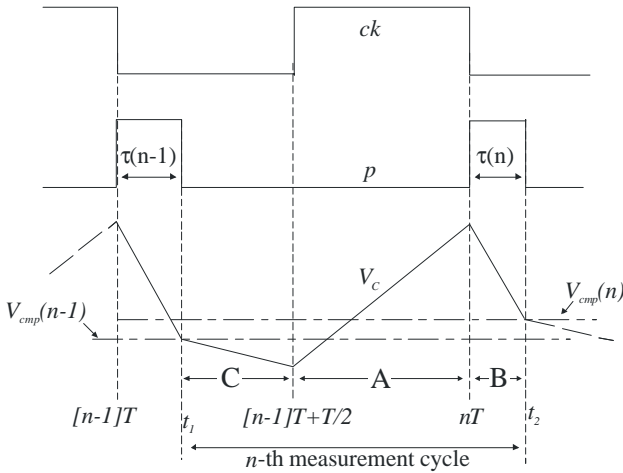

Fig. 6. Waveform V_C between two successive pulse trailing edges.

Indicating with I_C the ideal (noiseless) current flowing through capacitor C_O and with i_c the noise component superimposed to I_C, the following equation holds:

$$\int_{t_1}^{t_2} I_C\, dt + \int_{t_1}^{t_2} i_c\, dt = C_O \left[V_{cmp}(n) - V_{cmp}(n-1) \right] \tag{14}$$

The ideal component I_C is the sum of contributions from components ΔI_B, I_D and I_{CA}. The expressions of I_C in the three intervals of Fig. 6 are summarized in Table II, where the contribution of I_{CA} is represented by current I_A, given by:

$$I_A \equiv <\left| I_{CA} \right|> = \frac{\Delta V_S}{T}\,\Delta C \tag{15}$$

Note that Table II is a generalization of Table I for the case that the pulse width is not stationary.

TABLE II
CONTRIBUTION TO I_C OF CURRENTS I_A, I_D, ΔI_B (NON STATIONARY CASE)

Interval	Duration	I_C
A	$T/2$	$-I_D + \Delta I_B + I_A$
B	$\tau(n)$	$-I_D - \Delta I_B + I_A$
C	$T/2 - \tau(n-1)$	$I_D - \Delta I_B + I_A$

Summing up the charge contribution in the three zones, the following expression can be easily found:

$$\int_{t_1}^{t_2} I_C\, dt = \left(\Delta I_B - I_A - I_D \right)\tau(n-1) - \left(\Delta I_B - I_A + I_D \right)\tau(n) + T I_A \tag{16}$$

As far as the noise current i_c is concerned, its contribution in (14) can be represented by a random noise charge $q_{IC}(n)$ defined as:

$$q_{IC}(n) \equiv \int_{t_1}^{t_2} i_c\, dt \cong \int_{t_2-T}^{t_2} i_c\, dt \tag{17}$$

where the approximation of integrating over an exact clock period (T) introduces a negligible error if the following conditions hold:

$$\left| i_c \right| << \left| I_C \right| \quad \text{and} \quad \left| \tau(n) - \tau(n-1) \right| << T \tag{18}$$

The effect of comparator noise can be also modeled as a charge $q_{CP}(n)$ defined by:

$$q_{CP}(n) = C_O \left[V_{cmp}(n) - V_{cmp}(n-1) \right] \tag{19}$$

Combining (14-17) and (19) we obtain the difference equation:

$$a\tau(n) - b\tau(n-1) = \frac{T \cdot I_A + q_{IC}(n) - q_{CP}(n)}{2 I_D} \tag{20}$$

where:

$$a = \frac{\left(\Delta I_B - I_A + I_D \right)}{2 I_D}; \quad b = a - 1 \tag{21}$$

Equation (20) determines the sequence $\tau(n)$ produced by the forcing terms, represented in the right hand of (20) by the ideal stimulus $T \cdot I_A / 2 I_D$, and by the noise charge sequences $q_{IC}(n)$ and $q_{CP}(n)$.

Note that the ideal stationary solution, given by (5), can be also derived from (20) and (15), imposing $\tau(n) = \tau(n-1)$ and turning off the noise charges q_{IC} and q_{IP}.

Here we are interested in calculating the jitter $\tau_N(n)$ superimposed to the ideal solution. The analysis will be performed considering that ΔC is constant, thus also I_A and coefficients a and b in (20) are constant. In this way, it is possible to apply the discrete Fourier transform to (20), obtaining:

$$\tau_N(j\omega) = H(j\omega)\frac{q_{IC}(j\omega) - q_{CP}(j\omega)}{2I_D} \tag{22}$$

where, $\tau_N(j\omega)$, $q_{IC}(j\omega)$ and $q_{CP}(j\omega)$ are the discrete Fourier transforms of the sequences $\tau(n)$, $q_{IC}(n)$ and $q_{CP}(n)$, respectively, while $H(j\omega)$ is obtained by substituting $e^{j\omega T}$ into the Z-domain transfer function:

$$H(Z) = \frac{1}{a - bZ^{-1}} \tag{23}$$

derived from (20) by means of simple algebraic passages. Equation (22) represents an important result since it provides a method to derive the discrete power spectral density (D-PSD) of the jitter from the D-PSD of the noise charges by simple multiplication by $|H(j\omega)|^2$. Furthermore, since $q_{IC}(n)$ and $q_{CP}(n)$ can be reasonably considered independent stochastic processes, their contributions are additive and can be separately determined. The plot of $|H(j\omega)|^2$ vs. frequency in the interval $0.01f_{ck}$-$0.5f_{ck}$ is shown in Fig. 7 for various values of parameter a. Note that $H(j\omega)$ attenuates the high frequency components of the noise. The effect is stronger at higher values of parameter a. Equation (21) suggests that a can be increased by increasing the ratio of ΔI_B with respect to I_D and I_A. Considering (21) and (23) it can be easily shown that $H(Z)$ is stable for $a>0.5$ Design condition (1) guarantee that a is greater than one, thus $H(Z)$ cannot get unstable.
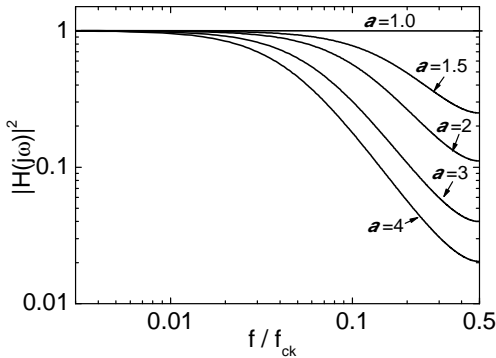

Fig.7. Frequency dependence of $|H(j\omega)|^2$ for varuius values of parameter a.

It should be observed that (20) implies also a low pass function for the signal term $TI_A/2I_D$. In particular, it can be easily shown that the small signal transfer function of the interface is proportional to $H(z)$. Thus, increasing a produces a benefit in terms of noise but also limits the signal bandwidth. Modeling of this effect for large signals is not as straightforward since the signal I_A is also present in coefficients a and b, that, in this case, cannot be assumed to be constant.

C. Contribution of the noise currents

In this paragraph, the dependence of the D-PSD of q_{IC} on the contributing current noise power spectral densities (PSDs) will be analyzed. First, indicating with $S_{IC}(f)$ the PSD of the total noise current i_c, and with $S_{QC}(f)$ the D-PSD of the noise charge q_{IC}, and using simple signal theory concepts, the following expression can be derived from (17):

$$S_{QC}(f) = \sum_{k=-\infty}^{+\infty} T^2 \text{sinc}^2[\pi T(f - kf_{ck})]S_{IC}(f - kf_{ck}) \tag{24}$$

where $\text{sinc}(x)=\sin(x)/x$. Since $S_{QC}(f)$ is a D-PSD, it is sufficient to consider its behavior only in the interval 0-$f_{ck}/2$. The noise current i_c can be expressed as the sum of three contributions:

$$i_C = [i_{CA} + (\Delta C/2C_M)i_R]m_1(t) + i_D \cdot m_2(t) \tag{25}$$

where i_{CA} is the output noise current of the CA block, i_R is the noise superimposed to the current integrated by the RG block to produce the waveform V_S (see Fig.3), and i_D is the noise superimposed to I_D. We will indicate with $S_{IA}(f)$, $S_{IR}(f)$ and $S_{ID}(f)$ the PSDs of i_{CA}, i_R and i_D, respectively. Modulation by the dimensionless signals $m_1(t)$ and $m_2(t)$, depicted in Fig.8, results from the combined effect of SA1 and SA2.
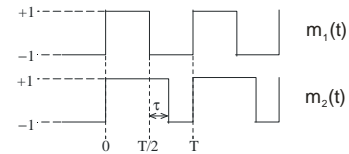

Fig.8. Representation of the dimensionless signals $m_1(t)$ and $m_2(t)$.

Note that $m_1(t)$ is a signal with zero mean value, so that its effect on i_{ca} is equivalent to a chopper modulation. According to [32], the result is a spectrum with a constant value $S_{IA}(f_{ck})$ except for small frequency intervals centered on clock odd harmonics, across which the amplifier d.c offset and flicker noise contributions are shifted. Since the sinc^2 weighting function nulls for every f_{ck} harmonics, these frequency intervals can be neglected and we can consider that the sinc^2 function is multiplied by just the constant term $S_{IA}(f_{ck})$. This would be strictly correct only if the CA bandwidth were infinite. However, the sinc^2 function rapidly decreases at high frequencies, thus the error produced by this approximation is reasonably small. Using this assumption into (24) and applying the following identity:

$$\sum_{k=-\infty}^{+\infty} \text{sinc}^2[\pi T(f - kf_{ck})] = 1 \tag{26}$$

the contribution of i_{CA} to the $S_{QC}(f)$ D-PSD turns out to be simply a constant spectrum equal to $T^2S_{IA}(f_{ck})$ in the whole frequency interval 0-$f_{ck}/2$.

The effect of $m_2(t)$ on i_D is less straightforward, since $m_2(t)$ depends on the impulse τ. If τ is zero, the mean value of $m_2(t)$ is zero as well, thus a pure chopper modulation occurs. If τ assumes its maximum value $(T/2)$, $m_2(t)$ is constantly equal to 1, so that the spectrum of i_D is left unchanged, including all the low frequency components. We will perform the analysis choosing this worst case. In addition, the sinc^2 function in (24) does not significantly alter the low frequency components, since it stays close to one over a relatively wide interval around the origin. For the flicker components only the replica with $k=0$ has to be considered in (24), owing to the $1/f$-like decrease of this kind of noise. On the other hand, thermal noise contributions are constant over a wide band and can be treated using (26). The result is that also the thermal noise

components are unaltered, thus the contribution of i_D to S_{QC} can be assumed to be simply equal to $T^2 S_{ID}(f)$.

The effect of i_R is the most complicated of the three to be studied. The following considerations apply: (i) i_R is actually the noise component of two distinct currents, namely I_{1M} and I_{2M}, acting in different clock half-cycles; (ii) the charge integrated by i_{2M} (noise component of I_{2M}) in its own half-cycle is opposite to that accumulated by i_{1M} in the previous half cycle, since the comparator CMP2 (that we will consider ideal for simplicity) stops the integration of I_{2M} when the voltage V_S has returned to the starting point; (iii) the sign of the charge accumulated by i_{2M} is reversed by $m_1(t)$ so that the charge contribution of i_{2M} into C_O simply duplicates the charge integrated by i_{1M} in the previous half cycle; (iv) I_{1M} and I_D are derived from the same reference source using current mirrors so that, considering (6), noise contributions from shared devices produce correlated effects that cancels out in the expression of τ.

The consequence of point (iii) is that i_R produces an effect equivalent to a noise current equal to $(\Delta C/2C_M)i_{1M}$, directly flowing into C_O with no chopper modulation effects. With the same considerations for i_D, we can reduce the action of (24) on the i_{1M} spectral contribution to a simple multiplication by T^2. The final expression deriving from the above consideration is:

$$S_{QC}(f) = T^2 \left[S_{IA}(f_{ck}) + S_{ID}(f) + (\Delta C/2C_M)^2 S_{IM}(f) \right] \quad (27)$$

where the PSD of i_{1M} has been indicated with $S_{IM}(f)$. The latter, similarly to S_{ID}, contributes to S_{QC} with also the flicker noise components. Fortunately, due to point (iv), only the uncorrelated components have to be considered in S_{ID} and S_{IM}. In practice, only the output MOSFETs of the corresponding current mirrors (M_{1M} in Fig.3 and M_{15} in Fig.4) contribute to S_{QC} and should be sized accordingly.

The thermal noise components of the three current PSDs have been calculated by approximating the current noise of the single MOSFETs with the saturation expression $S_I = 8/3 k_B T_A g_m (1+n_B)$, where k_B is the the Boltzmann constant, T_A the absolute temperature, and n_B the body effect coefficient, typically of the order of 0.2. The MOSFET transconductance is calculated using the drain current square law approximation, from which: $g_m = 2I_{DS}/(V_{GS}-V_t)$. The flicker current noise PSD, S_{IF}, is calculated with the expression: $f \cdot S_{IF} = g_m^2 N_F / WL$ where N_F is a process dependent constant and WL the gate area.

Considering that the clock frequency is high enough to neglect flicker noise in $S_{IA}(f_{ck})$, the following expression can be derived:

$$S_{IA}(f_{CK}) \cong \frac{2}{3} m_A (1+n_B) \frac{2I_{BIAS}}{(V_{GS}-V_t)_A} k_B T_A \quad (28)$$

where m_A is the number of devices that significantly contribute to the output noise (MOSFETs 1,2,3,4,14,16,17,18 in Fig. 4, i.e. $m_A=8$), which have been supposed to be biased with the same overdrive voltage $(V_{GS}-V_t)_A$ and d.c. bias current (I_{BIAS}). It can be easily shown that the noise current sources of

all these devices are transferred to the output current i_{CA} through a factor 0.5.

The thermal noise contribution of I_D and I_M can be neglected with respect to $S_{IA}(f)$ since these currents are set to a much smaller value than I_{BIAS}. We will consider their flicker contributions that, summed up, give:

$$S_{ID}(f) + (\Delta C/2C_M)^2 S_{IM}(f) \cong 2 \frac{4N_F I_D^2}{W_D L_D (V_{GS}-V_t)_D^2} \frac{1}{f} \quad (29)$$

where expression (6) has been used for the factor $(\Delta C/2C_M)$ with $\tau = \tau_{max} = T/2$ (worst case) to simplify the result. $W_D L_D$ and $(V_{GS}-V_t)$ are the gate area and overdrive voltage of I_D current source output MOSFET (M_{15}), assumed identical to that of the I_{M1} current source.

D. Contribution of comparator

The charge sequence given by (19) can be considered as the result of two operations: (i) sampling of the comparator noise at a rate that, neglecting the jitter, coincides with the clock frequency; (ii) extraction of the first difference from the sequence obtained by the sampling process. The first step produces thermal noise fold-over in the interval 0-$f_{ck}/2$, while, due to their band limited nature, low frequency components are not affected by aliasing. The difference operation introduce multiplication of the resulting spectrum by $\sin^2$ weighting function that practically rejects low frequency components, including flicker noise and possible comparator offset. The D-PSD of the comparator contributions can be then approximated by the formula:

$$S_{QCP}(f) = 4C_0^2 \sin^2\left(\pi \frac{f}{f_{CK}}\right) \frac{2B_C}{f_{CK}} S_{CBB} \quad (30)$$

where S_{CBB} and B_C are the comparator input referred broad band noise (thermal noise) and bandwidth, respectively.

E. Total jitter estimation.

A first interesting step is the calculation of the jitter D-PSD. From (22):

$$S_{\tau N}(f) = |H(j2\pi f)|^2 \frac{S_{QC}(f) + S_{QCP}(f)}{4I_D^2} \quad (31)$$

We will first assume that the comparator contribution is negligible, since, due to the form of (30), S_{QCP} includes only high frequency components which, in turn, are reduced by the low pass characteristics of $H(j\omega)$ (see Fig.7) when a>1. As far as S_{QC} is concerned, it is useful to calculate the flicker noise corner frequency, at which the $1/f$ component given by (29) is equal to the frequency independent contribution of (28). Note that, according to (5), if the clock frequency is varied, I_D should be adjusted to maintain an ideal duty-cycle excursion. Using the I_D value for which τ reach $T_{CK}/2$ for $\Delta C = \Delta C_{FS}$, the following result can be obtained:

$$f_k = \frac{6\Delta V_S}{m_A(1+n_B)} \frac{N_F}{W_D L_D} \frac{\Delta C_{FS}}{k_B T_A} \left(\frac{I_D}{I_{BIAS}}\right) \frac{(V_{GS}-V_t)_A}{(V_{GS}-V_t)_D^2} f_{ck} \quad (32)$$

With typical values for the process and design parameters in (32), corner frequencies several orders of magnitude smaller

than the clock frequency can be obtained even with moderate gate areas $W_D L_D$. For this reason and for the sake of simplicity, we will also neglect the contribution of currents I_M and I_D.

Therefore, the D-PSD of the jitter can be approximated by:

$$S_{\tau n}(f) \cong T^2 \frac{S_{IA}(f_{CK})}{4 I_D^2} |H(j 2 \pi f)|^2 \tag{33}$$

In order to determine the dynamic range of the interface the quantity of interest is the *rms* value of the jitter τ_N, coinciding with the standard deviation σ_τ of the output pulse. Normalizing σ_τ to the full scale value of the output pulse $\tau_{FS} = \Delta C_{FS} \Delta V_S / 2 I_D$, the inverse of the dynamic range can be derived. Integrating the spectral density in (33) over the interval 0-$f_{ck}/2$ we get:

$$\left(\frac{\sigma_\tau}{\tau_{FS}}\right)^2 = T^2 \frac{S_{IA}(f_{CK})}{\Delta C_{FS}^2 \Delta V_S^2} \int_0^{f_{ck}/2} |H(j 2 \pi f)|^2 df \tag{34}$$

Using (28) for $S_{IA}(f_{ck})$ and considering that:

$$\int_0^{f_{CK}/2} |H(j 2 \pi f)|^2 df = \frac{1}{2T(2a-1)} \tag{35}$$

the following expression is obtained:

$$\left(\frac{\sigma_\tau}{\tau_{FS}}\right)^2 = \frac{2 m_A (1 + n_B)}{3(2a-1)} \frac{I_{BIAS}}{f_{ck} (V_{GS} - V_t)_A} \frac{k_B T_A}{\Delta C_{FS}^2 \Delta V_S^2} \tag{36}$$

This result seems to indicate that increasing the clock frequency $(1/T)$ would be a viable method to reduce the relative jitter. Actually, if f_{ck} is increased, I_{BIAS} has to be increased as well, to satisfy condition (13) on the input impedance. Substitution of (13) into (36) results in the following interesting design relationship:

$$\left(\frac{\sigma_\tau}{\tau_{FS}}\right)^2 = \frac{2 \pi \sqrt{3 \alpha_Z}}{3(2a-1)} m_A (1 + n_B) \frac{C_{XM}}{\Delta C_{FS}} \frac{k_B T_A}{\Delta C_{FS} \Delta V_S^2} \tag{37}$$

where we have supposed that $(V_{GS}-V_t)_5 = (V_{GS}-V_t)_A$ for simplicity. The most important quantity in (37), is the ratio between the equivalent kT/C noise (mean square voltage) associated to the full scale sensor capacitance value and the square of the ramp peak-to-peak amplitude (ΔV_S). A penalizing factor is the ratio $C_{XM}/\Delta C_{FS}$, since C_{XM} (maximum value of capacitor C_X) can be affected by large offset capacitances (C_{X0}). In practical sensors, this ratio may be significantly greater than one. The clock frequency does not affect the noise performances of the circuit, at least until the assumptions made remain valid. Reducing the clock frequency improves power consumption through (13) but, beside obvious limitations on the available signal bandwidth, a noise increase will eventually occur when f_{ck} gets lower than the flicker noise corner frequency of the current amplifier, producing an increase of $S_{IA}(f_{ck})$ with respect to the value indicated by (28), where only the thermal contribution was taken into account.

IV. PROTOTYPE DESIGN AND EXPERIMENTAL RESULTS

A prototype has been designed using the $0.32\,\mu m/3.3$ V CMOS device subset of the STMicroelectronics process BCD6s. Several circuit functions can be tuned by changing a digital configuration word (24 bit) stored in internal registries accessed by means of a three-wire serial interface.

A programmable dummy sensor was included into the chip to facilitate the circuit characterization. C_R is implemented by a 500 fF capacitor while C_X was the sum of a constant capacitance, identical to C_R, and a variable capacitor made up of four binary weighted capacitors that could be selectively connected in parallel. The total differential capacitance ΔC could be varied from 16 to 256 fF with step 16 fF through four configuration bits. Due to the required small capacitance values, non-standard capacitors were designed using overlaps of the three available metal layers. All capacitance values were obtained by parallel connection of a single elementary capacitor. Polysilicon/n^+-implant capacitors have been used for C_0 and C_M. Blocks CMP1 and CMP2 are conventional low hysteresis comparators. Switch arrays SA1 and SA1b are implemented by means of n and p MOSFETs, respectively. Minimum size devices have been used to implement all the switches, in order to reduce charge injection. The circuit was designed to work with an external 30 kHz–50% duty cycle clock signal, from which the non overlapped clock phases, required to drive switch arrays SA1 and SA2, are internally generated. The main waveforms have been routed to diagnostic pads through low input capacitance buffers. A separate power supply line has been used for the buffers and the serial interface in order to allow power consumption measurement of just the proposed circuit.

Table III shows the size of the main transistors and the values of C_0 and C_M capacitors. All the currents in the circuit have been derived from a single reference source (threshold voltage referenced source [33]) by means of precision current mirrors. The nominal values of the relevant currents are presented in Table IV. Since I_{M1}, I_D and ΔI_B are digitally adjustable, the corresponding tuning range and number of control bits is specified in Table IV. Current tuning has been accomplished by varying the effective width of M_{1M-2M}, and M_{14-16} across the ranges reported in Table III. Digitally controlled parallels of MOSFETs have been used to produce the effective width variation indicated in Table III.

The value of I_{BIAS} results from (13) with $(V_{GS}-V_t)_5 = 0.2$ V, $C_{XM} = 0.75$ pF (maximum value) and $\alpha_z = 10^3$. Equation (6) was used to set the range of I_{M1} in order to keep ΔV_S within the maximum output swing of block RG (1.2 V) for all process corners.

TABLE III.
PROTOTYPE DESIGN DATA (W/L IN MICRONS)

Ramp Generator (SG)		Current Amplifier (CA)			
M_{1M}	10-18/50	M_{1-4}	4/12	M_{14}	56-53/50
M_{2M}	10-18/50	M_{5-8}	2/2.5	M_{15}	3-9/100
M_{3M}	2.5/8	M_9	43.5/10	M_{16}	44-47/50
M_{4M}	5/8	M_{10}	7.5/20	M_{17-18}	4/4
M_{5M}	4/2	M_{11}	36.8/10	C_0	0.5 pF
M_{6M}	50/50	M_{12}, M_{13}	4/1	C_M	3 pF

The ranges of I_D and ΔI_B were chosen in order to satisfy (1) when the maximum value of I_{CA}, calculated with (2), was present (for $\Delta C = \Delta C_{FS} = 256$ fF). The voltage V_{stop} (see Fig.3) was set to 1.25 V. Such a low value was required to prevent M_{5M} from being switched off.

TABLE IV
VALUES OF THE RELEVANT CURRENTS

Current	Value (nA)	Control bits
I_{BIAS}	700	-
I_{M1}	150-250	4
I_D	10-30	4
ΔI_B	40-85	2

An optical micrograph of the whole prototype cell, including the dummy sensor, bias sources and diagnostic buffers is shown in Fig.9. Dimensions are 1025×515 μm^2.

The chips, packaged into 32 pin ceramic cases, have been characterized with the experimental set-up shown in Fig.10.
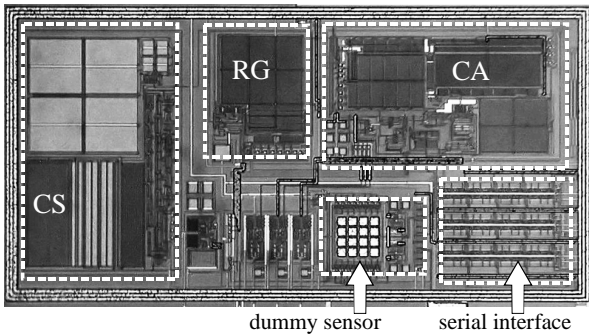

Fig. 9. Layout of the prototype cell with the main blocks indicated. CS: current source; RG: ramp generator; CA: current amplifier.
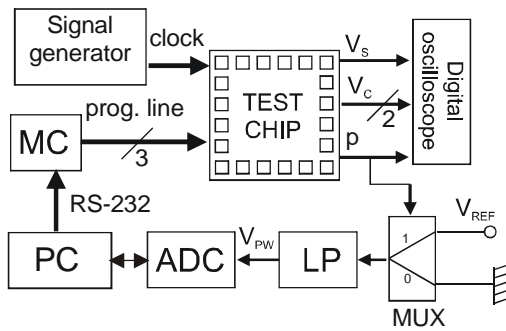

Fig. 10. Experimental set-up used to characterize the test chips.

The clock is provided by a HP 33120A signal generator while a digital oscilloscope (Tektronix TDS220) has been used to display and acquire the main circuit waveforms. To obtain the signal V_C, both differential lines V_{C1} and V_{C2} (see Fig.4) were acquired and the difference was calculated by numerical post-processing of the data. The duty-cycle of the output pulse (τ/T) has been estimated by converting it into a voltage (V_{pw}) with the simple approach shown in Fig.10: the block MUX (implemented with an analog switch) produces a waveform with the same behavior of the output PWM signal p, but with

the high level equal to the precise reference voltage V_{REF} (3 V). The average voltage V_{PW}, extracted by the low pass filter LP is equal to $(\tau/T)V_{REF}$. The signal V_{PW} is digitalized with 16 bit resolution using a computer controlled acquisition system (Pico Technology Ltd. ADC216). The LP filter is characterized by a 5th order Butterworth frequency response with 10 kHz bandwidth. A program running on a personal computer (PC) is used to calculate the power spectrum of the voltage V_{PW}. The on-chip registers were programmed from the PC through a purposely built board equipped with an Analog Devices ADuC847 microcontroller used to drive the serial interface. The power supply was set to 3.0 V and the clock frequency to 30 kHz in all tests.

Several configurations of the control bits were explored in order to find the best operating conditions. The value of current I_{M1} was chosen to obtain the maximum amplitude of the waveform V_S (limited by V_{stop} to 1.25 V), and, according to (36), minimize the relative jitter. A best value of 200 nA, (nominal value) resulting in $\Delta V_S = 1.1$ V was found. The current I_D sets the output pulse range through (6) but does not affect the relative jitter. Thus the midscale value $I_D = 20$ nA, was chosen. These I_D and I_{M1} settings were left unchanged in all the experiments performed on the prototype. The current ΔI_B was varied to verify its effect on the filtering function $H(j\omega)$. When not explicitly specified, ΔI_B was set to 55 nA.
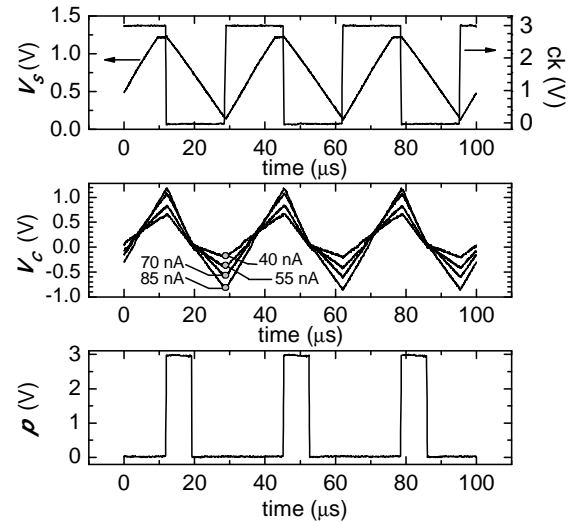

Fig. 11. Experimental waveform measured on the test chip with $\Delta C = 160$ fF.The parameter in the V_C plot is the current ΔI_B.

Fig. 11 shows the main waveforms in the circuit for $\Delta C = 160$ pF. The various curves of voltage V_C refer to different ΔI_B values, indicated in the figure. The output waveform p has been recorded for $\Delta I_B = 55$ nA; curves obtained with different ΔI_B values are practically indistinguishable on the scale of Fig.11.

The dependence of the pulse width on the differential capacitance ΔC is shown in Fig. 12 for 11 different samples. These measurements have been performed at room temperature. The sensitivity to temperature over the interval

0-80 °C was 300 ppm/°C [30]. Histograms of the offset and sensitivity errors, estimated from the curves of Fig. 12, are shown in Fig. 13.
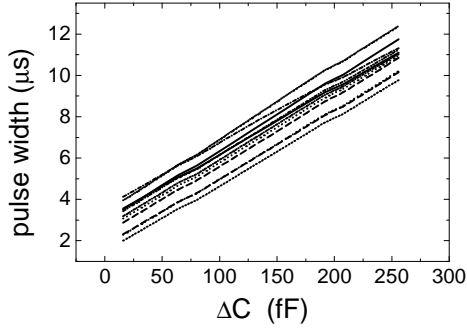

Fig. 12. Dependence of the output pulse duration as a function of the sensor differential capacitance, measured on a set of 11 different chips.
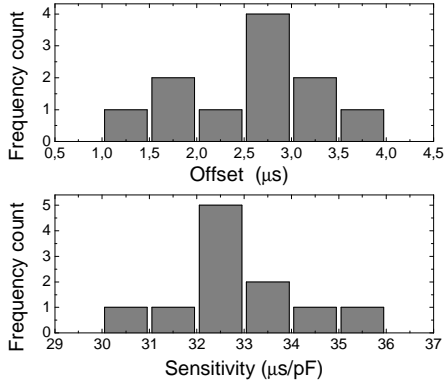

Fig. 13. Offset and sensitivity histograms estimated over the same sample set of Fig. 12.

The average sensitivity, calculated over the measured samples is 32.8 μs/pF, which is 18.4% higher than the theoretical value of 27.7 μs/pf predicted by (6). The discrepancy may be ascribed to possible uncertainties of the dummy capacitor values deriving from the use of custom cells. The visible systematic offset (around 2.5 μS) can be due to unwanted parasitic capacitive coupling between internal interconnects of the dummy capacitor. In addition to the systematic error, a significant dependence on process errors can be evinced from Fig.13. It should be pointed out that, with the present configuration, it is not possible to distinguish the contribution of the interface from that of the dummy sensor. As far as the interface is concerned, contributions to random errors are likely to derive from gain errors of the various current mirrors. In particular, the input mirrors of the CA (M1-M3 and M2-M4) handle the input currents I_X and I_R, which include a large common mode component, due to the common mode capacitance C_{X0}. Gain mismatch between the input current mirrors results in imperfect cancellation of the common components, producing an offset error. The latter, being modulated like the input signal, is not rejected by SA1. Inspection of Table III shows that there is margin to increase

the area of critical devices in order to reduce mismatch errors.

It is worth noting that the offset and gain errors were never as high as to produce saturation of the interface. In a real application, offset trimming can be achieved by introducing digitally variable capacitors in parallel to both the sensor capacitances C_X and C_R, while gain trimming can be obtained by varying C_M, I_{M1} or I_D.

The other important aspect to be taken into account is the effect of noise, visible as a jitter on the output pulse trailing edge. We have estimated the spectral density of the jitter by measuring the PSD of voltage V_{PW}, derived from the PWM output signal with the method shown in Fig.10. The relationship between the noise spectral density of the output pulse width ($S_{\tau N}$) and the spectral density of V_{PW} (S_{VPW}) is given by:

$$S_{VPW}(f) = \frac{S_{\tau N}(f)}{T^2} V_{REF}^2 \qquad (38)$$

The spectral density has been estimated by means of a standard algorithm running on the PC. Since the sequence $\tau(n)$ can be considered as a discrete time signal, only frequencies up to $f_{ck}/2$ (15 kHz) are significant. The LP filter effectively suppresses components at the clock frequency and higher order harmonics, preventing them from being aliased back to the band of interest through the ADC sampling function. The filter response has been experimentally characterized, obtaining an accurate interpolation function that has been used to correct the measured spectra. The background noise of the system was two orders of magnitude lower than the measured PSDs. The spectra have been recorded with ΔC=160 fF, varying ΔI_B. The results are shown in Fig. 14 for the four indicated ΔI_B values. According to (33), the frequency dependence of $S_{\tau N}$ (i.e. S_{VPW}, which is proportional to $S_{\tau N}$) is given by $|H(j\omega)|^2$. For each ΔI_B value, we have calculated the nominal value of parameter a, using (21) with I_A=5.3 nA, obtained from (15). The respective $|H(j\omega)|^2$ functions have been multiplied by a constant, equal to the noise level estimated in the almost flat region visible in the interval 100Hz−1kHz, where flicker noise is still negligible. In this way, the fitting curves shown in Fig.14 (smooth solid lines) have been obtained. The intrinsic low pass function is confirmed and a good agreement with the frequency response predicted by (33) can be observed.

The asymptotic noise level at low frequencies (in the absence of flicker noise) can be calculated using (33) and (38) with the S_{IA} value given by (28). With the design parameters reported in this section, a value of 1.0×10^{-9} V^2/Hz is obtained. This value is nearly 62 % of the measured noise level. The discrepancy has to be ascribed to the simple noise and current models used to derive (28). As far as flicker noise is concerned, a corner frequency equal to nearly 20 Hz can be estimated. This result is in agreement with the prediction of corner frequencies being much smaller than the clock frequency (see Sect. III).
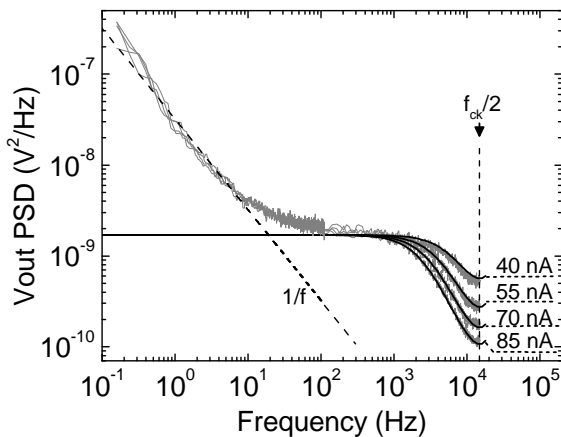
Fig.14. Noise power spectral density of the voltage V_{PW}, measured for different ΔI_B values. Solid lines represent the behavior predicted by (33). The dashed line represents a fit of the 1/f noise in the interval 0.15-7 Hz. The spectra have been obtained joining measurements performed over two different frequency interval.

The integral effect of noise is represented by standard deviation of the output pulse duration. This parameter has been estimated from 50 independent captures of the output pulse, taken using the digital oscilloscope. The test was performed with ΔI_B set to 40 nA and 85 nA, obtaining the results shown in Table V. The measured standard deviations, normalized to the full scale, are compared to the predictions made using (36) with the values of parameter a reported in the table.

TABLE V
MEASURED JITTER COMPARED TO PREDICTED VALUES

ΔI_B	a	σ_τ	σ_τ/τ_{FS}	σ_τ/τ_{FS} (predicted)	BW
40 nA	1.3	46 ns	0.63 %	0.48 %	7 kHz
85 nA	2.5	28 ns	0.38 %	0.31 %	2.6 kHz

The slight underestimation of the jitter is compatible with the mentioned discrepancy between the measured and predicted power spectra. These data indicate that equations (36) and (37) provide sufficient accuracy for estimating the circuit performances and guiding device sizing during the design phase. The dynamic range resulting from the data of

Table V varies from 44 to 48 dB. Note that these data have been calculated for a sampling rate equal to the clock frequency (30 kHz). In this case, the interface bandwidth (BW) is determined by the $H(j\omega)$ frequency response. The resulting BW values are reported in Table V. The actual contribution of the flicker noise can be found by integrating the corresponding PSD (estimated from the spectra of Fig.14) over the given BW. Considering a lower frequency limit of 0.1 Hz, the flicker noise contribution to the total jitter mean square value is less than 8% in all considered cases. Conversely, the presence of flicker noise should be taken into account if a further BW limitation is applied, for example by averaging successive samples in order to reduce noise.

The total power consumption of the interface (diagnostic buffers excluded) was 84 μW, corresponding to a 28 μA supply current, of which 12 μA are used by the two comparators, 6 μA by the current amplifier, 4 μA by the ramp generator. The remaining 8 μA are due to the current source and to circuits used to produce reference voltages and bias currents. Table VI compares the main circuit performance parameter with those of other state-of-art capacitance to time converters present in the literature. Sensitivity to parasitic capacitances for the proposed interface was estimated from simulations performed with a capacitor connected between one sensor terminal (node 1 or 2 in Fig.1) and ground. Due to stability requirements, the maximum parasitic capacitance value was 9 pF.

V. CONCLUSIONS

An original approach for converting small capacitance differences into pulse width has been described. The circuit exploits chopper modulation to reduce the effect of low frequency noise and mitigate the performance spread due to device mismatch. The ideal transfer function of the interface is expressed by equation (6), which includes only terms that can be easily made precise and temperature independent. Parasitic capacitances between sensor terminals and ground are rejected by the low impedance of the current amplifier. The main non-idealities affecting the actual performance of the circuit,

TABLE VI.
PERFORMANCE SUMMARY AND COMPARISON WITH RECENT WORKS

Reference	[23]	[27]	[28]	[26]	This work
Type (diff/unip)	unipolar	unipolar	unipolar	differential	differential
Sensitivity	1.82μs/pf	47 μs/pf	3.88 μs/pf	N/A	32 μs/pf
Resolution	13 aF	900 aF	2.8 fF	200 aF	800 aF
full scale cap. variation	9pF [a]	400fF	325fF	6.8pF	256fF
Power @ Vdd	60μW @ 1.0V	16.5mW @ 3.3V	54μW @ 3V	211μW @ 3.3V	84μW @ 3V
Sens/to/temp (total)	N/A [b]	300ppm/°C	N/A	low (N/A)	300 ppm/°C
Technology	CMOS 0.18 μm	CMOS 0.35 μm	CMOS 0.35 μm	CMOS 0.35 μm	CMOS 0.32 μm
Area	0.01 mm^2	0.2 mm^2	0.09 mm^2	0.51 mm^2	0.52 mm^2
Sensitivity to parasitic capacitances[c].	High (1.0)	Low (2×10^{-3})	High (1.0)	Low (N/A)	Low (3.7×10^{-4}) [d]
BW	16 kHz	10 kHz	25 kHz	65 Hz	2.6kHz

[a] Different full scales may be chosen changing an external resistor. [b] Proportional to the TCR of a reference resistor. [c] Normalized to the sensitivity to the input capacitance. [d] Simulated

namely the finite input impedance of the current amplifier and noise (i.e. jitter) have been thoroughly analyzed, obtaining important design indication.

In particular, (36) suggests that the relative jitter (inverse of the dynamic range) can be reduced by either increasing the clock frequency or reducing the bias current of the current amplifier. Unfortunately, the ratio between these two parameters is fixed by (13), once the ratio between the sensor impedance and amplifier input impedance (α_z) is decided. Following these design criteria the optimum relative jitter is given by the very general expression (37), where both f_{ck} and I_{bias} do not appear. In (37) the relative jitter is mainly affected by sensor characteristics (C_{XM}, ΔC_{FS}) and by the amplitude of the triangular waveform V_S.

Compared to other solutions, such as that described in [23], this is clearly a limitation since there are fewer possibilities to obtain large dynamic ranges. On the other hand, differently from other solutions, the bias current can be widely reduced without affecting the system performances, provided that the clock frequency is reduced of the same proportion. Another interesting aspect is the described intrinsic low pass property of the circuit that can be exploited to further reduce the total jitter.

Most of these features have been confirmed by the measurement performed on the prototype. The low temperature sensitivity is confirmed over a wide temperature range, while the measured sensitivity, noise spectral density and dynamic range are in good agreement with the prediction made on the basis of the mentioned design formulas. The only unexpected discrepancy was the presence of a systematic offset, which was attributed to charge injection due to parasitic capacitances among the internal interconnections of the dummy capacitor.

Comparison with other state-of-art capacitance-to-time converters shows that the strength of the proposed circuit is the combination of low power characteristics, low sensitivity to temperature, capability of handling differential sensors and low sensitivity to parasitic capacitances. Similar characteristics are offered only by [26], which, on the other hand, does not produce a real PWM output but require further processing to extract the information. The interface described in [23] presents comparable power consumption and considerably better resolution. Conversely, [23] requires a reference resistor, which may be a source of large temperature sensitivity unless a stable off-chip component is used. A minimal-change evolution of the proposed circuit, aimed at improving the noise and power consumption performances, has been recently invented and its effectiveness has been preliminary assessed by means of electrical simulations [31].

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