1 # Review

2 ## Inorganic Photovoltaics - Planar and Nanostructured Devices

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Abstract

Since its invention in the 1950s, semiconductor solar cell technology has evolved in great leaps and bounds. Solar power is now being considered as a serious leading contender for replacing fossil fuel based power generation. This article reviews the evolution and current state, and potential areas of near future research focus, of leading inorganic materials based solar cells, including bulk crystalline, amorphous thin-films, and nanomaterials based solar cells. Bulk crystalline silicon solar cells continue to dominate the solar power market, and continued efforts at device fabrication improvements, and device topology advancements are discussed. III-V compound semiconductor materials on c-Si for solar power generation are also reviewed. Developments in thin-film based solar cells are reviewed, with a focus on amorphous silicon, copper zinc tin sulfide, cadmium telluride, as well as nanostructured Cadmium telluride. Recent developments in the use of nano-materials for solar power generation, including silicon and gallium arsenide nanowires, are also reviewed.

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205 # 1.0 Introduction

206 The increase in energy demand, decline in conventional energy resources, and carbon
207 dioxide (CO_2) emission from fossil fuel sources has prompted research in photovoltaics (PV).
208 With current total global power needs of 15TW, and with a projection of 30TW by the year
209 2050 [1], renewable energy is expected to play a critical role in meeting those needs. Among
210 the renewable energy sources, the PV installation for energy harvesting was about 38.7GW in
211 2014, and in 2015, the demand rose to about 42.8GW [2]. Nevertheless, despite the
212 tremendous continuing economic effort on PV research, the total contribution coming from
213 the PV sector is only about 0.9% [3] of the total global electric energy consumption. In the
214 first quarter of 2015, the average price for solar cells, modules, and installed utility systems
215 were $0.31/watt, $0.72/watt, and $1.58/watt respectively [4]. Considering the current global
216 energy concerns (i.e. insufficient fossil energy supply due to high demand) together with the
217 problems related to excessive CO_2 gas emission, the huge interest in investing in the PV
218 sector is obvious. At the same time, if only about 0.1% of the Earth surface were covered
219 with PV modules with an average efficiency of 10%, this could fulfill the total energy needs
220 of humanity [5], which provides further impetus to research and development in the PV field.
221 As a side note, in every second, the sun produces $3x10^{26}$ W (or J/Sec) [6] of power, in other
222 words, in every second the sun produces ~500,000 years of our current energy requirements
223 [7].

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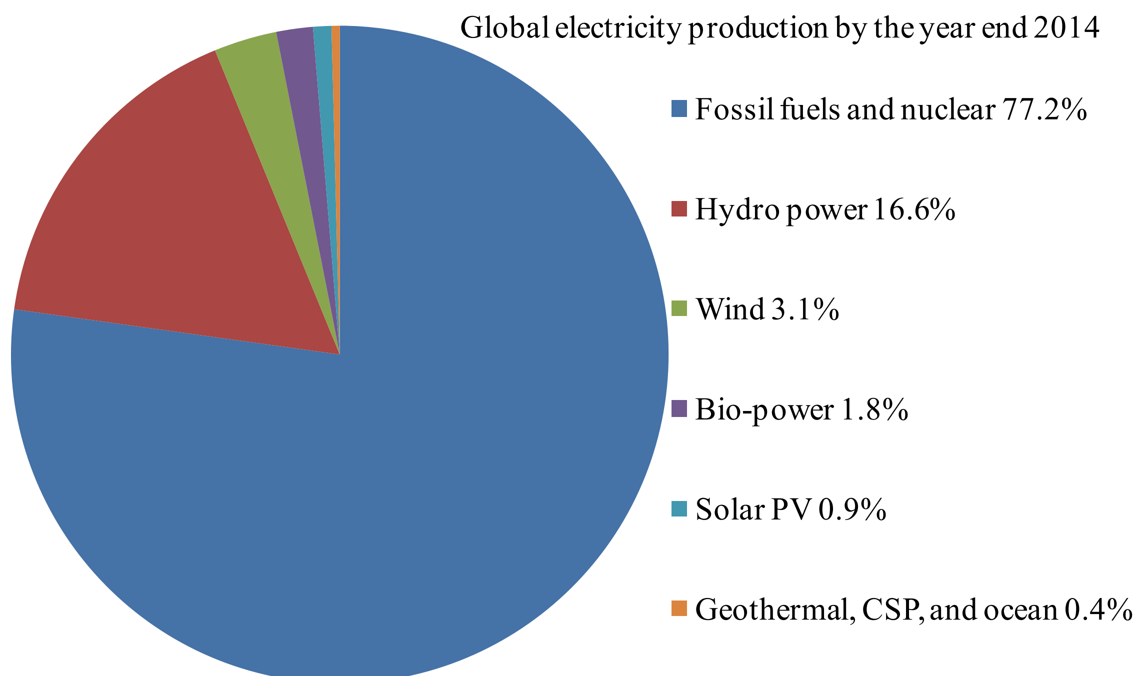

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227 Fig. 1 Percentage of global electricity production in 2014. Renewable energy accounts for 22.8%. Note that the
228 contribution from PV is only 0.9%. CSP stands for concentrating solar power. For high-efficiency solar cells,
229 <100> wafers are widely used in industry since easy texturing can be achieved by anisotropic etching.
230 Texturization of <100> c-Si results upright pyramids with <111> orientation that leads to higher surface
231 recombination rate due to an increased surface area in <111> orientation. Nevertheless, the decrease in optical
232 losses substantially compensates small reduction in voltage from solar cell. Fig.1 data from [3].

233

234 Various methods have been developed to harvest energy from the sun that involve
235 capturing and conversion, e.g. solar cells which absorb sun light and convert it into
236 electricity, solar thermal collectors which absorb and convert energy from the sun into usable
237 heat, and wind turbines (wind is an example of solar energy since it is created when the sun
238 heats the Earth) etc. Worldwide electrical energy production is shown in Fig. 1 [3]. Replacing
239 1kW of electrical energy from fossil fuel sources by PV cells would mitigate CO_2 production
240 [8] by 1 tonne/year. Fossil sources (oil, natural gas, coal) produce CO_2 an average of 260-
241 330g/kWh [9] and 48g/kWh [10] of CO_2 equivalent for PV. The latter is the average of CO_2
242 equivalent for various technologies such as crystalline silicon (c-Si), multicrystalline silicon
243 (mc-Si), amorphous silicon (a-Si:H), copper indium gallium selenide (CIGS), and cadmium
244 telluride (CdTe).

245 Among various PV technologies, conventional c-Si p-n junction solar cells currently
246 play a dominant role. These solar cells have improved over the decades and are expected to
247 play a prominent part in solar power generation for the foreseeable future. However, the
248 cost-per-watt peak ($/W_p$, the term "peak" refers to peak sun hours – global average of about
249 5 hrs/day) of c-Si solar cells are still relatively high. High-efficiency and reduced production
250 costs are crutial factors to achieve grid parity (cost of PV generated electricity on par with
251 grid electricity known as grid parity). There are two approaches for low-cost (i.e. low $/Wp)
252 c-Si solar cells: (i) lower the cost using cheaper consumables such as spin-on sources for
253 doping [11,12], low cost metallization schemes, thinner wafers and lower quality Si feedstock
254 etc., and (ii) increase the cell efficiency by using selective emitters, local back surface fields
255 etc., in front junction cells, or by using an interdigitated back contact structure in back
256 junction cells. In the back contact structure, the p-n junction lies at the rear side of the c-Si
257 wafer, and no contact grids are present at the front side. Therefore, the losses due to
258 shadowing are eliminated, which results in an increase in short circuit current and efficiency.
259 For c-Si based front junction and back junction solar cells, the metal/c-Si interface regions
260 are sites of high electron hole (e-h) recombination rates, and this affects efficiency. In the
261 case of front (a-Si/c-Si) heterojunction, and back (a-Si/c-Si) heterojunction (BHJ) cells, the
262 metal/a-Si interface is electronically separated from the c-Si bulk by inserting an intrinsic a-
263 Si:H layer, which also acts as a passivation layer to c-Si. A BHJ solar cell is a combination of
264 front heterojunction and back junction cells. In the BHJ design [13,14], shadowing loss can
265 be avoided completely due to a grid-less front side; an interdigitated pattern of p- and n-type
266 contacts collects the photogenerated current on the rear. In thin-film solar cells, fabrication of
267 a-Si:H cell is relatively simple with low fabrication cost [15]. However it also comes with
268 lower performance. Efficiency of thin-film heterojunction solar cells such as CIGS, copper-
269 zinc-tin-sulfide (CZTS) and CdTe based cells lie in between c-Si based cells and a-Si:H cells.

270 Nanowire (NW) solar cells such as Si nanowire (SiNW) [16] and gallium arsenide (GaAs)
271 have recently caught research attention. While optical absorption may be low in individual
272 NWs, the use of mats or forests of NWs in a solar cell potentially may overcome that issue.
273 Optical absorption is also potentially increased through light-trapping in those forests. NWs
274 may be used in different ways in a solar cell, which provides greater options for design. They
275 also lend themselves to flexible solar cells, an important current research focus.

276 In this article, we review inorganic wafer based solar cells that include c-Si based
277 solar cells- front junction, back junction, front heterojunction, and back heterojunction. We
278 also review multi-junction (III-V or perovskite on c-Si) solar cells, and thin-film solar cells,
279 viz. a-Si:H, CZTS, and CdTe based solar cells. Apart from planar devices, cadmium sulphide
280 (CdS)/CdTe, SiNW, and GaAs nanostructured solar cells are reviewed. We present current
281 developments in R&D, existing problems that need further research, and identify some points
282 where research is stagnant. We provide explanations to the problems associated with different
283 solar cells. Limiting factors for efficiency and how to improve efficiency are discussed.
284 Current challenges and possible strategies to overcome those challenges are mentioned.

285 2.0 c-Si based solar cells: Front junction

286 In this section, fabrication of conventional aluminum (Al) back surface field (Al-BSF)
287 solar cell is reviewed in detail. Other types of solar cells, such as passivated emitter rear
288 contact (PERC), passivated emitter rear locally-diffused (PERL), metal wrap-through
289 (MWT), and emitter wrap-through (EWT) cells are also discussed. Low-cost approaches for
290 producing cheap wafers, doping and metallization are outlined.

291 2.1 Historical approach: Evolution of the c-Si solar cells to present

292 The photovoltaic effect was first observed in 1839, when Becquerel [17] produced a
293 current intensity by exposing silver (Ag) electrodes to radiation in an electrolyte. Later, in
294 1877, Adams and Day observed that the exposure of selenium (Se) electrodes to radiation

295 produced electric voltage and current [18]. However, no significant research was reported on
296 the photovoltaic effect until 1949 when Shockley [19], Bardeen, and Brattain [20] reported
297 their work on the transistors and the physics of the p-n junction. The history of the modern
298 PV started at the Bell Labs in USA in 1954 when researchers, realized that p-n junction
299 diodes produced voltage under illumination. One year after this discovery, Bell Labs
300 produced a c-Si p-n junction solar cell with 6% efficiency [21]. In 1960, several authors
301 developed the fundamentals of the p-n junction solar cell and the relations between bandgap
302 (hereafter E_g or bandgap), incident sunlight dependence, the influence of temperature,
303 thermodynamics of the solar cells, efficiency limits, etc. In 1961, Shockley and Queisser [22]
304 reported the maximum theoretical efficiency of 29% (known as Shockley and Queisser limit
305 or S-Q limit) using a p-n junction solar cell, establishing the basis to understand the
306 performance of the solar cells and the losses mechanisms.

307 The first world oil embargo was instituted on 1973 by the Persian Gulf oil producers.
308 This incident produced a strong impulse for PV as many governments from industrialized
309 countries began programs to develop renewable energy and to reduce the oil dependence.
310 Consequently, the terrestrial application of photovoltaics was reinforced. During the 1980's,
311 the industry started producing Si PV modules, focusing in scaling up the fabrication systems,
312 the manufacturing processes, and reinforcing the cost analysis [23].

313 In 1985 the first high-efficiency c-Si solar cell under standard measurement
314 conditions was reported by University of New South Wales, Australia [24]. In the 1990's, the
315 use of solar cells for commercial purposes was extended. In 1995, a German project
316 demonstrated the use of PV installation on roofs, favoring PV legislation in Germany, Japan
317 and several countries encouraging the introduction of PV systems at homes. In 1997,
318 worldwide PV production reached 100MW, and in 1999 the cumulative worldwide installed
319 photovoltaic reached 1000MW. The annual production in 2014 has increased to 45GW

320 (reported production vary between 39 and 49GW_p), and the accumulated power installed
321 around the world has reached 183GW_p at the end of 2014 [25].

322 As shown in Fig. 2, the solar cell market is led by standard crystalline technology,
323 using single-junction solar cells, with 92% of the total market. Other technologies such as
324 CdTe, CI(G)S, and a-Si:H thin-films etc., make up the rest [26].

325 Single-junction c-Si solar cells present several advantages [27]. Si is an abundant non-
326 toxic material, composing about a 25% of the Earth's crust, and c-Si based photovoltaic
327 modules are long-term stable outdoors, with a lifetime longer than 20 years. The current
328 technology has relatively high energy conversion efficiency in comparison with many other
329 technologies and lower system costs. This enables installation of high-power systems. As we
330 will also discuss, single-junction technology still has a considerable potential for further cost
331 reductions.

332 On the other hand, the disadvantages of this technology include a limitation to
333 substantially increase the efficiency of the solar cells, as it is already close to its technical
334 limit. Moreover, at the present, fabrication of solar cells requires high-temperature and
335 energy. A large amount of Si is required for the wafer, and the wafering process (accounts
336 for 22% of the entire production cost of c-Si cell) [28] itself wastes approximately the 50% of
337 the Si ingot. The wafers are also very fragile. At a broader level, the c-Si solar cell
338 technology currently requires the support of three different factory equipments for wafer, cell,
339 and module production, and several times its integration in a single factory is not easy, which
340 in turn can affect the overall business if competitive prices are required.

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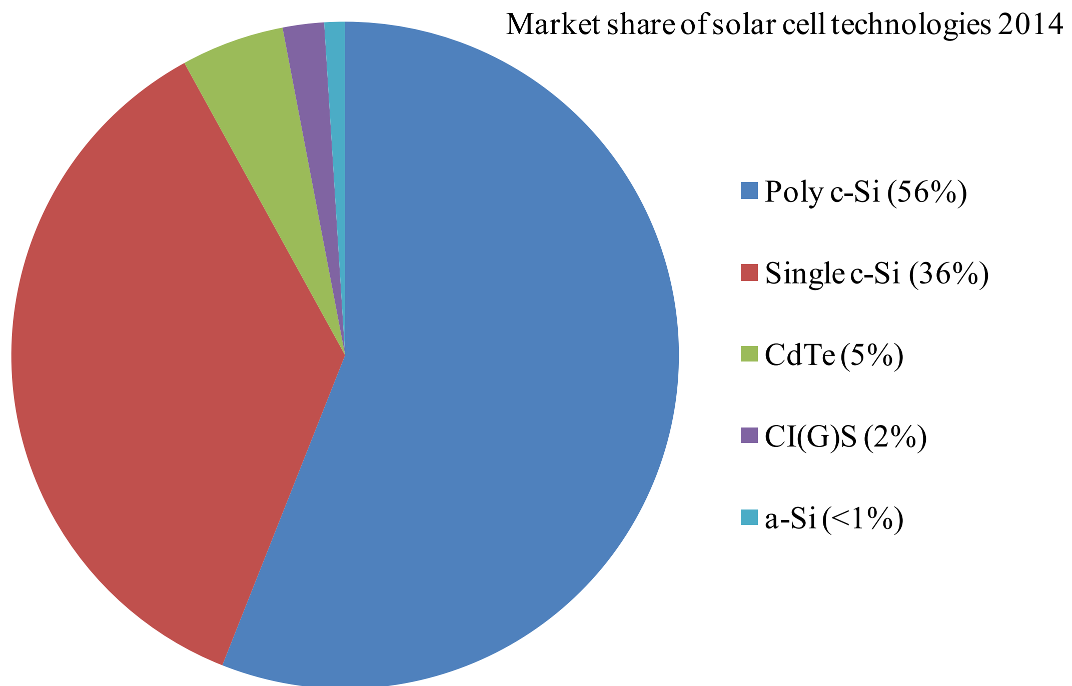

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343 Fig. 2 Market share of different solar cell materials in 2014 showing the dominance of c-Si (92%) followed by
344 CdTe [26]. In the case of a-Si:H solar cells, the main issue with a-Si:H, light induced degradation, has not been
345 solved so far. For CdTe solar cells, cadmium is abundant and tellurium is not abundant. CdTe is less toxic than
346 cadmium and disposal of CdTe solar panel is an issue in the large-scale commercialization since CdTe modules
347 pollute during decommissioning. CdTe disposal is a major concern in developing countries. As a side note, in
348 the middle and late 1980s, the use of indium tin oxide in LCD products has increased indium demand and price
349 rose to several hundred dollars per kilogram. Similarly, the demand for indium may increase with large
350 production of CIGS based solar cells, and may results in unstable price in CIGS module.

351

352 Considering the Carnot limit for a solar cell and due to the temperature of the Sun, the
353 thermodynamic efficiency limit is about 86%. However, this limit is only calculated in terms
354 of the working temperature of the system. As mentioned above, in 1961 the first study on the
355 efficiency limit of a solar cell was calculated [22] using a detailed balance. In that work the
356 electron generation due to the absorbed photons and radiative recombination was analyzed.
357 This efficiency limit was calculated for solar cells based on a semiconductor with a valence
358 and a conduction band separated by bandgap. This study has several assumptions: (i) there is
359 only one semiconductor material per solar cell, (ii) there is only one p-n junction per solar
360 cell, and (iii) the sunlight is not concentrated and all the energy is converted to heat from
361 photons with energy larger than the bandgap. The result of this calculation indicates that there
362 is a maximum efficiency of 33% for any type of single-junction solar cell. The limitation in

363 the efficiency is due to the 47% of the solar energy directly converted to heat, 18% not
364 absorbed by the solar cells and 2% lost in local recombination. However, according to S-Q
365 limit, a maximum efficiency of 29% can be obtained [22, 29, 30].

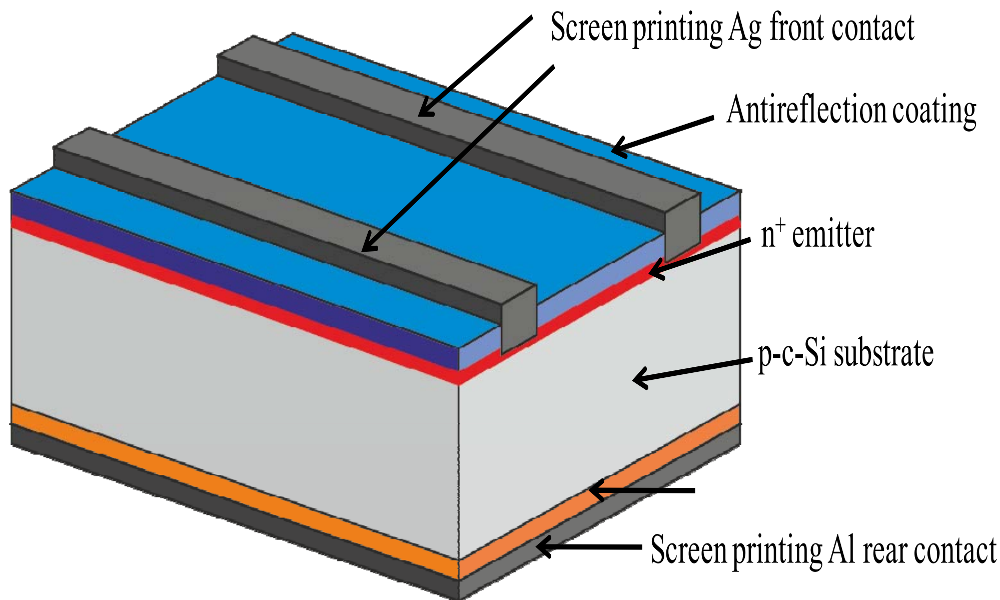
366 The evolution of the single-junction solar cells technology has been extensively
367 discussed [31]. Since the early 1950s there have been important milestones in the field. In
368 Bell Lab the first cells were fabricated on p-type c-Si and they showed efficiencies of around
369 4.5%. Using arsenic-doped n-type c-Si with a boron-doped emitter [21], the efficiency
370 reached values above 6%. In the early 1960s, due to requirements of solar cells for space
371 flights, p-type c-Si with a phosphorus-doped emitter was developed [32]. The second
372 important improvement occurred at the beginning of the 1980s, when the PERC solar cell
373 was produced. This reached 20% efficiency in 1985 [33]. Currently, the efficiency record for
374 p-n junction c-Si is ~25%, which was reached in 1998. For mc-Si the efficiency is 21.25%
375 (area 156x156 mm^2) which was reached in 2015 [34]. There has been no change in the
376 maximum efficiency for c-Si and mc-Si solar cells, from 1998 and 2004 respectively.
377 However, in the industrial production line, some steps as new texturization methods (to
378 increase photons absorption), local BSF, and selective emitter have been included by the
379 most important production lines manufacturers to increase the average commercial efficiency
380 to 19% for c-Si and 18% for mc-Si. One of the challenges of the industry and also one of the
381 reasons to review this section is to describe how these advances have been transferred from
382 laboratory to production scale, allowing at the same time high-throughput and high-efficiency
383 in the solar cells. Current challenges for this technology are the implementation of new
384 concepts to target and reduce the loss mechanisms.

385 Recombination losses can be reduced using new passivation layers and chemical
386 processes. However, from the point of view of the industry, most of these techniques are not
387 cost-effective due to the requirement of high vacuum and energy. Also the process times are

388 not affordable to accomplish a competitive industry production. On the other hand, light not
389 absorbed can be reduced using multiple anti-reflection coatings (ARCs), or including other
390 absorber materials. Both strategies have not been integrated in the industrial production lines
391 due to their high cost. In our opinion, these strategies should be subject of increased study in
392 the future.

393 2.2 Conventional c-Si based solar cells

394 To understand the single-junction solar cell fabrication steps, it is necessary to first
395 understand the device structure. A schematic diagram of a simple p-n junction p^+-p-n^+ type
396 solar cell is shown in Fig. 3. At the rear side, a heavily Al-doped p^+-region (Al-Si alloy) in p-
397 type c-Si forms a high-low (p^+/p) junction known as Al-BSF. The thickness of the Al-BSF
398 region is around 0.2 μm. The phosphorous diffused emitter thickness is around 0.8 μm.
399 Detailed fabrication steps are mentioned in Sec. 2.3.



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401 Fig. 3 Schematic diagram of p^+-p-n^+ type solar cell having Al-BSF [27]. Solar cell works as follows: Incident
402 light generates electron-hole pairs in the p-type c-Si absorber. Due to built-in electric field across the p-n
403 junction, electrons travel towards the n-type electrode and are in turn collected by the grid electrodes. Holes, on
404 the other hand, travel across bulk c-Si and are collected by the Al back electrode. The potential barrier at the
405 high-low (p^+/p) junction provides an additional mechanism to drive electrons away from reaching the back
406 electrode and towards the p-n junction. This increases V_{oc} and J_{sc} due to reduced back surface recombination
407 [11].

408

409 The wafer size used commercially has been increasing over the years. For a
410 considerable length of time, the Czochralski Si (Cz-Si) wafer diameter was 4” as it was the
411 standard size in the microelectronic industry and the Si wafers came mainly from stocks
412 offering quality standards just under those accepted by the microelectronic industry. Then,
413 due to the microelectronic industry requirement, and subsequently to the photovoltaic
414 industry requirement, the wafers have passed from 10x10cm^2 (4”x4”) to the current standard
415 15.6x15.6cm^2 (6”x6”). The wafer also has evolved from circular to pseudo-square and to
416 square shape to maximize the solar module active area. A pseudo-square wafer comes from a
417 circular wafer where the inner square is obtained showing the typical 45º cut corners.

418 In the case of mc-Si, the manufacturers have been offering square surfaces since the
419 beginning because of the fabrication procedure. The thickness of the wafer has been reduced
420 over the last decades to save Si, as it is the main component of the Si solar cell cost. Thus,
421 from 500μm at the beginning of the 1990s, currently the wafer thickness is around 180-220
422 μm [35]. There has been considerable research activity in relation to further reductions of
423 wafer thickness to save Si, and to obtain flexible properties for the wafer. However a
424 reduction in the wafer thickness may also result in reduction of the efficiency and yield of the
425 final solar cell unless appropriate light trapping and surface passivation solutions are
426 implemented.

427 The base doping level of the wafer is around 10^{16} atoms/cm^3, which correspond with a
428 resistivity of 1 Ω-cm. This doping level is related to the optimum recombination properties of
429 the wafer to improve the cell efficiency.

430 Currently, the c-Si PV market is dominated by p-type Si wafers. However p-type
431 wafers are sensitive to chemical impurities that can be activated in high-temperature
432 processes, resulting in efficiency loss. P-type c-Si solar cells possess degradation of minority-
433 carrier lifetimes induced by illumination or carrier injection [27]. This lifetime degradation is

434 stabilized after one day, which concomitantly also produces a degradation of the solar cell
435 efficiency. In some cases, depending of the wafer quality, this degradation can reach 1% of
436 the total efficiency. This effect is clearly related to the presence of boron and oxygen. N-type
437 c-Si solar cells are an alternative to avoid the carrier-induced degradation of p-type c-Si, as
438 the former do not present this effect, even when high concentrations of oxygen are detected in
439 the Si wafer. This difference is related with the ratio of electron to hole capture cross sections
440 of the corresponding defects, which is greater than unity. Therefore, n-type c-Si wafers have
441 higher minority-carrier lifetime and hence higher minority-carrier diffusion length for the
442 same concentration of impurities present in bulk Si.

443 A passivation layer on the crystal surface is used to reduce surface defects. In addition
444 the front side of the wafer is normally textured in order to improve the absorption of the
445 incident radiation. Also the front surface is doped with phosphorus to form the p-n junction.
446 The phosphorous surface concentration is around $2x10^{20}$ atoms/cm^3, with a sheet resistivity
447 (R_{sh}) between 50 and 75Ω/sq. The front side is a $\lambda/4$ (where λ is wavelength of light) coated
448 thin layer of amorphous hydrogenated SiN for an effective reduction of front reflection.
449 Finally the metallic contacts are placed by the screen printing technique: Ag is placed in the
450 front side, with a finger and busbar structure to allow solar incident radiation to the emitter,
451 and fully covered by an Al back side contact. The paste used must be dried and fired to
452 produce a proper Ohmic contact [36]. The solar cells are edge isolated (Fig. 4) in order to
453 avoid contact between front and the back side during the fabrication process.

454 In the standard cell process, the metal impurities can be reduced and even totally
455 deactivated when the wafers are submitted to the diffusion process, due to gettering effects
456 (explained in Sec. 2.3.3.). Below we review briefly on raw materials and wafer production
457 technology.

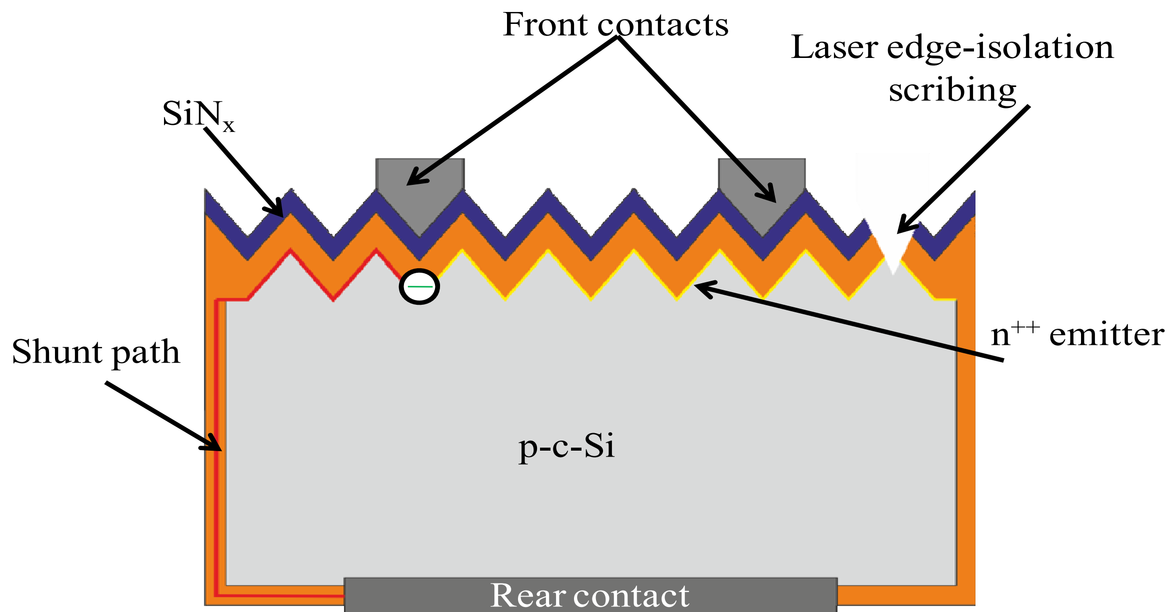
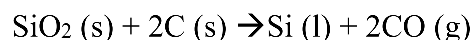


Fig. 4 Solar cells are edge isolated on both sides to avoid shunting between top and bottom contacts [37]. Edge isolation is performed by plasma etching, laser or laser scribing or chemical etching. In plasma etching, solar cells are coin stacked and then edges are etched away using plasma. If edge isolation is not performed, phosphorous diffusion on the edges provide short circuit to electrons and reach back electrode. For efficient solar cell operation, very high shunt resistance is required.

2.2.1 Raw materials

There are several processes involved in reaching the desired purity of c-Si for solar applications. To obtain solar grade Si, it is necessary to produce metallurgical grade Si (mg-Si) with a minimum of 98.5% Si content [23]. Mg-Si is produced by the introduction of the raw material in electric arc furnaces with quartz and carbon materials. The following reaction occurs:



$$SiO_2\ (s) + 2C\ (s) \rightarrow Si\ (l) + 2CO\ (g)$$

where SiO_2, C, CO are silicon dioxide, carbon and carbon monoxide respectively.

To carry out above reaction, lumpy quartz with appropriate purity and thermal resistance is required. The refined liquid Si is decanted from the ladle into a cast iron mold or onto a bed of Si fines. The casting should be removed from the mold while it is still not fully solidified. In this step, the mg-Si becomes mc-Si. This is smashed to obtain pieces of around 10cm. There are several processes [23] to produce electronic grade Si of highest purity

478 (99.9999999% or 9N purity). The most frequently used process is based on the
479 decomposition of trichlorosilane (TCS) with temperatures around 1100°C on a heated Si
480 filament placed in a deposition chamber. This process is called Siemens process [38].

481 2.2.2 Wafer technology description: Cz, Fz, and mc-Si

482 When the literature refers to crystalline Si, one (or more) of three different materials is
483 implied: the Cz-grown c-Si, float-zone (Fz c-Si), and mc-Si. C-Si ingots are formed by Cz
484 process, based on the melting of electronic grade Si and using a rotating Si seed. The ingot is
485 formed when the seed is pulled out of the crucible [23]. The cooling down process is critical
486 to obtaining high quality Si ingot. The rotation velocity can be adjusted to obtain different
487 sizes.

488 The floating zone process is performed on polysilicon rod to convert polysilicon into
489 single crystal Si ingot. In this process, seed crystal plays an important role. By heating one
490 end of the rod, seed crystal is fused and then seeded molten zone is passed through the length
491 polysilicon rod to convert it into single crystal Si ingot.

492 Directional solidification is the conventional method for producing mc-Si ingots. Si
493 seed crystal is not used to produce mc-Si ingots. In this method, Si scrap is used as the
494 starting material. After melting the starting material, molten Si is poured into a square shaped
495 crucible. By cooling, directional solidification takes place and large crystals grow in a
496 random direction. The mc-Si technology presents several advantages with respect to the Cz-
497 Si technology: (i) the fabrication procedure is easier, (ii) lower manufacturing costs, and (iii)
498 higher feedstock tolerance. Also, the mc-Si wafers are rectangular or square yielding a larger
499 utilization of the module area in comparison with round or pseudosquare Cz-Si or Fz-Si
500 wafers. However, as compared to Cz-Si and Fz-Si, mc-Si has much higher defect content,
501 which reduces the expected efficiency of the solar cells. Consequently, as the spot price of c-

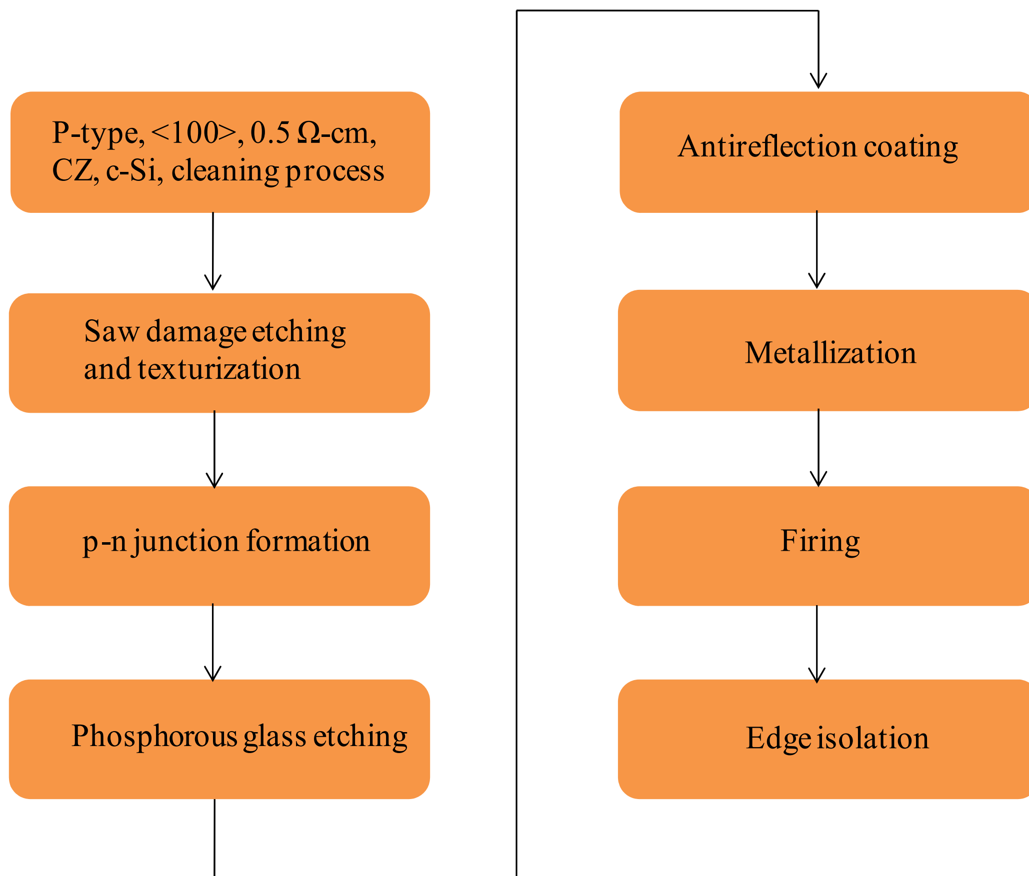
502 Si and mc-Si varies in the market and different wafer qualities can be purchased, it is not easy

503 to define the best wafer option for producing Si-based solar cells.

504 2.3. Fabrication of Al-BSF c-Si solar cell

505 The Al-BSF solar cells concept includes several physical structures with slight differences. In

506 the following flow chart (Fig. 5), the main steps are depicted.



507

508 Fig. 5 Processing steps for front junction c-Si solar cell. Since electron mobility is about three times higher than
509 the hole mobility, conventional solar cells are fabricated on p-type c-Si wafers for easy minority (electrons)
510 carrier collection. Also, it is easy to obtain high-quality phosphorous diffusion than boron diffusion. However,
511 boron-oxygen complex formation in Cz p-type c-Si reduces minority-carrier lifetime. In production, Fz c-Si
512 wafers are used due to less oxygen content in Si wafer. An ideal resistivity and thickness of c-Si are 0.5Ω-cm
513 and 180-200μm. For larger resistivity values, Al/p-Si interface becomes rectifying contact (Schottky barrier)
514 and reduces V_{oc} and fill factor due to narrow depletion width of schottky junction [39]. Energy payback time
515 [40] for c-Si solar cell is ~2 years.

516

517 Passivation of the front side is very important to obtain high-efficiency. To reduce

518 surface recombination velocity (SRV) at the rear side, it is necessary to carry out passivation

519 using a p^+-layer, otherwise the solar efficiency will decrease dramatically. The easiest

520 procedure to obtain the p^+-layer in the rear side is using boron doped Al paste to avoid high
521 recombination velocities in the rear side of the solar cell. This process is called Al-BSF [27].

522 2.3.1 Cleaning process

523 Cleaning process and the environmental control is critical to avoid contamination and
524 to allow high-efficiency. Several cleaning processes have been commonly used in R&D,
525 depending on the purpose. Radio Corporation of America (RCA) cleaning procedure [41] is
526 the standard process for removing contaminants from Si wafers. It consists of two steps:
527 (i) RCA 1 is used for organic cleaning. Organic contaminants are dissolved by immersing c-
528 Si wafer in a solution containing de-ionized (DI) water having resistivity of about 19MΩ.cm,
529 ammonium hydroxide (NH_4OH) and hydrogen peroxide (H_2O_2) in the ratio of 5:1:1. NH_4OH
530 is added to DI water and finally H_2O_2 is added. To remove organic residues, the wafer is
531 treated in the bath at 80°C for 15 min. This process oxidizes Si and leaves a thin oxide on the
532 Si surface that can be removed if pure Si surface is required.
533 (ii) RCA 2 is used to remove metal ions from c-Si wafer. The solution contains DI water,
534 hydrochloric acid (HCl) and H_2O_2 in the ratio of 5:1:1. HCl is added to DI water and then
535 finally H_2O_2 is added. This clean is performed around 90°C for 15 min.
536 Note that, to our best of knowledge, RCA cleaning process is not used in industry to
537 reduce production cost and to avoid the need of recycling chemicals. Before saw damage
538 removal, soap solutions are used to clean wafers.

539 2.3.2 Saw damage etching/texturing processes

540 The sawing process generates a high degree of damage on the “as-cut” surfaces,
541 producing a low quality surface with a large amount of defects on it [42]. These defects can
542 produce fracture during the solar cells processing and lower the performance of the solar cells
543 [43]. Thus, one of the necessary steps to obtain high-efficiency Si solar cell is to introduce

544 saw damage etching of the wafer at the beginning of the fabrication process, and it is carried
545 out by immersion of the wafer in a chemical solution [27].

546 Optical losses of the solar cells can be improved by means of a texturing process on
547 the front surface of the Si wafer [36]. The aim of the texturing process is to produce a specific
548 morphology on the Si surface able to redirect reflected light into the device to improve the
549 light absorption, i.e., diminish the reflection losses from the front surface. To carry out
550 texturing, several methods are available, such as mechanical grooving [43,44], reactive ion
551 etching (RIE), anisotropic alkaline etching [43], acidic etching [45], chemical etching using a
552 metallic catalyst [46], dry etching processes as plasma texturing [47], and laser texturization
553 [48]. Among these methods, wet chemical etching is the mostly used in industrial process and
554 commercially it is also the most commonly used procedure for c-Si solar cells. This is
555 because of its low-cost, high etching rate, and large-area uniformity [49]. Saw damage
556 etching and the texturization process can be carried out in the same step when chemical
557 solutions are used.

558 For c-Si, pyramid formation is due to anisotropic etching resulting from the difference
559 in etching rates for the <100>, <111> planes of c-Si. The pyramids size and height are highly
560 depending on the etchant and the etching parameters [43]. Mixed alkaline solutions, such as a
561 sodium hydroxide (NaOH) or a potassium hydroxide (KOH) solution, with isopropyl alcohol
562 (IPA) are used to texture the monocrystalline Si surface. However, IPA cost limits the use of
563 these solutions. For chemical anisotropic etching, the solutions without IPA have been
564 acquiring more relevance during recent years [50, 51]. Cheaper alternative solvents are
565 sodium carbonate (Na_2CO_3) [52], potassium carbonate (K_2CO_3) [53] and sodium phosphate
566 (Na_3PO_4) [54].

567 Recently a mixture of Na_2CO_3 and sodium bicarbonate ($NaHCO_3$) has been
568 optimized. This has significantly reduced the amount of the solvents and their costs [43], and

569 has proved to be the most promising to be used in c-Si texturing processes. Another chemical
570 used to perform wet chemical etching is tetramethyl ammonium hydroxide (TMAOH). It is
571 also a cost-effective procedure and does not produce metal contaminations on the wafers
572 [51].

573 As mc-Si is composed of several Si crystals or grains with different orientations,
574 anisotropic etching cannot be applied efficiently for random pyramid texturization. For this
575 reason, isotropic etching in acidic solutions is the most cost-effective procedure to texture
576 mc-Si wafers. Acidic texturing is normally based on solutions containing hydrofluoric acid
577 (HF) and nitric acid (HNO_3) in acetic acid (CH_3COOH) or DI water [55, 56]. Also vapor
578 etching using these solutions [57] has been applied because of a resultant enhanced etching
579 rate control. Other alternatives to control the etching rate, such as NaOH/sodium hypochlorite
580 (NaOCl) based solutions, have been reported [58]. For mc-Si wafers, the challenge is to find
581 out a reproducible process to decrease the reflectance and to increase the photocurrent. The
582 research is currently focused on RIE processes [59].

583 In addition to traditional approaches to texturization, several alternatives have also
584 been developed. Laser texturing, lithography and plasma texturing are mainly used in
585 laboratory scale due to their cost and requirements [45]. Laser texturing is a promising
586 technique to obtain nanostructured surfaces under certain illumination and power conditions.
587 The types of surfaces obtained are known as black Si [60]. Using a femtosecond laser a
588 reduction of the reflectance to around 3% when this is used [61] has been reported. Recently
589 a two-step laser surface texturing process has been proposed and studied, where a high-
590 fluence laser ablation step was followed by a low-fluence laser-induced melting, producing a
591 molten material flow and re-solidification step to smooth the ablated dimple bottom surface
592 [62]. This study shows that the two-step laser surface texturing process can produce micro
593 dimples with very smooth bottom surfaces.

594 Plasma texturing, also called RIE, includes lithographic techniques in some cases.
595 This technique encloses different approaches as selective etching through alumina template,
596 SiO_2 micro-masks, catalytic action of various metals and nano-imprint lithography. These
597 approaches have been developed for the fabrication of sub-wavelength structure surfaces that
598 act as black Si.

599 2.3.3 P-N junction formation: Doping from solid/liquid/gas sources

600 When p-type wafers are used as base material, phosphorus incorporation on front side
601 of c-Si is performed to obtain p-n junction. There are several methods to carry out the step,
602 diffusion and ion implantation being the most usual processes. The obtained doping profiles
603 are highly dependent on the used technique. Doping by ion implantation is mentioned in Sec.
604 2.5.4.

605 If the diffusion process is considered, there are two possibilities from the point of
606 view of the dopant: (i) doping using solid/liquid sources, and (ii) doping using gas sources.
607 Doping from solid/liquid sources, also called dopant oxide solid source (DOSS) processes,
608 where a liquid doping, normally H_3PO_4 (phosphoric acid) or PCl_3 (phosphorus trichloride), is
609 spin coated on the surface and a phosphorus glass is formed when the samples are introduced
610 in the furnace. In this case, the doping is considered constant and finite, and the obtained
611 profile can be represented by an erfc function.

612 When doping from gas sources, a carrier with samples is introduced in a hot tubular
613 furnace. Pure nitrogen is used as a carrier gas guided through a container of liquid
614 phosphorus oxychloride ($POCl_3$) and released to the chamber mixed with oxygen to perform
615 the pre-deposition. This deposited material is a phosphorus silicate glass (PSG) and the flow
616 of $POCl_3$ is closed [27]. In comparison with the spin on dopant technique, in-line diffusion
617 from gas sources avoids contamination from the ceramic rolls on the conventional furnace,
618 and is the most widely used technique in commercial fabrication lines.

The thermal processes used to diffuse the dopants into the wafer are usually based on the conventional furnace process (CFP) with a temperature around 850ºC and times around one hour. However rapid thermal processes (RTP) are increasing their importance [63] because the diffusion time is reduced to the range of few minutes. In both the CFP and RTP processes, after diffusion and thermal processes, phosphorus glass formed on top of the wafers is etched away by using 10% HF solution.

Over the last decade, research in diffusion processes has been focused in its optimization [52]. Current research in this step (i.e. emitter formation) is focused on producing optimized selective emitters to enhance efficiency. This is discussed in Sec.2.5.6.

At this point it is also important to mention gettering (absorption) process. After defect reduction in the saw damage etching step, electrically active metallic impurities in the wafer are still present that reduce the lifetime of photogenerated carriers. The thermal processes that diffuse the dopant to form the emitter can also neutralize the electrical activity of some of these impurities by gettering (i.e. absorption of impurities) the locations along the wafer into an inactive energy states, improving the diffusion lengths in the material. This gettering process can also be introduced when Al-based contacts are fired in the fabrication process of the cell. Just as etching is used for the formation of texturing and saw damage etching simultaneously, the formation of the emitter and the firing of Al-based contact are simultaneously used for producing gettering on the electrically active metallic impurities.

2.3.4 Anti-reflection/passivation coating

The c-Si solar cell has two types of losses - optical and electrical losses. Optical losses reduce the quantity of photons that can be absorbed in the Si wafer as they are reflected on the Si surface or on the front side metallic contacts. Also, photons with energy shorter than the bandgap are not absorbed.

643 Texturization, as discussed above, is one way to reduce optical losses. Another is the
644 deposition of ARC on the front side of the solar cell to enhance the solar radiation absorption
645 and, at the same time, to passivate the c-Si surface. C-Si wafers have an average reflectance
646 between 30% and 40% in the 300-1200 nm range, so an ARC is needed to improve the solar
647 cell. As the quantum efficiency (QE) of Si based solar cell is optimal at 600nm, the refractive
648 indices of air and Si at 600nm are 1 and 3.46, respectively, the ARC refractive index should
649 be around 2 and, consequently, the ARC thickness is around 75nm. For this purpose, Si
650 nitride (SiN) layer is deposited on the Si surface. This step is usually performed by means of
651 a plasma enhanced chemical vapor deposition (PECVD) system by mixing silane (SiH_4), and
652 ammonia (NH_3) in the reaction chamber to form SiN layer on top of Si surface [27].
653 Improvements in texturization has resulted in a strong focus on SiN as ARC since specific
654 area and the light beam path are different in a pyramidal textured wafers in comparison with
655 non-textured wafers [64].

656 A surface passivation process consists of the saturation of Si surface bonds to improve
657 and stabilize the electronic properties of the surface. This is used to control and minimize the
658 recombination rate of the charge carriers at the surface, since the charge carrier
659 recombination velocity of an unpassivated surface is very high (around 10^4-10^6 cm/s), which
660 decreases the photocurrent.

661 The SiN anti-reflecting layer acts as effective surface passivation layer for Si surfaces,
662 matching both requirements simultaneously for the fabrication of c-Si based solar cells. As it
663 has been mentioned, this layer is normally deposited using the PECVD technique [65] at a
664 low-temperature of ~300ºC. The effects of the bandgap and defects of SiN on carrier lifetime
665 and the transmittance in c-Si solar cells are currently being studied for increasing the values,
666 as the mixing of the precursor gases, flux ratios and temperatures greatly influence the final
667 properties of the solar cell.

668 Another option is indium tin oxide (ITO). This material is a transparent conductive
669 oxide widely used in solar cell applications. Its optical properties make it an excellent ARC,
670 and its high electrical conductivity allows it to improve the collection efficiency in solar cells.
671 Magnetron sputtering is the common technique used to deposit ITO. A subsequent annealing
672 of the wafer is required to improve the electrical properties of the device. Also, titanium
673 dioxide (TiO_2) has been largely used as ARC in solar cells because the deposition of this
674 material on the Si surface can be performed by atmospheric pressure chemical vapor
675 deposition (APCVD) at low-temperatures. Also, this material is non-toxic, non-corrosive, has
676 a low-cost and shows good surface passivation properties [66]. However, in the 1990s it was
677 replaced by SiN in the standard process because SiN has better surface passivation properties,
678 and can also passivate bulk defects by hydrogenation [23].

679 SiO_2 grown by thermal oxidation has also been used as ARC and surface passivation
680 layer. However the growth process here is carried out at high temperatures (900-1100ºC),
681 making it expensive and incompatible with certain steps that do not withstand those high
682 temperatures. The refractive index of SiO_2 is also not as optimal as SiN for c-Si based solar
683 cells. The amorphous Si oxynitride films observed in the interface between SiO_2/c-Si also
684 introduce recombination traps for carriers that reduce their lifetime. Alternatively, porous Si
685 formed by chemical [67], electrochemical [68] or vapor [57, 69] etching shows impressive
686 properties as ARC. Porous Si in combination with Si oxide (SiO_x, $0<x<2$) can be tuned to the
687 refractive index of the layer. However, the electrical properties of the Si wafer with porous Si
688 layers on the surface traditionally have been very poor for efficient solar cell applications
689 [70]. Hydrogen is the best passivating material for Si surfaces but it is meta-stable. Finally,
690 TiO_2 is an excellent ARC due to its high refractive index of 2.6 at 600 nm, and high
691 transmittance in the range of 300 and 1200 nm. Also, published results are promising because

it can be deposited by APCVD offering cost reduction and an easy implementation of this alternative in the semiconductor industry [71].

2.3.5 Metallization

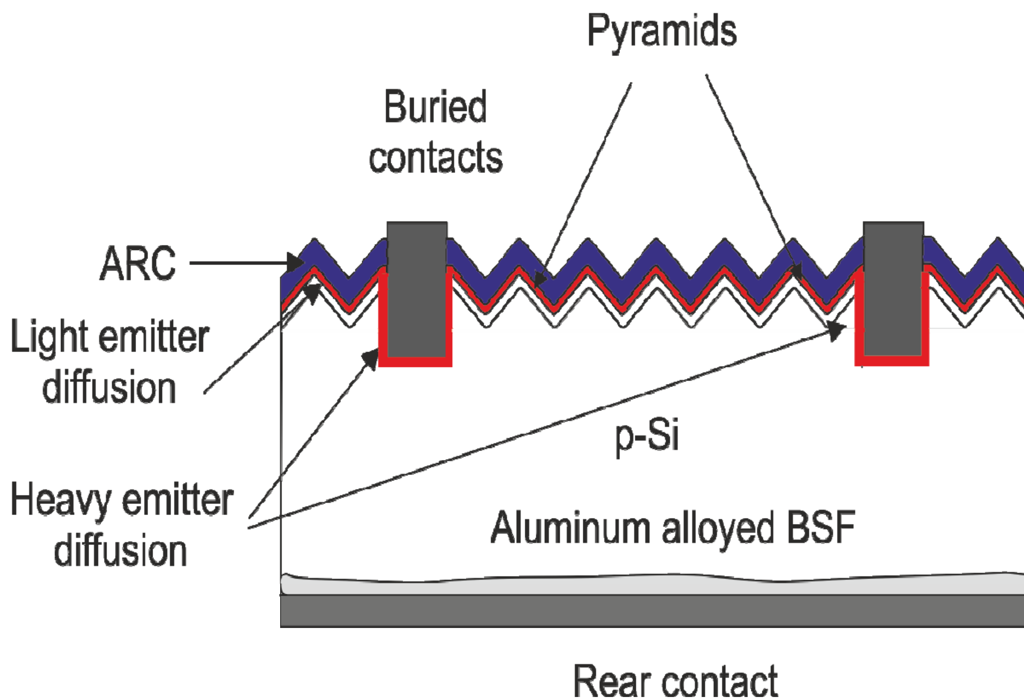
Once the p-n junction has been formed and the ARC deposited on top, the next step is the metallization on the top and bottom side of the cell. The front side metallization is a grid composed of busbars (usually two or three), and several thin fingers (70-100 µm wide) that cover the front side of the cell. The front side metallization produces shadowing losses, series resistance losses, and determines emitter diffusion profile and surface doping concentration, and influences the choice of a defined surface passivation technique [72]. For p-type c-Si wafer, Al is used for back contact and Ag is used for front contact.

A widely used technique to place the metallic contact is screen printing. In the mid-1970s screen-printed solar cell was first developed [73]. This technique uses a paste, an Al compound for the back side, and a Ag compound for the front side [74] with micrometric metal particles and additives. These compounds are pressed to pass through a mesh of steel or polyvinyl to print the metallic pattern on the Si surface. After the metallic paste is placed, a firing process is required to produce an Ohmic contact on the Si surface. This technique is commonly used for in-line c-Si solar cells manufacturing. It is a four step process that involves: (i) Ag front side metallization and drying, (ii) Ag back side metallization (busbars) to connect the solar cells into the solar module and another drying process, (iii) back side blanket Al metallization, and (iv) the firing process, normally between 750ºC-850ºC [75]. A complementary option is the finger roller-printing technique. This consists of a rubber wheel coated with a thin layer of metallization paste that rolls across the wafer for finger contact [76].

The rear contact also can be placed by physical vapor deposition methods such as sputtering, thermal or e-beam based evaporation. Using these techniques the formed layers

717 show very high conductivities. Therefore to reach the performance needed, thinner contact is
718 enough, compared to the screen-printed contacts [27].

719 One of the most promising techniques [77, 78], normally used with the selective
720 emitter, is the buried contact metallization (Fig. 6). It was commercially applied first by BP
721 Solar in the late 1990s. By means of laser fusion technology, it is possible to make a groove
722 of approximately 20 µm wide and up to 100 µm deep into Si surface. This technique provides
723 two advantages: (i) the reduction of the shadowing loss, from typically 8% from screen
724 printing solar cells to around 3%, and (ii) the filling of the grooves with contact material,
725 reducing around three times the standard width of the metallic, from typically 100 µm in
726 screen printing to 30 µm widths.



727

728 Fig. 6 Cross-sectional diagram shows buried contact solar cell. Buried contact solar cell was developed more
729 than 20 years ago and transferred to production line in the early 1990. Laser grooved buried contact solar cell is
730 a high-efficiency commercial technology. Buried contact overcomes disadvantages of screen-printed contacts
731 such as shadowing and series resistance caused by metal grid pattern. To lower shadowing loss and series
732 resistance, metal contact is buried inside the cell with high aspect (height/width) ratio. Using this technology, a
733 narrow strip of closely spaced metal grids can be used on the surface and at the same time high transparency can
734 be maintained. In screen-printed solar cells, 5-7% of incoming light is blocked due to shadowing, whereas in
735 buried contact solar cells, metal lines can be less than 20 µm and this corresponds to <3.5% shadowing. Lower
736 shadowing loss results less reflection from the surface, and improvement in J_{sc}.
737

738 The main reasons that the buried contact metallization has not been further introduced
739 in the industrial process for manufacturing solar cells are that this technique produces defects
740 on the Si surface, leading to decrease in cell performance and increase in the production cost.
741 Consequently, these drawbacks need to be overcome for the buried contact metallization to
742 surpass screen printing as the preferred technology for metallic contacts of Si solar cells.

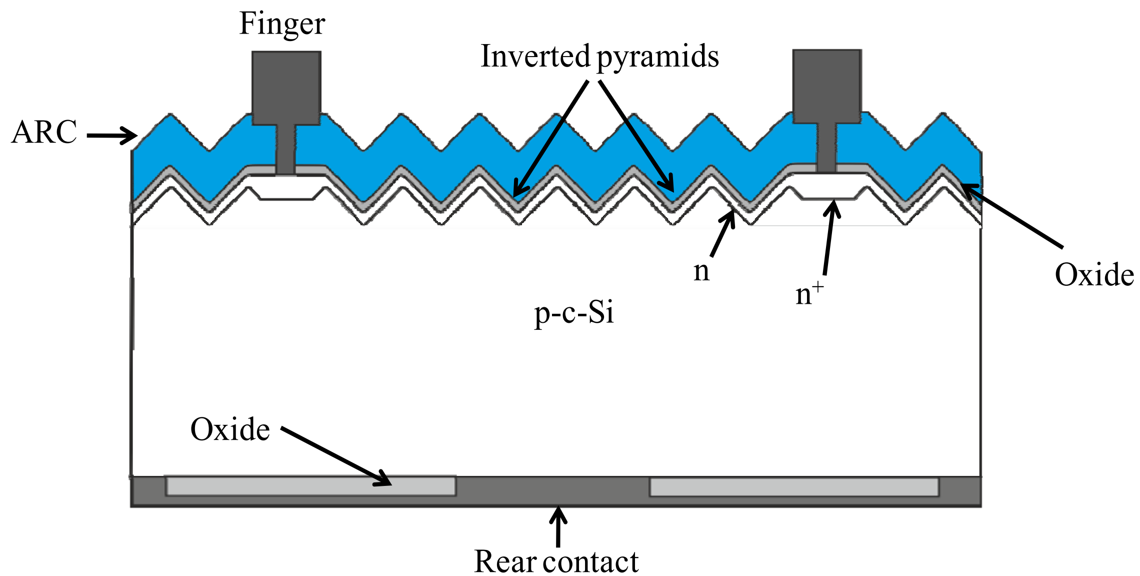
743 Currently, standard metals used for the front side and back side metallization are Ag
744 and Al, respectively. However other less expensive alternatives for the front side, such as
745 copper (Cu), has been studied for more than 10 years [79] to replace Ag. A recent work [80]
746 analyzes the current and future front side metallization scenario, suggesting that the
747 metallization with Ag is expected to be reduced in the coming next 10 years, decreasing from
748 the current 90% to a 50% of the market share. Simultaneously Cu and other alternative
749 materials will increase their relevance as substitutes of Ag. An important reason why one
750 metal may replace another over the years when it comes to solar cells is global demand-and-
751 supply of various metals.

752 ## 2.4 Other types of c-Si based solar cells

753 Some of the solar cells discussed in this section are very expensive compared to the
754 ones obtained by the standard procedure described in Sec. 2.3 and commonly used in the
755 industry. However as research into these solar cells continues, a subsequent reduction in
756 production costs may be expected. At the same time, some of the features of these solar cells
757 may be incorporated to current commercial standard procedures and result in efficiency and
758 cost improvements.

759 As reported [81], advanced solar cells such as PERC, bifacial solar cells (light
760 sensitive on both sides) and n-type solar cells have gained relatively considerable attention. In
761 the PERC structure, as shown in Fig. 7, full area Al-BSF is replaced by a dielectric
762 passivation, which is locally opened for the placement of the metallic contact [82]. 21.2%

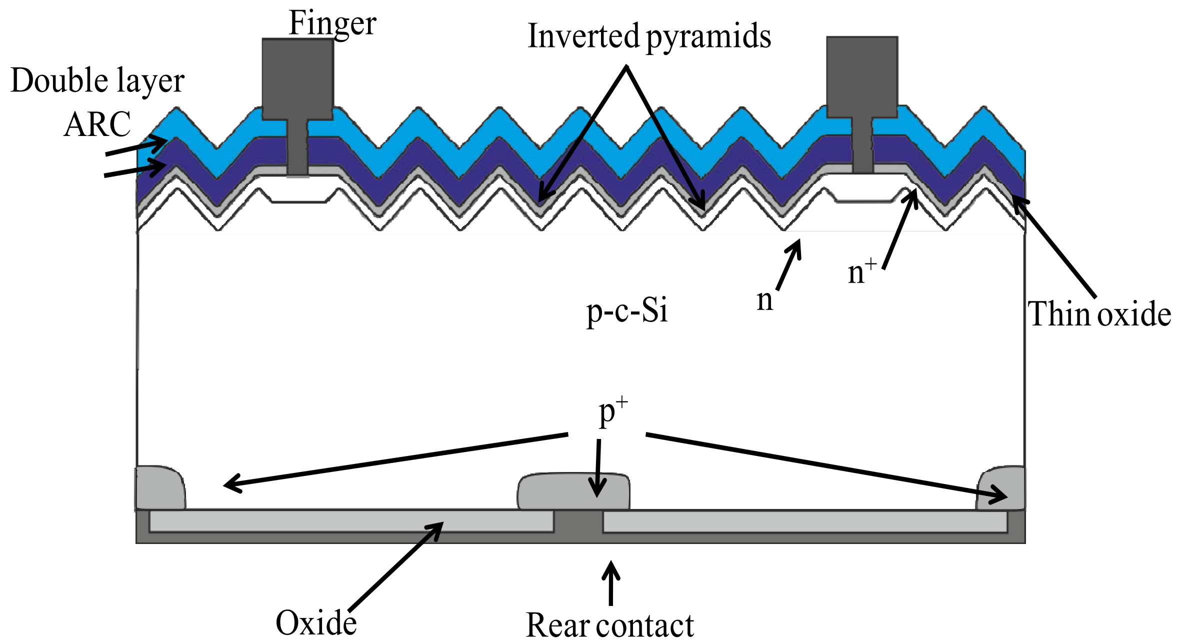
763 efficiency is the highest value reported so far [83]. Rear side dielectric passivation layer(s)
764 improve passivation quality and internal reflection compared to full area Al-BSF.



765

766 Fig. 7 Schematic diagram shows cross-section of PERC solar cell structure. The rear side of PERC cell is
767 passivated by dielectric/stack except at the region where contact metal is touching c-Si. Rear side dielectric
768 (oxide) acts as mirror, reflects light into the bulk and thereby improving photocurrent. A major advantage of
769 using rear side passivation instead of full area Al-BSF is the enhancement in J_{sc} that comes from enhanced
770 reflectivity of 90-95% at 1000 nm compared to 65% from full area Al-BSF [84]. By reducing metallization
771 fraction at the rear side, defects at metal/c-Si interface becomes less effective and the difference in V_{oc} and J_{sc}
772 between PERC and PERL cells becomes small. When thinner c-Si is used for fabrication, reflectivity from rear
773 structure becomes significant. PERC technology developed by Roth & Rau and successfully implemented under
774 the name MB-PERC.

775 In other words, compared to full area Al-BSF cell, PERC advantages are lower SRV
776 and an improved optical performance. However, additional reduction of the SRV and optimal
777 use of high-resistivity materials can be performed in the PERL cell structure, which has at
778 present 1 sun world efficiency record of 25% for c-Si based solar cells since 1998. PERL
779 type bifacial structures have also been introduced in the industrial production lines over the
780 last 5 years, substituting the inverted pyramids by chemically formed pyramids. Cross-
781 sectional diagram of PERL cell is shown in Fig. 8. Advantages and disadvantages of local
782 BSF are discussed in Sec.2.5.7.

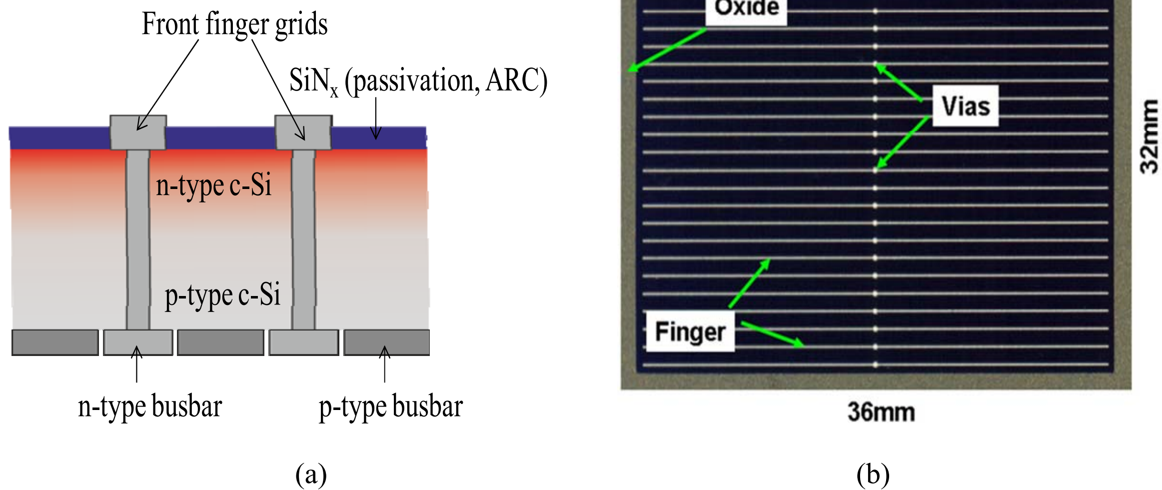


783

784 Fig. 8 Schematic diagram shows PERL solar cell structure. In the inverted pyramid surface, incident light
785 undergoes double bounces meaning that incident light will have two chances of transmission into c-Si. In PERL
786 structure, at the rear side, to reduce minority-carrier recombination at the metal/c-Si interface, boron diffusion is
787 performed locally under the metal contact, whereas in PERC structure local diffusion is not performed under the
788 metal contact. Local BSF in PERL cell improves V_{oc} and J_{sc} since electric field in the BSF region between p+/p
789 junction drives electrons away towards the p-n junction and reduces surface recombination at the defective
790 metal/c-Si interface. PERL cell technology named as Pluto was developed by Martin Green and Stuart Wenham
791 at University of New South Wales and commercialized by Suntech Power.

792

793 The MWT solar cell is a back contact solar cell that uses a technology very similar to
794 that of conventional screen-printed solar cells. MWT solar cell is shown in Fig. 9. As
795 compared to conventional solar cell technology, only two additional steps are required, viz.
796 (i) via drilling for the interconnection between front and back side, and (ii) the metallization
797 through vias (holes). An efficiency gain of about 0.5% in absolute terms and a current gain of
798 about 3.5% due to less shading on the front side are achieved as compared to the standard cell
799 concept [85]. A highest average and peak efficiency of 19.6% and 20.0% has been reported
800 for MWT c-Si solar cells [86].



801

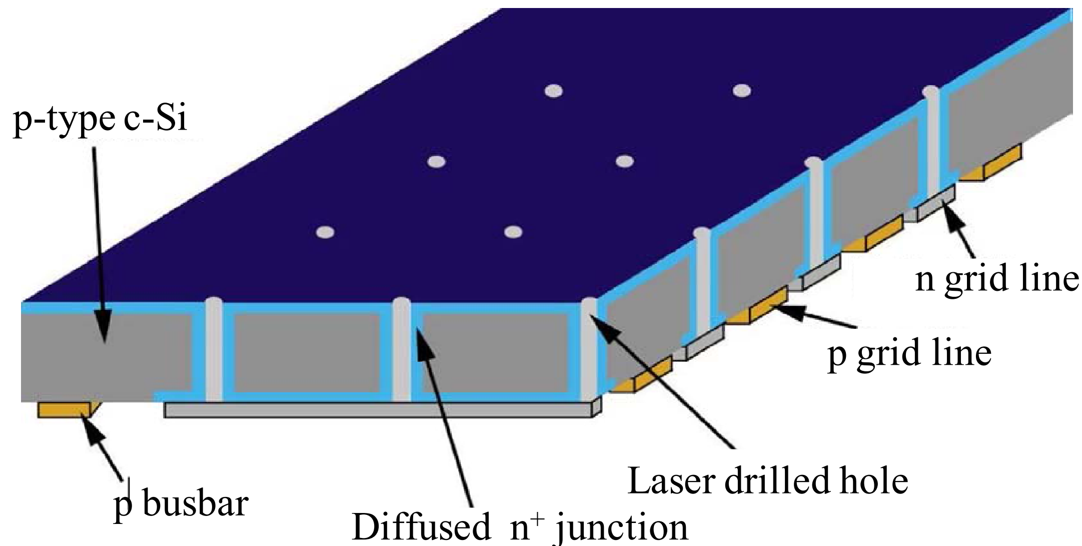
802 (a) (b)

803 Fig. 9 (a) Schematic diagram of MWT solar cell [87], and (b) top view showing front finger grids and absence
804 of busbars [88]. On the rear side busbars are wide and therefore, series resistance loss arising due to busbar can
805 be eliminated. MWT cells have higher efficiency (~0.5%) than conventional solar cells due 50% less
806 shading/metallization area on the front side [89, 90]. Less shadowing improves J_{sc} and fill factor. MWT c-Si
807 solar cell technology has been transferred successfully to production [86, 91] and the cells have produced an
808 average and peak efficiency of 19.6% and 20.0% respectively. For MWT cells, welding is not required when
809 assembling MWT cells into modules and results in lower power loss and lower cell breakage rate. Fig. 9 (b)
810 from [88], Tobias Fellmeth, Michael Menkoe, Florian Clement, Daniel Biro, Ralf Preu, Highly efficient
811 industrially feasible metal wrap through (MWT) Si solar cells, Solar Energy Materials & Solar Cells 94 (2010)
812 1996–2001. © Elsevier 2010. License number 3457011111677.

813

814 The EWT solar cells are similar to the MWT solar cells. The difference lies in the fact
815 that here the n-type contacts are placed on the rear side. The rear surface of the wafer presents
816 an emitter structure that is connected through with the front surface emitter. EWT solar cell is
817 shown in Fig. 10.

818 The emitters on the front and rear side can both collect charge carriers. This makes the
819 EWT cell very attractive for low lifetime materials. However this structure presents a series
820 resistance problem [27]. Moreover expensive metallic formation techniques are required. The
821 lack of significant current research focus on EWT, as gauged through the paucity of research
822 publications per year, suggests that the future of EWT solar cells is uncertain.



823

824 Fig. 10 Picture shows EWT solar cell structure [92] quite similar to back contact back junction solar cell. Laser
825 drilling is used to open 15000 vias (holes) having each 80μm diameter. Several thousands of vias/sec can be
826 drilled [93]. In EWT cell, no grids lines, and no busbars are present on the light entering side (note that in MWT
827 structure, grid lines are present on the light entering side, and no busbar is present). Both p-type and n-type grids
828 as well as busbars are placed on the rear side, and trade-off between shadowing loss and series resistance is
829 eliminated. Grid less front surface enhances light incident area and improves J_{sc}, fill factor since on the rear side
830 grid lines and busbars can be wide. Reproduced from [92], James M. Gee, Prabhat Kumar, James Howarth,
831 Todd Schroeder, Jeff Franklin, Jason Dominguez and David Tanner, Development of industrial high-efficiency
832 back-contact czochralski-Si solar cells, Prog. Photovolt: Res. Appl. 19 (2011) 887. © Copyright 2011 John
833 Wiley & Sons, Ltd. License number 3457020769998.

834
835 Another interesting area of current research is the realization of bifacial solar cell with
836 boron diffusion either from a gas source or a solid source such as a boron silicate glass. A
837 conversion efficiency of 18.4% has been obtained on c-Si wafers using boron BSF and Si
838 carbide (SiC)/SiN ARCs. This structure easily fits with the development of a selective emitter
839 at the front side of the cell and can potentially achieve conversion efficiencies above 19%
840 [94].

841 ## 2.5 Low-cost c-Si based solar cells

842 Since cost and efficiency of solar cells are the most important determining factors for
843 commercial utilization, it is worthwhile to further explore how these issues are being
844 currently addressed. In the context of solar cell development, low-cost always refers to cost
845 per unit of energy or power, being the figure of merit \$/Wp preferred to that of \$/kWh due to
846 the fact that the former focuses on technology and discards the influence of radiation, system

847 reliability and other factors. Lowering the cost means minimizing the $/Wp, and to fulfill this
848 goal, two approaches can be followed: reduce the numerator (so, looking for cheaper
849 processes) or increase the denominator (so, producing more efficient cells), or both.

850 To lower the cost of c-Si solar cell, the following routes are pursued: use of lower
851 quality Si feedstock and wafers, search for cheaper dopant sources, and search for cheaper
852 metallization schemes. To increase the efficiency, the efforts in the field of front junction
853 solar cells have been focused in implementing selective emitters at the front and reducing
854 BSF recombination at the rear by industrially feasible processes. All these concepts are
855 reviewed in the following sections.

856 2.5.1 Low-cost Si wafers: Relaxing feedstock specifications

857 The raw material for Si solar cells has traditionally come from the polysilicon market
858 for microelectronics, providing a ultrapure feedstock at a cost that accounts for around 15%-
859 20% of the total PV module cost (in $/Wp). The availability of Si due to the tremendous
860 growth of the PV sector and the search for cheaper purification routes have motivated
861 research into alternatives to the traditional so-called Siemens process. As mentioned in Sec.
862 2.2.1, in this process, metallurgical Si is transformed into a volatile compound, typically
863 TCS, which is further purified and then converted back to solid Si in a chemical vapor
864 deposition process. Some of the alternatives rely on the same basis, but introduce significant
865 changes in certain steps of the process. For example, using SiH_4 as the intermediate volatile
866 compound produces Si deposition in a fluidized bed reactor or a free space reactor [95]. Their
867 promoters claim that the quality of the resulting material is similar to the conventional one, so
868 no further adaptation of the solar cell process is needed. Recycling the byproducts efficiently
869 is also an option.

870 Another group of alternatives avoids the conversion of metallurgical Si into a volatile
871 compound, and upgrade the metallurgical Si through a combination of steps suited for

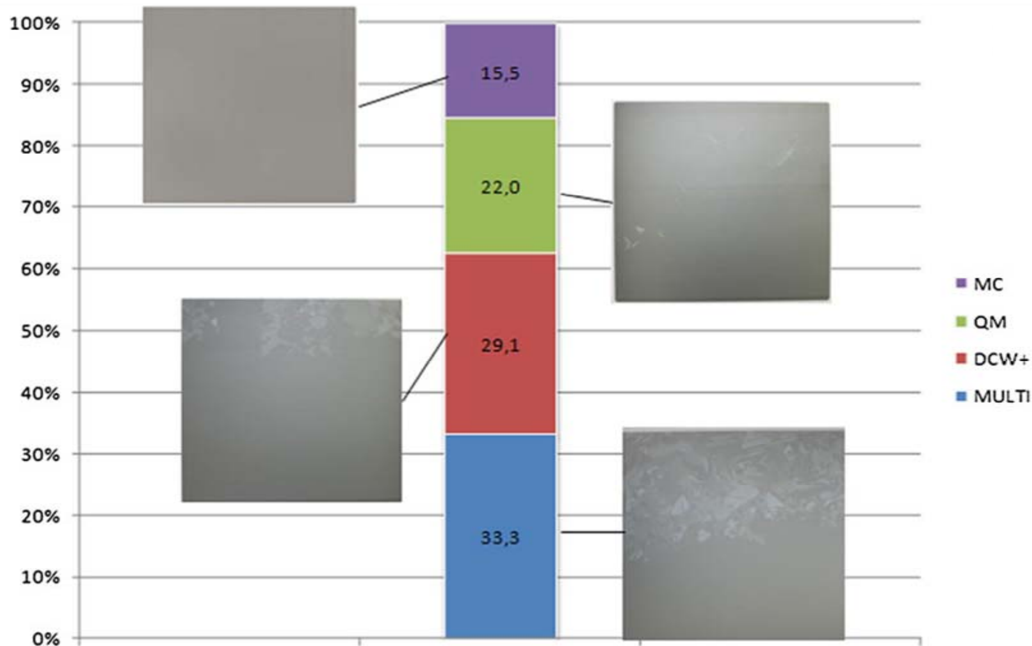
872 different impurities [96,97], decreasing to some extent the energy consumption in the
873 deposition step and hence the cost of the process. The purity usually reached with these
874 processes is lower than that of the TCS route, but that does not necessarily mean that the
875 material cannot be used for solar cells. In fact, by introducing some changes in the thermal
876 profiles of the crystallization and solar cell processing steps, similar solar cell efficiencies
877 have been achieved with this material to the semiconductor grade one [98-101].

878 At a broader level, though, a drastic reduction in cost of conventional polysilicon is
879 hindering the development of these alternatives. In order to be commercially viable, there is a
880 need to clearly justify their good performance versus satisfactory yield and cost-effectiveness
881 in order to undertake the large investments with the production.

882
2.5.2 Producing cheaper wafers
883

884 Si wafers for solar cells are made by slicing ingots grown by either monocrystalline
885 technique or the multicrystalline one. Recently, a new crystallization process has been
886 proposed that aims to combine the high-throughput of the latter with the better quality of the
887 former. This is done through the use of monocrystalline seeds on the bottom of the crucible in
888 a directional solidification furnace [102]. It has been called mono-like or quasi-mono, due to
889 the fact that the ingot is not 100% monocrystalline, as crystals of different orientations
890 nucleate from the walls of the crucible. Figure 11 depicts an example of wafer-type
891 distribution. Even though efficiency increases of 1-1.5% in absolute have been reported
892 compared to traditional casting, to fully exploit the potential of the material a few issues
893 should be industrially addressed: the need of sample classification to apply different solar cell
894 process conditions to different samples (which comes for example from the different
895 texturing techniques applied to mono and multi wafers), and the fact that part of the material,
896 even the monocrystalline one, is rich in dislocations [103-105].

897



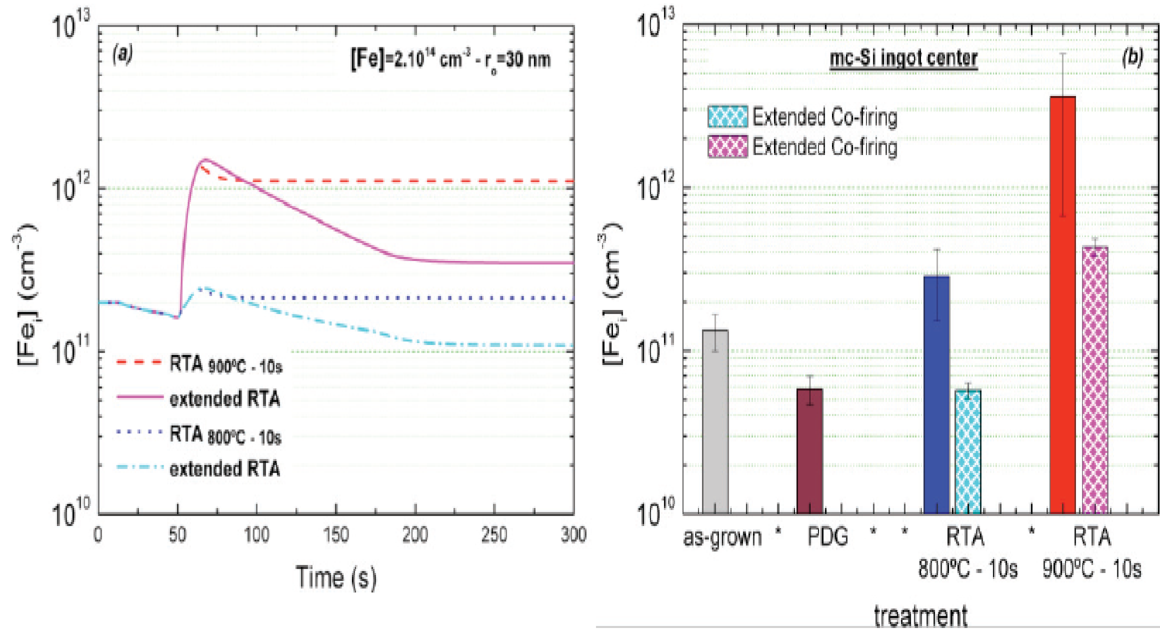
898

899 Fig. 11 Wafer-type distribution of a mono-like ingot according to their percentage of macroscopic
900 monocrystalline feature: MC: mono-casting (100% mono); QM: quasimono (>90% mono); DCW+: DC Wafers
901 PLUS (>75% mono); MULTI: mono/multi and mc-Si (<75% mono). With permission from [105], Ismael
902 Guerrero, Vicente Parra,Teresa Carballo, Andrés Black, Miguel Miranda, David Cancillo, Benito Moralejo,
903 Juan Jiménez, Jean-François Lelièvre, Carlos Cañizo, About the origin of low wafer performance and crystal
904 defect generation on seed-cast growth of industrial mono-like Si ingots, Prog. Photov: Res. Appl. **22** (2012)
905 923. Copyright © 2012 John Wiley & Sons, Ltd. License number 3457490569073.
906
907 Another approach that offers the advantage of eliminating the slicing process is the
908 growth of thin Si ribbons directly from a polysilicon melt. Several technologies, such as edge
909 defined film-fed growth, string ribbon, dentritic web (WEB, recently revisited as Ribbon on a
910 Sacrificial Template), and ribbon growth on wafer has been promoted [106]. Industrial
911 efficiencies in the range of 15-16% have been reached by the most advanced techniques,
912 while others are on the 13-14% level [107-109]. With more sophisticated processing,
913 efficiencies around 18% have been reached [110,111]. Although their cost reduction potential
914 remains, there are also other current market conditions that are slowing their development.
915 The drawback of all of them is the high density of defects (dislocations, grain boundaries,
916 impurities) and the uneven surfaces that require specific processes for texturing, phosphorus
917 diffusion, SiN) deposition or screen printing for implementing in the solar cell process. These

processes may even need replacement with alternative techniques, for example, the direct writing of Ag pastes for metallization [112,113].

2.5.3 Living with defects and impurities

Solar cell processing should integrate steps that can reduce the deleterious effect of impurities and crystalline defects. These steps are gathered under the concept of defect engineering. In fact, solar cells made of traditional Si sources already benefit from them, in particular from external gettering of impurities to the phosphorous and Al layers, as we explained in Sec. 2.3.3. In wafers from low-cost sources, or even in those coming from the border and edge regions of multicrystalline ingots where the density of impurities is higher due to in-diffusion from the crucible, defect engineering techniques aim at manipulating metal concentrations and distributions to reduce their impact in solar cell performance [114]. For example, it has been shown that a slow cool down or a low-temperature plateau after phosphorous diffusion reduces iron (Fe) interstitials, and increases carrier lifetime and solar cell efficiency [115-117]. Other strategies such as implementing thermal pretreatments or changing the firing step thermal profiles are being studied [118-120]. As an example taken from Ref. [119], Fig. 12 compares the effect of a standard firing step (realized in this case in a RTP furnace), which produces an increase in interstitial Fe concentration due to precipitate dissolution. On the other hand, with a modified one (which is called extended RTP) segregation gettering is enhanced and so contamination levels are reduced.



939

940 (a) (b)

941

942 Fig. 12 (a) Simulated interstitial iron [Fe_i] concentration as a function of time during a 10s standard and
943 extended RTP, for two different process temperatures and an arbitrary as-grown Fe concentration and
944 distribution, (b) measured Fe_i concentration obtained for mc-Si wafers taken from the center of an industrial
945 ingot, showing the reduction due to the extended RTP (stripped bars) as compared to the standard (full bars).
946 Reproduced from [119], S Glunz, A Aberle, R Brendel, A Cuevas, G Hahn, J Poortmans, R Sinton, A Weeber,
947 J-F. Lelièvre, J. Hofstetter, A. Peral, I. Hoces, F. Recart, C. del Cañizo, Dissolution and gettering of iron during
948 contact co-firing, Energy Procedia, **8** (2011) 257. Copyright © 2011 Published by Elsevier Ltd. License number
949 3457501260401.

950

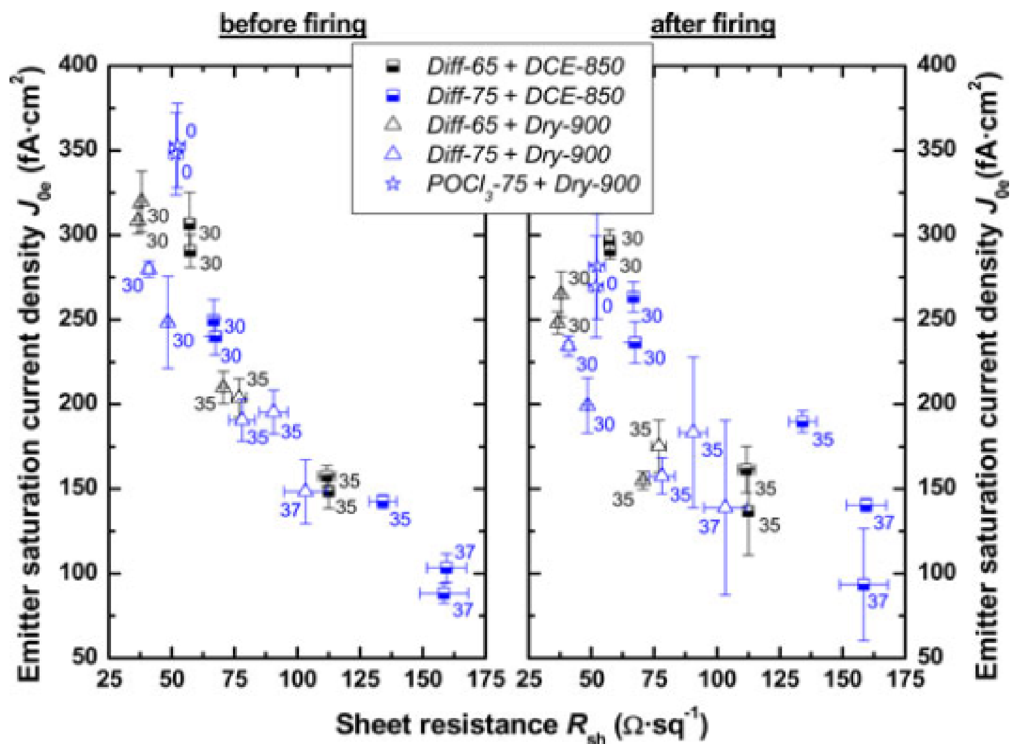
951 The challenge here is to implement defect engineering techniques at the industrial level,
952 where modifying thermal step profiles can impact throughput, and where tailoring processes
953 to specific wafers introduces further complexity.

954 ### 2.5.4 Low-cost approaches for doping

955 Emitter doping from a $POCl_3$ liquid source in a quartz furnace has the drawback of being
956 a batch type process, and in-line options are promoted, where a phosphorus source is applied
957 to the wafer surface, dried, and then diffused in an infra-red belt furnace, benefiting from
958 automation, high-throughput and the ability to implement temperature profiles. Dopant
959 sources can be screen-printed [121], spun-on [122-126], sprayed-on [127-130], deposited by
960 CVD [131] or even diffused from a gas source [132]. In some of the reported experiments,
961 dopant drive-in is performed by RTP and not in an infrared furnace.

962 Efforts in characterizing emitter performance have been successfully applied, in terms of
963 dopant diffusion, sheet resistance and emitter saturation current. An example of the
964 comparison of the saturation current with state-of-the-art $POCl_3$ diffusion is given in Fig.13,
965 taken from Ref. [131].

966



967

968 Fig. 13 Emitter saturation current densities (represents sum of all recombination currents in the emitter),
969 obtained from lifetime measurements, of passivated samples doped by the method proposed on [127] before and
970 after firing. Values for two different diffusion processes (Diff-65 and Diff-75) and two different oxidation
971 processes (DCE-850 and Dry-900) are given. The values are under those of a typical $POCl_3$ process (which is
972 marked with stars with the number 0). Reproduced with permission from [131], Fallisch A, Wagenmann D,
973 Keding R, Trogus D, Hofmann M, Rentsch J, Reinecke H, Biro D., Analysis of Phosphorus-Doped Si Oxide
974 Layers Deposited by Means of PECVD as a Dopant Source in Diffusion Processes. IEEE J. Photovoltaics, **2**
975 (2012) 450. Copyright © 2012 IEEE. License number 3504480294880.

976

977 Solutions currently exist that take advantage of these low-cost doping technologies,
978 addressing key aspects such as emitter homogeneity, lack of shunting and gettering ability,
979 and successful implementation of emitter profiles with convenient sheet resistances.
980 Furthermore, some of these approaches have the potential to achieve high-efficiencies, with
981 efficiencies of 18%-19% being reported for c-Si [125,126] and 15%-16% for mc-Si [123,133]
982 based solar cells.

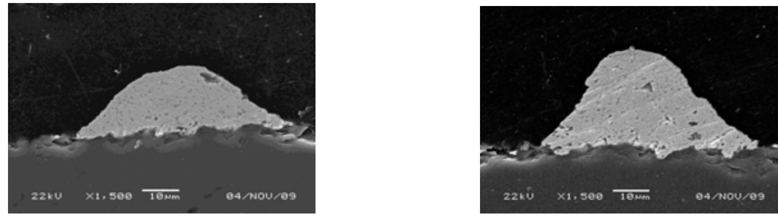
Boron, as a p-type dopant can substitute Al in BSF layers, reducing recombination and bowing, and can also form the p-n junction on n-type c-Si wafers. Cost-effective techniques to diffuse boron are being promoted [134-136], as the traditional boron tribromide (BBr_3) source in a diffusion furnace implies a batch type process, and a somewhat involved process optimization [137,138]. The use of these alternative dopant sources can also facilitate the implementation of local BSFs. Passivation of boron doped layers is also an aspect that needs specific solutions [139].

Finally, ion implantation is another option, for both phosphorus and boron doping [140,141] that benefits from its wide use in microelectronics. Ion implantation allows for an accurate control of the dose and depth of the dopant, and needs a subsequent annealing to reduce the damage introduced by the implantation.

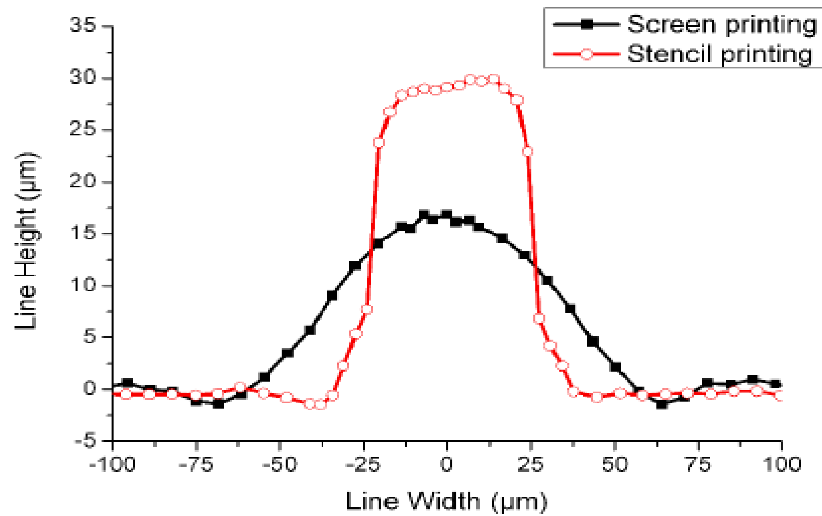
2.5.5 Low-cost approaches for metallization

Traditional screen printing metallization is evolving towards lower consumption of expensive Ag, thinner fingers to improve the aspect ratio (height/width), and different paste formulation to contact lowly doped emitters. Substituting mesh screens by stencil-based screens may help to reach finer lines (50-60 µm) with better aspect ratios, and benefit from a slower deterioration of the printed patterns [142]. Separating screen printing for fingers and busbars (which is called dual printing) may help in optimizing separately geometry and paste formulation [143].

1006



1007 (a) Single print Double print



1008

1009 Fig. 14 (a) Finger cross-section of single and double print [143], (b) Fired finger profile comparison between
1010 stencil (60µm) and screen (105µm opening) [142]. Figure 14 (a) from [143], Tung Pham, Weiming Zhang,
1011 Tracy Gou, Dean Buzby, Kristin Murphy, Improving electrical performance by double print method and non-
1012 contact busbars, 25th EU PVSEC/5th World Conference on Photovoltaic Energy Conversion, 6-10 September
1013 2010, Valencia, Spain, pp.2378-2380, permission granted. Figure 14 (b) from [142], Hoornstra J, Heurtault B,
1014 Stencil print applications and progress for crystalline silicon solar cells, 24th EU PVSEC Proc. European
1015 Photov.Sol .Ener. Conf., 21-25 September 2009, Hamburg, Germany 2009, pp.989-992. Permission granted.

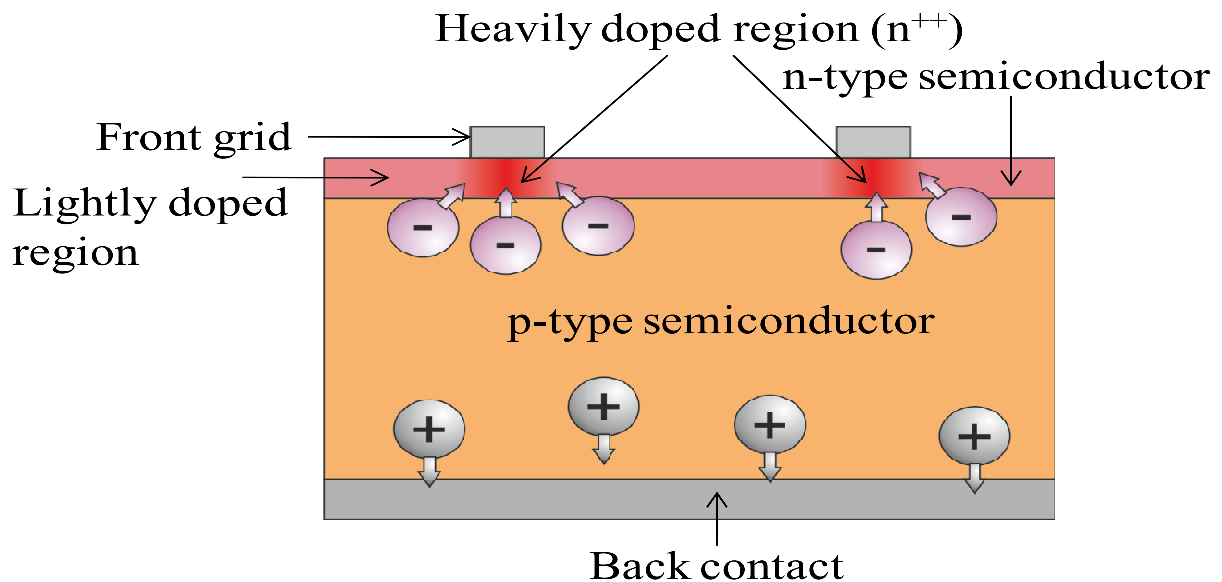
1016

1017 Another approach that is compatible with the use of stencil screens or the dual
1018 printing is to separate metal deposition in two steps: first a layer designed for good contact
1019 with Si is deposited, which is followed by a second layer designed to increase conductivity.
1020 The simplest would be to optimize the properties of two different pastes that are being used in
1021 industry as double printing or print-on-print [144,145]. Alternatively, the contact layer can be
1022 done by roller printing [146], pad printing [147] or nickel plating [148]. Inkjet printing is also
1023 being explored, as it can produce thin lines and as a non-contact method it can avoid
1024 mechanical problems with very thin wafers [149]. To overcome limitations in metal particle
1025 sizes that may obstruct the printer, an aerosol technique can be implemented instead [150].

1026 For thickening of the layer, light-induced electroplating is a good candidate that can give very
1027 favorable aspect ratios [151]. Examples of techniques resulting in improved finger cross
1028 sections are shown in Fig.14. The challenge in all these cases is to implement the techniques
1029 at the industrial level with sufficient throughput and reproducibility [152].

1030 2.5.6 Efficiency enhancement: Industrially feasible selective emitter
1031 technologies

1032
1033 A selective emitter [153] is formed by heavily doping underneath the contact grid and
1034 by weakly doping the illuminated area (Fig.15). This doping also results in an adequate sheet
1035 resistance to improve the electrical properties of the front metallic contact and low resistance
1036 in the illuminated areas.



1037

1038 Fig. 15 Schematic diagram shows the location of the selective emitter having a low sheet resistance of 35-55
1039 Ω/□. A selective emitter is a front junction, front contact solar cell configuration. Using this approach, in
1040 selective regions, i.e. surface regions underneath the grids are heavily doped to improve electrical (ohmic)
1041 contact between the grid and Si. The remaining emitter surface regions between the grids are lightly doped to
1042 minimize recombination losses and to improve cell's blue response. In other words, selective emitter structure is
1043 used to reduce losses originating from the front side. Selective emitter can be formed by laser doping, doped Ag
1044 paste, screen printing, etchback etc.

1045
1046 The optimum emitter profile is different for a contacted region than for a passivated
1047 non-contacted one (with higher surface concentration and longer junction depth in the first
1048 case). While in traditional cells a design compromise is reached, resulting in emitters of 50-
1049 75 Ω/square, the process here can implement selective emitters, provided the gain in

1050 efficiency justifies the increase in complexity. While selective emitters have been
1051 implemented in laboratory cells since long ago [154], recent efforts have succeeded in
1052 adapting the concept to an industrial environment through the use of a number of techniques
1053 [153].

1054 (i) Performing two separate diffusions, a heavier one restricted to the regions to be metallized
1055 by a screen-printed or deposited by mask [155].

1056 (ii) First diffusing a homogeneous thick emitter by conventional means; then applying a
1057 screen-printed or inkjet mask to protect the regions to be metallized, and removing the
1058 superficial dead layer in the non-protected region by a plasma etch [156], a wet etch [157] or
1059 an etching paste [158].

1060 (iii) Diffusing a solid dopant in the areas to be contacted, so that a highly doped emitter is
1061 formed there, while a much lighter diffusion takes place at the uncovered regions from the
1062 gas phase [159].

1063 (iv) Protecting the regions that will not be contacted with a mask, so that during phosporous
1064 diffusion a highly doped emitter is formed in the non-protected areas, while under the
1065 protected ones only a smaller dose of dopant is able to diffuse into the Si because the mask
1066 slows down penetration, giving thus a low doped emitter there. The mask is subsequently
1067 removed [160].

1068 (v) Forming first a high sheet resistance emitter, and then screen printing a metallization
1069 paste containing phosphorus, so that when firing, a heavily doped alloyed layer is formed
1070 under the metal fingers [161]. The drive-in of the heavier doped region can also be done by
1071 laser [162].

1072 Most of these techniques require some kind of pattern aligning to print the front contact
1073 fingers on the heavily-doped regions, something suitable for state-of-the-art automatic
1074 equipment. Gains in absolute efficiency of around 0.5% have been reported.

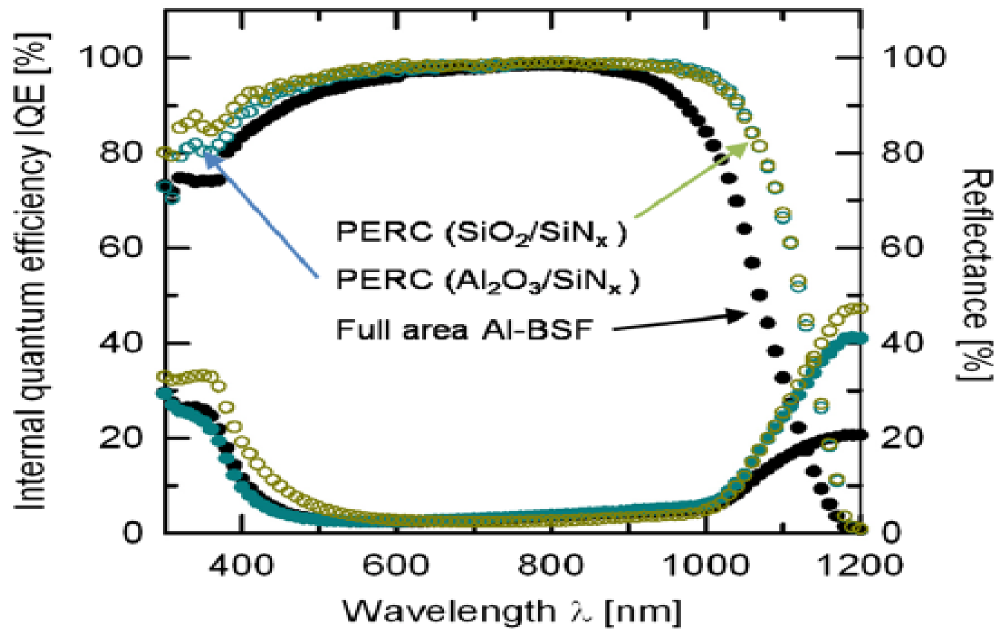
2.5.7 Local BSF at the rear: Advantages and drawbacks of the technologies implemented in industry

Passivating the rear surface with a dielectric film can increase cell efficiency, especially for wafers were carrier diffusion length is higher than thickness. Rear side recombination can be reduced as compared to a full BSF, and good reflecting properties can be achieved, provided the Si surface morphology is adequately prepared [163]. The rear metal contact can be implemented locally, in dots or lines, together with a BSF, or without it. In the second case, attention should be paid so that contact resistance is maintained in reasonable levels.

Since this concept has been implemented to produce high-efficiency laboratory solar cells [164], efforts have been made to transfer this technology to industry, with the focus on throughput. Layers such as SiO_x [165], Al oxide [166], Si oxynitride [167] and SiC [168] are the best potential candidates. A-Si:H has been also applied as rear side passivating layer [169], but its full potential is exploited in the heterojunction structure, as discussed in Sec.4.

Care must be taken with the potential loss of passivation due to the subsequent metallization, as high-temperature steps can degrade the passivating properties of the layers [170,171]. Another issue is the possibility of shunting by interaction between the layer and the metallization due to the existence of charges in the layer, as is the case of SiN layers [172].

With proper process optimization, or by combining several layers in stacks, the low effective rear surface recombination velocities, in the range of few cm/s, have been successfully obtained in solar cells to improve efficiency [173-177]. A clear proof of the gain obtained with the rear surface passivation can be seen in the internal quantum efficiency (IQE) curve in an example taken from Ref. [145], and shown in Fig. 2.16.



1099

1100 Fig. 16 Comparison of internal quantum efficiency and reflectance between cells with different rear passivation
1101 stacks, Al_2O_3/SiN and SiO_2/SiN, as compared to a full-area Al-BSF reference cell [145]. With permission from
1102 Thorsten Dullweber, Sebastian Gatz, Helge Hannebauer, Tom Falcon, Rene Hesse, Jan Schmidt, Rolf Brendel,
1103 Towards 20% efficient large-area screen-printed rear-passivated Si solar cells, Prog. in Photov: Res. Appl., **20**
1104 (2011) 630. Copyright © 2011 John Wiley & Sons, Ltd. License number 3457590457465.
1105

1106 2.6 Future outlook

1107 Efficiency of traditional c-Si solar cells has increased relatively significantly since
1108 their invention in the mid-twentieth century. To a great extent this has been due to several
1109 improvements related to larger photon and charge carrier collection, improved
1110 photoconversion processes, and shadowing reduction, as has been mentioned in previous
1111 sections. Consequently, the current efficiency for commercial c-Si solar cells is quite close to
1112 the world records obtained in lab. Due to the mass scale adaption of laboratory techniques in
1113 the industry, such as buried contacts, selective emitters, etc., in recent years the cost of these
1114 new techniques has been lowered sharply. One of the most important challenges of the c-Si
1115 technology is to increase short-circuit current density (J_{sc}), using low-cost manufacturing
1116 processes. Currently, the results obtained applying the RIE process are very promising, and
1117 its inclusion in the commercial production lines may be explored in to increase the J_{sc} values.
1118 Other improvements, such as the introduction of back reflectors, can be implemented with the
1119 current state-of-art of the metallization techniques such as evaporation. The main challenge

1120 for this technique is to become as cost-competitive as screen printing. Multilayers are also an
1121 attractive option for improving the J_{sc} values, especially as the price of the PECVD systems
1122 dropped in recent years. In order to improve the open-circuit voltage (V_{oc}) of the solar cells,
1123 ion implantation is one of the most interesting techniques to obtain more repeatable profiles.
1124 Also, it is possible to obtain higher accuracy in the doping profile, and also improve the
1125 current selective emitter formation procedure. However, due to Si material properties, V_{oc} for
1126 a single-junction solar cell is now very close to the theoretical limit. Further incremental
1127 improvements in V_{oc} require investments in sophisticated fabrication/manufacturing
1128 techniques, which will increase the cost. Finally, to reduce shadowing losses new pastes and
1129 materials have been tested in laboratories in recent years, which show remarkable results in
1130 terms of electrical performance improvements. Consequently, in the next 5 years narrower
1131 and thinner metallic contacts in the solar cells will be commercially applied to c-Si solar
1132 cells. These new materials will reduce shadowing and, at the same time, result in low series
1133 resistance. On a side note, the main challenge in solar cell is to reduce surface/bulk defects to
1134 achieve low emitter saturation current density.

1135 Conventional front junction cells also continue to make rapid advances. Many
1136 alternatives to front junction solar cells with front and rear contacts are being promoted, and
1137 the traditional structure has demonstrated strong potential to reduce costs. Over the last
1138 several years, impressive improvements have been achieved thanks to a successful transfer to
1139 industry of some of the concepts being pursued by the research community. These have
1140 included the use of lower cost feedstock, cheaper ingots and wafers, development of low-cost
1141 dopant and metallization schemes, and implementation of selective emitters and rear
1142 passivating stacks. These achievements have brought the cost of c-Si PV modules well below
1143 $1/Wp (excluding balance of systems), a reduction of around 75% in ten years. There is
1144 however still room for further improvement of front junction solar cells towards the

$0.50/Wp range, thanks to technology improvements and economies of scale. In a tough competitive environment, those concepts combining the lowest costs with the highest improvements in efficiency will become dominant.

3.0 c-Si based solar cells: Back junction

The major advantage of the interdigitated back contact (IBC) c-Si solar cells is the absence of front side metallization grid, since both p-type and n-type metal electrodes for emitter and base respectively are located on the rear side of the solar cell. Due to the absence of front side metallization grid, IBC cells exhibit zero-shading losses, which results in strongly increased J_{sc}. Moreover, the front surface can be optimized for optimum light trapping and surface passivation properties, without having to allow for the low contact resistance. This way the front surface recombination can be reduced and light trapping improved. Furthermore, the series resistance losses of the metallization grid can be reduced, because both electrodes are on the back side where the width and thickness of the metallization grid is not limited by the shading losses. All of these positive effects result in a relatively very high-efficiency potential of this type of c-Si solar cell.

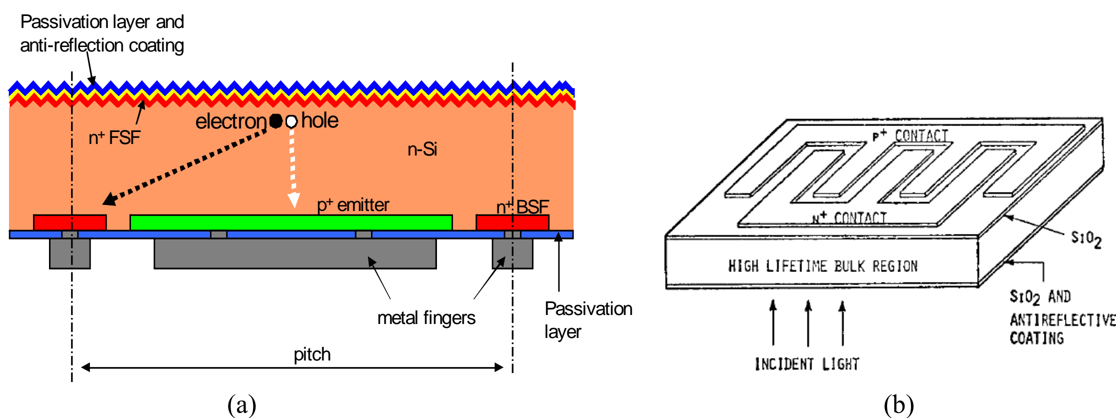
3.1 Introduction

The schematic diagram of IBC back junction solar cell is shown in Fig. 17. A remarkable example of the high-efficiency potential of this cell structure are the IBC cells developed by the SunPower Corp., with the highest reported efficiency for the large-area (155.1 cm^2 n-type Cz c-Si) IBC solar cell of 24.2% [178], and module based on IBC cells with efficiency over 20% [179]. The decrease in module efficiency is attributed to the fact that (i) the module area is not fully covered with solar cells (i.e. there is inactive area), (ii) the encapsulation foils and glass sheet in module introduce additional optical losses, and (iii) finally the interconnections of the individual solar cells in the PV modules cause some resistive losses.

1171 The IBC cell structure also offers advantages for the module manufacturing. Both
1172 electrodes on the rear side allow for the potentially easier and fully automated co-planar
1173 interconnection of the back-contact solar cells in the module assembly process. The issue of
1174 the module technology for the interconnection of the IBC cells is under investigation and
1175 should allow for further reduction of the PV modules based on the IBC cells structure [180-
1176 182]. Also, the attractive and uniform appearance of the finished IBC modules should be
1177 noted, as it is especially of importance in the field of building integrated photovoltaics
1178 (BIPV).

1179 The operating principle of the IBC c-Si solar cell is shown in Fig. 17 (a), and the
1180 examples of the photographs of the IBC solar cells are shown in Fig. 18. The incoming
1181 photons generate electron-hole pairs. Most of the absorption takes place close to the front
1182 surface of the IBC solar cell, resulting in a charge carrier (electrons and holes) concentration
1183 gradient through the c-Si bulk. The concentration gradient of the carriers results in the
1184 diffusion transport towards the rear side, where the p-n junction is located and carriers are
1185 collected by their respective electrodes. The p-n junction on the rear side may have a point-
1186 like structure, or a line structure with the respective width. The distance between two metal
1187 contacts of the same polarity is called pitch.

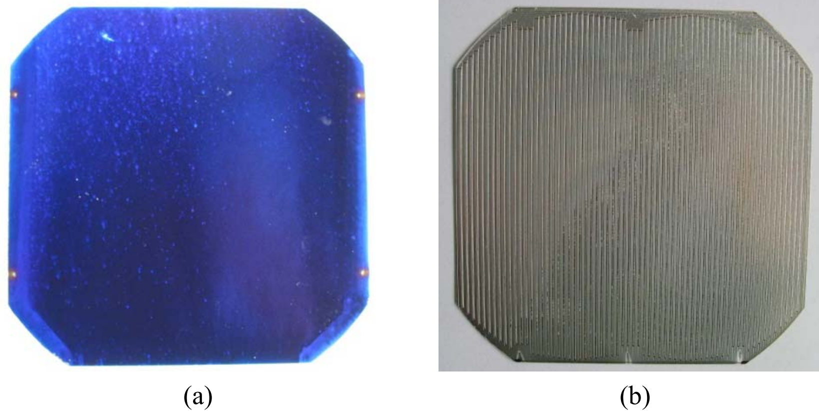
1188

1189 

1190 (a) (b)

1191 Fig. 17 (a) Schematic cross-section of an n-type high-efficiency IBC c-Si solar cell having p-n junction at the
1192 rear side, (b) schematic angle view of the IBC cell introduced by Lammert and Schwartz [183]. To avoid
1193 minority-carrier recombination at the rear side and to enhance the minority-carrier collection probability, emitter
1194 size is kept larger than the BSF size. Front surface field blocks minority carriers reaching the front surface. The

1195 drawings are not to scale. From [183], M.D. Lammert and R.J. Schwartz, “The interdigitated back contact solar
1196 cell: a silicon solar cell for use in concentrated sunlight”, IEEE Transactions on Electron Devices, ED **24** (1977)
1197 337-42. Copyright © 1977, IEEE. Permission granted. License number 3582481103872.



1198
1199 (a) (b)

1200 Fig. 18 Photographs of the (a) grid-less front side, and (b) rear side of the large area IBC solar cells developed in
1201 the course of the Quebec project at Fraunhofer ISE, without the use of photolithography [184]. Solar cell area is
1202 147.4 cm^2. Both p-type and n-type contacts are formed at the rear side of the c-Si wafer. Light enters from grid-
1203 less front side of c-Si wafer. Photogenerated carriers created at the front side travel across the bulk of the wafer
1204 due to concentrated gradient. Since electric field is present at the rear side across the p-n junction, these carriers
1205 are collected by their respective electrodes. From [184], F. Granek, Ph.D thesis, “High-efficiency Back-Contact
1206 Back-Junction Silicon Solar Cells”, Verlag Dr. Hut, ISBN 978-3-86853-348-4 (2009). Permission granted.

1207
1208 Historically, the concept of the IBC cells was introduced in 1977 by Lammert and
1209 Schwartz. Initially the IBC cells were developed for the operation under high level of
1210 sunlight concentration. The research group led by R.Swanson at Stanford University and at
1211 the SunPower Corp., founded by R. Swanson paved the way for the remarkable development
1212 of IBC cell physics, design, and technology [178,179,185-190]. Currently many research
1213 groups and industrial laboratories are investigating the IBC cell concept due to its inherent
1214 high-efficiency potential, with the goal to reduce the costs of the c-Si PV modules.

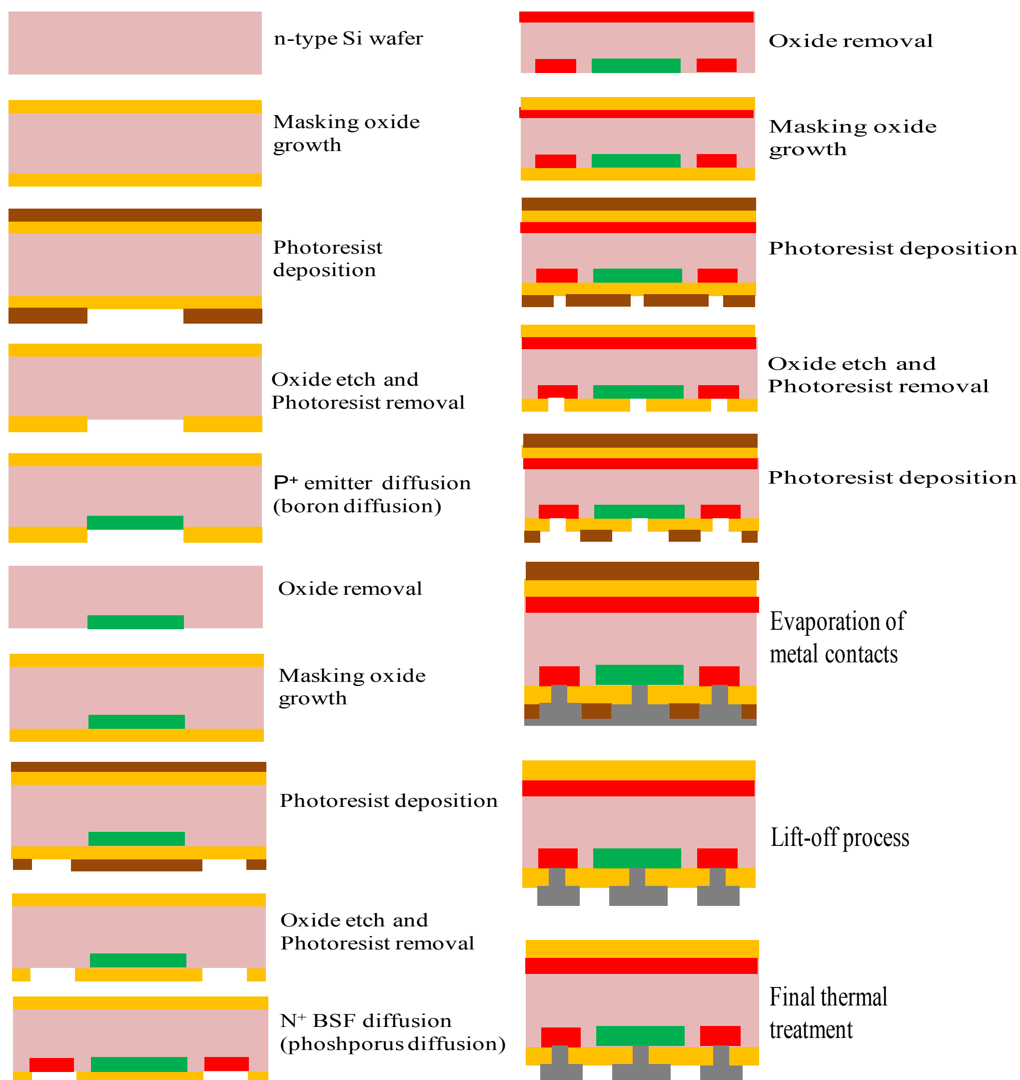
1215 The other two categories of the c-Si back contact solar cells are the MWT cells [191-
1216 193], in which the front surface collecting junction and the front metallization grid are
1217 connected to the interconnection pads on the back surface via laser-drilled holes (Fig.9), and
1218 the EWT cells [194-198], in which the front surface collecting junction is connected to the
1219 interdigitated contacts on the back surface via laser-drilled holes (Fig. 10). The MWT and
1220 EWT cell structures are covered in Sec. 2.4. The interested reader is referred to [199] and to
1221 the above listed references for more details.

1222 ## 3.2 Challenges related to c-Si back junction solar cells

1223 One of the main challenges to the spread of IBC solar cells into mass production is the
1224 complexity of the processing technology. Processing of major rear side features of IBC cells
1225 such as: (i) emitter and BSF doping areas, (ii) contact openings in the passivation layer, and
1226 (iii) the metallization grid, requires four to six masking steps. Laboratory development
1227 usually includes application of the photolithography process, as shown in Fig.19, for
1228 structuring of the rear side of the IBC cells.

1229

1230

1231 

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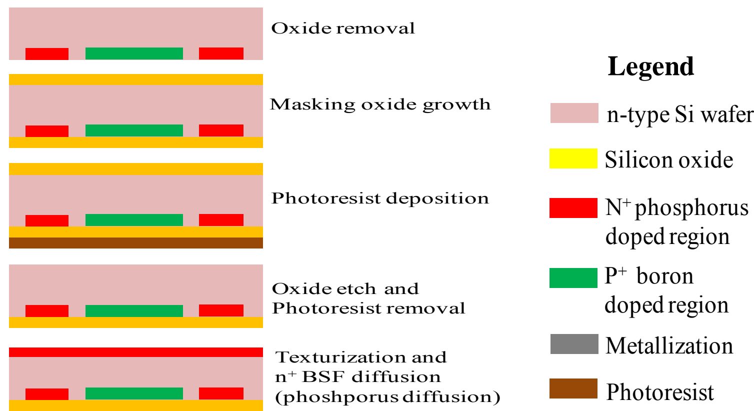


1233
1234
1235 Fig. 19 Possible example of a complex laboratory scale process flow for the IBC solar cell processing using
1236 photolithography and high-temperature diffusion processes. The sequence for fabrication is first the left column
1237 and later the right column. Highly pure, lightly doped Fz c-Si wafers with diffusion length at leaset 4 times
1238 higher than the wafer thickness, and life-time of 1-3 msec are required. High accuracy masking steps are
1239 required to avoid shunting between p-type and n-type electrodes. Instead of expensive photolithography process,
1240 laser processing and screen-printing are used to obtain high-throughput.

1241

1242 Photolithography is however not a cost-effective process for mass production in the
1243 photovoltaic industry. The processing sequence of the IBC cells is therefore much more
1244 complex than conventional c-Si solar cells, which results in increased manufacturing costs.
1245 There exists the need for simplified processing schemes, where costly photolithography
1246 process is replaced with low-cost and high-throughput structuring schemes using laser
1247 processing and screen-printing, etc. However since there exists a risk of fatal shunting
1248 between the p- and n-type electrodes due to errors in the masking processes, requirements of
1249 high positioning accuracy and resolution are imposed on the masking steps. In addition to the
1250 complexity of the processing technology, IBC require high quality of c-Si wafer and the high-
1251 quality passivation of the wafer surfaces.

1252 The above issues of processing complexity and c-Si material requirements are of
1253 major importance and are therefore discussed in detail in the following sections.

1254 3.3 Requirements for front surface passivation and bulk minority-1255 carrier lifetime

1256

1257 Due to absorption properties of c-Si, most of the photogeneration occurs at the front
1258 side of the cell (Fig. 17a). At the same time, in the IBC cell structure, the collecting p-n
1259 junction is located on the back side. Due to concentration gradient across the bulk,
1260 photogenerated charge carriers travel from front side to rear side and are collected by their
1261 respective electrodes. For poorly passivated front surface, photogenerated minority-carriers
1262 can be easily lost by recombining at the front surface instead of reaching the back junction.
1263 Moreover, even if the front surface is well passivated, a risk of recombination within the bulk
1264 c-Si exists. The carriers which need to diffuse through the wafer thickness can recombine in
1265 bulk c-Si before reaching the back junction if the bulk lifetime of the minority-carriers is
1266 insufficient. Therefore, minority-carrier lifetime in bulk (τ_{bulk}) and front SRV are the two
1267 most critical parameters in the IBC solar cell structure. The importance of these two critical
1268 parameters is shown in Fig. 20. The starting Si material needs to be of high quality (the
1269 minority-carrier lifetime should be in the range of 1-3ms) and its quality needs to be
1270 maintained during the whole solar cell processing sequence in order to reach high-
1271 efficiencies. The rule-of-thumb is that the diffusion length of the minority-carriers in c-Si
1272 needs to be at least four times higher than the thickness of the c-Si wafer in the IBC solar
1273 cells, to allow for efficiencies above 21-22%. This means that τ_{bulk} needs to be in the range of
1274 milliseconds. Simultaneously the front SRV needs to be kept extremely low in the finished
1275 device in order to enable high-efficiencies. The effective front SRV should be kept below
1276 10cm/s.

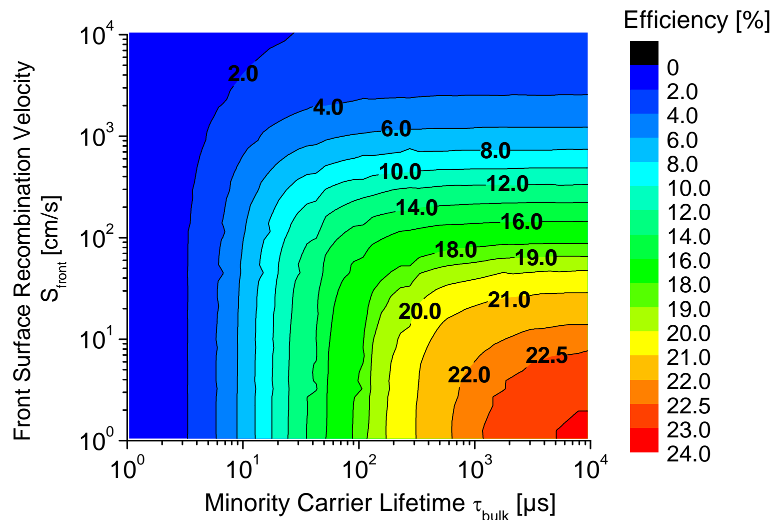


Fig. 20 Example of numerical simulations of the efficiency of a back junction solar cell structure as a function of bulk life-time and front surface recombination velocity. Front surface recombination velocity and diffusion length of minority-carriers are the ultimate parameters controlling the efficiency. For high-efficiency, effective front surface recombination velocity should be less than 10cm/s. Simulations were done using PC1D [200] program (graph adopted from [184]). From [184], F. Granek, Ph.D thesis, “High-efficiency Back-Contact Back-Junction Silicon Solar Cells”, Verlag Dr. Hut, ISBN 978-3-86853-348-4 (2009). Permission granted.

3.3.1 Minority-carrier lifetime considerations

The extremely high requirements for the minority-carrier lifetime can be in practice met only by an n-type Si as base material. In p-type boron-doped oxygen-contaminated c-Si, minority-carrier lifetime is strongly reduced under illumination or carrier injection [201, 202]. Due to the lack of boron in n-type Si, no degradation occurs. Also, n-type c-Si exhibits lower sensitivity to the impurities as interstitial Fe [203]. Many laboratories are developing front junction and rear junction solar cells based on n-type c-Si [137, 204-209**]**, and commercially available solar cells with the highest-efficiency are produced on n-type c-Si wafers [178]. The drive for low-cost in the PV world requires however that the Si wafers need to be manufactured using industrially relevant manufacturing methods. In reality only phosphorus doped n-type wafers cut from Cz-grown ingots meet these requirements [28, 210]. The lifetime of the minority-carriers in n-type c-Si is significantly higher than in the case of p-type c-Si. For example, extremely high minority-carrier lifetime in the range of milliseconds was reported for n-type mc-Si by Cuevas et al. [211].

3.3.2 Front surface passivation considerations

1301
1302 High quality of front surface passivation can be achieved by the application of
1303 dielectric passivation layers such a thin thermal SiO_2 layer covered by the PECVD SiN ARCs
1304 [212]. However, the front surface passivation is usually additionally improved by the
1305 additional phosphorus doping layer on the front side. This is called front surface field (FSF)
1306 and its role is to reduce the concentration of the minority charge carrier close to the wafer
1307 surface, and thus reduce the effective recombination velocity [213,214]. The methodology for
1308 numerical optimization of the doping profile of the FSF for the passivation purposes was
1309 presented by del Alamo and Swanson [215]. The application of the FSF has also additional
1310 important positive impacts on the IBC cell performance. FSF improves long-term stability of
1311 the front surface passivation under UV illumination [212]. It also improves the current
1312 linearity of the IBC cells at low light intensities, thus improving the efficiency at the low-
1313 illumination intensities [216]. An FSF layer is also seen to significantly improve lateral
1314 current transport by reducing the lateral base series resistance losses [217].

1315 3.4 Approaches to minimize losses related to the rear side 1316 structure

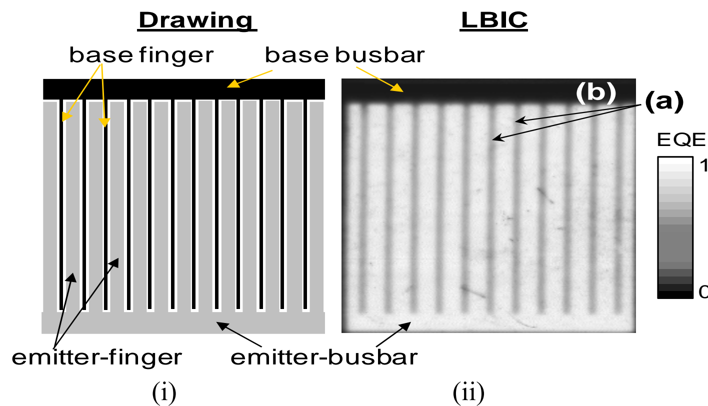
1317 The next main challenge in achieving very high conversion efficiencies in IBC cells is
1318 in the rear side structure. Introduction of the complex doping grid of the interdigitated emitter
1319 and base areas on the rear side is not only technologically challenging, but also accompanies
1320 some additional risks to achieving high-efficiencies. The recent study of Kluska et al. [218]
1321 investigates systematically the loss mechanisms on the high-efficiency IBC solar cells. Next
1322 to the front surface and bulk recombination of the minority-carriers, this study describes free
1323 carrier absorption and electrical shading as the critical loss mechanisms.

1324 In the free carrier absorption process [219,220], the incident photon's energy is
1325 absorbed by free carriers. This is a parasitic absorption (optical absorption that does not
1326 produce e-h pair is known as parasitic absorption) process, leading to a reduction of the

1327 photogenerated current. The free carrier absorption process is significant only in the highly
1328 doped c-Si wafers. A careful optimization of the doping profiles of the emitter and BSF
1329 regions is therefore a must when reducing the free carrier absorption losses and at the same
1330 time minimizing the rear surface recombination losses [221].

1331 Electrical shading losses are recombination losses of the minority-carriers at the rear
1332 side areas not covered by the emitter (shown schematically in Fig. 21). Electrical shading
1333 losses have a significant impact on the efficiency of the IBC solar cells. Therefore careful
1334 optimization of the rear side geometry, doping profiles, and rear surface passivation quality
1335 are crucial in order to achieve high-efficiency [221-224].

1336

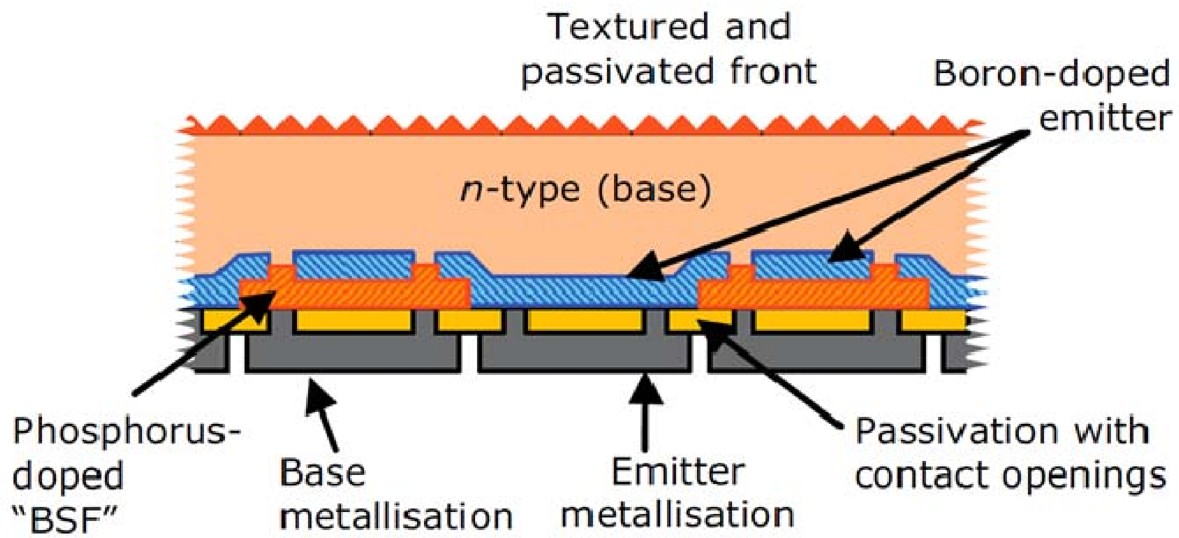


1337
1338 (i) (ii)

1339 Fig. 21 Sketch of the (i) rear side, and (ii) light beam induced current (LBIC) map of the laboratory scale
1340 (2x2cm²) IBC c-Si solar cell. The reduced signals above the base fingers and the base busbar due to electrical
1341 shading are clearly visible [222]. Here, (a) and (b) refers to base finger and base bus bar. Cell efficiency is
1342 affected by electrical shading (losses) at the rear side. Doping profile and pitch size at the rear side should be
1343 optimized for high-efficiency. With permission from [222], M. Hermle, F. Granek, O. Schultz-Wittmann, S. W.
1344 Glunz, "Shading Effects in Back-Junction Back-Contacted Silicon Solar Cells", 33rd IEEE Photovoltaic
1345 Specialist Conference, San Diego, CA (2008). Copyright © 2008, IEEE. Permission granted. License number
1346 3582490239489.

1347 In order to reduce the electrical shading losses, other approaches emerged recently to
1348 drastically reduce the rear side surface related losses apart from the optimization of the rear
1349 side emitter and BSF doping profiles in the classical IBC cell structure. These approaches are
1350 based on decoupling the geometries for the minority-carrier collection and metallization.
1351 They should allow for nearly complete elimination of the electrical shading losses. A
1352 prominent example of such approaches include buried emitter IBC solar cell [221, 225, 226],

1353 which introduces a local overcompensation of the emitter by the BSF doping and drastically
1354 improves the emitter coverage on the rear side seen from the front surface side (see Fig. 22
1355 for explanation of the buried emitter structure). Another example involves decoupling
1356 emitter from metallization geometry by the application of the insulating thin-films, which can
1357 lead to efficiencies up to 23% [227,228].



1358

1359 Fig. 22 Cross sectional view of the buried emitter back junction solar cell. When looking from the top of the
1360 solar cell, the boron emitter is extended over almost the entire rear side of the solar cell. This allows for efficient
1361 collection of minority-carriers at the rear side. At the same time the emitter regions are electrically insulated
1362 from the base metallization by BSF layer, which prevents shunts between base metallization and emitter doping
1363 [225, 229]. Burried emitter structure allows for using similar area fractions for base and emitter metallization,
1364 without the need for any dielectric insulation. Reprinted with permission from [225], N.-P. Harder, V. Mertens,
1365 and R. Brendel, Buried emitter solar cell structures: Decoupling of metallisation geometry and carrier collection
1366 geometry of back contacted solar cells, phys. stat. sol (RRL), **2** (2008) 148. Copyright © 2008 published by
1367 John Wiley & Sons. Permission granted. License number 3582490855869

1368

1369 3.5 Current developments for the low-cost IBC solar cell 1370 processing

1371

1372 Currently the focus in the processing of the IBC cells is on simplifications of the
1373 process flow, and overall cost reduction. The examples below show selected approaches to
1374 reduce the processing complexity, and cost of the IBC cells.

1375 3.5.1 Ion-implantation

1376

1377 Due to its directional character, the ion-implantation process allows for one-step
1378 patterning of the doped regions. This means that in the ion-implantation process only one

1379 single surface of the wafer is modified. Thus, unlike in the high-temperature diffusion
1380 process, there is no need to carefully protect the other (non-modified) surface during the
1381 implantation step. This feature of ion implantation can potentially allow for major
1382 simplifications in the processing of the complex rear side structure of the IBC cells.
1383 Moreover, a single high-temperature annealing process, at the final stage of the IBC cell
1384 processing, can deliver growth of the front and rear side Si oxide passivation layer and anneal
1385 multiple doping processes. A possible process flow to manufacture high-efficiency IBC cells
1386 with ion implantation is shown in Fig. 23. An ion-implantation application to the production
1387 of high-efficiency IBC cells is under development by various industrial and research groups
1388 [140, 230, 231]. In this example the front side oxide is removed (process step: oxide etch
1389 front) in order to grow a thin passivation oxide on the front surface, for the subsequent ARC
1390 SiN.

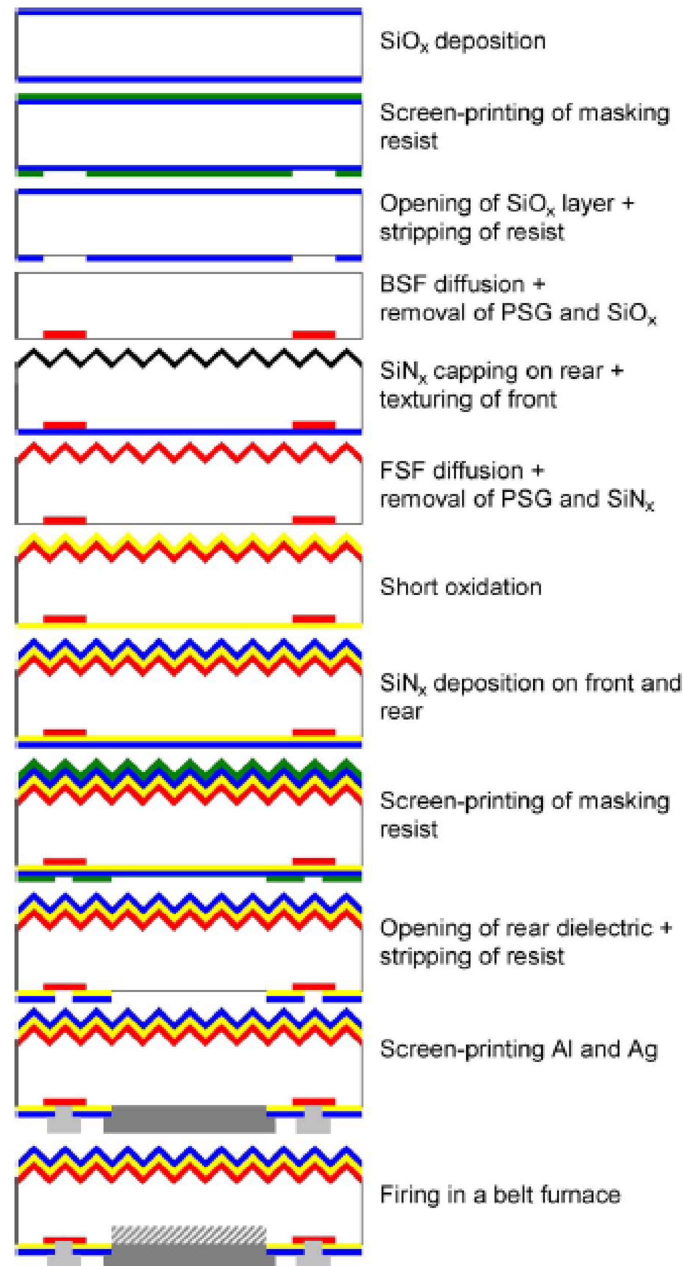
1391
1392
1393 Fig. 23 Example of a process flow used for processing of ion implanted IBC cells [230]. Ion implantation
1394 process allows one-step patterning of doped areas. Processing steps can be simplified by using ion implantation
1395 process. Multiple dopants can be annealed in a single annealing process. With permission from [230], N.
1396 Bateman, P. Sullivan, C. Reichel, J. Benick, M. Hermle, "High quality ion implanted boron emitters in an
1397 interdigitated back contact solar cell with 20% efficiency", Energy Procedia 8 (2011) 509. Copyright © 2011
1398 Published by Elsevier Ltd. Permission granted. License number 3584831043918.
1399

1400 3.5.2 IBC c-Si back heterojunction solar cells

1401
1402 Heterojunctions are known for their excellent surface passivation properties. Their
1403 application to the IBC solar cells can therefore improve the open circuit voltages
1404 significantly. At the same time, the deposition of the a-Si:H layers can be done through a
1405 mask at low-temperatures, which offers a potential of reduction of the complexity of the IBC
1406 cell process flow [232-234]. Si based back heterojunction solar cells are presented in Sec.5.

1407 ### 3.5.3 Epitaxial doping layers
1408
1409 Another opportunity for the simplification of the processing flow for the IBC cells is
1410 the epitaxy for the formation of the highly doped regions. Epitaxy is the method of deposition
1411 of the respective material on a crystalline wafer, in which the deposited material maintains
1412 the crystallographic orientation of the crystalline wafer. The technological process of epitaxy
1413 allows for the precise formation of the doping profiles, which are not possible to achieve with
1414 the traditional high-temperature diffusion process. A study by Baker-Finch and Basore [235]
1415 demonstrated the potential of the epitaxy process in the formation of the front surface field
1416 layer in the IBC cells.

1417 ### 3.5.4 Laser processing and screen-printing for low-cost structuring of IBC
1418 cells
1419
1420 The masking steps to process IBC cells are often performed using photolithography,
1421 which is costly and thus not applicable for mass production of IBC cells. Low-cost and high-
1422 throughput alternatives to photolithography are being developed and applied in the
1423 processing of IBC cells. These structuring alternatives include laser processing and screen-
1424 printing processes. Engelhart et al. demonstrated IBC cells with efficiency of 22% with
1425 application of laser structuring [196]. Granek et al. applied screen-printed processes for
1426 masking of the IBC cells to reach 21.3% efficiency [217]. Examples of the low-cost IBC cell
1427 processes with the focus on applying the screen-printed metallization on IBC cells were
1428 developed by Halm et al. [236], Castano et al. [237], Galbiati et al. [238], and Lamers et al.
1429 [239]. Wohl et al. [240, 241] developed an industrially feasible IBC process with the Al
1430 alloyed emitter, to eliminate the boron diffusion process. This process flow is shown in Fig.
1431 24.



1432

1433 Fig. 24 Process sequence for all-screen-printed IBC cell with Al alloyed emitter on an n-type wafer [240].
1434 Instead of diffused (boron) emitter process, p^+-Al alloyed emitter is formed during the firing process of the Al
1435 paste. Contact metals are formed by screen-printing Al and Ag. Reprinted with permission from [240], R.
1436 Woehl, J. Krause, F. Granek, D. Biro, 19.7% efficient all-screen-printed back-contact back-junction silicon solar
1437 cell with aluminum-alloyed emitter, IEEE Electron. Dev. Lett., **32** (2011) 345. Copyright © 2011, IEEE.
1438 Permission granted. License number 3582500441017.

1439

1440 **3.5.5 Formation of the interdigitated metallization grid**

1441

1442 The formation of the interdigitated metallization grid is often achieved using
1443 photolithography masking and thermal evaporation of the metal layers. However, as

mentioned earlier, photolithography is not cost-effective for solar cell production. Different methods to create interdigitated metallization grid from the full area deposited (e.g. by the means of thermal evaporation or sputtering) metal layer are under evaluation. These include: (i) bi-level metallization scheme proposed by Sinton et al. [242] and currently under development by De Vecchia et al. [243], (ii) self-aligned metallization scheme proposed by Sinton in 1988 [186], (iii) laser ablation of the masking layer and etching of the bulk metal [244], (iv) local etching of the metal layers through screen-printed masks [184], and (v) lift-off and laser assisted lift-off using screen-printed layers [184]. There exist another approach to metallization, namely direct plating of metal on the rear cell surface, which has been investigated for the front side metallization of the standard c-Si solar cells [245].

Broadly, research advances in this field have not been reported widely so far, which indicated a potential for further cost reduction and process flow simplifications in the processing of c-Si IBC solar cells.

3.6 Future outlook

Recetly Panasonic and Sharp [246,247] research laboratories have reported efficiencies of over 25 % at the laboratory scale for IBC solar cells, and the milestone of 26 % efficiency seems to be practically achievable with the single-junction c-Si IBC cell. These groups combine an IBC cell structure with high level of surface passivation for the metal contact regions using a heterojunction of a-Si:H/c-Si interfaces. Currently recombination losses at the metallized areas are one of the dominant recombination mechanisms in high-efficiency IBC cells. Therefore research efforts are currently focused on the introduction of industrially feasible passivated contact concepts with the goal of drastically reducing minority-carrier recombination rate at the metal contacts. One important area of recombination is at the edge. It is expected that in the future the best efficiencies of IBC cells would be reported on large solar cell surfaces, where the relative impact of the edges will be

low. The next significant modification to the IBC cell structure may be the application of a novel module interconnection technology based on patterned back-sheet foil [181]. Such interconnection will allow for eliminating the necessity of complicated metallization busbar and finger grids on the IBC cells side, and will allow for more design freedom for the solar cell engineers. This can potentially have a positive impact on the efficiency and packaging density of the solar cells in a module.

4. Crystalline Si based solar cells: Front heterojunction

A-Si:H/c-Si front heterojunction (hereafter called Si heterojunction or SHJ) solar cells are fabricated by deposition of a few nm thin intrinsic a-Si:H followed by doped a-Si:H onto (typically) c-Si wafers. Their working principle is very similar to conventional Si wafer cells with diffused junctions; it can be summarized briefly as follows (Fig. 25): The incident light generates electron-hole (e-h) pairs in the c-Si wafer. The minority charge carriers are collected on the cell's front side by the Si heterojunction, and are laterally transported towards the metal front grid through a thin transparent conducting oxide (TCO) layer that also acts as an anti-reflection coating. Majority charge carriers are collected by the BSF, which is also formed by an a-Si:H/c-Si heterojunction. The rear side contact is completed by a full area metallization. Often, another TCO layer is inserted between the a-Si:H and metal on the back side to improve the optical properties of the cell in the infrared part of the spectrum.

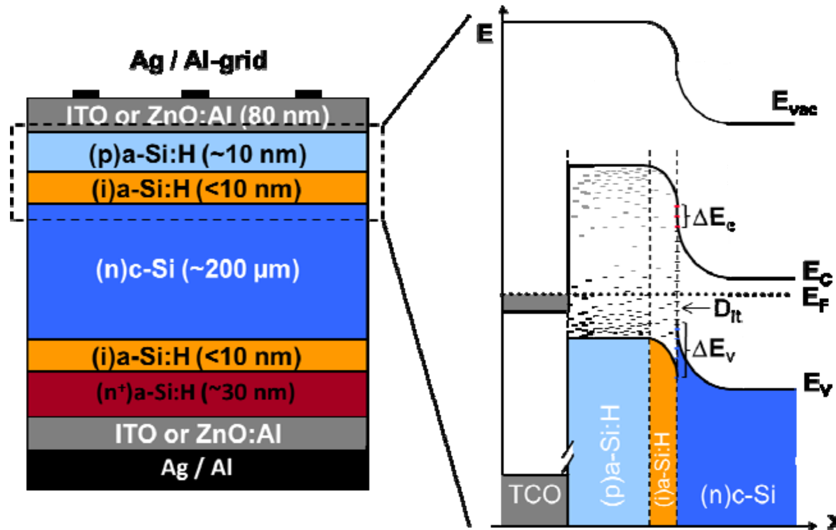
4.1 Introduction

Si heterojunction device architecture enables very high energy conversion efficiencies of 24.7% on industrially relevant cell sizes (>100cm²) [248] and above 21% (>18% module efficiency) in industrial production [249]. The key feature of this technology is that the metal contacts, where the recombination velocity is high in traditional diffused-junction cells, are

1495 spatially and electronically separated from the absorber by insertion of a wider bandgap a-
1496 Si:H layer. This general idea was introduced by Fuhs et al. in the 1970s using a direct
1497 heterojunction between doped a-Si:H and c-Si [250] and augmented by the company
1498 Sanyo in the 1990s with the introduction of a low-defect intrinsic a-Si:H buffer layer between
1499 the doped a-Si:H and the c-Si wafer [251]. It enables V_{oc}s above 700 mV. Furthermore, the
1500 cell process is based on comparatively simple full-area deposition steps and screen-printed
1501 contacts, whereas in conventional c-Si cells with diffused emitters, efficiencies well above
1502 20% can only be reached using local contacting schemes, which require expensive patterning
1503 techniques. Additionally, since all process steps occur at temperatures around or below
1504 200°C, the cell has a low thermal budget [252]. In contrast to conventional diffusion
1505 processes that lead to wafer bowing and increased breakage, the SHJ process is compatible
1506 with very thin wafers (the 24.7% cell was fabricated on a 98 µm thin wafer) or Si absorbers
1507 on glass with a thickness of few µm, which have indeed lately shown promising V_{oc}s and
1508 efficiencies of up to 656mV and 11.8%, respectively [253, 254].

1509 Many aspects of the SHJ device concept will be discussed only briefly in the
1510 following. For further reading, an extensive review article on SHJ solar cells published by de
1511 Wolf et al. [255], and a monograph [256] on the same subject are recommended.

1512 ## 4.2 c-Si based front heterojunction cell design – an overview



1513

1514 Fig. 25 Schematic cross-section and energy band diagram of a p-type a-Si:H/intrinsic a-Si:H/n-type c-Si
1515 heterojunction solar cell. The intrinsic a-Si:H acts as pasivation layer between c-Si (absorber) and recombination
1516 active metal (or TCO) contacts. Both p-n junction and BSF are formed by a-Si:H/c-Si heterojunctions. E_C, E_V
1517 are the band edges, ΔE_C, ΔE_V the band offsets between the intrinsic a-Si:H and the c-Si, E_F the Fermi level and
1518 D_{it} the density of defect states at the intrinsic a-Si:H/c-Si interface. Note the asymmetry of the band offset: ΔE_v
1519 is much larger than ΔE_c. For clarity, texturization of the wafer is not shown.

1520

1521 In SHJ cells, a-Si:H/c-Si heterojunctions are used to form the p-n junction and BSF of
1522 the cell. Figure 25 shows a simplified sketch of this cell type, including the intrinsic buffer
1523 layers, together with a schematic band diagram. Note that the usual texturization of the wafer
1524 has been omitted for clarity. As already mentioned above, the Si heterojunction is the solution
1525 to the conflicting requirements to (i) passivate electronically the surfaces of the c-Si absorber,
1526 where charge carriers are photogenerated, in order to obtain a large splitting of the quasi
1527 Fermi levels and thereby a high V_{oc}, and to (ii) extract the photogenerated charge carriers
1528 efficiently through the same surfaces, yielding a low series resistance/high fill-factor. In the
1529 SHJ concept, this problem is solved by inserting a passivating, semiconducting film between
1530 the absorber and the highly recombination active metal (or TCO, see below) contacts. This
1531 passivating a-Si:H film, in turn, is usually divided into two parts, i.e. the passivation layer
1532 proper, consisting of low-defect not intentionally doped (intrinsic) a-Si:H and a doped, more
1533 defective a-Si:H layer that induces the appropriate band bending to form the p-n junction or

1534 the BSF. Electrical contacts to the cell are then formed using TCOs and a metallization layer
1535 (grid/full-area).
1536 The main differences between semiconductors in the Si heterojunction cell and the equivalent
1537 homojunction cell are:
1538 **(i) Abrupt interfaces:** In contrast to the usual diffused emitter and BSFs, the Si
1539 heterojunction is abrupt on the monolayer length scale. Thus the doping profile usually is a
1540 step function. Similarly, it is believed that the second heterojunction in the cell, the TCO/n-
1541 a-Si:H junction, should also be as abrupt as possible.
1542 **(ii) Defect states in the a-Si:H bandgap and at the a-Si:H/c-Si interface:** These are an
1543 intrinsic property of overconstrained semiconducting glasses in general [257]. They consist of
1544 the so-called Urbach tails, i.e. exponential distributions of electronic states reaching from the
1545 band edges into the bandgap of the material, and of unsaturated, dangling Si bonds deep in
1546 the bandgap, which can be saturated by the hydrogen present in the a-Si:H film. At the
1547 a-Si:H/c-Si interface, surface contamination by atoms or molecules adsorbed to the c-Si
1548 wafer surface prior to a-Si:H deposition can lead to additional extrinsic defect states at the
1549 interface. Controlling surface contamination and the initial stages of a-Si:H growth are
1550 therefore key issues to obtaining low defect density a-Si:H/c-Si interfaces.
1551 **(iii) Band offsets:** The difference in E_g between c-Si (E_g ~ 1.12 eV at room temperature) and
1552 a-Si:H (E_g = 1.6-1.9 eV, depending on deposition conditions) gives rise to discontinuities in
1553 the valence and conduction band edges, usually denoted by ΔE_V and ΔE_C, respectively, see
1554 the schematic band diagram in Fig. 25. Band offsets also exist at the TCO/a-Si:H interface.
1555 For the contact layers, the differences to conventional homojunction cells are:
1556 **(iv) TCO:** Instead of the usual SiN ARC, SHJ cells use TCO, which provide both the ARC
1557 properties as well as a high lateral conductivity. This is necessary because even the
1558 conductivity of doped a-Si:H films is smaller by orders of magnitude. Thus, charge transport

1559 proceeds essentially perpendicular through the entire a-Si:H/c-Si/a-Si:H cell structure (Fig.
1560 25), then laterally through the TCO to the contact fingers.

1561 **(v) Metallization:** For industrially relevant cell processes, screen printing is widely used.
1562 Pastes for SHJ cells must yield good electrical properties for curing temperatures around
1563 200°C, which necessitates the use of a relatively high content of Ag. Lately, electroplated
1564 contacts have also been introduced successfully [258,259].

1565 Conceptually, the SHJ band offsets (i.e., band-edge misalignments) are the main
1566 difference to the p-n homojunction. They are an experimental approximation of the idea that
1567 contacts to a solar cell should act as a semi-permeable membrane through which charge
1568 carriers are extracted [260]. The unwanted charge carriers in the vicinity of a contact – i.e. the
1569 minority-carriers at the BSF, and the majority carriers at the p-n junction – are hindered by
1570 the band offsets in the heterojunctions and the low conductivity of the doped a-Si:H for the
1571 unwanted carrier polarity to reach the cell contacts, and thereby recombination at the contacts
1572 is effectively suppressed. Thus, a high separation of quasi-Fermi levels is obtained, and low
1573 reverse diode saturation currents and high V_{oc} can be expected in the cell. The advantage of
1574 having suitable band offsets at the contacts of a solar cell, similar to the case of
1575 heterostructure lasers, has been pointed out already in the 1980s, and their benefit to cell V_{oc}
1576 has been shown for the SiO_x/c-Si tunnel-heterojunction case, in the so-called semi-insulating
1577 polysilicon cell [261]. Another similar device is the metal-insulator-semiconductor cell [262],
1578 where a thin oxide layer acts as the semi-permeable membrane that has to be traversed, in this
1579 case by tunneling.

1580 4.3 c-Si wafers, surface texture and cleaning

1581 SHJ cells can be realized on both n- and p-type wafers, although the highest cell
1582 efficiencies have been demonstrated on n-type [263]. Typical doping levels are in the range
1583 also used for homojunction cells, 1-5 Ω-cm. In order to realize the high V_{oc} potential of SHJs,

a high minority charge carrier lifetime, i.e. low density of recombination-active defects in the wafer is needed. A bulk minority-carrier lifetime of several milliseconds for generation rates corresponding to air mass 1.5 (AM1.5) illumination is desired. Today, with improved crystal growth technology, this carrier lifetime range is readily achievable in low-cost Cz wafers.

As explained in Sec.2, the wafers are textured to improve light trapping, usually with a random pyramid texture, and thoroughly cleaned using the so-called RCA process developed as a standard cleaning process by the Radio Corporation of America [41] or a variant thereof. The native Si oxide layer grown in the last process is then usually removed by a short etch in diluted HF (1%, 1 min) immediately before the wafer is loaded into the PECVD system for a-Si:H deposition. Alternative pre-cleaning and oxide removal steps (chemical smoothing of wafer surface) have also been explored [264].

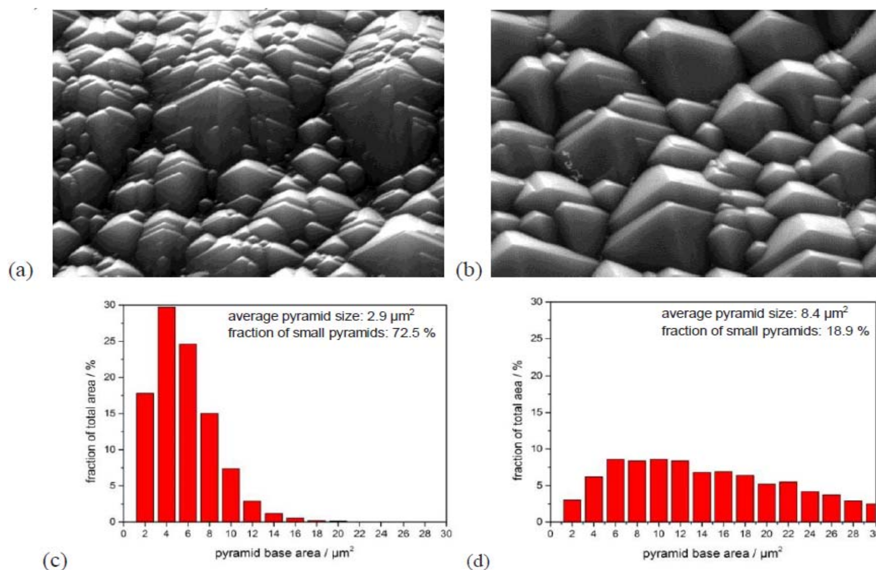
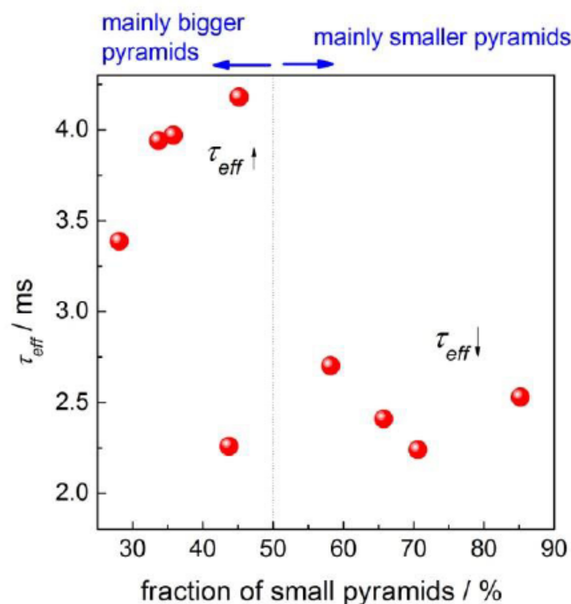


Fig. 26 SEM images of textured Si wafers: (a) after 5µm side damage etch removal and 20min texture etching time; (b) after 10µm side damage etch removal and 10min texture etching time. Scanning size of both images: 25µm × 19µm, tilt: 30°; (c and d) histograms of the statistical analysis of the corresponding pyramid sizes in the SEM images above. Data is obtained from at least 3 measurements at different positions on the sample. Reprinted with permission from [265], Bert Stegemann, Jan Kegel, Mathias Mews, Erhard Conrad, Lars Korte, Uta Stürzebecher, Heike Angermann "Passivation of Textured Si Wafers:Influence of Pyramid Size Distribution, a-Si:H Deposition Temperature, and Post-treatment." Energy Procedia, **38**(2013)881. Copyright © 2013 The Authors. Published by Elsevier Ltd. License number 3472391033286.

Recently, the influence of the random pyramid surface topology has been investigated in detail. Figure 26 shows that the morphology can be modified within a wide range to yield

1607 either mostly smaller pyramids or a broader distribution with predominantly large or very
1608 large ones. When passivated with a-Si:H, these surfaces behave very differently (Fig. 27).
1609 The effective minority charge carrier lifetime, a measure for the V_{oc} potential in cells
1610 produced with such passivation layers, increases strongly when the fraction of small
1611 pyramids is reduced [265]. It can be surmised that this behavior is related to the difficulty of
1612 growing well-passivating layers in the valleys and at edges of the pyramids [266]. With
1613 decreasing fraction of small pyramids, the line density of such valleys and ridges also
1614 decreases.



1615

1616 Fig. 27 Dependence of the effective carrier lifetime on the fraction of small pyramids. As can be seen, carrier
1617 lifetime increases when the fraction of small pyramids is reduced. This is probably due to the poor passivation
1618 quality in the valleys and edges of the pyramids. Reprinted with permission from [265], Bert Stegemann, Jan
1619 Kegel, Mathias Mews, Erhard Conrad, Lars Korte, Uta Stürzebecher, Heike Angermann "Passivation of
1620 Textured Si Wafers:Influence of Pyramid Size Distribution, a-Si:H Deposition Temperature, and Post-
1621 treatment." Energy Procedia, 38(2013)881. Copyright © 2013 The Authors. Published by Elsevier Ltd. License
1622 number 3472391033286.

1623 4.4 Hydrogenated amorphous Si

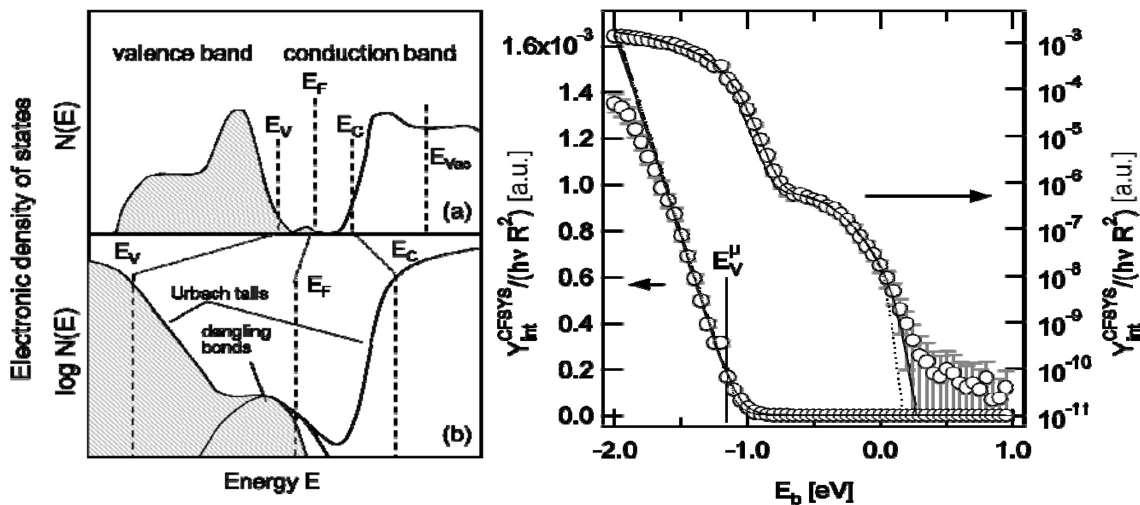
1624 As sketched in Fig.25, the emitter and BSF contacts of SHJ solar cells consist of
1625 doped and intrinsic a-Si:H films with a thickness of the order of 10 nm. These films are
1626 grown using PECVD at deposition temperatures around 200°C, with growth rates of the order
1627 of 10 nm per minute. Precursor gases for undoped a-Si:H films are SiH_4 and hydrogen (H_2).

1628 Doping is usually achieved by admixture of phosphine (PH_3) for n-type and diborane (B_2H_6)
1629 or trimethylboron ($B(CH_3)_3$) for p-type doping. Generally, processes are similar to those used
1630 for a-Si:H thin-film p-i-n solar cells. In the field of SHJ cells, most results have been reported
1631 for a-Si:H grown in conventional parallel plate reactors with radio frequency (RF,
1632 13.56 MHz) excitation, [267-269]. However, it appears that suitable deposition regimes can
1633 be found for most PECVD and related a-Si:H deposition techniques. Good surface
1634 passivation properties and/or solar cells have also been reported for a-Si:H grown with very
1635 high frequency (VHF≥ 40 MHz) excitation [263], hot-wire chemical vapor deposition
1636 (CVD) [270], DC saddle field PECVD [271], electron cyclotron resonance (ECR)-
1637 CVD [272] etc.

1638 The insertion of thin (2-8 nm) intrinsic a-Si:H interlayers for c-Si surface passivation
1639 between the c-Si wafer and the doped a-Si:H films used to form the p-n junction or BSF can
1640 be seen as a breakthrough for realizing the unique potential of SHJ cells, namely their
1641 outstandingly high V_{oc}. Indeed, Sanyo had patented this use of an intrinsic a-Si:H buffer and
1642 named their solar cells accordingly as heterojunction with intrinsic thin layer (HIT) cells
1643 [251]; the patent for the intrinsic buffer layer expired in 2011. This prompted attempts to
1644 achieve good cell performance also without using intrinsic a-Si:H (i-a-Si:H) layer with, at the
1645 time, notable results of 19.8% and 18.4% efficient cells for p-type a-Si:H/n-type c-Si and the
1646 inverse cell structure, respectively [273, 274]. However, V_{oc}s were generally much lower, of
1647 the order of only 630-640 mV. This is related to a doping-dependent defect generation
1648 mechanism in a-Si:H, as discussed below in Sec. 4.4.2. Thus, it is indeed essential to
1649 passivate the c-Si surface to reduce the density of defect states (D_{it}) in the bandgap (Fig. 25)
1650 by saturating dangling bonds at the c-Si surface using a low-defect i-a-Si:H layer.

1651 ### 4.4.1 Intrinsic a-Si:H films

1652 Many studies conducted in the past years have led to the conclusion that the microscopic
1653 structural and electronic configuration of ultrathin a-Si:H layers is governed by the same
1654 mechanisms as that of thick a-Si:H films, as described, for example, in Ref. [275,276]. The
1655 deposition conditions systematically affect the layer properties, and a combination of low-
1656 temperature deposition and a subsequent anneal was shown to yield best results in terms of
1657 a-Si:H/c-Si interface passivation. Interestingly, not only conventional hot plate anneals for
1658 several minutes, but also accelerated annealing using microwave radiation can be used. The
1659 latter process requires only a few seconds [277]. Furthermore, a cyclic sequence of short a-
1660 Si:H deposition and hydrogen plasma steps [278] or a post-treatment of the grown layer with
1661 a hydrogen plasma [279] have been useful in improving a-Si:H/c-Si interface passivation.



1662

1663 Fig. 28 Schematic sketch of the density of states (DOS) in the valence and conduction band of a-Si:H on the (a)
1664 linear and (b) semilog scale. The states occupied by electrons are marked as hatched area (left side), after [276].
1665 Urbach tails (i.e. exponentional distribution of electronic states from band edges into the bandgap) are induced
1666 by strain in the amorphous network. Occupied DOS as measured by using near-ultraviloet photoelectron
1667 spectroscopy, linear and semilog scale (right side). Reproduced with permission from [256], Wilfried G. J. H.
1668 M. van Sark, Lars Korte, Francesco Roca, Physics and Technology of Amorphous-Crystalline Heterostructure
1669 Silicon Solar Cells, 2011. Springer, 2011. Copyright © Springer-Verlag Berlin Heidelberg. License number
1670 3498221350973.

1671
1672 The density of states of a-Si:H is depicted in Fig. 28. In the valence and conduction
1673 bands, it is similar to that of c-Si, but has additional defect states in the bandgap. Urbach tails

1674 decay exponentially into the bandgap and are induced by strain in the amorphous network,
1675 whereas a broad distribution of defects near midgap consists of dangling (broken/unsaturated)
1676 Si-Si bonds, with density N_d. The exponential slope of the Urbach tails, the so-called Urbach
1677 energy (E_0), is a measure for the overall strain in the amorphous network (increased E_0 means
1678 increased strain), and dangling bonds are created when the strain in the bonds forming the
1679 Urbach tails becomes too large. Thus, it is intuitively clear that E_0 and the dangling bond
1680 density are related. Broadly speaking, if the a-Si:H network is in thermodynamic equilibrium,
1681 an increase in E_0 also yields an increased N_d. This is the gist of defect generation models
1682 proposed by Stutzmann [280] and by Powell & Deane [281,282]. The latter, so called defect
1683 pool model also considers electronic contributions to the system's free energy, which makes
1684 N_d and its distribution across the bandgap dependent on the position of the Fermi level.

1685 Electronically, the a-Si:H bandgap defects behave differently. While the band tail
1686 states act as traps for charge carriers from the band they are originating from, dangling bonds
1687 deeper in the gap are recombination centers. Dangling bonds are amphoteric defects, i.e., the
1688 sp^3 hybridized orbital of the dangling bond can be occupied by 0, 1 or 2 electrons, leading to
1689 the charge states D^+, D^0 and D^-. In the single-electron band diagram picture, the energy
1690 positions for the possible transitions of the dangling bond from unoccupied to singly
1691 occupied, $D^{+/0}$, and from singly to doubly occupied, $D^{0/-}$, are represented by two Gaussian
1692 distributions in the bandgap [281-283]. The $D^{+/0}$ states have donor character, the $D^{0/-}$ states
1693 are acceptor-like. In the description of recombination, this amphoteric character of the defects
1694 leads to a behavior that differs from the conventional Shockley-Read-Hall formalism [283-
1695 285].

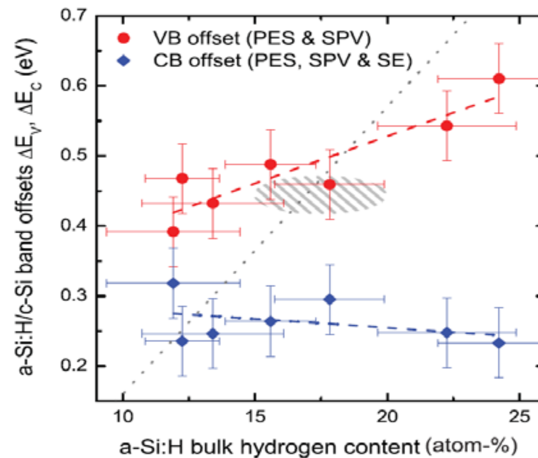


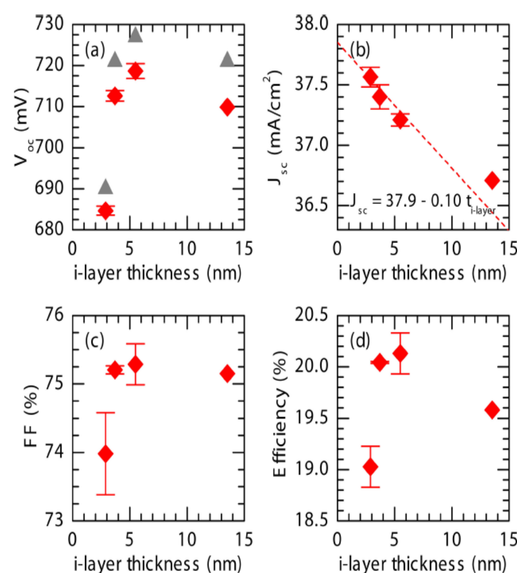
Fig. 29 Valence band offsets of i-a-Si:H/n-c-Si heterostructures with varying hydrogen content. The conduction band offset is determined based on the valence band offset, using the optical bandgap of the a-Si:H films as determined from spectral ellipsometry. As hydrogen content increases in the film, the main variation occurs in ΔE_V while ΔE_C is almost constant. For state of the art a-Si:H films (with 10-15% hydrogen) ΔE_V and ΔE_C are approximately 0.45eV and 0.25eV, respectively. Reproduced from [286] with permission, T. F. Schulze, L. Korte, F. Ruske, and B. Rech, Band lineup in amorphous/crystalline silicon heterojunctions and the impact of hydrogen microstructure and topological disorder, Phys. Rev. B **83** (2011) 165314. Copyright © 2011 American Physical Society. License number 3583611410416.

The deposition of a-Si:H on a c-Si wafer leads to the formation of a type I heterojunction (straddling gap, i.e., the gap of the smaller bandgap material is completely within the gap of the wider bandgap material). Thus, as can be seen from Fig. 25, the band offset at the a-Si:H/c-Si interface acts as barrier for both electrons and holes coming from the c-Si wafer. The value of the valence band offset ΔE_V can be determined reliably using near-UV photoelectron spectroscopy [287-289]. As the bandgap of a-Si:H can be varied by changing the hydrogen content of the film, the band offsets also have to vary. As shown in Fig. 29, it was found that the main variation occurs in ΔE_V, whereas ΔE_C is almost unchanged [286]. State of the art a-Si:H films (hydrogen concentration 10-15%) have $\Delta E_V \sim 0.45$ eV, $\Delta E_C \sim 0.25$ eV. No variation of the bandgap with film thickness or doping was found [288]. To date, there exist no systematic investigations of the influence of the increase in ΔE_V, i.e., in the barrier for hole transport, on solar cell properties.

At the a-Si:H/c-Si interface (Fig.25), as-deposited D_{it}/cm^2 is determined by the local network structure at the interface, which is in a non-equilibrium state for samples deposited at

1720 low-temperature [267]. The subsequent annealing step leads to thermodynamic equilibration
1721 between the a-Si:H bulk and the a-Si:H/c-Si interface. The equilibrated a-Si:H/c-Si interface
1722 region then does not possess unique electronic properties but is determined by the a-Si:H bulk
1723 density of states distribution [290]. The a-Si:H bulk volume defect density (N_d) /cm^3 is
1724 related to the a-Si:H/c-Si interface defect density by the relation $D_{it} = N_d \times d_t$, d_t is the
1725 characteristic length, in the nm range, over which charge carriers generated in the c-Si wafer
1726 can travel into the a-Si:H and then recombine via a-Si:H defects. A calculation based on the
1727 assumption that the charge carriers tunnel into the a-Si:H yields $d_t = 2.7$ nm [291]. Indeed,
1728 recombination at the a-Si:H/c-Si interface can be described consistently using a projected a-
1729 Si:H density of states as c-Si surface defect density of states [284].

1730 For high J_{sc}, photogeneration in the c-Si absorber must be maximized. Thus, it is
1731 desired to reduce parasitic absorption in the a-Si:H layers by reducing their thickness. Fig. 30
1732 shows an example of typical findings. Here, the j_{sc} decreases with a slope of ~ 0.1mA/cm² per
1733 additional nm of i-a-Si:H buffer layer thickness. However, it is found that a minimum i-a-
1734 Si:H buffer layer thickness of 5nm or slightly below is needed. For even thinner films (<5
1735 nm), the a-Si:H/c-Si interface passivation breaks down, therefore V_{oc} is reduced and the cell's
1736 fill factor also decreases [292].



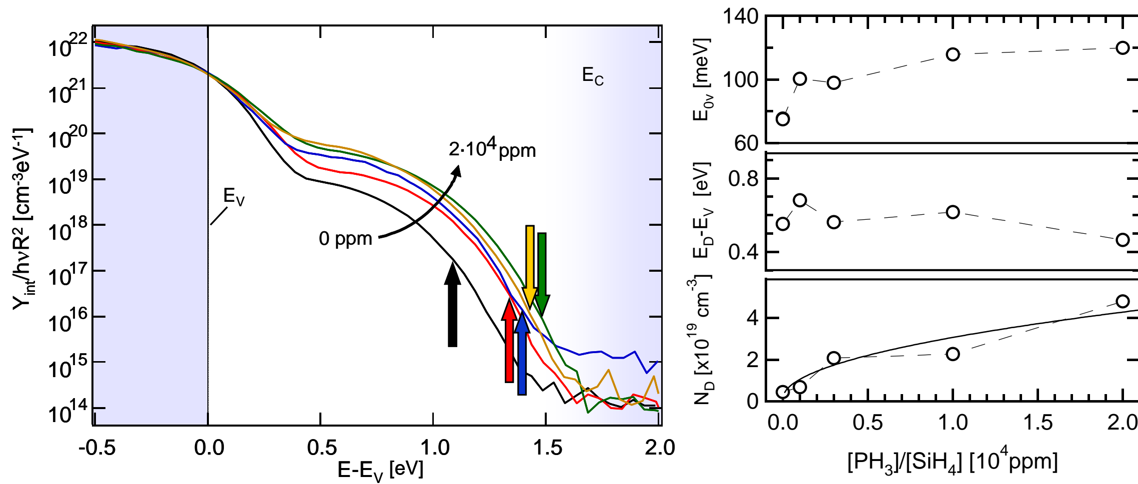
1737

1738 Fig. 30 Output characteristics of 4cm^2 solar cells with varying i-a-Si:H layer thickness. Each data point
1739 represents the average value of three cells, except the data for the thickest layer, for which only one cell was
1740 measured. The gray triangles in (a) represent the implied V_{oc}s of the cells prior to ITO deposition and
1741 metallization, determined from quasi-steady-state photoconductance (Sinton) measurements. The dashed line in
1742 (b) is the calculated dependence of J_{sc} on i-a-Si:H layer thickness. Reproduced from [292] with permission,
1743 Holman, Z.C.; Descoeudres, A.; Barraud, L.; Fernandez, F.Z.; Seif, J.P.; De Wolf, S.; Ballif, C., Current Losses
1744 at the Front of Silicon Heterojunction Solar Cells, IEEE Journal of Photovoltaics, **2** (2012)7. Copyright © 2012,
1745 IEEE. License number 3498231121849.

1746
1747

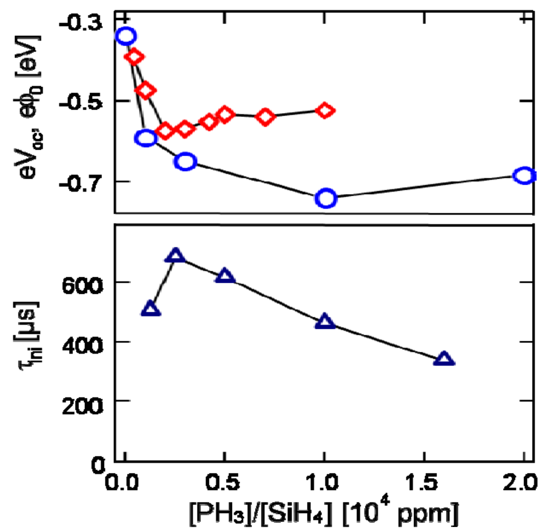
1748 **4.4.2 Doping of a-Si:H - formation of the p-n junction and doping induced defects**

1749 The a-Si:H film stack for the p-n junction and the BSF is completed by the deposition
1750 of doped a-Si:H layers on the i-a-Si:H buffers. As shown in Fig. 31, for increasing n-type
1751 doping of ~10 nm thin a-Si:H films, the defect density in a-Si:H increases with doping level,
1752 a behavior already well known for thick a-Si:H films [275]. Therefore, an optimum a-Si:H
1753 doping level exists for SHJ cells. For high doping levels, the increase in band bending at the
1754 heterojunction, which is beneficial for forming a well-working p-n junction (high cell V_{oc} and
1755 efficient carrier extraction, thus high fill factor, at the maximum power point), is balanced
1756 against increasing defect concentration. The latter is detrimental due to the enhanced
1757 recombination rate at the interface and in the a Si:H layers. This is exemplified in Fig. 32 for
1758 n-a-Si:H/p-c-Si solar cells without i-a-Si:H buffer: While the built-in potential of the p-n
1759 junction $e\phi_0$ increases up to a gas phase doping of 10^4 ppm, V_{oc} reaches a (rather low, due to
1760 the missing i-a-Si:H) maximum already at a moderate doping of ~2000 ppm and is reduced
1761 for higher doping. The minority-carrier lifetime τ_{ini} (in this case measured by surface
1762 photovoltage) follows the same trend as the V_{oc}: As shown in Fig. 32, lower panel, τ_{ini} peaks
1763 at the same doping level as the V_{oc}. Clearly, at doping levels above 2000 ppm, the increasing
1764 defect density at the a-Si:H/c-Si interface overcompensates the still (up to 10^4 ppm) slightly
1765 improving field effect passivation.



1766

1767 Fig. 31 Density of occupied states in the a-Si:H bandgap for increasing gas phase doping ($[PH_3]/[SiH_4]$ = 0 …
1768 10,000 ppm), arrows mark the Fermi level position (left side). Defect parameters, viz. valence band Urbach
1769 energy, energetic position and density of the dangling bond defect distribution (right side). As can be seen (right
1770 side), by increasing n-type doping in the a-Si:H film, defect density increases with doping level. Reproduced
1771 from [293], with permission, L. Korte, and M. Schmidt, Investigation of gap states in phosphorous-doped ultra-
1772 thin a-Si:H by near-UV photoelectron spectroscopy, J. Non-Cryst. Sol. **354** (2008) 2138. Copyright © 2008
1773 Elsevier B.V. License number 3472101463232.



1774

1775 Fig. 32 Upper panel: built-in potential $e\phi_0$ (circles) and solar cell V_{oc} (lozenges, rescaled to eV units). Lower
1776 panel: surface photovoltage decay time constant τ_{ini}. A heterojunction was formed between n-a-Si:H and p-c-Si
1777 without using a buffer layer (intrinsic a-Si:H). Note that minority-carrier lifetime (τ_{ini}) and V_{oc} peak at the same
1778 doping level. V_{oc} reaches a maximum at a doping level of 2000ppm and then decreases for higher doping. The
1779 built-in-potential increases up to a doping level of 10^4 ppm, then decreases slightly for higher doping.
1780 Reproduced with permission from [256], Wilfried G. J. H. M. van Sark, Lars Korte, Francesco Roca, Physics
1781 and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells, 2011. Springer, 2011. Copyright
1782 © Springer-Verlag Berlin Heidelberg. License number 3498221350973.

1783

1784 For doped a-Si:H deposited on i-a-Si:H buffer layers, an additional effect has to be
1785 considered: As shown by de Wolf et al. the shift in the i-a-Si:H Fermi level induced by
1786 deposition of the doped a-Si:H film on top of the i-a-Si:H leads to Si-Si bond rupture in the i-

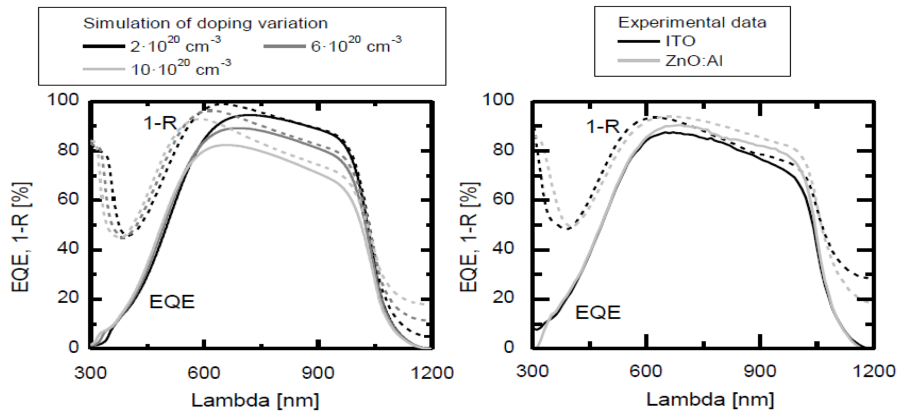
1787 a-Si:H buffer layer, i.e. generation of additional defects in the i-a-Si:H that counteract the
1788 movement of Fermi energy (E_F) and are recombination-active [294]. It can be surmised that
1789 this effect is closely related to the defect equilibration mechanisms described by the Fermi-
1790 level dependence of defect creation in the defect pool model.

1791
4.5 TCOs for SHJ heterojunction cells

1792 The TCO's role in SHJ cells is two-fold: (i) to provide sufficiently low contact and sheet
1793 resistance in order to transport the charge carriers coming from the a-Si:H to the metal
1794 contacts, and (ii) to act as an ARC, i.e. to maximize light incoupling into the solar cell. The
1795 quasi-standard TCO material in SHJ cells is ITO, another option is Al-doped zinc oxide
1796 (ZnO:Al) as shown in Fig.33, more recently indium oxide (In_2O_3) doped with hydrogen
1797 (In_2O_3:H) [295] or hydrogenated tungsten-doped In_2O_3 [296] have also been used.

1798 TCOs are degenerately doped wide bandgap semiconductors (E_g typically >3 eV): To
1799 fulfill the requirement (i), $R_{sh} < 100\ \Omega/sq$ is desired. Furthermore, the required refractive
1800 index around 2 together with the necessity to achieve destructive interference in the 600 nm
1801 range lead to a thickness of the order of $d_{TCO} = 80$ nm. Maximum carrier mobility (μ) is in the
1802 order of 10 to 70 cm²/Vs, thus with $R_{sh} = 1/(q\ N\ \mu\ d_{TCO})$, carrier concentrations (N) in the
1803 range of $10^{20}/cm^3$ are required. Such high carrier concentrations lead to a widening of the
1804 optical bandgap (Burstein-Moss shift), partially offset by a bandgap narrowing due to
1805 electron-impurity many body interactions, and an appreciable free carrier absorption in the
1806 longer wavelength range around the c-Si bandgap wavelength [292,297, 298]. Figure 33
1807 shows an exemplary comparison of simulated 1 – R and external quantum efficiency (EQE)
1808 curves for a HIT solar cell on flat wafer for various doping levels of a 85nm thick front
1809 ZnO:Al layer [299]. It is apparent from the simulation that for higher TCO doping, current is
1810 lost in the device due to inferior anti-reflection properties of the highly doped films (1 – R
1811 decreases) and increasing absorption in the TCO (area between 1 – R and the EQE increases).

1812 Comparison between the simulation (Fig. 33, left side) and experimental data obtained from
1813 ZnO:Al and ITO used as TCOs in HIT cells (Fig. 33, right side), shows that ZnO:Al yields a
1814 higher EQE due to the lower carrier concentration in the ZnO:Al. Further details can be found
1815 elsewhere [299].



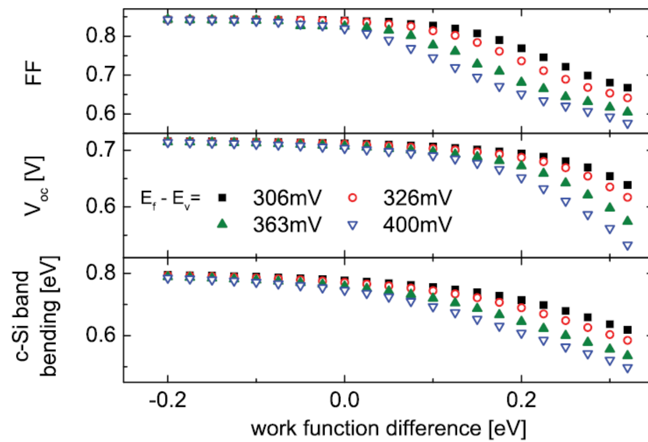
1816

1817 Fig. 33 Left side: Simulated reflectance (1-R) and EQE curves for a HIT solar cell on flat wafer for various
1818 doping levels of the 85nm thick front ZnO:Al layer. Right side: Experimental data for a similar system using
1819 ITO and ZnO:Al as front TCO materials. EQE is decreased for higher TCO doping. This is due to an increased
1820 absorption and poor anti-reflection properties in the highly doped TCO film. Experimental data from ITO and
1821 ZnO:Al used in HIT cells shows higher EQE for ZnO:Al film due to lower carrier concentration in ZnO:Al.
1822 Reprinted with permission from [299], R. Rößler, C. Leendertz, L. Korte, N. Mingirulli, and B. Rech, Impact of
1823 the transparent conductive oxide work function on injection-dependent a-Si:H/c-Si band bending and solar cell
1824 parameters, Journal of Applied Physics **113** (2013) 144513. Copyright © 2013 American Institute of Physics.
1825 License number 3472401268226.

1826

1827 Another aspect that has to be considered in optimizing a TCO for the use in SHJ cells
1828 is the band alignment with the a-Si:H (Fig.25). As shown in Fig. 34, the work function of the
1829 TCO plays an important role for the solar cell parameters. In the simulated case, a work
1830 function difference of only 0.1 eV between the TCO and the p-a-Si:H emitter already leads to
1831 an appreciable decrease in V_{oc} and, more pronouncedly, fill factor [299]. The reason is that
1832 on top of the desired p-n junction diode, an undesired counter diode is formed by the
1833 TCO/doped a-Si:H junction. This is depicted schematically in Fig.35, where an equivalent
1834 circuit consisting of the p-n diode and the TCO/p-a-Si:H counter diode with a parallel shunt
1835 resistance is sketched. These two diodes together with the resistance indeed yield a calculated
1836 current-voltage (I-V) curve that can go from slightly decreased fill factors to S-shapes. Such

1837 S-shaped I-V curves are observed experimentally [300,301] and also in numerical simulations
1838 such as the one used to generate Fig. 34 [302].

1839


1840 Fig. 34 Simulated solar cell parameters as a function of the work function difference between the TCO and the
1841 p-a-Si:H layer for different distances of the Fermi-level from the valence band. Between TCO and p-a-Si:H
1842 emitter, even a work function difference of 0.1eV leads to a significant decrease in V_{oc} and fill factor. This is
1843 due to an undesired counter diode formed by the TCO/doped a-Si:H junction. Reprinted with permission from
1844 [299], R. Rößler, C. Leendertz, L. Korte, N. Mingirulli, and B. Rech, Impact of the transparent conductive oxide
1845 work function on injection-dependent a-Si:H/c-Si band bending and solar cell parameters, Journal of Applied
1846 Physics **113** (2013) 144513. Copyright © 2013 American Institute of Physics. License number 3472401268226.

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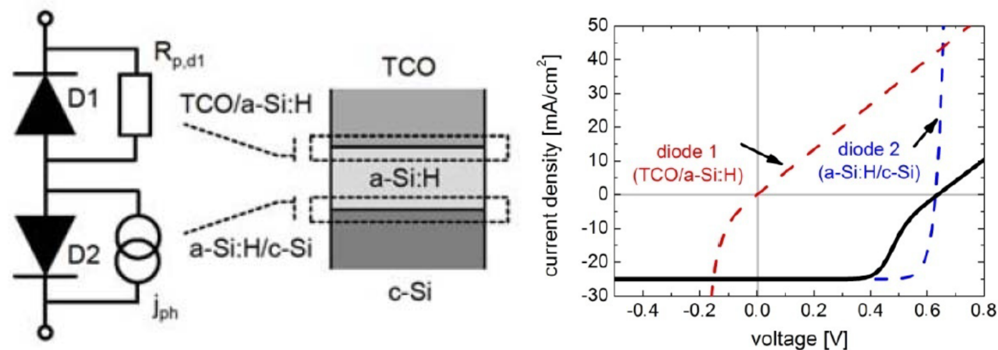


1850
1851 Fig. 35 Sketch of the TCO/a-Si:H/c-Si interface region, together with an equivalent circuit consisting of the
1852 desired a-Si:H/c-Si p-n junction and an antiparallel, parasitic TCO/a-Si:H diode (left side). Resulting I-V curve
1853 and contributions of the two diodes (right side). A parasitic diode is formed when there is a work function
1854 difference between TCO and doped a-Si:H. After [303], with permission, R. Rößler, L. Korte, C. Leendertz, N.
1855 Mingirulli, M. El Mhamdi, and B. Rech, ZnO:Al/(p)a-Si:H Contact Formation and Its Influence on Charge
1856 Carrier Lifetime Measurements, edited by G. Willeke, H. Ossenbrink, & P. Helm. Proc. 27th European
1857 Photovoltaic Solar Energy Conference and Exhibition, Munich: WIP Munich, 2012, p.1443.

1858
1859 This problem of an unsuitable work function is a general one for the usual n-type TCOs
1860 forming junctions with p-a-Si:H. However, it appears that it is less pronounced for the case of

1861 ITO than for ZnO:Al [299,303]. Still, one might speculate that this is a possible reason for the
1862 consistently lower fill factors in SHJ cells as compared to diffused junction cells with similar
1863 V_{oc} [255,290].

1864 4.6 Charge transport in SHJ: I-V curves and device operation

1865 For the SHJ cell, charge transport across the junctions may proceed both by diffusive
1866 transport as well as by tunneling processes, the detailed transport mechanisms being
1867 dependent on the materials properties (defect densities, bandgap/band offset height) as
1868 already discussed above, and also on the regime of the applied bias voltage. Under high
1869 forward bias, at the operating point of the cell, diffusive transport prevails at least in state-of-
1870 the art SHJ cells, and indications for tunnel transport are found in low forward and reverse
1871 bias [268,304,305]. If, for example, the band offset for the holes at the p-a-Si:H/n-c-Si
1872 contact depicted in the band diagram of Fig.25 becomes too high, charge carrier transport can
1873 be hindered because the charge carrier has to overcome the band offset barrier by thermionic
1874 emission or tunneling processes. Depending on the details of charge distribution and
1875 recombination at the heterointerface, this can manifest in the solar cell characteristics curve
1876 as an effect similar to a series resistance, or in an S-shaped I-V curve, [300,306] which,
1877 however, can also arise from the TCO/a-Si:H junction, as mentioned above. On the other
1878 hand, an increased band offset can also decrease the cell's sensitivity to high defect densities
1879 at the a-Si:H/c-Si junction. This is depicted in the simulation result in Fig.36, where together
1880 with a general trend of increasing cell efficiency with increasing minority-carrier band offset
1881 (in this case, ΔE_C, because an n-a-Si:H/p-c-Si cell is simulated), it is also observed that the
1882 drop in cell efficiency for increasing a-Si:H/c-Si interface defect densities is less severe if
1883 ΔE_C is large.

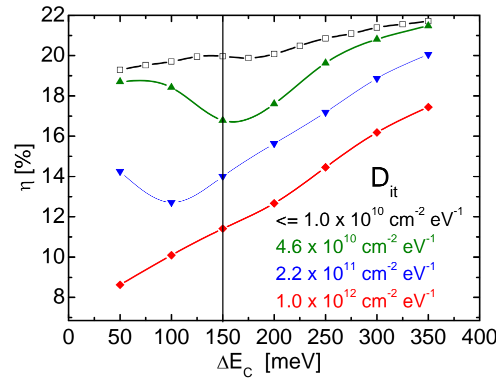


Fig. 36 Dependence of the simulated efficiency of n-a-Si:H/p-c-Si solar cells on the minority-carrier band offset and the interface trap density (D_{it}) at the a-Si:H/c-Si interface. Cell efficiency increases with increasing minority-carrier band offset (ΔE_C). An increased band offset decreases the cell's sensitivity to high defect densities at the n-a-Si:H/p-c-Si junction. Also, the drop in cell efficiency is less severe (for increasing D_{it} at the a-Si:H/c-Si interface) when ΔE_C is large. After [300], Froitzheim, A., K. Brendel, L. Elstner, W. Fuhs, K. Kliefoth, and M. Schmidt. "Interface recombination in heterojunctions of amorphous and crystalline silicon." J. Non-Cryst. Sol. **299-302** (2002) 663.

State of the art SHJ cells can be described very well with the usual 2-diode-model plus series and parallel resistance. Furthermore, it was found that the description of an a-Si:H/c-Si cell in high forward bias, i.e. notably, at the maximum power point, or V_{oc}, can be carried out in terms of the simple Shockley diffusion model, just as for (ideal) homojunction solar cells [268]. The SHJ cell essentially behaves like a single-sided junction (space-charge region only in the c-Si, recombination at the a-Si:H/c-Si interface), with one important difference: The analysis of the ideality factor (n_1) and activation energy of the reverse saturation current carried out in [268] shows that the heterojunction aspects of carrier transport across the p-n junction become more pronounced with enhanced interface passivation, and are responsible for a deviation from the ideal value of $n_1 = 1$.

4.7 Double sided SHJ solar cells - state of the art

De Wolf's review [255] provides an excellent and comprehensive overview on the R&D groups working on SHJ cells and their best published results. In the following, some important results are mentioned and updates are given. Note that single-sided SHJ cells are excluded from this summary, since they are discussed in Sec. 5.

1908 Many groups are today able to manufacture SHJ solar cells with efficiencies exceeding
1909 20%, and V_{oc}s well above 700 mV. However, since the rediscovery of the SHJ concept in the
1910 1990s, and the introduction of the i-a-Si:H buffer layer, the record in SHJ cell efficiency has
1911 been held by Sanyo, now Panasonic. The currently best double-sided SHJ cell has an
1912 efficiency of 24.7% (V_{oc} = 750mV, J_{sc} = 39.5mA/cm², fill factor = 83.2%) [248]. The cell
1913 was fabricated from a 98µm thin wafer on an area of 100cm². With this step, the HIT cell not
1914 only surpasses the best published result for a large area production type cell, i.e. SunPower's
1915 24.2% efficient rear contact cell [178], but falls short by only 0.3% of the PERL cell
1916 manufactured by UNSW that holds the world record for a c-Si solar cell and is fabricated on
1917 a small area (4cm²), with photolithographic processes that are incompatible with large-scale,
1918 low-cost industrial production. It is interesting to note that the improvement over Sanyo's
1919 previous 23.7% cell stems mainly from an improved fill factor, which went up by 2.3% as
1920 compared to the previous best cell. With a fill factor of 83.2%, the HIT cell has now indeed
1921 closed the fill factor gap that was (and, for other groups working in the field, still is) present
1922 between highest efficiency homojunction and heterojunction solar cells [303]. Furthermore,
1923 the high V_{oc} of Sanyo/Panasonic's cell is also related to the low wafer thickness. For solar
1924 cells with excellently passivated surfaces, the total (wafer thickness integrated) density of
1925 recombination-active states is dominated by the c-Si bulk recombination centers, thus scales
1926 with wafer thickness. Therefore, the photogenerated charge carrier density, thus the V_{oc},
1927 increases until the wafer is too thin to absorb the incoming sunlight sufficiently well.
1928 Therefore, the theoretical maximum V_{oc} peaks at 769mV for 100µm wafer thickness [307], a
1929 value that Sanyo has come surprisingly close to.

1930 Further remarkable high-efficiencies reported by the Institute of Microengineering (IMT)
1931 at Ecole Polytechnique Fédérale de Lausanne (EPFL), for SHJ cells based on n-type and p-

1932 type c-Si wafers [263] are 22.1% and 21.4%, respectively. To our knowledge, the latter is the
1933 highest reported for a SHJ cell on p-type wafers.

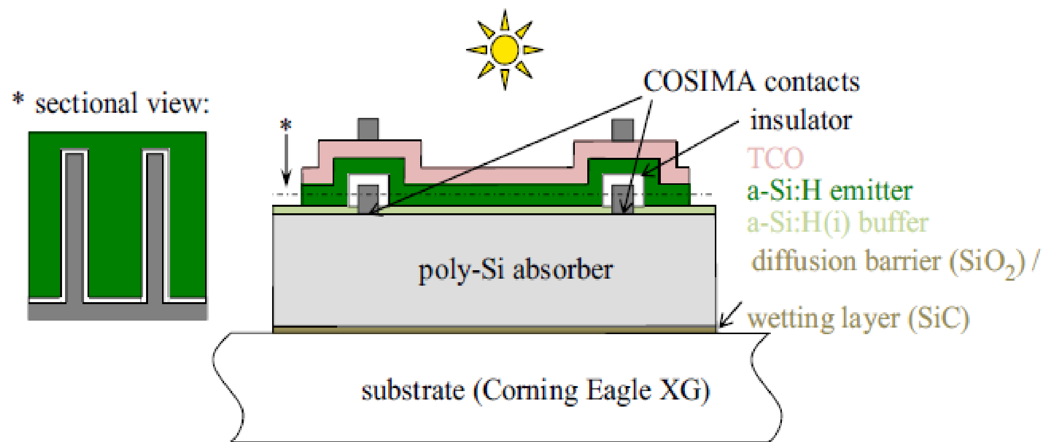
1934 Regarding highly efficient cells on large area and industrialization of the SHJ concept,
1935 Sanyo/Panasonic have shown above 21% cell efficiency (>18% module efficiency) in
1936 industrial production [249]. The French Institut National de l'Énergie Solaire (INES) has
1937 reported 21% and 22.2% efficient cells on $103 cm^2$ made with Ag screen-printed and Cu
1938 plated contacts, respectively [259], and Roth&Rau/Meyer Burger have shown large area (6")
1939 cells with 21.3% efficiency [308]. Very recently, Choshu industry has reported a 24.1%
1940 efficient SHJ cell on an area of $243.4 cm^2$, which features cerium oxide and hydrogen co-
1941 doped indium oxide films as TCOs [309]. Further important steps to lowering the levelized
1942 cost of energy are Roth&Rau's 21.6% efficient cell on a $239\ cm^2$ pseudosquare Cz wafer
1943 with a Ag-free front grid, cells above 21% efficiency on a pilot line equipment and their
1944 demonstration of a 303W SHJ module made of sixty 6" pseudosquare SHJ cells [310]. A
1945 production line with a throughput of 4800 wafers/h and a target efficiency of 21% is also
1946 available.

1947 Si heterojunctions have also been used in hybrid cell concepts, i.e. cells where only one of
1948 the junctions is formed as a SHJ. An example of this concept is an inverted SHJ hybrid cell,
1949 where in addition, the p-n junction is located on the rear of the cell instead of the front side
1950 that is facing the sun. With a rear side SHJ (i.e. back heterojunction) in combination with a
1951 diffused (thus, homojunction) front surface field and point contacts on the front, a cell
1952 efficiency of 22.8% has been reported [311].

1953 Another hybrid concept is pursued by Hekmatshoar et al. who introduce a thin, highly
1954 doped epitaxial c-Si film between the c-Si wafer and an a-Si:H on one side, and an a-Si:H
1955 heterojunction with an additional a-Ge:H interlayer on the rear, leading to a 21.4% efficient
1956 cell [312].

1957 # 4.8 Future direction

1958 Given the rapid progress discussed, it is very likely that c-Si wafer based SHJ technology
1959 will approach the 25% cell level efficiency in production. However, there remain many
1960 challenges for further improving SHJ cell technology. For example, in order to improve J_{sc},
1961 better transparency of the contact layers is needed. For the a-Si:H films, this might lead to
1962 their substitution by microcrystalline Si (µc-Si:H), amorphous Si oxide (a-SiO_x:H) or
1963 amorphous Si carbide (a-SiC_x:H) films. TCOs with increased transparency/carrier mobility
1964 could be based on hydrogen doped In_2O_3, or alloys of indium and oxygen with other metals
1965 [309]. For the TCO, the indium cost issue might be solved by its substitution, e.g. by ZnO:Al,
1966 although the problem of an unsuitable work function/parasitic diode on p-a-Si:H needs to be
1967 solved, probably by TCO/a-Si:H interface engineering (by insertion of suitable interlayers).
1968 Another cost driver is the high amount of Ag used in screen-printed contacts. This has
1969 already led to approaches using electroplating. However, their long-term reliability is as yet
1970 unproven. Looking further into the future of c-Si based PV, it is clear that SHJ are an ideal
1971 technology not only for fabricating cells on ever thinner wafers, but also for innovative
1972 approaches based on high quality wafer-like thin-film Si solar cells on glass. In this case, the
1973 key feature of the SHJ technology is that process temperatures stay below 200°C at all times,
1974 i.e. far below the melting temperature of the glass. Promising results have been demonstrated
1975 for SHJ on kerf-loss free Si thin-films transferred to a glass carrier [313], and also for a-
1976 Si:H/poly-Si cells (Fig. 37), where a ~10 µm thin Si film is deposited onto the glass with high
1977 rate e-beam evaporation, then recrystallized by scanning with a line-shaped electron or laser
1978 beam. This yields a polycrystalline Si film with grain sizes up to a cm^2 [314].



1979

1980 Fig. 37 Schematic cell design of the Front ERA (front contacted electron beam recrystallized absorber)
1981 a-Si:H/poly-Si heterojunction solar cell on glass. The poly-Si absorber is a ~10µm polycrystalline Si thin-film
1982 consisting of grains with a width in the mm range, and up to several cm long. Polycrystalline Si thin-film is
1983 deposited by e-beam evaporation with high deposition rate, and then recrystallized by electron or laser beam.
1984 Reproduced from [314], Haschke, J. and Jogschies, L. and Amkreutz, D. and Korte, L. and Rech, B.
1985 Polycrystalline silicon heterojunction thin-film solar cells on glass exhibiting 582mV open-circuit voltage, Solar
1986 Energy Materials & Solar Cells, **115** (2013) 7. Copyright © 2014 Elsevier B.V. License number
1987 3472100659635.

1988 Furthermore, their high-efficiency makes SHJ cells (and other high-efficiency c-Si
1989 based solar cells concepts) a very interesting candidate for combining them with wide
1990 bandgap cells into double-junction solar cells, which have the potential to break the
1991 efficiency limit of single-junction solar cells. Combinations of III-V based top cells with c-Si
1992 cells are discussed in Sec.6. However, due to the thermal constraints, the combination of III-
1993 V with SHJ cells is difficult. An alternative approach that has recently drawn much attention
1994 are metal halide perovskite-based top cells (see Sec. 10), which can be combined with SHJ
1995 cells in either monolithically integrated 2-terminal devices [315, 316, 317] or by mechanical
1996 stacking of the two sub-cells, leading to a 4-terminal device, where each subcell has its own
1997 electrical connection. For the monolithically integrated 2-terminal devices, efficiencies have
1998 reached 21.4% [315]. For the 4-terminal cells, efficiencies between 13 and 22.8% have been
1999 reported [318, 319,320].

2000 The development of compatible processes and, importantly, semi transparent contact
2001 systems for the perovskite top cells are currently an important field of research, with different
2002 approaches ranging from sputtered TCOs to solution processed layers such as Ag nanowires

2003 [319] or graphene [321]. Furthermore, it has been recognized that tuning of the perovskite top
2004 cell's bandgap to an optimum value of around 1.74eV will allow for further improvements of
2005 double-junction cell efficiency. Recently, it was experimentally shown that a photostable
2006 perovskite based on mixtures of cesium and formamidinium as well as mixed iodide and
2007 bromine can be employed to tune the bandgap to 1.74eV enabling a high V_{oc} of 1.2eV [322].

2008 5.0 Crystalline Si based solar cells: back heterojunction

2009
2010 A reasonable estimate for the technologically achievable efficiency limit of single-
2011 junction c-Si based solar cells is about 28% (J_{sc} = 42.5mA/cm^2, V_{oc} = 760mV, fill factor =
2012 87%) [323]. To approach the theoretical efficiency limit in Si based solar cell [307], several
2013 strategies can be explored. One of the most attractive technologies is the IBC cell structure.
2014 Here, as mentioned in Sec.3, both cell electrodes are located on the rear side of the solar cell
2015 and laid out as two interdigitated combs. If the front surface recombination processes have
2016 been reduced, this approach overcomes the main limitation to the J_{sc} of the cell imposed by
2017 the front grid shaped contact shadowing. The shadowing is about 8% of the cell area and can
2018 be reduced to 4% using relatively sophisticated and expensive techniques [76]. In the IBC
2019 structure the front side of the cell is completely exposed to the sun to maximize light
2020 absorption when an appropriate anti-reflection coating is deposited on the device surface.
2021 IBC concept, initially proposed by Lammert and Schwartz [183], is the most relevant feature
2022 of the SunPower solar cell that achieved a record efficiency of 24.2% on n-type Fz c-Si wafer
2023 [178]. Here, the choice of Si heterojunction, instead of high-temperature emitter diffusion to
2024 form a homojunction, has demonstrated several advantages, such as: (i) high V_{oc} due to the
2025 potentiality of SHJ and due to the good c-Si surface passivation promoted by the a-Si:H layer
2026 that reflects in high cell efficiency as demonstrated by several groups as listed in Ref.[324].
2027 Even though the SunPower homojunction record efficiency cell reaches a V_{oc} value of 720
2028 mV, the highest V_{oc} value of 750 mV, as well as cell efficiency of 24.7% on c-Si based

2029 101.8cm^2 solar cell have been recently demonstrated by Sanyo-Panasonic heterojunction HIT
2030 cell [325]; (ii) excellent stability since the extremely thin a-Si:H layer used in the HJ
2031 technology is not prone to the undesired Staebler-Wronski degradation effect [326] that still
2032 affects the a-Si:H thin-film solar cells; (iii) lower voltage reduction under thermal stress
2033 during sunlight exposure with respect to conventional c-Si based cells (-0.3%/°C vs -
2034 0.5%/°C). This represents a great advantage in operating conditions since the cells are
2035 packaged using glass and plastic and left under sunlight with low possibility to dissipate the
2036 thermal excess; (iv) lower cell manufacturing cost due to reduced process time and to lower
2037 thermal budget in the cell fabrication. The last allows the use of very thin c-Si wafer [327]
2038 that can strongly reduce the photovoltaic cost [29,328].

2039 By merging the SHJ and IBC concepts it is possible to realize a promising technology
2040 for c-Si solar cell [329]. In this section, relevant issues of IBC-SHJ (i.e. back heterojunction)
2041 design for solar cell fabrication will be discussed and the industrial perspective of this cell
2042 concept will be also be discussed.

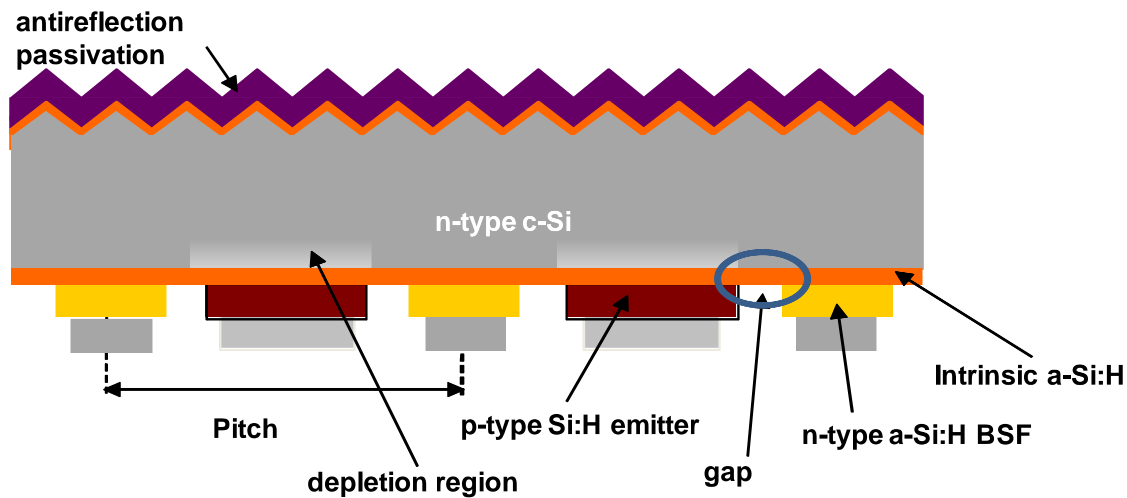
2043

2044 5.1 Brief history and status of art

2045 The idea to apply the IBC concept to the HJ cell, to take advantage of low thermal
2046 budget process and high V_{oc} together with a fully exposed sunward side, was proposed by Lu
2047 et al. [330]. They developed cells based on polished 2.5 Ω-cm n-type c-Si Fz 300μm thick
2048 wafer. Both 20 nm thick each p-type a-Si:H emitter and n-type a-Si:H base contact were
2049 deposited in a multi-chamber PECVD system at temperature of 200°C at the rear side of the
2050 cell to form an interdigitated structure, by photolithography, consisting of 1.2mm wide strips
2051 for emitter and 0.5mm for base contact, separated by 2μm wide non-diffused and non-
2052 passivated region. The sunward side was passivated by 20 nm intrinsic a-Si:H layer,
2053 subsequently covered with ITO and magnesium fluoride double layer as ARC. In subsequent
2054 publication [331] the same group of authors demonstrated the role of Si surface passivation

2055 between the doped regions to achieve higher cell efficiency. Tucci et al. presented a novel
2056 scheme for heterojunction called **B**ack **E**nhanced **H**eterostructure with **IN**ter**D**igitated
2057 (BEHIND) contact solar cell [332-334]. This method neither involved wet chemical steps,
2058 nor photolithography to pattern the two interdigitated back contacts. They were deposited by
2059 PECVD as a comb shape with the help of metallic masks, self-mechanically aligned in a
2060 specifically designed holder for both the c-Si wafer and the masks. In principle this method
2061 may easily be scaled up for large area cells, appropriate for industrial applications. The
2062 BEHIND solar cells were fabricated on 200μm thick, <100>, 1 Ω-cm p-type, Cz c-Si wafer.
2063 After front side alkaline texturing and RCA cleaning, a double layer stack of a-Si:H/SiN was
2064 deposited on the sunward side, acting as passivation and anti-reflection layer [335]. Then on
2065 the whole polished wafer backside, after a short 2% HF procedure to remove the native
2066 oxide, an intrinsic a-Si:H buffer layer was deposited before the n-type a-Si:H emitter. To
2067 increase the emitter conductivity a chromium silicide (CrSi) layer was then formed [336] by
2068 chromium (Cr) evaporation and wet chemical removal. A metallic mask, fabricated from a
2069 100μm thick molybdenum foil having a comb shaped aperture, was fixed over the emitter
2070 layer. A dry etching procedure using nitrogen trifuoride gas was performed to remove the n-
2071 type a-Si:H portion not covered by the mask, using settings defined on the base of previous
2072 experiments [337]. Subsequently, keeping the mask in the same position, the cell base contact
2073 was formed by an intrinsic a-Si:H buffer and a p-type a-Si:H layers. Through the same mask,
2074 a 30nm thick Cr layer was evaporated. Then a low-temperature sintering Ag paste was
2075 screen-printed on both interdigitated contacts [338]. The BEHIND cell was the first IBC-BHJ
2076 (Fig. 38) cell fabricated without any photolithographic step and it demonstrated the
2077 possibility to deposit a-Si:H film through metal masks. The total area of the solar cell was
2078 6.25cm^2. Different versions of the cell process were presented in literature and the best results

2079 are reported in Table 1. Schematic diagram of IBC-BHJ cell is shown in Fig. 38. Here, n-type
2080 c-Si, p-type a-Si:H and n-type a-Si:H acts as base, emitter and BSF respectively.



2081

2082
2083 Fig. 38 Schematic diagram of IBC-BHJ cell showing grid-less front surface. Neglecting the recombination at
2084 front and rear c-Si surface, when charge carriers are photogenerated within the c-Si wafer, due to concentration
2085 gradient, charge carriers diffuse to the rear side of the cell where they can be collected by their respective
2086 electrodes if charge carriers are able to arrive in the depletion region formed close to the p-type a-Si:H emitter
2087 layer. Therefore, in principle, the distance between two emitter regions should be thinner than half of minority
2088 carrier diffusion length. Photogenerated electrons can be collected in the n-type a-Si:H contact if able to
2089 overcome the intrinsic a-Si:H passivation layer. BHJ design eliminates shadowing effect caused by metal grids
2090 and allows sufficient metal to be used at the rear side to minimize resistive losses.
2091

2092 In early 2011, Helmholtz-Zentrum Berlin (HZB) together with Institute for Solar
2093 Energy Research Hamelin (ISFH) group developed a 20.2% efficient IBC-BHJ cell [232] on
2094 n-type 3Ω-cm Fz wafer. The front side was textured and phosphorous diffused to form a front
2095 surface field, and then passivated by SiO_2/SiN. The back side area was covered by 60%
2096 emitter contacts (p-type), 28% base contact (n-type) and 12% gap space between these,
2097 passivated by a SiO_2/SiN stack, with pitch in the range of millimetres. The metal contact was
2098 Al for both emitter and base regions. Two different approaches were considered: with or
2099 without intrinsic buffer layer just under the emitter, obtaining in both cases nearly 20%
2100 efficiency. In the first case V_{oc} is 40mV higher (673mV), but the fill factor is nearly 3%
2101 absolute lower (75.7%); due to the J_{sc} (39.7mA/cm^2) the efficiency was 20.2%. Without
2102 buffer layer the V_{oc} was 633mV but the fill factor was as high as 78.8% with the same

2103 current, so that the efficiency was 19.8%. The entire cell fabrication process was performed
2104 on 1cm^2 area by photolithographic steps. The best results are summarized in Table 1.
2105 The participants of the SHARCC project in France developed an innovative process
2106 called SLASH (Structuring by Laser Ablation of Si Heterojunction). They suggested the
2107 following sequence of steps: (i) emitter deposition and patterning by laser ablation; (ii) base
2108 contact deposition and laser patterning; (iii) front ARC deposition; (iv) ITO deposition; (v)
2109 screen-printing at low-temperature; (vi) laser ablation to separate the contacts. With this
2110 technology a 19% efficiency (Table 1) on 25 cm^2 area has been demonstrated [259,339].
2111 The IBC-BHJ proposed by IMEC Belgium started from Cz n-type, 3-4Ω-cm <100> c-
2112 Si wafer with thickness of either 150 or 280μm. Different front side passivation schemes
2113 were adopted: n^+-diffusion ($POCl_3$) and HJ on both textured and flat surface. Then on the rear
2114 side of the wafer a i-a-Si:H passivation layer, and p^+-doped emitter were deposited by
2115 PECVD at temperatures less than 200°C. An ITO transparent conductive oxide was deposited
2116 on the a-Si:H layers. Photoresist was spun on both sides of the wafer, and patterned on the
2117 rear side, before etching through the ITO. Openings through the a-Si:H layer were performed
2118 by wet chemical etch. After HF dip, Al base contacts were deposited by e-beam evaporation.
2119 The emitter contact was obtained by depositing Ti/Pd/Ag using e-beam evaporation on the
2120 ITO layer using shadow masks. A final anneal was performed in nitrogen at low-temperature.
2121 An efficiency of 15.2% efficiency was achieved on 1cm^2 area [340]. The best results are
2122 summarized in Table 1.
2123 The BACH (Back Amorphous-Crystalline Si Heterojunction) cell was developed at
2124 University of Toronto. The cell was fabricated on n-type 300μm thick 20 Ω-cm Fz c-Si
2125 wafer. In this case the fabrication process consisted of different photolithographic steps with
2126 at least 4 photomasks. The process sequence also included initial oxidation of the n-type
2127 wafer to have surface passivation, and electrical isolation between emitter and base contacts

2128 at the back side. The front surface was textured. The efficiency of IBC-BHJ cells with an area
2129 of circa 1cm^2 was of 16.7%, with V_{oc} of 641mV, and J_{sc} of 33.7mA/cm^2. However fill factor
2130 was appreciably higher than 77% [341,342]. The major limiting factor for both V_{oc} and J_{sc}
2131 was recognized due to surfaces passivation.

2132 The latest design is by LG Electronics. However very few details are available on the
2133 technology adopted. The design started on n-type Cz and Fz c-Si. After texturing, n-a-
2134 Si:H/ARC films were deposited for FSF front surface passivation. Then on the wafer rear
2135 side, n-type a-Si:H base and p-type a-Si:H emitter were deposited. On both doped regions the
2136 TCO was deposited and subsequently an Ag metal contact was screen printed, or Cu
2137 electrodes were electroplated [343]. In February 2014 Panasonic company announced
2138 efficiency higher than 25% [344] on very large area device as reported in Table 1, in which
2139 all the best results are reported.

2140 Table 1 List of PV parameters of the IBC-BHJ cells.
2141

Institution	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill factor (%)	Eff. (%)	Area (cm^2)	c-Si wafer	Patterning	Metallization
Panasonic	740	41.82	82.7	25.57	143.7	n-type	-	-
LG Electronics	723	41.8	77.4	23.4	4	n-type Fz	Photolithog.	Sputtered Al
	692	38.4	77.9	20.7	238.95	n-type Cz	Screen printing	Screen Printing Ag
	716	37.5	76.4	20.5	238.95	n-type Cz	Screen printing	Electroplated Cu
HZB	673	39.7	75.7	20.2	1	n-type 3 Ω-cm Fz	Photolithog.	Evaporated Al
INES-CEA	695	36.6	75.2	19	25	n-type 1-5 Ω-cm Fz	laser	Screen Printing Ag
University of Toronto	641	33.7	77.3	16.7	1	n-type 1 Ω-cm	Photolithog.	Evaporated
IMEC	605	39.1	64	15.1	1	n-type 1-4 Ω-cm	Photolithog.	Evaporated
ENEA	695	35.3	60.9	15	6.25	p-type 1 Ω-cm	Shadow mask	Evaporated
University of Delaware	602	26.7	73	11.8	1.32	n-type 2.5 Ω-cm	Photolithog.	Evaporated

2142

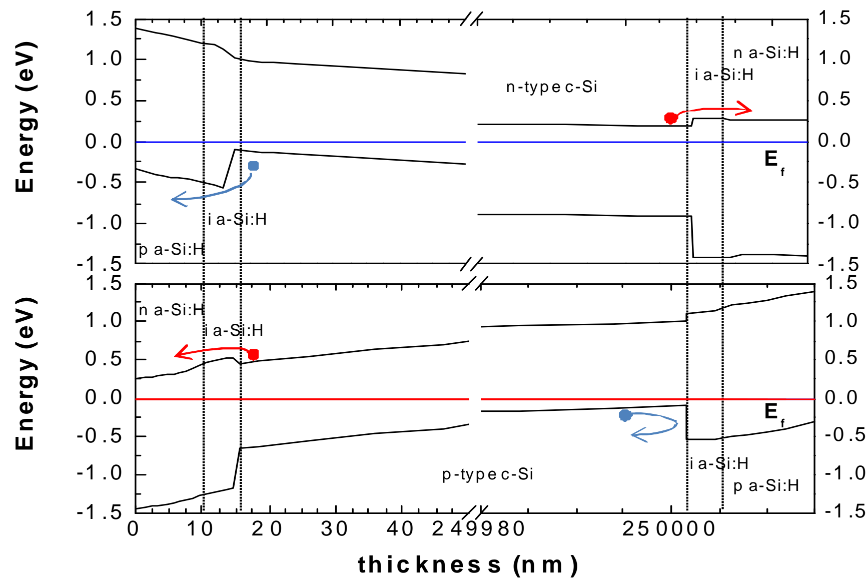
2143 ## 5.2 Interdigitated back contact design

2144 Several aspects of the device design are needed to be carefully accounted for to achieve
2145 high-efficiency solar cell. One of them is, for example, is having minority-carrier lifetime
2146 corresponding to diffusion length at least three times higher than the wafer thickness.
2147 Moreover other parameters have to be rightly addressed to design the highest efficiency solar

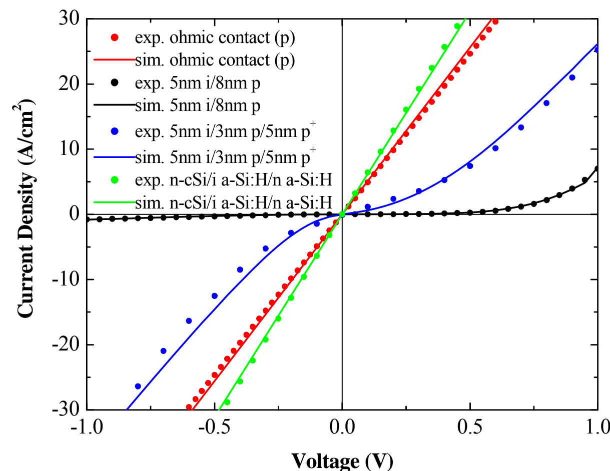
2148 cell. In this section the choice of materials and the design aspects needed to optimize the
2149 IBC-BHJ cell are reviewed.
2150
2151
5.2.1 Choice of c-Si wafer

2152 The choice of wafer type and doping level play a dominant role in device design due
2153 to the asymmetry of material properties respect to the carriers. Some considerations from
2154 physics, chemistry, and industrial engineering can drive that choice but sometime in opposite
2155 directions. Physically, p-type c-Si should be used in IBC solar cell since the minority
2156 photogenerated carriers move by diffusion and, when p-type is chosen, minority-carriers are
2157 electrons with lower effective mass and higher mobility than holes [341]. On the other hand
2158 n-type c-Si should be preferred to avoid boron-oxygen undesired complex formation, which
2159 is responsible for efficiency degradation under sunlight exposure [345]. The best HJ cell
2160 efficiency was demonstrated on n-type c-Si [327] due to useful band alignment at the both
2161 front and rear interfaces [346], as evident from the upper side of Fig. 39. The asymmetry in
2162 the offset displacement between a-Si:H and c-Si, higher in valence band than in conduction
2163 band [287], plays a role in the device design. It is not a serious problem for the main p-n
2164 junction due to the electric field arising from the junction built-in potential, but it introduces a
2165 difficulty for the base contact [347]. Band distributions, as deduced from numerical
2166 simulations [348] of HJ device based on the two different doping types of c-Si wafers, are
2167 compared in Fig. 39. The n-type c-Si/n-type a-Si:H contact forms an Ohmic contact and a
2168 spontaneous BSF helpful to keep holes away from the base metal electrode. The p-type c-
2169 Si/p-type a-Si:H contact needs some care to ensure the majority carriers collection with
2170 reduced probability of recombination at the base metal electrode. A comparison of I-V
2171 characteristics of HJ base contacts of devices based on p-type or n-type c-Si wafer is shown
2172 in Fig. 40, as deduced from numerical simulations (solid lines) performed on different a-Si:H
2173 layer thicknesses and experimental results (symbols). By comparing experiment and the

2174 simulation results, the perfect Ohmic behaviour of n-c-Si/i-a-Si:H/n-a-Si:H heterostructure is
2175 evident. In case of p-type c-Si, a p^+-layer is needed to approach the Ohmic characteristic as
2176 that obtainable using Al diffusion into p-type c-Si, shown in Fig. 40 as red symbols and solid
2177 lines. A density of states of $1x10^{15}/cm^3/eV$ within intrinsic a-Si:H layer has been used in
2178 performing the simulations.



2179
2180 Fig. 39 Band diagram comparison of HJ structure based on n-type c-Si wafer (upper side) and p-type c-Si wafer
2181 (lower side) as deduced from numerical simulations. The light impinges the heterostructure on the left side.
2182 Electrons (red dots) can easily cross the small band offset at the p-c-Si/n-a-Si:H interface as well as at n-c-Si/n-
2183 a-Si:H. Holes (blue dots) cross the n-c-Si/p-a-Si:H interface with the aid of electric field, but can be reflected at
2184 the p-c-Si/p-a-Si:H interface due to the large valence band offset between c-Si and a-Si:H materials. Note that
2185 band offset is higher in the valance band than in the conduction band, plays arole in the revice design. Both
2186 Ohmic contact and a spontaneous BSF is formed between n-type c-Si/n-type a-Si:H and keeps holes away from
2187 reaching the metal electrode.
2188



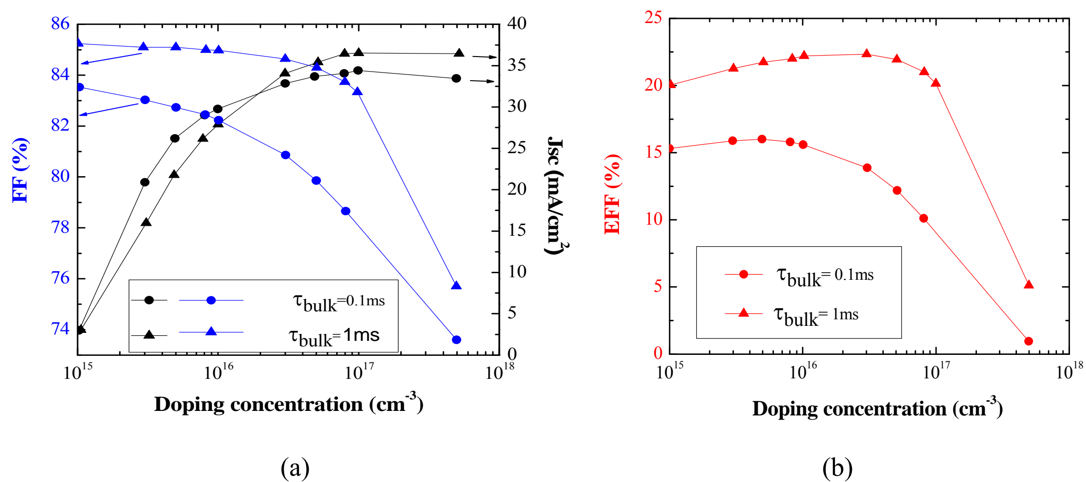
2189

2190 Fig. 40 I-V characteristics in dark conditions of heterojunctions based on p-type and n-type c-Si wafer.
2191 Experimental data (exp.) and simulations (sim.) are reported as symbols and solid lines respectively. A perfect

Ohmic contact can be seen for the n-c-Si/i-a-Si:H/n-a-Si:H heterostructure (green dots and curve). For p-c-Si, a p^+-layer is required for Ohmic contact which can be obtained by Al diffusion into p-c-Si (red dots and curve). Thicknesses and doping of a-Si:H films are relevant to achieve a properly working contact at p-c-Si/p-a-Si.H interface. The n-c-Si/n-a-Si:H is less critical, while the p-c-Si/p-a-Si:H contact needs particular care. Indeed only high doping values of p-a-Si:H layer can avoid a barrier formation against carrier transport, as evident comparing the blue dots and curve with the black ones.

Wafer doping and bulk lifetime play a role in interdigitated contact geometry as demonstrated by two dimensional numerical simulations of the IBC-BHJ device reported in [349], in which p-type c-Si wafer is adopted. As expected, J_{sc} reduces from 37mA/cm^2 by increasing the doping concentration from 10Ω-cm to 0.1Ω-cm due to bulk lifetime degradation in highly doped regions, where Auger mechanism dominates the recombination process. At the same time fill factor increases due to reduced bulk series resistance.

Figure 41 shows the effect of doping concentration on fill factor and cell efficiency for different bulk lifetime, taking into account a textured surface for the c-Si. In these simulations, the distance between the doped a-Si:H regions has been fixed at 100µm, and a p-type c-Si doping density of 5x10^{16}/cm^3 (0.5Ω-cm) should be preferred [330].

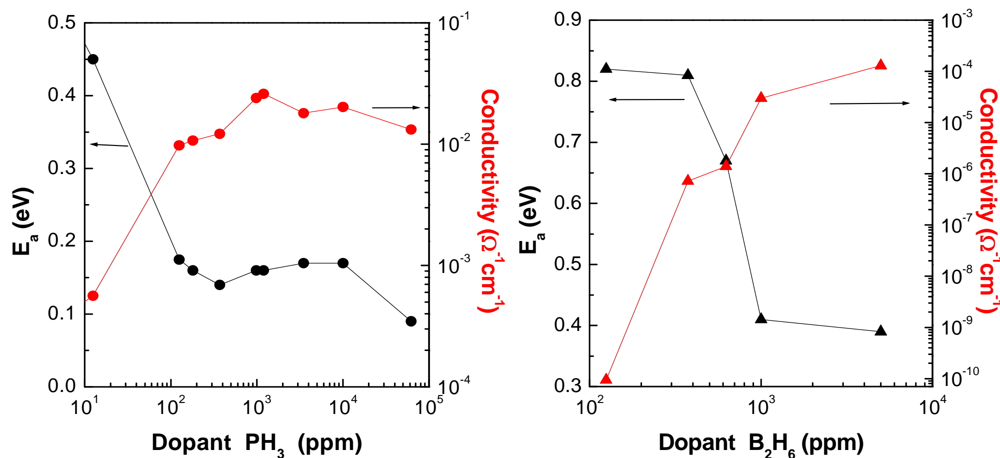


(a) (b)

Fig. 41 Simulation results on the effect of the p-c-Si wafer doping concentration on (a) fill factor (FF) and J_{sc}, and (b) efficiency (EFF) of an IBC-BHJ solar cell. As can be seen, preferred doping concentration is around 5x10^{16}/cm^3 (0.5Ω-cm). Fill factor and efficiency decreases beyond this concentration. Beyond the doping concentration of 5x10^{16}/cm^3, J_{sc} remains almost constant. The decrease in efficiency is due to the decrease in fill factor. Two different values of bulk lifetime are used in the simulations: 0.1ms and 1ms reported as circles and triangles respectively. Higher the bulk lifetime, better the cell performances. In this work, the distance between doped a-Si:H regions has chosen as 100µm.

5.2.2 a-Si:H doping

2220 Another asymmetry to be considered in device design is due to the difference between
2221 doping effectiveness of n- and p-type a-Si:H material. N-type (p-type) doping, obtainable by
2222 adding PH_3 (B_2H_6) to the SiH_4 in PECVD chamber during the plasma, ensures higher film
2223 conductivity and lower activation energy. In Fig. 42, activation energy and conductivities of
2224 p-and n-type a-Si:H films are reported as a function of dopant concentration in the gas
2225 mixture during the PECVD process [350]. Unfortunately, in doped a-Si:H thin layer, the
2226 thinner the film the higher the activation energy [351]. Therefore the choice of any emitter
2227 thickness should be carefully considered and verified to correctly design an IBC-BHJ solar
2228 cell.



2229

2230 Fig. 42 Left side: Dark conductivity and activation energy (E_a) of n-a-Si:H films versus phosphine (PH_3) content
2231 in the gas mixture during the film growth by PECVD. Rigth side: Dark conductivity and activation energy of p-
2232 a-Si:H films versus diborane (B_2H_6) content in the gas mixture during the film growth by PECVD. For both
2233 types of dopants, by increasing dopant concentration, activation energy decreases and conductivity increases.
2234 High film conductivity and low activation energy are required. Note that, thinner the film, higher the activation
2235 energy. In BHJ solar cells, doped a-Si:H is used as emitter. Therfore, to design BHJ solar cell, emitter thickness
2236 should be carefully chosen.
2237

2238 To improve the electrical properties of n-type a-Si:H layer, a chrome silicon (CrSi)
2239 formation on top of the amorphous film was suggested [336]. This CrSi can be obtained by
2240 depositing 30nm of Cr on doped a-Si:H and patterning it by wet chemical etch in a solution
2241 of 30g of cerium ammonium nitrate ($(NH_4)_2Ce(NO_3)_6$), 9ml CH_3COOH and 200ml of DI
2242 water. Activation energy reduction from 0.24eV down to 0.017eV was obtained. CrSi can
2243 also be useful in the case of p-type a-Si:H. Indeed the presence of the CrSi layer does not

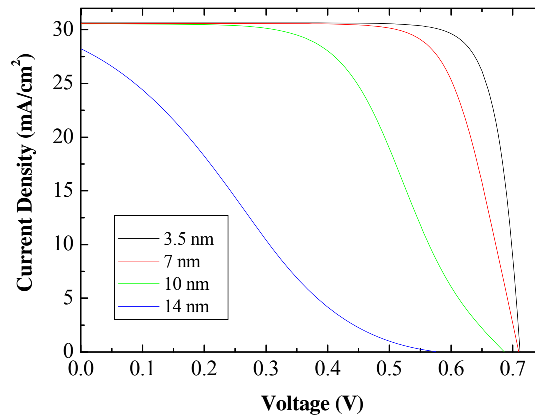
2244 affect the doping type of the doped a-Si:H film on which it is formed. Activation energy
2245 reduction from 0.36eV down to 0.14eV has been achieved [336]. This treatment improves the
2246 p-c-Si/i-a-Si:H/p-a-Si:H/p^+-a-Si:H heterojunction contact to form an effective ohmic contact,
2247 as shown in Fig. 40 [347]. Since both contacts are on the rear side of the cell the energy gap
2248 of the a-Si:H becomes less relevant. The a-Si:H film on the rear side does not work as a
2249 window layer. Therefore lower bandgap should be preferable in order to reduce the valence
2250 band offset at a-Si:H/c-Si interface, thus enhancing the charge collection as in the case of μc-
2251 Si:H cell [352]. Nevertheless the buffer layer should continue to be amorphous for better
2252 passivation of c-Si surface. On the other hand higher bandgap materials must be avoided as
2253 suggested in Ref. [13], otherwise the energy mismatch between the two valence bands at the
2254 heterojunction produces a high barrier that cannot be overcome by the electric field.

2255 5.2.3 Buffer layer - Intrinsic a-Si:H

2256 It is widely accepted that an effective heterojunction must have intrinsic, high quality
2257 a-Si:H buffer layer to passivate the c-Si surface and to separate the doped a-Si:H film
2258 [325,353]. Its thickness must be carefully optimized taking into account of the monohydrides
2259 (Si-H), dihydrides (Si-H_2) content at the beginning of the a-Si:H film deposition to avoid
2260 epitaxial growth [354]. Potential for further improvements are still under investigation to
2261 reduce the SRV [278, 355]. In the case of IBC-BHJ device, depending upon the patterning
2262 processes, the situation is more complex since the buffer layer should be the same for both
2263 base and emitter contacts. Two dimensional numerical simulations have been used to
2264 evaluate the effect of the buffer layer thickness. In Ref.[338] it is reported that increasing the
2265 i-a-Si:H buffer layer thickness, the light I-V characteristics under standard AM1.5G (G stands
2266 for global) condition are strongly affected resulting in a fill factor reduction. In the simulation
2267 a defect density of 10^{17}/cm^3/eV is homogeneously distributed along the buffer layer thickness.
2268 This effect is related to the recombination at the a-Si:H/c-Si interface. Indeed when the i-a-

Si:H layer becomes thicker, the p-type a-Si:H base contact is not able to collect the holes due to the valence band offset at the edge of a-Si:H/c-Si interface. These holes recombine through a-Si:H/c-Si interface defects, with electrons generated in the c-Si bulk and diffusing toward the n-type contact. This results in a barrier formation against carrier collection from the base contact. This recombination produces an S-shape in the I-V curve, such as coming from an anti-series double diode device. The simulated band bending at the edge of c-Si/i-a-Si:H/p-a-Si:H is already shown in Fig. 39. Of course the intrinsic layer cannot be completely removed otherwise the c-Si surface passivation in the region not covered by doped a-Si:H layer will be immediately lost [232]. However in IBC-BHJ, the c-Si rear side surface passivation is not the same as in the case of SHJ (i.e. front heterojunction) emitter. Indeed now the emitter region partially covers the buffer layer on the c-Si surface, while the other part is covered by the base contact HJ. A gap region between base and emitter contact also has to be considered, as evident from Fig. 38. This difference between SHJ and IBC-BHJ in surface passivation accounts for only ~ 2% of the fill factor change [234]. Moreover the higher the defect density within the buffer layer the stronger the undesired S-shape effect even for a relatively thin buffer layer.

The thickness of the intrinsic a-Si:H buffer layer is also important for consideration or improved performance. The thicker the buffer layer, the lower the cell fill factor as shown in Fig. 43. Increasing the buffer layer thickness from 3.5nm up to 14nm, a S-shape appears in the I-V characteristic. Further details concerning the two dimensional simulations shown in Fig. 43 can be found in Ref. [338].



2290

2291 Fig. 43 Simulated I-V curves as a function of intrinsic a-Si:H buffer layer thickness. By increasing buffer layer
2292 thickness from 3.5nm up to 14nm, an S-shape appears in the I-V characteristic. This effect refers to a barrier
2293 formation against carrier collections that forms at the heterojunction interface. Therefore very thin buffer layer
2294 should be adopted to obtain a proper working heterojunction device. On the other hand, buffer layer thickness
2295 should not be further reduced otherwise is very difficult to ensure a conformal coverage of Si surface. Moreover
2296 buffer layer thinner than 5nm does not represent a good choice. Indeed if this buffer is too thin, less than 5nm,
2297 surface passivation cannot be guaranteed, due to higher content of dihydrides (Si-H_2) radicals at the interface
2298 between c-Si and a-Si:H. A 5-7nm thick buffer layer represents the best choice for practical use.
2299

2300
5.2.4 Metal contacts

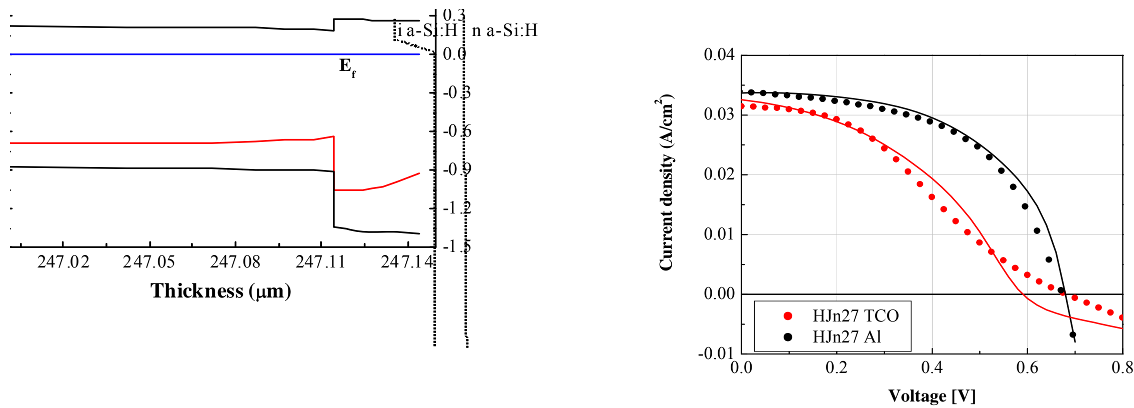
2301 The low conductivity of doped a-Si:H layer has a strong impact on IBC HJ cell. If the
2302 emitter region is not completely covered by any metal contact, the carriers have to travel
2303 laterally along the doped a-Si:H film to reach the metal electrode. The longer distance for
2304 lateral transport introduces resistance loss that results in fill factor reduction, whereas V_{oc} and
2305 J_{sc} are not affected by the reduction of the metal coverage. Numerical simulations of IBC-
2306 BHJ device reported in Ref. [349] show that decreasing the coverage ratio from 100% to 50%
2307 induces an absolute 5% reduction of fill factor, thus reducing the cell efficiency. Therefore
2308 the whole emitter area has to be contacted by a metal to achieve the best cell performance.
2309 Concerning the emitter coverage, the use of TCO represents a good choice to improve the
2310 lateral conductivity of the very low doped a-Si:H layers. This is because CrSi may not be
2311 sufficient to guarantee a sufficient lateral conduction if the metal contact is narrower than the
2312 emitter region.

2313 The challenge of TCO patterning without any photolithography processes remains. Up
2314 to now the most promising technologies are the use of physical shadow mask during the

2315 sputtering process [338, 340] and the laser ablation after TCO deposition [339].

2316 The choice of the electrodes deposited on both contacts represents another relevant
2317 issue. Indeed the electrode work function can affect the doped a-Si:H layer conductivity. In
2318 principle the n-type a-Si:H should be sufficiently thin to avoid series resistance enhancement
2319 and sufficiently doped to avoid depletion induced by the electrode contact due to the work
2320 functions not aligning within the a-Si:H layer. As an example, if the Fermi level assumes a
2321 distance of 4.2eV from the vacuum level to the edge of n-type a-Si:H emitter, work function
2322 of the electrode should not exceed that value to avoid depletion in the a-Si:H layer when in
2323 contact with that electrode, otherwise a Schottky barrier contact arises. This again deforms
2324 the light I-V characteristics introducing a S-shape.

2325 A comparison of band bending distributions at the rear side of the cell is reported in
2326 Fig. 44, as obtained by numerical simulations. Here two different work function values of 4.3
2327 eV (black for Al), and 4.6 eV (Red for TCO) have been applied as rear side metal contact of a
2328 n-c-Si/i-a-Si:H/n-a-Si:H heterostructure, keeping the same doping and density of state
2329 distribution within the n-type a-Si:H layer. The work function were simulated by fixing the
2330 Fermi level at the edge of the n-a-Si:H layer where the metal contact would be. As evident
2331 from Fig. 44, a depletion occurs in both n-type c-Si and a-Si:H that reflects in a barrier
2332 formation for the electrons being collected by the metal contact. This barrier results again in a
2333 S-shape in the light I-V characteristic as reported in Fig. 44 as continuous lines and compared
2334 for two different cells. The metal electrode has been varied from Al (work function = 4.3eV)
2335 to TCO (work function = 4.6eV). Also on the p-type a-Si:H layer an undesired depletion
2336 effect can be obtained if an uncorrected metal work function is chosen.

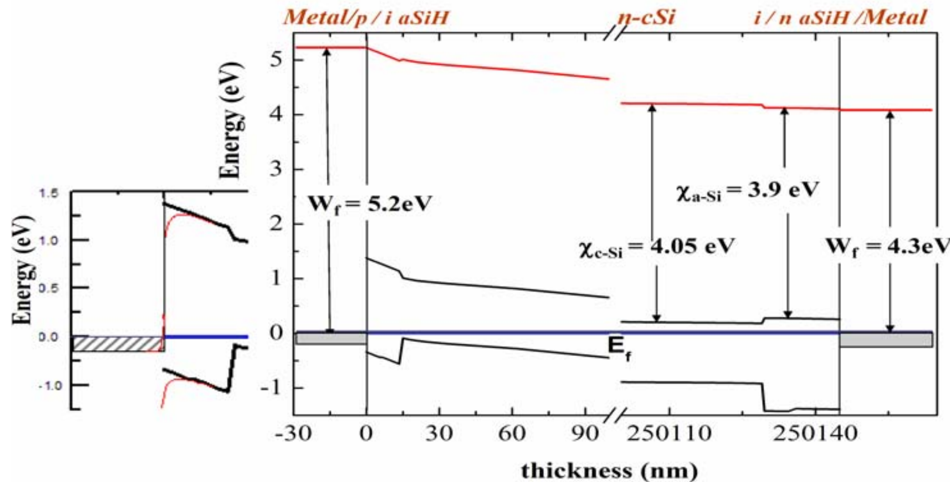


2337

2338 Fig. 44 Left side: Numerical simulations of band bending distributions of n-c-Si/i-a-Si:H/n-a-Si:H rear side of
2339 heterojunction solar cell, in which the work function of the metal contact to the n-a-Si:H has been varied from
2340 4.3 eV (black for Al) to 4.6 eV (red for TCO). Moreover black lines in the band diagram shifted a bit downward
2341 due to an electron accumulation (inside the barrier) induced by the metal work function. The barrier formation
2342 results in a S-shape light I-V curve (right side) reported as continuous lines; Right side: Comparison between
2343 experimental (dots) and numerically simulated (line) I-V characteristics under sun-light illumination of n-c-Si/n-
2344 a-Si:H rear side of heterojunction solar cell in which the work function of the metal contact to the n-a-Si:H has
2345 been varied from TCO = 4.6eV (red) to Al = 4.3eV (black).

2346

2347 To reach the highest efficiency, metal work function close to 4.3eV and 5.2eV should
2348 be used in case of n- and p-type a-Si:H regions, respectively [346]. According to this
2349 approach the built-in voltage of the device also can increase leading to higher V_{oc} values
2350 [327]. Band bending simulation of the n-type c-Si based a-Si:H/c-Si heterojunction cell with
2351 two different metals work function (5.2eV and 4.3eV) for the emitter and base contact
2352 respectively is shown in Fig. 45. This simulation refers to a HJ device able to reach V_{oc} of
2353 760mV and efficiency of 25%. At the left side the band bending at the edge between metal
2354 and p-type a-Si:H is magnified to remark the undesired band bending distribution when metal
2355 work function lower than 5.2eV is used for the contact.



2356

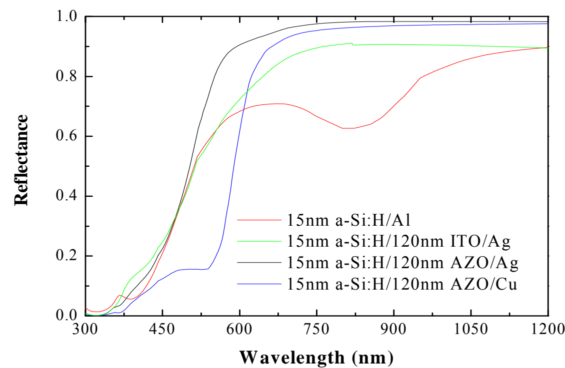
2357 Fig. 45 Band bending simulation of the n-type c-Si based a-Si:H/c-Si heterojunction cell. This simulation is for
2358 heterojunction device with V_{oc} and efficiency of 760mV and 25% respectively. Two different metals with work
2359 function (W_f) of 5.2 eV and 4.3 eV are adopted for the emitter and base contact respectively. These metals have
2360 the same effect of TCO films from the work function point of view. For small area (lab scale) devices, metal
2361 work function is not an issue. At the left side, the band bending at the edge between metal and p-type a-Si:H is
2362 magnified to illustrate the undesired band bending distribution when metal work function lower than 5.2 eV is
2363 used for the contact. Here, electron affinity and Fermi energy are denoted by E_f and χ respectively.

2364

2365 While at lab scale metal work function does not represent a problem, since different
2366 metals are commonly available and small area samples requires thin layers, the situation
2367 become more complex when production moves to industrial scale. Thicker layer due to large
2368 area device and low-cost metallization processes are needed to be competitive. Towards this,
2369 it is useful to look at the front heterojunction cell manufacturing process where the device
2370 commonly has two TCO for both front and rear side of the cell. TCO layers are usually
2371 obtained by magnetron sputtering, which is a standard technology for large area solar cell.
2372 Even if the TCO is also useful to work as anti-reflection coating, its resistivity around 10^{-4} Ω-
2373 cm is not sufficient to ensure lateral collection without introducing series resistance. Then Ag
2374 metal grids are needed to complete the cell. This metal is commonly using through screen
2375 printing process with thermal sintering at temperature below 200°C [346]. This technology
2376 can be applicable also to the IBC-BHJ device due to the low thermal budget required.

2377 Several TCOs such as Al-doped ZnO (ZnO:Al) and ITO can fit the work function
2378 requirements. In particular ITO can offer the possibility to tune the work function depending

2379 on the deposition conditions [356] as well as the amount of indium within the In_2O_3 target of
2380 the magnetron sputtering system. A 90% In_2O_3 and 10% SnO_2 result in work function of 5.5
2381 eV and 4.8eV respectively [357]. Moreover in the case of IBC-BHJ device, the TCO
2382 positioned on the rear side of the cell does not work as anti-reflection coating and thus may
2383 be thicker leading to a lower sheet resistance. Nevertheless the rear side contact should also
2384 work as mirror to reflect infrared radiation inward towards the cell, thus enhancing the light
2385 trapping. ZnO:Al/Ag contact represents a better choice with respect to ITO/Ag or Al. ITO or
2386 ZnO:Al also represent a good substrate to Cu plating applications to replace the expensive Ag
2387 layer. In Fig. 46, inward reflectance in the c-Si wafer from different rear side metal contacts
2388 are compared. All these reflectance curves are obtained using optical simulation software
2389 [358]. It is interesting to note that 15nm a-Si:H/Al as back contact does not form an optimum
2390 mirror due to the Al absorption in the wavelength range between 750nm and 1000nm. Cu and
2391 Ag are seen to behave quite similar as mirror in the near infrared portion of the spectrum
2392 between 900nm and 1200nm.



2393
2394 Fig. 46 Inward reflectance in the c-Si wafer from different rear side metal contacts. Al is not the best choice due
2395 to infrared absorption, while Cu and Ag act similar from 900nm to 1200nm. This reflectance is simulated with
2396 the aid of a numerical model developed in x-ray oriented programs (optical simulation software). Red curve
2397 shows that back contact formed by 15nm a-Si:H/Al shows an infrared wavelength absorption. Back contact
2398 should act as mirror, and should reflect infrared wavlenght towards bulk. That is, to enhance light trapping, rear
2399 side contact should reflect infrared radiation towards the bulk of c-Si wafer. ZnO:Al/Ag (i.e. AZO/Ag) is a
2400 better choice than ITO/Ag or ITO/Al. Also, Cu plating can be done easily over ZnO:Al. Therefore, an expensive
2401 Ag layer can be replaced easily by Cu.

2402
2403 Contact resistance contributes to series resistance. Contact resistance can be evaluated

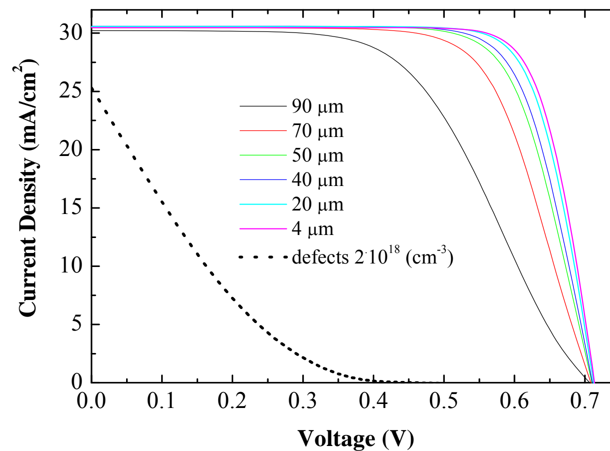
2404 with the aid of two-dimensional (2D) numerical model of the IBC-BHJ cell. To achieve cell
2405 fill factor as high as 83%, a specific contact resistivity of 0.01Ω-cm for both emitter and BSF
2406 contacts should be obtained. Higher contact resistances of 0.1Ω-cm and 1Ω-cm will lead to a
2407 fill factor of 80% and 54%, respectively [349]. Higher values of these parameters induce an
2408 S-shape in the light I-V sun lighted characteristic.

2409 Different metallization approaches have been proposed on a laboratory scale.
2410 According to the previous discussion, industrial production on large area metallization must
2411 fit cell cost and throughput. Since the heterojunction cells can only withstand temperatures
2412 lower than 300°C, screen printing using low-temperature sintering Ag pastes or metal plating
2413 are the only available alternatives. Both these techniques require an interlayer such as TCO
2414 [259] or evaporated metal [333] between the doped a-Si:H film and top metal (i.e. Ag paste)
2415 to fit the work function requirement, and to ensure metal adhesion.

2416 5.2.5 Distance between doped regions - gap between IBC contacts

2417 In IBC-BHJ cells the primary fill factor loss is due to lateral current flow. Indeed the
2418 emitter fingers should be much wider than base fingers for efficient minority-carrier
2419 collection; therefore the majority carrier collection is subject to more resistance losses [217].
2420 J_{sc} increases by about 3 mA/cm^2 as the emitter coverage increases from 50% to 95%, because
2421 of the increased area. The same effect is also demonstrated in a back-contacted diffused
2422 junction solar cell [359]. Fill factor increases along with emitter coverage up to a certain
2423 value and then decreases because of the increased series resistance related to the longer travel
2424 of the majority carriers to be collected in the base contact, and to the reduced width of the
2425 base. To better understand this issue several structures have been simulated having different
2426 distance between the two doped a-Si:H contacts. The simulated I-V characteristics in Fig. 47
2427 refer to distance varying between 4μm to 90μm. All the other parameters such as SRV, defect
2428 density at the interface, and doping density of the doped regions have been kept constant. To

2429 achieve the best efficiency the distance between doped contacts should be as short as
2430 possible. Increasing that distance results in a decrease in fill factor. This effect is due to the
2431 absence of electric field in crystalline region covered only by the intrinsic a-Si:H layer. The
2432 photogenerated carriers flowing into these regions cannot escape from c-Si/a-Si:H interface
2433 recombination. Indeed if the density of states in the i-a-Si:H layer were increased by one
2434 order of magnitude from $1x10^{17}/cm^3$, recombination will be stronger and its effect on the I-V
2435 characteristic will be dramatic, as evident looking at the dotted black characteristic reported
2436 in the Fig. 47 [338]. In practice it is difficult to obtain a distance between the two doped
2437 contacts as short as 4 μm without any photolithographic process.



2438

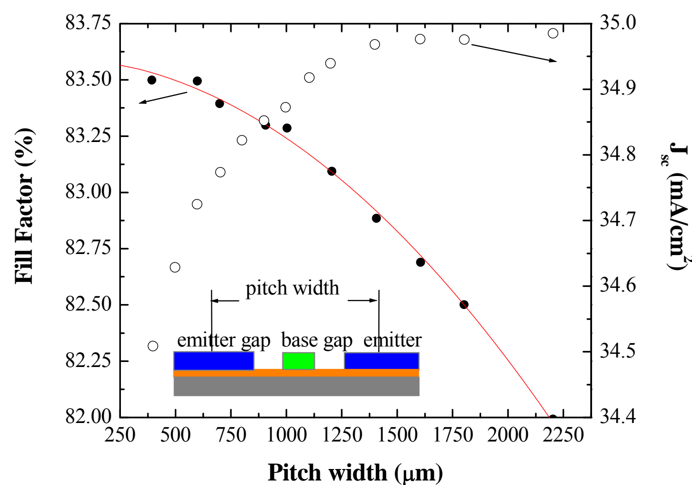
2439 Fig. 47 Influence of gap distance between the emitter and base contacts and the influence of defect density
2440 within the buffer layer. The simulated I-V characteristics refer to distance varying between 4mm to 90mm. All
2441 the other parameters such as as SRV, defect density at the interface and doping density of the doped regions
2442 have been kept the same for all the simulated distances. To achieve the best efficiency the distance between
2443 doped contacts should be as short as possible. Increasing that distance, a reduction of fill factor occurs, due to
2444 the reduction of electric field intensity within crystalline region covered by the intrinsic a-Si:H layer. If the
2445 density of states in the i-a-Si:H layer is increased to an order of magnitude from $1x10^{17}/cm^3$, the recombination
2446 would be stronger and its effect on the I-V characteristic would be dramatic as evident looking at the back
2447 dotted I-V curve.

2448

2449 Keeping the gap width fixed at 100μm, simulations show that increasing the base
2450 contact width, the J_{sc} quadratically decreases from 34 mA/cm^2 at 100μm down to 30 mA/cm^2
2451 at 750μm due to recombination at interface n-c-Si/i-a-Si:H/n-a-Si:H, which reduces the
2452 number of carriers able to reach the emitter region [349].

2453 To better define the rear side geometry of an IBC-BHJ solar cell, a definition of pitch

2454 as the sum of the base, the gaps and the emitter width, is used. Commonly it is in the
2455 millimetres range. From simulations it is possible to determine the optimum pitch,
2456 corresponding to the maximum cell efficiency, which is in the range between 600µm and 900
2457 µm. This optimum value is determined as a trade-off between emitter coverage and series
2458 resistance losses due to the increased lateral distances. While the pitch weakly influences the
2459 J_{sc} that instead strongly depends on SRV, in turn it affects the fill factor as shown in Fig. 48.
2460 As can be seen in Fig.48, fill factor quadratically decreases as pitch width increases as shown
2461 by the parabolic red curve fitting the simulation data. These data refer to simulations in which
2462 the base contact and gap widths were set at 150µm and 50µm respectively. J_{sc} data refers to a
2463 SRV of 50cm/s arising from a front surface field [360]. Instead, Mingirulli et al. [232]
2464 reported that to achieve the efficiency of 20%, suggests gap, base contact and emitter width
2465 in the ratio: 12%, 28% and 60% respectively of the pitch.



2466
2467 Fig. 48 Fill factor (line) and J_{sc} (symbols) as a function of pitch width resulting from numerical simulations.
2468 Continuous red line shows the quadratic behaviour of the fill factor versus pitch width. In the inset, a sketch of
2469 pitch width definition is shown. In the simulation, base width and gap width were set at 150µm and 50µm
2470 respectively. By increasing pitch width about an order of magnitude from 250µm, J_{sc} increased slightly, being
2471 weakly influenced by pitch width. Whereas fill factor decreases quadratically as pitch width increases. J_{sc} data
2472 corresponds to a surface recombination velocity of 50cm/s. Maximum efficiency corresponds to a pitch width
2473 between 600 and 900µm.
2474

2475 ### 5.2.6 Front surface

2476 Since the carriers are mostly generated close to the front side of the cell and the

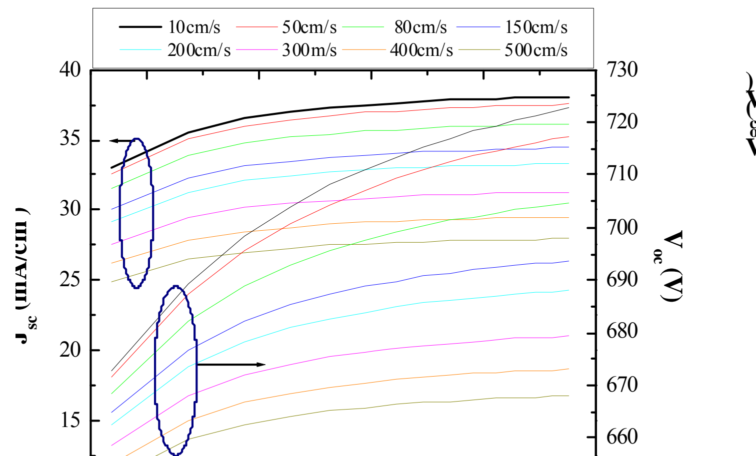
2477 diffusion mechanism toward the back contact is the only way for the collection, the front side
2478 plays a very relevant role in IBC-BHJ cells. An effective front surface passivation is strongly
2479 needed to reduce the SRV, and achieve high-efficiency. From numerical simulations of IBC-
2480 BHJ solar cell, reported in Ref. [360], it is evident that both J_{sc} and V_{oc} are affected by the
2481 front side SRV. In particular, increasing the SRV from 0 to 1000cm/s, the J_{sc} and V_{oc} reduce
2482 from $36mA/cm^2$ to $15mA/cm^2$ and from 760mV to 660mV, respectively, thus reducing the
2483 cell efficiency. The fill factor does not seem to be very strongly influenced. An anti-reflection
2484 coating able to ensure low front SRV can be achieved by SiN passivation, or even more
2485 promising, using a-Si:H/SiN stack double layer [335], or SiO_2/SiN [232]. A front SRV as low
2486 as 10cm/s on p-type was demonstrated in Ref. [213 ,361]. Moreover SiN deposited on front
2487 side of n-type c-Si surface layer can also form a front surface field due to the electron
2488 accumulation induced by the positive charge lying within the SiN film [362].

2489 In principle the use of a front surface field can be very useful to achieve an effective
2490 surface passivation. In Ref. [213] the impact of the front SRV on the QE of IBC cell has been
2491 demonstrated leading to the conclusion that the SRV affects more the cell fabricated on
2492 higher doped c-Si base. As an example, a J_{sc} of $38.5mA/cm^2$ can be achieved for base doping
2493 concentration of $10^{14}cm^{-3}$ even in case of SRV = 40000cm/s, whereas the same SRV reduces
2494 the J_{sc} to less than $30mA/cm^2$ for base doping concentrations of above $7x10^{15}cm^{-3}$.
2495 Calculations have shown that front surface field on lower base doping results in higher J_{sc} and
2496 reduce the influence of the front SRV [213]. This result is relevant for industrial cell
2497 manufacturing, where good passivation on large areas is still difficult to attain [360]. In
2498 practice it is easier to perform a good passivation on FSF fabricated by light phosphorous
2499 diffusion on n-type c-Si wafer, as suggested in Ref. [232], with respect to light boron
2500 diffusion on p-type c-Si wafer [363]. In turn this approach to the front surface field is in
2501 contrast to the primary goal of achieving a full low-temperature (< 200°C) process able to

2502 reduce the cell manufacturing cost at industrial scale. On the other hand, J_{sc} as high as 38.5
2503 mA/cm^2 have been presented by LG [343] using a n-type a-Si:H/i-a-Si:H front surface field.
2504 In this case, however, an undesired absorption within a-Si:H film occurs that reduces the J_{sc}
2505 of at least 1mA/cm^2. Therefore the use of higher bandgap n-type thin-film to form an
2506 effective front surface field is highly desirable. Doped SiO_x film obtainable by PECVD
2507 process [364] can be a valid solution to overcome the undesired absorption at the front side.

2508 The key issue to obtain high J_{sc} depends not only on SRV but also on diffusion length,
2509 in the bulk c-Si wafer. The effect of both parameters has been explored in Ref. [333], in
2510 which the J_{sc} and V_{oc} of the cell have been simulated by varying the diffusion length and front
2511 side SRV, as depicted in Fig. 49. A numerical model based on PC1D software [365] suggests
2512 that the front side SRV has a greater effect on device performances than diffusion length.
2513 Indeed while a diffusion length of 500μm is acceptable to collect the photogenerated carriers
2514 over the entire light spectrum ranging from 350nm to 1200nm, SRV values higher than
2515 100cm/s strongly decreases the J_{sc} values, thus reducing the advantage of front metal grid
2516 absence. To obtain high-efficiency solar cell on a p-type 200μm thick c-Si wafer, the model
2517 suggests that SRV as low as 10cm/s and diffusion length around 1 mm are needed to achieve
2518 J_{sc} and V_{oc} values of 38mA/cm^2 and 720mV, respectively. A diffusion length value of 1mm
2519 corresponds to a 300μs of bulk lifetime. To obtain the same diffusion length on n-type doped
2520 c-Si wafer, a 1ms bulk lifetime is required [329] because of lower mobility of holes compared
2521 to that of electrons.

2522



2523 Fig. 49 PC1D simulations of J_{sc} and V_{oc} values as a function of diffusion length for different values of front side
2524 surface recombination velocity. These values are chosen in the range between 10cm/s and 500 cm/s. While the
2525 former refers to very good Si surface passivation, and the latter refers to a surface passivation commonly
2526 achieved in the cell production line. Front surface recombination velocity has more influence on device
2527 performance than diffusion length, and a high J_{sc} depends on these two parameters. To collect photogenerated
2528 carriers over the spectrum range between 350 and 1200nm, a diffusion length of at least 500µm is required.
2529 When surface recombination velocity >100cm/s, J_{sc} decreases strongly and reducing the advantage of grid-less
2530 front surface.

2531

2532 5.2.7 Towards high-efficiency

2533 Currently the highest IBC-BHJ cell efficiency of 25.6% has been demonstrated by
2534 Panasonic [344]. This result overcomes the 25% efficiency barrier in place for many years in
2535 a lab device obtained through photolithography steps [366]. It is interesting to note that this
2536 record has been obtained on very large area device (143.7cm^2), and therefore is closer to
2537 production line than laboratory scale. Moreover this result demonstrated that the IBC-BHJ
2538 concept is among the most promising approach to achieve the highest efficiency on c-Si
2539 based solar cell. Since the record cell shows V_{oc} a bit lower than the maximum reached on
2540 HIT cell [325], there is room to further improve the IBC-BHJ cell.

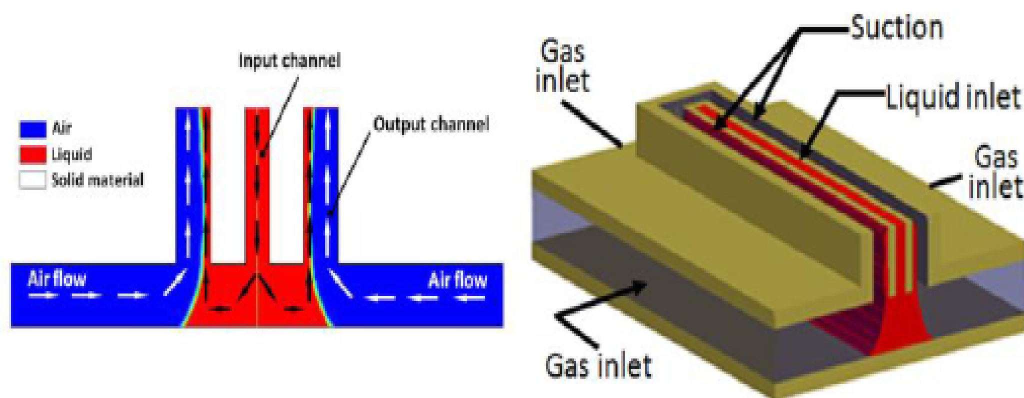
2541 Record efficiency higher than 25% can be achieved if the cell fill factor will reach a
2542 value of 83%, as obtainable reducing the cell pitch and the contact resistance between metal
2543 electrodes and a-Si:H layers. But if the IBC-BHJ cell achieves fill factor values lower than
2544 83% then the cell V_{oc} must be enhanced to compensate for the lower fill factor. Even though

2545 V_{oc} value as high as 750 mV has been recently demonstrated by Sanyo-Panasonic on
2546 conventional transverse heterojunction cell, the same V_{oc} seems not easy to achieve due to
2547 difficulties in performing a surface passivation of the gap between the two contacts able to
2548 nullify the SRV.

2549 5.3 Future direction

2550 The way to reduce the Si based solar cell cost and then the PV market price is
2551 represented by thickness reduction of Si wafer down to 100μm. On this thin wafer, low
2552 thermal budget technologies should be applicable to avoid wafer warping due to thermal
2553 stress. Si heterojunction device represents a valid choice as already demonstrated by Sanyo-
2554 Panasonic even on thin wafer [367]. Nevertheless Si heterojunction technology has three
2555 important unresolved issues. The first is the use of ITO, which is not available for very large
2556 cell production due to the presence of rare indium. The second is the Ag screen-printed pastes
2557 for the electrodes; indeed Ag cost has not been reducing as the rest of the cell, and accounts
2558 for about 30% of the total cell cost [368]. The third is the connection between cells within the
2559 module now ensured by conductive tape that introduced large series resistance. IBC-BHJ cell
2560 represents a potential solution for these issues. ITO can be potentially successfully replaced
2561 by ZnO:Al since the lateral conductivity is not an issue due to subsequent metallization. In
2562 order to reduce the cell cost, the Ag screen-printed contacts must be replaced by Cu plating.
2563 With respect to conventional solar cells, in which the front side grid shrinks to dimensions
2564 lower than 80μm to reduce the shadowing effect and material cost, the IBC device has lower
2565 geometrical constraints. Therefore the use of metal plating, in principle, should be easier to
2566 manage. But the adhesion of plated Cu still represents an issue that can be overcome by
2567 interlayer insertion such as nickel (Ni) or tin (Sn). Moreover the large amount of chemicals
2568 waste produced by the metal plating baths still represents environmental and cost concerns
2569 for the industry. To overcome this problem an innovative solution has been recently proposed

2570 in Ref. [369]. It is based on locally plating by dynamic liquid meniscus formation, as depicted
2571 in Fig. 50. With the aid of this meniscus all the wet chemical technologies can be performed,
2572 such as local plating, etching and deposition from liquid phase. Since the liquid meniscus is
2573 only locally in touch with the wafer, it can be used to deposit Cu or other metals only where
2574 there is a specific necessity, thus strongly reducing the waste chemicals produced by
2575 conventional light induced plating systems [370]. With the aid of this new approach the metal
2576 contact of the IBC-BHJ may potentially not represent an issue [369]. The problem related to
2577 low fill factor of PV module due to the cell interconnection, conventionally made by
2578 conductive tape between the heterojunction within the module, can be easily overcome in
2579 IBC cell.



2580
2581
2582 Fig. 50 Schematic diagram of dynamic liquid meniscus formation in touch with the substrate. From the pictures
2583 it is evident that the red fluid flowing from the center inlet is recalled back through suction at the left and right
2584 outlet. Therefore the fluid in contact with the substrate is always refreshed. With the aid of this meniscus all the
2585 wet chemical technologies can be performed, such as local plating, etching and deposition from liquid phase.
2586 Since the liquid meniscus is only locally in touch with the substrate, it can be used to deposit Cu or other metals
2587 only where there is a specific necessity, thus strongly reduce the waste chemicals always produced by
2588 conventional light induced plating systems. With this new approach, an issue related to low fill factor of PV
2589 module can easily be solved.
2590
2591 The design of module can be completely rewritten taking into account that both
2592 contacts are now on the same side of the cell. Therefore the IBC cells can potentially be done
2593 on a low-cost printed circuit board, instead of a conventional mylar sheet, where two
2594 interdigitated comb shape metal strips can ensure larger contact area between cells and

2595 interconnections with respect to conventional ribbons. This can enhance the cell fill factor
2596 and the overall module efficiency.

2597 6.0 III-V multi-junction on c-Si

2598 Significant effort has been undertaken till date to reduce the cost of multi-junction
2599 solar cell (MJSC) technology by developing methods to manufacture them on low-cost
2600 wafers. The integration of III-V semiconductors on c-Si aims to improve efficiency and to
2601 solve the limitations encountered with other wafers such as germanium (Ge) or gallium
2602 arsenide (GaAs).

2603 This review section focuses on the most relevant work done in the last years on the
2604 integration of III-V semiconductors on c-Si for the manufacture of multi-junction solar cells.
2605 Current state-of–the-art of the two most important techniques (epitaxial growth and wafer
2606 bonding) used for such integration are discussed. In addition to highlighting the most novel
2607 results obtained with each technology, current challenges and possible strategies to overcome
2608 them are also pointed out.

2609 6.1 Introduction

2610 MJSCs have demonstrated significant potential to reduce the cost and increase solar
2611 cell efficiency. Concentrator PV systems based on multi-junction solar cells boosts electricity
2612 generation and are expected to reduce the cost of PV.

2613 The first key for the success of this technology lies in the ability to make affordable
2614 PV cells with very high-efficiency. Using concentration, the maximum conversion efficiency
2615 that can be achieved by a PV device with a single p-n junction on c-Si is 44% [371] for cells
2616 made from a material with an optimal bandgap (E_g ~1.3 eV). MJSCs are formed by stacks of
2617 several p-n junctions connected in series, each of which is intended to transform a portion of
2618 the solar spectrum into electrical energy with minimum losses. The ultimate efficiency of

MJSC with an infinite number of junctions is 86% [371], almost twice of that of cells with a single-junction. The second key factor for its success lies in the existence of a family of materials, namely III-V semiconductors, with excellent PV properties and ranges of suitable bandgaps to implement MJSCs.

The integration of III-V semiconductors on Ge has been successfully investigated in the last two decades. A MJSC on Ge has recently beaten the efficiency record for any PV device, achieving efficiency close to 42% [372]. However, the exploration of alternative wafers to Ge continues because of the shortage and relatively high costs of Ge.

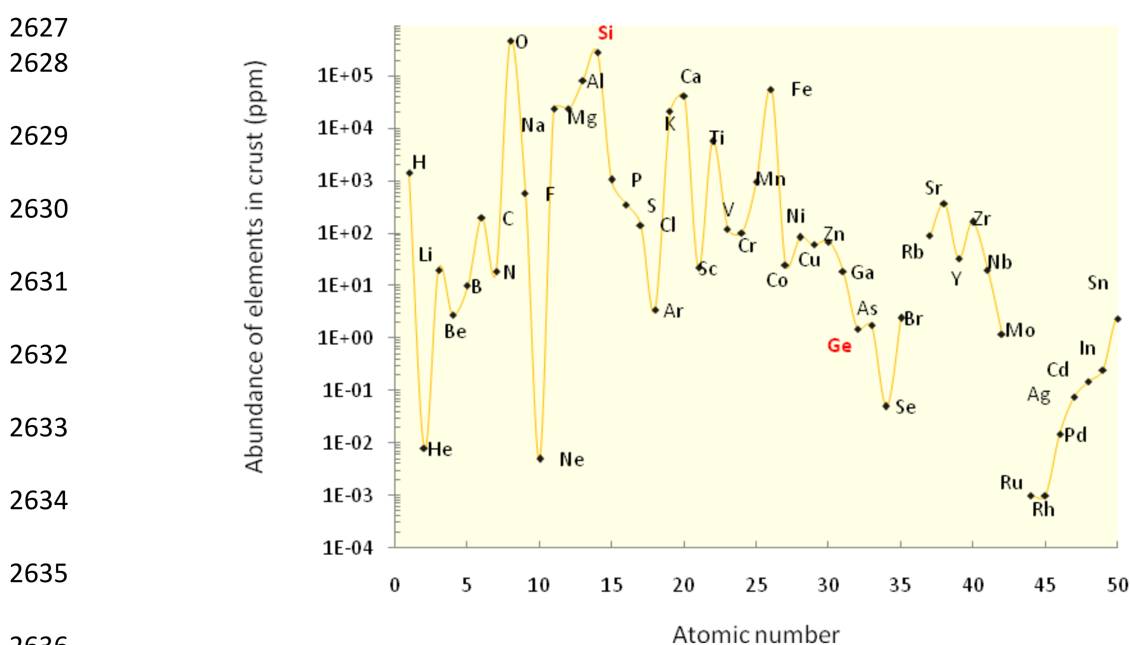


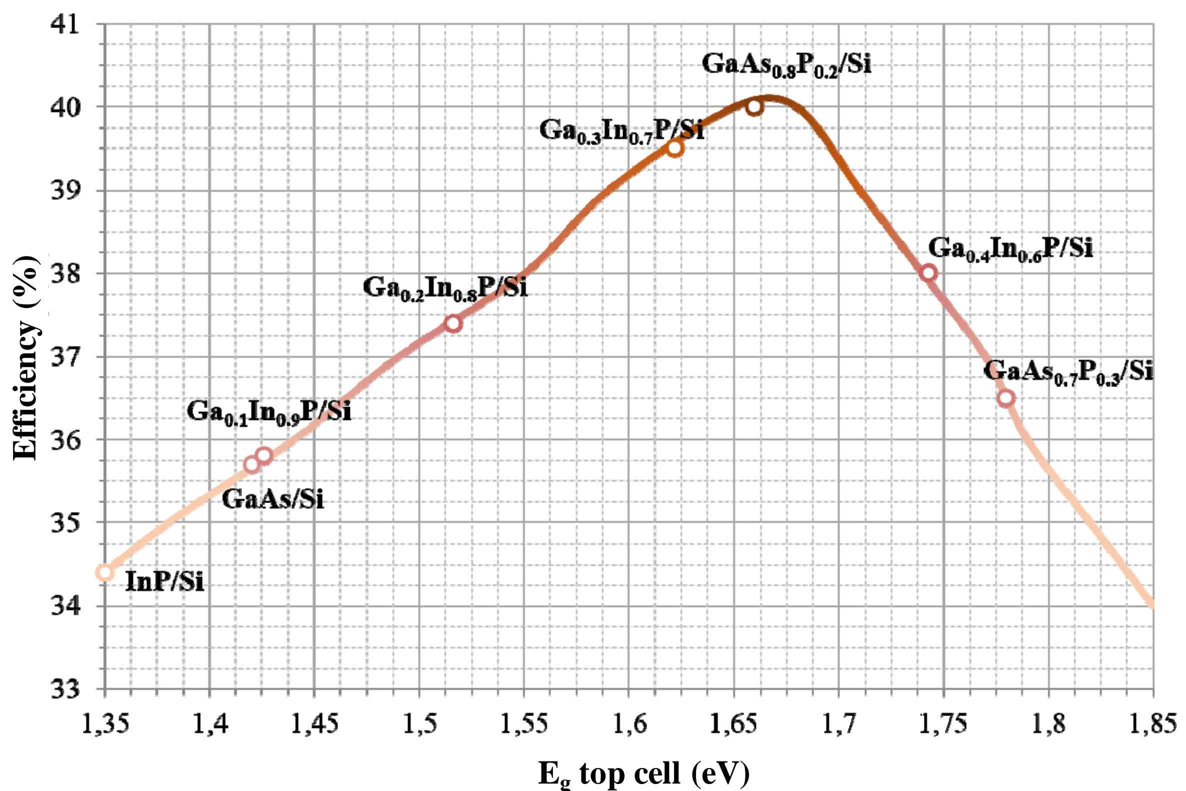
Fig. 51 Abundance of some elements in the Earth's crust versus atomic number. The graph evidences the abundance difference existing between the Si and Ge (highlighted in red) in the Earth's crust. Si is more abundant than Ge by a factor of $2x10^5$. This difference turns into a big discrepancy in terms of the material cost and thus, the selection of Si as an alternative to Ge is clearly justified. Also, semiconductor devices are fabricated using Si, a unique electronic and PV material. An ideal candidate for multi-junction solar cells is Si. Data taken from [373], David R. Lide, ed., CRC Handbook of Chemistry and Physics, 85th Ed., CRC Press, Boca Raton, Fla., Taylor & Francis Group, 2005.

Figure 51 represents a plot of the abundance of some elements [373] in the Earth's crust versus their atomic number. This plot shows that Si is a factor of $\sim 2x10^5$ times more abundant than Ge in the Earth's crust. Accordingly, the ideal candidate on which to manufacture multi-junction solar cells is c-Si (Fig. 51), the ubiquitous electronic and PV

2648 material. Indeed about 95% of semiconductor devices are presently fabricated using c-Si
2649 [374].

2650 According to the iso-efficiency contour maps for concentrated light depicted by
2651 Wanlass et al. [375] for a double-junction solar cell, theoretical efficiencies between 34 and
2652 40% can be achieved with a c-Si bottom cell if an appropriate material with bandgap ranging
2653 from 1.34eV to 1.84eV is used for the top cell. Figure 52 makes evident that there is a wide
2654 variety of III-V materials that meet this requirement. Hence the challenge is to develop
2655 strategies to grow them with good PV quality on a c-Si wafer, which in turn has to be
2656 processed to obtain an equally good performing bottom cell.

2657



2658
2659 Fig. 52 Theoretical efficiency of double-junction solar cells grown on c-Si wafer as a function of top cell
2660 bandgap. For top cell, an appropriate material is required with bandgap ranging between 1.34 and 1.84eV.
2661 According to this graph, the maximum theoretical efficiency can be obtained for III-V/c-Si double-junction solar
2662 cell by using gallium arsenide phosphide (GaAsP) as top cell with arsenic content of 0.8%. This GaAsP/c-Si
2663 couple has an excellent bandgap combination for maximimum utilization solar spectrum. Data from [375],

Wanlass M W, Coutts T J, Ward J S, Emery K A, Gessert T A, Osterwald C R., Advanced high-efficiency concentrator double-junction solar cells, Proc. 22nd IEEE PVSC (Alaska) 1991.

6.2 Challenges and difficulties

The integration of III-V semiconductors on c-Si has been a long-sought desire by the microelectronic industry [374,376]. In the PV field, the integration of III-V compounds on c-Si was intensively investigated in the 1990s, achieving good results [377-379]. Here, it is worth mentioning the works reported by Fitzgerald's group at the Massachusetts Institute of Technology, U.S.A., Umeno's group at the Nagoya Institute of Technology, Japan. All these groups demonstrated the production of solar cells with efficiencies above 20% by following a variety of approaches. Despite the excellent results published for an AlGaAs/c-Si solar cell with a V_{oc} of 1.57 eV, J_{sc} of 23.6mA/cm^2 and efficiency up to 20% [380], the technology was not transferred to industry, possibly due to reproducibility issues or complexity in the process.

In spite of these excellent results, the intensity of research declined considerably during the late 1990's due to the difficulties in improving material quality, and the rapid progress of Ge based MJSC technology. The above groups pointed out that the main challenges for III-V heteroepitaxy on c-Si are: (i) lattice mismatch, (ii) mismatch in thermal parameters, and (iii) defect confinement. In the following sub-sections, we review each of these challenges in detail.

6.2.1 Lattice mismatch

The obvious problem for III-V heteroepitaxy on c-Si has been the lattice mismatch between epilayer and wafer (Fig.53). For instance, the lattice constants of c-Si and GaAs– the two materials whose integration has been long sought, differ by around 4%.

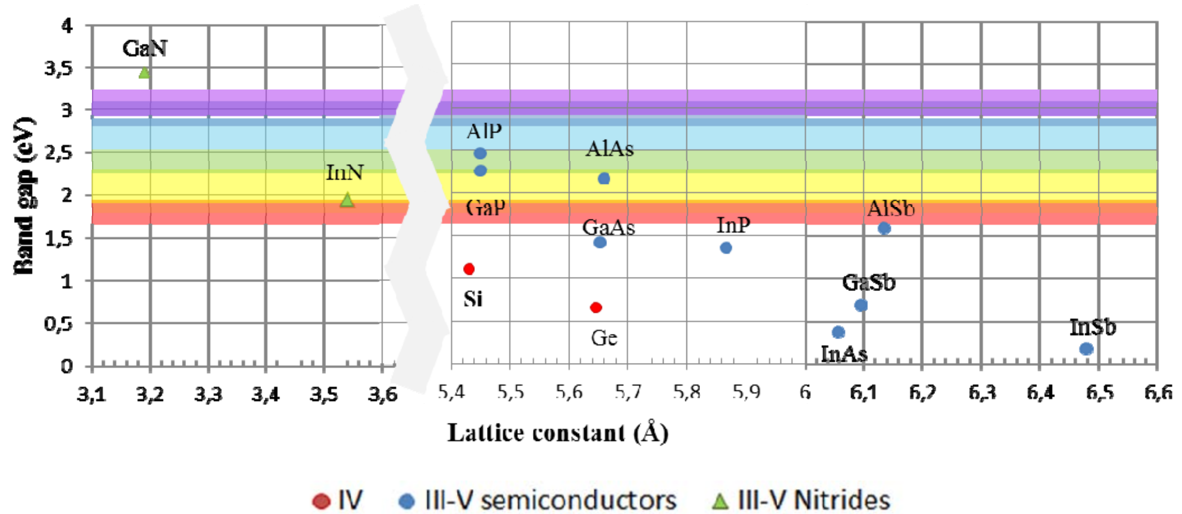


Fig.53 Room temperature bandgap versus lattice constant of common elemental and binary compound semiconductors. Lattice mismatch is an issue between epilayer (III-V, fro example GaAs) and c-Si wafer. This plot evidences the lattice mismatch between gallium arsenide (GaAs) and c-Si, and a small difference between gallium phosphide (GaP) and c-Si lattice constants. Lattice mismatch between GaAs and c-Si is around 4%. Epitaxial growth can accommodate lattice mismatched materials either by growing strained material or by growing material relaxed to its lattice constant. Multi-colored band in the figure is the energy range corresponding to visible spectrum.

Therefore, the development of strategies for epitaxial growth, which can accommodate this difference, has received special attention. These strategies consider either growing the material compressed/strained (i.e. pseudomorphic material) [381,382], or by growing the material relaxed to its natural lattice constant (i.e. metamorphic material) [383-387].

6.2.2 Mismatch in thermal parameters

One of the major problems for the growth of III-V materials on c-Si has been managing the different thermal properties of both materials [374]. Indeed, the problem of heteroepitaxy is not epitaxial growth itself, which is performed at high temperature, but the subsequent cooling of the samples. When samples are still at high temperature, their quality can be made excellent, despite the lattice mismatch. During the cool-down process, different thermal stresses in the sample generate dislocations, other crystalline defects or even cracks in extreme cases. To solve these issues, several efforts, such as lowering the growth temperature without losing quality in the samples, have been explored to develop epitaxial routines that produce lower thermal stress.

2713 ### 6.2.3 Defect confinement

2714 Most crystalline defects, originating during the III-V/c-Si integration, occur at the
2715 hetero-interface. However, they can propagate vertically and eventually reach active layers of
2716 the solar cell, producing a degradation of its properties [374,388,389]. Therefore, the
2717 development of epitaxial growth procedures that favor the annihilation or the confinement of
2718 crystal defects in parts of the structure far from the active layers of the solar cell have been
2719 recently pursued.

2720 ## 6.3 Approaches for PV integration

2721 Interest in the integration of III-V materials on c-Si has re-emerged lately in the PV
2722 research community [374, 386, 387, 390-394]. Currently, the most developed technique for
2723 such integration is the direct epitaxial growth of III-V compound on c-Si, due to reasonable
2724 scientific understanding of the processes involved in the heteroepitaxy. However, the search
2725 for alternatives has continued. In particular, wafer-bonding technique has received special
2726 attention by demonstrating promising results based on its ability to solve the limitations of
2727 epitaxial growth.

2728 Here we review both techniques by describing their state-of-the-art, emphasizing the
2729 most novel results obtained with each technology, pointing out current challenges, and
2730 possible strategies to overcome them. Finally, the limiting factors and hurdles for efficiency
2731 improvements in each technology are also presented.

2732 ## 6.3.1 III-V on c-Si epitaxy

2733 As we have mentioned before, the interest in III-V on c-Si integration, and
2734 particularly the III-V/c-Si epitaxy, has experienced a breakthrough over the last few years.
2735 The reasons for this are based on the progress in understanding the heteroepitaxy process of
2736 III-V semiconductors on c-Si [376]. Moreover, a new generation of metal organic vapor
2737 phase epitaxy (MOVPE) reactors has been developed, and metalorganic precursors adapted

2738 for the growth at low-temperature are readily available. As mentioned above, the use of lower
2739 growth temperature provides more opportunities to handle thermal stress associated with
2740 heteroepitaxy. Finally, the adaptation of new techniques (i.e. strategies to overcome the
2741 defect confinement) to c-Si wafers applied to the metamorphic growth of the InGaAs/Ge has
2742 also contributed to this progress [395].

2743 Despite the wide variety of III-V compounds (Fig. 53), only a few of them are suitable for
2744 direct integration on c-Si wafers. On the one hand, the materials have to be selected in a way
2745 that the bandgap combination (bottom and top cell) is optimum for harnessing the solar
2746 spectrum. On the other hand, the lattice mismatch between both materials has to be
2747 minimized for reducing the formation of structural defects. Unfortunately, only a very small
2748 number of III-V compounds meet both requirements. Thus, two different approaches are
2749 generally used for handling the epitaxial integration of III-V on c-Si: (i) the lattice
2750 mismatched (or metamorphic), and (ii) the lattice matched approach.

2751 **(i) Lattice mismatched approach**

2752 A metamorphic material is the one that grows on a wafer with a different lattice
2753 constant in a way that promotes its relaxation (i.e. its transition to its own lattice parameter)
2754 mainly through the occurrence of misfit and threading dislocations at the interface.
2755 Accordingly, the lattice mismatch approach consists of integrating two materials with a
2756 different lattice constant, in a way that its accommodation is achived by the generation of
2757 structural defetcts at the heterointerface. If the propagation of threading dislocations is
2758 minimized and the relaxation process is completed, then the resulting top surface has the
2759 desired lattice constant and a good crystalline quality (this is known as virtual wafer).

2760 Under this approach, III-V materials that can be integrated on c-Si are relatively are
2761 larger, since lattice matching is no longer a requirement. Hence, III-V candidates are selected
2762 to offer an optimum combination of bandgaps when integrating on a c-Si bottom cell. Two

2763 compounds, viz. GaAs and GaAsP, are generally used for achieving high quality
2764 metamorphic III-V/c-Si double-junction solar cells (Fig. 52).

2765 GaAs/c-Si: The integration of GaAs on c-Si wafer consists of direct growth
2766 (monolithic) of the III-V material on the wafer [374, 396]. The bandgap of the GaAS makes it
2767 very attractive for top cell (middle cell) in double-junction solar cell (triple-junction solar
2768 cell), as depicted in Fig. 52. However, as mentioned in Sec. 6.2, several problems exist for
2769 obtaining a defect-free and high quality GaAs/c-Si structure [397-400]. First, the growth of a
2770 polar on a non-polar semiconductor leads to the formation of a high density of antiphase
2771 domains (APDs) which should be controlled for a high quality structure. Work has been done
2772 for minimizing the formation and propagation of these defects [397,401]. Another problem
2773 found during the direct growth of GaAs on c-Si was related to the existing difference in their
2774 lattice parameter (Fig. 53). This difference promotes the generation of misfit dislocations at
2775 the GaAs/c-Si interface and threading dislocations, which can potentially propogate through
2776 the whole structure, and degrade the quality of the solar cell. Finally, the difference in
2777 thermal expansion co-efficients will not only favor the formation of dislocations, but also will
2778 promote the appearance of cracks during the cool down phase in the GaAs layer [397].

2779 Different approaches intended to seal off these limitations have been used [398-400,
2780 402-404]. As an example, the use of III-V intermediate layers based on compositionally
2781 graded buffers, together with thermal cycle annealing [398-400], and the use of lower
2782 temperature for the first few nanometers of the growth [399,402] were implemented for
2783 decreasing the dislocation density. The use of these techniques has brought the dislocation
2784 density from 10^9-10^{10}cm^{-2}, for direct GaAs on c-Si, down to 10^7cm^{-2}, which is equivalent to
2785 1-4 ns in terms of minority-carrier lifetime in n-GaAs [405]. However, to produce high-
2786 efficiency III-V top cells, these lifetime values are still low [403,404]. In fact, a low V_{oc} of

2787 ~900mV under AM0 conditions for single-junction GaAs cells on inactive c-Si wafers was
2788 measured in those cells [391].

2789 The above mentioned incompatibilities make it very difficult to achieve a high quality
2790 GaAs/c-Si monolithic device. Hence, another alternative was considered for such integration.
2791 This approach consists of modifying the lattice constant of the c-Si wafer through the use of
2792 group-IV buffer layers. The most developed method so far is the use of a Ge_xSi_{1-x}/c-Si virtual
2793 wafer [386,391,406-408]. The SiGe is an intermediate layer aimed to modify the Si lattice
2794 constant by increasing the Ge content during the epitaxial growth. Therefore, the lattice
2795 constant can be increased from 5.43Å (Si) to 5.64Å (Ge), and provide a new template with a
2796 lattice constant closer to the one of GaAs (5.65 Å). However, during the relaxation process,
2797 some misfit dislocations are generated. Some of them can eventually fold up and turn into
2798 threading dislocations, which degrade the device performance [406].

2799 Despite the limitations of this technique, promising results were obtained for GaAs solar
2800 cells grown on SiGe/Ge wafers. Recently, dislocation densities as low as $8x10^5cm^{-2}$ within
2801 the relaxed GaAs layer were obtained using Si/Ge wafers for III-V/c-Si integration. This
2802 value corresponds to a minority-carrier lifetime of 10ns for n-type GaAs. To the authors'
2803 knowledge, this is the highest value reported so far for GaAs grown on c-Si [409], resulting
2804 in efficiencies higher than 18% for single-junction GaAs solar cells on c-Si wafers [383,409].

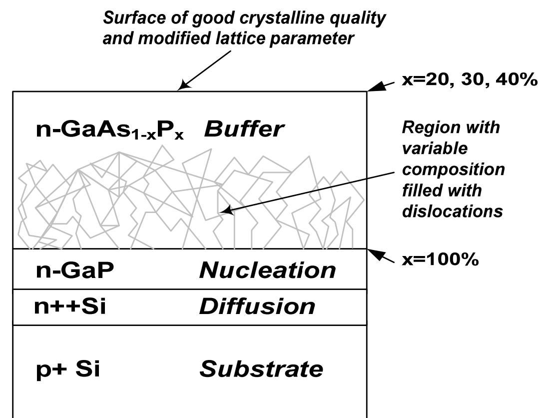
2805 Promising results have been reported recently on MJSCs based on SiGe wafers
2806 386,391,406-408]. High quality indium gallium phosphide (InGaP)/GaAs double-junction
2807 solar cells have been successfully grown on c-Si wafer through the use of Ge virtual wafers
2808 with SiGe step-graded buffers [386] achieving V_{oc} of 2.2V and an efficiency of 15.3 % for
2809 AM0 conditions [386, 410]. A InGaP/GaAs/SiGe triple-junction solar cell with an efficiency
2810 of 20% under AM0 (1 sun) illumination, and an open circuit voltage higher than 2.6V has
2811 been recently reported [411]. Wang et al. [412] have recently reported a GaAsP/SiGe double-

2812 junction solar cell with an improved bottom cell structure, within a current matching
2813 scenario, with efficiencies up to 20.6% using 1 sun illumination. This work proposes the use
2814 of light trapping techniques and a further optimization of the bottom cell for maximizing the
2815 device performance.

2816 GaAsP/c-Si solar cell: As it has been described before, in the metamorphic approach,
2817 materials are selected to offer an optimum combination of bandgaps. In this respect, the
2818 maximum theoretical efficiency of 40% has been obtained for a III-V/c-Si double-junction
2819 soalr cell with top cell material bandgap of 1.66 eV (Fig.52). This ideal material can be
2820 obtained by adding arsenic to GaP to produce $GaAs_{1-x}P_x$ (or simply GaAsP). In particular, the
2821 optimum composition (see Fig. 52) is a GaAsP alloy with 80% arsenic and 20% phosphorus
2822 in the group-V sublattice (i.e. $GaAs_{0.8}P_{0.2}$).

2823 Due to the mismatch between top and bottom cell materials, the integration of GaAsP
2824 on c-Si is performed through the creation of a virtual wafer, which takes care of the lattice
2825 constant transition and the defect confinement [413, 414]. Therefore, the resulting top surface
2826 has the desired lattice constant and a good crystalline quality, in which the GaAsP top cell
2827 could be easily integrated.

2828 The virtual wafer consists of an initial III-V layer lattice matched to c-Si to obtain a
2829 defect-free III-V template and addresses the problems related to the growth of a polar on a
2830 non-polar c-Si wafer [415-418]. The ideal material for this is GaP since it has a lattice
2831 constant reasonably close to that of Si (Fig. 53). After this step, the growth of a GaAsP
2832 graded buffer layer is included on top of the nucleation layer to handle the lattice parameter
2833 transition from Si to GaAsP and confinement of threading/misfit dislocations (Fig. 54).



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2835 Fig. 54 Schematic diagram for the metamorphic integration of gallium arsenide phosphide (GaAsP) on c-Si
2836 wafer. This process involves the growth of polar material (gallium phosphide GaP) on non-polar wafer (c-Si)
2837 which results poor morphological quality (i.e. non-homogeneous nucleation layer/isolated islands). To ensure
2838 high morphological quality, layer-by-layer growth is required for the integration of GaP over c-Si. GaP acts as
2839 virtual wafer. The integration of GaAsP over c-Si is performed through the virtual wafer. The virtual wafer takes
2840 care of lattice constant transition (from Si to GaAsP). Therefore, GaP is grown over c-Si since GaP has lattice
2841 constant close to Si. GaAsP graded buffer is grown on top of a GaP nucleation layer for accommodating the
2842 lattice mismatch between the top and the bottom subcell materials (i.e. p^+-c-Si and GaAsP).
2843

2844 While GaP has been reported to be the most ideal candidate for the nucleation layer,
2845 the growth of GaP on c-Si presents some limitations, mainly due to the growth of a polar
2846 (GaP) on a non-polar c-Si wafer [415-418]. In fact, the growth of a polar on a non-polar
2847 wafer has been reported to favor a non-homogeneous nucleation layer, formed by isolated
2848 islands, typical from a three-dimensional (3D) growth [419-421]. Moreover, the important
2849 thermal expansion co-efficient mismatch [417] (the one for GaP is 2.3 times larger than that
2850 of Si) hinders this integration. In general, a layer-by-layer growth is pursued for the
2851 integration of GaP on c-Si wafers to guarantee a high morphological quality of the nucleation
2852 layer. Moreover, wafers must be properly treated before nucleation (i.e. single domain
2853 structure formed by double steps in the absence of silicon oxide) for minimizing the
2854 appearance of planar defects, which otherwise, might ruin the electrical behavior of the solar
2855 cell; and for obtaining a defect-free template for the integration of the GaAsP graded buffer.

2856 Inspite of the significant amount of effort that has been done to find the best
2857 conditions for obtaining a continuous, defect-free GaP surface, this topic remains an open
2858 issue. The beneficial effect of low-temperature nucleation on obtaining a high quality and

defect-free surface has been reported [422, 423]. On the other hand, Ref.[388, 424] support the idea of using high nucleation temperatures, together with very high V/III ratios to obtain a smooth and APD-free structure [388, 424]. In any of those cases, a defect-free GaP layer has been successfully grown on vicinal <100> c-Si wafers. The resulting GaP/c-Si virtual wafers serve as templates for further III-V integration.

Going from GaP to GaAsP involves a significant increase in the lattice constant that, if not addressed properly, will produce a high concentration of dislocations and crystal defects that will ruin the PV performance [384,387]. In this case, a metamorphic GaAsP buffer layer, with variable arsenic content, is grown on the GaP nucleation layer (Fig. 54). The purpose of the buffer layer is to make an optimal transition between the nucleation layer and the layer with the composition needed for the top subcell (ideally $GaAs_{0.8}P_{0.2}$, in this case). This layer will absorb/avoid the propagation or will even annihilate crystal defects that will be generated when the gradual change of the lattice constant (i.e. the composition) occurs during growth. In other words, the goal of the buffer layer is to create a III-V virtual wafer of high crystalline quality with a different lattice constant than that of the Si that supports it. Eventually, this virtual wafer will serve as template where GaAsP top cells of the adequate bandgap can be integrated, thus forming a GaAsP/c-Si double-junction solar cell (Fig. 55a) with a high theoretical efficiency (Fig. 52).

The development of metamorphic GaAsP/c-Si solar cells has received special attention over the years. Several research groups [377, 384, 385, 425, 426] have been working on the development of the structure depicted in Fig. 55a. Their efforts have been mostly directed towards the optimization of key steps in the epitaxial growth of III-V compounds on c-Si, such as nucleation layer, graded buffer, and top subcell. The main target has been the minimization and confinement of crystal defects in the structure. Consequently,

2883 high structural quality graded buffers and promising results in the reduction of the dislocation
2884 density and annihilation of APD have been reported [384, 388, 390].

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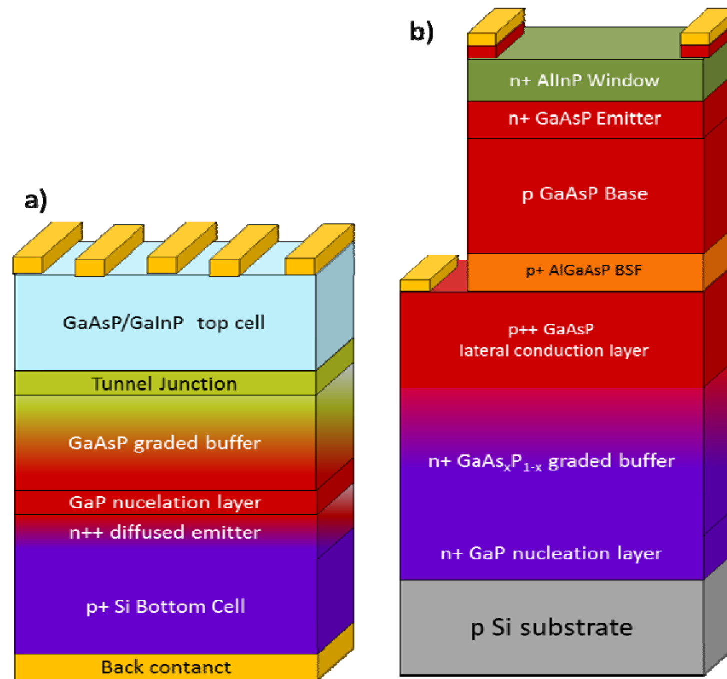

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2895 Fig. 55 (a) Ideal GaAsP/c-Si (or GaInP/c-Si) double-junction solar cell structure based on the metamorphic
2896 approach. The accomodation of the lattice mismatch is handled through the growth of a GaAsP graded buffer
2897 layer. The simplification of this structure turns into a single-junction GaAsP solar cell grown on top of an
2898 inactive c-Si wafer, as depicted in (b). When c-Si wafer acts as template (inactive wafer), technical challenges
2899 associated between the formation of c-Si bottom subcell and the subsequent formation of the tunnel junction can
2900 be avoided. Therefore, III-V subcell optimization can be done easily. Data for the latter from [427], Grassman T
2901 J, Carlin J A, Ratcliff C, Chmielewski D J, Ringel S A., Epitaxially-grown metamorphic GaAsP/c-Si double-
2902 junction solar cells, 39th IEEE PV Specialist Conf. (Florida) 2013, pp. 0149-0153.

2903
2904 However, there are still some key parts of the structure which have not received
2905 enough attention in the past, and those optimization is crucial for obtaining high quality
2906 double-junction solar cell.

2907 The first key point is the formation of c-Si bottom subcell with an optimum emitter (in
2908 terms of doping and thickness) and maintaining low roughness over the c-Si surface for
2909 subsequent epitaxial growth. Although an important progress on the optimization of bottom
2910 cell has been reported recently [428], most groups so far used c-Si wafer as a mere template
2911 (i.e. inactive wafer) and did not work on bottom cell optimization [377,384,385,387,390].
2912 This alternative (i.e. c-Si as inactive wafer) simply avoids the problems associated between

2913 the formation of the c-Si bottom subcell and the subsequent growth of the tunnel junction
2914 since c-Si wafer only acts as mechanical support and crystallographic template for the
2915 structure. In this way, the optimization of the III-V subcell can proceed independently and a
2916 lateral conduction layer is often included in the III-V solar cell [427] to ease the formation of
2917 rear contact (Fig. 55b). Both top and bottom contacts are formed on III-V layers. Promising
2918 results on obtaining a high-efficiency single-junction GaAsP grown on an inactive wafer has
2919 been reported so far. Lang et al. presented n^+/p-GaAsP/c-Si solar cell with V_{oc} of 1.10V
2920 [385]. Furthermore, Grassman et al. [384] reported promising light I–V (V_{oc} = 1.04V, J_{sc} =
2921 13.1mA/cm^2) and EQE results for a GaAsP/c-Si single-junction prototype solar cell. The idea
2922 is that these structures could be eventually integrated on optimized c-Si bottom subcells for
2923 obtaining high quality GaAsP/c-Si double-junction solar cell.

2924 The second key point is the formation of a tunnel junction to electrically connect the
2925 bottom and the top cell. The aim is to introduce highly doped ($>10^{19}$/cm^3) layers of a GaAsP
2926 homostructure [429] or a GaInP/GaAsP heterostructure. Latter is preferred since it has been
2927 recently demonstrated that its use reduces optical losses [426]. Preliminary work has been
2928 performed in this area, and promising results were obtained for c-Si based MJSC [426].
2929 However, still some work [429] has to be done to refine the structure and to reduce optical
2930 absorption of the tunnel junction.

2931 Although a great deal of work has to be still done for achieving high quality III-V on
2932 c-Si double-junction solar cell, a prototype of a GaAsP/c-Si double-junction solar cell
2933 [425,427] has recently been reported. This structure has been epitaxially grown by combining
2934 the use of molecular beam epitaxy (MBE) and metal organic chemical vapor deposition
2935 (MOCVD) reactors. The success of this prototype lies in the use of an optimized (i.e. defect-
2936 free) GaP nucleation layer, which acts as a template for a high quality GaAsP metamorphic

2937 graded buffer. Interesting results were obtained in this case, demonstrating the operation of a
2938 double-junction solar cell, with V_{oc} of 1.62V and J_{sc} of 11.0mA/cm^2 [425].

2939 Though interesting results reported [425,427] for as-grown tunnel junction test
2940 structure (i.e. peak tunneling current densities of 3A/cm^2), its integration on the double-
2941 junction structure degrades its properties as a result of its exposure to high temperatures
2942 during the top cell growth. Thus, it limits the electrical behavior of the double-junction solar
2943 cell. Nevertheless, the obtained results are promising, demonstrating that the technology for
2944 such integration is progressing and that current technology is not very far from obtaining a
2945 high quality GaAsP/c-Si metamorphic double-junction solar cell.

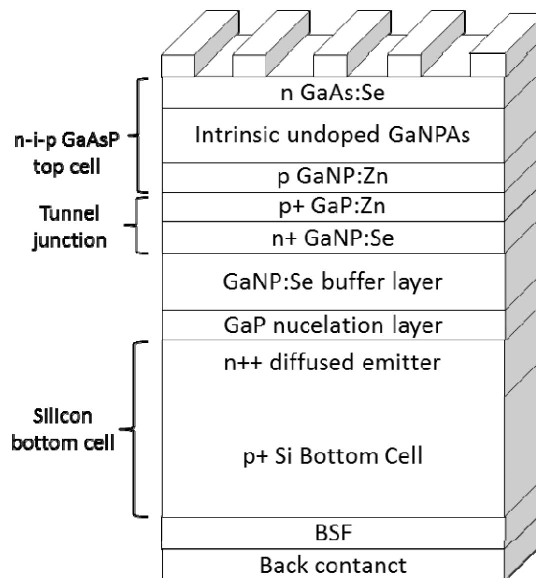
2946 **(ii) Lattice matched approach**

2947 As discussed above, one of the main limitations of III-V on c-Si epitaxy is the
2948 mismatch in lattice parameters. Hence, it is straightforward to assume that a lower lattice
2949 mismatch between the wafer and III-V compound implies a better structural quality of the
2950 resulting structure. Despite the fact that GaP seems to be the ideal candidate for the top cell
2951 material due to its lattice constant proximity to that of c-Si (Fig. 53), its large bandgap (2.2
2952 eV) makes it unsuitable for the top cell material. Therefore, a different material must be
2953 considered for the top cell. In this case, the most studied material for such integration is the
2954 quaternary alloy GaNPAs [381, 382, 430].

2955 Here, the lattice mismatch between the bottom (c-Si) and the top cell (GaAsP) is
2956 reduced by introducing nitrogen into the III-V semiconductor that decreases its lattice
2957 constant and brings it closer to that of Si. The idea is to grow the direct bandgap III-V alloy
2958 $GaN_xP_{1-x-y}As_y$ (hereafter GaNPAs) onto the c-Si wafer and minimize the formation of
2959 structural defects [381, 382, 430] for high-efficiency double-junction solar cell. In 2004,
2960 Geisz et al. first reported the lattice-matched GaNPAs on c-Si double-junction solar cell
2961 [381]. As depicted in Fig.56, the cell is formed by a n-on-p c-Si bottom subcell, a

2962 GaP:Zn/GaNP:Se tunnel junction, and a GaNPAs (E_g ~1.8 eV) top subcell. As in the case of
2963 the metamorphic approach, to minimize the occurrence of crystalline defects [381, 382], a
2964 GaP nucleation layer is also grown before the GaNPAs layer.

2965 The use of nitrides (even diluted nitrides) for reducing the lattice mismatch presents
2966 an important drawback: the formation of nitrogen-related defects, which greatly reduce the
2967 diffusion length in the GaNPAs layer, and limits the performance of the top junction [390].
2968 Geisz et al. [381] proposed the use of a field-aided device through a p-i-n configuration in the
2969 top cell to maximize its IQE, and to avoid the limitations of the extremely short diffusion
2970 length measured in the top cell. Thus, a thick GaNPAs intrinsic layer was grown to enhance
2971 the performance of the device (see Fig. 56).



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2973 Fig. 56 GaNPAs/c-Si lattice matched double-junction solar cell. To reduce the lattice mismatch between the top
2974 cell and bottom cell, nitrogen is introduced in the III-V structure to reduce its lattice constant and bring it close
2975 to that of Si. Also, nitrogen minimizes structural defects. In the bottom cell, BSF acts as reflector for minority
2976 carriers and causes the minority carriers (electrons in this case) to move to the bulk towards the p-n junction and
2977 reduces surface recombination at the rear side. The internal quantum efficiency has been maximized through the
2978 introduction of a field-aided device in the top cell (i.e. p-i-n configuration). In this double-junction structure, top
2979 cell limits the device current. Redrawn from [381], Geisz J F, Olson J M, Friedman, D J. Toward a monolithic
2980 lattice-matched III-V on c-Si double-junction solar cell, 19th European Photovoltaic Solar Energy Conference
2981 (Paris) 2004.

2982

2983 Interesting results were obtained for each subcell measured separately [431]. For c-Si
2984 bottom cell, V_{oc} of 536mV and J_{sc} of 14.5mA/cm^2 have been reported. GaNPAs (E_g ~1.8eV)

2985 top cell showed V_{oc} of 1.09 V and J_{sc} of 5.7 mA/cm^2. This double-junction structure has the
2986 potential for further improvement, since the top cell limits the device current (V_{oc} = 1.53V, J_{sc}
2987 = 6.3 mA/cm^2, AM1.5G efficiency = 5.2%). Currently, efforts are mainly focused on: (i)
2988 reducing the dislocation densities of the buffer layer through a better control of the GaP
2989 nucleation layer, (ii) forming a functioning tunnel junction by increasing the p-type doping,
2990 and (iii) increasing the top cell current by reducing the emitter sheet resistance and
2991 controlling the material quality of the GaNAsP top cell [431].

2992 **6.3.2 III-V on c-Si using bonding technique**

2993 Different alternatives for the epitaxial integration of III-V semiconductors on c-Si
2994 wafers have been reviewed so far. However, as described above, this technique presents some
2995 limitations, which include: (i) as described in Sec.6.3.1.2, monolithic integration is limited
2996 due to lattice matching requirements, which highly reduce the range of III-V materials that
2997 can be integrated on c-Si, (ii) the use of metamorphic growth techniques for integrating
2998 lattice-mismatched compounds is limited due to relatively high dislocation density formed in
2999 the buffer layer (Sec.6.3.1.1). In this regard, alternatives to this process have been recently
3000 explored. In particular, the mechanical stack has emerged as an alternative to avoid the
3001 limitations of the epitaxial process.

3002 Unlike epitaxially grown structures, the wafer bonding interfaces are incoherent. This
3003 implies that it is possible to accommodate any lattice mismatched material without the
3004 formation of the above mentioned misfit dislocations [393,394]. Therefore, the use of wide
3005 variety of materials, including the ones discarded for conventional epitaxial growth, is
3006 allowed for this technique.

3007 The physical concept of wafer bonding is based on the idea that two surfaces can stick
3008 together as long as the surfaces are perfectly polished, resulting in relatively very little
3009 friction between them [432]. In particular, in the wafer bonding technique, this consists on

3010 transferring a thinned wafer of III-V compound (such as GaAs) to a c-Si wafer. The bonding
3011 can be carried out even at room temperature as a result of the interaction of pure surfaces by
3012 van der Waals forces. In order to guarantee a high quality bonding, surfaces have to be
3013 specularly polished and completely clean to avoid any organic contamination [433].

3014 There are different wafer bonding approaches for the integration of III-V compounds
3015 on c-Si wafers for PV applications. One of them is based on high-temperature sticking of
3016 wafers. In this case, wafers are covered by a glass-like coating that bonds the wafers once the
3017 softening temperature is reached. However, this technique presents some limitations due to
3018 the use of high temperatures that may cause some problems such as defect generation,
3019 diffusion of impurities, thermal stress, etc. [434, 435].

3020 An interesting alternative is the smart cut technology. The procedure for wafer
3021 bonding using this technique is depicted in Fig.57. Initially, handle (c-Si) and donor (GaAs)
3022 wafers are coated with a thin Si oxide, since the bonding of Si oxide surfaces can be done at
3023 room temperature in air. In some cases, a thin SiN layer is deposited before the oxide layer, in
3024 order to favor the adhesion of the III-V compound to the oxide (Fig. 57a). Then, a weakened
3025 layer (formed by hydrogen or helium bubbles) is generated within the donor wafer by the ion
3026 bombardment method (Fig. 57b) [392]. This layer will eventually serve as a predetermined
3027 breaking point. Next step is the preparation of the surfaces for lowering the surface roughness
3028 to obtain good wafer bonding. After putting them into close contact, both wafers are bonded
3029 together as a result of the oxide softening and the application of pressure (Fig. 57c). After
3030 wafer bonding, the exfoliation, i.e. detachment of GaAs wafer along the implanted layer, is
3031 achieved by a heat treatment (Fig. 57d). In order to avoid shearing of interfaces and
3032 separation of both connected materials, it is preferable to work with the lowest possible
3033 temperature, especially when materials with very different thermal expansion co-efficients
3034 are bonded. Several groups are exploring different ways for reducing the exfoliation

temperature [394,436]. Finally, chemical and mechanical treatments of the exposed GaAs surface are required for obtaining high quality surface for subsequent epitaxial growth. In this technology, the donor wafer can be reused after exfoliation, and therefore the cost of the process is highly reduced (as compared to epitaxial growth on GaAs wafers).

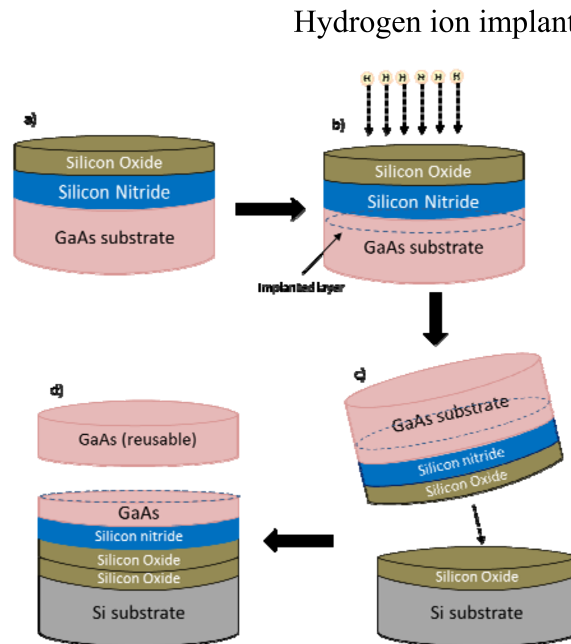

Fig. 57 Illustration of the smart cut technology for GaAs/c-Si structures: (a) the process starts with two different wafers (i.e. GaAs as donor wafer and c-Si as handle wafer), both are oxidized to favor bonding. To improve adhesion between GaAs and Si oxide, in the donar wafer, a thin SiN layer is deposited before the oxide layer deposition. (b) a weakened layer is generated within the donar wafer by hydrogen ion implantation through the oxide, (c) two wafers are hydrophilically bonded together due to oxide softening and external pressure, (d) finally, after bonding, the GaAs wafer is cut away using the implanted region as a reference. Heat treatment is used to detach GaAs wafer. Chemical and mechanical treatment is required for the exposed GaAs surface for subsequent epitaxial growth. The remaining GaAs wafer can be reused afterward for subsequent processes.

The use of smart cut technology leads to good quality crystals with a low dislocation density below $4x10^5 cm^{-2}$ [392]. Using smart cut technology, 12% efficiency GaAs/c-Si single-junction solar cells have been reported [392].

Other III-V materials such as indium phosphide (InP) have also been used as donor wafers for their direct bonding on c-Si wafers [437, 438]. These InP/c-Si stacks have been used as templates for subsequent III-V epitaxial growth, obtaining InGaAs/InP solar cells on inactive c-Si wafers [437] with V_{oc} of 0.30 V, J_{sc} of 24.9 mA/cm^2 and AM1.5G efficiency of 13.6%. This InGaAs solar cell is a good candidate for working as the bottom cell of a high-

3057 efficiency triple-junction cell, since it may be current matched with InGaP/GaAs double-
3058 junction solar cells [439, 440].

3059 However, the use of this technique presents an important drawback: the bonding
3060 layers are made of Si oxide, an insulating material. Thus, the c-Si wafer is not the active
3061 region of the structure; on the contrary, it is merely acting as a mechanical support for the
3062 structure without any active PV role. Hence, this technology requires the development of a
3063 new solar cell design for contacting the rear side of the solar cell. With this aim, as shown in
3064 Fig. 58, a lateral conduction layer [392] is grown on the top of the III-V seed layer (before
3065 growing III-V solar cell epitaxially) for contacting the base layer of the active region.

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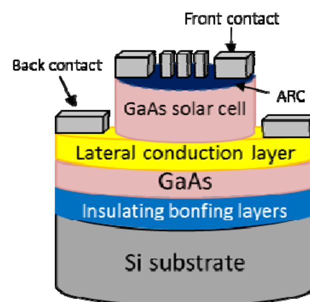

3071 Fig. 58 Single-junction GaAs solar cell on GaAs/c-Si wafer using smart cut technology. Since the c-Si wafer is
3072 not an active part of the structure, the conventional back contact must be relocated so that the back side the solar
3073 cell can be contacted. In this case, a lateral conduction layer is grown on top of the GaAs seed layer. Back side
3074 contact is formed on top of the lateral conduction layer and grid lines are formed at the front side of the solar
3075 cell for front contact. Lift-off process using photolithography is the conventional method used for the formation
3076 of front grid contact. Redrawn from [392], Schone J, Dimroth F, Bett A W, Tauzin A, Jaussaud C, Roussin J C,
3077 III-V solar cell growth on wafer-bonded GaAs/c-Si-wafer, IEEE 4th World Conference on Photovoltaic Energy
3078 Conversion (Hawaii) 2006.
3079

3080 Many groups have been working on solving the drawback of the inactive wafers [393,
3081 441, 442]. As a result, an improvement of smart cut technique has been achieved. The main
3082 modification is the substitution of the insulating bonding layer by a conductive layer. The
3083 surface-activated wafer bonding process has been illustrated in Fig. 59 [442]. In this case, the
3084 GaAs wafer is used as a template for epitaxial growth of III-V compounds (Fig. 59 a-c). An
3085 etch-stop layer and a bonding layer are grown on top of GaAs wafer, before the epitaxial
3086 growth (Fig. 59b). Simultaneously, as shown in Fig. 59 (d-f), the c-Si wafer is processed

3087 before stacking, so a single-junction c-Si solar cell is formed. The whole structure is then
3088 attached to a wax-type transfer substrate. Afterwards, the etch-stop layer is etched away
3089 laterally, so the GaAs wafer is physically detached from the structure in a way that allows for
3090 its reuse (Fig. 59c). In this process, the surfaces of the cell structures are cleaned by a beam
3091 of argon (Ar) atoms in a ultra high vacuum chamber. The wafers are brought into intimate
3092 contact immediately after the surface activation to initialize the bonding (Fig. 59g). Finally,
3093 the wax-type transfer substrate is removed and the mechanical stacked solar cell is eventually
3094 processed (Fig. 59h).

3095 To our knowledge, the first direct wafer bonded MJSCs with a c-Si subcell was
3096 reported on 2012 by Tanabe et al. [393], using an AlGaAs/c-Si double-junction solar cell,
3097 with an efficiency of 25.2% under one sun ($100mW/cm^2$) illumination. GaInP/GaAs/c-Si
3098 triple-junction solar cell with an efficiency of 20.5% under one sun, and 23.6% under 71 suns
3099 illumination (AM1.5 conditions) was also reported using the same technique [441, 442].
3100 Recently, a GaInP/c-Si double-junction solar cell formed by a rear heterojunction GaInP and
3101 a back junction, back contacted c-Si bottom cell has been reported [443] with an encouraging
3102 efficiency of 26.2% at 1 sun illumation (AM1.5G).

3103

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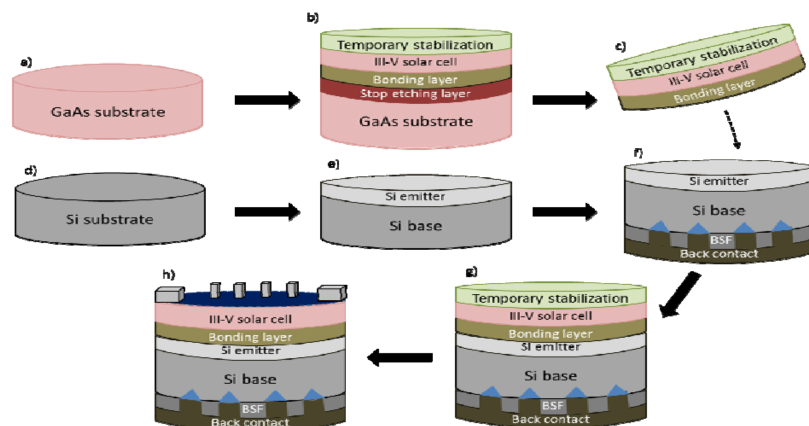
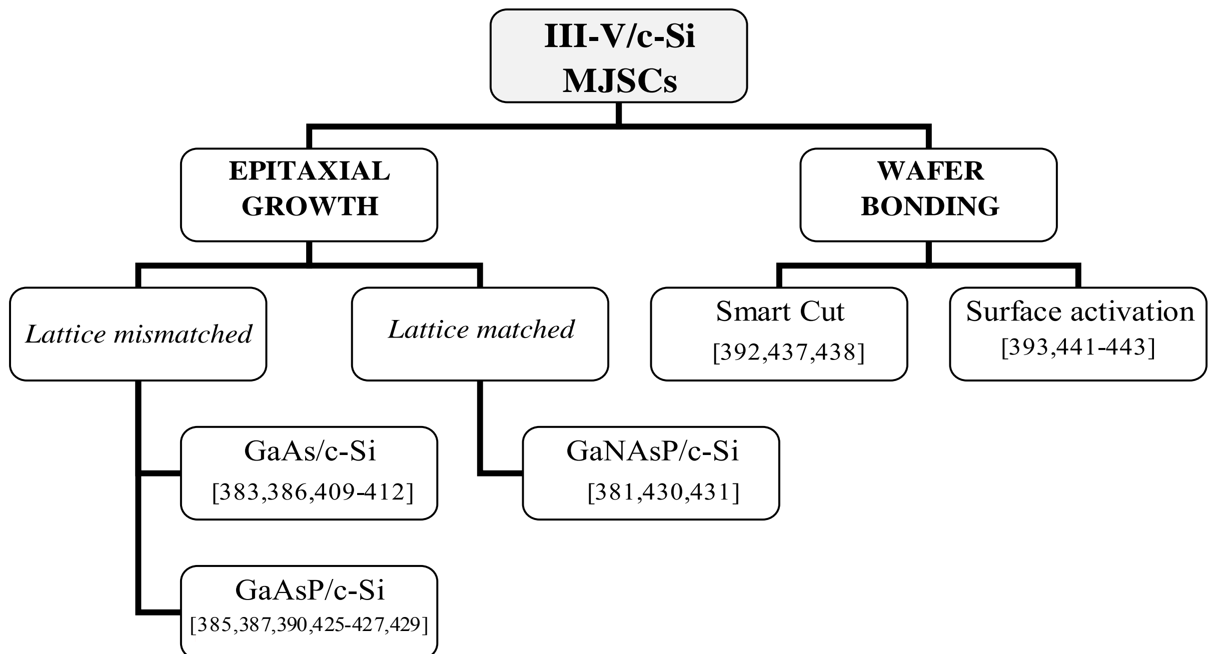


3105
3106 Fig. 59 III-V/c-Si multi-junction solar cell by surface activated wafer bonding process: (a) GaAs wafer for
3107 epitaxial growth of III-V compound, (b) etch-stop layer and bonding layer are grown right before the epitaxial
3108 growth of III-V solar cell and then attached to a transfer substrate, (c) lateral etching remove etch-stop layer and

3109 GaAs wafer is detached for reuse, (d-f) single-junction c-Si solar cell process, (g) after cleaning and activating
3110 the surfaces, wafers are bonded together, (h) wax-type transfer substrate is removed and stacked MJSC cell is
3111 processed for top contact. This process is an improvement of smart cut technique, supporting wafer (c-Si) is not
3112 inactive. Supporting wafer is active and used to form bottom cell.
3113

3114 Although promising results have been achieved recently, the main bottlenecks of this
3115 technology are the resistance of the bonding surface, and current mismatch between the
3116 subcells, which limits the device performance. This is primarily limited by the c-Si bottom
3117 cell [441]. For a better visual comparison of various technologies associated with III-V on c-
3118 Si MJSC, a block diagram is shown in Fig.60.

3119



3120

3121 Fig. 60 Different III-V compounds on c-Si technology. The integration of III-V semiconductors on c-Si wafers
3122 by epitaxial growth using two different approaches: lattice matched and lattice mismatch (or metamorphic)
3123 approach. The main difference between these two approaches lies on handling the lattice mismatch between the
3124 top and the bottom cell materials. These two different approaches have been found to produce successful results
3125 for the integration of III-V on c-Si wafers through the wafer bonding approach. An important process is the
3126 surface activated process, which replaces the isolating bonding layer (used in the smart cut technology) by a
3127 conductive layer, and thus, the c-Si wafer takes place in the active region of the structure and acting as bottom
3128 cell.

3129 6.4 Future outlook

3130 Two different technologies have been predominantly used so far for the integration of
3131 III-V on c-Si: epitaxial growth, and wafer bonding. Epitaxial growth of III-V semiconductors

3132 on c-Si wafers has received a lot of attention over the last decades, resulting in a reasonable
3133 scientific understanding of this process. Although a great deal of work has to be still done for
3134 achieving high quality monolithic III-V on c-Si double-junction solar cell, a prototype of a
3135 GaAsP/c-Si double-junction solar cell [425,427] has been recently reported. This structure
3136 has been epitaxially grown by combining two different techniques: MBE, and MOCVD.
3137 Interesting results were obtained in this case, demonstrating the operation of a double-
3138 junction solar cell, with V_{oc} of 1.62 V and J_{sc} of 11.0 mA/cm^2 [425]. These results are
3139 promising, and demonstrate that the technology for such integration is progressing. Future
3140 work will be directed towards the development of the tunnel junction and its integration into
3141 the double-junction solar cell, which is the main bottleneck for this structure, limiting the
3142 electrical behavior of the double-junction solar cell. Moreover, future activity must be
3143 directed towards simplification of the technology by means of the development of a
3144 GaAsP/c-Si metamorphic double-junction solar cell into a single reactor (i.e. MOCVD).

3145 On the other hand, wafer bonding has emerged as an alternative for epitaxial growth.
3146 In particular, the surface-activated wafer bonding technology is seen as a promising option
3147 for III-V on c-Si integration. In this respect, a GaInP/c-Si double-junction solar cell formed
3148 by a rear heterojunction GaInP and a back junction back contacted c-Si bottom cell has been
3149 recently reported [443] with an encouraging efficiency of 26.2% at 1 sun illumation
3150 (AM1.5G). In this case work must be directed to overcome the current limitations, such as
3151 resistance of the bonding surface and current mismatch between cells, which are currently the
3152 limiting factors of the cell electrical properties.

3153 7. Amorphous Si solar cells

3154 A-Si:H has seen rapid development in industrial processing in the last decade, and has
3155 led to multiple types of large area and roll-to-roll deposition systems. While the Si material

development appears to have reached saturation, the passive parts of devices, such as surface texture, light trapping designs, development of thinner cells, and cells on new exquisite nanopillar and nanohole structures have made tremendous progress. Moreover, third generation concepts are beginning to be applied to thin-films Si devices, making a paradigm shift in the way a solar cell operates, with existing fabrication tools.

7.1 Introduction

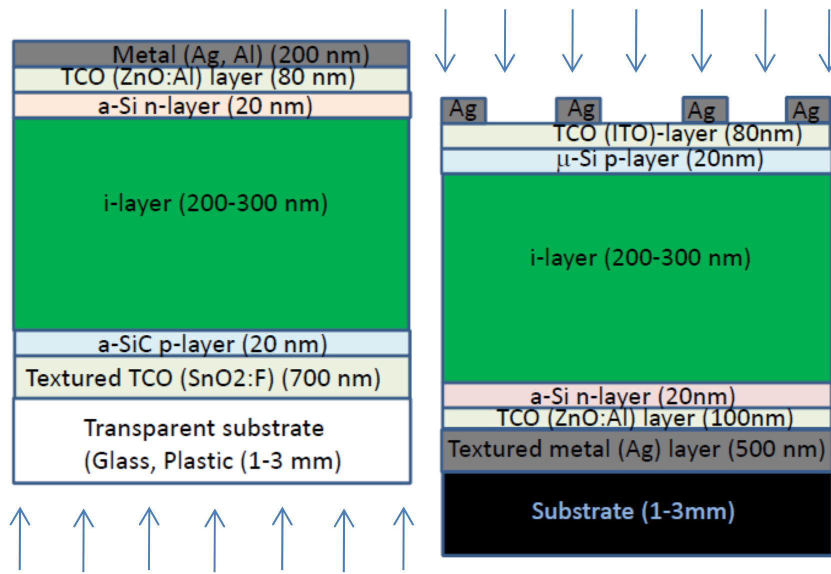
According to European Photovoltaic Industry Association (EPIA) the global cumulative installed solar power capacity in 2015 crossed 228GW [444]. The learning curves [445] show a 22% reduction in price for PV; thin-film PV shows a slightly higher rate of cost reduction compared to c-Si wafer type of cells. Though the cost of thin-film Si modules commercially is less than that of c-Si, the cost of electricity is essentially similar in both cases. This makes a c-Si module still most attractive because of its high-efficiency. Among thin-film PVs, CdTe is the most attractive, due to a very small energy payback time of 0.5 years [446] at the cost of ~$0.6/W [447]. These advances clearly pose a commercial challenge for a-Si:H PV.

The commercial single-junction a-Si:H modules have an efficiency of 4-8%, whereas the best laboratory efficiencies are in the range of 9.5-10%. According to International Renewable Energy Agency, among thin-film technologies, a-Si:H thin-film is perhaps the most challenged by the current low-cost c-Si [448]. Its future is rather uncertain as some producers have recently either stopped or reduced part of manufacturing capacity, even though in laboratory it is demonstrated that using a simple thin a-Si:H absorber a stabilized efficiency of 10% can be achieved [449,450]. Moreover, the energy payback time of thin-film a-Si:H, as was claimed by TEL Solar Japan (formerly Oerlikon), is less than 1 year, and a cost of electricity of $0.088/kWh for ground mounted system is estimated [451]. The wholesale price of thin-film a-Si:H PV module in July 2013 is only $0.46/Wp and thin-film

3181 a-Si:H/μc-Si:H (micromorph) is at \$0.59/W_p, much lower than \$1.74/W_p in the beginning of
3182 2010 [452].

3183 According to EPIA fact sheet [453], the most critical materials used in PV
3184 technologies are indium, tellurium and Ag. The first two of these are indispensible elements
3185 of the state-of-the-art CIGS and CdTe solar cells respectively. However, these elements are
3186 not absolutely necessary for thin-film Si PV, especially for superstrate type of cells. Typical
3187 schematic diagram of a p-i-n (also called superstrate type) and an n-i-p (also called substrate
3188 type) a-Si:H cell is given in Fig.61. ITO is generally used on the top TCO for n-i-p cells, and
3189 Ag is used as rough template on which n-i-p cell is made. The former can be replaced by an
3190 alternative TCO, such as doped ZnO:Al [454], whereas many types of light trapping features
3191 at the back side can be made; patterning of the substrate (through lithography or embossing
3192 techniques) [455], naturally grown textured ZnO [454], and texture etched ZnO [456]. For p-
3193 i-n cells, white paints [457-459], white sheet (developed by Dupont for Oerlikon) [460], and
3194 Al [461] can be used as back reflector. However, Ag is still used by many companies to
3195 maintain a high-efficiency. A trade-off has to be made between gain in price for high-
3196 efficiency, and the loss due to high cost of Ag in comparison to Al. Since the price of Ag has
3197 fallen recently after a peak in 2011 of above \$1100/kg to now (in 2016) around \$500/kg
3198 [462], this may currently not be an issue with PV, but may be sensitive to future demand-and-
3199 supply. As efficiency increase is an option to reduce the cost [463] (every 1% increase in PV
3200 module efficiency reduces the balance of system (BOS) cost by between \$0.07 and \$0.10/W),
3201 micromorph cells are best suited to serve this purpose with relative simplicity and high-
3202 efficiency. Commercial micromorph module efficiencies are between 6.5 and 9%, though
3203 best laboratory efficiencies are currently in the range of 12-13%. It should be noted that
3204 prototype module efficiencies of up to 11% have been demonstrated. Further efficiency
3205 increase by employing higher number of junctions will have to take into account the possible

3206 cost benefit of a high-efficiency and complexity of production. Bankruptcy of Unisolar
3207 Ovonics (US) after years of experience in triple-junction cells, and difficulty of other
3208 companies, especially Kaneka Co. (Japan), in commercializing such products warns us that
3209 careful design and process simplicity have to be developed for cost reduction, especially the
3210 capital expenditure (CAPEX), and a new industrially viable processing is a necessity.



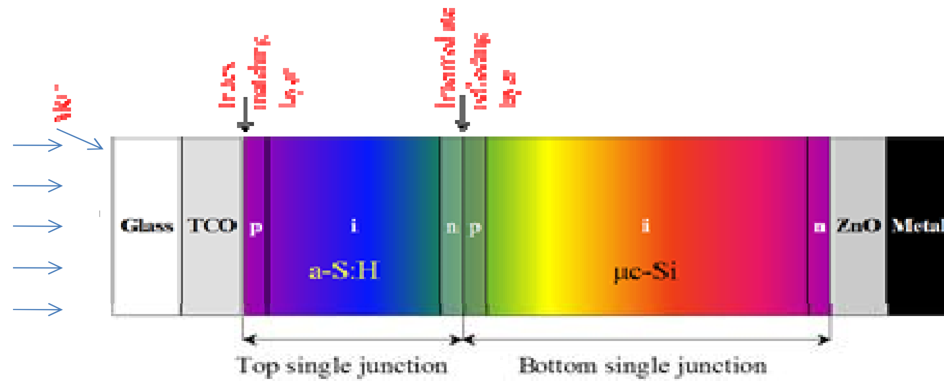
3211
3212
3213
3214 Fig.61 Schematic diagram of a p-i-n or superstrate type (left side) and an n-i-p or substrate type (right side) a-
3215 Si:H solar cell. In both type of cells, light enters through the p-layer side since hole mobility is lower than the
3216 electron mobility. Substrate type cells have the advantage that substrate need not be transparent, e.g. metal
3217 (steel, Al) foil, non-transparent plastics (such as Kapton), tiles, fabrics etc. For superstrate cell, texture etched
3218 ZnO:Al is also widely used, however, in that case a double p-layer (microcrystalline/amorphous) is used.
3219 Several types of light trapping features can be made at the rear side such as naturally grown textured ZnO,
3220 texture etched ZnO and patterning the substrate. Same cell designs are used for μc-Si:H cells (p, i and n layers
3221 all are μc-Si:H, i-layer thickness 1-2μm) and a-SiGe cells (U, V, or E type graded i-layer 100-150nm).
3222

3223 In this section we will look at how the thin-film Si technology has evolved through the
3224 years and show that, in spite of current uncertainty in market, why it is still one of the most
3225 promising technology for the future.

3226
7.2 Brief history and status of thin-film Si technology

3227 A-Si:H came into existence in 1960s. Amorphous structure contains short range order
3228 similar to c-Si but deviates in medium range and long range order. The second difference is
3229 that critical (average) network coordination for a-Si is 2.4 compared to coordination of 4 for

3230 c-Si. Breaking of bonds allows the material to reduce the coordination. Hydrogen has a big
3231 role in reducing the network coordination while retaining local four-fold coordination.
3232 Hydrogen is situated at monohydrides, dihydrides, polyhydrides $(Si\text{-}H_2)_n$, SiH_3 and voids.
3233 The material can be described as continuous random network which contains randomly
3234 distributed weak bonds and dangling bonds. However, the structure also contains another
3235 phase which is hydrogen rich, with low density regions and voids. It was in 1976 that an a-
3236 Si:H solar cell with 2% efficiency was made, with a prediction of 15% efficiency in the
3237 future [464]. However, it was realized that these materials (cells) suffer from light induced
3238 degradation, also called Staebler-Wronski effect, discovered in 1977 [326]. This
3239 phenomenon, with a decrease by an order of magnitude in both dark and light
3240 photoconductivity under illumination from the initial state, is metastable. All optoelectronic
3241 characteristics can be reverted back to the initial state by annealing of the sample above
3242 150ºC (above the glass transition temperature of hydrogen in amorphous material). This
3243 phenomenon is caused by a change in midgap density of states (increase in dangling bond
3244 density) resulting in shift of Fermi level towards midgap and increase in recombination.
3245 There are basically two divergent models proposed as origin of this effect; (i) (weak) bond
3246 breaking (hydrogen mediated) that creates isolated defects [465-467], and (ii) voids/volume
3247 deficiencies [468-470]. Hydrogen seems to play an important role in this effect. To mitigate
3248 the Staebler-Wronski effect, materials have been fabricated with low hydrogen content,
3249 smaller $Si\text{-}H_2/Si\text{-}H$ ratio, lower microstructure factor/void content, lower Urbach energy
3250 (weak-bond density), etc. To that end, high hydrogen dilution of precursor (SiH_4) gas during
3251 deposition is invariably used. Now, use of thinner absorber layers and multi-junctions cell
3252 design has made it possible to control the light induced degradation of efficiency to an
3253 acceptable range below10%.



3254

3255 Fig. 62 Schematic diagram of typical micromorph superstrate type double-junction cells. An efficient tunnel
3256 recombination junction made of p- and n-μc layers allows Ohmic contact between the cells. ARC, normally a
3257 graded refractive-index layer (n) coating reduces partly the 4% reflection loss at the glass/air interface.
3258 Refractive index matching layer such as TiO_2 has the function to reduce reflection at the TCO (n~2)/p-layer
3259 (n~4) interface; intermediate reflector selectively reflects light at the tunnel recombination junction to the top
3260 cell, a technique by which the top cell thickness can be substantially reduced for better stability. Typical
3261 intermediate reflector is made from oxides - SiOx (n or p-type) or ZnO or a Bragg reflector. Typical thickness
3262 and bandgap of the top cell and the bottom cell are ~200nm, 1.8eV and 1-2μm, 1.1eV respectively.
3263

3264 Later, alloying a-Si:H with C, Ge, N, O, etc. allowed fabrication of multi-junction
3265 solar cells with wide bandgap doped layers, and tunnel recombination junction. This was
3266 considered a major advantage as compared to c-Si cells. Up to beginning of 1990s, a-Si:H
3267 cells in combination with an a-SiGe:H alloy cells in multi-junction structure were considered
3268 as among the best options, and a number of industries focused on this technology (Solarex
3269 [471], Unisolar [472], Sanyo[473] and Fuji electric [474]). By 1990, double and triple-
3270 junction devices using a-SiGe:H as bottom cell(s) reached global AM1.5 initial efficiency of
3271 13.0% and 13.7%, respectively. Throughout this period, however, a-Si:H PV went through a
3272 technological challenge because of “degrading cells” (the Staebler-Wronski effect of a-Si:H
3273 [326]), and even a-SiGe:H alloys showed substantial degradation [475]. However, the advent
3274 of device-quality nanocrystalline Si (nc-Si:H) absorber layer in mid 1990s, [476,477] and
3275 demonstration by Kaneka with cell efficiency of >10% at a high deposition rate (0.5nm/s)
3276 [478] changed the scenario. Thus, a-Si:H in combination with nc-Si:H (also called μc-Si:H)
3277 became desirable. This structure, called micromorph cell (Fig.62), allowed a greater range of
3278 solar spectrum to be absorbed, avoided the toxic and expensive germane gas, and
3279 demonstrated enhanced stability. This nc-Si:H material has attracted immense research

3280 interest because of its complex structure and yet to be fully understood growth process [479].
3281 A debate exists on whether a-SiGe:H or nc-Si:H is a more profitable proposition as the
3282 bottom cell [480]. The arguments are based on two different scenarios, i.e. whether to use
3283 expensive germane gas, lower deposition rate (~0.1nm/sec), but relatively thinner (~100 nm)
3284 absorber layer for a-SiGe:H, or a much thicker layer (>2μm), accompanied with degradation
3285 of cell performance at high deposition rates for nc-Si:H [481]. One of the strong arguments
3286 used for thin-film Si solar cells has been the non-toxic nature of base materials compared to
3287 other types of thin-films PVs. Germane gas is highly toxic, due to which the preference in
3288 the last decade has tilted in favor of nc-Si:H. Thin-film Si processing also uses toxic dopant
3289 gases (PH_3, B_2H_6 etc.), however, their concentrations are very small in the gas mixture.

3290 At present the most widely used industrial process is the micromorph structure. TEL
3291 Solar has provided even turnkey solutions for these double-junction cells. Though the use of
3292 a-SiGe:H in a double-junction structure is now rare, because a-Si:H/nc-Si:H potentially
3293 delivers higher efficiency due to perfect bandgap combination of 1.8 eV/1.1eV [482], a-
3294 SiGe:H still holds a lot of promise in triple-junctions, especially for the adjustable bandgap
3295 middle cell. The cell with current record initial efficiency of 16.3% (initial) uses a-SiGe:H in
3296 the middle cell [483] in an n-i-p cell configuration. Though the record stabilized efficiency is
3297 achieved without Ge in a p-i-n type a-Si:H (E_g ~1.73eV)/nc-Si:H (E_g ~1.1eV)/nc-Si:H (E_g
3298 ~1.1eV) structure [484,485], LG is exploring to use a-SiGe:H films to improve this
3299 technology [486]. LG developed a-SiGe:H cell with a modified E-shape bandgap profile,
3300 originally demonstrated at Utrecht University [487,488], which was used as the middle cell
3301 of a triple-junction structure and delivered an initial efficiency of 14.9%. Moreover, the
3302 direction towards thinner cells (to be discussed shortly) can only be achieved by using a-
3303 SiGe:H, even for double-junction cells. Moreover, it has already been demonstrated that a
3304 very stable a-SiGe:H can be made with protocrystalline (pc-Si:H) condition [489] (i.e. films

3305 deposited just before the onset of microcrystalline regime known as protocrystalline
3306 condition), though at a low deposition rate (~0.06nm/sec). The success will depend on the
3307 fabrication of stable low bandgap a-SiGe:H (E_g ~1.3-1.4 eV) cell, especially at acceptable
3308 deposition rates (> 0.1nm/s). In this aspect, two types of development have taken place:
3309
3310 (i) μc-SiGe:H [490], which allows a use of a thinner bottom cell of a double (a-Si:H/μc-
3311 $Si_{0.83}Ge_{0.17}$:H [491]), and triple-junction (p-i-n type a-Si:H/μc-Si:H /μc-$Si_{0.9}Ge_{0.1}$:H [492], p-
3312 i-n type a-Si:H/μc-$Si_{0.6}Ge_{0.4}$:H/μc-$Si_{0.91}Ge_{0.09}$:H [493]). The total thickness of the double-
3313 junction [491] and the triple-junction [493] are only 1000nm and 1800nm, respectively.
3314
3315 (ii) HWCVD a-SiGe:H has [494] shown that good photosensitive materials can be made for
3316 bandgap even below 1.4eV, much better than PECVD grown materials. However, this
3317 process demands high gas flow rate to avoid depletion of the germane gas. The cost
3318 implication of high germane consumption has to be considered. Table 2 shows the record
3319 efficiencies of single, double, and triple-junction Si thin-film cells.

3320 Table 2 Record thin-film Si cells. The bandgap and thickness of the layers are: a-Si:H (1.7-1.9 eV, ~200 nm), a-
3321 SiGe:H (~1.5eV, ~150 nm) and nc-Si:H (1.1eV, ~2000 nm). A-Si:H layers are deposited in protocrystalline
3322 condition. Whereas the stabilized efficiency of single-junction (even initial efficiency) is well below the S-Q
3323 limit of 29%, the maximum stabilized efficiency (13.44%) is still much below the theoretically estimated triple-
3324 junction of ~48%. The results suggest enough room for improvement in the cell performance for thin-film Si.
3325 *independently measured.
3326

Cell	Group	Eff. (% initial)	Eff. (% stabilized)	Ref.
a-Si:H	Sanyo	12.7	-	[495]
a-Si:H	EPFL	-	10.1*	[449]
a-Si:H/a-SiGe:H	Sanyo	11.6	10.6	[496]
nc-Si:H	EPFL	10.9, 10.7*	-	[497]
nc-Si:H	UU	-	10	[498]
a-Si:H/nc-Si:H	EPFL	14.4	-	[499]
a-Si:H/nc-Si:H	Kaneka	14.7	-	[500]
a-Si:H/nc-Si:H/nc-Si:H	LG	-	13.44*	[501]
a-Si:H/nc-Si:H/nc-Si:H	Unisolar	-	13.6	[502]

a-Si:H/a-SiGe:H/nc-Si:H	LG	16.1	-	[501]
a-Si:H/a-SiGe:H/nc-Si:H	Unisolar	16.3	-	[503]

3327

3328 ## 7.3 Challenges to a-Si:H technology

3329 As compared to c-Si technology (which dominates around 87% of the market), thin-
3330 film PV has a relatively small share of 13% in the PV market. This is further dominated by
3331 CdTe, leaving behind only a very small market for thin-film Si. The main argument against c-
3332 Si PV is its high cost due to, among others, the use of thick absorber material compared to a-
3333 Si. However, this argument is now challenged. First, high price of c-Si in 2006, due to Si
3334 ingot price increase from $200/kg to $400/kg between 2007 and 2008 [504], led to a 30%
3335 reduction of Si material in the manufacturing process. Using thinner wafers (180-200μm now
3336 from earlier ~300μm), process automation and waste recycling, the Si use has now reached a
3337 low 5-10g/W_p [448]. The target is to reach the level of 3 g/W_p or less between 2030 and
3338 2050, pushing the limit further. Moreover, Panasonic showed their best efficiency of 24.7%
3339 for HIT solar cell for a wafer thinner than 100 μm [505], and even 70μm flexible cells can be
3340 made. Attempts are now being made to push it further down to less than 50μm, though
3341 sawing and yield require further technological advancement. Moreover, thin-film c-Si by lift-
3342 off methods are also in progress [506], and 16.8% efficiency for 18 μm c-Si has been
3343 reported and cells even with 10μm (8.7%) have been made. Second, the price of polysilicon
3344 has dropped sharply and reached $20/kg in 2011 [504]. Third, the large production of c-Si
3345 based modules has reduced the price [445]. Moreover, the large over capacity has forced
3346 dumping of PV at low price (around 25GW of global installation compared to around 60GW
3347 of ramped module capacity in 2011) due to which even c-Si modules can be purchased at
3348 very low price and pushed thin-films PV to margin.

3349 Among thin-film PV technology, CdTe made up 46% of total module production in
3350 2012, followed by thin-film Si (a-Si:H single and multi-junctions, 35%) and CIGS (19%).
3351 However, CdTe production is dominated by only one company (First Solar) and CIGS is
3352 predominantly by Solar Frontier, clearly showing that these productions are still very much
3353 process specific. Wide use of off-the-shelf deposition facilities has still not taken place,
3354 unlike with thin-films Si, for which even turnkey solutions are available. Si, though, is
3355 expected to maintain its advantage over other thin-film materials, since it is non-toxic and
3356 abundant.
3357
3358
7.4 Deposition related issues

3359 A-Si:H is grown from gas phase in a vacuum chamber. It is a very reproducible
3360 material, and is very weakly dependent on process parameters, deposition systems, reactor
3361 volume or pumping speeds, etc. Standard a-Si:H films are routinely made at many labs with
3362 various deposition processes, such as standard radio frequency (RF) PECVD, VHF PECVD,
3363 hot-wire CVD, microwave PECVD, PhotoCVD, etc., with deposition rates of 0.1-0.3nm/s
3364 with almost comparable physical characteristics, delivering around 10% initial efficiency in
3365 single-junction cells. However, for better stabilized efficiency, the deposition process is
3366 adapted. The first indication for a better stability against light soaking came with the hot-wire
3367 CVD a-Si:H [507] with a smaller hydrogen content (~1%) than that is in standard device-
3368 quality a-Si:H of 10%. Since then, it is more or less established that a-Si:H deposited under
3369 high atomic hydrogen ambient, which is generally, but not necessarily, made with high
3370 hydrogen dilution of SiH_4, just at the edge of transition to nanocrystalline regime is the most
3371 stable material. The amount of dilution H_2/SiH_4 depends on other deposition conditions; for
3372 example, LG uses a very high H_2/SiH_4 value of 60 for their a-Si:H top cell [501]. This
3373 material, called pc-Si (as mentioned already in Sec. 7.2) [508] is, however, sensitive to
3374 deposition process and is fabricated in a narrow deposition regime. Hence, it is prone to

3375 irreproducibility and therefore needs good control in deposition process. Unlike a-Si:H, a pc-
3376 Si:H is thickness dependent. Hence it can make a transition to nc-Si:H with slight change in
3377 thickness. A competing process to make stable materials, and claims to be thickness
3378 independent, is the so called polymorphous Si (pm-Si:H) [509]. So far the stabilized
3379 efficiency with pm-Si:H has still not reached its full potential, and is yet to reach the
3380 efficiency that is obtained by pc-Si:H. One common denominator in all these materials is that
3381 they contain crystalline nanoparticles, brought in the material either by nucleation in the
3382 amorphous matrix (as in case of pc-Si:H), or embedded from gas phase (as in case of pm-
3383 Si:H). The correlation of stability with nanocrystalline incorporation, irrespective of its origin
3384 (whether through hydrogen dilution or Ar dilution of SiH_4) has been speculated for a long
3385 time [510].

3386 Nc-Si:H can be made by a variety of techniques [511], the same that are used for a-
3387 Si:H. Control of ion energy with very VHF RF power and high process pressure have led to
3388 high quality nc-Si:H material, and cells with high-efficiencies above 10%. On the other hand,
3389 high RF power and high gas flows in high pressure gas depletion condition (also called HPD)
3390 has led to high growth rates. However, the monotonic decrease in material quality and solar
3391 cell performance at higher deposition rates [479] is still a lingering issue that needs solution.

3392
7.5 Recent trends to push the limits: Light management

3393
3394 Light trapping in the absorber (intrinsic) layer is one of the most widely used concepts
3395 in thin-film Si solar cells for the purpose of either to increase the current or decrease the
3396 thickness of the absorber layer. This is essentially achieved in three ways [512]: (i) scattering:
3397 a random texture is generally used, (ii) geometric optics: features larger than the wavelength
3398 of light is used, the total internal reflections at interfaces of absorber layer is used for this
3399 purpose leading to $4n^2$ light passes in Yablonovitch limit [513], and (iii) diffraction: periodic
3400 pattern. The periodic designed pattern is brought about by hot embossing or nanoimprint

3401 technology [455,514], photolithography plus etching [515], and direct pattering of the hard
3402 substrate, such as glass [499]. The highest cell performance is still dominated by substrates
3403 with random textures. A very recent study indicates that for thick cells with thickness in the
3404 range of or higher than the wavelength of light, also called as geometric thickness, the
3405 random structures will provide excellent light trapping effect. However, for thicknesses much
3406 smaller than wavelength of light, a designed structure is needed to obtain higher current than
3407 the random structure [516].

3408 There are a number of techniques to manipulate the light behavior in a solar cell using
3409 the light interaction at the interfaces of materials of dissimilar refractive indices. The novelty
3410 here is to gain absorption without developing macroscopic textures that have adverse effect
3411 on the growth of the absorber material, and lead to micro/macro defect states. Moreover, very
3412 thin absorber layers can be used without the fear of shunting. Plasmonic effect of light
3413 interaction at the interface of a metal (negative refractive index) and dielectric material
3414 (positive refractive index) is exploited by embedded metallic nanoparticles/structures in a
3415 solar cell [517]. The near field effect of increased absorption and the plasmon polariton
3416 propagation of waves perpendicular to the length of the cells, bring down the necessary
3417 thickness for the cell, whereas the scattering from the plasmonic structures additionally
3418 benefit even thicker cells.

3419 One of the positive outcomes of the research on designed substrate texture
3420 architecture has been the development of almost any design and fine structure on any type of
3421 substrate [518]. This has allowed for the fabrication of high-efficiency solar cells on
3422 temperature sensitive substrates, such as cheap plastics PET, PEN [519], PC [520] etc. These
3423 have temperature limitations due to their glass transition temperatures being less than 150°C,
3424 which is much lower than the optimum deposition temperature (~200°C) of amorphous, or
3425 nc-Si:H material.

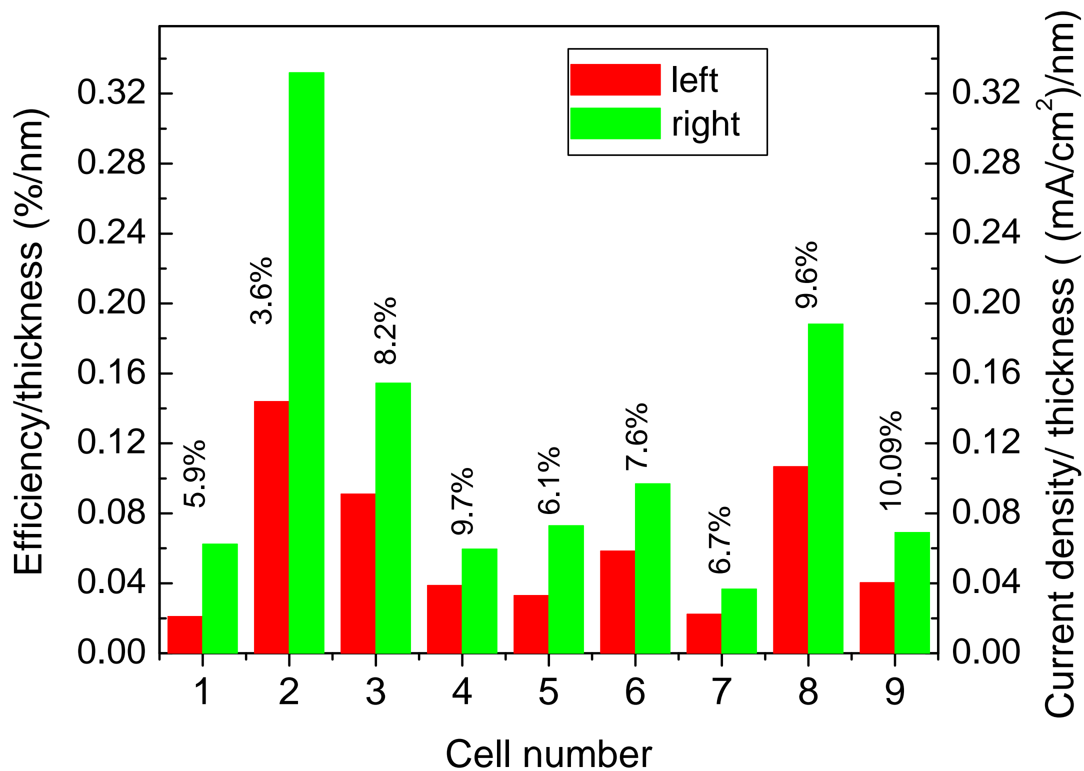
3426 # 7.6 Current trend

3427 Not withstanding all the developments that have taken place for a-Si:H cells (see Sec.
3428 7.2), efficiency is still an issue. The best stabilized efficiency for a triple-junction is still
3429 much lower than the best that CdTe (21% First Solar [521]) or CIGS (21.7% ZSW [522])
3430 cells can deliver. Even with significant efforts, the defect density for a-Si:H and nc-Si:H
3431 intrinsic layers are still in $10^{15}/cm^3$ range, and a-SiGe:H has even more than an order higher
3432 defects. Moreover, light induced degrdation issue of amorphous materials still persists. In the
3433 last few years, there has been limited research in the material side, and efforts have been
3434 directed towards the passive parts of the cells structure, mostly the optical design and light
3435 trapping. It has now been realized that with the best design used so far (solar cell on textured
3436 surface), the efficiency cannot be increased much further [523]; nc-Si:H growth limits the
3437 maximum root mean square roughness and opening angle of the surface feature that can be
3438 used, whereas the defect density limits the thickness of the a-Si:H and a-SiGe:H layers.
3439 Hence, new unconventional designs are being developed, of which two extreme cases are
3440 presented below; solar cells on (i) high aspect ratio structures, and (ii) flat surface.

3441 ## 7.6.1 Extremely thin cells

3442 Traditionally, light trapping schemes, such as that described in the above section, are
3443 employed to mitigate the adverse effect of lower quality of a-Si:H layers compared to
3444 crystalline counterpart that compels the allowed thickness of the a-Si:H or nc-Si:H solar cells
3445 to be much smaller than the penetration depth of visible light. Industries, as well as research
3446 laboratories, are aiming for better stabilized efficiencies that are achieved with thinner cells.
3447 TEL Solar clearly identified this strategy as they brought out ThinFab and popularized the
3448 concept of Think Thin. The strategy provides higher stabilized module power, and
3449 significantly increases the throughput using thin cells. The 2nd generation ThinFab
3450 (ThinFab™140), presented at the World Future Energy Summit 2012, boasts a CAPEX

3451 below $1.4/$W_p$ (approx. $0.97/$W_p$ for integrated end-to-end manufacturing line at 140MW).
3452 This represents a production cost of only $0.48/W, and electricity generation costs of
3453 $0.10/kWh [457], while providing a decent efficiency of 10.8%. In fact, a very attractive
3454 system cost of $1.4/$W_p$ (ground mounted system) in China has been claimed, which shows
3455 enormous potential in other (sunny) developing countries such as India, Brazil, South Africa,
3456 etc. In this context, industries are now looking for new cell designs (and not an incremental
3457 progress in efficiency) to substantially decrease the tact time.
3458



3459
3460 Fig.63 Efficiency (initial) and current density per thickness of various one dimensional structured a-Si:H solar
3461 cells compared to the record stabilized a-Si:H cell [449] on random textured surface. Cell no. 1-9 (9 as reference
3462 cell) and the corresponding references are mentioned in Table 3. Tandem cell (no. 10 in Table 3) is not
3463 mentioned in this figure. The cells are electrically thin optically thick. Thickness of the absorber layer is smaller
3464 than the diffusion length; this ensures collection of carriers at the contacts avoiding recombination. Anti-
3465 reflection at the top surface and increased absorption due to light trapping in the nanorod arrays result in current
3466 enhancement. The efficiency is still small compared to standard [449] cells on textured surface, mainly due to
3467 low V_{oc} and fill factor resulting from non-conformal growth on the nanorods, especially on sidewalls, leading to
3468 porous regions and shunt paths.
3469

3470 Researchers are now responding to that call by introducing extreme thin cells using
3471 the concept of electrically thin optically thick absorber layers. There are essentially two types
3472 of proposed structures, viz. nanorods [524,525,526] and nanoholes [527,528]. In the first
3473 category, a number of reports are now available with different nomenclatures- nanopillar
3474 [529], nanodome [530], nanorod [524], and nanocoax [531] etc. These types of structures
3475 have been made by either top-down or bottom-up approaches. The details of top-
3476 down/bottom-up growth method can be found in Ref. [16] and Sec. 12. The top-down
3477 approach is suitable for c-Si rod cells. Si nanowire solar cells are made by etching of c-Si
3478 substrates by chemicals [532] or plasma (RIE), and a conversion efficiency reaching 10%
3479 [533] has been achieved. However, bottom-up approach with metal induced c-Si nanorod
3480 solar cells have also been demonstrated [534]. For a-Si:H type of cells, on the other hand, a
3481 bottom-up approach is more suitable. Normally a seed layer is used, and the columnar growth
3482 occurs via a combination of mechanisms, viz. preferential direction growth, and growth on a
3483 catalyst seed. A typical catalyst method uses precipitated metal, such as gold induced vapor–
3484 liquid–solid (VLS) growth process [535,536]. In this VLS process, gold film (3-5 nm)
3485 deposited onto c-Si wafer is heated to form Au-Si alloy islands (droplets). When exposed to
3486 source gas (e.g. SiH_4), these islands decompose source gas, and Si diffuses into droplet and
3487 absorbed. After supersaturation, Si precipitates and SiNW grows out of precipitation [16].

3488 Using Sn catalyst, an efficiency of 5.6% has been reported for a radial junction p-i-n
3489 a-Si:H solar cell on p-type c-Si nanowire [537]. Creating such structures directly on the
3490 substrate (such as glass) is an option.

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3501 Table 3 Thin-film Si cells on one dimensional structures. The efficiency of cells on nanoholes or nanorods have
3502 still not reached the efficiency of cells on standard (~10%) textured surface [449]. However, cells with absorber
3503 thickness below 100nm, even as small as 25nm are encouraging. This is possible due to flexible structure of
3504 amorphous material to form homogeneous coating (though still not fully conformal) on these high aspect ratio
3505 structures. The structures are made either by top-down (etching) or bottom-up (deposition) approaches.
3506
3507

Cell No.	Cell type	Substrate	Intrinsic layer thickness (nm)	Source	Current density (mA/cm^2)	Eff. (%)	Ref.
1	n-i-p (a-Si:H)	Nanodome	280	Stanford University, USA	17.5	5.9	[538]
2	n-i-p (a-Si:H)	Nanorod	25	Univ. Utrecht	8.3	3.6	[525]
3	n-i-p (a-Si:H)	Nanocoax	90	Stanford University+Solasta Inc.+EPFL(IMT), Neuchatel	13.9	8.2	[539]
4	n-i-p (a-Si:H)	nanocone	250	Stanford University/EPFL(IMT), Neuchatel/	14.9	9.7	[540]
5	p-i-n (a-Si:H)	nanotube	185	Stanford University, USA	13.5	6.1	[531]
6	p-i-n (a-Si:H)	nanocone	130	IBM T.J. Watson Research Center, USA	12.6	7.6	[541]
7	p-i-n (a-Si:H)	nanorod	300	Carl von Ossietzky University Oldenburg, Germany/University of Bremen, Germany	11.0	6.7	[526]
8	p-i-n (a-Si:H)	Plasmonic nanoprint	90	Univ. Utrecht/AMOLF	16.94	9.6	[542]
9	p-i-n (a-Si:H) (Reference cell)	Random textured surface	250	EPFL	17.28	10.09	[449]
10	p-i-n Tandem (a-Si:H/ nc-Si:H)	Nanohole (Swiss Cheese)	-	Institute of Physics, Prague+Oerlikon Solar-Lab, Switzerland	10.0	10.3	[528]

3508

3509 Table 3 shows the performance of these one dimensional (1D) cells from different
3510 laboratories. Figure 63 shows the current density and efficiency per thickness of such cells
3511 compared to that in a standard cell structure [449]. The expected high stability of these cells

against light soaking has, however, not been demonstrated yet and making conformal growth on such 1D structure remains a technological challenge.

7.6.2 Flat cells

In order to improve light trapping without macro or microscopic textures that generally lead to defects in the layers grown on them, electrically flat optically rough surfaces have been developed [543]. Flat cells employing a structure of mixed materials of different refractive indices, called flattened light-scattering substrate (FLiSS), have been demonstrated [544] in a nc-Si:H cell (Fig.64). The efficiency obtained for a nc-Si:H cell on FLiSS is comparable to that on a textured surface (efficiency ~8%), however, the V_{oc} and FF are substantially improved. Further improvement in FLiSS is needed to enhance the current to make it comparable or higher than that is obtained on textured surface.

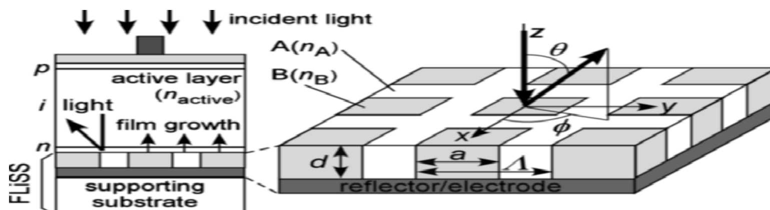


Fig.64 Schematic of a FLiSS (flattened light-scattering substrate or FLiSS) solar cell structure demonstrated in a nc-Si:H cell [544]. In this type of cells, mixed materials with different refractive indices are used. The substrate is a flattened light-scattering substrate, with a high reflective index contrast consisting of two dimensional ZnO grating filled with n-a-Si:H. For a nc-Si:H cell, the FLiSS structure provides substantial improvement in the infrared region (almost comparable to textured surface), while maintaining high V_{oc} and fill factor, which can be obtained only on flat surfaces. With permission from [544], H. Sai, Y. Kanamori, and M. Kondo, Flattened light-scattering substrate in thin-film Si solar cells for improved infrared response, Appl. Phys. Lett. 98 (2011) 113502. Copyright © 2011 American Institute of Physics. License number 3513100577119.

7.7 Industrial competitiveness

One of the industrial successes of a-Si:H is large-scale displays, especially in the 1990s when Si based thin-film PV was in an initial phase. The processing technologies of these large area devices on glass substrates, and the roll-to-roll fabrication on flexible foils have been the main arguments in favor of thin-film Si PV. Applied Materials' SunFab with

3541 5.7m^2 substrate was rolled out to many factories - Moser Baer in India, Signet Solar and
3542 SunFilm in Germany, Masdar Solar in UAE, T-Solar in Spain, Best Solar in China and Green
3543 Energy Technology in Taiwan. The strategy was that large glass would mean faster
3544 throughput, with fewer pieces delivering the same capacity, lowering the cost per watt,
3545 installation costs and BOS savings. As per experience from LCD-display industry, Applied
3546 Materials had seen that every time the glass grew larger, the industry was able to cut costs
3547 dramatically. However this strategy turned out to be a mistake for PV. A SunFab factory
3548 costs about 30% more than standard solar manufacturing equipment- $80 million to $160
3549 million price tag for a single line. Glass this large is hard to handle, and few equipment
3550 manufacturers had tools that could deal with it. Signet, Sunfilm, Green Energy Technology
3551 and T-solar became bankrupt. Most SunFab owners ended up selling largely ¼ sized panels
3552 that were the same size as typical solar panels. In contrast, the competitor, Oerlikon company
3553 was more successful, selling a robust technology on an easily processable substrate (1.4 m^2),
3554 and a high-efficiency double-junction cell processing at a high growth rate, due to its VHF
3555 technology. However, in the meantime TEL Solar has discontinued the solar business since
3556 2014 and many of industries with TEL Solar/Oerlikon equipments have applied for
3557 insolvency- GADIR Solar, S.A in Spain, Pramac in Switzerland (30MW end-to-end turnkey
3558 line), Inventux in Germany, Auria Solar in Taiwan, Schuco Solar in Germany (Oerlikon and
3559 Applied Material SunFab) and Bosch Solar in Germany (30MW).

3560 Roll-to-roll (R2R) technology on flexible substrates has so far shown the best
3561 promise. However it faces stiff commercial and technological challenges. A lower CAPEX,
3562 high-throughput, and simple processing are needed, particularly for low-cost encapsulation
3563 that should have the moisture barrier property comparable to that of glass. Recent reports
3564 show that using a multilayer of inorganic and organic materials made by same hot-wire CVD
3565 technique results in a water vapor transmission rate of 5×10^{-6}g/m^2/day at a temperature of

3566 60°C and a relative humidity of 90%, which will increase the life time of PV to >30 years
3567 [545]. Nuon (the technology previously owned by Akzo Nobel) had to abandon their
3568 indigenously developed R2R technology (Helianthos concept) as it could not commercialize
3569 the product and the new owner of this technology HyET Solar is precisely putting its effort to
3570 make the technology cost-effective.

3571 Though thin-film Si PV manufacturing is currently passing through a trying phase, the
3572 processing has matured, and fast multi-GW large-scale manufacturing is possible once the
3573 bubble of low priced c-Si sector has deflated. Moreover, the problem of light induced
3574 degradation that bothered the industries and investors, has been largely overcome. Applying
3575 all the new developments, such as thin cells, stable materials, and multi-junction, a
3576 degradation of as low as around 4% has been achieved by Unisolar [502].

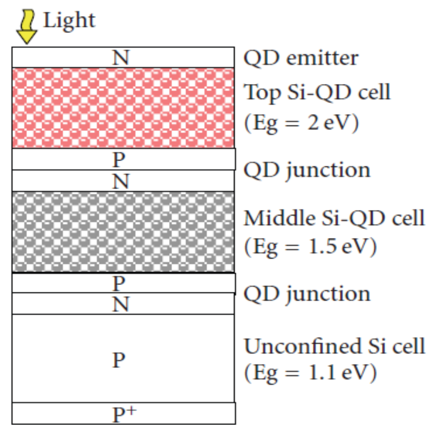
3577 7.8 Looking towards future: Bridge to third generation PV

3578 In order to cross the S-Q limit of solar cell efficiency, several third generation PV
3579 concepts, most of which are still in conceptual phase, have been proposed [546]. The idea is
3580 to increase the efficiency to around 40-60% while keeping the cost of production low by
3581 using thin-films PV fabrication process. A few of these concepts, most relevant to thin-film
3582 Si, are described below.

3583 7.8.1 Hot Carriers

3584 The importance of thin absorber layer in PV cost reduction was discussed in Sec.
3585 7.6.1. One more advantage of this structure is the ability to use a third generation concept of
3586 tapping the hot carriers before they thermalize, which is caused by phonon interaction in the
3587 lattice. This process can substantially increase the V_{oc}. The underlying principle of this type
3588 of solar cell is to slow down the rate of relaxation of photoexcited carriers, which is achieved
3589 by a quantum dot (QD) Si absorber layer, to allow time for carriers to be collected while they
3590 are still at high energies. The collection of carriers is through a selective (narrow) energy

3591 contact, which can be achieved by single (doped) layer of Si QD providing the resonant level
3592 through which carriers can tunnel. A theoretical efficiency of 65% under 1 sun can be
3593 achieved by this solar cell design.

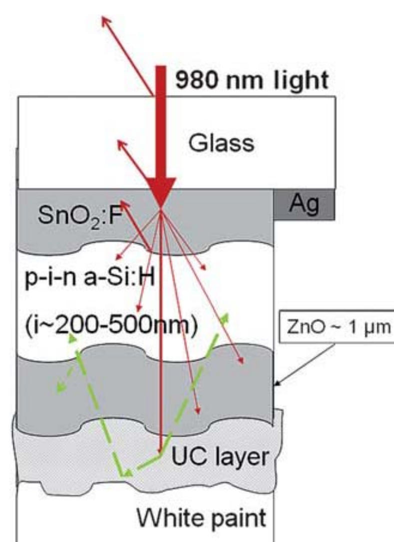


3594
3595
3596 Fig.65 Schematic diagram of proposed quantum dot triple-junction solar cell [547]. The doped layers can be
3597 standard amorphous and microcrystalline thin-films. The Si quantum dot layers can be made either by
3598 deposition of nanoparticles from gas phase by various PECVD processes, or by annealing (solid phase
3599 crystallization) of amorphous materials (a-SiC_x, SiN, a-SiO_x) at high temperature. Monodispersed (<5% size
3600 distribution) Si nanaoparticles of size less than the Bohr's radius (5nm) are embedded in an amorphous matrix
3601 (which acts as a passivation layer in addition to its role in quantum confinement) with spacings that allow
3602 current tunneling. Fully quantum dot cells can be made by using SiGe quantum dot, instead of the conventional
3603 c-Si wafer as the bottom cell. Bandgap is varied by tuning the quantum dot size. Reprinted with permission from
3604 [539], G. Conibeer, Si and Other Group IV Quantum Dot Based Materials for Tandem Solar Cells, Energy
3605 Procedia 15 (2012) 200. Copyright © 2014 Elsevier B.V. License number 3513101114061.
3606

3607 **7.8.2 Quatum dots**

3608 One very promising outcome of the thin-film Si research is the material in which
3609 nanocrystallites are embedded in an amorphous matrix with 50% crystalline volume fraction
3610 that leads to high-efficiency nc-Si:H solar cells. This trend can be developed further by
3611 shrinking the size of the nanoparticles, below the Bohr's radius, and thereby using quantum
3612 confinement. The resulting QD will be a milestone for third generation solar cells where the
3613 various properties of QDs such as decoupling of the electronic states from lattice, discrete
3614 electronic states, direct bandgap nature of light absorption, tuning the bandgap and absorption
3615 profile by tuning the particle size can be exploited. Though a multi-junction structure has
3616 been proposed in the third generation concept, this has been used for thin-film Si over a long
3617 time; in labs and commercial companies triple-junctions using a-Si:H, a-SiGe:H and nc-Si:H

3618 have been made. However, even in lab scale the efficiency has not reached the S-Q limit. It is
3619 expected that the QDs are internally defect free and their surfaces can be passivated using
3620 appropriate shell or embedding in a passivating matrix. This way, bandgap variations can be
3621 made (by appropriate dot size) without increase of defects, which is encountered when
3622 changing bandgap with alloying such as a-SiGe or a-SiC. Figure 65 shows the schematic of a
3623 triple-junction based on QD layers. A theoretical efficiency of 47.5% for such a cell is
3624 expected [546]. Notwithstanding the advantages, the reports so far on solar cell devices with
3625 QDs have not proved their potential. A c-Si/QD-Si heterojunction cell has shown a
3626 reasonable V_{oc} of 0.52V, but a very low fill factor of 0.2. QD superlattice as intrinsic layer in
3627 an n-i-p cell has shown an efficiency of 3.8% with V_{oc}, fill factor and J_{sc} of 518mV, 0.51 and
3628 14.3 mA/cm^2, respectively [548]. One of the causes behind the bad performance (in both c-
3629 Si/QD-Si heterojunction and QD superlattice as intrinsic layer in an n-i-p cell) is that in
3630 phosphorous-doped QD, the structural distortion is less significant than that for boron-doped
3631 case [549], and phosphorous-doping significantly increases the QD size compared to boron-
3632 doping [547]. Defect passivation of the QDs is still an open question. Si QDs have also been
3633 employed in QD sensitized solar cells whose theoretical efficiency is 44% [550].



3634

3635 Fig.66 Schematic diagram of a single-junction a-Si:H cell with upconversion layer [551]. The TCO layers have
3636 to be highly transparent for near-infrared photons (lowly doped), highly conductive (high mobility) and thick to
3637 minimize resistance losses. A non-conducting diffuse back reflector (white paint or foil) instead of Ag is used.
3638 Upconverter powders (e.g. NaYF4: 2% Er3+, 18% Yb3+, dissolved in chloroform with Poly(methyl

3639 methacrylate)) can be drop casted on the back contact. A high bandgap layer with small sub-bandgap absorption
3640 is the most suitable absorber (intrinsic layer) for upconversion cell. This concept is more suitable for high
3641 bandgap absorber materials. Sub-bandgap photons are transmitted through the high bandgap absorber material
3642 used in the cell, and are not utilized for electron-hole pair creation. In upconversion process, two below bandgap
3643 energy photons (transmitted through the cell) are added by the upconcersion layer and converted to a single
3644 photon with higher energy and then reflected back to the bulk of the cell for absorption [15].
3645

3646 **7.8.3 Up conversion**

3647 Light spectrum below the bandgap is lost in a solar cell and this long wavelength
3648 spectrum can be converted to above bandgap, thereby utilizing a part of the unused light.
3649 This third generation concept will be most useful for high bandgap absorber materials where
3650 there is a substantial transmission loss, and a-Si:H, especially the pc-Si:H type cell, is a test
3651 case because of its high bandgap of 1.8-2.0eV [551] (Fig. 66). Using lanthanide type up-
3652 converter materials, up-conversions have been achieved for broad band light. However, for a
3653 realistic improvement, a concentrated light of ~500 suns is needed. Use of up-conversion
3654 based on sensitized triplet–triplet-annihilation in organic molecules at the back side of a-Si:H
3655 cell has shown 1% increase in efficiency at 48 suns illumination [552]. However, a solid state
3656 material by a deposition technique is most desirable. One of the solutions to capture a wide
3657 spectrum by a broad band absorption can be achieved by using quantum dot sensitizers or
3658 transition metal ions, which emit at the resonance energy of the up-converter. The latter
3659 (transition metal ions) is yet to be experimentally successfully demonstrated, but the former
3660 has shown promise; QDs absorb over a broad spectral range in the IR, and emit in a narrow
3661 line, e.g. around 1520 nm, resonant with the Er^{3+} upconversion wavelength to which it makes
3662 a radiative transfer [553]. Use of plasmonic structure to either increase the absorption
3663 strength or emission has also been proposed and has also been shown as proof of concept.
3664 One more technique is to use nanofocussing to achieve the light concentration. This can be
3665 done externally using nanolenses, or internally through nanafocussing at a tapered metallic
3666 structure at its edge [554].

3667

7.9 Future outlook

Thin-film Si based PV technology, like all other thin-film technologies, will continue to face commercial pressure from Si wafer based PV for some time to come and will mostly cater to the niche market. These include small power sources in consumable goods, in addition to a dedicated market in building integration, thanks to its aesthetics. Once the dominance of c-Si PV eases, thin-film Si PV technology market is expected to expand rapidly, as this is the most matured and robust technology positioned to upscale. Gigawatt level production is possible with its technology with relatively small effort. In this regard, the large display size solar panels and long rollable modules will be preferred choices because of the maturity of the fabrication process and technology.

As far as absorber material is concerned, a new direction on deposition/fabrication is needed. At present, the stabilized efficiency of single-junction cells, whether a-Si:H or nc-Si:H, is far below (less than half the S-Q limit) the theoretical optimum efficiencies for the respective band gaps. The stabilized efficiencies of even triple-junction cells are around one third of the theoretical efficiency of multi-junction. However, considering the enormous room for improvements in defect density, mobility, etc., considerable scientific interest remains for long-term efforts. Production of nanowires and quantum dots will be of enormous scientific interest, however, multi-junction solar cells based on quantum dots, notwithstanding their potential for high-efficiency beyond S-Q limit, will remain academic for some time to come, just as other third generation concepts.

In terms of industrial production, a-Si:H will remain central to SHJ type solar cells. However, as far as pure thin-film Si PV is concerned, there are challenges ahead. There are ongoing efforts on implementing these type of cells along with others to fabricate parallel connected (e.g. two terminal devices with optical couplers or honeymoon cells) devices. The previous decade had experienced great success in developing the passive parts of thin-film Si

3693 cells, especially optical management and light trapping effects, which included nano-textured
3694 surfaces, nanowall/nanopillars and plasmonic effects. Many of these were developed by
3695 groups specializing in optical studies, not necessarily experts in solar cells and device
3696 fabrication. The knowhow of many of these effects is currently being incorporated in solar
3697 cells. Industrial fabrication processes implementing these optical enhancing effects may soon
3698 be developed. This will be the best possible way to increase stabilized cell efficiency to 15%,
3699 which will make the thin-film Si based PV truly industrially competitive. The solar cells on
3700 flexible foils, especially plastics, still remain one of the most fascinating inventions in thin
3701 film silicon based solar cells. It is to be seen how low-cost encapsulating moisture barrier
3702 layers develops in near future to make the plastic solar cells a real success, opening up
3703 applications in wide ranging areas, especially large roof tops.

3704 8.0 CZTSSe (Kesterite) Solar Cells

3705 The desire for large-scale PV technology based on environmentally friendly, low-cost
3706 absorber compatible with high-throughput fabrication has resulted in an increased research
3707 interest in the kesterite-type $Cu_2ZnSn(S,Se)_4$ systems known as CZTS (or CZTSSe in some
3708 cases when Se is present). With similar optoelectronic properties to high-efficiency CIGS and
3709 CdTe materials, and at the same time devoid of highly toxic (such as Cd) and high-demand
3710 rare elements (such as indium), this material has produced solar cells with steadily increasing
3711 efficiency during the recent years [555]. Remarkably, CZTSSe progress has been accelerated
3712 by chemical ink-based approaches surpassing in performance classical high-vacuum
3713 techniques and pushing the efficiency record of these materials by about 1 absolute % per
3714 year up to its current level of 12.6% [556-559] . The combination of these advantages
3715 together with a huge potential for improvement has motivated an expanding volume of
3716 studies, ranging from kesterite synthesis to advanced materials and device modeling. A
3717 number of detailed works have already provided exhaustive coverage of the significant body

of literature on the subject [555,560,561]. Here we will focus on the key aspects of CZTSSe material and device developments during the recent years, analyzing the main challenges ahead of currently one of the most tempting and complex PV absorber materials.

8.1 CZTSSe materials

Copper zinc tin sulfide (Cu_2ZnSnS_4) was conceived in the 1980s as a promising PV material to provide alternative to indium-based chalcopyrites such as $CuInSe_2$ and later $Cu(In,Ga)(S,Se)_2$ that at the time were reaching 11% efficiencies, close to the 2013 efficiency values of CZTSSe devices [562]. The material comprises a next level of evolution of the adamantine (i.e. diamond-like) family of analogous structures where 4-valence atoms are consecutively substituted with isoelectronic combinations of growing complexity, for example [563], carbon (or Si)→ZnS→$CuInS_2$→$CuZnSnS_4$ (Fig.67). The substitution of indium (III valence) in the chalcopyrite with Zn (II valence) and Sn (IV valence) in kesterite results in very similar optoelectronic properties – i.e. high absorption co-efficient due to direct bandgap, tunable from approximately 1eV to 1.5eV with varying S/Se ratio, the lowest values corresponding to pure selenide and the highest to pure sulfide materials.

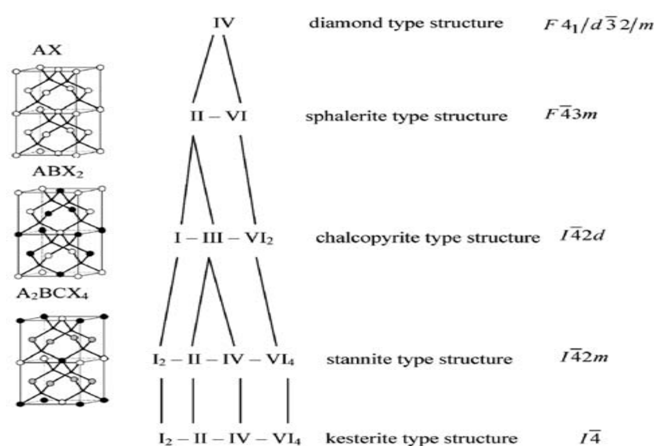


Fig. 67 Schematic diagram of a part of the adamantine compound family, including kesterite materials. Isoelectronic combinations of different atoms are substituting Roman numbers indicate the valence state of the cations (big spheres A,B,C) and anions (small spheres) respectively. The sum of the valences at each step is double the sum of the previous. The structure models at the left side are (from top to down) the sphalerite-type structure, the chalcopyrite-type structure and the stannite-type structure. CZTS is a kesterite material used as absorber in the CZTS solar cell due to its high absorption co-efficient, optimum bandgap of around 1.5eV, and its elemental constituents are earth-abundant. Reprinted from Ref. [563], S. Schorr, Structural aspects of

3741 adamantine like multinary chalcogenides, 515 (2007) 5985. Copyright © 2014 Elsevier B.V. Permission
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3743

3744 The dilemma whether to use the classical sulphide or selenide or mixed materials is
3745 similar to that in chalcopyrite technology. On the one hand, sulfur is more benign and orders
3746 of magnitude more Earth-abundant than Se – therefore the natural choice for large-scale
3747 environmentally friendly manufacturing. On the other hand, Se-based materials produce
3748 higher-quality polycrystalline layers and are more tolerant to processing conditions. Neither
3749 long-term availability of Se nor its potential toxicity has yet been viewed as a major limiting
3750 factor for the growth of PV technologies employing it. Se is a largely unused byproduct from
3751 Cu refining and, although harmful in excessive concentrations, is a key micronutrient for
3752 living organisms. An important advantage of mixed sulfoselenide alloys is the ease of
3753 controlling the bandgap from about 1eV (pure selenide) to about 1.5eV (pure sulfide)
3754 analogously to $CuIn(SSe)_2$. The use of the pentanary $Cu_2ZnSn(S,Se)_4$ system allows to take
3755 advantage of the optical and materials quality benefits of the combination of S and Se and has
3756 been employed in the highest-efficiency CZTSSe devices to date [558,559].

3757 The high complexity of the kesterite materials makes them particularly vulnerable to
3758 secondary phase formation – a major challenge for the fabrication of high quality absorbers.
3759 The high temperatures (over 500°C) required for device-quality kesterite film crystallization
3760 [564,565] combined with the high volatility of multiple intermediate species are a serious
3761 challenge [566] for CZTSSe (not only S and Se as in CIGS technology, but also of elemental
3762 Zn and Sn chalcogenide phases). Materials optimization is made even more difficult by the
3763 fact that the two of the most likely secondary phases, viz. Zn(S,Se) and $Cu_2Sn(S,Se)_3$ are
3764 difficult to distinguish by standard characterization techniques such as x-ray diffraction
3765 (XRD) due to peak overlap with the targeted CZTSSe. Raman scattering [567,568] and other
3766 techniques such as neutron diffraction [569] and x-ray absorption near edge structure
3767 [570,571] have been successfully used for phase detection, although there is still a need for

3768 further development of techniques for routine and reliable secondary phases detection in
3769 CZTSSe, especially in the pentanary system.

3770 Some secondary phases can be more detrimental than others. Generally, secondary
3771 phases with bandgaps lower than CZTSSe (for example $Cu_2Sn(SSe)_3$, bandgap of 0.8-1eV),
3772 are considered particularly undesirable as they reduce the V_{oc} of the device. It has been
3773 pointed out that the presence of a material with a bandgap lower by only 100meV will reduce
3774 the maximum achievable efficiency by 8% absolute [561]. High-conductivity phases, such as
3775 $Cu_x(S,Se)$ are especially damaging performance well due to their shunting effect. Similarly to
3776 chalcopyrite PVs employing CIGS or $CuInS_2$, they must be avoided by relying on a Cu-poor
3777 absorber or removal techniques such as potassium cyanide (KCN) etch [572,573].

3778 Phases with higher bandgap than CZTSSe are considered less detrimental [561] but
3779 may have negative impact in specific locations – for instance Zn(S,Se) (bandgap of 2.7-
3780 3.8eV) in the bulk of the film is much less harmful than on the absorber surface [574]. HCl
3781 etch has been successfully applied to remove surface Zn excess leading to improved V_{oc}
3782 [575]. Tin chalcogenides, Sn(S,Se), may have different impact depending on exact
3783 composition, while SnSe has a relatively high bandgap of 1.3eV and may have little effect on
3784 device performance, SnS has an indirect bandgap of 1eV and can be potentially harmful
3785 [561]. This could be one of the reasons why pure sulphide CZTSSe has lower maximum
3786 efficiency than materials with higher Se content.

3787 All above considerations are in empirical agreement with the currently best strategies
3788 for high-efficiency devices that employ mixed S-Se materials with slightly Zn-rich and Cu-
3789 poor composition [558,559].

3790

3791 ## 8.2 Fabrication approaches

3792 Numerous vacuum and non-vacuum CZTSSe fabrication approaches have been
3793 reported [555,556,572,576,577]. One distinguishing property of these materials is Sn-

3794 chalcogenide volatility, especially at high-temperature and in vacuum. This has made direct
3795 process such as co-evaporation at high substrate temperature very difficult to optimize CZTS
3796 films, which was possible with CIGS. Currently, the most successful CZTSSe fabrication
3797 processes are two-step vacuum and non-vacuum deposition techniques where the high-
3798 temperature (over 500°C) crystallization step is done at atmospheric pressure.

3799 The first report on the deposition of CZTSSe films by employing sputtering from
3800 quaternary targets and its use in PV device was performed by Ito and Nakazawa in 1988
3801 [562]. Katagiri et al. [578] employed sputtering from metal targets to systematically study an
3802 extensive matrix of composition and processing parameters. Careful optimization determined
3803 the beneficial Cu-poor, Zn-rich composition, and with the demonstration of 5.75% efficiency
3804 in 2007 [579] that was increased later to 6.8% by simple wet etching technique [555,580],
3805 triggered a rapid growing research interest in CZTSSe PV. Among numerous other reports on
3806 sputtering, the company Solar Frontier has reported the highest efficiency of 9.2% that was
3807 furthermore measured over the total area of a 25cm^2 mini module [581].

3808 Co-evaporation at high substrate temperature was the technique used for the first time
3809 to demonstrate over 2.3% efficient CZTSSe solar cell in 1997 [566] at the University of
3810 Stuttgart, highlighting for the first time the Sn-loss challenges mentioned above. Fast co-
3811 evaporation helped mitigate this issue and increase the efficiency to 4.1% [582]. Recently the
3812 National Renewable Energy Laboratory team was able to adapt their high-performance CIGS
3813 co-evaporation process to CZTSe, reaching 9.2% efficiency by maintaining temperatures no
3814 higher than 500°C and providing higher Sn flux throughout the whole process [583]. The
3815 same group reported that, similarly to CIGS, Na incorporation in CZTSe has strong impact on
3816 the electronic properties [584]. Successful grading of the composition to create advantageous
3817 bandgap profile similarly to highest performance co-evaporated CIGS has not been reported
3818 yet.

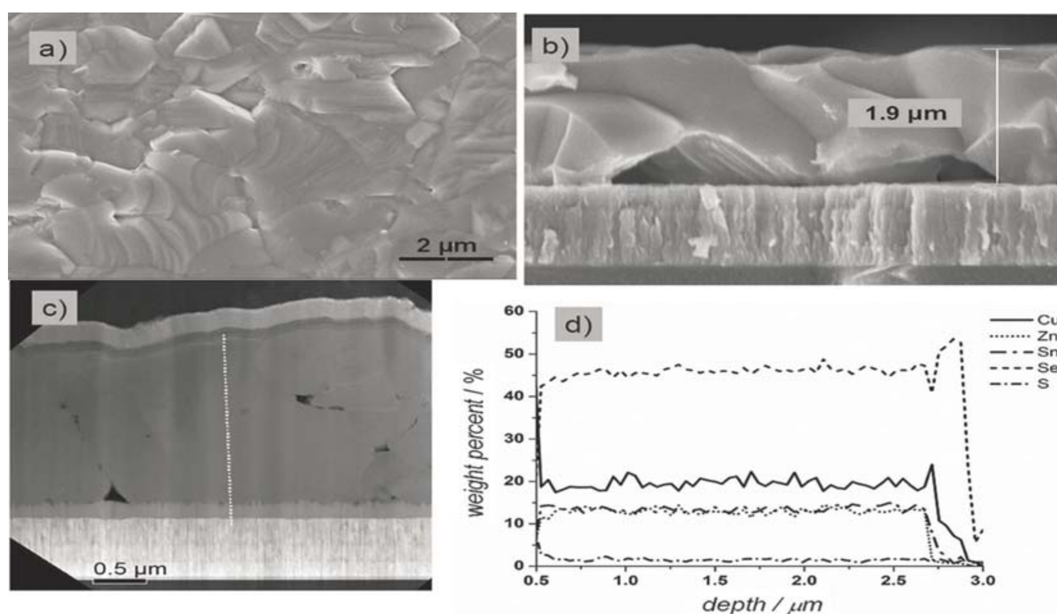
3819 Sequential processes based on evaporation at relatively lower temperature (<200°C)
3820 followed by high-temperature (>500°C) crystallization step have also lead to successful
3821 CZTSSe developments. The first one in this category was reported in 1997 by employing
3822 500°C sulfurization of Zn/Sn/Cu stacks. It yielded 0.66% efficiency [585], which was later
3823 improved to 5.45% by Na incorporation together with optimization of other parameters [586].
3824 The impact of Sn vapor pressure during the high-temperature crystallization step of CZTS
3825 precursors was demonstrated by using sealed-tube anneal with a small amount of Sn source,
3826 where an efficiency of 5.4% was observed [587]. The highest efficiency pure sulfide CZTS
3827 devices were developed at IBM by co-evaporation followed by anneal and have reached 8.4%
3828 [588]. Mixed sulfoselenides by a similar process have demonstrated 8.9% efficiency by use
3829 of TiN diffusion barrier at the back contact [576].

3830 Electrodeposition is a mature industrial non-vacuum deposition technique, attractive
3831 for large-scale CZTSSe manufacturing. Single step and multi-step electrodeposition of
3832 CZTSSe thin-films have been reported [572,573,589,590]. Stacked metal precursor layers,
3833 subjected to sulfurization and KCN etch yielded 3.2% efficiency [572]. Co-electrodeposited
3834 Cu-rich metal precursors, with KCN etching to remove copper sulfide reached 3.4% [573].
3835 IBM process based on electrodeposition of stacked elemental layers with subsequent
3836 sulfurization has reached 7.3% efficiency [590].

3837 Ink-based fabrication processes are compatible with ultrahigh-throughput fabrication
3838 techniques such as printing and casting. Different ink approaches based on solutions,
3839 nanoparticle suspension and mixed solution-nanoparticle slurries could offer unprecedented
3840 scaling potential to CZTSSe.

3841 The first report on nanoparticle CZTSSe deposition involved hot reaction in ethylene
3842 glycol [591]. Guo et al. [592] employed higher-temperature hot injection in oleylamine, and
3843 achieved 7.2% efficient devices. This value was later increased to 8.5% by use of binary zinc

3844 sulphide (ZnS) and ternary copper tin sulphide (Cu_2SnS_3) particles that were subjected to
3845 selenization [593]. Hybrid solution-nanoparticle slurries in hydrazine based on dissolved Cu-
3846 Sn-S-Se systems and dispersed Zn-Se phases were developed at IBM, and reached a
3847 breakthrough 9.66 % efficiency in 2010 [556]. The method was further improved to yield
3848 10.1% [557] and recently achieved CZTSSe efficiency of 11.1% [558]. Figure 68 shows the
3849 pinhole-free large-grained microstructure of these materials. The absorber thickness is close
3850 to 2 μm and the elemental distribution measured by energy-dispersive x-ray spectroscopy
3851 (EDX) is flat across the film. It must be noted that contrary to CIGS, with CZTSSe no reports
3852 on successful elemental grading targeting bandgap engineering for enhanced efficiency has
3853 been reported to date. This however, as will be shown below, is not the main performance-
3854 limiting factor so far, as efficiencies over 15% [594] have been achieved with CIGS even
3855 with flat elemental profiles.



3856

3857 Fig. 68 Record efficiency of 11.1% [558] CZTSSe device: (a) SEM top-view, (b) cross-section, (c) TEM cross -
3858 section, and (d) EDX depth profile. A common feature of high-efficiency kesterite devices is the predominant
3859 presence of large grains, spanning from the top to the bottom of the film. Voids within the layer and near the
3860 back contact appear to be benign. Composition profile is relatively flat across the film despite efforts to produce
3861 gradients for band gap engineering. Figure 68 from [558], Teodor K. Todorov, Jiang Tang, Santanu Bag, Oki
3862 Gunawan, Tayfun Gokmen, Yu Zhu and David B. Mitzi, Beyond 11% Efficiency: Characteristics of State-of-
3863 the-Art $Cu_2ZnSn(S,Se)_4$ Solar Cells, Advanced Energy Materials, 3 (2013) 34. Copyright © 2013 WILEY-VCH

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Pure solution inks potentially have advantages for uniform synthesis of multinary compound layers over particle-containing systems due to greater homogeneity at a molecular scale, as well as reduced probability for aggregate formation causing coating defects. Pure solutions of metal salts and thiourea in dimethyl sulfoxide have been used to achieve 4.1% efficient devices [595]. CO_2 solutions in hydrazine (forming hydrazinocarboxylic acid) were successfully used to dissolve Zn species in hydrazine-based inks, yielding 8.1% efficient devices [593]. Another pure solution approach for hydrazine systems based on substitution of elemental Zn with Zn salts was developed with reported efficiency of 10.6% [596].

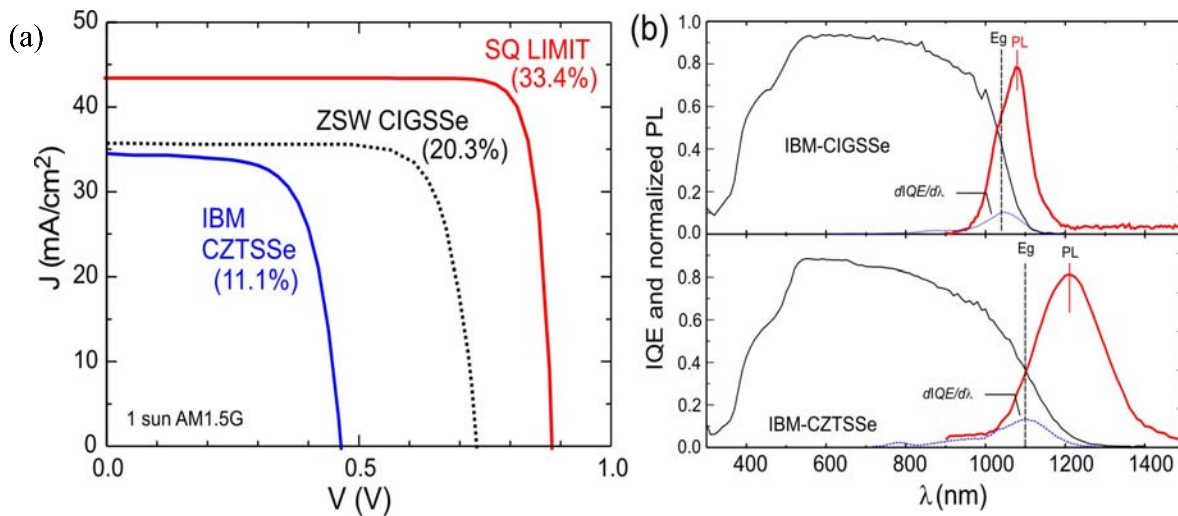
8.3 Device Characteristics

Here, we review device characteristics of the high performing CZTSSe cell and benchmark it against the high performing CIGSSe cells, as well as a hypothetical S-Q single-junction solar cell (S-Q limit cell) to understand the key problems in the current generation of CZTSSe cell. We will discuss the general device characteristics of CZTSSe (Sec.8.3.1), including the V_{oc} deficit issue (Sec. 8.3.2), which is among the leading challenges facing CZTSSe technology.

8.3.1 Electrical Characteristics

Figure 69 shows the (a) J-V curve, (b) IQE and photoluminescence (PL) spectra of CZTSSe and CIGSSe solar cells. Table 4 shows the J-V characteristics of an example of leading CZTSSe (IBM-CZTSSe) device with efficiency of 11.1% [558], the leading CIGSSe cell (20.3% efficiency) from Zentrum für Sonnenergie-und Wasserstoff-Forschung (ZSW), Germany [597] and the S-Q limit cell with the same bandgap (1.13eV) (similar discussions will also apply to the current CZTSSe record efficiency of 12.6%). This S-Q limit cell presents the ultimate limit of a single-junction solar cell based on S-Q limit calculation

3891 [22,598]. In Table 4, we also present electrical characteristics of a high performance CIGSSe
3892 cell (IBM-CIGSSe) with 15.2% efficiency made by analogous hydrazine-based processing
3893 [594]. The bandgap in these cells are determined from the inflection point (i.e. the maxima of
3894 |dQE/dλ| curve) of the QE curve near the bandgap cut-off wavelength [599]. In order to
3895 perform a fair comparison of J_{sc} and V_{oc} among these cells with little variation in bandgap,
3896 V_{oc} deficit value, i.e. $V_{oc\ def} = E_g/q - V_{oc}$ and normalized J_{sc} value, i.e., $J_{sc,N} = J_{sc}/J_{sc,\ MAX}$
3897 where $J_{sc,\ MAX}$ is the J_{sc} of an S-Q limit cell or the maximum J_{sc} assuming a 100% EQE, are
3898 monitored.



3899

3900 Fig. 69 (a) J-V characteristics of IBM-CZTSSe, ZSW-CIGSSe leading cells, and a S-Q limit cell with similar
3901 bandgap (1.13 eV). The S-Q limit is calculated for a single-junction cell with AM1.5G illumination. (b) internal
3902 quantum efficiency and the photoluminescence spectra (red curve) at room temperature of the 11.1% IBM-
3903 CZTSSe [558] and the 15.2% IBM–CIGSSe cells [594]. The bandgap (marked as E_g) is determined from the
3904 inflection point (or the maximum slope) of the external quantum efficiency curve. Fig. 69 (b) reproduced from
3905 Ref. [600], Tayfun Gokmen, Oki Gunawan, Teodor K. Todorov and David B. Mitzi, Band tailing and efficiency
3906 limitation in kesterite solar cells, Appl. Phys. Lett. 103 (2013) 103506. Copyright © 2013 AIP Publishing LLC.
3907 Permission granted.

3908

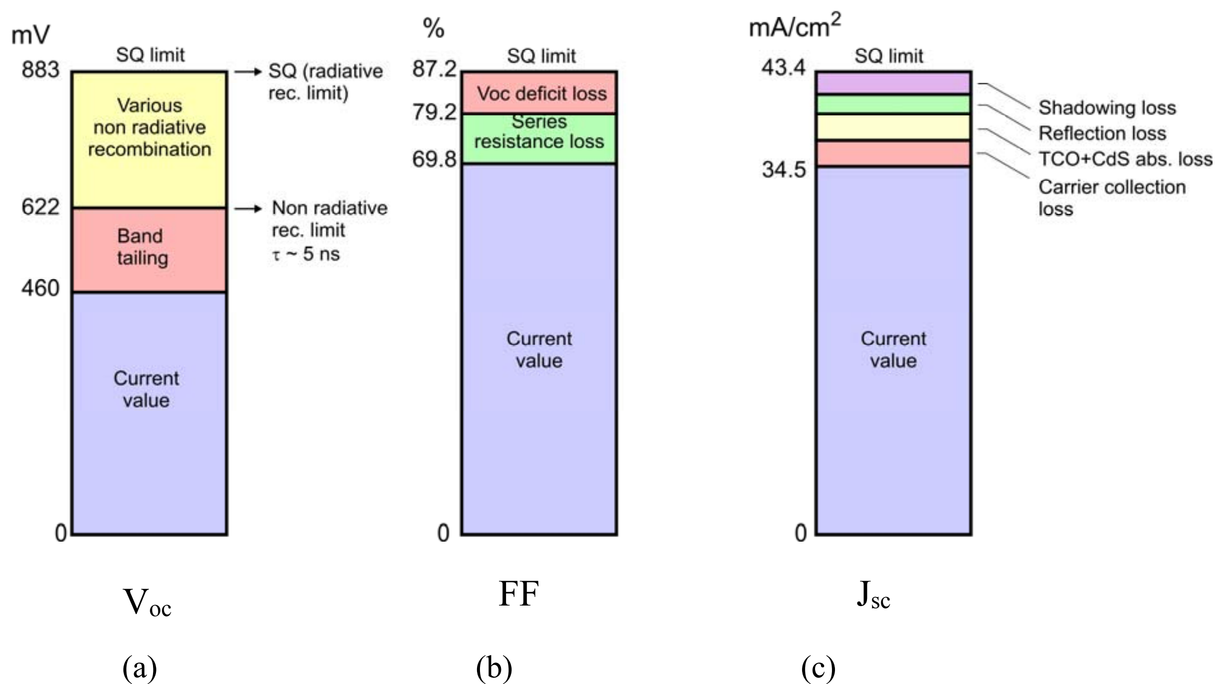
3909 Table 4. Device performance of leading CZTSSe and CIGSSe (from IBM and ZSW respectively) based solar
3910 cells. The parameters R_{SL}, A, and J_0 respectively are series resistance under light, diode ideality factor and
3911 reverse saturation current determined using Sites' method [601]. $J_{sc,N}$ and $V_{oc,def}$ are normalized J_{sc} and V_{oc}
3912 deficit, respectively (see text).

3913

3914

Solar cell	V_{oc} (V)	J_{sc} (mA/ cm^2)	Fill factor	Eff. (%)	E_g (eV)	$J_{sc,N}$ (%)	$V_{oc,def}$ (V)	R_{SL} (Ω)	Area (cm^2)	J_o (mA/cm^2)	Ref.
IBM-CZTSSe	0.460	34.5	69.8	11.1	1.13	79.5	0.670	0.40-0.60	1.48	1.34×10^{-4}	[558]
IBM-CIGSSe	0.623	32.6	75.0	15.2	1.16	78.2	0.547	0.75	1.49	9.8×10^{-6}	[594]
ZSW-CIGSSe	0.730	35.7	77.7	20.3	1.14	83.2	0.410	0.23	1.38	4.2×10^{-8}	[597]
SQ 1.13 eV	0.883	43.4	87.2	33.4	1.13	100	0.247	0	1	4.55×10^{-14}	-

3915

3916 

3917 V_{oc} FF J_{sc}

3918 (a) (b) (c)

3919 Fig. 70 breakdown analysis of various loss mechanisms diagram of the 11.1 % CZTSSe cell [558] benchmarked
3920 against S-Q limit: (a) V_{oc}, (b) fill factor (FF), and (c) J_{sc}. V_{oc} deficit is the number one problem in CZTSSe
3921 technology and is mainly attributed to various non-radiative recombination, interface recombination, bulk
3922 recombination, back contact recombination and band tailing. The second dominant factor is the fill factor loss
3923 attributed to the V_{oc} loss, and series resistance losses from various sources such as metal contact resistance, bulk
3924 resistance, potential barrier across the contact, and grain boundaries. For higher bandagp or higher [S]/[Se] ratio,
3925 series resistance tends to increase. The last and least loss factor is the J_{sc} loss which is attributed to the common
3926 loss factors in thin film solar cells.

3927 We have performed a more detailed breakdown analysis of various loss mechanisms
3928 for the IBM-CZTSSe cell in the frame work of S-Q limit as shown in Fig. 70. The leading

3929 CZTSSe cell has V_{oc} at 52.1%, fill factor at 80.0% and J_{sc} at 79.5% of the S-Q limit cell. It is
3930 clear that the V_{oc} deficit (Fig. 70 (a)) is the number one problem in the current generation
3931 CZTSSe. We will discuss factors that account for this V_{oc} deficit in more detail in later
3932 section.

3933 Second issue is the shortcoming of fill factor. A majority of the fill factor loss is due
3934 to various sources of series resistances (Fig. 70b) that accounts for 9.4 % absolute from the of
3935 S-Q limit fill factor such as top metal contact resistance, bulk resistance across the film,
3936 current blocking secondary phase like ZnS(e) [602] and possible potential barrier
3937 contribution across back contact or grain boundaries [603]. Note that the CZTSSe series
3938 resistance tends to increase with higher bandgap, or with higher [S]/[Se] ratio. Overall, the
3939 series resistance of IBM-CZTSSe is comparable, even slightly better, than the analogous
3940 hydrazine-processed IBM-CIGSSe device (Table 4). The lowest series resistance (R_S ~0.2Ω-
3941 cm^2) is found in selenide (no sulfur) kesterite CZTSe cell with lowest bandgap [583,604].

3942 Another contribution of the fill factor losses is accounted by V_{oc} deficit loss [Fig.
3943 70(b), 8% absolute the maximum fill factor], as low V_{oc} value also inadvertently drags down
3944 the fill factor. The maximum possible fill factor at a given V_{oc} can be calculated by the
3945 following phenomenological relationship [605]:

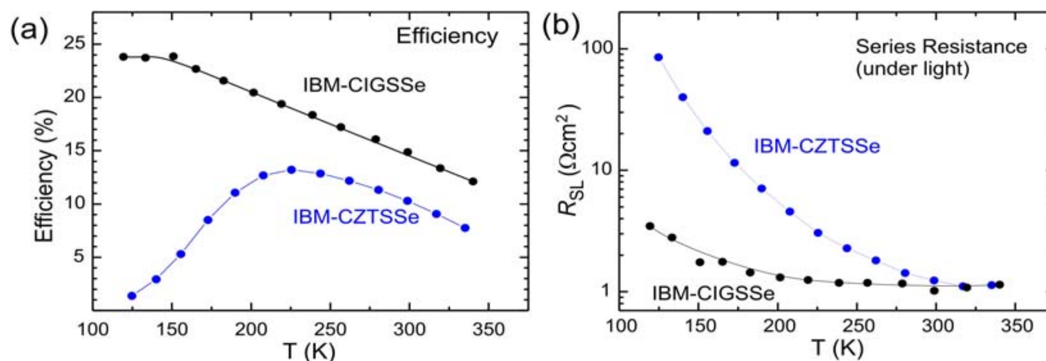
3946 Fill factor = $[V_{OC,N} - \ln(V_{OC,N} + 0.72)]/(V_{OC,N} + 1)$, where $V_{OC,N}$ is the normalized V_{OC}, and

3947 $V_{OC,N} = qV_{OC}/Ak_BT$, with q is the electronic charge, A is the diode ideality factor, k_B is the
3948 Boltzmann constant and T is the temperature.

3949 CZTSSe has a dramatically different temperature characteristics at low-temperature
3950 compared to that of CIGSSe. Figure 71(a) shows that the CZTSSe efficiency collapses at
3951 low-temperature (T <150K) while in contrast the CIGSSe cell efficiency keeps increasing.
3952 The series resistance diverges as much as 100 times from 340K to 120K [603] as shown in

3953 Fig. 71(b). This causes a drastic collapse in fill factor, and correspondingly a decrease in
3954 observed efficiency [603,606]. This effect is suspected due to dielectric freeze out effect in
3955 the bulk CZTSSe [607] because of the absence of shallow acceptor in CZTSSe [607,608].
3956 This is consistent with the theoretical calculation using density functional theory that suggests
3957 Cu_{Zn} antisite as the dominant, deep acceptor defect in CZTSSe [608,609]. Bandgap
3958 dependence study indicates that this defect level increases with increasing bandgap or sulfur
3959 content [607,610]. An alternative view suggests the presence of secondary phase ZnS(e) at
3960 the absorber/buffer interface limits the transport across the cell and causes this divergence in
3961 series resistance [602].

3962 The J_{sc} of IBM-CZTSSe cell is surprisingly very good, with $J_{sc,N}$ value slightly better
3963 than that of the IBM-CIGSSe cell. This is most likely a fortuitous effect of the tail states in
3964 CZTSSe that extend the absorption below the CZTSSe bandgap [600]. The effect of the tail
3965 states is visible in the QE curve as shown in Fig. 69(b) where we observe more tailing in the
3966 CZTSSe QE curve around the bandgap cut-off wavelength. Several factors still affect the
3967 IBM-CZTSSe J_{sc} compared to the S-Q limit J_{sc}. These are shadowing loss of the top metal
3968 grid, reflection loss mainly from the top stack, absorption loss of the TCO and cadmium
3969 sulphide (CdS) layer and carrier collection losses in the bulk, which is apparent from lower
3970 QE response at long wavelength near the bandgap cut-off wavelength. Each of these
3971 components accounts for about 4-5% loss with respect to the maximum J_{sc}.



3972

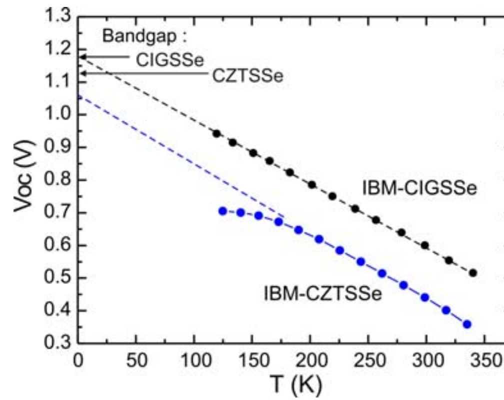
Fig. 71 Temperature dependence of (a) efficiency, and (b) series resistance under light condition of the IBM-CIGSSe versus IBM-CZTSSe solar cells. The measurement is performed in a liquid nitrogen cooled cryostat under simulated 1 sun AM1.5G illumination. CIGSSe cell efficiency keeps increasing even at low-temperature. Compared to CIGSSe, at low-temperature, CZTSSe has different temperature characteristics. Cell efficiency decreases rapidly at low tempearature (<200K) which is related to the divergence in series resistance and drastic decrease in fill factor. This effect is attributed to the freeze-out effect in the CZTSSe absorber film due to the loss of free carrier at low-temperature which can be attributed to the deep acceptor level in CZTSSe. As can be seen in (b), CZTSSe series resistance diverges about 100 times from 340K to120K.

8.3.2 The V_{oc} deficit in CZTSSe

The high V_{oc} deficit ($V_{oc,def} = (E_g/q)-V_{oc}$) is among the biggest challenges facing CZTSSe-based solar cell, and thus merits a special discussion. Several factors account for severe V_{oc} deficit in CZTSSe solar cell. They can be categorized into two major loss components as shown in Fig. 70(a): (i) non-radiative recombination, and (ii) band tailing effect.

The majority of the V_{oc} deficit loss is accounted for by non-radiative recombination (~25% of S-Q limit V_{oc}). Several factors contribute to this loss components, such as interface recombination (that may also induce Fermi level pinning at the interface) and bulk recombination due to electrically active defects and back contact recombination.

We study the V_{oc} versus temperature characteristics of the CIGSSe and CZTSSe, as shown in Fig. 72. The activation energy of the dominant recombination process can be obtained (assuming a constant diode ideality factor) from the intercept of the V_{oc} versus T extrapolation line at 0K [603,611]. The IBM-CIGSSe cell has activation energy equal to the bandgap, as expected for a very good solar cell. However, the activation energy for CZTSSe falls short of its bandgap value. This behavior can be accounted by the two V_{oc} deficit factors discussed above: (i) non-radiative interface recombination and its consequent Fermi level pinning behavior, and (ii) the effect of tail states that artificially lowers the bandgap of CZTSSe thus lowering activation energy [600].



4001

4002 Fig. 72 Temperature dependence of V_{oc} for IBM-CIGSSe and IBM-CZTSSe solar cells. The intercept of the
4003 (extrapolated line at 0K) V_{oc} versus temperature plot at 0K is the activation energy of the dominant
4004 recombination process. Activation energy is equal to the bandgap for the CIGSSe cell (and other ideal solar
4005 cells) while for CZTSSe activation energy is smaller than its bandgap. This is attributed to dominant non-
4006 radiative interface recombination, Fermi level pinning, and tail states that effectively reduces CZTSSe bandgap
4007 and activation energy.

4008

4009 There are several possible sources of severe interface recombination in CZTSSe solar
4010 cells, such as defective buffer-absorber interface or secondary phases like ZnS(e) [561] at the
4011 interface. Another possible source is a cliff-like band alignment where the conduction band of
4012 the CdS is lower than the absorber layer [612]. However an ultraviolet-photoelectron
4013 spectroscopy study on CZTSSe reveals the opposite, i.e. a spike-like band alignment in
4014 CZTSSe solar cell across all bandgap [613]. Separate study suggests that high bandgap (or
4015 full sulfur) CZTS has a cliff-like band alignment [614]. The discrepancy to earlier study
4016 [613] is suspected due to variation in sample preparation.

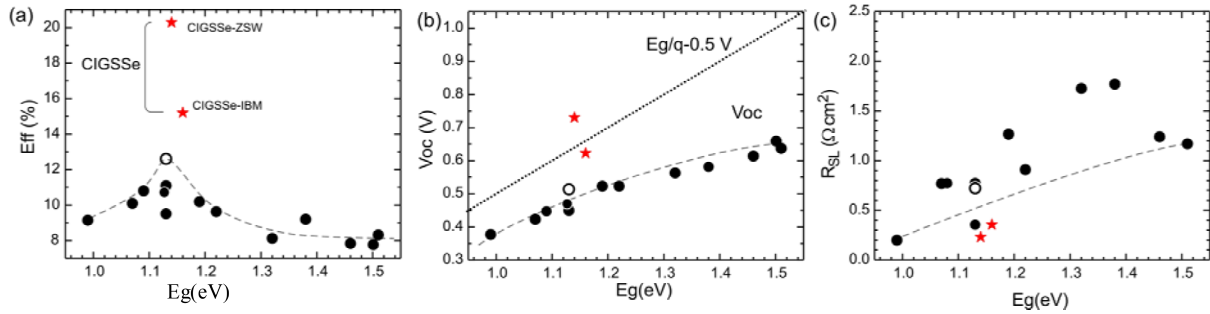
4017 The second major factor that contributes to the V_{oc} deficit in CZTSSe solar cell is the
4018 tail states that arise from electrostatic potential fluctuations induced by high concentration of
4019 native defects and strong compensation [600,615,616]. Temperature dependence study of
4020 time-resolved PL [676] and laser intensity dependence study [616] provide evidence that
4021 supports this potential fluctuation model. A thorough theoretical study by Chen et al.
4022 [617,618] on CZTSSe absorber revealed several major features in the electronics properties
4023 of CZTSSe, such as strong phase competition between the kesterites and secondary
4024 compounds, intrinsic p-type conductivity due to Cu_{Zn} antisite, Cu vacancies and existence of

4025 charge-compensated defect clusters such as [$2Cu_{Zn} + Sn_{Zn}$], [$V_{Cu} + Zn_{Cu}$] and [$Zn_{Sn} + 2Zn_{Cu}$].
4026 These defect clusters contribute to the severe potential fluctuation in CZTSSe.

4027 One evidence of the tail states effect in CZTSSe can be observed from the weak tail of
4028 the QE curve near the bandgap cut-off as shown in Fig. 69(b). Another evidence is found in
4029 the PL characteristics as shown in Fig. 69(b). CZTSSe PL peak occurs at lower energy values
4030 than its bandgap [561,600]. In contrast, the PL peak of CIGSSe is close to its bandgap values
4031 as expected for a high quality material [600]. This suggests that these tail states artificially
4032 lower the CZTSSe bandgap, thus in effect also lowering the V_{oc} [600]. Furthermore lower
4033 dielectric constant (ε_r ~7-8.5) [607,619] in CZTSSe (compared to CIGSSe ε_r ~12) also
4034 causes more severe band tailing effect [600].

4035 The CZTSSe bandgap, which can be controlled by the [S]/[Se] ratio, also plays an
4036 important role in the V_{oc} deficit characteristics. We observe an efficiency versus bandgap
4037 profile that peaks around bandgap of 1.15 eV as shown in Fig. 73(a). We found that V_{oc} does
4038 not increase at the same rate as the bandgap [e.g. see (E_g/q) - 0.5V reference line for
4039 comparison in Fig. 73(b)]. In other words, the V_{oc} deficit gets larger at larger bandgap or at
4040 larger [S]/[Se] ratio. Several factors can account for this behavior such as (i) a constant deep
4041 level defect at 0.8eV from the valence band detected by transient photocapacitance study
4042 [620], (ii) electron trapping [$2Cu_{Zn}+Sn_{Zn}$] defect clusters that becomes more abundant in
4043 CZTS (full sulfur) [617], and (iii) lower dielectric constant at higher bandgap [619] that leads
4044 to more severe tail states [600], (iv) more severe interface recombination at higher bandgap.

4045 An increasing V_{oc} deficit with bandgap is partly responsible to efficiency profile that
4046 peaks around 1.15eV bandgap as shown Fig. 73(a). Another factor that contributes to this
4047 behavior is increasing series resistance with bandgap [Fig. 73(c)] that lower the fill factor at
4048 high bandgap. Note that analogous effect of increasing V_{oc} deficit and similar optimum
4049 bandgap around 1.15eV have also been observed in CIGSSe [621].



4050
4051 Fig. 73 Bandgap dependence characteristics of champion CZTSSe (circles) and CIGSSe cells (stars): (a)
4052 efficiency, (b) V_{oc} and (E_g/q) – 0.5V reference line, and (c) series resistance from light I-V. Empty circles are
4053 data point for the current CZTSSe champion [559]. Dashed curves are guide to the eye. For CZTSSe solar cell,
4054 efficiency peaks around 1.15eV and V_{oc} does not increase at the same rate. V_{oc} deficit becomes higher at higher
4055 bandgap is due to electron trapping defects, lower dielectric constant at higher bandgap, higher interface
4056 recombination at higher bandgap and increasing series resistance with bandgap.
4057

4058 8.4 Future direction

4059 Over the past few years CZTSSe PV technology has experienced rapid growth both in
4060 conversion efficiency and materials understanding. These advances have been achieved by
4061 the collective effort of an expanding research community interested in this challenging and
4062 promising multinary material with yet unachieved efficiency potential. Future breakthroughs
4063 in fabrication strategies are expected to improve phase and electrical uniformity and address
4064 issues related to the main device limitations. The predominant problem is the V_{oc} deficit,
4065 which is mainly attributed to the band tail states due to high concentration of native defects
4066 and strong compensation; and severe non-radiative recombination processes due to bulk
4067 defects and possible interface recombination. Fortuitously these tail states increase the sub-
4068 bandgap absorption that boosts the J_{sc} and leads to surprisingly good J_{sc} characteristics in
4069 CZTSSe solar cells on par with CIGSSe. An understanding and control over interface
4070 recombination and the defects that give rise to the tail states is needed to reduce the V_{oc}
4071 deficit, and improve the performance of CZTSSe solar cells.

4072 Several approaches can be pursued to reduce the V_{oc} deficit such as:

4073 (i) Alternative buffer engineering in attempt to increase the absorber interface quality or to
4074 alter the bulk property. Recently an In_2S_3/CdS double emitter structure has been shown to

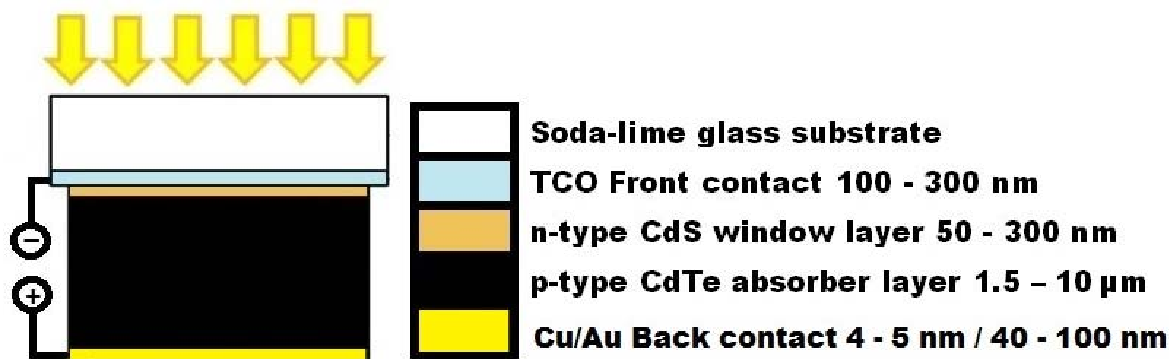
4075 yield a record V_{oc} deficit in lower bandgap CZTSSe [622]. Some of the improvement is
4076 partly attributed to the effectiveness of indium doping to CZTSSe that helps increases the
4077 V_{oc}.

4078 (ii) Focus on low bandgap (selenide) CZTSSe (~1.0 eV) to achieve better V_{oc} deficit.

4079 (iii) Effort to minimize the tail states by using alternative elemental substitutions.

4080 9. Planar thin-film and nanostructured CdTe solar cells

4081 While the first generation (1G, mainly Si based) solar cell manufacturing and
4082 installation costs are relatively low, the development of second generation (2G) thin-films
4083 polycrystalline solar cells still face higher costs compared to efficiency. Given that c-Si
4084 (commercial wafer thickness 180μm) based a-Si:H/c-Si solar cells have demonstrated 25.6%
4085 efficiency [484], while planar 2G CdTe solar cells (CdTe thickness ~2μm) have shown
4086 22.1% efficiency [623,624], there is a scope for extensive research on CdTe based solar cells
4087 to bridge the difference. The schematic diagram of CdTe solar cell is shown in Fig. 74.
4088 Considering that the major barrier for an ultra-large-scale use of solar energy is the high
4089 production cost and low efficiency of the solar cells, one may easily understand the
4090 importance of any investment in strategies to solve these drawbacks. Within this context,
4091 third generation (3G) nanostructured solar cell will play an important role in the future with
4092 the use of new strategies with a competitive efficiency that have been theoretically
4093 understood but experimentally not yet demonstrated.



4094

4095 Fig. 74 Planar (thin-film) CdS/CdTe solar cell. About 1µm thick thin-film CdTe (E_g around 1.5 eV) can absorb
4096 90% of the solar spectrum. In standard process, soda-lime glass or flexible poly(ethylene terephthalate or PET)
4097 commercial substrate is used. Transparent conductive oxides (TCO) such as tin oxide, indium tin oxide, fluorine
4098 doped tin oxide and Al-doped zinc oxide are the most widely used materials for the front contact. Window layer
4099 is deposited over TCO followed by CdTe as absorber layer. Before back contact deposition, cadmium chloride
4100 ($CdCl_2$) treatment is essential to improve electronic properties, texture, grain size and hence cell efficiency.
4101 Also, $CdCl_2$ treatment reduces lattice mismatch between CdS and CdTe; chlorine compensates native defects in
4102 the CdTe structure.

4103
4104 In the above context, CdTe is an essential player in general in materials science, and
4105 in particular in the solar cell market, playing an important role both in planar 2G and
4106 nanostructured 3G solar cell where significant efforts are being currently undertaken both for
4107 enhancing efficiency and reducing costs. In fact, CdTe is an ideal absorber where 1µm thick
4108 2G solar cell can absorb 90% of the solar spectrum with good conversion efficiency [30,625],
4109 considering a bandgap around 1.5 eV depending on the dopant used. Together with this, the
4110 use of simple and low cost manufacturing process makes CdTe based solar cell an
4111 extraordinary candidate in the photovoltaic field, with the production of commercial 2G
4112 modules of 16.1% efficiency and US $0.68/W obtained by First Solar [626,627]. This is still
4113 significantly less than the theoretically expected maximum value of 29% for CdTe solar cells
4114 [626]. Recently, an efficiency of 12% has been reported for nanostructured CdS/CdTe solar
4115 cells [628]

4116 In this section the most important results published in the last years are reviewed for
4117 both 2G and 3G CdTe solar cells. After a brief presentation of the CdTe properties, which

4118 makes this material an ideal candidate for absorber, the review is focused on thin-films 2G,

4119 and nanostructured 3G CdTe solar cells.

4120 9.1 Properties of materials used in CdS/CdTe solar cells

4121 The materials used as front contact are transparent conductive oxides, i.e. materials
4122 that conduct electricity and also allow the light to pass through them. Tin oxide (SnO_2), ITO,
4123 fluorine doped tin oxide (FTO) and ZnO:Al are the most widely used materials. CdS is used
4124 as window layer in this type of cells, while CdTe is used as an absorber. Physical properties
4125 of materials used in CdTe based solar cells, and interface properties of CdS/CdTe solar cells
4126 are presented in Table 5.

4127

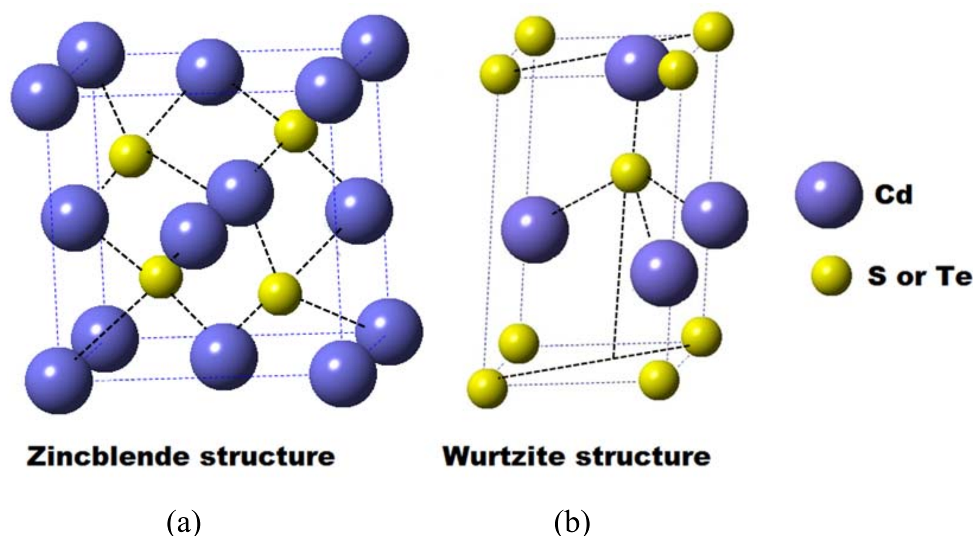
4128 Table 5 Important properties of CdTe based solar cell.

4129

Properties	Value	Ref.
TCO (SnO₂, ITO, FTO and ZnO:Al)		
Lattice constant SnO_2 (Å)	a=4.72; c=3.19	[629]
Lattice constant ITO (Å)	a=1.12	[630]
Lattice constant FTO (Å)	a=4.69; c=3.16	[631]
Lattice constant ZnO:Al (Å)	a=3.24; c=5.16-5.16	[632,633]
Work function SnO_2 (eV)	4.7-5.7	[634]
Work function ITO (eV)	4.7	[635]
Work function FTO (eV)	4.4	[636]
Work function ZnO:Al (eV)	3.83	[637]
TCOs Optical Transmision	>80%	[638]
TCOs Resistivity ρ (Ω·cm)	10^{-4}	[638]
Bandgap energy SnO_2 (eV)	3.9	[629]
Bandgap energy ITO (eV)	3.6	[639]
Bandgap energy FTO (eV)	3.3-3.6	[640,641]
Bandgap energy ZnO:Al (eV)	3.0-3.4	[642]
Window layer (CdS)		
Lattice constant Cubic (Å)	a=5.83	[643]
Lattice constant Hexagonal (Å)	a= 4.14 c = 6.75	[644]
Work function (eV)	4.7	[645]
Bandgap energy (eV)	2.4	[627,639]
Absorber layer (CdTe)		
Lattice constant (Å)	a=6.48	[646]
Work function (eV)	3.88-4.09	[647]
Enthalpy of formation (J/mol)	10^6	[648]
Standard entropy (J/mol.K)	-4.3±0.8	[648]

Carrier concentration/cm^3 (p-type CdTe)	10^{14}	[625, 649,650]
Lifetime electron/holes τ (s) 2μm	10^{-9}	[626]
Bandgap energy (eV)	1.45	[639]
Interface (CdS/CdTe)		
Mistmatch cubic CdTe and hexagonal CdS	9.7%	[651, 652]
Mistmatch cubic CdTe and cubic CdS	-	-
CdTe Absorption co-efficient/cm (at ~600nm)	>10^5	[625, 626,653]
Dielectric constant CdS/CdTe ($\varepsilon/\varepsilon_o$)	10/9.4	[639]
Electron mobility μ_e CdS/CdTe (cm^2/Vs)	350/500-1100	[639, 654]
Hole mobility μ_h CdS/CdTe (cm^2/Vs)	50/60-100	[639,654]
Minority-carrier diffusion length (μm)	<0.8	[625]
Capture cross section electrons σ_e CdS/CdTe (cm^2)	$10^{-17}/10^{-12}$	[639]
Capture cross section holes σ_h CdS/CdTe (cm^2)	$10^{-12}/10^{-15}$	[639]

From crystallographic point of view, the lattice mismatch and crystallographic structure among all components that form the solar cell heterostructure are of essential importance. Figure 75 shows the crystallographic structure of both CdTe and CdS layers in the cubic zincblende (Fig.75a) and hexagonal Wurtzite structure (Fig.75b).



(a) (b)

Fig. 75 Crystallographic structure of (a) zincblende, and (b) hexagonal Wurtzite. In the zincblende structure, tellurium or sulphor atoms occupy the tetrahedral position surrounded by cadmium atoms located in a face-centered cubic structure. While in the Wurtzite structure, tetrahedron is formed when the S atom is in the interior of the hexagonal structure. CRYSTALMAKER program is used to create the structure even though this is a well known structure.

9.2 Thin-film CdS/CdTe solar cells

In general, the transport of the photogenerated minority-carriers in bulk thin film materials and single crystals has the advantage of fast transportation due to low number of

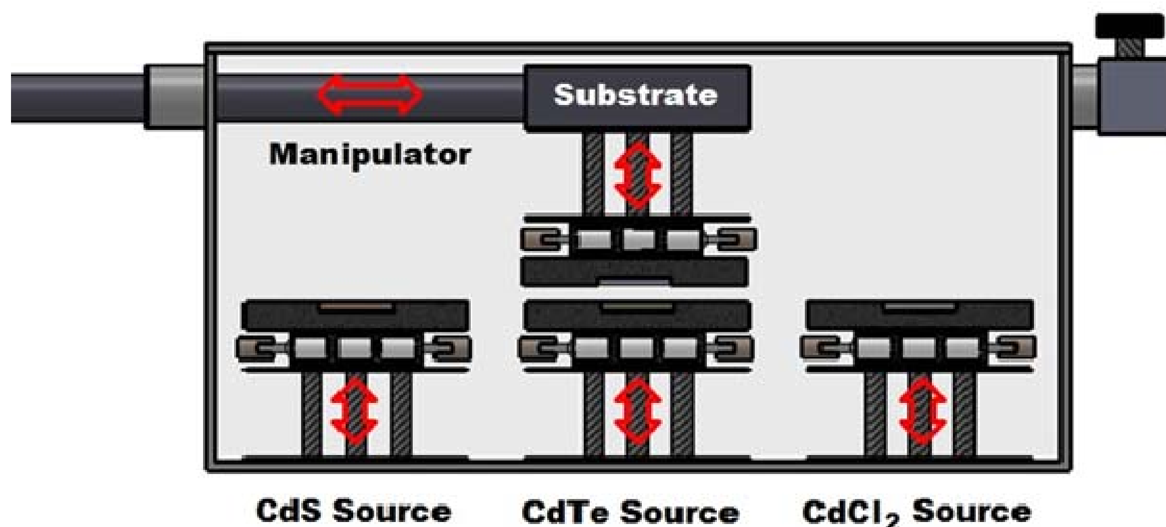
4147 defects. At the same time there is a disadvantage that the production methods require high
4148 energy consumption at high cost and large mass of initial starting materials. The fabrication
4149 of CdS/CdTe solar cell has been mainly carried out using chemical bath deposition (CBD),
4150 sputtering and evaporation, close space sublimation (CSS), and MOCVD [627].

4151 9.2.1 Concepts and preparation methods
4152
4153 P-type CdTe possesses an optimum direct bandgap (1.45eV) and high optical
4154 absorption co-efficient ($5x10^5$/cm) in the visible spectral range. A 0.5 μm thick CdTe is able
4155 to absorb a large percentage (99%) of the solar spectrum [625,652,655]. To form
4156 heterojunction, n-type CdS between 10 and 50 nm layer is required to minimize the photon
4157 absorption losses, without reducing the V_{oc} [652]. Currently work is being carried out in
4158 order to improve the window layer.

4159 For CdS/CdTe solar cells, superstrate configuration is the most commonly used with
4160 the structure illustrated in Fig. 74 [625,656]. Substrate configuration with low-cost flexible
4161 metal substrate is also used [657]. In these configurations, most of the efforts are
4162 concentrated on improving the quality of both window and absorber layers. This is along with
4163 reducing losses through the other components and interfaces due to light absorption in layers
4164 other than the CdTe. Developing a successful solar cell requires a combination of improving
4165 the quality of all components including the electrodes, enhancement of charge transport, and
4166 hence cell efficiency [30].

4167 For the preparation of CdS layer by CBD method, a mixture of KOH, ammonium
4168 nitrate, $CdCl_2$, and thiourea are generally used at a working pH value of 8-9 in the
4169 temperature range of 75-90ºC. A magnetic stirrer in the solution is used to maintain a
4170 homogenous solution and to control the thickness of the CdS film. In order to obtain the
4171 required thickness, the most important parameters in the growth process are pH, temperature,
4172 stirring rate, and time [658, 659].

4173 CSS method is a physical deposition technique where the source and the substrate are
4174 very close to each other, thus allowing the sublimation of the source and creating epitaxial
4175 thin films without using ultra high vacuum. Using this technique both the window and the
4176 absorber layers are prepared [625, 651, 655, 660-662]; the most sophisticated CSS system are
4177 located in the Technical University of Darmstadt (with *in situ* characterization tools for a
4178 complete study of the solar cell) [656, 662], and CTF Solar GmbH [663]. Figure 76 shows
4179 the schematic diagram of a CSS system for the deposition and processing of CdS and CdTe
4180 layers. A general approach for the CSS method [649, 656, 662, 663] uses commercial
4181 halogen lamps for heating the source and substrate. As an alternative to halogen lamp,
4182 resistance heaters (SiC) have been recently proposed as an approach to reduce the duration of
4183 the process and improving the grain size and homogeneity [664]. Several deposition
4184 parameters must be taken into account, such as controlled high-vacuum or inert atmosphere,
4185 source temperature in the range of 500-650ºC, substrate temperature in the range of 300-
4186 500ºC, distance between source and substrate of 2-5mm, and deposition time of 5-20 min. A
4187 fast (1 min) or slow (15 min) cooling process after the CdTe layer preparation in the 300-
4188 500ºC range has been considered as an important step with great influence in the absorber
4189 layer preparation, with fast cooling yielding slightly thicker Cd layer. This thick Cd-layer
4190 could influence the $CdCl_2$ diffusion [649] and affect efficiency.



4191

4192 Fig. 76 Shematic diagram of close space sublimation system for the preparation of CdS and CdTe films [665].
4193 Distance between the source and substrate is 2-5mm and the deposition time is around 5-20min. In order to
4194 reduce the contamination between three sources, a precise shutter is located over each source, and a vacuum
4195 process is done before CdS layer deposition. Source temperature and substrate temperature is in the range of
4196 500-650ºC, and 300-500ºC respectively. The top substrate is located in a moveable piece over fixed sources
4197 with the capability for depositing several consecutive different layers of CdS, and CdTe. At the same time,
4198 cadmium chloride ($CdCl_2$) treatment could be carried out in the same system. After each layer deposition, $CdCl_2$
4199 treatment is required to improve electronic properties.

4200

4201 For CdS/CdTe cell fabrication, there is a general agreement that after the deposition
4202 of each layer (CdS and CdTe), $CdCl_2$ treatment is necessary to improve electronic properties,
4203 recrystallization, grain growth [666] and hence cell efficiency. Prior to $CdCl_2$ treatment,
4204 Major et al. [649] showed the importance of creating (tens of nanometers thick) Cd-rich
4205 surface using nitric-phosphoric acid etching to increase the chlorine and oxygen in-difussion
4206 associated with an improvement in the efficiency from <3% to 12%. The absence of this
4207 etching process will, however, produce a blocking layer of $Cd_3O_2Cl_2$.

4208 For CdS layers, $CdCl_2$ treatment is used because of the resulting benefits of the
4209 window layer causing a recrystallization and increasing the grain size with improvement of
4210 the structural and optoelectronic properties [625,661, 662-665, 667].

4211 For CdTe layers, post treatment with a $CdCl_2$ treatment is generally used as a process
4212 to promote the interdiffusion of CdS/CdTe layer and recrystallization. The result is the
4213 improvement of the texture and grain size, and reduction of porosity, with reduction of the

4214 point defects [625, 657, 662]. However, CdTe surface roughness increases after $CdCl_2$
4215 treatment [666]. At the same time, the introduction of chlorine can compensate native defects
4216 in the CdTe structure [668]. In the end, this post treatment affects the interdiffusion at the
4217 CdTe/CdS interface with the consequence of reducing the negative factor of the large
4218 mistmatch between both materials [651,652,655].

4219 Other important layers to be considered are the front and back contact, where some
4220 novelties have been reported. For the front contact, the ZnO:Al is increasingly used, although
4221 their lower thermal stability has many advantages compared to other (ITO, FTO) front
4222 contact materials [642, 662]. For the back contact, a 4-5nm Cu, followed by a 40-100nm gold
4223 (Au) layer, is the most used. The Au layer is replaced by antimony telluride to avoid the Cu
4224 diffusion towards the interface [650, 662, 663, 669]. In a complementary way, the use of
4225 selective acidic etching for a formation of tellurium or a p^+-layer prior to the contact
4226 formation is an interesting process, which will improve the back contact [647,662].

4227
9.2.2 CdTe solar cell parameters and properties

4228 Table 6 shows CdTe solar cell parameters. It can be seen that the device with
4229 maximum efficiency of 19% has the best V_{oc} and J_{sc} values [670]. Figure 77 shows the
4230 efficiency versus V_{oc} values, where a clear dependence among both values is demonstrated.

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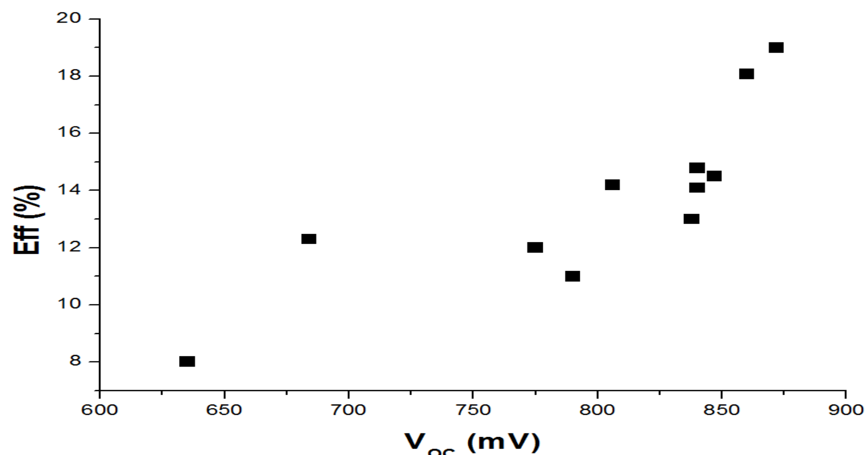


4242 Fig. 77 Relationship between V_{oc} and efficiency. The data corresponds to the values shown in Table 6. As can
4243 be seen, there is a direct relationship between V_{oc} and efficiency. Efficiency >14% has been obtained when V_{oc}
4244 is greater than 750mV. To obtain high V_{oc} and J_{sc}, CdTe thickness of 2-5μm is required.

4245
4246 Table 6 CdS/CdTe solar cell output parameters.
4247

Institution	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill factor (%)	Eff. (%)	Ref.
University of Liverpool	635	20.2	47.1	8	[671]
Darmstadt University of Technology	775	23.9	64.9	12	[662]
University of Chicago	684	25.8	71	12.3	[641]
CTF Solar GmbH	838	21.8	71.1	13	[663]
University of Oregon	790-840	23.0-24.4	62-72	11-14	[668]
University of Toledo	806	25.2	69.8	14.2	[669]
University of Toledo	847	24.4	69.8	14.5	[672]
University of Durham	840	24	73.41	14.8	[649]
Ferdowsi University of Mashhad	860	25.7	81.8	18.1	[639]
First Solar, Inc	872	28	78	19	[670]
First Solar, Inc	875	30.2	79.4	21	[484]

4248
4249
4250 The dependence of V_{oc} and J_{sc} on CdTe layer has been studied extensively [626, 646
4251 654]. For CdTe, absorption in the solar spectrum is ~93% for 1μm thickness, while 99%
4252 absorption requires ~20μm thickness. For 1μm thickness, J_{sc} decreases more than 20% with
4253 strong interdiffusion effects on the CdS/CdTe layer, while it decreases only ~5% for 2-3 μm
4254 [654]. For this reason, in order to obtain an optimum value of V_{oc} and J_{sc}, a critical thickness
4255 of 2-5μm may be required [652, 654, 657, 663].

4256 ## 9.2.3 Defects in CdTe solar cells

4257 Defects such as dislocations, traps, and grain boundaries are important factors that
4258 affect efficiency in planar CdTe solar cells. For this reason, defects have been investigated
4259 experimentally, as well as theoretically in order to study the influence of these on the
4260 optoelectronic properties and consequently on the solar cell efficiency. The quality

improvement for each component, viz. front contact, window layer, absorber layer and back contact is essential to increase cell performance. The following improve device performance:

(i) A good texture of TCO layer will enhance orientation of CdS film.

(ii) Pin hole free CdS window layer is essential to reduce losses that are associated with recombination at interfaces. CdS layer thickness below 80 nm could produce pinholes and increase shunting effects [627,656].

(iii) The presence of grain boundaries affect preferential interdiffusion of sulfur (S) from CdS to CdTe as a consequence of assisted diffusion mechanism leading to the formation of the $CdTe_{1-x}S_x$ phase. Grain boundaries induce dislocations, trap minority carriers, and influence V_{oc} [653] which reduces cell efficiency. At the same time the internal electric field that exists between the grain boundary core and the bulk material will deteriorate the electrical conductivity of the material [653, 673].

(iv) CdTe layer requires a thickness of 3-5μm to avoid pinholes and shunting phenomena.Therefore, a double CdTe layer structure formation has been prepared with two consecutive temperature steps [650].

(v) All interfaces must be carefully controlled. In fact, distorted bonds at the interfaces introduce extra electronic states, hole traps, and accumulation of positive charges [653].

9.2.4 Novelties and improvements

For the development of planar CdS/CdTe solar cells some general novelties have been proposed:

(i) With spin coating process, tens of sequentially controlled thickness layers can be produced [641].

(ii) The use of nanoparticles as source material in CSS method will reduce the time for obtaining a pre-determined thickness of the CdTe layers. As one example, for a given 5μm thickness, a reduced time of 35% is obtained [641].

4288 (iii) In CSS high vacuum process, a double layer structure formation with two consecutive
4289 temperature steps for both window and absorber layer is suggested in Ref. [650].

4290 The new features and improvements that have been introduced recently in the
4291 development of CdS and CdTe layers as well as developments in the characterization
4292 techniques are described below:

4293 (i) An extra oxide layer between the TCO and the window layer to minimize shunting effects
4294 has been introduced. However, it also comes with the disadvantage of increasing production
4295 cost [627]. In fact a ZnO buffer layer before the CdS window layer has been proposed as a
4296 factor for reducing pinholes and voids on the window layer [657].

4297 (ii) CdS window layer prepared with low oxygen content in the order of 2% O_2/Ar gives a
4298 good adhesion layer after $CdCl_2$ treatment, while without O_2 treatment, the interface is
4299 delaminate [674]. At the same time, the O_2 partial pressure will enhance the transmission
4300 below 500nm with slightly increase in efficiency of 1% [674].

4301 (iii) Widening CdS layer bandgap to allow more region of the solar spectrum to reach the
4302 absorber layer with improving photocurrent. For example $Cd_{1-x}Zn_xS$ composition enhances
4303 the blue-region of solar spectrum with increasing Zn concentration being the bandgap energy
4304 values 2.4-3.5 eV for $Cd_{1-x}Zn_xS$ ($0<x<0.9$) [627]; Also, smoother and denser CdS layers have
4305 been proposed as a measure to reduce the light absorption in the high energy UV range [627,
4306 656].

4307 (iv) The doping of p-type CdTe layer has been proposed as a way to modify carrier
4308 recombination and increase the shallow acceptors in p-type CdTe to improve bulk minority-
4309 carrier lifetime [625]. It is also a way to increase the work function with dopants such as
4310 arsenic, although arsenic segregation at the grain boundaries will increase the acceptor
4311 concentration in these regions [647]. Furthermore, a step doping profile of the absorber layer
4312 has been done with a structure of p/p+ with thickness ratio of 2.24/1.26μm as a way to create

4313 an electric field that improves carrier collection [639], resulting in an improvement in V_{oc},
4314 improved fill factor, efficiency, and reduction of the series resistance [639].

4315 (v) Large difference in the valence band offset at the interface will form a barrier for holes,
4316 with an increase in the contact resistance. To obtain negligible valance band offset for
4317 efficiency enhancement, wide bandgap materials such as $Cd_{1-x}Zn_xTe$ (E_g ~1.5-2.4eV), Cd_{1-}
4318 $_xMn_xTe$ (E_g ~1.5-3.2eV) and $Cd_{1-x}Mg_xTe$ (E_g ~1.5-3.6eV) are used with appropriate
4319 composition ratios of Zn, manganese (Mn) and magnesium (Mg), all of them having high
4320 solubility in CdTe [625,626].

4321 (vi) For absorption of low energy photons, an intermediate narrow metallic bandgap material
4322 is used between the n/p type semiconductors [30].

4323 (vii) In the absorber/contact interface, the use of electron reflector barriers such as CdXTe
4324 (X:Mn, Zn, Mg) are useful for reducing back surface recombination, which allows increased
4325 values of 0.2V for V_{oc} and 3% for the efficiency. This is a strategy used for CIGS and Si-
4326 based solar cells, although here the quality of the interface between absorber/electron barrier
4327 must be improved [626]. The other way of increasing efficiency is the use of highly doped
4328 ($10^{18}/cm^3$) buffer layer at the interface between absorber/contact in the substrate
4329 configuration [657].

4330 Apart from classical techniques such as XRD, scanning electron microscope (SEM),
4331 EDX etc. it is of special interest to know new tools that have been successfully used in the
4332 past few years for better understanding the properties of CdTe solar cell. These include
4333 scanning Kelvin probe microscopy for the Fermi level shift determination and CdTe work
4334 function [647], laser beam induced current for photoelectronic properties [653], electron
4335 beam induced current [664] and electron back-scatter diffraction to demonstrate that the grain
4336 structure and the grain boundaries dominate the electrical activity [673], x-ray photoelectron
4337 spectrometer for *in situ* measurements in the CSS chamber [656], thermo photocurrent

4338 measurements to investigate the compensating levels introduced by $CdCl_2$ treatment [668]
4339 etc.

4340 9.3 CdTe nanostructured solar cells

4341
4342 Extensive research has been carried out in the field of 3G solar cells over the past
4343 several years [623,628, 635, 657, 667, 675-684]. The basic structure of these nanostructured
4344 solar cells follows the general configuration of the planar solar cells, where the front and back
4345 contacts, window layers, and absorber layers must be present. In this general configuration of
4346 the solar cell, nanostructures can be incorporated through top-down and bottom-up processes.
4347 Top-down processes such as the lithography, low energy ion sputtering [675], and laser
4348 irradiation [684] can change the solar cell properties, producing an improvement in
4349 luminescence and the crystallinity.

4350 Due to a large number of possibilities, this section will focus on the bottom-up
4351 structures where the nanostructures are created as an intermediate step in the fabrication of
4352 solar cell, and on the superstrate configuration.

4353 Excellent reviews have been published [671, 685] about the new perspectives of the
4354 enhancement of the solar cells efficiencies with the use of 1D nanostructures, nanopatterning
4355 and their applications, in particular dye/quantum dots sensitized solar cells, and single/double
4356 wall carbon nanotubes as strategies for new nanostructured architecture of inorganic and
4357 organic solar cells. This new technology is being used in CdS/CdTe solar cells.

4358 9.3.1 Concepts and advantages

4359 The concept of nanostructure on CdTe solar cell, requires a general configuration of a
4360 superstrate structure (glass/TCO/CdS/CdTe/back contact), with the presence of
4361 nanostructures in some of the layers. These nanostructures play an important role with
4362 promising properties in metals, oxides, semiconductors, etc. having an extraordinary

4363 importance in PV energy production due to the decoupling of light absorption and carrier
4364 separation into orthogonal special directions [676].

4365 The concept and structure of nanostructures embedded in bulk film indicates that the
4366 longitudinal direction is long, allowing for optimal and enhanced light absorption due to more
4367 internal reflections and longer path length compared with thin-films, while the orthogonal
4368 direction is thin allowing for an effective minority-carrier collection [676]. The size and
4369 spacing are in the order of the light wavelength, resulting in positive anti-reflective and light
4370 trapping properties, with a reduction of the reflectance of two orders of magnitude compared
4371 to the equivalent planar structures. This allows for a high performance without a reduction of
4372 the J_{sc} [657, 676].

4373 In the nanostructured solar cell, apart from lower defect trapping, the diffusion length
4374 of minority-carriers in the lateral direction is shorter than that of a thin-film solar cell [686].
4375 Nanojunctions generate an electric field in the lateral direction that gives the option to the
4376 minority-carrier to move between the core and the shell, resulting in relatively short carrier
4377 transit length, and consequently the recombination loss is reduced [657,687]. Broadening of
4378 the optical bandgap with the use of nanostructure could maximize the S-Q efficiency limit
4379 which is an attractive electronic property.

4380

4381 9.3.2 Types of nanostructures and mechanisms of formation

4382 There are different types of nanostructures that follow the general scheme of a core
4383 structure of ZnO or CdS embedded by the shell structure of CdS or CdTe respectively, named
4384 as ZnO/CdS [681, 683] or CdS/CdTe core/shell structure [677, 685], although there are some
4385 exceptions to this rule. As mentioned in Sec. 7.6.1, the nanostructures can be classified
4386 according to their structure as follows: nanowires [677, 681, 683, 685], nanocones [676, 684,
4387 686], nanopillars [685] and whiskers or needles [677].

4388 There are several methods for core formation. The most general processes use Au and
4389 Ni as catalyst for nanowire core formation through the VLS process [16, 657, 677, 680, 687].
4390 Nevertheless, there are other methods used for core formation: porous anodic alumina
4391 substrates embedded in polycrystalline thin-films for p-type CdTe formation [685], patterned
4392 nanoelectrodes defined on the TCO substrate through e-beam lithography with hole size of
4393 0.4-1nm [688], and magnetron sputtering deposition using Ar [678].

4394 For core/shell formation, the core begins from a seed material where nanowire
4395 crystallizes or grows, as it happens with Au catalyst. Other methods are: a µm layer of CdTe
4396 as a seed for the growth of CdTe nanowire in substrate configuration [657]; a nm thick
4397 ZnO:Al buffer layer on ITO substrate and using CVD process to develop nanocones shaped
4398 ZnO [686]; TiO_2 nanoparticles deposited by dip-coating on FTO substrate for the preparation
4399 of ZnO nanowire by chemical solution, followed by the growth of nanotubes of CdS in a
4400 chemical galvanostatic process [679]; another alternative for the ZnO nanowire is the
4401 previous creation of ZnO seed layer, with the added advantage that this layer could avoid
4402 shunting paths [681, 683, 686].

4403 The other alternatives that may be of high interest for CdTe nanostructured solar cell
4404 are: the use of nanoink solution processes containing organic ligands and applied in ambient
4405 conditions as a way for nanolayer formation [623]; the use of graphene monolayer with
4406 conductive polymer interlayers, and a spin coating of zinc layer as a mean for ZnO nanowire
4407 preparation in aqueous solutions at a relatively low-temperature [682].

4408 The growth mechanism of CdTe nanowire solar cell has been rarely studied.
4409 Nevertheless, Ref. [678] demonstrates that the CdTe nanowire formation follows the
4410 Stranski-Krastanov model determined by the free energy of the substrate surface (σ_s),
4411 interface free energy (σ_i) and heteroepitaxial surface free energy (σ_f). In consequence, the
4412 seed crystal is nucleated in the 2D layer when σ_s is larger than the addition of the other two,

4413 and 3D islands are formed when σ_s is smaller than the addition of the other two. The growth
4414 process is controlled by the concentration of the nanowire and depends on the temperature
4415 and the type of substrate used.

4416 Growth process indicates that growth rates up to 1μm could be obtained due to solid
4417 and vapor phase growth mechanism [657]. A preferential orientation of <111> in CdTe film
4418 over the ZnO nanowires, with the appearance of side wall facets has been reported [657,
4419 686]. An interesting sulfidation process has been proposed using the following route: ZnO
4420 nanowire produced through a chemical solution is followed by sulfidation (with
4421 thioacetamine) of the ZnO nanowire for the production of ZnO/ZnS core/shell structure, and
4422 completed by the ion exchange Zn-Cd with the result of ZnO/CdS core/shell nanowire
4423 structure. This is due to the fact that the solubility product of CdS is 10^4 times lower than ZnS
4424 [683]. Also, nanowire heterostructures on III-V Wurtzite/zin-blende cubic compounds [680]
4425 with similar crystallography structures of CdS/CdTe have been studied, and a growth
4426 mechanism is explained through the competition between the Gibbs-Thomson effect and the
4427 different diffusion mechanisms.

4428 The post growth process that follows the nanostructure formation is similar to that of
4429 planar solar cell. To improve efficiency, $CdCl_2$ treatment in one or several steps is essential
4430 for recrystallization controlling the interdiffusion at the CdS/CdTe interfaces and passivation
4431 of the grain boundary interfaces [657, 667, 686, 689].

4432 9.3.3 Characteristics of nanostructures and CdTe nanostructured solar 4433 cells

4434 Table 7 shows the most important characteristics of the nanostructures used in CdTe
4435 solar cells, with indication of the preparation methods and nanowire characteristics such as
4436 diameter, height, density, and spacing between the nanowires. There are different methods
4437 from chemical solution to vapor, which produce nanowire geometries with clear difference

4438 between them. Considering the three nanowires geometric properties of diameter, height and
4439 density, if one considers that the ratio between height and diameter is critical for efficiency, a
4440 general conclusion to draw is that the VLS method is the most adequate for nanowire
4441 formation. In the spacing data, there are differences between the reported values that appear
4442 to be related to preparation method.

4443
4444 Table 7 Characteristics of the CdTe Nanostructures.
4445

Nanowire Structure	Method	Diameter (nm)	Height (μm)	Density ($/cm^2$)	Spacing (nm)	Ref.
ZnO	CBD	140	5		0.3	[681]
ZnO	CVD	80-300	1	10^9	20-200	[686]
ZnO	Dip-coating	80	1	10^{10}	20-40	[679]
CdS	PLD	40-100	0.4-1	$2 \cdot 10^9$		[677]
CdS	Electro-deposition	60	100	$1.14 x 10^{10}$	106	[628]
CdTe	VLS	50-200	10-100	10^7-10^8		[657]
CdTe	Sputtering	100-150	3	~10^9	20-50	[678]
CdTe	Electro-deposition	400-1000	1	~$5x10^9$	2000	[688]

4446
4447
4448 The output characteristics of the CdTe nanostructured solar cells are indicated in
4449 Table 11.8, where the relatively low efficiency can be observed if one compares these data
4450 with planar solar cell, although the improvement has been steadily increasing over the years.
4451 An example of this increment is a new efficiency record for this type of devices of 12% using
4452 CdS nanowires embedded in CdTe [628], with a high value of J_{sc} (26mA/cm^2).

4453
4454 Table 11.8 Output characteristics of nanostructured CdTe solar cells under AM 1.5 conditions
4455

Institution	V_{oc} (mV)	J_{sc} (mA/cm^2)	Fill factor (%)	Eff. (%)	Ref.
Oak Ridge National Laboratory	630	8.3	38	2	[686]
University of Liverpool	520	13.9	34.3	2.49	[657]
Oak Ridge National Laboratory	610	13.8	38	3.10	[686]
University of Kentucky	770	26	60	12	[628]

9.4 Future direction

More work and investment must be done considering the predicted maximum theoretical efficiency of 29%. Here are some research paths that could be followed to improve the efficiency: (i) improvements in front contacts by replacing TCO by graphene, pure and doped, together with buffer layers allowing for Ohmic contacts [682, 690], (ii) well aligned CdTe nanowires with optimum value of the diameter/thickness ratio, (iii) strategic alloys and compounds to increase the bandgap of the buffer layer for improving efficiency, and (iv) adequate buffer layers for lattice mismatch reduction in order to improve the crystallographic quality.

10.0 SiNW solar cells

With the beginning of this millennium it was rapidly realized that nanostructures such as SiNWs offer a flexible platform for novel 3D solar cell concepts [691-693]. Nanowires show several advantages over planar solar cell geometries such as the potential for increased device density, and device development on flexible substrates. Direct bandgaps in smaller diameter SiNWs also offer the potential for increased efficiency. Since Si is well understood in terms of its properties, SiNWs come with a solid platform for extending current fabrication technology in their use as active solar cell materials.

This section will give a short overview about SiNW based solar cells, present the competing concepts and show the most promising candidates for highly efficient and cost-effective solar cells.

The term nanowire is often substituted by related terms like nano-rods, whiskers, pillars, columns or cones. A recent review by Kuang et al. therefore formed the description “elongated nanostructures” to combine all these different terms with a similar meaning [694].

10.1 SiNW formation

4481 SiNWs can be prepared by several different techniques and every method has its own
4482 advantages and drawbacks. The large increase in surface area enables an efficient light
4483 trapping due to multiple scattering events and optical path increase inside the SiNW. In
4484 general, the nanowire synthesis methods are arranged in bottom-up growth and top-down
4485 etching techniques.

4486 In the case of bottom-up synthesis, the VLS growth, which was developed by Wagner
4487 & Ellis in 1964, is the most popular approach of preparation [695]. As mentioned in
4488 Sec.7.6.1, in a VLS process, a metal catalyst which forms a eutectic with Si (Au, Al, Cu and
4489 Ag etc.) is heated in vacuum and is exposed to a gaseous Si source like SiH_4,
4490 tetrachlorosilane ($SiCl_4$), sputtered or laser ablated Si [696-699]. Most research groups used
4491 SiH_4 precursors for SiNW growth since it can produce well controlled wire dimensions and is
4492 relatively easy to handle once the toxicity is kept under control. A VLS process requires a
4493 high or ultrahigh vacuum chamber in which a substrate covered with the catalyst metal, in the
4494 form of particles or a thin-film, is heated above the eutectic temperature. The SiH_4 molecules
4495 are decomposed on the metal surface and the Si is introduced into the metal droplet, forming
4496 the eutectic. By further insertion of Si, the droplet gets oversaturated and excess Si is
4497 displaced to the contact surface of the droplet to the substrate. In this way a wire arises below
4498 the droplet. By controlling the catalyst geometry, chemistry and process parameters, it is
4499 possible to create nanowires with precise lengths, diameter, direction, doping and pitch. The
4500 advantage of high control has to be weighed by the disadvantages of high costs for vacuum
4501 equipment, highly poisonous gases and catalyst metal contamination inside the wires, which
4502 is the major drawback especially for Au catalyzed SiNWs [700].

4503 Nevertheless, there are many groups that successfully created solar cells out of VLS-
4504 grown SiNWs. Hochbaum et al. showed the advantages of using $SiCl_4$ as a precursor [701].
4505 During the decomposition of the precursor molecules HCl vapor is formed which etches and

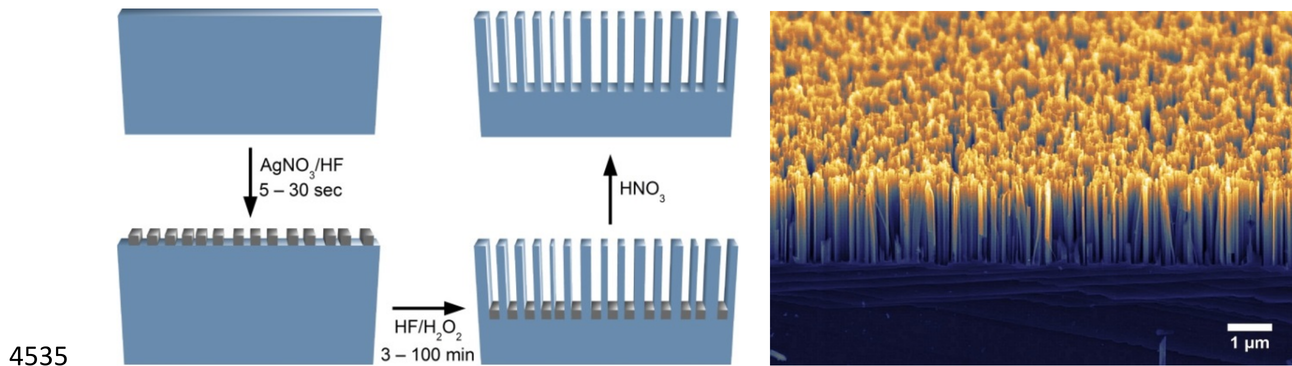
thus cleans both the SiNW sidewalls as well as the substrate surface. In this way it became possible to grow highly ordered epitaxial SiNWs, which was not possible with SiH_4. The electrical modification of SiNWs is achieved by adding doping precursors like B_2H_6 or PH_3 into the chamber during growth which leads to p- or n-type doping [692,702] respectively. In 2006, Wang et al. described the growth of SiNWs by using Al catalyst to avoid the deep-level electronic states that are caused inside the Si when using a gold catalyst [698]. On the other hand Al comes with another drawback: it needs an extremely clean environment at UHV conditions to avoid oxidation of the Al which drives the production costs to a disproportionate level.

Garnett & Yang [532] and Stelzner et al. [703] developed the first solar cell devices based on carpets of SiNWs grown by VLS method. Their efficiencies were quite low, but they established a basis for a complete new field of nanostructured solar cells.

In contrast to the bottom-up growth methods, the top-down synthesis of SiNWs uses existing layer of Si like single- or multicrystalline wafers or deposited layers on supporting substrates to create wires inside these layers. The most prominent processes are the metal-catalyzed electroless etching, which was developed by Peng et al. [693] in 2002, and the RIE [704,705]. Both processes can form randomly distributed or ordered SiNWs.

In a metal-catalyzed electroless etching (MCEE) preparation, a metal catalyzed anisotropic etching of Si forms the desired SiNWs. The most prominent recipe was developed by Peng et al. [693,706]. Ag nanoparticles are deposited on Si in a mixture of HF/silver nitrate and are subsequently used for the anisotropic etching in a HF/H_2O_2 mixture. The Si is catalytically oxidized at the Si/metal interface and immediately etched by the HF. In this way, the metal particles move into the Si layer, forming a carpet of SiNWs. Since the anisotropic etching at room temperature only occurs in the Si<100> direction [707], perpendicular SiNWs are formed on a Si(100) wafer (Fig. 78), while the use of a Si <111> wafer leads to

4531 zig-zag shaped wires [708]. In multicrystalline layers, each grain is independently etched into
4532 the <100> direction [709]. MCEE processes are easily scalable and relatively cheap in
4533 contrast to bottom-up growth which is why it is an attractive way of generating highly
4534 absorbing structures for photovoltaics.

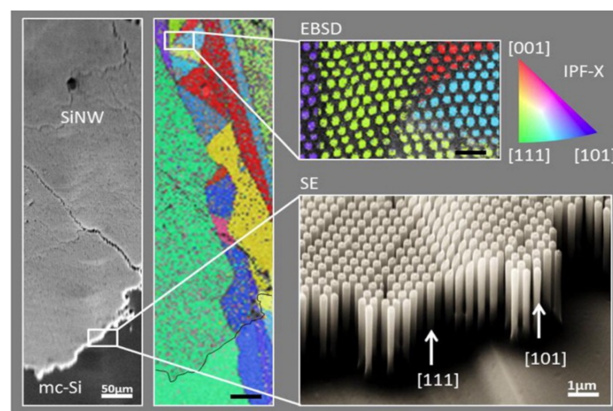
4535 

4536
4537 Fig. 78 Left side: Schematic model of the preparation of wet-chemically etched SiNWs. Ag nanoparticles are
4538 deposited by rinsing a wafer in a silver nitrate/HF mixture. These particles act as catalysts in the subsequent
4539 etching of Si in HF/hydrogen peroxide which is highly dependent on the crystal orientation of the wafer. In the
4540 final step Ag is removed by nitric acid. Right side: A tilted (55°), colored SEM micrograph of an etched
4541 Si<100> wafer with SiNW length of 2µm. Such a structure acts as a nearly perfect light absorber with an
4542 absorption of over 90% in a wavelength range from 400 – 1000nm. SEM image originally published in [710],
4543 Björn Hoffmann, Vladimir Sivakov, Sebastian W. Schmitt, Muhammad Y. Bashouti, Michael Latzel, Jiří
4544 Dluhoš, Jaroslav Jiruse and Silke Christiansen, "Wet–Chemically Etched Silicon Nanowire Solar Cells :
4545 Fabrication and Advanced Characterization in Nanowires"- Recent Advances., InTech; 2012. Edited by Xihong
4546 Peng. pp-211-230. Reproduced here under CC BY 3.0 license. Copyright © 2012 InTech.

4547

4548 In addition to wet-chemical processes there is much effort put into the development of
4549 dry-etching of Si in a deep RIE (DRIE) approach. The process works without metal catalysts
4550 and can be applied either in a self-organized or a mask-supported process. Two particular
4551 approaches will be mentioned here: the formation of so-called black Si and the preparation of
4552 highly regular SiNWs by the use of nanosphere lithography. The term black Si is used for
4553 many variations of etched Si and refers to the dark appearance of such a layer. In the most
4554 popular results, a fluorine-based etching [711-713 827-829] creates random pyramidal or
4555 needle-like structures that can be compared to MCEE results. The advantage is that no
4556 lithography step for catalysts or masks is needed. Halbwax et al. used a femtosecond laser to
4557 form Si nanostructures that also carry the name black Si [714].

4558 By combining a RIE process with a prior decoration with a monolayer of silica
4559 spheres in a Langmuir-Blodgett deposition, Hsu et al. gained a high control over the
4560 dimensions of the resulting nanostructured Si [705]. Since the RIE approach produces SiNWs
4561 with a high dimensional reproducibility, which offers a precise tailoring of optical properties,
4562 it is one of the most promising fabrication mechanisms at the moment. Garnett & Yang have
4563 investigated the light trapping properties of RIE-prepared SiNWs in c-Si wafers and found an
4564 increase in path length of incident light inside the SiNW layer by a factor of 73 [715]. In
4565 2012, Schmitt et al. have shown that such a combination of nanosphere lithography and RIE
4566 also produces regular vertical SiNWs in multicrystalline Si layers on glass and that the SiNW
4567 orientation is not influenced by the original grain orientations [716]. Figure 79 shows SEM
4568 micrographs and electron backscatter diffraction investigations of such prepared SiNWs.
4569 Since this process is more complicated and expensive, it is mostly used for fundamental
4570 research of optical properties or comparisons with theoretical models. Nevertheless,
4571 impressive results have been obtained with RIE prepared SiNWs and the current progress is
4572 very promising.

4573 

4574 Fig.79 SEM and electron backscatter diffraction mappings of multicrystalline thin-film Si that was patterned
4575 with regular SiNWs. This figure shows that the reactive ion etching doesn't interfere with the crystal orientation
4576 of the substrate. All wires are perpendicular to the surface. Furthermore, even wires with a grain boundary
4577 inside them remain in a regular shape. Reprinted with permission from [716], Sebastian W. Schmitt, Florian
4578 Schechtel, Daniel Amkreutz, Muhammad Bashouti , Sanjay K. Srivastava, Björn Hoffmann, Christel Dieker,
4579 Erdmann Spiecker, Bernd Rech, and Silke H. Christiansen, Nanowire Arrays in Multicrystalline Si Thin Films
4580 on Glass: A Promising Material for Research and Applications in Nanotechnology, Nano Lett., 12 (2012) 4050.
4581 Copyright © 2012 American Chemical Society. Permission granted.

4582

4583 ## 10.2 Nanowire solar cell concepts

4584 SiNWs open up new prospects in fundamental research and applications. Lieber and
4585 co-workers created the first reported single nanowire solar cells in axial [717] and radial
4586 [718] geometry and reached efficiencies of 3.4% in the case of radial/coaxial cells and 0.5%
4587 in case of the axial geometry. These fundamental studies showed the potential and limitations
4588 of nanowire-based solar cells and influenced the whole research community since then.

4589 In this review we focus more on realistic applications and industry relevant
4590 realizations of nanowire solar cells. Therefore we will present several different concepts of
4591 radial or axial geometries, bulk or thin-film based SiNWs and random or organized SiNW-
4592 based solar cells. In general, nearly all concepts that are realized in planar geometries, which
4593 were already presented in this article, can be transferred to nanowire-based solar cells.

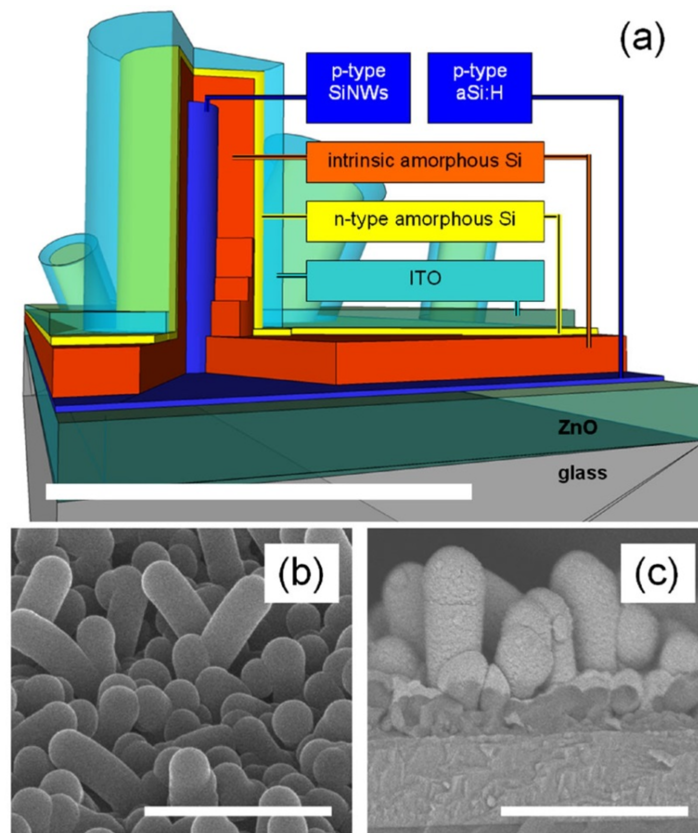
4594 ### 10.2.1 Axial and radial junctions

4595 Nearly all SiNW solar cell concepts with a reasonable efficiency or a promising
4596 geometry are based on radial junctions instead of axial junctions, since one of the major
4597 advantages in a radial concept is the decoupling of absorption path and charge carrier
4598 separation path. Nevertheless, there are several realizations of axial solar cells reported. In
4599 2004 Peng et al. fabricated p-n junctions along SiNW carpets by using MCEE on planar p-n
4600 junction wafers [719]. Even though the realized junctions were not suitable for solar cells,
4601 Sivakov et al. were able to use a similar preparation on multicrystalline Si thin-films on glass
4602 to form axial p^+-n-n^+ junctions which showed a conversion efficiency of 4.4% [709].

4603 A radial junction geometry is more and more preferred for SiNW-based solar cells in
4604 the last years. In 2005, Kayes, Atwater and Lewis published a theoretical modelling of radial
4605 p-n junctions in Si nanorods and the model showed that a large increase in efficiency is
4606 possible compared to planar p-n junctions [720]. The calculations also showed the crucial
4607 points that had to be concerned: low minority-carrier diffusion lengths compared to the

4608 optical thickness and low depletion region recombination. This concept shows the potential
4609 of utilization of lower quality Si materials and cost reduction towards a possible mass
4610 production.

4611 In the early days (2007-2008) of radial SiNW solar cell development mostly VLS
4612 grown SiNWs were used [535,703], but the efficiency only reached very low values of 0.1%.
4613 Nevertheless, these initial studies found the crucial points which have to be optimized, like
4614 the contamination with catalyst atoms or the junction quality. Recently, VLS grown SiNWs
4615 undergo a renaissance, as Cho et al. prepared SiNWs with Sn as a catalyst and reached nearly
4616 5% efficiency [721]. Their concept uses a crystalline p-type Si core with intrinsic and n-type
4617 a-Si:H shells grown on ZnO:Al covered glass, as shown in Fig. 80. One year later in 2013,
4618 the same group improved their cell concept to an excellent efficiency of 8.14% by optimizing
4619 the nanowire density [722].

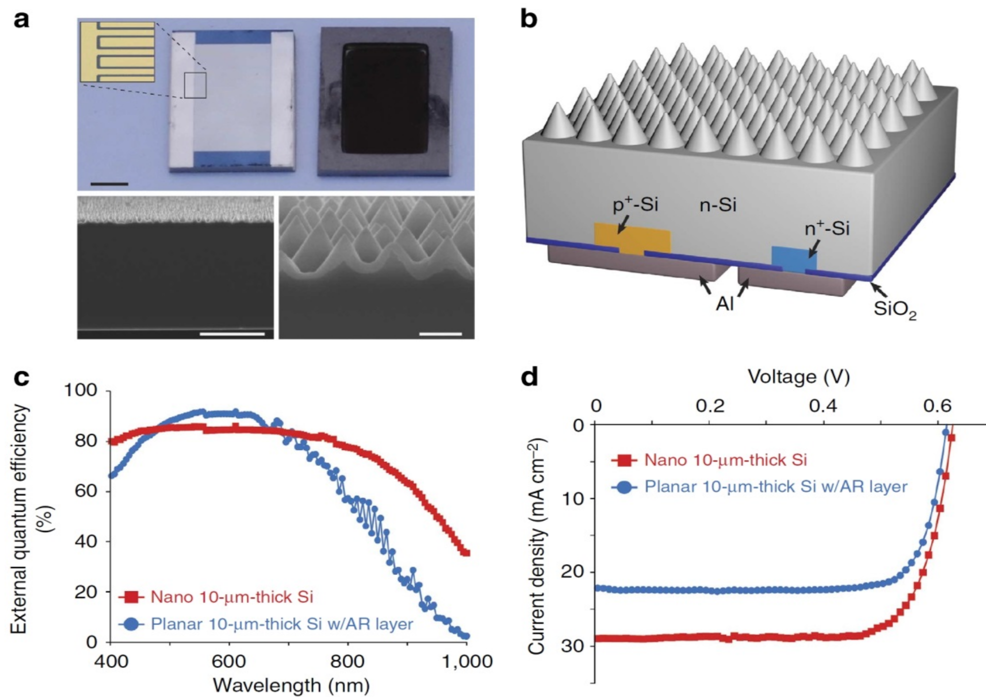


4620

4621 Fig. 80 (a) Schematic of a p-c-Si/i-a-Si:H/n-a-Si:H junction geometry on glass substarte. The SiNWs are grown
4622 on ZnO covered glass and both SiNWs and substrate are subsequently covered by an intrinsic and an n-type a-Si

4623 layer. A conformal coating with ITO forms the contact. (b) tilted, and (c) cross-section SEM micrograph
4624 showing the conformal coating wrapping the CVD grown SiNWs. Reprinted with permission from [721],
4625 Jinyoun Cho, Benedict O'Donnell, Linwei Yu, Ka-Hyun Kim, Irène Ngo and Pere Roca i Cabarrocas, Sn-
4626 catalyzed silicon nanowire solar cells with 4.9% efficiency grown on glass, Prog. Photovolt: Res. Appl., 21
4627 (2013) 77. Copyright © 2012 John Wiley & Sons, Ltd. License number 3493530552428.
4628

4629 In terms of scalability, and thus industry relevance, top-down prepared SiNWs play a
4630 more important role. In 2010, Garnett and Yang presented radial p-n junction SiNW solar
4631 cells that were prepared by assembly of monolayers of silica beads and subsequent DRIE,
4632 followed by boron diffusion, and reached an efficiency of 5.3% [715]. In 2012 Oh et al.
4633 managed to reduce both Auger and surface recombination in MCEE prepared black Si by
4634 using a special chemical treatment to reduce the surface area of the SiNWs by smoothening
4635 the nanoscale roughness of the sidewalls and thus reached an excellent efficiency of 18.2%
4636 [723]. The authors also suggest that efficiencies above 20% can be reached by optimizing the
4637 nanostructure and by improving the passivation of the back while using point contacts.
4638 Another promising concept was published by the group of Yi Cui from Stanford University in
4639 2013 and describes the formation of Si nanocones on top of ultrathin Si layers [724]. The RIE
4640 fabricated nanocones (Fig. 81) have the advantage of strong light scattering and absorption
4641 while the surface area is much smaller in comparison to long wires. Furthermore they used an
4642 all-back-contact scheme to reduce Auger recombination losses and reached an overall
4643 efficiency of 13.7%.
4644



4645

4646 Fig. 81 (a) Photographs of the metallized back side (top, left side) and the nanostructured front side (top, right side) as well as SEM cross section micrographs of the complete thin-film device (bottom, left side) and the Si nanocones (bottom right side). (b) schematic diagram of the device showing the highly doped, all back-contact design. (c) external quantum efficiency of a nanostructured 10µm thin Si solar cell and a planar control device with the same thickness. (d) J-V measurements of nanostructured and planar solar cells, showing that the nanostructuring leads to a massive increase in current density. Reprinted with permission from [724], Sangmoo Jeong, Michael D. McGehee & Yi Cui, All-back-contact ultra-thin Si nanocone solar cells with 13.7% power conversion efficiency, Nature communications, **4** (2013) 2950. Copyright © 2013 Nature Publishing group. License number 3493530933967.

4655

10.2.2 Substrate variations and random versus organized SiNWs

During the development of nanowire based solar cells, mostly c-Si wafers were used as substrate for growth or etching of wires. Over the last years new processes have been developed to grow SiNWs on cheap substrates like glass [709] or metal foils or to etch SiNWs into multicrystalline deposited Si thin-films on cheap substrates [716]. In order to reach cost competitiveness with industrial scale production, SiNWs need to be realized on substrates that are suitable for existing PV equipment.

The distinction between bottom-up growth and top-down etching are the random distribution and organized distribution of SiNWs respectively. The NW axis direction as well as the diameter can either be controlled or remain random. Depending on the process this control can easily be achieved or needs a very complex treatment. NW orientation and

4667 diameter distribution play an important role for the optical properties of the NW carpet, while
4668 the electrical properties are mostly influenced by the diameter.

4669 The diameter of bottom-up VLS grown SiNWs can be narrowed down easily by the
4670 size of the initial metal catalyst particles. The orientation of VLS grown NWs on the other
4671 hand, can only elaborately be controlled by a very clean environment and the usage of
4672 problematic precursors like $SiCl_4$ [701]. On the contrary, mats from randomly oriented
4673 SiNWs can also show superior optical properties and they can even be explained by statistical
4674 models as Brönstrup et al. have shown [725].

4675 Recently, top-down etched SiNWs are showing a higher relevance for nanostructured
4676 solar cells. Both wet-chemical etching as well as reactive ion etching yields highly absorbing
4677 randomly shaped SiNWs without using any pre-structuring or lithography steps. The
4678 advantage of high absorption is counteracted by the poor electrical quality, since a random
4679 etching leads to a large distribution of diameters and severe surface roughness. If the wires
4680 are too thin, they can be fully depleted or absorb only a little amount of light, while too thick
4681 wires could show a decreased charge carrier separation due to long needed diffusion lengths
4682 to the contact. Therefore many groups try to gain control over the SiNW diameter to gain
4683 defined electrical properties, without losing the advantage of high optical absorption.

4684 10.3 Current Status, challenges

4685 There are many challenges when it comes to a possible commercialization of SiNW
4686 solar cells. One of the main problems of SiNW solar cells is the high surface recombination.
4687 Currently, two different approaches try to minimize these effects: The first method is to
4688 minimize the surface area by tuning the geometry of the SiNWs, especially the aspect ratio.
4689 Here, a combination of electro-optical modeling and experimental investigations is
4690 promising. The second approach is the optimization of surface passivation to reduce the
4691 recombination. For high aspect ratio structures the atomic layer deposition is the most

valuable technique that is also compatible with PV industrial mass production. For instance, the passivation with ultrathin Al_2O_3 layers is investigated very intensively in the last years and shows promising results.

10.3.1 Challenges for mass production

On the way to an integration of SiNWs into commercial mass production many challenges have to be overcome. The large-scale synthesis is still a large problem for both bottom-up and top-down processes. The drawbacks of VLS growth are the needed high-temperature reactors, the typically used catalyst material and the general reactor design, which is limited to substrates with sizes of a few cm^2 at the moment. Furthermore, an integration into existing PV production lines is a challenge. On the other hand, RIE is a promising technique that can be scaled to large substrates, but here the masking layer of typically used micro- or nanospheres is the problem. A solution to this obstacle could be nanoimprint lithography which could replace the nanosphere mask and offers the possibility of large-scale and fast patterning.

Even if SiNW solar cells reach high-efficiencies while remaining cheaper than typical Si thin-film solar cells, they have to be integrated into a complete PV line including module formation and packaging. Here, a drop-in replacement of typical wafers without the need of new processes and equipment would be the best solution. However, this is mainly ignored in the research community by now. So far, the competition against planar devices, which are extremely advanced because they have been improved with immense investment over the past several decades, remains tough. A large-scale industrial involvement in the development of SiNW solar cells would boost their competitiveness. However, in times of hard competition in the PV market at the moment, the industry mainly concentrates on the further improvement of their running products instead of investing in novel structures. Therefore, academic research needs to show the superior properties of SiNWs in large-scale solar cells.

4717 ## 10.4 Future outlook on promising concepts

4718 Since the field of SiNW solar cell research is still in the early stages of development,
4719 there exist several competing PV cell architecture concepts. From the viewpoint of
4720 fundamental research, SiNWs are still under intense investigation.

4721 Parallel to the improvement of existing concepts, there is still a large community for
4722 innovative and new ideas, such as hybrid inorganic-organic solar cells [726-728], or
4723 graphene for Schottky junction solar cells [729] or novel contact materials [730].

4724 SiNW solar cells are still a very complex topic with a multitude of subfields. So far, no
4725 concept was able to show its superiority and thus many of them are under investigation
4726 concurrently. Here, many challenges remain for both research and industry.

4727 To gain a more detailed overview about the field, we suggest some of the recent reviews
4728 by Peng & Lee [731], Kuang et al. [694], Garnett et al. [732], and Ramanujam & Verma
4729 [16].

4730 # 11. GaAs and its related NWs for solar cells

4731 III-V compound semiconductors are very promising materials for NW based PV
4732 devices due to their high absorption co-efficient (e.g. 10^6/cm at 0.3 μm for GaAs) and
4733 availability of direct bandgaps within the solar spectrum. Aligned NW arrays are very
4734 promising building blocks for various nanoelectronic devices, such as nanolasers [733,734],
4735 field-effect transistors [735], light-emitting diodes [736, 737] and field emitters [738,739].
4736 Compared to polycrystalline films, vertically oriented NW arrays are particularly
4737 advantageous for PV applications, because the oriented geometry provides direct conduction
4738 paths for photogenerated carriers to transport from the junction to the external electrode,
4739 thereby resulting in high carrier collection efficiency [740, 741]. Moreover, NW arrays have

significantly smaller optical reflectance and enhanced light absorption in comparison to thin-films due to the foresting effect [742,743]. It is important to note that due to the strain accommodation at the NW sidewalls, NWs are less restricted by lattice mismatch, which provides greater freedom for bandgap engineering and the substrate selection [744]. Thus, a much wider range of material bandgaps may be used in multi-junction NW cells to optimize solar cell efficiency without the restriction of lattice matching in comparison to the planar geometry.

11.1 Basics of GaAs NWs growth

As for GaAs based arrays, in most cases, NWs can be formed via the so-called VLS growth mechanism [695] using different epitaxial techniques, such as MOCVD [745-747], magnetron sputtering [748] or MBE [749-756]. The main stages of the NW growth are following: (i) the formation of a liquid droplet on the substrate surface (for instance, Au or another metal), (ii) the deposition of the desired material onto the surface. The droplet on the surface acts as catalyst, the growth of the NWs is dictated by the diameter and the appropriate place of the droplet. The catalyst in the liquid state should not wet the semiconductor surface, which is necessary for formation of three-dimensional seeding droplets and nucleation of NWs. Additionally, a solution of the catalyst and the semiconductor should have a reasonable melting point (lower than typical growth temperatures). Since NWs feature the predominant direction of growth along the [111] axis, the wafers with orientation <111> (for example, Si <111> or GaAs <111>B) are used in order to obtain the crystals oriented perpendicularly to the surface. In most cases, at least for MOCVD, magnetron sputtering or MBE, the growth is conducted via so called diffusion driven mechanism, where the NW length exceeds several times the effective thickness of deposited material. In the majority of cases, the dependence of the length (L) of NW on their radius (R) is power law, $L \sim 1/R$ and $L \sim 1/R^2$ [757,758].

Figure 82 shows the typical SEM image and corresponding L(R) dependency for GaAs. Similar behavior was observed for (Al, Ga)As NWs.

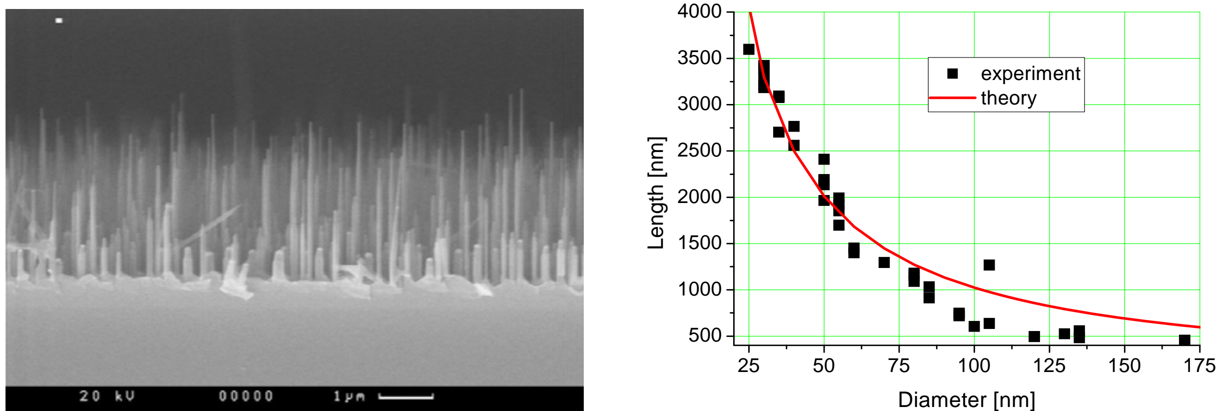


Fig. 82 SEM image and dependence of the length on diameter of GaAs nanowires grown by molecular beam epitaxy (MBE) on GaAs<111>B wafer. The growth temperature was set at 585^{0}C. GaAs layer effective thickness was 500nm. The deposition rate of GaAs was 1.0 monolayer/s. MBE technique is mainly used for GaAs nanowire growth due to precise control over the shape, height, surface density and doping of the nanowires. Nanowire growth is conducted via diffusion driven mechanism, where the nanowire length exceeds several times the effective thickness of deposited material. Data from [757], Diffusion-induced growth of GaAs nanowhiskers during molecular beam epitaxy: Theory and experiment, V. G. Dubrovskii, G. E. Cirlin, I. P. Soshnikov, A. A. Tonkikh, N. V. Sibirev, Yu. B. Samsonenko, and V. M. Ustinov, Phys. Rev. B 71 (2005) 205325. Permission granted. License number 3582351478488.

One of the most important features of MBE growth is the ability to precisely control the shape, height, diameter and surface density of the NWs by an appropriate choice of technological parameters by exploring the diffusion induced growth mode, as well as to monitor the formation and time evolution of NWs *in situ* by the reflection high-energy electron diffraction (RHEED) technique [759]. These peculiarities (i.e. control over growth parameters, doping possibility, growth processes monitoring) allow one to fabricate first PV prototypes based on GaAs NWs [760-762] grown by MBE.

11.2 GaAs NW based PV structures

A coaxial GaAs NWs structure in which a doped NW core is surrounded by a shell of opposite doping type, forming a core-shell p-n junction grown on GaAs<111>B wafer was proposed and successfully realized [760]. Schematic diagram of the MBE grown GaAS nanowire and I-V characteristics are presented in Fig. 83 (a) and (b) respectively.

11.2.1 PV devices based on GaAs NW arrays

It is well known that Si is commonly used n-type doping impurity during conventional MBE. In VLS growth, in contrast, Si incorporation may be amphoteric and both n- and p-type conductivity may appear, depending on Ga or As site substitution [760]. To avoid this, group VI element tellurium was used. In this study, core-shell p-n structures were fabricated by switching from n- to p-type doping during the growth. Tellurium from a GaTe loaded effusion cell was used for n-type doping, and beryllium from an effusion cell was used for p-type doping. PV devices were fabricated in five steps [760]. First, a ~200 nm layer of SiO_x was deposited over the NWs by PECVD. Next, the sample was covered with Shipley S1808 photoresist by spin coating. After the photoresist application, the sample was placed in an oxygen plasma reactive ion etch chamber to remove the photoresist from the tip of the oxide-covered nanowires. Next, using the photoresist as an etch mask, the oxide was removed from the tip of the NWs using buffered HF etch followed by acetone rinse to remove the photoresist. This process isolates the contact to the tips of the NWs and prevents direct contact to the thin-film that grows simultaneously between the NWs. Either opaque contacts or transparent contacts were deposited on top of the NWs for top contact. The procedure was finalized by the contact deposition on the back of the wafer. As a result, several PV prototypes were synthesized with a maximum conversion efficiency of 0.83%. Corresponding I-V data taken in the dark and under illumination is presented in Fig.83 (b).

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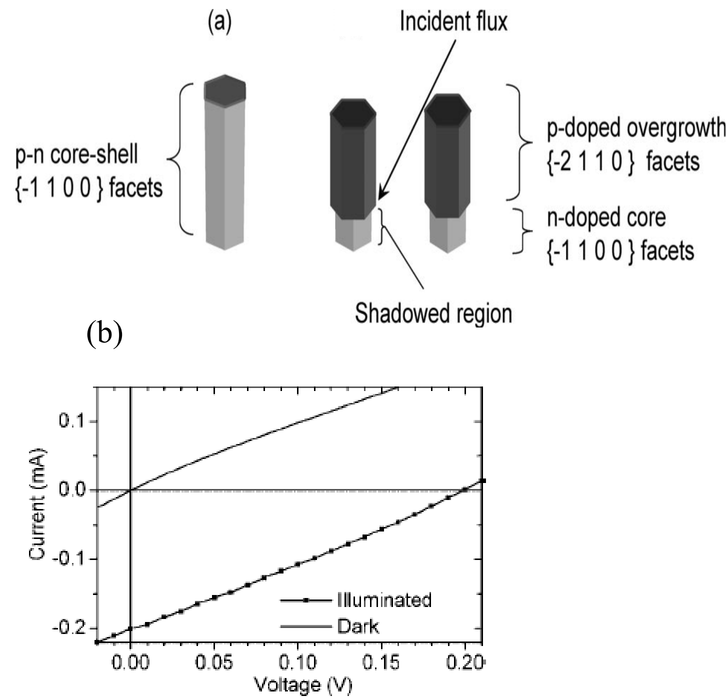


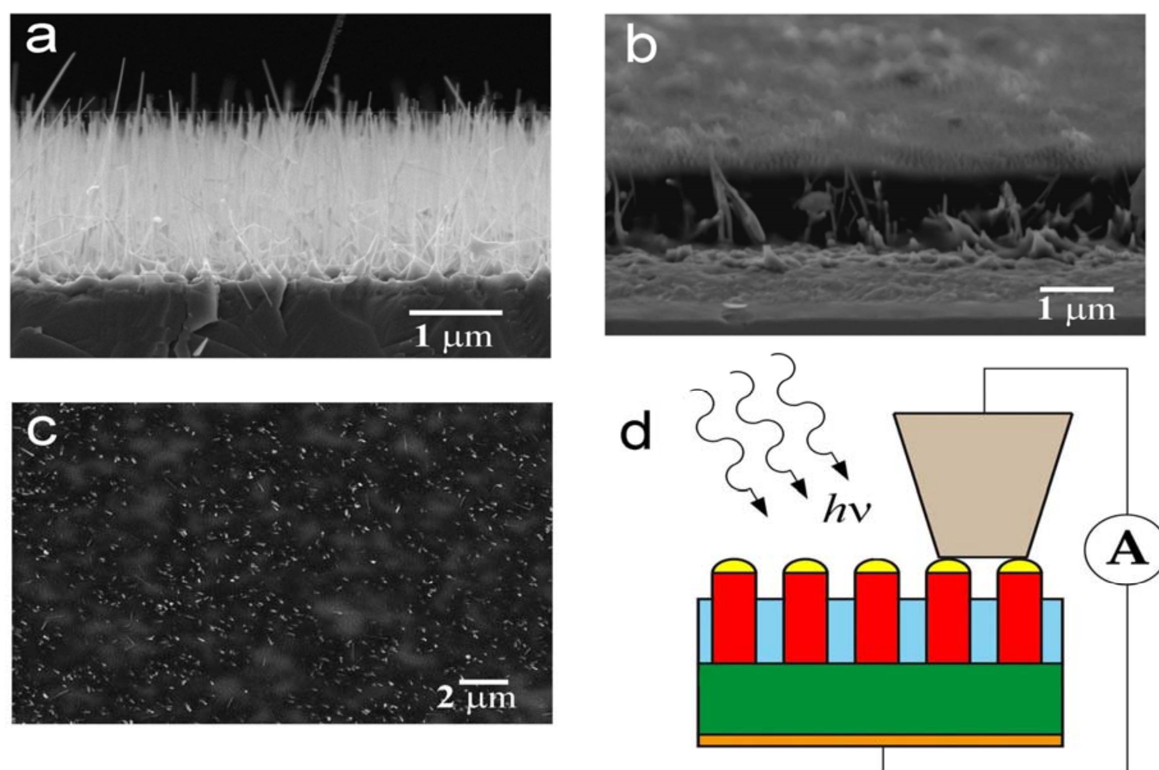
4809

4810 Fig. 83 (a) Schematic diagram of the MBE grown p-n core-shell type GaAs nanowire grown by switching
4811 doping type during the growth, (b) I-V curves of optimized sample in dark and illuminated conditions. The
4812 GaAs nanowire samples are grown by MBE on GaAs<111>B wafer. Si is used as n-type dopant. In VLS
4813 growth, Si incorporation may be n-type or p-type depending upon Ga or As site substitution. Therefore, group
4814 VI element tellurium (Te) from a GaTe loaded effusion cell is used for n-type doping, and beryllium from an
4815 effusion cell is used for p-type doping. A maximum efficiency of 0.83% has been obtained. Figure 83 from
4816 [760], Josef A. Czaban , David A. Thompson and Ray R. LaPierre, GaAs Core−Shell Nanowires for
4817 Photovoltaic Applications, Nano Lett., 9 (2009) 148. Copyright © 2008 American Chemical Society.
4818 Permission granted.

4819

4820 Another PV prototype concept was proposed in Ref. [756]. Here, GaAs p-type NW
4821 arrays are grown on the n-type GaAs<111>B wafer at different wafer temperatures.
4822 Additionally, to prepare the p-n junction, the spaces between the NWs are filled with
4823 insulating photoresist (Poly (methyl methacrylate) or PMMA) via spin coating. In this
4824 particular case, PMMA was used for electrical insulation and contact mechanical support.
4825 After photoresist deposition, the sample surface is treated in oxygen plasma until the tips of
4826 GaAs NWs are exposed. Conventional ohmic contacts for the backside of n-type wafer are
4827 fabricated by electron-beam evaporating of AuGe (30nm) and Ni/Au (10/150nm)
4828 combination having resulting contact resistance ~1x10^{-6}Ohm/cm^2. After each stage, the
4829 samples are studied by applying the SEM technique as shown in Fig.84 (a-c), together with
4830 schematics of the device structure. I-V characteristics are measured using a Keithley 238

4831 source meter (Fig.84d). The samples are placed on a Cu base from backside of the wafer; a
4832 metallic sharp tip (D~0.5mm) is used as top contact to the NWs/PMMA array. The efficiency
4833 is determined by illuminating the structures with one sun illumination. For the given
4834 geometry, the highest conversion efficiency 1.65%, with J_{sc} of 27.4mA/cm^2 and the V_{oc} of
4835 245 mV and fill factor of 25% is achieved when the substrate growth temperature was set at
4836 550°C.



4837

4838 Fig.84. SEM images taken at different stages of device structure preparation, (a) as-grown GaAs NWs array, (b)
4839 after insulating photoresist (PMMA) deposition for electrical isolation and mechanical support, (c) top view of
4840 the resulting structure (after oxygen plasma treatment), and (d) schematic view of the device testing structure.
4841 The MBE growth of beryllium-doped GaAs NWs on n-type GaAs<111>B wafer is carried out at wafer
4842 temperature 550°C with GaAs growth rate at 1 monolayer/s. An efficiency of 1.65% has been obtained due to a
4843 low fill factor of 0.25. From [761], G.E. Cirlin, A.D. Bouravleuv, I.P. Soshnikov, Yu.B. Samsonenko, V.G.
4844 Dubrovskii, E.M. Arakcheeva, E.M. Tanklevskaya, and P. Werner, Photovoltaic Properties of p-type GaAs
4845 Nanowire Arrays Grown on n-Type GaAs(111)B wafer, Nanoscale Res Lett., 5(2010)360. Permission granted.
4846

4847 Different approach was utilized in Ref. [762,763] to combine GaAs and polymer
4848 films. These hybrid solar cells were fabricated by spin-coating poly (3-hexylthiophene)
4849 (P3HT) polymer onto vertically aligned n-type GaAs NW arrays synthesized by MBE [762]
4850 and MOCVD [763]. In both approaches, GaAs<111>B wafer was used. In the last case,

4851 patterned GaAs nanopillars were used as a PV prototype base. According to the scheme
4852 [762], the highest occupied molecular orbital ($HOMO_{P3HT}$) and lowest unoccupied molecular
4853 orbital, ($LUMO_{P3HT}$) for P_3HT is −4.76 eV and −2.74 eV, respectively. The electron affinity
4854 of GaAs is χ_{GaAs}~4.07 eV. Therefore, GaAs NWs are suitable as electron acceptor, and P_3HT
4855 as the electron donor. For this concept, 1.04% and 1.44% conversation efficiencies were
4856 achieved, respectively, showing alternative and less expensive approach to fabricate NWs
4857 based solar cells.

4858 Another way to increase the solar cells efficiency was demonstrated in [764] where p–
4859 n junction GaAs NW solar cell devices of two types consisting of ITO contact dots or opaque
4860 Au finger electrodes, were investigated. Lateral carrier transport from the NWs to the contact
4861 fingers was achieved via a p-type GaAs surface conduction layer. NWs between the opaque
4862 contact fingers had sidewall surfaces exposed for passivation by sulphur. Using this
4863 approach, the relative cell efficiency was increased by 19% upon passivation. Before and
4864 after passivation, efficiency was 1.8% and 2.04% respectively.

4865 It is known that Au-assisted VLS growth can lead to an unintentional Au
4866 contamination [765]. To overcome this disadvantage, it is desirable to utilize the same
4867 material serving the NWs growth catalyst. One of the major steps towards the new PV
4868 prototypes was an introduction of self catalyzed NWs growth where the metal droplet
4869 (catalyst) is a seed particle that is a constituent of the NW itself, e.g. Ga for GaAs NWs
4870 growth [766-771]. A key point is the formation of liquid Ga nanoparticles at the initial stage
4871 in the openings of SiO_x grown on the GaAs<111>B wafer [766], or in a native oxide layer on
4872 the Si<111> wafer [767].

4873 In case of GaAs/Si self catalyzed NWs, the growth procedure is as follows: before
4874 introduction into the growth chamber, the wafers are chemically treated in HF (10% in DI
4875 water) for 1 min, and then rinsed in de-ionized water. Before the growth of NWs, the wafer

4876 temperature is increased to the desired value within the range 560ºC-630ºC, and is kept
4877 constant during the whole growth process. In this temperature window, a native oxide layer
4878 on Si<111> wafer loses continuity, and openings (i.e. the holes penetrating through the oxide
4879 towards the wafer surface) are formed. The surface density of those openings depends on the
4880 temperature. Above 630ºC, the oxide layer is completely desorbed, as detected by the
4881 corresponding transformation of RHEED pattern. After the formation of openings, the Ga
4882 flux is supplied to the surface for several seconds, while the arsenic shutter is closed. This
4883 initiates the formation of Ga droplets in the openings. When the arsenic flux is switched on,
4884 the NW growth is started after an incubation time. The latter is clearly detected by the
4885 transformation of the RHEED pattern and typically amounts to 2-10s, depending on the
4886 temperature. During the NW growth, the RHEED pattern features pronounced 3D spots of
4887 cubic zinc blende phase regardless of the temperature. The spot structure does not change
4888 during the whole growth process excluding the very final stage after the Ga shutter is closed.

4889 The ability to position regularly the group III droplets in the holes patterned in the
4890 oxide film (by using, e.g. e-beam lithography or focused ion beam techniques) is very
4891 attractive to tune the spacing between the NWs, and hence to maximize light absorption.
4892 Additionally, the self-assisted process is compatible with III–V integration on Si platform,
4893 which will lead to lower cost PV devices. Possible device structures based on self-catalyzed
4894 GaAs NWs are presented in the next section.

4895 11.2.2 PV devices based on single GaAs NW

4896 One of the first demonstrations of the self-catalyzed p-i-n radial GaAs NWs applied to
4897 the PV devices was presented in [771], where the fabrication procedure was as follows: GaAs
4898 <111>B wafers coated with a sputtered 10nm thick SiO_2 were used as substrates. The NWs
4899 growth was carried out at a nominal GaAs growth rate of 0.25Å/s, arsenic partial pressure of
4900 $2x10^{-6}$ mbar (Ga rich conditions), a temperature of 630°C. The core of the p-i-n NW junction

4901 was p-type. This was achieved by adding a Si flux during the NWs growth. As it was
4902 mentioned above, Si is an amphoteric impurity in GaAs, and its incorporation can lead to n-
4903 or p-type doping, depending on whether it is incorporated in As or Ga sites, i.e. incorporation
4904 of Si in As (Ga) site results in p-GaAs NW (n-GaAs NW). In the case of Ga-assisted GaAs
4905 NWs growth, incorporation of Si mostly results in a p-type doping [771]. To overcome this
4906 problem, the growth was stopped and the conditions were changed toward planar MBE
4907 growth. Arsenic partial pressure was increased, which resulted in the crystallization of the Ga
4908 droplet. The fabrication of the p-i-n junction continued by the growth of an intrinsic (i) and
4909 an n-type layer on the facets of the nanowires. For this purpose, the temperature was lowered
4910 to 465°C. These conditions had previously been shown to be ideal for growth on {110}
4911 nanofacets [772]. For this growth conditions, due to the lower temperature and higher As_4
4912 beam flux, the incorporation of Si leads to n-type layer [773]. After the growth, the p-i-n
4913 GaAs NW structures were transferred on an oxidized c-Si wafer. The p-type core of the NW
4914 was contacted by first etching a section of the n-type and intrinsic layers of the NW. The
4915 etching was performed with a citric acid solution. Next, a Pd/Ti/Au (70/10/120 nm) layer was
4916 evaporated to form an Ohmic contact with the p-type core. A second lithographic step was
4917 realized with the purpose of contacting the n-type shell. For this, a Ti/Au (10/240 nm) layer
4918 was used. A sketch of the contacted p-i-n nanowire structure is presented in Fig. 85(a). There
4919 the three coaxial layers can be observed, as well as the contacting between the inner and
4920 exterior layers. SEM of a real structure is shown in Fig. 85(b).
4921

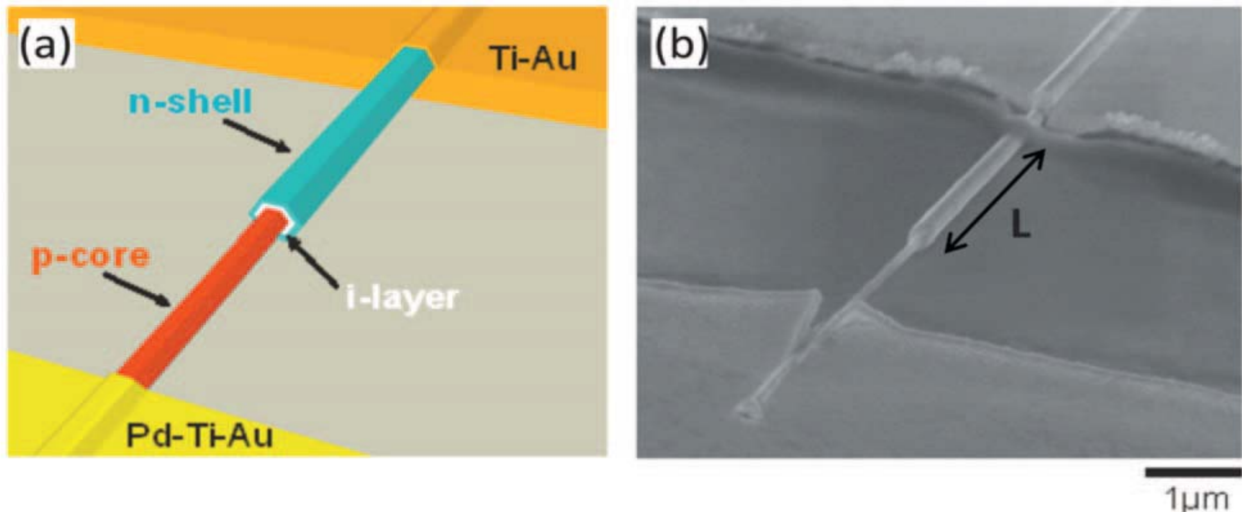
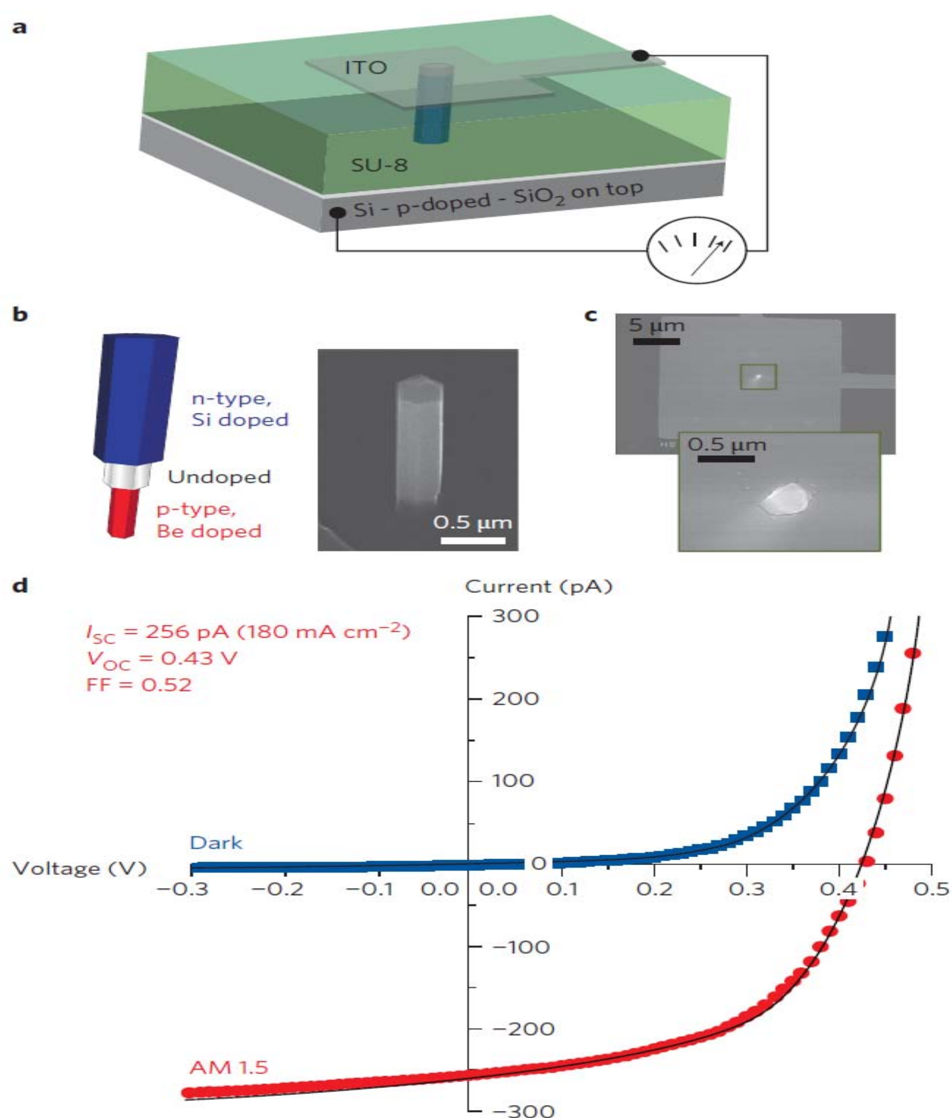


Fig. 85 (a) Sketch of the coaxial p-i-n GaAs nanowire structure showing the contacts to the p-type inner core and n-type outer shell, and (b) SEM of a typical PV device. After fabrication, p-i-n GaAs nanowire structure is transferred on an oxidized c-Si wafer. The p-type core of the NW is contacted by first etching a section of the n-type layer and then intrinsic layer of the NW. Citric acid solution is used as an etchant. For p-type core ohmic contact, evaporated palladium-titanium-gold is used. For n-type shell contact, titanium-gold is used. From [771], C. Colombo, M. Heiβ, M. Grätzel and A. Fontcuberta i Morral, Gallium arsenide p-i-n radial structures for photovoltaic applications, Appl. Phys. Lett. 94(2009)173108. Copyright © 2009 American Institute of Physics. License Number 3486980323906.

To further characterize the p-i-n junction, the light emitted by the NW in forward bias was measured (which corresponds to the regime in which the junction works as a light emitting diode) at room temperature. The emission peak at 1.42 eV is in good agreement with bandgap of GaAs. The existence of electroluminescence at room temperature constitutes a further proof of the quality of the p-i-n junction in the NW, crystallinity and optical quality. The efficiency of the NW device was measured under 1.5 AM illumination conditions. The total efficiency was calculated by dividing the maximum generated power density by the total incident energy density at 1.5 AM. The total area considered was the projected area of the p-i-n junction. For the best sample, a value of 4.5% was obtained with fill factor equal to 0.65.

Very impressive result was obtained recently based on the GaAs single NW solar cells, grown on a c-Si wafer, where the p-type is contacted through a highly doped wafer and the n-type through a transparent top contact [774]. Here, the NWs were grown on oxidized Si<111> with 100nm apertures using a self-catalyzed method. The p-doping of the core was achieved by adding a flux of beryllium during axial growth. The shell was obtained at lower

4946 wafer temperature, the procedure used before in Ref. [771], and the n-type doping was
4947 obtained by adding Si at this growth stage. Next, SU-8 was spun onto the wafer. An oxygen
4948 plasma etching was then performed to expose the NW tip. The top contact was defined by
4949 electron-beam lithography followed by evaporation of ITO, and the bottom contact was
4950 obtained by gluing Ag to the back side of the structure. In Fig. 86 (a-d) a sketch of the device
4951 structure, corresponding microscope images, and I-V characteristics are presented.



4952
4953
4954
4955
4956 Fig. 86. (a) Schematic diagram of the vertical p-i-n type single nanowire device connected to a p-type c-Si wafer
4957 by epitaxial growth, (b) Left side: doping structure of the GaAs nanowire. The p-type core is in contact with the
4958 doped c-Si wafer and the n-type shell is in contact with the ITO. Right side: SEM image of a GaAs nanowire

4959 solar cell before adding the top contact, (c) SEM images of the device seen from the top electrode, (d) I-V
4960 characteristics of the device in the dark and light under AM 1.5G illumination. From [774], Peter Krogstrup,
4961 Henrik Ingerslev Jørgensen, Martin Heiss, Olivier Demichel, Jeppe V. Holm, Martin Aagesen, Jesper Nygard,
4962 Anna Fontcuberta i Morral, Nature Photonics 7(2013)306. Nature publishing group, copyright © 2013
4963 Macmillan Publishers Limited, Permission granted.

4964

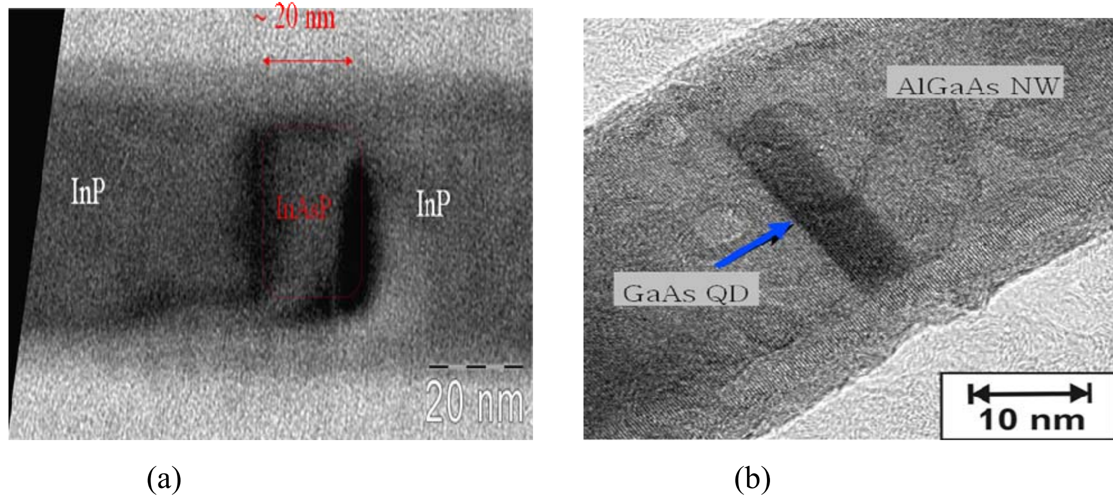
4965 The authors observed a remarkable boost in absorption in single NW solar cells and
4966 explained this observation as due to a vertical configuration of the NW, and by a resonant
4967 increase in the absorption cross-section. For the best case, the PV device exhibits a J_{sc} of
4968 180mA/cm^2 when normalized to the projected area. This leads to an apparent efficiency of
4969 40%, which is beyond the S-Q limit [22], and opens a new route to third generation solar
4970 cells.

4971 11.3 PV devices based on other III-V material NW arrays

4972 As concern to another III-V materials used for the NW based solar cells prototypes,
4973 one should mention InP/Si<111> NWs double-junction structure grown by MOVPE [775],
4974 InGaAs/Si<111> NWs using MOVPE [776], MOCVD grown InGaP/GaAs<111>B NWs
4975 [777], GaAsP/Si<100> MOCVD grown NWs [778], GaAsP/Si<111> NWs using MBE [779]
4976 etc. More detailed information can be found here [780]. But one of the results has to be
4977 outlined separately. The record efficiency for a Au-assisted InP axial p–i–n nanowire array on
4978 an InP<111>B substrate, which was achieved recently an efficiency of 13.8% [781]. This
4979 high value is attributed to the use of the patterned array, more optimal geometry, and lower
4980 SRV in indium phosphide material.

4981 An important aspect, aiming to increase the absorption of the light in the NW based
4982 PV structure, is the use of a combination of several materials inside a NW. Among the
4983 different geometries (e.g. core/shell homo- and heterostructures, or double-junction
4984 structures), a structure consisting of the nanostructures with combined dimensionality,
4985 namely QD inside a nanowire, has additional advantages, such as spreading of the absorption
4986 spectrum and, due to the small sizes, facilitating of the strain relaxation. Recently, a

4987 remarkable progress was achieved in this field. In Fig. 87 (a) and (b), typical transmission
4988 electron microscopy for the InAsP/InP/InAsP [782] and AlGaAs/GaAs/AlGaAs [783] QD
4989 inside a NW combined structures are presented. These nano insertions have typically ~5-20
4990 nm size and exhibit zero-dimensional behavior. Moreover, these structures are optically
4991 bright up to the room temperature, demonstrating outstanding potential for PV applications.

4992 

4993 (a) (b)

4994 Fig.87 Transmission electron microscope images for the quantum dot inside a nanowire structure: (a)
4995 InAsP/InP/InAsP [from 782], and (b) AlGaAs/GaAs/AlGaAs [from 783]. The details of the grown structures are
4996 presented in the corresponding references. Figure 87 (a) from [782], Maria Tchernycheva, George E. Cirlin,
4997 Gilles Patriarche, Laurent Travers, Valery Zwiller, Umberto Perinetti, and Jean-Christophe Harmand, Growth
4998 and Characterization of InP Nanowires with InAsP Insertions, Nano Lett., 7(2007)1500. Copyright © 2007
4999 American Chemical Society. Permission granted. Figure 87 (b) from [783], V. N. Kats, V. P. Kochereshko, A.
5000 V. Platonov, T. V. Chizhova, G. E. Cirlin, A.D. Bouravleuv, Yu B Samsonenko, I. P. Soshnikov, E. V.
5001 Ubyivovk J. Bleuse, H. Mariette, Optical Study of GaAs quantum dots embedded into AlGaAs nanowires,
5002 Semicond. Sci. Technol., 7 (2012) 015009. Copyright ©2012 IOP Publishing Ltd. Permission granted.

5003

5004 11.4 Future outlook

5005 There is a strong interest in the fabrication of novel PV devices based on III-V
5006 material NWs, in particular, GaAs NWs. These structures may provide a lower cost, higher
5007 efficiency devices in PV market. Additionally, different materials combination within a
5008 single, defect-free NW, may lead to higher absorption efficiency. Nevertheless, further
5009 investigations are required to make NWs based PV large-scale solar cell commercial devices.
5010 For better understanding of the processes involved in PV conversion, intensive numerical
5011 simulation and theoretical approaches with an emphasis on optimizing the NW design has

5012 been performed [784, 785]. Important factors, such as surface charge density, SRV, doping
5013 concentration, and NW geometry were investigated in detail.

5014 The particular interests in this area are: (i) the variation in V_{oc} with NW diameter and
5015 change in J_{sc} with tip length indicates the importance of a monodisperse distribution in NW
5016 dimensions, (ii) the minimum NW diameter should be greater than the bulk and surface
5017 depletion widths, which are determined by the doping concentrations [784] and (iii)
5018 importance of a core-shell geometry of NW solar cells [785]. Based on the analysis of
5019 numerous experimental and theoretical data in this area, the following attributes should be
5020 considered for the use of these NWs for PV applications [780]:

5021 (i) Controlled NW morphology
5022 (ii) Stacking-fault-free crystalline structure
5023 (iii) Orthogonal NWs with optimum diameter, and length to maximize optical absorption
5024 (iv) Patterned arrays using cost-effective processes (perhaps nanoimprint lithography)
5025 (v) Dimensions below the critical thickness or critical diameter to avoid misfit dislocations,
5026 which is very important, in particular, when III-V material NWs are grown on c-Si wafers
5027 [786]
5028 (vi) Removal of catalyst droplets to avoid reflection loss and/or Schottky barrier contacts at
5029 the tip of NWs, and possible elimination of Au as a catalyst due to deep level defects
5030 (vii) Controlled doping for p–i–n junctions
5031 (viii) Surface passivation

5032 12. Conclusions

5033 We have reviewed the development and current state of inorganic materials based PV,
5034 with a focus on planar devices and recent developments involving a range of nano-materials.
5035 c-Si based traditional solar cells have dominated the solar cell market for decades, and are
5036 expected to continue playing a dominant role, in particular with recent developments towards
5037 low-cost fabrication. At the same time, other technologies have emerged to address the
5038 limitations and progress the state-of-the-art. For example, a method to overcome optical

5039 shadowing losses completely is to use a back junction design. These cells have shown
5040 efficiencies as high as 24.2%. An important concept is a c-Si based BHJ solar cell. Very
5041 high-efficiency of 25.6% has been reported [246] for BHJ solar cells, and recent simulation
5042 study shows an efficiency of >26%.

5043 Another area of intensive focus is the integration of III-V or metal halide perovskite
5044 based materials on c-Si. This may provide a cost breakthrough for PV technology, unifying
5045 the low-cost of c-Si and the efficiency potential of III-V/c-Si or perovskite/Si multi-junction
5046 solar cells. However, despite the promising potential of these structures, the integration of III-
5047 V on c-Si has been challenging due to mismatches in lattice constants and thermal parameters
5048 of III-V compounds and c-Si, whereas for perovskite/Si cells, the stability of the perovskite
5049 top cell currently appears to be the greatest challenge.

5050 An important challenge for the larger PV community has been to cross the S-Q limit
5051 of solar cell efficiency (29% in case of c-Si). One possible way to achieve this, besides the
5052 use of multi-junction devices based on well-establised single-junction cells as mentioned
5053 above, is to use quantum dots. This may include the use of a quantum dot Si absorber layer,
5054 where charge-carriers are collected before they are able to thermalize (hot carrier effect).
5055 Another potential method is to develop solar cells using nano-crystalline Si solar cells. The
5056 use of up-conversion and plasmonics has also garnered immense interest. However, much
5057 further research work needs to be done here to approach the theoretically predicted potential.

5058 Among non-Si based inorganic solar cells, one technology that has been adopted by
5059 the industry has been CIGS solar cells. At the same time, CZTSSe PV technology has
5060 experienced rapid growth both in conversion efficiency and materials understanding, and
5061 future breakthroughs in fabrication methodologies are expected to make this technology a
5062 serious commercial contender. At the same time, the work carried out over the last few years

5063 in perovskite and CdTe solar cells has been significant for both planar and nanostructured
5064 solar cells.

5065 In terms of very nascent technologies, the field of SiNW solar cell research is still in
5066 the early stages of development, and there exist several competing PV cell architecture
5067 concepts. SiNWs are still under intense investigation, and many challenges remain for both
5068 research and industry. Similarly there is a strong interest in the fabrication of novel PV
5069 devices based on III-V material NWs, in particular, GaAs NWs. These structures may
5070 provide lower cost, higher efficiency devices for the PV market. Additionally, different
5071 materials combinations within a single, defect-free NW, may lead to higher absorption
5072 efficiency. Nevertheless, further investigations are required to make NWs based PV large-
5073 scale solar cell commercial devices.

5074

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REFERENCES

[1] http://www.bbc.com/specialfeatures/horizonsbusiness/wp-content/uploads/2013/04/Energy1.pdf

[2] http://cleantechnica.com/2015/02/17/japanese-domestic-solar-shipments-increase-10/

[3] http://www.ren21.net/wp-content/uploads/2015/07/GSR2015_KeyFindings_lowres.pdf

[4] http://solarcellcentral.com/cost_page.html

[5] Michael Grätzel, Solar Energy Conversion by Dye-Sensitized Photovoltaic Cells, Inorg. Chem., 44 (20), pp 6841–6851

[6] http://ec.europa.eu/research/energy/euratom/fusion/at-a-glance/index_en.htm

[7] http://www.boston.com/news/science/articles/2005/09/05/

[8] http://www.sustainablevillage.com/node/83

[9] Ramchandra Pode and Boucar Diouf, Solar Lighting, p.15, Springer-Verlag London Limited.
2011.

[10] Vytautas Adomavičius, Mantas Kaminickas, Analysis of PV power future development possibilities, Energetika. 2014. T. 60. Nr. 4. P. 233–248.

[11] Gajendra Singh, Amit Verma, R. Jeyakumar, Fabrication of c-Si solar cells using boric acid as spin-on dopant for back surface field, R. Soc. Chem. Adv. 4 (2014) 4225-4229.

[12] Akash Yadav, Gajendra Singh, Reza Nekovei, R. Jeyakumar, c-Si solar cells formed from spin-on phosphoric acid and boric acid, Renewable Energy, 80 (2015) 80-84

[13] R. Jeyakumar, T. K. Maiti, Amit Verma, Influence of emitter bandgap on interdigitated point contact back heterojunction (a-Si:H/c-Si) solar cell performance, Solar Energy Materials and Solar Cells, 109 (2013) 199-203.

[14] R. Jeyakumar, T. K. Maiti, Amit Verma, Two-dimensional simulation studies on high-efficiency point contact back heterojunction (a-Si:H/c-Si) solar cells, Solar Energy, 105 (2014) 109-115.

[15] Jeyakumar Ramanujam and Amit Verma, Photovoltaic properties of a-Si:H films grown by plasma enhanced chemical vapor deposition: A Review, Materials Express, 2 (2012) 177-196.

[16] Jeyakumar Ramanujam, Daryoush Shiri and Amit Verma Silicon nanowire growth and properties: A Review, Materials Express, **1** (2011) 105-126.

5151 [17] Becquerel AE. Recherches sur les effets de la radiation chimique de la lumiere solaire
5152 au moyen des courants electriques. Comptes Rendus de L'Academie des Sciences
5153 1839;9:145-9.

5154 [18] Adams WG, Day RE. The action of Light on Selenium. Proceeding of the Royal
5155 Society of London 1877;167:313-49.

5156 [19] Shockley W. The Theory of p-n Junctions in Semiconductors and p-n Junction
5157 Transistors. Bell Syst Tech J 1949;28:435-89.

5158 [20] Bardeen J, Brattain H. The Transistor, A Semi-Conductor Triode. Phys Rev
5159 1948;74:230–1.

5160 [21] Chapin, DM, Fuller, CS, Pearson, GL. A new silicon p-n junction photocell for
5161 converting solar radiation into electrical power. J Appl Phys 1954;25:676-7.

5162 [22] Shockley W, Queisser HJ. Detailed Balance Limit of Efficiency of p-n Junction Solar
5163 Cells. J Appl Phys 1961;32:510–9.

5164 [23] Byrne J, Kurdgelashvili L. The Role of Policy in PV Industry Growth: Past, Present
5165 and Future. In: In: Luque A, Hegedus S, editors. Handbook of Photovoltaic Science
5166 and Engineering, West Sussex: John Wiley & Sons; 2011 (2nd edition), p. 39-81.

5167 [24] Green MA, Blakers AW, Wenham SR, Narayanan S, Willison MR, Taouk M et al.
5168 Improvements in Silicon Solar Cell Efficiency. Proceeding. 18th IEEE Photovoltaic
5169 Specialists Conference. IEEE, Las Vegas 1985;39–42.

5170 [25] https://www.ise.fraunhofer.de/de/downloads/pdf-files/aktuelles/photovoltaics-report-in-
5171 englischer-sprache.pdf (accessed January 2016)

5172 [26] http://www.idtechex.com/research/articles/global-photovoltaic-shipments-jump-15-in-
5173 2014-00007454.asp

5174 [27] Glunz SW, Preu R, Biro D. Crystalline Silicon Solar Cells. In: Ali Sayigh Editor-in-
5175 Chief. Comprehensive Renewable Energy, Germany: Elsevier. 2012; 353-87.

5176 [28] Schumann M, Orellana Peres T, Riepe S. The solar cell wafering process, Photovolt
5177 Int 2009;5:53-9.

5178 [29] Swanson RM. Approaching the 29% limit efficiency of silicon solar cells.
5179 Photovoltaic Specialists Conference, 2005. Conference Record of the Thirty-first
5180 IEEE, 2005, p. 889–94.

5181 [30] Asim N, Sopian K, Ahmadi S, Saeedfar K, Alghoul MA, Saadatian O, et al. A review
5182 on the role of materials science in solar cells. Renew Sustain Energy Rev
5183 2012;16:5834–47.

5184 [31] Green MA. The Path to 25 % Silicon Solar Cell Efficiency: History of Silicon Cell
5185 Evolution. Prog Photovolt: Res Appl 2009;17:183–9.

5186 [32] Mandelkorn J, McAfee C, Kesperis J, Schwart L, Pharo W. Fabrication and
5187 characteristics of phosphorus-diffused silicon solar cells. J Electrochem Soc
5188 1962;109:313-8.

5189 [33] Blakers AW, Green MA. 20% efficiency silicon solar cells. Appl Phys Lett
5190 1986;48:215-7.

5191 [34] Green MA, Emery K, Hishikawa Y, Warta W, Dunlop ED. Solar cell efficiency tables
5192 (version 43). Prog Photovolt: Res Appl 2014;22:1–9.

5193 [35] Sung Yean Yoon, Jeong Kim, and Kyoon Choi, Effects of Phosphorus Diffusion on
5194 Gettering of Metal Impurities in UMG Silicon Wafers, International Journal of
5195 Photoenergy, Volume 2013 (2013), Article ID 313904, 7 pages,
5196 http://dx.doi.org/10.1155/2013/313904

5197 [36] Goetzberger A, Knobloch J, Voss B. Crystalline Silicon Solar Cells. First edition.
5198 New York: Wiley, 1998.

5199 [37] Fig. 2.3 Courtesy to McMaster University, Hamilton, ON, Canada.

5200 [38] Pizzini S. Towards solar grade silicon: Challenges and benefits for low cost
5201 photovoltaics. Solar Energy Mater Solar Cells 2010;94:1528–33.

5202 [39] Lee SH. Development of high-efficiency silicon solar cells for commercialization, J
5203 Korean Phys Soc 2001;39:369-73.

5204 [40] Wild-Scholten MJ. Energy payback time and carbon footprint of commercial
5205 photovoltaic systems, Solar Energy Mater Solar Cells 2013;119:296-305.

5206 [41] Kern W. The Evolution of Silicon Wafer Cleaning Technology. J Electrochem Soc
5207 1990;137:1887-92.

5208 [42] Neuhaus DH, Munzer A. Industrial Silicon Wafer Solar Cells. Adv Optoelectron,
5209 2007;2007:1-15.

5210 [43] Montesdeoca-Santana A, Jiménez-Rodríguez E, González-Díaz B, Borchert D,
5211 Guerrero-Lemus R. Ultra-low concentration Na_2CO_3/$NaHCO_3$ solution for
5212 texturization of crystalline silicon solar cells. Prog Photovolt: Res Appl 2012;20:191–
5213 6.

5214 [44] Nakaya H, Nishida M, Takeda Y, Moriuchi S, Tonegawa T, Machida T et al.
5215 Polycrystalline silicon solar cells with V-grooved surface. Solar Energy Mater Solar
5216 Cells 1994;34:219-25.

5217 [45] González-Díaz B, Guerrero-Lemus R, Haro-González P, Borchert D, Hernández-
5218 Rodríguez C. Down-conversion properties of luminescent silicon nanostructures
5219 formed and passivated in HNO_3-based solutions. Thin Sol Films 2006;511-2:473–7.

5220 [46] Tsujino K, Matsumura M, Nishimoto Y. Texturization of multicrystalline silicon
5221 wafers for solar cells by chemical treatment using metallic catalyst. Solar Energy
5222 Mater Solar Cells 2006;90:100–10.

5223 [47] Xiao SQ, Xu S. Plasma-aided fabrication in Si-based photovoltaic applications: an
5224 overview. J Phys D: Appl Phys 2011;44:174033 1-12.

5225 [48] Abbott M, Cotter J. Optical and Electrical Properties of Laser Texturing for High-
5226 efficiency Solar Cells. Prog Photovolt: Res Appl 2006;14:225–35.

5227 [49] Cheng Y-T, Ho J-J, Tsai S-Y, Ye Z-Z, Lee W, Hwang D-S, et al. Efficiency improved
5228 by acid texturization for multi-crystalline silicon solar cells. Solar Energy
5229 2011;85:87–94.

5230 [50] Montesdeoca-Santana, González-Díaz B, Jiménez-Rodríguez E, Ziegler J, Velázquez
5231 JJ, Hohage S, et al. Influence of stain etching on low minority carrier lifetime areas of
5232 multicrystalline silicon for solar cells. Mater Sci Engineer B 2011;176:1541–5.

5233 [51] Ali K, Khan SA, Jafri MZM. Low cost anisotropic etching of monocrystalline Si
5234 (100): Optimization using response surface methodology. Superlatt Microstruct
5235 2012;52:782–92.

5236 [52] Marrero N, González-Díaz B, Guerrero-Lemus R, Borchert D, Hernández-Rodríguez
5237 C. Optimization of sodium carbonate texturization on large-area crystalline silicon
5238 solar cells. Solar Energy Mater Solar Cells 2007;91:1943–7.

5239 [53] Chaoui R, Lachab M, Chiheub F, Seddiki N. Texturisation of monocrystalline silicon
5240 with potassium carbonate solutions. 14th European Photovoltaic Solar Energy
5241 Conference 1997;812-4.

5242 [54] Xi Z, Yang D, Que D. Texturization of monocrystalline silicon with tribasic sodium
5243 phosphate. Solar Energy Mater Solar Cells 2003;77:255–63.

5244 [55] Kim K, Dhungel SK, Jung S, Mangalaraj D, Yi J. Texturing of large area multi-
5245 crystalline silicon wafers through different chemical approaches for solar cell
5246 fabrication. Solar Energy Mater Solar Cells 2008;92:960–8.

5247 [56] Montesdeoca-Santana A, Jiménez-Rodríguez E, González-Díaz B, Díaz-Herrera B,
5248 Rinio M, Borchert D et al. Phosphorous gettering in acidic textured multicrystalline
5249 solar cells. Phys Statu Solidi C 2011;8:743–6.

5250 [57] Ju M, Gunasekaran M, Kim K, Han K, Moon I, Lee K, et al. A new vapor texturing
5251 method for multicrystalline silicon solar cell applications. Mater Sci and Engineer B
5252 2008;153:66–9.

5253 [58] Gangopadhyay U, Dhungel SK, Basu PK, Dutta SK, Saha H, Yi J. Comparative study
5254 of different approaches of multicrystalline silicon texturing for solar cell fabrication.
5255 Solar Energy Mater Solar Cells 2007;91:285–9.

5256 [59] Kim K-R, Kim T-H, Park H-A, Kim S-Y, Cho S-H, Yi J et al. UV laser direct
5257 texturing for high efficiency multicrystalline silicon solar cell. Appl Surf Sci
5258 2013;264:404–9.

5259 [60] Yuan H-C, Yost VE, Page MR, Stradins P, Meier DL, Branz HM. Efficient black
5260 silicon solar cell with a density-graded nanoporous surface: Optical properties,
5261 performance limitations, and design rules. Appl Phys Lett 2009;95:123501.

5262 [61] Torres R, Vervisch V, Halbwax M, Sarnet T, Delaporte P, Sentis M. Femtosecond
5263 laser texturization for improvement of photovoltaic cells : Black Silicon. J
5264 Optolectron Adv Mater 2010;12:621–5.

5265 [62] Gao Y, Wu B, Zhou Y, Tao S. A two-step nanosecond laser surface texturing process
5266 with smooth surface finish. Appl Surf Sci 2011;257:9960–7.

5267 [63] Horzel J, Allebe C, Szlufcik J, Sivoththaman S. Development of RTP for industrial
5268 solar cell processing. Sol Energy Mater Sol Cells 2002;72:263–9.

5269 [64] Saenger MF, Sun J, Schädel M, Hilfiker J, Schubert M, Woollam JA. Spectroscopic
5270 ellipsometry characterization of SiN_x anti-reflection films on textured multicrystalline
5271 and monocrystalline silicon solar cells. Thin Sol Films 2010;518:1830–4.

5272 [65] Lamers MWPE, Butler KT, Harding JH, Weeber A. Interface properties of a-
5273 SiN_x:H/Si to improve surface passivation. Solar Energy Mater Solar Cells
5274 2012;106:17–21.

5275 [66] Richards BS. Single-material TiO_2 double-layer anti-reflection coatings. Solar Energy
5276 Mater Solar Cells 2003;79:369–90.

5277 [67] González-Díaz B, Guerrero-Lemus R, Borchert D, Hernández-Rodríguez C, Martínez-
5278 Duart JM. Low-porosity porous silicon nanostructures on monocrystalline silicon
5279 solar cells. Phys E 2007;38:215–8.

5280 [68] Guerrero-Lemus R, Moreno JD, Martín-Palma RJ, Ben-Hander FA, Martínez-Duart
5281 JM, Fierro JLG, et al. Influence of oxidation and carbon-containing contamination in
5282 the stabilization of the luminescence in porous silicon. Thin Sol Films 1999;354:34–7.

5283 [69] Mockevičienė S, Adlienė D, Prosyčevas I, Kundrotas J, Čerškus A, Baltušnikas A.
5284 Fabrication influence on the surface morphology and structure of vapour etched
5285 porous silicon, Lithuanian J Phys 2011;51:237-47.

5286 [70] Bilyalov RR, Lüdemann R, Wettling W, Stalmans L, Poortmans J, Nijs J et al.
5287 Multicrystalline silicon solar cells with porous silicon emitter. Solar Energy Mater
5288 Solar Cells 2000;60:391–420.

5289 [71] Hocine D, Belkaid MS, Pasquinelli M, Escoubas L, Simon JJ, Rivière GA et al.
5290 Improved efficiency of multicrystalline silicon solar cells by TiO2 anti-reflection
5291 coatings derived by APCVD process. Mater Sci Semicond Process 2013;16:113–7.

5292 [72] Szlufcik J, Agostinelli G, Duerinckx F, Van Kerschaver E, Beaucarne G. Low Cost
5293 Industrial Technologies of Crystalline Silicon Solar Cells. In: Markvart T, Castañer L.
5294 editors. Solar Cells: Materials, Manufacture and Operation. Germany: Elsevier, 2005,
5295 p 89-120.

5296 [73] Ralph EL. Recent advancements in low cost solar cell processing, Proc. 11th IEEE
5297 Photovoltaic Specialists Conference, Scottsdale, Arizona, May 6-8, 1975:315-6

5298 [74] Schubert G, Huster F, Fath P. Physical understanding of printed thick-film front
5299 contacts of crystalline Si solar cells—Review of existing models and recent
5300 developments. Solar Energy Mater Solar Cells 2006;90:3399–406.

5301 [75] Kwon T, Kim S, Kyung D, Jung W, Kim S, Lee Y et al. The effect of firing
5302 temperature profiles for the high efficiency of crystalline Si solar cells. Solar Energy
5303 Mater Solar Cells 2010;94:823–9.

5304 [76] Spiegel M, Gerhards C, Huster F, Jooss W, Fath P, Bucher E. Industrially attractive
5305 front contact formation methods for mechanically V-textured multicrystalline silicon
5306 solar cells. Solar Energy Mater Solar Cells 2002;74:175–82.

5307 [77] Chong CM, Wenham SR, Green MA. High-efficiency, laser grooved, buried contact
5308 silicon solar cells. Appl Phys Lett 1988;52:407–9.

5309 [78] Ho AWY, Wenham SR. Buried contact solar cells with innovative rear localised
5310 contacts. Prog Photovoltaics Res Appl 2004;12:297–308.

5311 [79] Kang J, You J, Kang C, Pak JJ, Kim D. Investigation of Cu metallization for Si solar
5312 cells. Solar Energy Materials and Solar Cells 2002;74:91–6.

5313 [80] Beaucarne G, Schubert G, Hoornstra J, Horzel J, Glunz SW. Summary of the Third
5314 Workshop on Metallization for Crystalline Silicon Solar Cells. Energy Procedia
5315 2012;21:2–13.

5316 [81] Riegel S, Mutter F, Lauermann T, Terheiden B, Hahn G. Review on screen printed
5317 metallization on p-type silicon. Energy Procedia 2012;21:14–23.

5318 [82] Urrejola E, Peter K, Plagwitz H, Schubert G. Silicon diffusion in aluminum for rear
5319 passivated solar cells. Appl Phys Lett 2011;98:153508/3.

5320 [83] Hannebauer H, Dullweber T, Baumann U, Falcon T, Brendel R. 21.2%-efficient
5321 fineline-printed PERC solar cell with 5 busbar front grid. Phys. Status Solidi (RRL)
5322 Rapid Res Lett 2014;8:675-9.

5323 [84] Lauermann T, Fröhlich B, Hahn G, Terheiden B. Design Considerations for Industrial
5324 Rear Passivated Solar Cells. 38th IEEE Photovoltaic Specialists Conference (PVSC)
5325 2012:001710–5.

5326 [85] Clement F, Menkoe M, Erath D, Kubera T, Hoenig R, Kwapil W et al. High
5327 throughput via-metallization technique for multi-crystalline metal wrap through

5328 (MWT) silicon solar cells exceeding 16% efficiency. Solar Energy Mater Solar Cells
5329 2010;94:51–6.

5330 [86] http://www.solarpowerworldonline.com/2013/05/ja-solar-mass-produces-metal-wrap-
5331 through-solar-cells/

5332 [87] http://www.engineersonline.nl/nieuws/id16444-ja-solar-en-ecn-bundelen-krachten-
5333 voor-introductie-van-hoogrendement-pv-modules.html

5334 [88] Fellmeth T, Menkoe M, Clement F, Biro D, Preu R. Highly efficient industrially
5335 feasible metal wrap through (MWT) silicon solar cells. Solar Energy Mater Solar
5336 Cells 2010;94:1996–2001.

5337 [89]https://www.itri.org.tw/eng/Content/MsgPic01/Contents.aspx?SiteID=1&MmmID=6201
5338 70236661141772&MSid=620170245320003156

5339 [90] Fellmeth T, Fritz S, Menkoe M, Mingirulli N, Glatthaar M, Clement F et al.
5340 Development of crystalline silicon based metal wrap through (MWT) solar cells for
5341 low concentrator (2-30X) supplications, 24th European PV Solar Energy Conference
5342 and Exhibition, 21-25, Hamburg, Germany 2009: 711-6.

5343 [91] Clement F, Menkoe M, Hoenig R, Haunschild J, Biro D, Preu R et al. Pilot-line
5344 processing of screenprinted Cz-Si MWT solar cells exceeding 17% efficiency.
5345 Proceeding of the 34th IEEE PVSC, Philadelphia, USA 2009:1-5.

5346 [92] Gee JM, Kumar P, Howarth J, Schroeder T, Franklin J, Dominguez J et al.
5347 Development of industrial high-efficiency back-contact czochralski-silicon solar cells.
5348 Prog Photovolt: Res Appl 2011;19:887–93.

5349 [93] Schoonderbeek A, Ostendorf A. Novel industrial approaches in solar-cell production,
5350 SPIE 2008:10.1117/2.1200804.1132-1-3.

5351 [94] Auriac N, Grange B, Cabal R, Maris-Froelicha A, Ribeyron PJ. High efficiency
5352 bifacial solar cell developed on monocrystalline Si and transferred to multicrystalline
5353 Si. Energy Procedia 2011;8:427–34.

5354 [95] Ceccaroli B, Lohne O. Solar grade silicon feedstock. In: Luque A, Hegedus S, editors.
5355 Handbook of Photovoltaic Science and Engineering, West Sussex: John Wiley &
5356 Sons; 2011 (2nd edition), p. 265 - 308.

5357 [96] Yuge N, Abe M, Hanazawa K, Baba H, Nakamura N, Kato Y, Sakaguchi Y, Hiwasa
5358 S, Aratani F, Purification of metallurgical-grade silicon up to solar grade, Prog in
5359 Photov: Res. Appl. 2001;9:203.

5360 [97] Zahedi C, Enebakk E, Friestad K, Dolmen MG, Heide J, Buseth T, Tronstad R,
5361 Dethloff C, Peter K, Kopecek R, Melnyk I, Fath P. Solar grade silicon from
5362 metallurgical route. In Technical Digest of the International PVSEC 2004;14:26.

5363 [98] Hoffmann V, Peter K, Djordjevic-Reiss J, Enebakk E, Hakedal JT, Tronstad R,
5364 Vlasenko T, Buchkovskaja I, Beringov S, Bauer M, First results on industrialization
5365 of Elkem Solar Silicon at Pillar JSC and Q-Cells, Proc. European Photov. Sol. Ener.
5366 Conf. 2008;23:1117.

5367 [99] Liang ZC, Chen DM, Liang XQ, Yang ZJ, Shen H, Shi J, Crystalline Si solar cells
5368 based on solar grade silicon materials, Renewable Energy2010;35:2297.

5369 [100] Kraiem J, Drevet B, Cocco F Enjalbert N, Dubois S, Camel D, Grosset-Bourbange D,
5370 Pelletier D, Margaria T, Einhaus R, High performance solar cells made from 100%
5371 UMG silicon obtained via the PHOTOSIL process, Proc. IEEE Photovoltaic
5372 Specialists Conf 2010;35:1427.

5373 [101] Míguez JM, Bullón, Ordás R, Diéguez J, Miranda A, Souto A, Pérez A,
5374 MoralejoB,Carballo T, Martínez O, Jiménez J, Parra V, UMG-Si based PV materials
5375 and devices: current status and future trends, International Workshop on Crystalline
5376 Silicon Solar Cells 2012;6:6.O.1

5377 [102] Stoddard N, Wu B, Witting I, Wagener M, Park Y, Rozgonyi G, Clark R. Casting
5378 Single Crystal Silicon: Novel Defect Profiles from BP Solar's Mono2TM Wafers.
5379 Solid State Phenomena 2008;131-133:1.

5380 [103] Gu X, Yu X, Guo K, Chen L, Wang D, Yang D, Seed-assisted cast quasi-single
5381 crystalline silicon for photovoltaic application: Towards high efficiency and low cost
5382 silicon solar cells, Sol. Energy Mat. Sol.Cells 2012;101:95.

5383 [104] Jouini A, Ponthenier D, Lignier H, Enjalbert N, Marie B, Drevet B, Pihan E, Cayron
5384 C, Lafford T, Camel D, Improved multicrystalline silicon ingot crystal quality through
5385 seed growth for high efficiency solar cells, Prog. Photovolt: Res. Appl. 2012;20:735.
5386

5387 [105] Guerrero I, Parra V, Carballo T, Black A, Miranda M, Cancillo D, Moralejo B,
5388 Jiménez J, Lelièvre JF, del Cañizo C, About the origin of low wafer performance and
5389 crystal defect generation on seed-cast growth of industrial moonlike silicon ingots,
5390 Prog. in Photov: Res. Appl. DOI: 10.1002/pip.2344. pp.923-32

5391 [106] Kalejs JP, Silicon ribbons and foils—state of the art, Sol. Energy Mat. Sol. Cells
5392 2002;72:139.

5393 [107] Hahn G, Gabor AM, 16% efficiency on encapsulated large area screen printed string
5394 ribbon cell, Proc. World Conf. Photov. Ener. Conv. 2003;3:1289.

5395 [108] Seren S, Kaes M, Gutjahr A, Burgers AR, and Schönecker A, Efficiency potential of
5396 RGS silicon from current R&D production, Proc. European Photov. Solar Ener. Conf.
5397 2007;22:855.

5398 [109] Derbouza A, Slaoui A, Jolivet E, de Moro F, Belouet C, N-type silicon RST ribbon
5399 solar cells, Sol. Energy Mat. Sol.Cells 2012;107:212.

5400 [110] Kaes M, Hahn G, Metz A, Agostinelli G, Ma Y, Junge J, Zuschlag A, Groetschel D,
5401 Progress in High Efficiency Processing of EFG Silicon Solar Cells, Proc. European
5402 Photov. Solar Ener. Conf. 2007;22:897.

5403 [111] Rohatgi A, Kim DS, Nakayashiki K, Yelundur V, Rounsaville B, High-efficiency
5404 solar cells on Edge-Defined Film-Fed Grown (18.2%) and String Ribbon (17.8%)
5405 Silicon by Rapid Thermal Processing, Appl. Phys. Let. 2004;84(1):145.

5406 [112] Schmidt W, Woesten B, Kalejs J, Manufacturing technology for ribbon silicon (EFG)
5407 wafers and solar cells, Prog. in Photov: Res. Appl. 2002;10(2):129.

5408 [113] Cichoszewskia J, Reuter J, Werner JA, , +0.4% Efficiency gain by novel texture for
5409 String Ribbon solar cells, Sol. Energy Mat. Sol.Cells 2012;101:1.

5410 [114] Buonassisi T, Istratov A, Marcus M, Lai B, Cai Z, Heald S,Weber E, Engineering
5411 metal-impurity nanodefects for low-cost solar cells, Nat. Mater. 2005;4:676.

5412 [115] Härkönen J, Lempinen VP, Juvonen T, Kylmäluoma J, Recovery of minority carrier
5413 lifetime in low-cost multicrystalline silicon, Sol. Energ. Mat. Sol. Cells 2003;73:125.

5414 [116] Pickett MD, Buonassisi T, Iron point defect reduction in multicrystalline silicon solar
5415 cells, Applied Physics Letters 2008:92;122103.

5416 [117] Rinio M, Yodyunyong A, Keipert-Colberg S, Mouafi YPB, Borchert D,
5417 Montesdeoca-Santana A, Improvement of multicrystalline silicon solar cells by a low
5418 temperature anneal after emitter diffusion, Prog. Photovoltaics Res. Appl.
5419 2011;19(2):165.

5420 [118] Talvitie H, Vähänissi V, Haarahiltunen A, Yli-Koski M, Savin H, Phosphorus and
5421 boron diffusion gettering of iron in monocrystalline silicon, J. Appl. Physics
5422 2011;109(9):93505.

5423 [119] Lelièvre JF, Hofstetter J, Peral A, Hoces I, Recart F and del Cañizo C, Dissolution and
5424 gettering of iron during contact co-firing, Energy Procedia 2011;8:257.

5425 [120] Hofstetter J, Fenning DP, Lelièvre JF, del Cañizo C, Buonassisi T, Engineering metal
5426 precipitate size distributions to enhance gettering in multicrystalline silicon, Phys.
5427 Status Solidi A 2012;209(10):1861.

5428 [121] Salami J, Pham T, Khadilkar Ch, McViker K, Shaikh A, Characterization of screen
5429 printed phosphorous diffusion paste for silicon solar cells, Technical Digest Intern.
5430 Photov. Sol. Ener. Conf 2004;14:263.

5431 [122] Gangopadhyay U, Park S, Kim K, Park J, Kim D, Yi J, Large area mono-crystalline
5432 silicon solar cell using SOD, Proc. World Conf. Photovoltaic Ener. Conv.
5433 2003;3:1431.

5434 [123] Hoornstra J, van Strien W, Lamers M, Tool K, Weeber A, High throughput in-line
5435 diffusion: emitter and cell results, Proc. European Photov. Solar Ener. Conf.
5436 2007;22:1586.

5437 [124] Liu Z, Takato H, Togashi C, Sakata I, Oxygen-atmosphere heat treatment in spin-on
5438 doping process for improving the performance of crystalline silicon solar cells, Appl.
5439 Phys. Let. 2010;96:153503.

5440 [125] Lee YY, Ho WJ, Syu JK, Lai QR, Yu CM, 17.9% efficiency silicon solar cells by
5441 using spin-on films processes, Prog. Electromag. Res. Symp. (PIERS) Proc. 2011:780.

5442 [126] Ramanathan S, Meemongkolkiat V, Das A, Rohatgi A, KoehlerI, Understanding and
5443 fabrication of 20% efficient cells using spin-on-based simultaneous diffusion and
5444 dielectric passivation, IEEE J. Photovoltaics 2012:2(1):22.

5445 [127] Bentzen A, Holt A, Christensen JS, Svensson BG, High concentration in-diffusion of
5446 phosphorus in Si from a spray-on source, J. Appl. Phys. 2006;99:64502.

5447 [128] Kim DS, Hilali MM, Rohatgi A, Nakano K, Hariharan A, Matthei K, Development of
5448 a Phosphorus Spray Diffusion System for Low-Cost Silicon Solar Cells,
5449 J.Electrochem. Soc. 2006;153:A1391.

5450 [129] Voyer C, Buettner T, Bock R, Biro D, Preu R. Microscopic homogeneity of emitters
5451 formed on textured silicon using in-line diffusion and phosphoric acid as the dopant
5452 source, Sol. Energ. Mat. Sol. Cells 2009;93:932.

5453 [130] Armigliato A, Nobili D, Solmia S, Blendin G, Schum B, Lachowicz A, Horzel J,
5454 Characterization of the PSG/Si interface of H3PO4 doping process for solar cells, Sol.
5455 Ener. Mat. Sol. Cells2011;95:3099.

5456 [131] Fallisch A, Wagenmann D, Keding R, Trogus D, Hofmann M, Rentsch J, Reinecke H,
5457 Biro D, Analysis of phosphorus-doped silicon oxide layers deposited by means of
5458 PECVD as a dopant sourcein diffusion processes, IEEE J. Photovoltaics
5459 2012;2(4):450.

5460 [132] Horzel J, Choulat P, Szlufcik J, Nijs J, Völk P, Rechart J, Piechulla A, Haase J, Möller
5461 R, Wangdel G, Wahl G, Schomann F, Schmitt W, High throughput diffusion for
5462 industrial solar cell production, Proc. European Photov. Sol. Ener. Conf.
5463 2001;17:1367.

5464 [133] Pletzer TM, Stegemanny EFR, Windgassen H, Suckow S, Bätznerz DL, Kurz H,
5465 Gettering in multicrystalline silicon wafers with screen-printed emitters, Prog.
5466 Photovolt: Res. Appl. 2011;19:946.

5467 [134] Recart F, Freire I, Pérez L, Lago-Aurrekoetxea R, Jimeno JC, Bueno G, Screenprinted
5468 boron emitters for solar cells, Sol.Ener. Mat. Sol. Cells 2007;91:897.

5469 [135] Das A, Kim DS, Nakayashiki K, Rounsaville B, Meemongkolkiat V, Rohatgi A,
5470 Boron diffusion with boric acid for high efficiency silicon solar cells, J.Electroch.
5471 Soc. 2010;157(6):H684.

5472 [136] Ryu K, Upadhyaya A, Ok YW, Kang MH, Upadhyaya W,Metin L, Xu H, Bhanap A,
5473 Rohatgi A, High-efficiency n-type Si solar cells with novel inkjet-printed boron
5474 emitters, IEEEElectr. Device Let. 2012;33(6):854.

5475 [137] Mihailetchi VD, Komatsu Y, Geerligs LJ, Nitric acid pretreatment for the passivation
5476 of boron emitters for n-typebase silicon solar cells, Appl. Phys. Let. 2008:92:63510.

5477 [138] Phang SP, Liang W, Wolpensinger B, Kessler MA, Macdonald D, Tradeoffs between
5478 impurity gettering, bulk degradation and surface passivationof boron-rich layers on
5479 silicon solar cells, IEEE J. Photovoltaics 2013:3(1):261.

5480 [139] Altermatt PP, Plagwitz H, Bock R,Schmidt J, Brendel R, Kerr MJ, Cuevas A, The
5481 surface recombination velocity at boron-doped emitters: comparison between various
5482 passivation techniques, Proc. European Photovoltaic. Sol. Ener. Conf. 2006;21:647.

5483 [140] Pawlak BJ, Janssens T, Singh S, Kuzma-Filipe I, Robbelein J, Posthuma NE,
5484 Poortmans J, Cristiano F, Bazizi EM, Studies of implanted boron emitters for solar
5485 cellapplications,Prog. Photovolt: Res. Appl. 2012;20:106.

5486 [141] Benick J, Müller R, Bateman N, Hermle M, Fully implanted n-type PERT solar cells,
5487 Proc. European Photov. Sol. Ener. Conf. 2012;27:676.

5488 [142] Hoornstra J, Heurtault B, Stencil print applications and progress for crystalline silicon
5489 solar cells, Proc. European Photov.Sol .Ener. Conf. 2009;24:989.

5490 [143] Pham T, Zhang W, Gou T, Buzby D, Murphy K, Improving electrical performance by
5491 double print method and non-contact busbars, Proc. European Photov. Sol. Ener.
5492 Conf. 2010;25:2378.

5493 [144] Galiazzo M, Furin V, Tonini D, Cellere G, Baccini A, Double printing of front contact
5494 Ag in c-Si solar cells, Proc. European Photov. Sol. Ener. Conf. 2010;25:2338.

5495 [145] Dullweber T, Gatz S, Hannebauer H, Falcon T, Hesse R, Schmidt J, Brendel R,
5496 Towards 20% efficient large-area screen-printed rear-passivated silicon solar cells,
5497 Prog. Photovolt: Res. Appl. 2012;20:630.

5498 [146] Huster F, Fath P, Bucher E, Roller printed mc-Si solar cells with optimized fill factors
5499 of 78%, Proc. European Photov.Sol .Ener. Conf. 2001;17:1743.

5500 [147] Huljic DM, Thormann S, Preu R, Lüdemann R, Willeke G, Pad printing front contacts
5501 for c-Si solar cells-a technological and economical evaluation, Proc. IEEE
5502 Photovoltaic Solar Specialist Conf. 2002;29:126.

5503 [148] Braun S, Emre E, Raabe B, Hahn G, Electroless nickel and copper metallization:
5504 contact formation on crystalline silicon and background plating behavior on PECVD
5505 SiNx:H layers, Proc. European Photov. Sol. Ener. Conf. 2010;25:1892.

5506 [149] Martín J, Montalbán C, Apraiz A, Aguerre JP , Jimeno JC, Gutiérrez R, Gizachew
5507 YT, Escoubas L, Simon JJ, Pasquinelli M, Loiret J, Leguen PY, Silicon solar cells
5508 metallization by inkjet printing, Proc. European Photov. Sol. Ener. Conf.
5509 2010;25:1997.

5510 [150] Mette A, Richter PL, Hörteis M, Glunz SW, Metal aerosol jet printing for solar cell
5511 metallization, Prog. Photovolt: Res. Appl. 2007;15:621.

5512 [151] Mette A, Schetter C, Wissen D, Lust S, Glunz SW, Willeke G, Increasing the
5513 efficiency of screen-printed silicon solar cells by light-induced silver plating, Proc.
5514 World Conf. Photovol. Energy Conv. 2006;4:1056.

5515 [152] van Hest M, Habas SE, Underwood JM, Pasquarelli RM, Hersh P, Miedaner A, Curtis
5516 CJ, Ginley DS, Direct write metallization for photovoltaic cells and scaling thereof,
5517 Proc. IEEE Photov. Specialists Conf. 2010;35:3626.

5518 [153] Rahman MZ. Status of Selective Emitters for p-Type c-Si Solar Cells. Optics and
5519 Photonics Journal 2012;2:129–34.

5520 [154] Zhao XJ, Wang A, Altermatt PP, Wenham SR, Green MA. 24% efficient PERL
5521 silicon solar cell: recent improvement in high efficiency silicon cell research. Solar
5522 Energy Materials and Solar Cells 1996; 41/42: 87–99.

5523 [155] Kim LH, Cho KY, Oh DJ, Shim JM Lee EJ, Lee HW, Choi JY, Kim JS, Shin JE, Lee
5524 Sh, Lee HS, Exceeding 19% efficient 6 inch selective emitter crystalline silicon solar
5525 cell by screen printed metal contacts: transition of heavy and shallow emitter
5526 conditions, Proc. European Photov. Sol. Ener. Conf. 2010;25:2694.

5527 [156] Zerga A, Slaoui A, Muller JC, Bazer-Bachi B, Ballutaud D, Lê Quang N, Goaer G,
5528 Selective emitter formation for large-scale industrially mc-Si solar cells by hydrogen
5529 plasma and wet etching, Proc. European Photov. Sol. Ener. Conf. 2006;21:865.

5530 [157] Haverkamp H, Dastgheib-Shirazi A, Raabe B, Book F, Hahn G, Minimizing the
5531 electrical losses on the front side: development of a selective emitter process from a
5532 single diffusion, Proc. IEEE Photov. Special. Ener. Conf. 2008;33:430.

5533 [158] Rudolph D, Peter K, Meijer A, Doll O, Köhler I, Etch Back Selective Emitter Process
5534 with Single POCl3 Diffusion, Proc. European Photov. Sol. Ener. Conf. 2011;26:1349.

5535 [159] Horzel J, Szlufcik J, Nijs J, High efficiency industrial screen-printed selective emitter
5536 solar cels, Proc. European Photov. Sol. Ener. Conf. 2000;16:1112.

5537 [160] Esturo-Breton A, Masouleh FB, Breselge M, Frieß T, Geiger M, Holbig E, Isenberg J,
5538 Keller S, Kühn T, Maier J, Münzer A, Schlosser R, Schmid A, Voyer C, Winter P,
5539 Bayer K, Krümberg J, Henze S, Melnyk I, Schmidt M, Klingbeil S, Walter F,
5540 Kopecek R, Peter K, Fath P, Crystalline Si solar cells with selective emitter for
5541 industrial mass production, Proc. European Photov. Sol. Ener. Conf. 2009;24:1068.

5542 [161] Uzuma A, Hamdi A,NagashimaS, Suzuki S, Suzuki H, YoshibaS, DhamrinM,
5543 KamisakoK, Sato H, Katsuma K, Kato K, Selective emitter formation process using
5544 single screen-printed phosphorus diffusion source, Solar Ener. Mat. Sol. Cell.
5545 2013;109:288.

5546 [162] Hallam B, Wenham S, Lee H, Lee E, Lee H, Lee H, Kim J, Shin J, Cho K, Kim J,
5547 Record efficiency on large area p-type Czochralski silicon substrates, Jap. J. Appl.
5548 Phys. 2012:51:10NA08.

5549 [163] Glunz SW, High-efficiency crystalline silicon solar cells, Advances in
5550 Optoelectronics 2007, article ID 97370, doi 10.1155/2007/97370.

5551 [164]Green MA, Zhao J, Wang A, Wenham SR, Progress and Outlook for High Efficiency
5552 CrystallineSilicon Solar Cells, Sol. Ener.Mat. Solar Cells 2001;65:9.

5553 [165] Das A, Meemongkolkiat V, Kim DS, Ramanathan S, Rohatgi A, 20% efficient
5554 screen-printed cells with spin-on dielectric passivated boron back surface field, IEEE
5555 Trans. Elect. Dev. 2010;57(19):2462.

5556 [166] Schmidt J, Merkle A, Brendel R, Hoex B, van de Sanden MCM, Kessels WMM,
5557 Surface passivation of high-efficiency silicon solar cells by atomic-layer-deposited
5558 Al_2O_3, Prog. Photov: Res. Appl.2008;16:461.

5559 [167] Hallam B, Tjahjono B, Wenham S, Effect of PECVD silicon oxynitride film
5560 composition on the surface passivation of silicon wafers, Solar Ener. Mat. Cell.
5561 2012;96:173.

5562 [168] Suwito D, Jäger U, Benick J, Janz S, Hermle M, Glunz SW, Industrially feasible rear
5563 passivation and contactingscheme for high-efficiency n-type solar cellsyielding a Voc
5564 of 700 mV, IEEE Trans. Elect. Dev. 2010;57(8):2032.

5565 [169] Rostan PJ, Rau U, Nguyen VX, Kirchartz T, Schubert MB, Werner JH, Low
5566 temperatura a-Si:H/Zn/Al back contacts for high-efficiency silicon solar cells, Sol.
5567 Energy Mat. Sol.Cells 2006;90(9):1345.

5568 [170] Chen F, Romijn I, Weeber A, Tan J, Hallam B, Cotter J, Relationship between
5569 PECVD silicon nitride film composition and surface and edge passivation, Proc.
5570 European Photov. Sol. Ener. Conf. 2007;22:1053.

5571 [171] Vermang B, Goverde H, Lorenz A, Uruena A, Vereecke G, Meersschaut G,
5572 Cornagliotti E, Rothschild A, John J, Poortmans J, Mertens R, On the blistering of
5573 atomic layer deposited Al2O3 as Si surface passivation, Proc. IEEE Photov. Specialist
5574 Conf. 2011;37:3562.

5575 [172] Dauwe S, Mittelstädt L, Metz A, Hezel R, "Experimental evidence of parasitic
5576 shunting in silicon nitride rear surface passivated solar cells, Prog. Photovolt: Res.
5577 Appl. Prog.in Photov: Res. Appl. 2002;10(4):271.

5578 [173] Mack S, Wolf A, Brosinsky C, Schmeisser S, Kimmerle A, Saint-Cast P, Hofmann M,
5579 Biro D, Silicon surface passivation by thin thermal oxide/PECVD layer stack systems,
5580 IEEE J. Photov. 2011;1(2):135.

5581 [174] Ortega P, Martín I, López G, Colina M, Orpella A, Voz C, Alcubilla R, p-type c-Si
5582 solar cells based on rear side laser processing of Al2O3/SiCx stacks, Sol. Ener. Mat.
5583 Cell. 2012;106;80.

5584 [175] Vermang B, Goverde H, Tous L, Lorenz A, Choulat P, Horzel J, John J, Poortmans J,
5585 Mertens R, Approach for Al2O3 rear surface passivation of industrial p-type Si PERC
5586 above 19%, Prog. Photovol.: Res. Appl. 2012;20:269.

5587 [176] Wang Z, Han P, Lu H, Qian H, Chen L, Meng Q,Tang N, Gao F, Jiang Y, Wu J, Wu
5588 W, Zhu H, Ji J, Shi Z, Sugianto A, Mai L, Hallam B, Wenham S, Advanced PERC
5589 and PERL production cells with 20.3%record efficiency for standard commercial p-
5590 type siliconwafers, Prog. Photovolt: Res. Appl. 2012;20:260.

5591 [177] J. Schmidt, J. D. Moschner, J. Henze, S. Dauwe and R. Hezel, Recent progress in the
5592 surface passivation of silicon solar cells using silicon nitride, Proc. 19th EUPVSEC, 7-
5593 11 June 2004, Paris, France (2004), pp. 391-396.

5594 [178] P. Cousins, *et* al., “Generation 3: Improved performance at lower cost”, in
5595 Proceedings of the *35th*. PVSEC Hawaii, Honolulu, USA, pp. 275–78, (2010).

5596 [179] D. DeCeuster, P. Cousins, D. Rose, D. Vicente, P. Tipones, W. Mulligan, “Low cost,
5597 high volume production of >22% efficiency silicon solar cells”, Proc 22nd
5598 EUPVSEC, pp. 816-819 (2007).

5599 [180] M. Späth, P.C. de Jong, and J. Bakker, “A novel module assembly line using back
5600 contact solar cells”, in Technical Digest of the17th International Photovoltaic Solar
5601 Energy Conference, Fukuoka, Japan, 436 (2007).
5602
5603 [181] I. Bennett, W. Eerenstein, V. Rosca, „Reducing the cost of back-contact module
5604 technology”, Energy Procedia 38, 329 – 333 (2013).
5605
5606 [182] A. Drews et al., “HIP-MWT Solar Cells – Pilot-Line Cell Processing and Module
5607 Integration”, in Proceedings of the 27th European Photovoltaic Solar Energy
5608 Conference, Frankfurt, Germany, 828 - 831 (2012).
5609
5610 [183] M.D. Lammert and R.J. Schwartz, “The interdigitated back contact solar cell: a silicon
5611 solar cell for use in concentrated sunlight”, IEEE Transactions on Electron Devices,
5612 ED-24 (4), 337-42, (1977).
5613
5614 [184] F. Granek, Ph.D thesis, “High-efficiency Back-Contact Back-Junction Silicon Solar
5615 Cells”, Verlag Dr. Hut, ISBN 978-3-86853-348-4 (2009).
5616
5617 [185] R.M. Swanson, A.K. Beckwith, R.A. Crane, W.D. Eades, Y.H. Kwark, and R.A.
5618 Sinton, “Point-contact silicon solar cells”, IEEE Transactions on Electron Devices, 31
5619 (5), 661-4, (1984).
5620
5621 [186] R.A. Sinton, P. Verlinden, D.E. Kane, and R.M. Swanson, “Development efforts in
5622 silicon backside-contact solar cells”, in Proceedings of the 8th European Photovoltaic
5623 Solar Energy Conference, Florence, Italy, 1472-6 (1988).
5624
5625 [187] R.R. King, R.A. Sinton, and R.M. Swanson, “One-Sun, Single-Crystalline Silicon
5626 Solar Cell Research”, Solid State Electronics Laboratory, Stanford University,
5627 Stanford, (1991).
5628
5629 [188] R.A. Sinton, P.J. Verlinden, R.A. Crane, R.M. Swanson, C. Tilford, J. Perkins, and K.
5630 Garrison, “Large-area 21% efficient Si solar cells”, in Proceedings of the 23rd IEEE
5631 Photovoltaic Specialists Conference, Louisville, Kentucky, USA, 1490, 157-61
5632 (1993).
5633
5634 [189] P.J. Verlinden, R.A. Sinton, K. Wickham, R.A. Crane, and R.M. Swanson, “Backside-
5635 contact silicon solar cells with improved efficiency for the `96 world solar challenge”,

5636 in Proceedings of the 14th European Photovoltaic Solar Energy Conference,
5637 Barcelona, Spain, 96-9 (1997).
5638
5639 [190] W.P. Mulligan, D.H. Rose, M.J. Cudzinovic, D.M. De Ceuster, K.R. McIntosh, D.D.
5640 Smith, and R.M. Swanson, “Manufacture of solar cells with 21% efficiency”, in
5641 Proceedings of the 19th European Photovoltaic Solar Energy Conference, Paris,
5642 France, 387-90 (2004).
5643
5644 [191] E. van Kerschaver, R. Einhaus, J. Szlufcik, J. Nijs, and R. Mertens, “A novel silicon
5645 solar cell structure with both external polarity contacts on the back surface”, in
5646 Proceedings of the 2nd World Conference on Photovoltaic Energy Conversion,
5647 Vienna, Austria, 1479-82 (1998).
5648
5649 [192] J.H. Bultman, M.W. Brieko, A.R. Burgers, J. Hoornstra, A.C. Tip, and A.W. Weeber,
5650 “Interconnection through vias for improved efficiency and easy module
5651 manufacturing of crystalline silicon solar cells”, Solar Energy Materials and Solar
5652 Cells, 65, 339-45, (2001).
5653
5654 [193] F. Clement, et al., “Industrially feasible MC-Si metal wrap through (MWT) solar cells
5655 with high emitter sheet resistances exceeding 16% efficiency”, in Proceedings of the
5656 23rd European Photovoltaic Solar Energy Conference, Valencia, Spain, (2008).
5657
5658 [194] J.M. Gee, W.K. Schubert, and P.A. Basore, “Emitter wrap-through solar cell”, in
5659 Proceedings of the 23rd IEEE Photovoltaic Specialists Conference, Louisville,
5660 Kentucky, USA, 265-70 (1993).
5661
5662 [195] D. Kray, et al., “Progress in high-efficiency emitter-wrap-through cells on medium
5663 quality substrates”, in Proceedings of the 3rd World Conference on Photovoltaic
5664 Energy Conversion, Osaka, Japan, 1340-3 (2003).
5665
5666 [196] P. Engelhart, N.-P. Harder, R. Grischke, A. Merkle, R. Meyer, and R. Brendel, “Laser
5667 structuring for back junction silicon solar cells”, Progress in Photovoltaics: Research
5668 and Applications, 15, 237-43, (2006).
5669
5670 [197] S. Hermann, et al., “21.4%-efficient emitter wrap-through RISE solar cell on large
5671 area and picosecond laser processing of local contact openings”, in Proceedings of the
5672 22nd European Photovoltaic Solar Energy Conference, Milan, Italy, 970-5 (2007).
5673
5674 [198] A. Kress, O. Breitenstein, S. Glunz, P. Fath, G. Willeke, and E. Bucher,
5675 “Investigations on low-cost back-contact silicon solar cells”, Solar Energy Materials
5676 and Solar Cells, 65, 555-60, (2001).
5677
5678 [199] E.V. Kerschaver, G. Beaucarne, “Back-contact solar cells: a review”, Progress in
5679 Photovoltaics: Research and Applications, 14, 107-123 (2006).
5680

5681 [200] D.A. Clugston and P.A. Basore, "PC1D version 5: 32-bit solar cell modeling on
5682 personal computers", in Proceedings of the 26th IEEE Photovoltaic Specialists
5683 Conference, Anaheim, California, USA, 207-10 (1997).
5684
5685 [201] J. Schmidt and A. Cuevas, "Electronic properties of light-induced recombination
5686 centers in boron-doped Czochralski silicon", Journal of Applied Physics, 86 (6), 3175-
5687 80, (1999).
5688
5689 [202] S.W. Glunz, S. Rein, J.Y. Lee, and W. Warta, "Minority carrier lifetime degradation
5690 in boron-doped Czochralski silicon", Journal of Applied Physics, 90 (5), 2397-404,
5691 (2001).
5692
5693 [203] D. Macdonald and L.J. Geerligs, "Recombination activity of interstitial iron and other
5694 transition metal point defects in p- and n-type crystalline silicon", Applied Physics
5695 Letters, 85 (18), 4061-3, (2004).

5696 [204] J. Libal, et al., "N-type multicrystalline silicon solar cells: BBr3-diffusion and
5697 passivation of P^+-diffused silicon surfaces", in Proceedings of the 20th European
5698 Photovoltaic Solar Energy Conference, Barcelona, Spain, 793-6 (2005).
5699
5700 [205] C.J.J. Tool, H.C. Rieffe, R. Kinderman, R. Kopecek, K. Wambach, and L.J. Geerligs,
5701 "Solar cells on n-type multicrystalline silicon wafers by industrial processing
5702 techniques", in Proceedings of the 19th European Photovoltaic Solar Energy
5703 Conference, Paris, France, (2004).
5704
5705 [206] A. Cuevas, C. Samundsett, M.J. Kerr, D.H. Macdonald, H. Mäckel, and P.P.
5706 Altermatt, "Back junction solar cells on n-type multicrystalline and CZ silicon
5707 wafers", in Proceedings of the 3rd World Conference on Photovoltaic Energy
5708 Conversion, Osaka, Japan, 1, 963-6 (2003).
5709
5710 [207] J. Zhao and A. Wang, High Efficiency Real Emitter PERT Solar Cells on n-type FZ
5711 Single Crystalline Silicon Substrates, in 20th European Photovoltaic Solar Energy
5712 Conference and Exhibition, Barcelona, Spain, (2005).
5713
5714 [208] C. Schmiga, M. Hermle, and S.W. Glunz, Towards 20 % efficient n-type silicon solar
5715 cells with screen-printed aluminium-alloyed rear emitter, in Proceedings of the 23rd
5716 European Photovoltaic Solar Energy Conference and Exhibition, Valencia, Spain,
5717 (2008).
5718
5719 [209] J. Benick, B. Hoex, M.C.M. Van de Sanden, W.M.M. Kessels, O. Schultz, and S.
5720 Glunz, "Effective passivation of boron emitters with Al2O3 for high-efficiency n-type
5721 solar cells", Applied Physics Letters, 92 (24), 253504-1, (2008).
5722 [210] K.R. McIntosh, M.J. Cudzinovic, D.D. Smith, W.P. Mulligan, R.M. Swanson, "The
5723 choice of silicon wafer for the production of low-cost rear-contact solar cells", 3rd

5724 World Conference on Photovoltaic Energy Conversion; Osaka, Japan, (2003) 971-
5725 974.
5726 [211] A. Cuevas, M.J. Kerr, C. Samundsett, F. Ferrazza, and G. Coletti, “Millisecond
5727 minority carrier lifetimes in n-type multicrystalline silicon”, Applied Physics Letters,
5728 81 (26), 4952-4, (2002).
5729
5730 [212] F. Granek, C. Reichel, „Back-Contact Back-Junction Silicon Solar Cells under UV
5731 Illumination”, Solar Energy Materials and Solar Cells, 94, 1734 1740 (2010).
5732
5733 [213] M. Hermle, F. Granek, O. Schultz, and S. W. Glunz, „Analyzing the effects of front-
5734 urface fields on back-junction silicon solar cells using the charge-collection
5735 probability and the reciprocity theorem”, Journal of Applied Physics 103, 054507
5736 (2008)
5737
5738 [214] C. Reichel, F. Granek, J. Benick, O. Schultz-Wittmann, S. W. Glunz, „Comparison of
5739 Emitter Saturation Current Densities Determined by Injection-Dependent Lifetime
5740 Spectroscopy in High and Low Injection Regimes”, Progress in Photovoltaics:
5741 Research and Applications, Vol. 20, No. 1, 21-30 (2012).
5742
5743 [215] J.A. del Alamo and R.M. Swanson, “The physics and modeling of heavily doped
5744 emitters”, IEEE Transactions on Electron Devices, ED-31 (12), 1878-88, (1984).
5745
5746 [216] F. Granek, M. Hermle, C. Reichel, A. Grohe, O. Schultz-Wittmann, S. Glunz,
5747 “Positive effects of front surface fielding high-efficiency back-contact back-junction
5748 n-type silicon solar cells”, 33rd IEEE Photovoltaic Specialist Conference, San Diego,
5749 CA (2008).

5750 [217] F.Granek, M. Hermle, D. M. Huljić, O. Schultz-Wittmann and S. W. Glunz,
5751 “Enhanced lateral current transport via the front n^+-diffused layer of n-type high-
5752 efficiency back-junction back-contact silicon solar cell”, Progress in Photovoltaics 17,
5753 47-56 (2009).
5754 [218] S. Kluska, F. Granek, M., Rüdiger, H. Hermle, S. W. Glunz, “Modeling and
5755 optimization study of industrial n-type high-efficiency back-contact back-junction
5756 silicon solar cells”, Solar Energy Materials and Solar Cells, 94, 568-577 (2010)
5757
5758 [219] D.K. Schroder, R.N. Thomas, and J.C. Swartz, “Free carrier absorption in silicon”,
5759 IEEE Transactions on Electron Devices, ED-25 (2), 254-61, (1978)
5760
5761 [220] J. Isenberg and W. Warta, “Free carrier absorption in heavily doped silicon layers”,
5762 Applied Physics Letters, 84 (13), 2265-7, (2004).
5763
5764 [221] C. Reichel, M. Bivour, F. Granek, M. Hermle, S. W. Glunz, „Improved diffusion
5765 profiles in back-contacted back-junction Si solar cells with an overcompensated
5766 boron-doped emitter”, physica status solidi (a), Vol. 208, No. 12, 2871–2883, (2011)

[222] M. Hermle, F. Granek, O. Schultz-Wittmann, S. W. Glunz, “Shading Effects in Back-Junction Back-Contacted Silicon Solar Cells”, 33rd IEEE Photovoltaic Specialist Conference, San Diego, CA (2008)

[223] F. Dross, E. Van Kerschaver, and G. Beaucarne, “Minimization of the shadow-like losses for inter-digitated back-junction solar cells”, in Proceedings of the 15th International Photovoltaic Science & Engineering Conference, Shanghai, China, p. 971-2, (2005).

[224] C. Reichel, F. Granek, M. Hermle, S.W. Glunz, „Short-Circuit Current Losses in Back-Contacted Back–Junction Si Solar Cells: Experiment and Simulation of the Charge Collection Probability”, IEEE Journal of Photovoltaics, Vol. 3, Issue 1, 217 – 223 (2013).

[225] N.-P. Harder, V. Mertens, R. Brendel, Buried emitter solar cell structures: Decoupling of metallisation geometry and carrier collection geometry of back contacted solar cells, phys. stat. sol (RRL), vol. 2, pp.148-150, (2008).

[226] F. Granek, M. Hermle, C. Reichel, O. Schultz-Wittmann, S. W. Glunz, „High-efficiency back-contact back-junction solar cell: Research at Fraunhofer ISE”, 23rd European Photovoltaic Solar Energy Conference, Valencia, Spain, pp. 991-995, (2008)

[227] C. Reichel, M. Reusch, F. Granek, M. Hermle, S. W. Glunz, "Decoupling charge carrier collection and metallization geometry of back-contacted back-junction silicon solar cells by using insulating thin films", 35th IEEE Photovoltaic Specialist Conference, Honolulu, Hawaii, (2010)

[228] C. Reichel, F. Granek, M. Hermle, S.W. Glunz, „Back-contacted back-junction n-type silicon solar cells featuring an insulating thin film for decoupling charge carrier collection

[229] V. Mertens, S. Bordihn, Y. Larionova, N.-P. Harder, and R. Brendel, “The buried emitter cell concept: Interdigitated back-junction structure with virtually 100% emitter coverage of the cell area”, in Proceedings of the 24th European Photovoltaic Solar Energy Conference, Hamburg, Germany, (2009).

[230] N. Bateman, P. Sullivan, C. Reichel, J. Benick, M. Hermle, “High quality ion implanted boron emitters in an interdigitated back contact solar cell with 20% efficiency”, Energy Procedia 8, pp. 509–514 (2011)

[231] A. Grohe et al., “High-Efficient Ion Implanted Back Contact Cells for Industrial Application”, presented at 28th European Photovoltaic Solar Energy Conference, Paris, France (2013).

[232] N. Mingirulli, et al., “Efficient interdigitated back-contacted silicon heterojunction solar cells”, Physica status solidi (RRL), 5, pp. 159-61 (2011)

[233] U. Das et al. “Progress towards high efficiency all-back-contact heterojunction c-si solar cells”. Proc. 18th Workshop on Crystalline Silicon Solar Cells and Modules, pp. 70-7, (2008)

[234] Z. Shu, U. Das, J. Allen, R. Birkmire, S. Hegedus, “Experimental and simulated analysis of front versus all-back-contact silicon heterojunction solar cells: effect of interface and doped a-Si:H layer defects”, Progress in Photovoltaics: Research and Applications, published online, (2013).

[235] S. Baker-Finch, P. Basore, "Leveraging Silicon Epitaxy to Fabricate Excellent Front Surface Regions for Thin Interdigitated Back Contact Solar Cells", IEEE Journal of Photovoltaics, vol.PP, no.99, pp.1-6, 2013.

[236] Halm et al., “The Zebra cell concept – large area n-type interdigitated back contact solar cells and one-cell modules fabricated using standard industrial processing equipment”, in Proc. 27th European Photovoltaic Solar Energy Conference and Exhibition, Frankfurt, Germany, pp. 567-570, (2012).

[237] F. Castano, et al., “Industrially feasible >19% efficiency IBC cells for pilot line processing”, Proc. 37th IEEE Photovoltaic Specialists Conference, Seattle, USA (2011).

[238] G. Galbiati, V. Mihailetchi, R. Roescu, A. Halm, L. Koduvelikulathu, R. Kopecek, K. Peter, J. Libal, “Large-Area Back-Contact Back-Junction Solar Cell With Efficiency Exceeding 21%”, IEEE Journal of Photovoltaics , Vol. 3 , Iss. 1, 560 – 565, (2013)

[239] M. Lamers et al., “Towards 21% efficient n-Cz IBC based on screen-printing”, in Proc. 26th European Photovoltaic Solar Energy Conference and Exhibition, Hamburg, Germany (2011)

[240] R. Woehl, J. Krause, F. Granek, D. Biro, „19.7% efficient all screen-printed back-contact back-junction silicon solar cell with aluminum-alloyed emitter”, IEEE Electron. Dev. Lett., **32** (2011) 345.

[241] R. Woehl, “All-Screen-Printed Back-Contact Back-Junction Silicon Solar Cells with Aluminum-Alloyed Emitter”, Verlag Dr. Hut, ISBN 978-3-8439-0445-2 (2011)

[242] R. Sinton, et al., “Developments in module ready Si backside-contact solar cells”, Proc. 21st IEEE Photovoltaic Specialists Conference, pp.302-306, (1990)

[243] S. De Vecchia et al., “New metallization scheme for interdigitated back contact silicon heterojunction solar cells”, Energy Procedia Vol. 38, pp. 701 – 706 (2013)

[244] A. Teppe, P. Engelhart, and J. Müller, Method for the contact separation of electrically-conducting layers on the back contacts of solar cells and corresponding solar cells in US Patent, USA, WO 2006/042698 A1, (2006).

5853
5854 [245] D. Kray et al., "Industrial LCP selective emitter solar cells with plated contacts", Proc.
5855 35th IEEE Photovoltaic Specialists Conference, Honolulu, USA (2010).

5856 [246] Panasonic Press Release, Panasonic HIT® solar cell achieves world's highest energy
5857 conversion efficiency of 25.6% at research level, Panasonic Corp., Osaka, Japan,
5858 April 10, 2014
5859 (http://panasonic.co.jp/corp/news/official.data/data.dir/2014/04/en140410-
5860 4/en140410-4.html accessed January 11, 2016).

5861 [247] K. K. N. Koide, T. Sakai, T. Kuniyoshi, H. Katayama, N. Asano, T. Hieda, and J.
5862 Nakamura, "High efficient crystalline Si solar cells with rear heterojunction emitter
5863 and antireflective passivation layer," presented at the 23rd Photovoltaic Specialist
5864 Conf., Taipei, Taiwan, 2013.

5865 [248] Taguchi, Mikio, et al. "24.7% record efficiency HIT solar cell on thin silicon wafer."
5866 *IEEE Journal of Photovoltaics* 4 (2014): 96-99

5867 [249] Panasonic. *Panasonic HIT Module VBHN2xx SE19 EN data sheet.* https://eu-
5868 solar.panasonic.net/en/service/downloads-
5869 panasonic/?eID=tx_datamintsdamsearch_download&damId=2585 (accessed July
5870 2013).

5871 [250] Fuhs, W., K. Niemann, and J. Stuke. "Heterojunctions of amorphous silicon and
5872 silicon single crystals." *Tetrahedrally Bonded Amorphous Semiconductors.* Yorktown
5873 Heights, 1974. 345-50.

5874 [251] Tanaka, M., et al. "Development of New {a-Si/c-Si} Heterojunction Solar Cells: ACJ-
5875 HIT (Artificially Constructed Junction-Heterojunction with Intrinsic Thin-Layer)."
5876 *Jpn. J. Appl. Phys.* 31 (1992): 3518-22.

5877 [252] Baroughi, M. F., Jeyakumar, R., Vygranenko, Y., Khalvati, F., Sivoththaman, S.,
5878 Fabrication and characterization of amorphous Si/crystalline Si heterojunction devices
5879 for photovoltaic applications, J. Vac. Sci. and Technol. A **22** (2004): 1015-19.

5880 [253] Haschke, J.; Amkreutz, D.; Korte, L.; Ruske, F. & Rech, B. Towards wafer quality
5881 crystalline silicon thin-film solar cells on glass. Solar Energy Materials and Solar
5882 Cells , 2014, 128, 190 – 197.

5883 [254] Kühnapfel, S.; Gall, S.; Rech, B. & Amkreutz, D. Towards monocrystalline silicon thin
5884 films grown on glass by liquid phase crystallization. Solar Energy Materials and Solar
5885 Cells, Elsevier, 2015, 140, 86-91.

5886 [255] de Wolf, S., Descoeudres, A., Holman, Z.C. and Ballif, C. "High-efficiency Silicon
5887 Heterojunction Solar Cells: A Review." *Green* 2 (2012): 7-24.

[256] Sark, Wilfried G. J. H. M. van, Lars Korte, and Francesco Roca, *Physics and Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells.* 2011. Springer, 2011.

[257] Lucovsky, G., Y. Wu, H. Niimi, V. Misra, and J. C. Phillips. "Bonding constraint-induced defect formation at Si-dielectric interfaces and internal interfaces in dual-layer gate dielectrics." *J. Vac. Sci. Technol. B* 17 (1999): 1806-12.

[258] Hernández, J L, et al. "High Efficiency Copper Electroplated Heterojunction Solar Cells." *Proc. 27th European Photovoltaic Solar Energy Conference.* 2012. 655-656.

[259] Muñoz, D., et al. "Key Aspects on Development of High Efficiency Heterojunction and IBC-Heterojunction Solar Cells: Towards 22% Efficiency on Industrial Size." *Proc. 27th European Photovoltaic Solar Energy Conference.* 2012. 576-9.

[260] Würfel, Peter, and Uli Würfel. *Physics of Solar Cells: From Basic Principles to Advanced Concepts.* Weinheim: John Wiley & Sons, 2009.

[261] Yablonovitch, E., T. Gmitter, R. M. Swanson, and Y. H. Kwark. "A 720 mV open circuit voltage SiOx:c-Si:SiOx double heterostructure solar cell." *Applied Physics Letters* 47 (1985): 1211.

[262] Green, M.A., F.D. King, and J. Shewchun. "Minority carrier {MIS} tunnel diodes and their application to electron- and photo-voltaic energy {conversion--I.} Theory." *{Solid-State} Electronics* 17 (1974): 551-561.

[263] Descoeudres, A., Holman, Z. C., Barraud, L., Morel, S., de Wolf, S. and Ballif, C. ">21% Efficient Silicon Heterojunction Solar Cells on n- and p-Type Wafers Compared." *IEEE Journal of Photovoltaics* 3 (2013): 83-89.

[264] Angermann, H., et al. "Optimisation of electronic interface properties of a-Si:H/c-Si hetero-junction solar cells by wet-chemical surface pre-treatment." *Thin Solid Films* 516 (2008): 6775-81.

[265] Stegemann, Bert, et al. "Passivation of Textured Silicon Wafers:Influence of Pyramid Size Distribution, a-Si:H Deposition Temperature, and Post-treatment." *Energy Procedia* 38, no. 0 (2013): 881-889.

[266] Olibet, Sara, et al. "Properties of interfaces in amorphous/crystalline silicon heterojunctions." *physica status solidi (a)* 207, no. 3 (2010): 651-656.

[267] Schulze, T. F., H. N. Beushausen, C. Leendertz, A. Dobrich, B. Rech, and L. Korte. "Interplay of amorphous silicon disorder and hydrogen content with interface defects in amorphous/crystalline silicon heterojunctions." *Applied Physics Letters* (AIP) 96 (2010): 252102.

5922 [268] Schulze, T. F., L. Korte, E. Conrad, M. Schmidt, and B. Rech. "Electrical
5923 transport mechanisms in a-Si:H/c-Si heterojunction solar cells." *J. Appl. Phys.*
5924 107 (2010): 023711.

5925 [269] de Nicolas, S. Martin, D. Munoz, A.S. Ozanne, N. Nguyen, and P.J. Ribeyron.
5926 "Optimisation of doped amorphous silicon layers applied to heterojunction solar
5927 cells." *Energy Procedia* 8, (2011): 226-231.

5928 [270] Schüttauf, J.W.A., C.H.M. van der Werf, W.G.J.H.M. van Sark, J.K. Rath, and
5929 R.E.I. Schropp. "Comparison of surface passivation of crystalline silicon by a-
5930 Si:H with and without atomic hydrogen treatment using Hot-Wire Chemical
5931 Vapor Deposition." *Thin Solid Films* 519 (2011) 4476-4478.

5932 [271] Bahardoust, B., et al. "Passivation study of the amorphous-crystalline silicon
5933 interface formed using DC saddle-field glow discharge." *physica status solidi (a)*
5934 207 (2010): 539-43.

5935 [272] v. Maydell, K., E. Conrad, and M. Schmidt. "Efficient silicon heterojunction solar
5936 cells based on p- and n-type substrates processed at temperatures < 220°C." *Prog.*
5937 *in Photovolt.* 14 (2006): 289-95.

5938 [273] Conrad, E., et al. "Development and Optimization of a-Si:H/c-Si Heterojunction
5939 Solar Cells Completely Processed at Low Temperatures." Edited by a. W.
5940 Hoffmann 21st European Photovoltaic Solar Energy Conference: proceedings of
5941 the international conference held in Dresden, Germany, 4 - 8 September 2006.
5942 Munich, Florence: WIP, ETA, 2006. 784-7.

5943 [274] Korte, L., E. Conrad, H. Angermann, R. Stangl, and M. Schmidt. "Advances in a-
5944 Si:H/c-Si Heterojunction Solar Cell Fabrication and Characterization." *Sol. En.*
5945 *Mat. Sol. Cells* 93 (2009): 905-10.

5946 [275] Street, R. A. *Hydrogenated Amorphous Silicon.* Cambridge University Press,
5947 1991.

5948 [276] Tanaka, K., E. Maruyama, T. Shimada, and H. Okamoto. *Amorphous Silicon.*
5949 John Wiley & Sons, 1999.

5950 [277] Schulze, T. F., H. N. Beushausen, T. Hansmann, L. Korte, and B. Rech.
5951 "Accelerated interface defect removal in amorphous/crystalline silicon
5952 heterostructures using pulsed annealing and microwave heating." *Appl. Phys.*
5953 *Lett.* 95 (2009): 182108.

5954 [278] Descoeudres, A., et al. "Improved amorphous/crystalline silicon interface
5955 passivation by hydrogen plasma treatment." *Applied Physics Letters* 99 (2011):
5956 123506.

5957 [279] Mews, Mathias, Tim F. Schulze, Nicola Mingirulli, and Lars Korte. "Hydrogen
5958 plasma treatments for passivation of amorphous-crystalline silicon-

5959 heterojunctions on surfaces promoting epitaxy." *Applied Physics Letters* 102
5960 (2013): 122106.

5961 [280] Stutzmann, M. "The defect density in amorphous silicon" *Phil. Mag. B* 60 (1989):
5962 531-46.

5963 [281] Powell, M. J., and S. C. Deane. "Improved Defect-Pool Model for Charged
5964 Defects in Amorphous Silicon." *Phys. Rev. B* 48 (1993): 10815-27.

5965 [282] Powell, M. J., and S. C. Deane. "Defect-pool model and the hydrogen density of
5966 states in hydrogenated amorphous silicon." *Phys. Rev. B* 53 (1996): 10121-32.

5967 [283] Steingrube, S., R. Brendel, and P. P. Altermatt. "Limits to model amphoteric
5968 defect recombination via SRH statistics." *physica status solidi (a)* 209 (2012):
5969 390–400.

5970 [284] Leendertz, C., R. Stangl, T. F. Schulze, M. Schmidt, and L. Korte. "A
5971 recombination model for a-{S}i:{H}/c-{S}i heterostructures." *physica status*
5972 *solidi c* 7 (2010): 1005-10.

5973 [285] Olibet, S., E. Vallat-Sauvain, and C. Ballif. "Model for a-Si:H/c-Si interface
5974 recombination based on the amphoteric nature of silicon dangling bonds." *Phys.*
5975 *Rev. B* 76 (2007): 35326.

5976 [286] Schulze, T. F., L. Korte, F. Ruske, and B. Rech. "Band lineup in
5977 amorphous/crystalline silicon heterojunctions and the impact of hydrogen
5978 microstructure and topological disorder." *Phys. Rev. B* 83 (2011): 165314.

5979 [287] Sebastiani, M., L. Di Gaspare, G. Capellini, C. Bittencourt, and F. Evangelisti.
5980 "Low-Energy Yield Spectroscopy as a Novel Technique for Determining Band
5981 Offsets: Application to the c-Si(100)/a-Si:H Heterostructure." *Phys. Rev. Lett.* 75
5982 (1995): 3352-5.

5983 [288] Korte, L., and M. Schmidt. "Doping type and thickness dependence of band
5984 offsets at the amorphous/crystalline silicon heterojunction." *Journal of Applied*
5985 *Physics* 109 (2011): 063714-1--6.

5986 [289] Korte, L., T. F. Schulze, C. Leendertz, M. Schmidt, and B. Rech. "Band
5987 alignment at amorphous/crystalline silicon hetero-interfaces." *MRS Symp Proc.*
5988 2011. mrss11-1321-a15-03 (6 pages).

5989 [290] de Wolf, S, C Ballif, and M Kondo. "Kinetics of a-Si:H bulk defect and a-Si:H/c-
5990 Si interface-state reduction." *Phys. Rev. B* 85 (2012): 113302.

5991 [291] Schulze, T.F., C. Leendertz, N. Mingirulli, L. Korte, and B. Rech. "Impact of
5992 Fermi-level dependent defect equilibration on Voc of amorphous/crystalline
5993 silicon heterojunction solar cells." *Energy Procedia* 8 (2011): 282-287.

5994 [292] Holman, Z.C., et al. "Current Losses at the Front of Silicon Heterojunction Solar
5995 Cells." *Photovoltaics, IEEE Journal of* 2, no. 1 (jan. 2012): 7-15.

5996 [293] L. Korte, L. and Schmidt, M. “Investigation of gap states in phosphorous-doped
5997 ultra-thin a-Si:H by near-UV photoelectron spectroscopy.” *J. Non-Cryst. Sol.* 354
5998 (2008): 2138-43

5999 [294] de Wolf, Stefaan, and Michio Kondo. "Nature of doped a-Si:H/c-Si interface
6000 recombination." *Journal of Applied Physics* 105 (2009): 103707.

6001 [295] Barraud, L., et al. "Hydrogen-doped indium oxide/indium tin oxide bilayers for
6002 high-efficiency silicon heterojunction solar cells." *Solar Energy Materials and*
6003 *Solar Cells* 115 (2013): 151-6.

6004 [296] Kobayashi, E., N. Nakamura, and Y. Watabe. "Reduction of Optical and
6005 Electrical Losses in Silicon Heterojunction Solar Cells by Hydrogenated
6006 Tungsten-Doped In2O3 ." *Proc. 27th European Photovoltaic Solar Energy*
6007 *Conference.* 2012. 1619-1623.

6008 [297] Ruske, Florian. "Deposition and Properties of TCOs." Chap. 9 in *Physics and*
6009 *Technology of Amorphous-Crystalline Heterostructure Silicon Solar Cells*, edited
6010 by Wilfried G.J.H.M. Sark, Lars Korte, & Francesco Roca, 301-330. Berlin,
6011 Heidelberg: Springer, 2011.

6012 [298] Holman, Zachary C, et al. "Infrared light management in high-efficiency silicon
6013 heterojunction and rear-passivated solar cells." *Journal of Applied Physics* (AIP)
6014 113, no. 1 (2013): 13107-13107.

6015 [299] Rößler, R., C. Leendertz, L. Korte, N. Mingirulli, and B. Rech. "Impact of the
6016 transparent conductive oxide work function on injection-dependent a-Si:H/c-Si
6017 band bending and solar cell parameters." *Journal of Applied Physics* 113 (2013):
6018 144513.

6019 [300] Froitzheim, A., K. Brendel, L. Elstner, W. Fuhs, K. Kliefoth, and M. Schmidt.
6020 "Interface recombination in heterojunctions of amorphous and crystalline
6021 silicon." *J. Non-Cryst. Sol.* 299-302 (2002): 663-7.

6022 [301] van Cleef, M.W.M., et al. "Photocarrier collection in a-SiC : H/c-Si
6023 heterojunction solar cells." *Journal Of Non-crystalline Solids* 227 (1998): 1291-
6024 1294.

6025 [302] Kanevce, Ana, and Wyatt K. Metzger. "The role of amorphous silicon and
6026 tunneling in heterojunction with intrinsic thin layer {(HIT)} solar cells." *Journal*
6027 *of Applied Physics* 105, no. 9 (#may# 2009): 94507-7.

6028 [303] Rößler, R., L. Korte, C. Leendertz, N. Mingirulli, M. El Mhamdi, and B. Rech.
6029 "ZnO:Al/(p)a-Si:H Contact Formation and Its Influence on Charge Carrier
6030 Lifetime Measurements." Edited by G. Willeke, H. Ossenbrink, & P. Helm. *Proc.*

6031 *27th European Photovoltaic Solar Energy Conference and Exhibition.* Munich:
6032 WIP Munich, 2012. 1443-1447.

6033 [304] Taguchi, Mikio, Eiji Maruyama, and Makoto Tanaka. "Temperature Dependence
6034 of Amorphous/Crystalline Silicon Heterojunction Solar Cells." *Japanese Journal*
6035 *of Applied Physics* 47 (2008): 814-818.

6036 [305] Schulze, T. F., L. Korte, E. Conrad, M. Schmidt, and B. Rech. "High-forward-
6037 bias transport mechanism in a-Si:H/c-Si heterojunction solar cells." *phys. stat.*
6038 *sol. a* 207 (2010): 657–60.

6039 [306] Datta, A., M. Rahmouni, M. Nath, R. Boubekri, P. Roca i Cabarrocas, and P.
6040 Chatterjee. "Insights gained from computer modeling of heterojunction with
6041 instrinsic thin layer "HIT" solar cells." *Solar Energy Materials and Solar Cells*
6042 94, (2010): 1457-1462.

6043 [307] Tiedje, T., W. Yablonovitch, G. D. Cody, and B. G. Brooks. *IEEE Trans.*
6044 *Electron Dev.* 31 (1984): 711.

6045 [308] Bätzner, D., et al. "Characterisation of Over 21% Efficient Silicon Heterojunction
6046 Cells Developed at Roth & Rau Switzerland ." *Proc. 26th European Photovoltaic*
6047 *Solar Energy Conference.* 2011. 1073-1075.

6048 [309] Watabe, Y.; Yamamoto, T. & Yamada, Y. Cerium oxide and hydrogen co-doped
6049 indium oxide films for high-efficiency silicon heterojunction solar cells. Solar
6050 Energy Materials and Solar Cells, 2016, 149, 75–80

6051 [310] Papet, P., et al. "Module Integration for High Efficient Heterojunction Solar
6052 Cells." *Proc. 27th European Photovoltaic Solar Energy Conference.* 2012. 3541-
6053 3545.

6054 [311] Bivour, M., Reichel, C., Hermle, M., and Glunz, S.W. "Improving the a-Si:H(p)
6055 rear emitter contact of n-type silicon solar cells." *Solar Energy Materials and*
6056 *Solar Cells* 106 (2012): 11-16.

6057 [312] Hekmatshoar, Bahman, Davood Shahrjerdi, Marinus Hopstaken, John A. Ott, and
6058 Devendra K. Sadana. "Characterization of thin epitaxial emitters for high-
6059 efficiency silicon heterojunction solar cells." *Appl. Phys. Lett.* 101 (2012)
6060 103906.

6061 [313] J. Govaerts, S. N. Granata, T. Bearda, F. Dross, C. Boulord, G. Beaucarne, F.
6062 Korsos, K. Baert, I. Gordon and J. Poortmans. Development of a-Si:H/c-Si
6063 heterojunctions for the i^2-module concept: Low-temperature passivation and
6064 emitter formation on wafers bonded to glass. Solar Energy Materials and Solar
6065 Cells **113**, 52-60 (2013)

6066 [314] Haschke, J. and Jogschies, L. and Amkreutz, D. and Korte, L. and Rech, B.
6067 "Polycrystalline silicon heterojunction thin-film solar cells on glass exhibiting

6068 582mV open-circuit voltage." *Solar Energy Materials & Solar Cells* 115 (2013):
6069 7-10.

6070 [315] Mailoa, J. P.; Bailie, C. D.; Johlin, E. C.; Hoke, E. T.; Akey, A. J.; Nguyen, W.
6071 H.; McGehee, M. D.; Buonassisi, T. Applied Physics Letters 2015, 106, 121105.

6072 [316] Werner, J.; Weng, C.-H.; Walter, A.; Fesquet, L.; Seif, J. P.; De Wolf, S.; Niesen,
6073 B.; Ballif, C. The Journal of Physical Chemistry Letters 2015, 161.

6074 [317] Albrecht, S.; Saliba, M.; Correa Baena, J. P.; Lang, F.; Kegelmann, L.; Mews,
6075 M.;Steier, L.; Abate, A.; Rappich, J.; Korte, L.; Schlatmann, R.; Nazeeruddin, M.
6076 K.; Hagfeldt, A.; Grätzel, M.; Rech, B. Energy Environ. Sci. 2016, 9, 81.

6077 [318] Loper, P.; Moon, S.-J.; Martin de Nicolas, S.; Niesen, B.; Ledinsky, M.; Nicolay,
6078 S.; Bailat, J.; Yum, J.-H.; De Wolf, S.; Ballif, C. Physical Chemistry Chemical
6079 Physics 2015, 17, 1619.

6080 [319] Bailie, C. D.; Christoforo, M. G.; Mailoa, J. P.; Bowring, A. R.; Unger, E. L.;
6081 Nguyen, W. H.; Burschka, J.; Pellet, N.; Lee, J. Z.; Gratzel, M.; Noufi, R.;
6082 Buonassisi, T.; Salleo, A.; McGehee, M. D. Energy & Environmental Science
6083 2015, 8, 956

6084 [320] Werner, J.; Dubuis, G.; Walter, A.; Löper, P.; Moon, S.-J.; Nicolay, S.; Morales-
6085 Masis, M.; De Wolf, S.; Niesen, B.; Ballif, C. Solar Energy Materials and Solar
6086 Cells 2015, 141, 407

6087 [321] Lang, F.; Gluba, M. A.; Albrecht, S.; Rappich, J.; Korte, L.; Rech, B.; Nickel, N.
6088 H. J Phys Chem Lett 2015, 6, 2745

6089 [322] McMeekin, D. P.; Sadoughi, G.; Rehman, W.; Eperon, G. E.; Saliba, M.;
6090 Hörantner, M. T.; Haghighirad, A.; Sakai, N.; Korte, L.; Rech, B.; Johnston, M.
6091 B.; Herz, L. M.; Snaith, H. J. Science 2016, 351, 151.

6092 [323] Aberle AG, Altermatt PP, Heiser G, Robinson SJ, Wang A, Zhao J, Krumbein
6093 U, Green MA. Limiting loss mechanisms in 23% efficient silicon solar cells. J
6094 Appl Phys 1995;77:3491-04.

6095 [324] Sakata H, Tsunomura Y, Inoue H, Taira S, Baba T, Kanno H, et al. R&D
6096 Progress of Next-Generation Very Thin HITtm Solar Cells. Proc of 25th
6097 EUPVSEC Valencia (Spain) 2010;1102-6.

6098 [325] Yano A, Tohoda S, Matsuyama K, Nakamura Y, Nishiwaki T , Fujita K, Taguchi
6099 M, Maruyama E. 24.7% Record Efficiency HIT® Solar Cell on Thin Silicon
6100 Wafer. Proc of 28th EUPVSEC Paris (France) 2013;748-51

6101 [326] Staebler DL, Wronski CR. Reversible conductivity changes in discharge
6102 produced amorphous Si, Appl Phys Lett 1997;31:292-4.

6103 [327] Taguchi M, Kawamoto K, Tsuge S, Baba T, Sakata H, Morizane M, et al. HIT
6104 (TM) cells - High-efficiency crystalline Si cells with novel structure. Prog
6105 Phototovolt Res. Appl 2000;8:503-13.

6106 [328] Mulligan WP, Carandang MA, Dawson M, De Ceuster DM, Stone CN, Swanson
6107 RM. Reducing silicon consumption by leveraging cell efficiency. Proc of 21st
6108 EUPVSEC Dresden (Germany) 2006;1301-04.

6109 [329] Diouf D, Kleider JP, Desrues T, Rideyron PJ. Study of interdigitated back contact
6110 silicon heterojunction solar cells by two-dimensional numerical simulations. Mat
6111 Sci Eng B 2009;159-160:291-4.

6112 [330] Lu M, Bowden S, Das U, Birkmire R. Interdigitated back contact silicon
6113 heterojunction solar cells and the effect of front surface passivation. Appl Phys
6114 Lett 2007;91:063507.

6115 [331] Lu M, Das U, Bowden S, Birkmire R. Rear surface passivation of interdigitated
6116 back contact silicon heterojunction solar cell and 2D simulation study. Proc of
6117 33th IEEE PVSC San Diego (USA) 2008;11-5.

6118 [332] Tucci M, Serenelli L, Salza E, Rattè M, De Iuliis S, Geerligs LJ, et al. Innovative
6119 design of amorphous/crystalline silicon heterojunction solar cell. Thin Solid
6120 Films 2008;516:6771-4.

6121 [333] Tucci M, Serenelli L, Salza E, Pirozzi L, de Cesare G, Caputo D, et al. BEHIND
6122 (Back Enhanced Heterostructure with INterDigitated contact) solar cell. Proc.
6123 23rd EUPVEC Valencia (Spain) 2008;1749-52.

6124 [334] Tucci M, Serenelli L, Martufi P, Salza E, De Iuliis S, Geerlig LJ, de Cesare G,
6125 Caputo D, Ceccarelli M. Back enhanced heterostructure with interdigitated
6126 contact – BEHIND - solar cell, Proc of IEEE COMMAD 2008; 242-5.

6127 [335] Tucci M and Serenelli L. Metastability of SiNx / a-Si:H crystalline silicon
6128 surface passivation for PV application. Thin Solid Films 2008;516:6939-42.

6129 [336] Caputo D, de Cesare G, Ceccarelli M, Nascetti A, Tucci M, Meda L, Losurdo M,
6130 Bruno G. Characterization of chromium silicide thin layer formed on amorphous
6131 silicon films. J Non-Cryst Solids 2008;354:2171-5.

6132 [337] Cecchetto L, Serenelli L, Agarwal G, Izzi M, Salza E, Tucci M. Highly textured
6133 multi-crystalline silicon surface obtained by dry etching multi-step process. Sol
6134 En Mat Sol Cells 2013;116:283-90.

6135 [338] Tucci M, De Iuliis S, Serenelli L, Izzi M, Salza E, De Luca V, Velardi F
6136 Sanseverino N, de Cesare G, Caputo D. Behind 2.0: The Back Enhanced
6137 Heterostructure with Interdigitated Contact Solar Cell Evolution. Proc of 25st
6138 EUPVSEC Valencia (Spain) 2010;2089-92.

6139 [339] Desrues T, Martín I, De Vecchi S, Abolmasov S, Diouf D, Lukyanov A, et al.
6140 Silicon Heterojunction for Advanced Rear Contact Cells: Main Results of the
6141 SHARCC Project. Proc of 28th EUPVSEC Paris (France) 2013;1135-8.

6142 [340] O'Sullivan BJ, Bearda T, Qiu Y, Robbelein J, Gong C, Posthuma NE, Gordon I,
6143 Poortmans J. Interdigitated rear contact solar cells with amorphous silicon
6144 heterojunction emitter. Proc of 35th IEEE PVSEC Honolulu (USA) 2010;3549-52.

6145 [341] Hertanto A, Liu H, Yeghikyan D, Rayaprol BG, Kherani NP, Zukotynski S. Back
6146 Amorphous Crystalline silicon Heterojunction (BACH) photovoltaic device. Proc
6147 of 34th IEEE PVSC Philadelphia (USA) 2009;1767-70.

6148 [342] Chowdhury ZR and Kherani NP. Back amorphous-crystalline silicon
6149 heterojunction (BACH) photovoltaic device with facile-grown, oxide - PECVD
6150 SiNx passivation. Prog Photovolt Res Appl 2014;23:821-8.

6151 [343] LG Electronics Oral Presentation at 27th EUPVSEC Conference Paris 2013.

6152 [344] http://www.pv-tech.org/news/back_contact_hit_solar_cell_from_
6153 panasonic_pushes_efficiency_record_to_25.6

6154 [345] Mac Donald D, Rougieux F, Cuevas A, Lim B, Schmidt J, Di Sabatino M,
6155 Geerligs, LJ. Light-induced boron-oxygen defect generation in compensated p-
6156 type Czochralski silicon. J Appl Phys 2009;105:093704.

6157 [346] Tucci M, Serenelli L, De Iuliis S, Izzi M, de Cesare G, Caputo D. Contact
6158 Formation on a-Si:H/c-Si Heterostructure Solar Cells. Physics and Technology of
6159 Armophous-Crystalline: Springer Ed 2011;321-75.

6160 [347] Tucci M, Serenelli L, De Iuliis S, Izzi M, de Cesare G, Caputo D. Back contact
6161 formation for p-type based a-Si:H/c-Si heterojunction solar cells. Physica Status
6162 Solidi C. 2011;8(3):932-5.

6163 [348] Tucci M, della Noce M, Bobeico E, Roca F, de Cesare G, Palma F. Comparison
6164 of amorphous / crystalline heterojunction solar cells based on n and p type
6165 crystalline silicon. Thin solid Films 2004;451:355-359.

6166 [349] Diouf D, Kleider JP, Desrues T, Ribeyron PJ. Interdigitated Back Contact a-
6167 Si:H/c-Si Heterojunction Solar Cells Modelling: Limiting Parameters Influence
6168 on Device Efficiency. Proc of 23rd EUPVSEC Valencia (Spain) 2008;1949-52.

6169 [350] Caputo D, de Cesare G, Palma F, Tucci M, Minarini C, Terzini E. Investigation
6170 of amorphous silicon compensated materials over a wide range of dopant
6171 concentration. Thin Solid Films 1997;303:269-72.

6172 [351] Brodsky MH, Evangelisti F, Fischer R, Johnson RW, Reuter W, Solomon I.
6173 Thickness-dependent conductivity and photoconductivity of hydrogenated
6174 amorphous silicon. Solar Cells 1980;2:401-6.

6175 [352] Lu M., Das U, Bowden S, Hegedus S, Birkmire R. Optimization of interdigitated
6176 back contact silicon heterojunction solar cells: tailoring hetero-interface band
6177 structure while maintaining surface passivation. Prog in Photovolt: Res Appl
6178 2011;19:326-38.

6179 [353] Tucci M. Optimization of n-doping in n-type a-Si:H / p-type textured c-Si
6180 heterojunction for photovoltaic applications. Sol En Mat Sol Cells 1999;57:249-
6181 57.

6182 [354] Fujiwara H, Kondo M. Real-time monitoring and process control in
6183 amorphous/crystalline silicon heterojunction solar cells by spectroscopic
6184 ellipsometry and infrared spectroscopy. Appl Phys Lett 2005;86:032112.

6185 [355] Tucci M, Martini L, Serenelli L, Izzi M, Caputo D, Asquini R, de Cesare G.
6186 Effect of Hydrogen in a-Si:H/c-Si Heterojunction. Proc of 28th EUPVSEC Paris
6187 (France) 2013; 1971-5.

6188 [356] de Cesare G, Caputo D, Tucci M. Electrical properties of ITO/crystalline-silicon
6189 contact at different deposition temperatures. IEEE El Dev Lett 2012;33:327-9.

6190 [357] Sato Y, Ashida T, Oka N, Shigesato . Carrier Density Dependence of Optical
6191 Band Gap and Work Function in Sn-Doped In_2O_3Films. Appl Phys Expr
6192 2010;3:061101.

6193 [358] http://www.esrf.eu/computing/scientific/xop2.1/

6194 [359] Reichel C, Granek F, Hermle M, Glunz S. Investigation of electrical shading
6195 effects in back-contacted back-junction silicon solar cells using the two
6196 dimensional charge collection probability and the reciprocity theorem. J Appl
6197 Phys 2011;109:024507.

6198 [360] Diouf D, Kleider JP, Desrues T, Ribeyron JP. Effects of the front surface field in
6199 n-type interdigitated back contact silicon heterojunction solar cells. Energy
6200 Procedia 2010;2:59-64.

6201 [361] Engelhart P, Harder NP, Grischke R, Merkle A, Meyer R, Brendel R. Laser
6202 Structuring for Back Junction Silicon Solar Cells. Prog in Photov: Res and Appl
6203 2006;15(3):237-43.

6204 [362] Tucci M, Serenelli L, De Iuliis S, Izzi M. Characterization of SiNx/a-Si:H
6205 crystalline silicon surface passivation under UV light exposure. Thin Solid Films
6206 2007;515:7625-8.

6207 [363] Feldmann F, Bivour M, Reichel C, Hermle M, Glunz SW. Passivated rear
6208 contacts for high-efficiency n-type Si solar cells providing high interface
6209 passivation quality and excellent transport characteristics. Sol En Mat Sol Cel
6210 2014;120A:270-4.

6211 [364] Izzi M, Tucci M, Serenelli L, Mangiapane P, Della Noce M, Usatii I, Esposito E,
6212 Mercaldo LV, Delli Veneri P. Doped SiOx emitter layer in amorphous/crystalline
6213 silicon heterojunction solar cell. Appl Phys A 2014;115:705-12.

6214 [365] PC1D version 5.3 P.A. Basore, D.A. Clugston. University of New South Wales
6215 (1998).

6216 [366] Green MA, Emery K, Hishikawa Y, Warta W. Solar cell efficiency tables
6217 (version 37). Prog Photovolt: Res Appl 2011;19:84-92.

6218 [367] Taira S, Yoshimine Y, Baba T, Taguchi M, Kanno M, Kinoshita H, et al. Our
6219 approach for Achieving HIT Solar Cells with More Than 23% Efficiency. Proc of
6220 22nd EUPVSEC Milan (Italy) 2007;932-5.

6221 [368] International Technology Roadmap for Photovoltaics (ITRPV) Edition March
6222 2013.

6223 [369] Balucani M, Kholostov K, Nenzi P, Crescenzi R, Ciarniello D, Bernardi D
6224 Serenelli L, Izzi M, Tucci M. New selective processing technique for solar cells.
6225 Energy Procedia 2013;43:54-65.

6226 [370] Horzel J, Bay N, Knarozovskiy T, Träger A, Passig M, Burschik J, et al. Different
6227 Concepts of Implementing a Directly Plated Front Side Metallization into
6228 Industrial Solar Cell Mass Production. Proc of 28th EUPVSEC Paris (France)
6229 2013;1374-9.

6230 [371] Martí A, Araújo GL. Limiting efficiencies for photovoltaic energy conversion in
6231 multigap systems. Solar Energy Materials and Solar Cells 1996;43(2):203-22.

6232 [372] King RR, Boca A, Hong W, Liu X-Q, Bhusari D, Larrabee D, et al. Band-Gap-
6233 Engineered Architectures for High-Efficiency Multijunction Concentrator Solar Cells.
6234 In: 24th European Photovoltaic Solar Energy Conference (EU PVSEC); 2009.

6235 [373] Lide DR. CRC Handbook of Chemistry and Physics Vol. 85th. Florida: T.F. Group;
6236 2005.

6237 [374] Bolkhovityanov YB, Pchelyakov OP. III-V Compounds-on-Si: Heterostructure
6238 fabrication, application and prospects. The Open Nanoscience Journal 2009:3:20-33.

6239 [375] Wanlass M.W, Coutts TI, Ward S, Emery KA, Gessert TA, Osterwald CR. Advanced
6240 high-efficiency concentrator tandem solar cells. In: Photovoltaic Specialists
6241 Conference; 1991.

6242 [376] Ayers JE. Heteroepitaxy of semiconductors. Theory,growth and characterization. New
6243 York: CRC Press; 2007.

6244 [377] Hayashi K, Soga T, Nishikawa H, Jimbo T, Umeno, M. MOCVD growth of GaAsP
6245 on Si for tandem solar cell application. In: Proceedings of the 24th IEEE
6246 Photovoltaics Specialist Conference; 1994.

6247 [378] Lee J-W, Salzman J, Emerson D, Shealy JR, Ballantyne JM. Selective area growth of
6248 GaP on Si by MOCVD. Journal of Crystal Growth 1997;172(1-2):53-7.

6249 [379] Suzuki T, Soga T, Jimbo T, Umeno M. Growth mechanism of GaP on Si substrate by
6250 MOVPE. Journal of Crystal Growth 1991;115(1-4):158-63.

6251 [380] Umeno M, Soga T, Baskar K, Jimbo T. Heteroepitaxial technologies on Si for high-
6252 efficiency solar cells. Solar Energy Materials and Solar Cells 1998;50(1-4):203-12.

6253 [381] Geisz J, Olson JM, Friedman DJ. Toward a monolithic lattice-matched III-V on
6254 silicon tandem solar cell. In: 19th European PV Solar Energy Conference and Exhibit;
6255 2004.

6256 [382] Yonezu H. Control of structural defects in group III-V-N alloys grown on Si.
6257 Semiconductor Science and Technology 2002;17(8):762-8.

6258 [383] Andre CL, Carlin JA, Boeckl JJ, Wilt DM, Smith MA, Pitera AJ et al. Investigations
6259 of high-performance GaAs solar cells grown on Ge-Si1-xGex-Si substrates. IEEE
6260 Transactions on Electron Devices 2005;52(6):1055-60.
6261
6262 [384] Grassman TJ, Brenner MR, Gonzalez M, Carlin AM, Unocic RR, Dehoff RR, et al.
6263 Characterization of metamorphic GaAsP/Si materials and devices for photovoltaic
6264 applications. IEEE Transactions on Electron Devices 2010;57(12):3361-9.

6265 [385] Lang JR, Faucher J, Tomasulo S, Yaung KN, Lee ML. GaAsP solar cells on GaP/Si
6266 grown by molecular beam epitaxy. In; IEEE 39th Photovoltaic Specialists Conference
6267 (PVSC); 2013.

6268 [386] Ringel SA, Andre CL, Fitzgerald EA, Pitera AJ, Wilt DM. Multi-junction III-V
6269 photovoltaics on lattice-engineered Si substrates. In: Photovoltaic Specialists
6270 Conference; 2005.

6271 [387] Roesener T, Döscher H, Beyer A, Brückner S, Klinger V, Wekkeli A, et al. MOVPE
6272 growth of III-V solar cells on silicon in 300mm closed coupled showerhead reactor.
6273 In: 25th European Photovoltaic Solar Energy Conf. and Exhibition; 2010.

6274 [388] Soga T, Jimbo T, Umeno M. Epitaxial growth of a two-dimensional structure of GaP
6275 on a Si substrate by metalorganic chemical vapor deposition. Applied Surface Science
6276 1994;82-83(0):64 -9.

6277 [389] Takagi Y, Yonezu H, Samonji K, Tsuji T, Ohshima N. Generation and suppression
6278 process of crystalline defects in GaP layers grown on misoriented Si (100) substrates.
6279 Journal of Crystal Growth 1998;187(1):42-50.

6280 [390] Geisz JF, Olson JM, Romero MJ, Jiang C-S, Norman AG. Lattice-mismatched GaAsP
6281 solar cells grown on silicon by OMVPE. In: IEEE 4th World Conference on
6282 Photovoltaic Energy Conversion; 2006.

6283 [391] Ringel SA, Carlen JA, Andre CL, Hudait MK, Gonzalez M, Wilt DM, et al. Single-
6284 junction InGaP/GaAs solar cells grown on Si substrates with SiGe buffer layers.
6285 Progress in Photovoltaics: Research and Applications 2002;10(6):417-26.

6286 [392] Schöne J, Dimroth F, Bett AW, Tauzin A, Jaussaud C, Roussin JC. III-V solar cell
6287 growth on wafer-bonded GaAs/Si-substrates. In: IEEE 4th World Conference on
6288 Photovoltaic Energy Conversion; 2006.

6289 [393] Tanabe K, Watanebe K, Arakawa Y. III-V/Si hybrid photonic devices by direct fusion
6290 bonding. Sci. Rep. 2012;2:3491-6.

6291 [394] Woo HJ, Choi HW, Kim GD, Kim JK. Fabrication of GaAs on Si heterostructures by
6292 helium implantation and direct wafer bonding. Journal of the Korean Physical Society
6293 2009;54(5):2060-5.
6294 [395] King RR, Law DC, Edmondson KM, Fetzer CM, Kinsey GS, Yoon H, et al.
6295 Advances in high-efficiency III-V multijunction solar cells. Advances in
6296 OptoElectronics 2007;2007:1-8.

6297 [396] Okada Y, Shimomura H, Kawabe M. Low dislocation density GaAs on Si
6298 heteroepitaxy with atomic hydrogen irradiation for optoelectronic integration. Journal
6299 of Applied Physics 1993;73(11):7376-84.

6300 [397] Fang SF, Adomi K, Iyer S, Morkoç H, Zabel H, Choi C, Otsuka N. Gallium arsenide
6301 and other compound semiconductors on silicon. Journal of Applied Physics
6302 1990;68(7):R31-R58.

6303 [398] Lee JW, Shichijo H, Tsai HL, Matyi RJ. Defect reduction by thermal annealing of
6304 GaAs layers grown by molecular beam epitaxy on Si substrates. Applied Physics
6305 Letters 1987;50(1): 31-33.

6306 [399] Tachikawa M, Mori H, Sugo M, Itoh Y. Continuous GaAs film growth on epitaxial Si
6307 surface in initial stage of GaAs/Si heteroepitaxy. Japanese Journal of Applied Physics
6308 1993;32(Part 2, No. 9A):L1252-5.

6309 [400] Yamaguchi M, Nishioka T, Sugo M. Analysis of strained-layer superlattice effects on
6310 dislocation density reduction in GaAs on Si substrates. Applied Physics Letters
6311 1989;54(1):24-6.

6312 [401] Doscher H, Hannappel T, Kunert B, Beyer A, Volz K, Stolz W. In situ verification of
6313 single-domain III-V on Si(100) growth via metal-organic vapor phase epitaxy.
6314 Applied Physics Letters 2008;93(17):1721101-3.

6315 [402] Vinokurov DA, Lantratov VM, Sinitsyn MA, Ulin VP, Faleev NN; Fedorova OM, et
6316 al. Properties and special features of crystallization of epitaxial GaAs films grown on
6317 Si (100) substrates by the method of 2-stage deposition using the MOCVD hydride
6318 process. Sovietic physics: Semiconductors 1991;25:617-21.

[403] Soga T, Kawai M, Otsuka K, Jimbo T, Umeno M. In Proceedings of the 2nd World Conference on Photovoltaic Solar Energy Conversion; 1998.

[404] Wang G, Zhao GY, Soga T, Jimbo T, Umeno M. Effects of H plasma passivation on the optical and electrical properties of GaAs-on-Si. Japanese Journal of Applied Physics 1998;37(11A):L1280-2.

[405] Venkatasubramanian R, Posthill J, Timmons ML, Ahrenkiel R. Aspects of "High Minority-Carrier Lifetime" GaAs on Si Using A Novel SiGe/Ge Buffer. MRS Proceedings 1991; 221.

[406] Ginige R, Corbett B, Modreanu M, von Kaenel H. Characterization of Ge-on-Si virtual substrates and single junction GaAs solar cells. Semiconductor Science and Technology 2006;21(6):775-80.

[407] Carlin JA, Ringel SA, Fitzgerald A, Bulsara M. High-lifetime GaAs on Si using GeSi buffers and its potential for space photovoltaics. Solar Energy Materials and Solar Cells 2001;66(1–4):621-30.

[408] Chriqui Y, Largeau L, Patriarche G, Kermarrec LO. Direct growth of GaAs-based structures on exactly (0,0,1)-oriented Ge/Si virtual substrates: reduction of the structural defect density and observation of electroluminescence at room temperature under CW electrical injection. Journal of Crystal Growth 2004; 265(1–2):53-9.

[409] Carlin JA, Ringel SA, Fitzgerald EA, Bulsara M, Keyes BM. Impact of GaAs buffer thickness on electronic quality of GaAs grown on graded Ge/GeSi/Si substrates. Applied Physics Letters 2000;76(14):1884-6.

[410] Lueck MR, Andre CL, Pitera AJ, Lee ML, Fitzgerald EA, Ringel SA. Dual junction GaInP/GaAs solar cells grown on metamorphic SiGe/Si substrates with high open circuit voltage. Electron Device Letters, IEEE 2006;27(3):142-4.

[411] Carlin AM, Fitzgerald EA, Ringel SA. III-V/SiGe on Si Radiation Hard Space Cells with Voc>2.6V. In: 42nd IEEE PV Specialist Conf.; 2015.

[412] Wang L, Conrad B, Soeriyadi A, Diaz M, Xin Zhao ; Dun Li et al. Current matched GaAsP/SiGe tandem device on Si over 20% efficiency under indoor measurement. In: 42nd IEEE PV Specialist Conf.; 2015.

[413] Ernst F, Pirouz P. Formation of planar defects in the epitaxial growth of GaP on Si substrate by metal organic chemical-vapor deposition. Journal of Applied Physics 1988;64(9):4526-30.

[414] Narayanan V, Sukidi N, Bachmann KJ, Mahajan S. Origins of defects in self assembled GaP islands grown on Si (001) and Si(111). Thin Solid Films 1999;357(1):53-6.

6354 [415] Dixit VK, Ganguli T, Sharma TK, Kumar R, Porwal S, Shukla V, et al. Studies on
6355 MOVPE growth of GaP epitaxial layer on Si (001) substrate and effects of annealing.
6356 Journal of Crystal Growth 2006;293(1):5-13.

6357 [416] Döscher H, Brückner S, Dobrich A, Höhn C, Kleinschmidt P, Hannappel T. Surface
6358 preparation of Si (100) by thermal oxide removal in a chemical vapor environment.
6359 Journal of Crystal Growth 2011;315(1):10-5.

6360 [417] Kohama Y, Uchida K, Soga T, Jimbo T, Umeno M. Quality improvement of
6361 metalorganic chemical vapor deposition grown GaP on Si by AsH_3 preflow. Applied
6362 Physics Letters 1988;53(10):862-4.

6363 [418] Soga T, Jimbo T, Umeno M. Initial stage of GaPSi heteroepitaxial growth by
6364 metalorganic chemical vapor deposition. Journal of Crystal Growth 1996;163(1-
6365 2):165-70.

6366 [419] Grassman TJ, Brenner MR, Rajagopalan S, Unocic R, Dehoff R, Mills M et al.
6367 Control and elimination of nucleation-related defects in GaP/Si(001) heteroepitaxy.
6368 Applied Physics Letters 2009;94(23):2321061-3

6369 [420] Soga T, Suzuki b, M. Mori b, T. Jimbo b, M. Umeno b Suzuki T, Mori M, Jimbo T,
6370 Umeno M. The effects of the growth parameters on the initial stage of epitaxial
6371 growth of GaP on Si by metalorganic chemical vapor deposition. Journal of Crystal
6372 Growth 1993;132(1–2):134-40.

6373 [421] Yamane K, Kawai T, Furukawa Y, Okada H, Wakahara A. Growth of low defect
6374 density GaP layers on Si substrates within the critical thickness by optimized shutter
6375 sequence and post-growth annealing. Journal of Crystal Growth 2010;312(15):2179-
6376 84.

6377 [422] Németh I, Kunert B, Stolz W, Volz K. Heteroepitaxy of GaP on Si: Correlation of
6378 morphology, anti-phase-domain structure and MOVPE growth conditions. Journal of
6379 Crystal Growth 2008;310(7-9):1595-601.

6380 [423] Volz K, Beyer A, Witte W, Ohlmann J, Németh I, Kunert B, Stolz W. GaP-nucleation
6381 on exact Si (001) substrates for III/V device integration. Journal of Crystal Growth
6382 2011;315(1):37-47.

6383 [424] Takano Y, Takagi T, Matsuo Y, Fuke S. Surface evolution of GaP grown on Si
6384 substrates using metalorganic vapor phase epitaxy. Japanese Journal of Applied
6385 Physics 2010;49(3R):0355021-5.

6386 [425] Grassman TJ, Chmielewski DJ, Carnevale SD, Carlin JA, Ringel SA. Progress in the
6387 Development of Epitaxial GaAsP/Si Dual-Junction Solar Cells. In: 42nd IEEE PV
6388 Specialist Conf.; 2015.

6389 [426] Chmielewski DJ, Grassman TJ, Carlin AM, Carlin JA, Speelman A, Ringel SA. High-
6390 Performance Metamorphic Tunnel Junctions on Si for III‐V/Si Multijunction Solar
6391 Cells. In: 42nd IEEE PV Specialist Conf.; 2015.

6392 [427] Grassman TJ, Carlin JA, Ratcliff C, Chmielewski DJ, Ringel SA.. Epitaxially-grown
6393 metamorphic GaAsP/Si dual-junction solar cells. In: 39th IEEE PV Specialist Conf.;
6394 2013

6395 [428] García-Tabarés E, Martin D, Garcia I, Rey-Stolle I. Optimization of the silicon
6396 subcell for III-V on silicon multijunction solar cells: Key differences with
6397 conventional silicon technology. AIP Conference Proceedings 2012;1477(1):5-9.

6398 [429] Chmielewski DJ, Grassman TJ, Carlin AM, Carlin JA, Speelman A, Ringel SA..
6399 Metamorphic tunnel junctions for high efficiency III-V/IV multi-junction solar cell
6400 technology. In: Photovoltaic Specialists Conference (PVSC); 2013.

6401 [430] Bhusal L, Zhu W, Freundlich A. Dilute nitride III-V superlattices lattice-matched to
6402 silicon. In: IEEE 4th World Conference on Photovoltaic Energy Conversion; 2006.

6403 [431] Geisz JF, Olson JM, Friedman DJ, Jones KM, Reedy RC, Romero MJ. Lattice-
6404 matched GaNPAs-on-silicon tandem solar cells. In: Photovoltaic Specialists
6405 Conference; 2005.

6406 [432] Dawson D. History of Tribology. London: Longman Group Limited; 1979.

6407 [433] Tong QY. Low temperature wafer direct bonding. Microelectromech. Syst. 1994;3:7.

6408 [434] Howlader MMR, Watanabe T, Suga T. Investigation of the bonding strength and
6409 interface current of p-Si/n-GaAs wafers bonded by surface activated bonding at room
6410 temperature. Journal of Vacuum Science & Technology B: Microelectronics and
6411 Nanometer Structures 2001;19(6):2114-8.

6412 [435] Zhou YC, Zhu ZH, Crouse D, Lo YH. Electrical properties of wafer-bonded GaAs/Si
6413 heterojunctions. Applied Physics Letters 1998;73:2337.

6414 [436] Hayashi K, Bruno D, Goorsky MS. Temperature dependence of hydrogen-induced
6415 exfoliation of InP. Appl. Phys. Lett. 2004;85:3.

6416 [437] Zahler JM, Tanabe K, Ladous C, Pinnington T, Newman FD, Atwater HA. High
6417 efficiency InGaAs solar cells on Si by InP layer transfer. Applied Physics Letters
6418 2007;91(1):012108.

6419 [438] Fontcuberta i Morral A, Zahler JM, Atwater HA. InGaAs/InP double heterostructures
6420 on InP/Si templates fabricated by wafer bonding and hydrogen-induced exfoliation.
6421 Applied Physics Letters 2003;83:3.

6422 [439] Takamoto T, Ikeda E, Kurita H, Ohmori M. Over 30% efficient InGaP/GaAs tandem
6423 solar cells. Appl. Phys. Lett. 1997;70:3.

6424 [440] Jackrel DB, Ptak A, Bank S, Yuen H, Wistey M, Friedman D, et al. GaInNAsSb solar
6425 cells grown by molecular beam epitaxy. In: Proceeding of the IEEE 4th World
6426 Conference on Photovoltaic Energy Conversion; 2006.

6427 [441] Derendorf K, Essig S, Oliva E, Klinger V, Roesener T, Philipps SP, et al. Fabrication
6428 of GaInP/GaAs//Si Solar Cells by Surface Activated Direct Wafer Bonding. IEEE
6429 Journal of Photovoltaics 2013;99:1-6.

6430 [442] Essig S, Derendorf K, Oliva E, Wekkeli A, Benick J, Hermele M, et al. Development
6431 of GaInP/GaAs/Si solar cells using surface activated wafer bonding. In: Pacific Rim
6432 Meeting on Electrochemical ans Solid-State Science; 2012.

6433 [443] Essig S, Geisz JF, Steiner MA, Merkle A, Peibst R, Schmidt J, et al. Development of
6434 highly-efficient GaInP/Si Tandem Solar Cells. In: 42nd IEEE PV Specialist Conf.;
6435 2015.

6436 [444] http://solarpowereurope.org/media/press-releases/ (accessed Mar 2016)

6437 [445] IRENA (2012), "Renewable energy technologies: cost analysis series", Solar
6438 Photovoltaics,
6439 http://www.irena.org/DocumentDownloads/Publications/RE_Technologies_Cost
6440 _Analysis-SOLAR_PV.pdf (accessed Mar 2016)

6441 [446] Held M, Ilg R. Update of environmental indicators and energy payback time of
6442 CdTe PV systems in Europe. Prog Photovolt: Res Appl 2011; 19:614–626

6443 [447] S.Mehta, PV technology, production and cost outlook: 2010-2015,
6444 http://www.gtmresearch.com/report/pv-technology-production-and-cost-outlook-
6445 2010-2015 (accessed March 2016)

6446 [448] Solar Photovoltaics Technology Brief, IEA-ETSAP and IRENA© Technology
6447 Brief E11 – January 2013, www.etsap.org – www.irena.org

6448 [449] Benagli S, Borrello D, Vallat-Sauvain E, Meier J, Kroll U, Hötzel J, et al. High-
6449 efficiency amorphous silicon devices on LPCVD-ZNO TCO prepared in
6450 industrial KAI-M R&D Reactor. Proc 24thEuropean Photovoltaic Solar Energy
6451 Conference Hamburg 2009; 3BO.9.3:2293-2298

6452 [450] Kluth O, Kalas J, Fecioru-Morariu M, Losio PA, Hoetzel J. The Way to 11 %
6453 Stabilized Module Efficiency Based on 1.4 m^{2}Micromorph® Tandem. Proc.26th
6454 European Photovoltaic Solar Energy Conference and Exhibition 2011;
6455 3BO.3.6:2354-2357

6456 [451] ThinFab™ 140, www.solar.tel.com (accessed Mar 2016)

6457 [452] http://www.solarserver.com/service/pvx-spot-market-price-index-solar-pv-
6458 modules.html (accessed Mar 2016)

6459 [453]
6460 http://www.epia.org/index.php?eID=tx_nawsecuredl&u=0&file=/uploads/tx_epia
6461 factsheets/Fact_sheet_on_Materials_Availability.pdf&t=1416583533&hash=645
6462 0f47fb2df12d705681560473e1fd360eb47c6 (accessed Mar 2016)

6463 [454] Biron R, H¨anni S, Boccard M, Pahud C, Soderstrom K, Duchamp M, et al. New
6464 progress in the fabrication of n–i–p micromorph solar cells for opaque substrates.
6465 Solar Energy Materials & Solar Cells 2013; 114:147-155

6466 [455] Battaglia C, Escarre J, Soderstrom K, Erni L, Ding L, Bugnon G, et al.
6467 Nanoimprint Lithography for High-Efficiency Thin-Film Silicon Solar Cells.
6468 Nano Letters 2011; 11: 661-665

6469 [456] Brinza M, Rath JK, Schropp REI. Thin film silicon n-i-p solar cells with high
6470 open circuit voltage deposited on low cost plastic substrates. Proc.24th European
6471 Photovoltaic Solar Energy Conference, Hamburg 2009; 3AV.2.50:2727-2730

6472 [457] http://www.solar.tel.com/technologies/thin-film-silicon-solar-technology
6473 (accessed Mar 2016)

6474 [458] Meillaud F, Billet A, Battaglia C, Boccard M, Bugnon G, Cuony P, Charrière M,
6475 et al. Latest developments of high-efficiency micromorph tandem silicon solar
6476 cells implementing innovative substrate materials and improved cell design. IEEE
6477 Journal of Photovoltaics 2012; 2(3): 236-240

6478 [459] de Wild J, Meijerink A, Rath JK, van Sark WGJHM, Schropp REI. Towards
6479 upconversion for amorphous silicon solar cells. Solar Energy Materials and Solar
6480 Cells 2010; 94:1919-1922

6481 [460] http://www2.dupont.com/Photovoltaics/en_US/news_events/article20100422.html
6482 (accessed Mar 2016)

6483 [461] Vetter M, Borrajo JP, Fonrodona M, Otero P, Rodriguez JA, Andreu J, et al. High
6484 Efficient Very Large Thin Film Silicon Photovoltaic Modules (HELATHIS).
6485 Proc.25th European Photovoltaic Solar Energy Conference and Exhibition / 5th
6486 World Conference on Photovoltaic Energy Conversion, Valencia 2010;
6487 3AV.2.24:3220-3223

6488 [462] http://www.bullionvault.com/silver-price-chart.do (accessed Mar 2016)

6489 [463]https://www.irena.org/DocumentDownloads/Publications/RE_Technologies_Cost_Anal
6490 ysis-SOLAR_PV.pdf (accessed March 2016)

6491 [464] Carlson DE, Wronski CR. Amorphous silicon solar cell. Applied Physics Letters
6492 1976; 28: 671

6493 [465] Stutzmann M, Jackson WB, Tsai CC. Light-induced metastable defects in
6494 hydrogenated amorphous silicon: A systematic study. Physical Review B 1985;
6495 32(1): 23–47

6496 [466] Street RA. Hydrogen diffusion and electronic metastability in amorphous silicon.
6497 Physica B 1991; 170: 69-81

6498 [467] Branz HM. Hydrogen collision model: Quantitative description of metastability in
6499 amorphous silicon. Physical Review B 1999; 59(8): 5498–5512

6500 [468] Carlson DE. Hydrogenated microvoids and light-induced degradation of
6501 amorphous silicon solar cells. Applied Physics A 1986; 41(4): 305–309

6502 [469] Fehr M, Schnegg A, Rech B, Astakhov O, Finger F, Bittl R, et al. Metastable
6503 defect formation at microvoids identified as a source of light-induced degradation
6504 in a-Si:H. Physical Review Letters 2014; 112; 066403

6505 [470] Melskens J, Schouten M, Mannheim A, Vullers AS, Mohammadian Y, Eijt SWH,
6506 at al. The Nature and the Kinetics of Light-Induced Defect Creation in
6507 Hydrogenated Amorphous Silicon Films and Solar Cells. IEEE Journal Of
6508 Photovoltaics 2014; 4 (6): 1331-1336

6509 [471] Arya RR, Oswald RS, Li YM, Maley N, Jansen K, Yang L, at al. Progress in
6510 Amorphous Silicon-based Multijunction Modules. Conference Record of the 24th
6511 IEEE Photovoltaic Specialists Conference 1994; 395-400

6512 [472] Yang Y, Ross R, Glatfelter T, Mohr R, Guha S. Amorphous Silicon Germanium
6513 Alloy Solar Cells with Profiled Band Gaps. Mat. Res. Soc. Symp. Proc. 1989;
6514 149: 435-440

6515 [473] Terakawa A, Shima M, Sayama K, Tarui H, Nishiwaki H, Tsuda S. Hydrogenated
6516 Amorphous Silicon Germanium Alloy for Stable Solar Cells. Mat Res Soc Symp
6517 Proc 1994; 336: 487

6518 [474] Ichikawa Y, Tabuchi K, Kato S, Takano A, Sasaki T, Tanda M, et al. A new
6519 structure a-Si solar cell with plastic film substrate, Proceedings of the First
6520 WCPEC Hawaii 1994; 441

6521 [475] Guha S, Yang J, Effect of microvoids on initial and light-degraded efficiencies of
6522 hydrogenated amorphous silicon alloy solar cells, Applied Physics Letters 1992;
6523 61: 1444

6524 [476] Meier J, Fluckiger R, Keppner H, Shah A, Applied Physics Letters 1994; 65:860

6525 [477] Fischer D, Dubail S, Anna Selvan JA, PellatonVaucher N, Platz R, Hof Ch, et al.
6526 The "micromorph" solar cell: extending a-Si:H technology towards thin film
6527 crystalline silicon. Proc 25thIEEE Photovoltaic Specialists Conference,
6528 Washington D.C.1996;1053

[478] Yamamoto K, Yoshimi M, Tawada Y, Okamoto Y, Nakajima A, Igari S. Thin-film poly-Si solar cells on glass substrate fabricated at low temperature. Applied Physics A 1999; 69: 179-185

[479] Rath JK. Progress and Challenges of Photovoltaic Applications of Silicon Nanocrystalline Materials. In: Zhang S, editor. CRC Handbook of Nanostructured Thin Films and Coatings, CRC Press; 2010, Ch.3, 109-128

[480] Shima M, Isomura M, Maruyama E, Okamoto S, Haku H, Wakisaka K, et al. Development of Stable a-Si/a-SiGe Tandem Solar Cell Submodules Deposited by a Very High Hydrogen Dilution at Low Temperature. Mat Res Soc Symp Proc 1998; 507:145-156

[481] Rath JK. Nanocystalline silicon solar cells. Applied Physics A 2009; 96: 145-152

[482] Meillaud F, Shah A, Droz C, Vallat-Sauvain E, Miazza C. Efficiency limits for single-junction and tandem solar cells. Solar Energy Materials and Solar Cells 2006; 90: 2952-2959

[483] Yan B, Yue G, Sivec L, Yang J, Guha S, Jiang CS. Innovative dual function nc-SiOx:H layer leading to a >16% efficient multi-junction thin-film silicon solar cell. Applied Physics Letters 2011; 99: 113512

[484] Green MA, Emery K, Hishikawa Y, Warta W, Dunlop ED. Solar cell efficiency tables (version 45). Prog Photovolt: Res Appl 2015; 23:1–9

[485] Green MA, Emery K, Hishikawa Y, Warta W, Dunlop ED. Solar cell efficiency tables (version 41). Prog Photovolt: Res Appl 2013; 21:1

[486] Chung JW, Park JW, Lee YJ, Ahn SW, Lee HM, Park O. Graded Layer Modification for High Efficiency Hydrogenated Amorphous Silicon–Germanium Solar Cells. Japanese Journal of Applied Physics 2012;51:10NB16

[487] Zambrano RJ, Rubinelli FA, Rath JK, Schropp REI. Improvement in the spectral response at long wavelength of a-SiGe:H solar cells by exponential band gap design of the i-layer. J Non-Cryst Solids 2002; 299–302: 1131-1135

[488] Zambrano RJ, Rubinelli FA, Arnoldbik WM, Rath JK, Schropp REI. Computer-aided band gap engineering and experimental verification of amorphous silicon-germanium solar cells. Solar Energy Materials and Solar Cells 2004; 81: 73-86

[489] Gordijn A, Zambrano RJ, Rath JK, Schropp REI. IEEE Trans. Electron Devices 2002; 49: 949-952

[490] Rath JK, Tichelaar FD, Schropp REI. Heterogeneous growth of microcrystalline silicon germanium. Solar Energy Materials and Solar Cells 2002; 74:553-560

6563 [491] Matsui T, Jia H, Kondo M. Thin film solar cells incorporating microcrystalline
6564 $Si_{1-x}Ge_x$ as efficient infrared absorber: an application to double junction tandem
6565 solar cells. Prog Photovolt: Res Appl 2010:18:48-53

6566 [492] Matsui T, Jia H, Kondo M, Mizuno K, Tsuruga S, Sakai S, Takeuchi Y.
6567 Application of microcrystalline $Si_{1-x}Ge_x$ infrared absorbers in triple junction solar
6568 cells. IEEE Photovoltaic Specialists Conference 2010; 5615904:311-316.

6569 [493] Cao Y, Zhang J, Li C, Li T, Huang Z, Ni J, et al. Hydrogenated microcrystalline
6570 silicon germanium as bottom sub-cell absorber for triple junction solar cell. Solar
6571 Energy Materials &Solar Cells 2013; 114:161-164

6572 [494] Mahan AH, Xu Y, Gedvilas LM, Williamson DL. A direct correlation between
6573 film structure and solar cell efficiency for HWCVD amorphous silicon
6574 germanium alloys. Thin Solid Films 2009; 517: 3532-3535

6575 [495] Hishikawa Y, Sasaki M, Tsuge S, Okamoto S, Tsuda S. Material Control for
6576 High-Efficiency Amorphous Silicon Solar Cells. Mater Res Soc Symp Proc 1993;
6577 297:779-784

6578 [496] Terakawa A, Shima M, Sayama K, Tarui H, Nishiwaki H, Tsuda S. Optimization
6579 of a-SiGe:H Alloy Composition for Stable Solar Cells. Japanese Journal of
6580 Applied Physics 1995; 34:1741-1747

6581 [497] Hänni S, Bugnon G, Parascandolo G, Boccard M, Escarré J, Despeisse M, et al.
6582 High-efficiency microcrystalline silicon single-junction solar cells. Prog
6583 Photovolt: Res Appl 2013;21: 821-826

6584 [498] Gordijn A, Rath JK, Schropp REI. High-Efficiency μc-Si Solar Cells Made by
6585 Very High-Frequency Plasma-Enhanced Chemical Vapor Deposition. Prog
6586 Photovolt: Res Appl 2006; 14: 305–311

6587 [499] Kroll U, Meier J, Fesquet L, Steinhauser J, Benagli S, Orhan JB, et al. Recent
6588 Developments of High-Efficiency Micromorph Tandem Solar Cells in KAI-M/
6589 Plasmabox PECVD Reactors. Proc.26th European Photovoltaic Solar Energy
6590 Conference and Exhibition 2011; 3BO.2.6:2340-2343

6591 [500] Yamamoto K, Nakajima A, Yoshimi M, Sawada T, Fukuda S, Suezaki T, et al.
6592 Novel hybrid thin film silicon solar cell and module. Proc 3rd World Conf on
6593 Photovoltaic Energy Conversion Osaka 2003; 3: 2789-2792

6594 [501] Kim S, Chung JW, Lee H, Park J, Heo Y, Lee HM. Remarkable progress in thin-
6595 film silicon solar cells using high-efficiency triple-junction technology. Solar
6596 Energy Materials & Solar Cells 2013; 119:26-35

6597 [502] Yue G, Yan B, Sivec L, Su T, Zhou Y, Yang J, Guha S. Hydrogenated
6598 nanocrystalline silicon based solar cell with 13.6% stable efficiency. Mat Res Soc
6599 Symp Proc 2012;1426: 33-38

6600 [503] Guha S, Yang J, Yan B. High efficiency multi-junction thin film silicon cells
6601 incorporating. Solar Energy Materials and Solar Cells 2013; 119:1-11.

6602 [504] Goodrichn A, Hacke P, Wang Q, Sopori B, Margolis R, James TL, Woodhouse
6603 M. A wafer-based monocrystalline silicon photovoltaics road map: Utilizing
6604 known technology improvement opportunities for further reductions in
6605 manufacturing costs. Solar Energy Materials & Solar Cells 2013; 114:110-135

6606 [505] Taguchi M, Yano A, Tahoda S, Matsuyama K, Nakamura Y, Nishiwaki T, Fujita
6607 K, Maruyama E, 24.7% record efficiency HIT solar cell on thin silicon wafer.
6608 IEEE Journal of Photovoltaics, 2014; 4:96-99,

6609 [506] Lochtefeld A, Wang L, Carroll M, Han J, Stryker D, Bengtson S, et al. 15%, 20
6610 Micron Thin, Silicon Solar Cells on Steel, *Proc 39th IEEE PVSC Tampa*
6611 2013;1364-1365

6612 [507] Mahan AH, Vanecek M. A reduction in the Staebler-Wronski effect observed in
6613 low H content a-Si:H films deposited by the hot wire technique. In: Amorphous
6614 Silicon Materials and Solar Cells. AIP Conf Proc 1991; 234:195-202

6615 [508] Guha S, Yang J, Banerjee A, Yan B, Lord K. High quality amorphous silicon
6616 materials and cells grown with hydrogen dilution. Solar Energy Materials & Solar
6617 Cells 2003;78:329-345

6618 [509] Kim KH, Kasouit S, Johnson EV, Cabarrocas PRi. Substrate versus superstrate
6619 configuration for stable thin film silicon solar cells. Solar Energy Materials and
6620 Solar Cells 2013;119:124–128

6621 [510] Rath JK, Das UK, Chaudhuri P. Reduced light induced degradation in a-Si:H
6622 solar cells with i-layer deposited by glow discharge decomposition of silane-
6623 argon mixture. Proc. 13th European Photovoltaic Solar Energy Conference, Nice
6624 1995; p 280.

6625 [511] Rath JK. Low temperature polycrystalline silicon: a review on deposition,
6626 physical properties and solar cell applications. Solar Energy Materials & Solar
6627 Cells 2003;76:431-487

6628 [512] de Jong MM, Baggerman J, van Rijn CJM, Sonneveld PJ, Swinkels GLAM,
6629 Holterman HJ, et al. Scattering, Diffraction, and Geometric Light Trapping in
6630 Thin Film Amorphous Silicon Solar Cells on Plastic Substrates. Mat Res Soc
6631 Symp Proc 2012;1426:155-160

6632 [513] Yablonovitch E. Statistical ray optics. Journal of the Optical Society of America
6633 1982; 72:899-907

6634 [514] Meier, M., Paetzold, U.W., Ghosh, M., Zhang, W., Merdzhanova, T., Jost, G.,
6635 Sommer, N., Michard, S., Gordijn, A., Fabrication of light-scattering multiscale

6636 textures by nanoimprinting for the application to thin-film silicon solar cells,
6637 IEEE Journal of Photovoltaics, 2014; 4 :772-777

6638 [515] Sai H, Matsui T, Bidiville A, Koida T, Yoshida Y, Saito K, Kondo M. Light
6639 Management Using Periodic Textures for Enhancing Photocurrent and
6640 Conversion Efficiency in Thin-Film Silicon Solar Cells. Mat Res Soc Symp Proc
6641 2013; 1536:3-15

6642 [516] Ganapati E, Miller OD, Yablonovitch E, Light trapping textures designed by
6643 electromagnetic optimization for subwavelength thick solar cells, IEEE Journal
6644 of Photovoltaics 2014; 4:175-182.

6645 [517] Atwater HA, Polman A. Plasmonics for improved photovoltaic devices. Nature
6646 Materials 2010; 9:205-213

6647 [518] Battaglia C, Escarre J, Soderstrom K, Charriere M, Despeisse M, Haug FJ, Ballif
6648 C. Nanomoulding of transparent zinc oxide electrodes for efficient light trapping
6649 in solar cells. Nature photonics 2011;5:535-538

6650 [519] Pahud C, Savu C, Klein B, Vazquez-Mena MC, Soderstrom OD, Haug KA, et al.
6651 Stencil-nanopatterned back reflectors for thin-film amorphous silicon n-i-p solar
6652 cells. Proc 38th IEEE PVSC Austin 2012; 694-696

6653 [520] de Jong MM, Sonneveld PJ, Baggerman J, van Rijn CJM, Rath JK, Schropp REI.
6654 Utilization of geometric light trapping in thin film silicon solar cells: simulations
6655 and experiments. Prog Photovolt: Res Appl 2012; 22:540-547.

6656 [521] http://www.firstsolar.com (accessed Mar 2016)

6657 [522] http://www.pv-magazine.com/news/details/beitrag/zsw-sets-217-thin-film-
6658 efficiency-record_100016505/#axzz3EJGmgHsk (accessed Mar 2016)

6659 [523] Li HBT, Franken RH,Rath JK, Schropp REI. Structural defects caused by a rough
6660 substrate and their influence on the performance of hydrogenated nano-crystalline
6661 silicon n-i-p solar cells. Solar Energy Materials and Solar Cells 2009; 93(3):338–
6662 349

6663 [524] Andrew Barnabas Wong, Sarah Brittman, Yi Yu, Neil P. Dasgupta, and Peidong
6664 Yang, Core–Shell CdS–Cu_2S Nanorod Array Solar Cells, Nano Lett., 2015, 15
6665 (6), pp 4096–4101.

6666 [525] Kuang Y, van der Werf CHM, Houweling ZS, Schropp REI. Nanorod solar cell
6667 with an ultrathin a-Si:H absorber layer. Applied Physics Letters 2011; 98: 113111
6668 (1-3).

6669 [526] GeiBendörfer S, Vehse M, Voss T, Richters JP, Hanke H, von Maydell K, Agert
6670 C. Integration of n-doped ZnOnanorod structures as novel light-trapping concept

6671 in amorphous thin film silicon solar cells. Solar Energy Materials and Solar Cells
6672 2013;111:153-159.

6673 [527] Aixue Shang, Xiongfei Zhai, Cheng Zhang, Yaohui Zhan, Shaolong Wu,
6674 Xiaofeng Li, Nanowire and nanohole silicon solar cells: a thorough
6675 optoelectronic evaluation, Prog. Photovolt: Res. Appl., 2015; 23: 1734–1741.

6676 [528] Vanecek M, Babchenko O, Purkrt A, Holovsky J, Neykova N, Poruba A, et al.
6677 Nanostructured three-dimensional thin film silicon solar cells with very high
6678 efficiency potential. Applied Physics Letters 2011; 98:163503 (1-3)

6679 [529] Avra Kundu, Sonali Das, S.M. Hossain, Swapan K. Datta, Hiranmay Saha,
6680 Tapered Silicon Nanopillars for Enhanced Performance Thin Film Solar Cells,
6681 Energy Procedia 2014; 54: 389-399

6682 [530] Lei Hong, Rusli, Xincai Wang, Hao Wang, Xiaoyan Xu, Lining He, Hongyu
6683 Zheng, Towards Perfect Anti-Reflection and Absorption for Nanodome-Array
6684 Thin Film Silicon Solar Cell, Energy Procedia, 2013; 33: 150-156.

6685 [531] Paudel T, Rybczynski J, Gao YT, Lan YC, Peng Y, Kempa K, et al. Nanocoax
6686 solar cells based on aligned multiwalled carbon nanotube arrays. Physica Status
6687 Solidi (A), Applications and Materials Science 2011; 208(4): 924-927

6688 [532] Garnett EC, Yang PD. Silicon Nanowire Radial p-n Junction Solar Cells. J Am
6689 Chem Soc 2008; 130: 9224-9225

6690 [533] Lu YR, Lal A. High-Efficiency Ordered Silicon Nano-Conical-Frustum Array
6691 Solar Cells by Self-Powered Parallel Electron Lithography. Nano Letters 2010;
6692 10:4651-4656

6693 [534] Putnam MC, Boettcher SW, Kelzenberg MD, Turner-Evans DB, Spurgeon JM,
6694 Warren EL, et al. Si microwire-array solar cells. Energy Environ Sci 2010;
6695 3:1037-1041

6696 [535] Tsakalakos L, Balch J, Fronheiser J, Korevaar BA, Sulima O, Rand J, Silicon
6697 nanowire solar cells. Applied Physics Letters 2007; 91:233117 (1-3)

6698 [536] Kendrick CE, Yoon HP, Yuwen YA, Barber GD, Shen HT, Mallouk TE, et al.
6699 Radial junction silicon wire array solar cells fabricated by gold-catalyzed vapor–
6700 liquid-solid growth. Applied Physics Letters 2010; 97:143108 (1-3)

6701 [537] O'Donnell B, Yu L, Foldyna M, Cabarrocas PRi. Silicon nanowire solar cells
6702 grown by PECVD. Journal of Non-Crystalline Solids 2012; 358: 2299-2302

6703 [538] Zhu J, Hsu CM, Yu Z, Fan S, Cui Y. Nanodome Solar Cells with Efficient Light
6704 Management and Self-Cleaning. Nano Letters 2010; 10:1979-1984

6705 [539] Naughton MJ, Kempa K, Ren ZF, Gao Y, Rybczynski J, Argenti N, et al.
6706 Efficient nanocoax-based solar cells. Phys. Status Solidi RRL 2010; 4:181-183

6707 [540] Hsu CM, Battaglia C, Pahud C, Ruan Z, Haug FJ, Fan S, et al. High-efficiency
6708 amorphous silicon solar cell on a periodic nanocone back reflector. Advanced
6709 Energy Materials 2012; 2(6):628-633

6710 [541] Kim J, Hong AJ, Nah JW, Shin B, Ross FM, Sadana DK. Three-dimensional a-
6711 Si:H solar cells on glass nanocone arrays patterned by self-assembled Sn
6712 nanospheres. ACS Nano 2012; 6(1): 265-271

6713 [542] Ferry VE, Verschuuren MA, van Lare MC, Schropp REI, Atwater HA, Polman
6714 A. Optimized Spatial Correlations for Broadband Light Trapping Nanopatterns in
6715 High Efficiency Ultrathin Film a-Si:H Solar Cells. Nano Letters 2011;11: 4239-
6716 4245

6717 [543] Söderström K, Bugnon G, Haug FJ, Ballif C. Electrically flat/optically rough
6718 substrates for efficiencies above 10% in n-i-p thin-film silicon solar cells. Mat
6719 Res Soc Symp Proc 2012; 1426: 39-44

6720 [544] Sai H, Kanamori Y, Kondo M. Flattened light-scattering substrate in thin film
6721 silicon solar cells for improved infrared response. Applied Physics Letters 2011;
6722 98: 113502 (1-3)

6723 [545] Spee D, van der Werf K, Rath J, Schropp R. Excellent organic/inorganic
6724 transparent thin film moisture barrier entirely made by hot wire CVD at 100 °C.
6725 Phys. Status Solidi RRL 2012;6:151–153

6726 [546] Conibeer G, Green M, Cho EC, Konig D, Cho YH, Fangsuwannarak T, et al.
6727 Silicon quantum dot nanostructures for tandem photovoltaic cells. Thin Solid
6728 Films 2008; 516:6748-6756

6729 [547] Conibeer G. Si and Other Group IV Quantum Dot Based Materials for Tandem
6730 Solar Cells. Energy Procedia 2012;15:200-205

6731 [548] Shcherbyna L, Torchynska T. Si quantum dot structures and their applications.
6732 Physica E 2013; 51:65-70

6733 [549] Zeng J, Yu H. A First-Principle Study of B- and P-Doped Silicon Quantum Dots.
6734 Journal of Nanomaterials 2012; 147169(1-7)

6735 [550] H. Seo, Y. Wang, M. Sato, G. Uchida, K. Kamataki, N. Itagaki, et al.
6736 Improvement of Si Adhesion and Reduction of Electron Recombination for Si
6737 Quantum Dot-Sensitized Solar Cells. Japanese Journal of Applied Physics 2013;
6738 52: 01AD05(1-5)

6739 [551] de Wild J, Meijerink A, Rath JK, van Sark WGJHM, Schropp REI. Upconverter
6740 solar cells: materials and applications. Energy Environ Sci 2011; 4:4835-4848

6741 [552] Cheng YY, Fuckel B, MacQueen RW, Khoury T, Clady RGCR, Schulze TF, et
6742 al. Improving the light-harvesting of amorphous silicon solar cells with
6743 photochemical upconversion. Energy Environ Sci 2012; 5;6953-6959

6744 [553] Pan AC, del Canizo C, Canavos E, Santos NM, Leitao JP, Luque A.
6745 Enhancement of up-conversion efficiency by combining rare-earth-doped
6746 phosphors with PbS quantum dots. Solar Energy Materials and Solar Cells 2010;
6747 94:1923-1926

6748 [554] Verhagen E, Kuipers L, Polman A. Enchanced Nonlinear Optical Effects with a
6749 Tapered Plasmonic Waveguide. Nano Letters 2007; 7:334-337.

6750 [555] Katagiri H, Jimbo K, Maw W S, Oishi K, Yamazaki M, Araki H, and Takeuchi
6751 A, Development of CZTS-based thin film solar cells, Thin Solid Films
6752 2009;517:2455-2460.

6753 [556] Todorov T K, Reuter K B, and Mitzi D B, High-efficiency solar cell with earth-
6754 abundant liquid-processed absorber, Adv. Mat. 2010;22:E156.

6755 [557] Barkhouse D A R, Gunawan O, Gokmen T, Todorov T K, and Mitzi D B, Device
6756 characteristics of a 10.1% hydrazine-processed Cu2ZnSn(Se,S)4 solar cell, Prog.
6757 Photovolt: Res. Appl. 2012;20:6-11.

6758 [558] Todorov T K, Tang J, Bag S, Gunawan O, Gokmen T, Zhu Y, and Mitzi D B,
6759 Beyond 11% efficiency: Characteristics of state-of-the-art Cu2ZnSn(S,Se)4 solar
6760 cells, Adv. Ener. Mater. 2013;3:34-38.

6761 [559] Wang W, Winkler M T, Gunawan O, Gokmen T, Todorov T K, Zhu Y, and Mitzi
6762 D B, Device characteristics of CZTSSe thin film solar cell with 12.6% efficiency,
6763 Adv. Ener. Mater. 2014;4:1301465.

6764 [560] Mitzi D B, Gunawan O, Todorov T K, Wang K, and Guha S, The path towards a
6765 high-performance solution-processed kesterite solar cell, Sol. Energy Mater. Sol.
6766 Cells 2011;95:1421-1436.

6767 [561] Siebentritt S, Why are kesterite solar cells not 20% efficient?, Thin Solid Films
6768 2013;535:1-4.

6769 [562] Ito K and Nakazawa T, Electrical and optical properties of stannite-type
6770 quaternary semiconductor thin films, Jpn. J. Appl. Phys. 1988;27:2094-2097.

6771 [563] Schorr S, Structural aspects of adamantine like multinary chalcogenides, Thin
6772 Solid Films 2007;515:5985-5991.

6773 [564] Weber A, Mainz R, Unold T, Schorr S, and Schock H W, In-situ XRD on
6774 formation reactions of Cu2ZnSnS4 thin films, Phys. Status Solidi (c)
6775 2009;6:1245-1248.

6776 [565] Schorr S, Weber A, Honkimäki V, and Schock H W, In-situ investigation of the
6777 keterite formation from binary and ternary sulfides, Thin Solid Films 2009;517
6778 2461-2464.

6779 [566] Friedlmeier T M, Wieser N, Walter T, Dittrich H, and Schock H W,
6780 Heterojunctions based on Cu2ZnSnS4 and Cu2ZnSnSe4 thin films, in Proc. 14th
6781 Eur. Photovolt. Sol. Energy Conf., 1997, 1242-1245.

6782 [567] Fontane X, Calvo-Barrio L, Izquierdo-Roca V, Saucedo E, Perez-Rodriguez A,
6783 Morante J R, Berg D M, Dale P J, and Siebentritt S, In-depth resolved Raman
6784 scattering analysis for the identification of secondary phases: Characterization of
6785 Cu2ZnSnS4 layers for solar cell applications, Appl. Phys. Lett. 2011;98:181905.

6786 [568] Yoo H et al., Investigation of the solid state reactions by time-resolved X-ray
6787 diffraction while crystallizing kesterite Cu2ZnSnSe4 thin films, Thin Solid Films
6788 2013;535:73-77.

6789 [569] Schorr S, Hoebler H J, and Tovar M, A neutron diffraction study of the stannite-
6790 kesterite solid solution series, European Journal of Mineralogy 2007;19:65-73.

6791 [570] Just J, Lutzenkirchen-Hecht D, Frahm R, Schorr S, and Unold T, Determination
6792 of secondary phases in kesterite Cu2ZnSnS4 thin films by x-ray absorption near
6793 edge structure analysis, Appl. Phys. Lett. 2011;99:262105.

6794 [571] Gao F, Yamazoe S, Maeda T, Nakanishi K, and Wada T, Structural and Optical
6795 Properties of In-Free Cu2ZnSn(S,Se)4 Solar Cell Materials, Jpn. J. Appl. Phys.
6796 2012;51:10NC29.

6797 [572] Scragg J J, Berg D M, and Dale P J, A 3.2% efficient kesterite device from
6798 electrodeposited stacked elemental layers, J. Electroanal. Chem. 2010;646:52-59.

6799 [573] Ennaoui A et al., Cu2ZnSnS4 thin film solar cells from electroplated precursors:
6800 Novel low-cost perspective, Thin Solid Films 2009;517:2511-2514.

6801 [574] Hsu W-C, Repins I, Beall C, DeHart C, Teeter G, To B, Yang Y, and Noufi R,
6802 The effect of Zn excess on kesterite solar cells, Sol. Energy Mater. Sol. Cells
6803 2013;113:160-164.

6804 [575] Fairbrother A, Garcia-Hemme E, Izquierdo-Roca V, Fontane X,
6805 Pulgarin Agudelo F A, Vigil-Galan O, Perez-Rodriguez A, and Saucedo E,
6806 Development of a selective chemical etch to improve the conversion efficiency of
6807 Zn-rich Cu2ZnSnS4 solar cells, J. Am. Chem. Soc. 2012;134:8018-8021.

6808 [576] Shin B, Zhu Y, Bojarczuk N A, Chey S J, and Guha S, Control of an interfacial
6809 MoSe2 layer in Cu2ZnSnSe4 thin film solar cells: 8.9% power conversion
6810 efficiency with a TiN diffusion barrier, Appl. Phys. Lett. 2012;101:053903.

6811 [577] Cao Y et al., High-efficiency solution-processed Cu2ZnSn(S,Se)4 thin-film solar
6812 cells prepared from binary and ternary nanoparticles, J. Am. Chem. Soc.
6813 2012;134:15644-15647.

6814 [578] Katagiri H, Jimbo K, Tahara M, Araki H, and Oishi K, The influence of the
6815 composition ratio on CZTS-based thin film solar cells, Mater. Res. Soc. Symp.
6816 Proc. 2009;1165:M04-01.

6817 [579] Jimbo K, Kimura R, Kamimura T, Yamada S, Maw W S, Araki H, Oishi K, and
6818 Katagiri H, Cu2ZnSnS4-type thin film solar cells using abundant materials, Thin
6819 Solid Films 2007;515:5997-5999.

6820 [580] Katagiri H, Jimbo K, Yamada S, Kamimura T, Maw W S, Fukano T, Ito T, and
6821 Motohiro T, Enhanced conversion efficiencies of Cu2ZnSnS4-based thin film
6822 solar cells by using preferential etching technique, Appl. Phys. Expr.
6823 2008;1:41201.

6824 [581] Hiroi H, Sugimoto H, and Kato T, High voltage Cu2ZnSnS4 submodules by
6825 hybrid buffer layer, in IEEE PVSC Specialist Conference, 2013.

6826 [582] Schubert B A, Marsen B, Cinque S, Unold T, Klenk R, Schorr S, and Schock H-
6827 W, Cu2ZnSnS4 thin film solar cells by fast coevaporation, Prog. Photovolt: Res.
6828 Appl. 2011;19:93-96.

6829 [583] Repins I et al., Co-evaporated Cu2ZnSnSe4 films and devices, Sol. Energy Mater.
6830 Sol. Cells 2012;101:154.

6831 [584] Li J V, Kuciauskas D, Young M R, and Repins I L, Effects of sodium
6832 incorporation in Co-evaporated Cu2ZnSnSe4 thin-film solar cells, Appl. Phys.
6833 Lett. 2013;102:163905.

6834 [585] Katagiri H, Sasaguchi N, Hando S, Hoshino S, Ohashi J, and Yokota T,
6835 Preparation and evaluation of Cu2ZnSnS4 thin films by sulfurization of E-B
6836 evaporated precursors, Sol. Energy Mater. Sol. Cells 1997;49:407-414.

6837 [586] Katagiri H, Jimbo K, Monya K, and Tsuchida K, Solar cell without
6838 environmental pollution by using CZTS thin film, in Proc. World. Conf. on
6839 Photvoltaics Energy Conversion III, 2003, 2874-2879.

6840 [587] Redinger A, Berg D M, Dale P J, and Siebentritt S, The consequences of kesterite
6841 equilibria for efficient solar cells, J. Am. Chem. Soc. 2011;133:3320–3323.

6842 [588] Shin B, Gunawan O, Zhu Y, Bojarczuk N A, Chey S J, and Guha S, Thin film
6843 solar cell with 8.4% power conversion efficiency using earth abundant
6844 Cu2ZnSnS4 absorber, Prog. Photovolt: Res. Appl. 2013;21:72.

6845 [589] Scragg J J, Dale P J, and Peter L M, Synthesis and characterization of
6846 Cu2ZnSnS4 absorber layers by an electrodeposition-annealing route, Thin Solid
6847 Films 2009;517:2481-2484.

6848 [590] Ahmed S, Reuter K B, Gunawan O, Guo L, Romankiw L T, and Deligianni H, A
6849 high efficiency electrodeposited Cu2ZnSnS4 solar cell, Adv. Ener. Mater.
6850 2012;2:253-259.

6851 [591] Todorov T, Kita M, Carda J, and Escribano P, Cu2ZnSnS4 films deposited by a
6852 soft-chemistry method, Thin Solid Films 2009;517:2541-2544.

6853 [592] Guo Q, Ford G M, Yang W C, Walker B C, Stach E A, Hillhouse H W, and
6854 Agrawal R, Fabrication of 7.2% efficient CZTSSe solar cells using CZTS
6855 nanocrystals, J. Am. Chem. Soc. 2010;132:17384-17386.

6856 [593] Yang W, Duan H S, Bob B, Zhou H, Lei B, Chung C H, Li S H, Hou W W, and
6857 Yang Y, Novel solution processing of high-efficiency earth-abundant
6858 Cu2ZnSn(S,Se)4 Solar Cells, Adv. Mat. 2012;24:6323-6329.

6859 [594] Todorov T K, Gunawan O, Gokmen T, and Mitzi D B, Solution-processed
6860 Cu(In,Ga)(S,Se)2 absorber yielding 15.2% efficient solar cell, Prog. Photovolt:
6861 Res. Appl. 2013;21:82-87.

6862 [595] Ki W and Hillhouse H W, Earth abundant element photovoltaics directly from
6863 soluble precursors with high yield using a non toxic solvent, Adv. Ener. Mater.
6864 2011: vol. 1, 732-735.

6865 [596] Todorov T, Sugimoto H, Gunawan O, Gokmen T, and Mitzi D B, High-efficiency
6866 devices with pure solution-processed Cu2ZnSn(S,Se)4 absorbers, IEEE J.
6867 Photovoltaics 2014;4:483.

6868 [597] Jackson P, Hariskos D, Lotter E, Paetel S, Wuerz R, Menner R, Wischmann W,
6869 and Powalla M, New world record efficiency for Cu(In,Ga)Se2 thin film solar
6870 cells beyond 20%, Prog. Photovolt: Res. Appl. 2011;19:894-897.

6871 [598] Rau U and Werner J H, Radiative efficiency limits of solar cells with lateral
6872 band-gap fluctuations, Appl. Phys. Lett. 2004;84:3735.

6873 [599] Y. S. Lee, T. Gershon, O. Gunawan, T. K. Todorov, B. Shin, T. Gokmen, Y.
6874 Virgus, and S. Guha, Cu2ZnSnSe4 thin-film solar cells by thermal co-evaporation
6875 with 11.6% power conversion efficiency and improved minority carrier diffusion
6876 length, Adv. Ener. Mater. 5, 1401372 (2015).

6877 [600] Gokmen T, Gunawan O, Todorov T K, and Mitzi D B, Band tailing and
6878 efficiency limitation in kesterite solar cells, Appl. Phys. Lett. 2013;103:103506

6879 [601] Sites J R and Mauk P H, Diode quality factor determination for thin-film solar
6880 cells, Sol. Cells 1989;27:411-417.

[602] Watjen J T, Engman J, Edoff M, and Platzer-Bjorkman C, Direct evidence of current blocking by ZnSe in Cu2ZnSnSe4 solar cells, Appl. Phys. Lett. 2012;100:173510.

[603] Gunawan O, Todorov T K, and Mitzi D B, Loss mechanisms in hydrazine-processed Cu2ZnSn(Se,S)4 solar cells, Appl. Phys. Lett. 2010;97:233506.

[604] Repins I L et al., Indications of short minority-carrier lifetime in kesterite solar cells, J. Appl. Phys. 2013;114:084507.

[605] Green M A, Solar cell fill factors-General graph and empirical expressions, Solid State Electronics 1981;24:788.

[606] Krustok J, Josepson R, Danilson M, and Meissner D, Temperature dependence of Cu2ZnSn(SexS1-x)4 monograin solar cells, Sol. Energy 2010;84:379-383.

[607] Gunawan O et al., Electronic properties of the Cu2ZnSn(Se,S)4 absorber layer in solar cells as revealed by admittance spectroscopy and related methods, Appl. Phys. Lett. 2012;100:253905.

[608] Kask E, Raadik T, Grossberg M, Josepson R, and Krustok J, Deep defects in Cu2ZnSnS4 monograin solar cells, Energy Procedia 2012;10:261-265.

[609] Chen S, Yang J H, Gong X G, Walsh A, and Wei S H, Intrinsic point defects and complexes in the quaternary kesterite semiconductor Cu2ZnSnS4, Phys. Rev. B 2010;81:245204.

[610] Duan H-S, Yang W, Bob B, Hsu C-J, Lei B, and Yang Y, The role of sulfur in solution-processed Cu2ZnSn(S,Se)4 and its effect, Advanced Functional Materials vol.23, 1466-1471, 2013.

[611] Nadenau V, Rau U, Jasenek A, and Schock H W, Electronic properties of CuGaSe-based heterojunction solar cells. Part I. Transport analysis, J. Appl. Phys. 2000;87:584.

[612] Minemoto T, Matsui T, Takakura H, Hamakawa Y, Negami T, Hashimoto Y, Uenoyama T, and Kitagawa M, Theoretical analysis of the effect of conduction band offset of window/CIS layers on performance of CIS solar cells using device simulation, Sol. Energy Mater. Sol. Cells 2001;67:83-88.

[613] Haight R, Barkhouse A, Gunawan O, Shin B, Copel M, Hopstaken M, and Mitzi D B, Band alignment at the Cu2ZnSn(SxSe1-x)4/CdS interface, Appl. Phys. Lett. 2011;98:253502.

[614] Bär M et al., Cliff-like conduction band offset and KCN-induced recombination barrier enhancement at the CdS/Cu2ZnSnS4 thin-film solar cell heterojunction, Appl. Phys. Lett. 2011;99:222105.

6916 [615] Krustok J, Josepson R, Raadik T, and Danilson M, Potential fluctuations in
6917 Cu2ZnSnSe4 solar cells studied by temperature dependence of quantum
6918 efficiency curves, Phys. B: Cond. Matt. 2010;405:3186-3189.

6919 [616] Halliday D P, Claridge R, Goodman M C J, Mendis B G, Durose K, and Major J
6920 D, Luminescence of Cu2ZnSnS4 polycrystals described by the fluctuating
6921 potential model, J. Appl. Phys. 2013;113:223503.

6922 [617] Chen S, Wang L W, Walsh A, Gong X G, and Wei S H, Abundance of CuZn+
6923 SnZn and 2CuZn+ SnZn defect clusters in kesterite solar cells, Appl. Phys. Lett.
6924 2012;101:223901-223904.

6925 [618] Chen S, Walsh A, Gong X G, and Wei S H, Classification of lattice defects in the
6926 kesterite Cu2ZnSnS4 and Cu2ZnSnSe4 earth abundant solar cell absorbers, Adv.
6927 Mat. 2013;25:1522-1539.

6928 [619] Persson C, Electronic and optical properties of Cu2ZnSnS4 and Cu2ZnSnSe4, J.
6929 Appl. Phys. 2010;107:053710.

6930 [620] Miller D W, Warren C W, Gunawan O, Gokmen T, Mitzi D B, and Cohen J D,
6931 Electronically active defects in the Cu2ZnSn(Se, S)4 alloys as revealed by
6932 transient photocapacitance spectroscopy, Appl. Phys. Lett. 2012;101:142106.

6933 [621] Contreras M A, Ramanathan K, AbuShama J, Hasoon F, Young D L, Egaas B,
6934 and Noufi R, Diode characteristics in state-of-the-art ZnO/CdS/Cu(In1-xGax)Se2
6935 solar cells, Prog. Photovolt: Res. Appl. 2005;13:209-216.

6936 [622] Kim J et al., High Efficiency Cu2ZnSn(S,Se)4 Solar Cells by Applying a Double
6937 In2S3/CdS Emitter, vol. 26, 7427-7431, Adv. Mat. 2014.

6938 [623] Stolle CJ, Harvey TB, Korgel BA. Nanocrystal photovoltaics: a review of recent
6939 progress. Current Opinion in Chemical Engineering 2013;2:160-7.

6940 [624] http://www.pv-magazine.com/news/details/beitrag/first-solar-raises-bar-for-cdte-with-
6941 215-efficiency-record_100018069/#axzz3zBrMPbaC

6942 [625] Birkmire RW, McCandless BE. CdTe thin film technology: Leading thin film PV
6943 into the future. Current Opinion in Solid State and Materials Science
6944 2010;14:139-42

6945 [626] Hsiao KJ. Energy-band barrier to improve open-circuit voltage of CdTe solar
6946 cells. Solar Energy Materials and Solar Cells 2014;120:647-53.

6947 [627] Kartopu G, Clayton AJ, Brooks WS, Hodgson SD, Barrioz V, Maertens A, et al.
6948 Effect of window layer composition in Cd1xZnxS/CdTe solar cells Progress in
6949 Photovoltaics: Research and Applications 2014;22:18-23

6950 [628] Dang H, Singh VP, Guduru S, Hastings JT. Embedded nanowire window layers
6951 for enhanced quantum efficiency in window-absorber type solar cells like
6952 CdS/CdTe. Solar Energy Materials and Solar Cells 2016;144:641-51.

6953 [629] Muruganantham G, Ravichandran K, Saravanakumar K, Ravichandran AT,
6954 Sakthivel B. Effect of solvent volume on the physical properties of undoped and
6955 fluorine doped tin oxide films deposited using a low-cost spray technique.
6956 Superlattices and Microstructures 2011;50:722-33.

6957 [630] Chauhan RN, Anand RS, Kumar J. Structural, electrical and optical properties of
6958 radio frequency sputtered indium tin oxide thin films modified by annealing in
6959 silicon oil and vacuum. Thin Solid Films 2014;556:253-9.

6960 [631] Aouaj MA, Diaz R, Belayachi A, Rueda F, Abd-Lefdil M. Comparative study of
6961 ITO and FTO thin films grown by spray pyrolysis. Materials Research Bulletin
6962 2009;44:1458-61.

6963 [632] Benramache S, Chabane F, Benhaoua B, Lemmadi FZ. Influence of growth time
6964 on crystalline structure, conductivity and optical properties of ZnO thin films.
6965 Journal of Semiconductors 2013;34:023001.

6966 [633] Mass J, Bhattacharya P, Katiyar RS. Effect of high substrate temperature on Al-
6967 doped ZnO thin films grown by pulsed laser deposition. Materials Science and
6968 Engineering: B 2003;103:9-15.
6969
6970 [634] Klein A, Körber C, Wachau A, Säuberlich F, Gassenbauer Y, Harvey SP et al.
6971 Transparent conducting oxides for photovoltaics: manipulation of Fermi level,
6972 work function and energy band alignment. Materials 2010;3:4892-914.

6973 [635] Liu TL, Jiang N, Wang DK, Luo DY, Yu LM, White R, et al. Formation of
6974 Metal-like Junction at Indium Tin Oxide/C60 Interface. Journal of The
6975 Electrochemical Society 2014;161:21-4.

6976 [636] Helander MG, Greiner MT, Wang ZB, Tang WM, Lu ZH. Work function of
6977 fluorine doped tin oxide. Journal of Vacuum Science and Technology A
6978 2011;29:011019.

6979 [637] Wang W, Feng Q, Jiang K, Huang J, Zhang X, Song W, et al. Dependence of
6980 aluminum-doped zinc oxide work function on surface cleaning method as studied
6981 by ultraviolet and X-ray photoelectron spectroscopies. Applied Surface Science
6982 2011;257:3884-7.

6983 [638] Calnan S, Tiwari AN. High mobility transparent conducting oxides for thin film
6984 solar cells. Thin Solid Films 2010;518:18349-9.

6985 [639] Hosroabadi S, Keshmiri SH. Design of high performance CdS/CdTe solar cells
6986 by optimization of step doping and thickness of the CdTe absorption layer.
6987 Electrical Engineering (ICEE) 2013;1-4.

6988 [640] Bu IYY. Sol–gel deposition of fluorine-doped tin oxide glasses for dye sensitized
6989 solar cells. Ceramics International 2014;40:417-22.

6990 [641] Panthani MG, Kurley JM, Crisp RW, Dietz TC, Ezzyat T. Luther J.M, et al. High
6991 Efficiency Solution Processed Sintered CdTe Nanocrystal Solar Cells: The Role
6992 of Interfaces. Nano letters 2014;14:670-5.

6993 [642] Luka G, Krajewski TA, Witkowski BS, Wisz G, Virt IS, Guziewicz E, et al.
6994 Aluminum-doped zinc oxide films grown by atomic layer deposition for
6995 transparent electrode applications. Journal of Materials Science: Materials in
6996 Electronics 2011;22:1810-5.

6997 [643] Han YX, Yang CL, Sun YT, Wang MS, Ma XG. The novel optical properties of
6998 CdS caused by concentration of impurity Co. Journal of Alloys and Compounds
6999 2014;585:503-9

7000 [644] Zhang H, Ma X, Ji Y, Xu J, Yang D. Single crystalline CdS nanorods fabricated
7001 by a novel hydrothermal method. Chemical physics letters 2003;377:654-7.

7002 [645] Liu G, Schulmeyer T, Brötz J, Klein A, Jaegermann W. Interface properties and
7003 band alignment of Cu 2 S/CdS thin film solar cells. Thin Solid Films
7004 2003;431:477-82.

7005 [646] Salavei A, Rimmaudo I, Piccinelli F, Romeo A. Influence of CdTe thickness on
7006 structural and electrical properties of CdTe/CdS solar cells. Thin Solid Films
7007 2013;535:257-60.

7008 [647] Brooks WSM, Irvine SJC, Taylor DM. Scanning Kelvin probe measurements on
7009 As-doped CdTe solar cells. Semiconductor Science and Technology
7010 2013;28:105024.

7011 [648] Brebrick RF. High Temperature Thermodynamic Data for CdTe (c). Journal of
7012 phase equilibria and diffusion 2010;31:260-9.

7013 [649] Major JD, Proskuryakov YY, Durose K. Impact of CdTe surface composition on
7014 doping and device performance in close Space sublimation deposited CdTe solar
7015 cells. Progress in Photovoltaics: Research and Applications 2011;21: 436-43.

7016 [650] Krishnakumar V, Barati A, Schimper HJ, Klein A, Jaegermann W. A possible
7017 way to reduce absorber layer thickness in thin film CdTe solar cells. Thin Solid
7018 Films 2013;535:233-6.

7019 [651] Luschitz J, Siepchen B, Schaffner J, Lakus-Wollny K, Haindl G, Klein A, et al.
7020 CdTe thin film solar cells: Interrelation of nucleation, structure, and performance.
7021 Thin Solid Films 2009;517:2125-31

7022 [652] Razykov TM, Ferekides CS, Morel D, Stefanakos E, Ullal HS, Upadhyaya HM.
7023 Solar photovoltaic electricity: Current status and future prospects. Solar Energy
7024 2011;85:1580-608.

7025 [653] Leite MS, Abashin M, Lezec HJ, Gianfrancesco AG, Talin AA, Zhitenev NB.
7026 Mapping the Local Photoelectronic Properties of Polycrystalline Solar Cells
7027 Through High Resolution Laser-Beam-Induced Current Microscopy. IEEE
7028 Journal of photovoltaics 2014;1:311-6

7029 [654] Kosyachenko LA, Mathew X, Roshko VY, Grushko EV. Optical absorptivity and
7030 recombination losses: The limitation simposed by the thickness of absorber layer
7031 in CdS/CdTe solar cells. Solar Energy Materials and Solar Cells 2013;114:179-
7032 85.

7033 [655] Novruzov VD, Fathi NM, Gorur O, Tomakin M, Bayramov AI, Schorr S, et al.
7034 CdTe thin film solar cells prepared by a low-temperature deposition method.
7035 Physica status solidi (a) 2010;207:730-3.

7036 [656] Schaffner J, Feldmeier E, Swirschuk A, Schimper HJ, Klein A, Jaegermann W.
7037 Influence of substrate temperature, growth rate and TCO substrate on the
7038 properties of CSS deposited CdS thin films. Thin Solid Films 2011;519:7556-9.

7039 [657] Williams BL, Taylor AA, Mendis BG, Phillips L, Bowen L, Major JD, et al.
7040 Core-shell ITO/ZnO/CdS/CdTe nanowire solar cells. Applied Physics Letters
7041 2014;104:053907.

7042 [658] Oliva-Avilés AI, Patino R, Oliva AI. CdS films deposited by chemical bath under
7043 rotation. Applied Surface Science 2010;256:6090-5.

7044 [659] Rubio S, Plaza JL, Diéguez E. Influence of CdS deposition technique for
7045 CdS/CdTe solar cells applications. Journal of Crystal Growth 2014;401:550-3.

7046 [660] Schumm B, Althues H, Kaskel S. CdTe nanoparticles for deposition of CdTe
7047 films using close spaced sublimation. Journal of Crystal Growth 2010;312:2449-
7048 53.

7049 [661] Saikia D, Godol PK, Saikia PK. Structural and optical properties of
7050 nanostructured CdS thin films deposited at different preparative conditions.
7051 Chalcogenide Letters 2010;7:317-24.

7052 [662] Schaffner J, Motzko M, Tueschen A, Swirschuk A, Schimper H. J, Klein A, et al.
7053 12% efficient CdTe/CdS thin film solar cells deposited by low temperature close
7054 space sublimation. Journal of Applied Physics 2011;110:064508.

7055 [663] Siepchen B, Drost C, Späth B, Krishnakumar V, Richter H, Harr M, Bossert S,
7056 Grimm M, Häfner K, Modes T,. Zywitzki O,. Morgner H. Thin film CdTe solar
7057 cells by close spaced sublimation: Recent results from pilot line. Thin Solid Films
7058 2013; 535: 224–228.

7059 [664] Plaza JL, Martínez O, Rubio S, Hortelano V, Diéguez E. Growth of CdS and
7060 CdTe films by close space vapour sublimation by using SiC resistive elements.
7061 Cryst.Eng.Comm 2013;15: 2314-18.

7062 [665] Rubio S, Shkir M, Plaza JL, Diéguez E. Sistema para la fabricación de multicapas
7063 para células solares y procedimiento para la fabricación de éstas. P201331206
7064 (Spanish Patent) (08/2013).

7065 [666] I. M. Dharmadasa, Review of the CdCl2 Treatment Used in CdS/CdTe Thin Film
7066 Solar Cell Development and New Evidence towards Improved Understanding,
7067 Coatings 2014, 4, 282-307; doi:10.3390/coatings4020282.

7068 [667] Kong L, Li J, Chen G, Zhu C, Liu W. A comparative study of thermal annealing
7069 effects under various atmospheres on nano-structured CdS thin films prepared by
7070 CBD. Journal of Alloys and Compounds 2013;573:112-7.

7071 [668] Boucher JW, Miller DW, Warren CW, Cohen JD, McCandless BE, Heath JT, et
7072 al. Optical response of deep defects as revealed by transient Photocapacitance and
7073 photocurrent spectroscopy in CdTe/CdS solar cells. Solar Energy Materials and
7074 Solar Cells 2014;129:57-63.

7075 [669] Paudel NR, Wieland KA, Young M, Asher S, Compaan AD. Stability of sub-
7076 micron-thick CdTe solar cells. Progress in Photovoltaics: Research and
7077 Applications 2014;22:107-14.

7078 [670] Gloeckler M, Sankin I, Zhao Z. CdTe solar cells at the threshold to 20%
7079 efficiency. Photovoltaics, IEEE Journal of. 2013;3(4):1389-93.

7080 [671] Williams BL, Major JD, Bowen L, Phillips L, Zoppi G, Forbes I, et al.
7081 Challenges and prospects for developing CdS/CdTe substrate solar cells on Mo
7082 foils. Solar Energy Materials and Solar Cells 2014;124:31–8.

7083 [672] Paudel NR, Young M, Roland PJ, Ellingson RJ, Yan Y, Compaan AD. Post-
7084 deposition processing options for high-efficiency sputtered CdS/CdTe solar cells.
7085 Journal of Applied Physics 2014;115:064502.

7086 [673] Li C, Poplawsky J, Wu Y, Lupini AR., Mouti A, Leonard DN, et al. From atomic
7087 structure to photovoltaic properties in CdTe solar cells. Ultramicroscopy
7088 2013;134:113-25.

7089 [674] Kephart JM, Geisthardt R, Sampath WS. Sputtered, Oxygenated CdS Window
7090 Layers for Higher Current in CdS/CdTe Thin Film Solar Cells. Photovoltaic
7091 Specialists Conference (PVSC) 2012;38:854-8.

7092 [675] Bensalah H, Hortelano V, Plaza JL, Martínez O, Crocco J, Zheng Q, et al.
7093 Characterization of CdZnTe after argon ion beam bombardment. Journal of
7094 Alloys and Compounds 2012;543:233-8.

7095 [676] Hiralal P, Unalan HE, Amaratunga GA. Nanowires for energy generation. 7096 Nanotechnology 2012;23:194002.

7097 [677] Chen L, Fu X, Lai J, Sun J, Ying Z, Wu J, et al. Growth of CdS Nanoneedles by 7098 Pulsed Laser Deposition. Journal of electronic materials 2012;41:1941-7.

7099 [678] Luo B, Deng Y, Wang Y, Tan M, Cao L. Independent growth of CdTe nanorod 7100 arrays on different substrates with enhanced photoelectrical property. Journal of 7101 Nanoparticle Research 2012;14:1-8.

7102 [679] Ling T, Wu M, Du X. Template synthesis and photovoltaic application of CdS 7103 nanotube arrays. Semiconductor Science and Technology 2012;27:055017.

7104 [680] Lugani L, Ercolani D, Sorba L, Sibirev NV, Timofeeva MA, Dubrovskii VG. 7105 Modeling of InAs–InSb nanowires grown by Au-assisted chemical beam epitaxy. 7106 Nanotechnology 2012;23:095602.

7107 [681] Rawal SB, Sung SD, Moon SY, Shin YJ, Lee WI. Optimization of CdS layer on 7108 ZnO nanorod arrays for efficient CdS/CdSe co-sensitized solar cell. Materials 7109 Letters 2012;82:240-3.

7110 [682] Park H, Chang S, Jean J, Cheng JJ, Araujo PT, Wang M, et al. Graphene 7111 cathode-based ZnO nanowire hybrid solar cells. Nano letters 2012;13:233-9.

7112 [683] Zhu YF, Fan DH, Zhou GH, Lin YB, Liu L. A suitable chemical conversion route 7113 to synthesize ZnO/CdS core/shell heterostructures for photovoltaic applications. 7114 Ceramics International 2014;40:3353-9.

7115 [684] Medvids A, Onufrijevs P, Dauksta E, Sobolev NA. Homo-and Hetero-Structure 7116 Formation in Semiconductors by Laser Radiation: First Stage of Quantum Cones 7117 Formation. Solid State Phenomena 2014;205:475-9.

7118 [685] Fan Z, Ruebusch DJ, Rathore AA, Kapadia R, Ergen O, Leu PW, et al. 7119 Challenges and prospects of nanopillar-based solar cells. Nano Research 7120 2009;2:829-843.

7121 [686] Lee SH, Zhang X, Parish CM, Lee HN, Smith DB, He Y, et al. Nanocone tip-film 7122 solar cells with efficient charge transport. Advanced Materials 2011;23: 4381-5

7123 [687] Tang J, Huo Z, Brittman S, Gao H, Yang P. Solution-processed core-shell 7124 nanowires for efficient photovoltaic cells. Nature nanotechnology 2011;6:568-72.

7125 [688] Mishra S, Nath M. Growth of vertically aligned CdTe nanorod arrays through 7126 patterned electrodeposition. Nano Energy 2013;2:1207-13.

7127 [689] MacDonald BI, Martucci A, Rubanov S, Watkins SE, Mulvaney P, Jasieniak JJ. 7128 Layer-by-Layer Assembly of Sintered CdSe x Te1–x Nanocrystal Solar Cells. 7129 ACS nano 2012;6:5995-6004.

7130 [690] Lin T, Huang F, Liang J, Wang Y. A facile preparation route for boron-doped
7131 graphene, and its CdTe solar cell application. Energy and Environmental Science
7132 2011;4(3):862-5.
7133
7134 [691] Cui Y, Lauhon LJ, Gudiksen MS, Wang J, Lieber CM. Diameter-controlled
7135 synthesis of single-crystal silicon nanowires. Appl Phys Lett 2001;78:2214.
7136
7137 [692] Cui Y, Duan X, Hu J, Lieber CM. Doping and Electrical Transport in Silicon
7138 Nanowires. J Phys Chem B 2000;104:5213–6.
7139
7140 [693] Peng K-Q, Yan Y-J, Gao S-P, Zhu J. Synthesis of Large-Area Silicon Nanowire
7141 Arrays via Self-Assembling Nanoelectrochemistry. Adv Mater 2002;14:1164.
7142
7143 [694] Kuang Y, Vece M Di, Rath JK, Dijk L Van, Schropp REI. Elongated
7144 nanostructures for radial junction solar cells. Rep Prog Phys 2013;76:106502.
7145
7146 [695] Wagner R, Ellis W. Vapor-Liquid-Solid Mechanism of Single Crystal Growth.
7147 Appl Phys Lett 1964;4:89–90.
7148
7149 [696] Schmidt V, Senz S, Gösele U. Diameter dependence of the growth velocity of
7150 silicon nanowires synthesized via the vapor-liquid-solid mechanism. Phys Rev B
7151 2007;75:1–6.
7152
7153 [697] Sunkara MK, Sharma S, Miranda R, Lian G, Dickey EC. Bulk synthesis of
7154 silicon nanowires using a low-temperature vapor–liquid–solid method. Appl Phys
7155 Lett 2001;79:1546.
7156
7157 [698] Wang Y, Schmidt V, Senz S, Gösele U. Epitaxial growth of silicon nanowires
7158 using an aluminium catalyst. Nat Nanotechnol 2006;1:186–9.
7159 [699] Eisenhawer B, Zhang D, Clavel R, Berger A, Michler J, Christiansen S. Growth
7160 of doped silicon nanowires by pulsed laser deposition and their analysis by
7161 electron beam induced current imaging. Nanotechnology 2011;22:075706.
7162
7163 [700] Allen JE, Hemesath ER, Perea DE, Lensch-Falk JL, Li ZY, Yin F, et al. High-
7164 resolution detection of Au catalyst atoms in Si nanowires. Nat Nanotechnol
7165 2008;3:168–73.
7166
7167 [701] Hochbaum AI, Fan R, He R, Yang P. Controlled growth of Si nanowire arrays for
7168 device integration. Nano Lett 2005;5:457–60.
7169
7170 [702] Gudiksen MS, Lauhon LJ, Wang J, Smith DC, Lieber CM. Growth of nanowire
7171 superlattice structures for nanoscale photonics and electronics. Nature
7172 2002;415:617–20.
7173

7174 [703] Stelzner T, Pietsch M, Andrä G, Falk F, Ose E, Christiansen S. Silicon nanowire-
7175 based solar cells. Nanotechnology 2008;19:295203.
7176
7177 [704] Morton KJ, Nieberg G, Bai S, Chou SY. Wafer-scale patterning of sub-40 nm
7178 diameter and high aspect ratio (>50:1) silicon pillar arrays by nanoimprint and
7179 etching. Nanotechnology 2008;19:345301.
7180
7181 [705] Hsu C-M, Connor ST, Tang MX, Cui Y. Wafer-scale silicon nanopillars and
7182 nanocones by Langmuir–Blodgett assembly and etching. Appl Phys Lett
7183 2008;93:133109.
7184
7185 [706] Peng KQ, Hu JJ, Yan YJ, Wu Y, Fang H, Xu Y, et al. Fabrication of Single-
7186 Crystalline Silicon Nanowires by Scratching a Silicon Surface with Catalytic
7187 Metal Particles. Adv Funct Mater 2006;16:387–94.
7188
7189 [707] Peng K, Lu A, Zhang R, Lee S-T. Motility of Metal Nanoparticles in Silicon and
7190 Induced Anisotropic Silicon Etching. Adv Funct Mater 2008;18:3026–35.
7191
7192 [708] Sivakov V, Brönstrup G, Pecz B, Berger A, Radnoczi GZ, Krause M, et al.
7193 Realization of Vertical and Zigzag Single Crystalline Silicon Nanowire
7194 Architectures. J Phys Chem C 2010;114:3798–803.
7195
7196 [709] Sivakov V, Andrä G, Gawlik A, Berger A, Plentz J, Falk F, et al. Silicon
7197 nanowire-based solar cells on glass: synthesis, optical properties, and cell
7198 parameters. Nano Lett 2009;9:1549–54.
7199
7200 [710] Hoffmann B, Sivakov V, Schmitt SW, Bashouti MY, Latzel M, Dluhoš J, et al.
7201 Wet – Chemically Etched Silicon Nanowire Solar Cells : Fabrication and
7202 Advanced Characterization. In: Peng X, editor. Nanowires: Recent Advances,
7203 InTech; 2012, p. 211-230.
7204
7205 [711] Jansen H, Boer MD, Legtenberg R, Elwenspoek M. The black silicon method: a
7206 universal method for determining the parameter setting of a fluorine-based
7207 reactive ion etcher in deep silicon trench etching with profile control. J
7208 Micromechanics Microengineering 1995;5:115–20.
7209
7210 [712] Yoo JS, Parm IO, Gangopadhyay U, Kim K, Dhungel SK, Mangalaraj D, et al.
7211 Black silicon layer formation for application in solar cells. Sol Energy Mater Sol
7212 Cells 2006;90:3085–93.
7213
7214 [713] Füchsel K, Kroll M, Käsebier T, Otto M, Pertsch T, Kley E-B, et al. Black silicon
7215 photovoltaics. In: Wehrspohn R, Gombert A, editors. Photonics for Solar Energy
7216 Systems IV, Proc. of SPIE Vol. 8438, 84380M-1-84380M–8 doi:
7217 10.1117/12.923748

7218
7219 [714] Halbwax M, Sarnet T, Delaporte P, Sentis M, Etienne H, Torregrosa F, et al.
7220 Micro and nano-structuration of silicon by femtosecond laser: Application to
7221 silicon photovoltaic cells fabrication. Thin Solid Films 2008;516:6791–5.
7222
7223 [715] Garnett E, Yang P. Light trapping in silicon nanowire solar cells. Nano Lett
7224 2010;10:1082–7.
7225
7226 [716] Schmitt SW, Schechtel F, Amkreutz D, Bashouti M, Srivastava SK, Hoffmann B,
7227 et al. Nanowire arrays in multicrystalline silicon thin films on glass: a promising
7228 material for research and applications in nanotechnology. Nano Lett
7229 2012;12:4050–4.
7230
7231 [717] Kempa TJ, Tian B, Kim DR, Hu J, Zheng X, Lieber CM. Single and tandem axial
7232 p-i-n nanowire photovoltaic devices. Nano Lett 2008;8:3456–60.
7233
7234 [718] Tian B, Zheng X, Kempa TJ, Fang Y, Yu N, Yu G, et al. Coaxial silicon
7235 nanowires as solar cells and nanoelectronic power sources. Nature 2007;449:885–
7236 9.
7237
7238 [719] Peng KQ, Huang ZP, Zhu J. Fabrication of Large-Area Silicon Nanowire p–n
7239 Junction Diode Arrays. Adv Mater 2004;16:73–6.
7240
7241 [720] Kayes BM, Atwater HA, Lewis NS. Comparison of the device physics principles
7242 of planar and radial p-n junction nanorod solar cells. J Appl Phys
7243 2005;97:114302.
7244 [721] Cho J, O'Donnell B, Yu L, Kim K, Ngo I, Cabarrocas PRi. Sn-catalyzed silicon
7245 nanowire solar cells with 4.9% efficiency grown on glass. Prog Photovoltaics Res
7246 Appl 2013;21:77–81.
7247
7248 [722] Misra S, Yu L, Foldyna M, Cabarrocas PRi. High efficiency and stable
7249 hydrogenated amorphous silicon radial junction solar cells built on VLS-grown
7250 silicon nanowires. Sol Energy Mater Sol Cells 2013;118:90–5.
7251
7252 [723] Oh J, Yuan H-C, Branz HM. An 18.2%-efficient black-silicon solar cell achieved
7253 through control of carrier recombination in nanostructures. Nat Nanotechnol
7254 2012:1–6.
7255
7256 [724] Jeong S, McGehee MD, Cui Y. All-back-contact ultra-thin silicon nanocone solar
7257 cells with 13.7% power conversion efficiency. Nat Commun 2013;4:2950.
7258
7259 [725] Brönstrup G, Garwe F, Csáki A, Fritzsche W, Steinbrück A, Christiansen S.
7260 Statistical model on the optical properties of silicon nanowire mats. Phys Rev B
7261 2011;84:1–10.

7262
7263 [726] Bashouti MY, Pietsch M, Brönstrup G, Sivakov V, Ristein J, Christiansen S. Heterojunction based hybrid silicon nanowire solar cell: surface termination, photoelectron and photoemission spectroscopy study. Prog Photovoltaics Res Appl 2013;22,1050-61.
7264
7265
7266
7267
7268 [727] Jeong S, Garnett EC, Wang S, Yu Z, Fan S, Brongersma ML, et al. Hybrid silicon nanocone-polymer solar cells. Nano Lett 2012;12:2971–6.
7269
7270
7271 [728] Wei W, Tsai M-L, Ho S-T, Tai S, Ho C-R, Tsai S-H, et al. Above-11%-efficiency organic-inorganic hybrid solar cells with omnidirectional harvesting characteristics by employing hierarchical photon-trapping structures. Nano Lett 2013;13:3658–63.
7272
7273
7274
7275
7276 [729] Fan G, Zhu H, Wang K, Wei J, Li X, Shu Q, et al. Graphene-silicon nanowire Schottky junction for enhanced light harvesting. ACS Appl Mater Interfaces 2011;3:721–5.
7277
7278
7279
7280 [730] Wu Y, Zhang X, Jie J, Xie C, Zhang X, Sun B, et al. Graphene Transparent Conductive Electrodes for Highly Efficient Silicon Nanostructures-Based Hybrid Heterojunction Solar Cells. J Phys Chem C 2013;117:11968–76.
7281
7282
7283
7284 [731] Peng K-Q, Lee S-T. Silicon nanowires for photovoltaic solar energy conversion. Adv Mater 2011;23:198–215.
7285
7286
7287 [732] Garnett EC, Brongersma ML, Cui Y, McGehee MD. Nanowire Solar Cells. Annu Rev Mater Res 2011;41:269–95.
7288
7289
7290 [733] Huang MH, Mao S, Feick H, Yan H, Wu Y, Kind H et al. Room-temperature ultraviolet nanowire nanolasers. Science 2001;292:1897-9.
7291
7292
7293 [734] Yang P, Yan H, Mao S, Russo R, Johnson J, Saykally R, et al. Controlled growth of ZnO nanowires and their optical properties. Adv Funct Mater;2002:323–31.
7294
7295
7296 [735] Ng HT, Han J, Yamada T, Nguyen P, Chen YP, Meyyappan M. Single crystal nanowire vertical surround-gate field-effect transistor. Nano Lett 2004;4:1247-52.
7297
7298
7299 [736] Kim HM, Cho YH, Lee H, Kim SI, Ryu SR, Kim DY et al. High-brightness light emitting diodes using dislocation-free indium gallium nitride/gallium nitride multiquantum-well nanorod arrays. Nano Lett 2004;4:1059-62.
7300
7301
7302
7303 [737] Wang X, Summers CJ, Wang ZL. Large-scale hexagonal-patterned growth of aligned ZnO nanorods for nano-optoelectronics and nanosensor arrays. Nano Lett 2004;4:423-6.
7304
7305

7306
7307 [738] Wan Q, Feng P, Wang T.H. Vertically aligned tin-doped indium oxide nanowire
7308 arrays: Epitaxial growth and electron field emission properties. Appl Phys Lett
7309 2006;89:123102.
7310
7311 [739] Tang YB, Cong HT, Wang ZM, Cheng HM. Catalyst-seeded synthesis and field
7312 emission properties of flowerlike Si-doped AlN nanoneedle array. Appl Phys Lett
7313 2006;89:253112.
7314
7315 [740] Martinson ABF, Elam JW, Hupp JT, Pellin MJ. ZnO Nanotube based dye-
7316 sensitized solar cells. Nano Lett 2007;7:2183-7.
7317
7318 [741] C. Y. Jiang CY, Sun HW, Lo GQ, Kwong DL, Wang JX. Improved dye-
7319 sensitized solar cells with a ZnO-nanoflower photoanode. Appl Phys Lett
7320 2007;90:263501.
7321
7322 [742] Lee YJ, Ruby DS, Peters DW, McKenzie BB, Hsu JWP. ZnO nanostructures as
7323 efficient antireflection layers in solar Cells, Nano Lett 2008;8:1501-5.
7324
7325 [743] Hu L, Chen G. Analysis of optical absorption in silicon nanowire arrays for
7326 photovoltaic applications. Nano Lett 2007;7:3249-52.
7327
7328 [744] Glas F. Critical dimensions for the plastic relaxation of strained axial
7329 heterostructures in free-standing nanowires. Phys Rev B 2006;74:121302R.
7330 [745] Seifert W, Borgström M, Deppert K, Dick KA, Johansson J, Larsson MW.
7331 Growth of one-dimensional nanostructures in MOVPE. J Cryst Growth
7332 2004;272:211-20.
7333
7334 [746] Persson AI, Larsson MW, Stengström S, Ohlsson BJ, Samuelson L, Wallenberg
7335 LR. Solid-phase diffusion mechanism for GaAs nanowire growth Nature Mater
7336 2004;3:677-81.
7337
7338 [747] Thelander C, Nilsson HA, Jensen LE, Samuelson L. Nanowire single-electron
7339 memory. Nano Lett 2005;5:635-8.
7340
7341 [748] Dubrovskii VG, Soshnikov IP, Sibirev NV, Cirlin GE, Ustinov VM. Growth of
7342 GaAs nanoscale whiskers by magnetron sputtering deposition. J Cryst Growth
7343 2006;289:31-6.
7344
7345 [749] Noborisaka J, Motohisa J, Fukui T. Catalyst-free growth of GaAs nanowires by
7346 selective-area metalorganic vapor-phase epitaxy. Appl Phys Lett
7347 2005;86:213102.
7348

7349 [750] Mohan P, Motohisa J, Fukui T. Controlled growth of highly uniform, axial/radial
7350 direction-defined, individually addressable InP nanowire arrays. Nanotechnology
7351 2005;16:2903-7.
7352
7353 [751] Harmand JC, Patriarche G, Péré-Laperne N, Mérat-Combes MN, Travers L, Glas
7354 F. Analysis of vapor-liquid-solid mechanism in Au-assisted GaAs nanowire
7355 growth. Appl Phys Lett 2005;87:203101.
7356
7357 [752] Harmand JC, Tchernycheva M, Patriarche G, Travers L, Glas F, Cirlin G. GaAs
7358 nanowires formed by Au-assisted molecular beam epitaxy: Effect of growth
7359 temperature. J Crys. Growth 2007;853:301-2.
7360
7361 [753] Plante MC, LaPierre RR. Growth mechanisms of GaAs nanowires by gas source
7362 molecular beam epitaxy. J Cryst Growth 2006;286:394-9.
7363
7364 [754] Colombo C, Spirkoska D, Frimmer M, Abstreiter G, Fontcuberta i Morral A. Ga-
7365 assisted catalyst-free growth mechanism of GaAs nanowires by molecular beam
7366 epitaxy. Phys Rev B 2008;77:155326.
7367
7368 [755] Dubrovskii VG, Soshnikov IP, Cirlin GE, Tonkikh AA, Samsonenko YuB,
7369 Sibirev NV et al. On the non-monotonic lateral size dependence of the height of
7370 GaAs nanowhiskers grown by molecular beam epitaxy at high temperature. Phys
7371 Stat Sol (b) 2004;241:R30-3.
7372
7373 [756] Wu ZH, Sun M, Mei XY, Ruda HE. Growth and photoluminescence
7374 characteristics of AlGaAs nanowires. Appl Phys Lett 2004;85:657-9.
7375
7376 [757] Dubrovskii VG, Cirlin GE, Soshnikov IP, Tonkikh AA, Sibirev NV, Samsonenko
7377 YuB et al. Diffusion-induced growth of GaAs nanowhiskers during molecular
7378 beam epitaxy: Theory and experiment. Phys Rev B 2005;71:205325.
7379
7380 [758] Cirlin GE, Dubrovskii VG, Sibirev NV, Soshnikov IP, Samsonenko YuB,
7381 Tonkikh AA et al. The diffusion mechanism in the formation of GaAs and
7382 AlGaAs nanowhiskers during the process of molecular-beam epitaxy.
7383 Semiconductors 2005;39:557-64.
7384
7385 [759] Samsonenko YuB, Cirlin GE, Egorov VA, Polyakov NK, Ulin VP, Dubrovskii
7386 VG. Specific features of formation of GaAs nanowire crystals during molecular
7387 beam epitaxy on different silicon surfaces. Semiconductors 2008;42:1445-9.
7388
7389 [760] Czaban JA, Thompson DA, LaPierre RR. GaAs Core−Shell Nanowires for
7390 Photovoltaic Applications. Nano Lett 2009;9:148-54.
7391

7392 [761] Cirlin GE, Bouravleuv AD, Soshnikov IP, Samsonenko YuB, Dubrovskii VG,
7393 Arakcheeva EM et al. Photovoltaic properties of p-doped GaAs nanowire arrays
7394 grown on n-type GaAs(111)B substrate. Nanoscale Res Lett 2010;5:360-3.
7395
7396 [762] Bi H, LaPierre RR. A GaAs nanowire/P3HT hybrid photovoltaic device.
7397 Nanotechnology 2009;20:465205.
7398
7399 [763] Mariani G, Laghumavarapu RB, Tremolet de Villers B, Shapiro J, Senanayake P
7400 et al. Hybrid conjugated polymer solar cells using patterned GaAs nanopillars.
7401 Appl Phys Lett 2010;97:013107.
7402
7403 [764] Tajik N, Peng Z, Kuyanov P, LaPierre RR. Sulfur passivation and contact
7404 methods for GaAs nanowire solar cells. Nanotechnology 2011;22:225402.
7405
7406 [765] Bar-Sadan M, Barthel J, Shtrikman H, Houben L. Direct Imaging of Single Au
7407 Atoms Within GaAs Nanowires. Nano Lett 2012;12: 2352-6.
7408
7409 [766] Fontcuberta i Morral A, Colombo C, Abstreiter G, Arbiol J, Morante JR.
7410 Nucleation mechanism of gallium-assisted molecular beam epitaxy growth of
7411 gallium arsenide nanowires. Appl Phys Lett 2008;92:063112.
7412
7413 [767] Cirlin GE, Dubrovskii VG, Samsonenko YuB, Bouravleuv AD, Durose K,
7414 Proskuryakov YY et al. Self-catalyzed, pure zincblende GaAs nanowires grown
7415 on Si(111) by molecular beam epitaxy. Phys Rev B 2010;82:035302.
7416
7417 [768] Mandl B, Stangl J, Hilner e, Zakharov AA, Hillerich K, Dey AW et al. Growth
7418 Mechanism of Self-Catalyzed Group III−V Nanowires. Nano Lett 2010;10:4443-
7419 9.
7420
7421 [769] Fontcuberta i Morral A. Gold-Free GaAs nanowire synthesis and optical
7422 properties. IEEE J Sel Top Quantum Electron 2011;17:819-28.
7423
7424 [770] Plissard S, Larrieu G, Wallart X, Caroff P. High yield of self-catalyzed GaAs
7425 nanowire arrays grown on silicon via gallium droplet positioning.
7426 Nanotechnology 2011;22:275602.
7427
7428 [771] Colombo C, Heiss M, Grätzel M, Fontcuberta i Morral A. Gallium arsenide pin
7429 radial structures for photovoltaic applications. Appl Phys Lett 2009;94:173108.
7430
7431 [772] Heigoldt M, .Arbiol J, Spirkoska D, Rebled JM, Conesa-Boj S, Abstreiter G and
7432 et al. Long range epitaxial growth of prismatic heterostructures on the facets of
7433 catalyst-free GaAs nanowires. J Mater Chem 2009;19:840-8.
7434

7435 [773] Gardner NR, Woods NJ, Domnguez PS, Tok ES, Norman CE, Harris JJ.
7436 Electrical properties of lateral p - n junctions formed on patterned (110) GaAs
7437 substrates. Semicond Sci Technol 1997;12:737-41.
7438
7439 [774] Krogstrup P, Jørgensen HI, Heiss M, Demichel O, Holm JV, Aagesen M et al.
7440 Single-nanowire solar cells beyond the Shockley-Queisser limit. Nature Photon
7441 2013;7:306-10.
7442
7443 [775] Heurlin M, Wickert P, Falt S, Borgstrom MT, Deppert K, Samuelson L et al.
7444 Axial InP nanowire tandem junction grown on a silicon substrate. Nano Lett
7445 2011;11:2028-31.
7446
7447 [776] Shin JC, Kim KH, Yu KJ, Hu H, Yin L, Rogers JA et al. $In_x Ga_{1-x}$ As nanowires
7448 on silicon: one-dimensional heterogeneous epitaxy, bandgap engineering, and
7449 photovoltaics. Nano Lett 2011;11:4831-8.
7450
7451 [777] Gutsche C, Lysov A, Braam D, Regolin I, Keller G, Geller M et al. n-
7452 GaAs/InGaP/p-GaAs core-multishell nanowire diodes for efficient light-to-
7453 current conversion. Adv Funct Mater 2012;22:929-36.
7454
7455 [778] Tchernycheva M, Rigutti L, Jacopin G, de Luna Bugallo A, Lavenus P,. Julien
7456 FH et al. Photovoltaic properties of GaAsP core–shell nanowires on Si(001)
7457 substrate. Nanotechnology 2012;23:265402.
7458
7459 [779] Holm JV, Jørgensen HI, Krogstrup P, Nygård J, Liu H, Aagesen M. Surface-
7460 passivated GaAsP single-nanowire solar cells exceeding 10% efficiency grown
7461 on silicon. Nature Commun 2013;4:1498-502.
7462
7463 [780] LaPierre RR, Chia ACE, Gibson SJ, Haapamaki CM, Boulanger J, Yee R et al.
7464 III–V nanowire photovoltaics: Review of design for high efficiency. Phys Stat Sol
7465 RRL 2013;7:815-830.
7466
7467 [781] Wallentin J, Anttu N, Asoli D, Huffman M, Aberg I, Magnusson MH et al. InP
7468 nanowire array solar cells achieving 13.8% efficiency by exceeding the ray optics
7469 limit. Science 2013;339:1057-60.
7470
7471 [782] Tchernycheva M, Cirlin GE, Patriarche G, Travers L, Zwiller V, Perinetti U et al.
7472 Growth and Characterization of InP Nanowires with InAsP Insertions. Nano Lett
7473 2007;7:1500-4.
7474
7475 [783] Kats VN, Kochereshko VP, Platonov AV, Chizhova TV, Cirlin GE, Bouravleuv
7476 AD et al. Optical study of GaAs quantum dots embedded into AlGaAs nanowires.
7477 Semicond Sci Technol 2012;7:015009.
7478

7479 [784] LaPierre RR. Numerical model of current-voltage characteristics and efficiency
7480 of GaAs nanowire solar cells. J Appl Phys 2011;109:034311.
7481
7482 [785] Wen L, Zhao Z, Li X, Shen Y, Guo H, Wang Y. Theoretical analysis and
7483 modeling of light trapping in high efficicency GaAs nanowire array solar cells.
7484 Appl Phys Lett 2011:99:143116.
7485
7486 [786] Cirlin GE, Dubrovskii VG, Soshnikov IP, Sibirev NV, Samsonenko YuB,
7487 Bouravleuv AD and et al. Critical diameters and temperature domains for MBE
7488 growth of III–V nanowires on lattice mismatched substrates. Phys Status Solidi
7489 RRL 2012;3:112-4.
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